

## E0C623A

### 4-bit Single Chip Microcomputer



- Core CPU Architecture
- SVD Circuit
- Super Low Operating Voltage (0.9V)
- High Quality Display LCD Driver

#### DESCRIPTION

The E0C623A is an advanced single-chip CMOS 4-bit microcomputer consisting of the E0C6200A CMOS 4-bit core CPU. It also contains the ROM, RAM, LCD driver circuit, time base counter and stopwatch counter. The E0C623A provides an excellent solution for low-power consumption systems with clock functions.

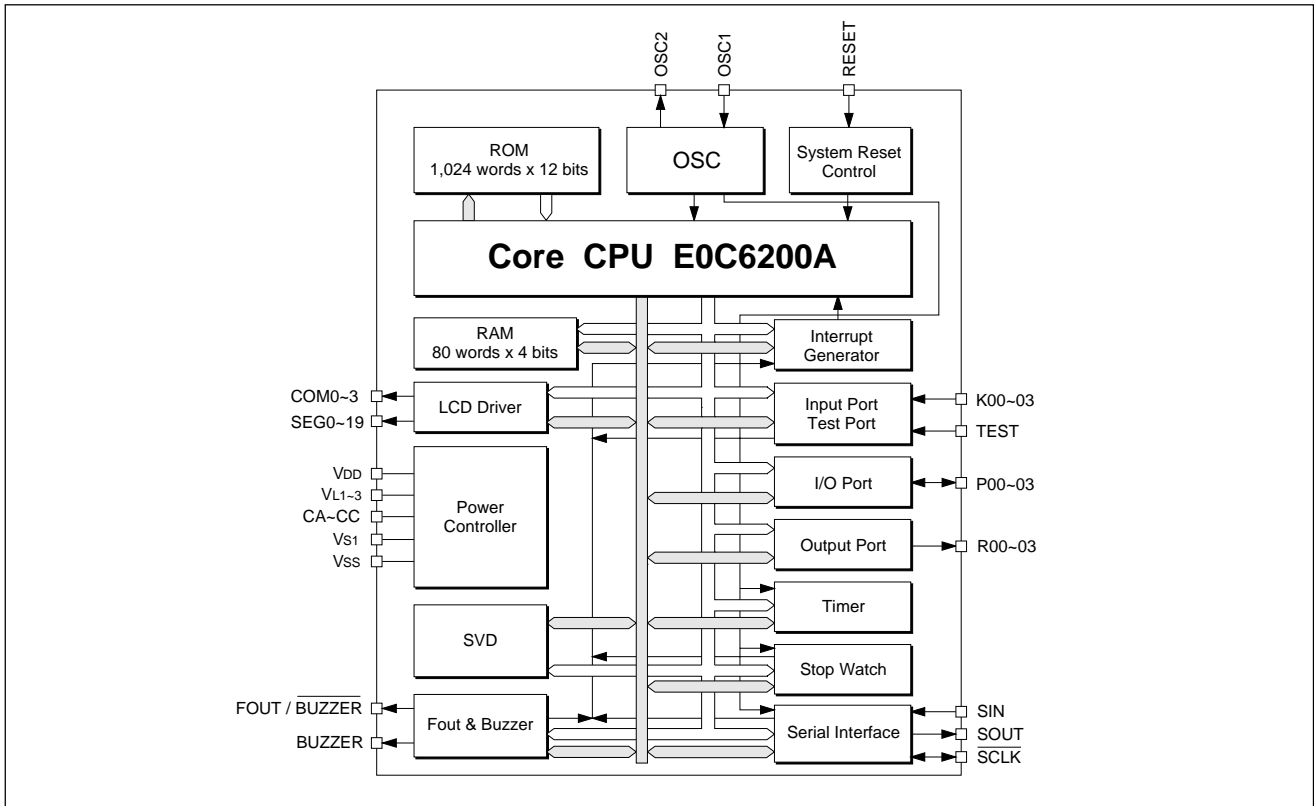
#### FEATURES

- CMOS LSI ..... 4-bit parallel processing
- Clock ..... 32.768kHz (Typ.)
- Instruction set ..... 100 instructions
- Instruction cycle time ..... 153μsec, 214μsec or 366μsec (depending on instruction)
- ROM capacity .....  $1,024 \times 12$  bits
- RAM capacity .....  $80 \times 4$  bits
- Input port ..... 4 bits  
(pull-down resistors are available by mask option)
- Output port ..... 4 bits
- Serial I/F ..... 8 bits (clock sync.)
- I/O port ..... 4 bits
- LCD driver ..... 20 segments  $\times$  3 commons, 1/3 duty or 4 commons, 1/4 duty  
(constant voltage power supply is built in)
- Built-in supply voltage detection (SVD) circuit
- Interrupts ..... Externa : Input interrupt                      1 line  
Internal : Timer interrupt                                  2 lines  
Serial interface interrupt                                  1 line
- Supply voltage ..... 1.5V/3.0V (Minimum operating voltage: 0.9V/1.8V)
- Current consumption ..... HALT mode                      : 1.0μA/1.0μA (Typ.)  
OPERATING mode : 2.5μA/2.5μA (Typ.)
- Package ..... QFP12-48pin (plastic), QFP6-60pin (plastic)  
Die form

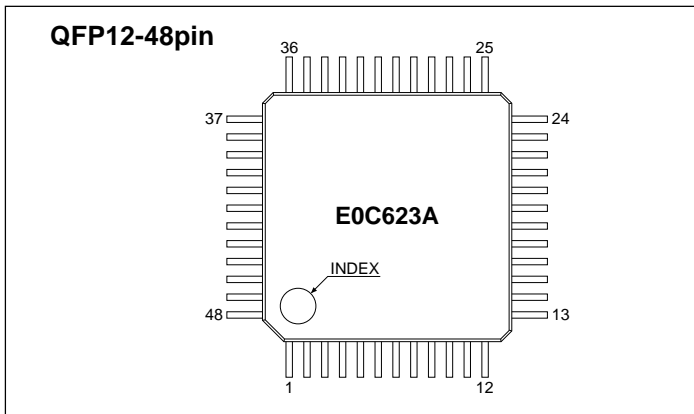
#### LINE UP

Model	Supply voltage	Clock
E0C62L3A	1.5V (0.9V to 2.0V)	32kHz (Crystal or CR oscillation)
E0C623A	3.0V (1.8V to 3.5V)	32kHz (Crystal or CR oscillation)

■ BLOCK DIAGRAM

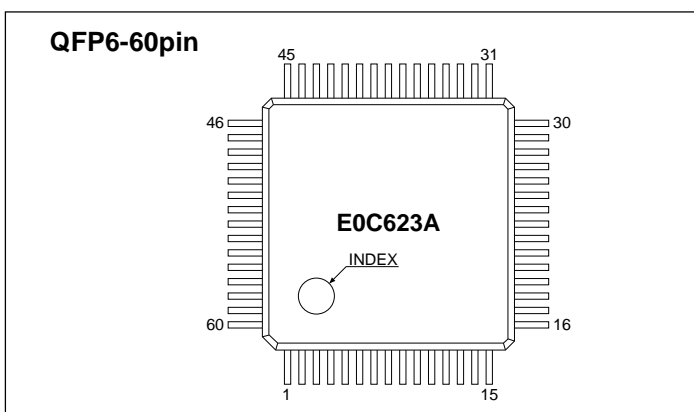


■ PIN CONFIGURATION



No.	Pin name	No.	Pin name	No.	Pin name	No.	Pin name
1	COM2	13	SEG12	25	P00	37	VDD
2	COM3	14	SEG13	26	N.C.	38	OSC1
3	SEG0	15	SEG14	27	RESET	39	OSC2
4	SEG1	16	SEG15	28	K00	40	Vs1
5	SEG2	17	SEG16	29	K01	41	CA
6	SEG3	18	SEG17	30	K02	42	CB
7	SEG4	19	SEG18	31	K03	43	CC
8	SEG6	20	SEG19	32	R00	44	VL1
9	SEG8	21	TEST	33	R01	45	VL2
10	SEG9	22	P03	34	R02	46	VL3
11	SEG10	23	P02	35	R03	47	COM0
12	SEG11	24	P01	36	VSS	48	COM1

N.C. = No Connection



No.	Pin name	No.	Pin name	No.	Pin name	No.	Pin name
1	P00	16	OSC1	31	COM3	46	SEG13
2	N.C.	17	OSC2	32	N.C.	47	SEG14
3	RESET	18	Vs1	33	SEG0	48	SEG15
4	K00	19	N.C.	34	SEG1	49	SEG16
5	K01	20	N.C.	35	SEG2	50	SEG17
6	K02	21	CA	36	SEG3	51	SEG18
7	K03	22	CB	37	SEG4	52	SEG19
8	R00	23	CC	38	SEG5	53	TEST
9	R01	24	N.C.	39	SEG6	54	N.C.
10	R02	25	VL1	40	SEG7	55	N.C.
11	R03	26	VL2	41	SEG8	56	N.C.
12	N.C.	27	VL3	42	SEG9	57	N.C.
13	N.C.	28	COM0	43	SEG10	58	P03
14	VSS	29	COM1	44	SEG11	59	P02
15	VDD	30	COM2	45	SEG12	60	P01

N.C. = No Connection

■ PIN DESCRIPTION

Pin name	Pin No.		In/Out	Function
	QFP12-48pin	QFP6-60pin		
VDD	37	15	I	Power source (+) terminal
VSS	36	14	I	Power source (-) terminal
Vs1	40	18	O	Oscillation and internal logic system regulated voltage output terminal
VL1	44	25	O	LCD system regulated voltage output terminal (approx. -1.05 V)
VL2	45	26	O	LCD system booster output terminal (VL1 x 2)
VL3	46	27	O	LCD system booster output terminal (VL1 x 3)
CA-CC	41-43	21-23	-	Booster capacitor connecting terminal
OSC1	38	16	I	Crystal or CR oscillation input terminal
OSC2	39	17	O	Crystal or CR oscillation output terminal
K00-K03	28-31	4-7	I	Input terminal
P00-P03	25-22	1, 60-58	I/O	I/O terminal
R00-R03	32-35	8-11	O	Output terminal
SEG0-4	3-7	33-37	O	LCD segment output terminal (Convertible to DC output by mask option)
SEG5	-	38		
SEG6	8	39		
SEG7	-	40		
SEG8-19	9-20	41-52		
COM0-3	47, 48, 1, 2	28-31	O	LCD common output terminal
RESET	27	3	I	Initial reset input terminal
TEST	21	53	I	Test input terminal

■ ELECTRICAL CHARACTERISTICS

● Absolute Maximum Ratings

(VDD=0V)

Rating	Symbol	Value	Unit
Supply voltage	Vss	-5.0 to 0.5	V
Input voltage (1)	Vi	Vss - 0.3 to 0.5	V
Input voltage (2)	Viosc	Vss - 0.3 to 0.5	V
Operating temperature	Topr	-20 to 70	°C
Storage temperature	Tstg	-65 to 150	°C
Soldering temperature / Time	Tsol	260°C, 10sec (lead section)	-
Permissible dissipation *1	Pd	250	mW

\*1: In case of plastic package (QFP12-48pin).

● Recommended Operating Conditions

E0C623A

(Ta=-20 to 70°C)

Condition	Symbol	Remark	Min.	Typ.	Max.	Unit
Supply voltage	Vss	VDD=0V	-3.5	-3.0	-1.8	V
Oscillation frequency	fosc1	Crystal oscillation		32.768		kHz
	fosc2	CR oscillation, R=420kΩ		65	80	kHz
Booster capacitor (1)	C1		0.1			μF
Booster capacitor (2)	C2		0.1			μF
Capacitor between VDD and VL1	C3		0.1			μF
Capacitor between VDD and VL2	C4		0.1			μF
Capacitor between VDD and VL3	C5		0.1			μF
Capacitor between VDD and Vs1	C6		0.1			μF

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(Ta=-20 to 70°C)

Condition	Symbol	Remark	Min.	Typ.	Max.	Unit
Supply voltage	Vss	VDD=0V *3	-2.0	-1.5	-1.1	V
		VDD=0V, With software control *1	-2.0	-1.5	-0.9 *2	V
Oscillation frequency	fosc1	Crystal oscillation		32.768		kHz
	fosc2	CR oscillation, R=420kΩ		65	80	kHz
Booster capacitor (1)	C1		0.1			μF
Booster capacitor (2)	C2		0.1			μF
Capacitor between VDD and VL1	C3		0.1			μF
Capacitor between VDD and VL2	C4		0.1			μF
Capacitor between VDD and VL3	C5		0.1			μF
Capacitor between VDD and Vs1	C6		0.1			μF

\*1: When the heavy load protection mode is set by software and the SVD circuit is turned off.

\*2: The voltage which can be displayed on the LCD panel will differ according to the characteristics of the LCD panel.

\*3: When there is no software control during CR oscillation or crystal oscillation.

● DC Characteristics

E0C623A

(Unless otherwise specified: VDD=0V, VSS=-3.0V, fosc=32.768kHz, Ta=25°C, VS1/VL1-VL3 are internal voltage, C1-C6=0.1μF)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
High level input voltage (1)	V <sub>IH1</sub>		K00-K03, P00-P03	0.2•V <sub>SS</sub>	0	V
High level input voltage (2)	V <sub>IH2</sub>		RESET, TEST	0.15•V <sub>SS</sub>	0	V
Low level input voltage (1)	V <sub>IL1</sub>		K00-K03, P00-P03	V <sub>SS</sub>	0.8•V <sub>SS</sub>	V
Low level input voltage (2)	V <sub>IL2</sub>		RESET, TEST	V <sub>SS</sub>	0.85•V <sub>SS</sub>	V
High level input current (1)	I <sub>IH1</sub>	V <sub>IH1</sub> =0V, No pull down resistor	K00-K03, P00-P03	0	0.5	μA
High level input current (2)	I <sub>IH2</sub>	V <sub>IH2</sub> =0V, With pull down resistor	K00-K03	5	16	μA
High level input current (3)	I <sub>IH3</sub>	V <sub>IH3</sub> =0V, With pull down resistor	P00-P03	30	100	μA
Low level input current	I <sub>IL</sub>	V <sub>IL</sub> =V <sub>SS</sub>	K00-K03, P00-P03 RESET, TEST	-0.5	0	μA
High level output current (1)	I <sub>OH1</sub>	V <sub>OH1</sub> =0.1•V <sub>SS</sub>	R02, R03, P00-P03		-1.0	mA
High level output current (2)	I <sub>OH2</sub>	V <sub>OH2</sub> =0.1•V <sub>SS</sub> (built-in protection resistance)	R00, R01		-1.0	mA
Low level output current (1)	I <sub>OL1</sub>	V <sub>OL1</sub> =0.9•V <sub>SS</sub>	R02, R03, P00-P03	3.0		mA
Low level output current (2)	I <sub>OL2</sub>	V <sub>OL2</sub> =0.9•V <sub>SS</sub> (built-in protection resistance)	R00, R01	3.0		mA
Common output current	I <sub>OH3</sub>	V <sub>OH3</sub> =-0.05V	COM0-COM3		-3	μA
	I <sub>OL3</sub>	V <sub>OL3</sub> =V <sub>L3</sub> +0.05V		3		μA
Segment output current (during LCD output)	I <sub>OH4</sub>	V <sub>OH4</sub> =-0.05V	SEG0-SEG19		-3	μA
	I <sub>OL4</sub>	V <sub>OL4</sub> =V <sub>L3</sub> +0.05V		3		μA
Segment output current (during DC output)	I <sub>OH5</sub>	V <sub>OH5</sub> =0.1•V <sub>SS</sub>	SEG0-SEG19		-300	μA
	I <sub>OL5</sub>	V <sub>OL5</sub> =0.9•V <sub>SS</sub>		300		μA

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(Unless otherwise specified: VDD=0V, VSS=-1.5V, fosc=32.768kHz, Ta=25°C, VS1/VL1-VL3 are internal voltage, C1-C6=0.1μF)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
High level input voltage (1)	V <sub>IH1</sub>		K00-K03, P00-P03	0.2•V <sub>SS</sub>	0	V
High level input voltage (2)	V <sub>IH2</sub>		RESET, TEST	0.15•V <sub>SS</sub>	0	V
Low level input voltage (1)	V <sub>IL1</sub>		K00-K03, P00-P03	V <sub>SS</sub>	0.8•V <sub>SS</sub>	V
Low level input voltage (2)	V <sub>IL2</sub>		RESET, TEST	V <sub>SS</sub>	0.85•V <sub>SS</sub>	V
High level input current (1)	I <sub>IH1</sub>	V <sub>IH1</sub> =0V, No pull down resistor	K00-K03, P00-P03	0	0.5	μA
High level input current (2)	I <sub>IH2</sub>	V <sub>IH2</sub> =0V, With pull down resistor	K00-K03	2.0	16	μA
High level input current (3)	I <sub>IH3</sub>	V <sub>IH3</sub> =0V, With pull down resistor	P00-P03	9.0	100	μA
Low level input current	I <sub>IL</sub>	V <sub>IL</sub> =V <sub>SS</sub>	K00-K03, P00-P03 RESET, TEST	-0.5	0	μA
High level output current (1)	I <sub>OH1</sub>	V <sub>OH1</sub> =0.1•V <sub>SS</sub>	R02, R03, P00-P03		-200	μA
High level output current (2)	I <sub>OH2</sub>	V <sub>OH2</sub> =0.1•V <sub>SS</sub> (built-in protection resistance)	R00, R01		-200	μA
Low level output current (1)	I <sub>OL1</sub>	V <sub>OL1</sub> =0.9•V <sub>SS</sub>	R02, R03, P00-P03	700		μA
Low level output current (2)	I <sub>OL2</sub>	V <sub>OL2</sub> =0.9•V <sub>SS</sub> (built-in protection resistance)	R00, R01	700		μA
Common output current	I <sub>OH3</sub>	V <sub>OH3</sub> =-0.05V	COM0-COM3		-3	μA
	I <sub>OL3</sub>	V <sub>OL3</sub> =V <sub>L3</sub> +0.05V		3		μA
Segment output current (during LCD output)	I <sub>OH4</sub>	V <sub>OH4</sub> =-0.05V	SEG0-SEG19		-3	μA
	I <sub>OL4</sub>	V <sub>OL4</sub> =V <sub>L3</sub> +0.05V		3		μA
Segment output current (during DC output)	I <sub>OH5</sub>	V <sub>OH5</sub> =0.1•V <sub>SS</sub>	SEG0-SEG19		-100	μA
	I <sub>OL5</sub>	V <sub>OL5</sub> =0.9•V <sub>SS</sub>		130		μA

● Analog Circuit Characteristics and Current Consumption

**E0C623A (Normal Mode)**

(Unless otherwise specified: V<sub>DD</sub>=0V, V<sub>SS</sub>=-3.0V, f<sub>osc</sub>=32.768kHz, T<sub>a</sub>=25°C, C<sub>G</sub>=25pF, V<sub>S1</sub>/V<sub>L1</sub>-V<sub>L3</sub> are internal voltage, C<sub>1</sub>-C<sub>6</sub>=0.1μF)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Internal voltage	V <sub>L1</sub>	Connect 1MΩ load resistor between V <sub>DD</sub> and V <sub>L1</sub> (without panel load)	-1.15	-1.05	-0.95	V
	V <sub>L2</sub>	Connect 1MΩ load resistor between V <sub>DD</sub> and V <sub>L2</sub> (without panel load)	2•V <sub>L1</sub> -0.1		2•V <sub>L1</sub> ×0.9	V
	V <sub>L3</sub>	Connect 1MΩ load resistor between V <sub>DD</sub> and V <sub>L3</sub> (without panel load)	3•V <sub>L1</sub> -0.1		3•V <sub>L1</sub> ×0.9	V
SVD voltage	V <sub>SVD</sub>		-2.55	-2.40	-2.25	V
SVD circuit response time	t <sub>SVD</sub>				100	μS
Current consumption	I <sub>OP</sub>	During HALT		1.0	2.5	μA
		During execution *1	Without panel load	2.5	5.0	μA

\*1: The SVD circuit is turned off.

**E0C623A (Heavy Load Protection Mode)**

(Unless otherwise specified: V<sub>DD</sub>=0V, V<sub>SS</sub>=-3.0V, f<sub>osc</sub>=32.768kHz, T<sub>a</sub>=25°C, C<sub>G</sub>=25pF, V<sub>S1</sub>/V<sub>L1</sub>-V<sub>L3</sub> are internal voltage, C<sub>1</sub>-C<sub>6</sub>=0.1μF)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Internal voltage	V <sub>L1</sub>	Connect 1MΩ load resistor between V <sub>DD</sub> and V <sub>L1</sub> (without panel load)	-1.15	-1.05	-0.95	V
	V <sub>L2</sub>	Connect 1MΩ load resistor between V <sub>DD</sub> and V <sub>L2</sub> (without panel load)	2•V <sub>L1</sub> -0.1		2•V <sub>L1</sub> ×0.85	V
	V <sub>L3</sub>	Connect 1MΩ load resistor between V <sub>DD</sub> and V <sub>L3</sub> (without panel load)	3•V <sub>L1</sub> -0.1		3•V <sub>L1</sub> ×0.85	V
SVD voltage	V <sub>SVD</sub>		-2.55	-2.40	-2.25	V
SVD circuit response time	t <sub>SVD</sub>				100	μS
Current consumption	I <sub>OP</sub>	During HALT		2.0	5.5	μA
		During execution *1	Without panel load	5.5	10.0	μA

\*1: The SVD circuit is turned off.

**E0C62L3A (Normal Mode)**

(Unless otherwise specified: V<sub>DD</sub>=0V, V<sub>SS</sub>=-1.5V, f<sub>osc</sub>=32.768kHz, T<sub>a</sub>=25°C, C<sub>G</sub>=25pF, V<sub>S1</sub>/V<sub>L1</sub>-V<sub>L3</sub> are internal voltage, C<sub>1</sub>-C<sub>6</sub>=0.1μF)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Internal voltage	V <sub>L1</sub>	Connect 1MΩ load resistor between V <sub>DD</sub> and V <sub>L1</sub> (without panel load)	-1.15	-1.05	-0.95	V
	V <sub>L2</sub>	Connect 1MΩ load resistor between V <sub>DD</sub> and V <sub>L2</sub> (without panel load)	2•V <sub>L1</sub> -0.1		2•V <sub>L1</sub> ×0.9	V
	V <sub>L3</sub>	Connect 1MΩ load resistor between V <sub>DD</sub> and V <sub>L3</sub> (without panel load)	3•V <sub>L1</sub> -0.1		3•V <sub>L1</sub> ×0.9	V
SVD voltage	V <sub>SVD</sub>		-1.30	-1.20	-1.10	V
SVD circuit response time	t <sub>SVD</sub>				100	μS
Current consumption	I <sub>OP</sub>	During HALT		1.0	2.5	μA
		During execution *1	Without panel load	2.5	5.0	μA

\*1: The SVD circuit is turned off.

**E0C62L3A (Heavy Load Protection Mode)**

(Unless otherwise specified: V<sub>DD</sub>=0V, V<sub>SS</sub>=-1.5V, f<sub>osc</sub>=32.768kHz, T<sub>a</sub>=25°C, C<sub>G</sub>=25pF, V<sub>S1</sub>/V<sub>L1</sub>-V<sub>L3</sub> are internal voltage, C<sub>1</sub>-C<sub>6</sub>=0.1μF)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Internal voltage	V <sub>L1</sub>	Connect 1MΩ load resistor between V <sub>DD</sub> and V <sub>L1</sub> (without panel load)	-1.15	-1.05	-0.95	V
	V <sub>L2</sub>	Connect 1MΩ load resistor between V <sub>DD</sub> and V <sub>L2</sub> (without panel load)	2•V <sub>L1</sub> -0.1		2•V <sub>L1</sub> ×0.85	V
	V <sub>L3</sub>	Connect 1MΩ load resistor between V <sub>DD</sub> and V <sub>L3</sub> (without panel load)	3•V <sub>L1</sub> -0.1		3•V <sub>L1</sub> ×0.85	V
SVD voltage	V <sub>SVD</sub>		-1.30	-1.20	-1.10	V
SVD circuit response time	t <sub>SVD</sub>				100	μS
Current consumption	I <sub>OP</sub>	During HALT		2.0	5.5	μA
		During execution *1	Without panel load	5.5	10.0	μA

\*1: The SVD circuit is turned off.

**E0C623A (CR, Normal Mode)**

(Unless otherwise specified: V<sub>DD</sub>=0V, V<sub>SS</sub>=-3.0V, f<sub>OSC</sub>=65kHz, R<sub>CR</sub>=420kΩ, T<sub>a</sub>=25°C, V<sub>S1</sub>/V<sub>L1</sub>-V<sub>L3</sub> are internal voltage, C1-C6=0.1μF)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Internal voltage	V <sub>L1</sub>	Connect 1MΩ load resistor between V <sub>DD</sub> and V <sub>L1</sub> (without panel load)	-1.15	-1.05	-0.95	V
	V <sub>L2</sub>	Connect 1MΩ load resistor between V <sub>DD</sub> and V <sub>L2</sub> (without panel load)	2•V <sub>L1</sub> -0.1		2•V <sub>L1</sub> ×0.9	V
	V <sub>L3</sub>	Connect 1MΩ load resistor between V <sub>DD</sub> and V <sub>L3</sub> (without panel load)	3•V <sub>L1</sub> -0.1		3•V <sub>L1</sub> ×0.9	V
SVD voltage	V <sub>SVD</sub>		-2.55	-2.40	-2.25	V
SVD circuit response time	t <sub>SVD</sub>				100	μS
Current consumption	I <sub>OP</sub>	During HALT		8.0	15.0	μA
		During execution *1	Without panel load	15.0	20.0	μA

\*1: The SVD circuit is turned off.

**E0C623A (CR, Heavy Load Protection Mode)**

(Unless otherwise specified: V<sub>DD</sub>=0V, V<sub>SS</sub>=-3.0V, f<sub>OSC</sub>=65kHz, R<sub>CR</sub>=420kΩ, T<sub>a</sub>=25°C, V<sub>S1</sub>/V<sub>L1</sub>-V<sub>L3</sub> are internal voltage, C1-C6=0.1μF)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Internal voltage	V <sub>L1</sub>	Connect 1MΩ load resistor between V <sub>DD</sub> and V <sub>L1</sub> (without panel load)	-1.15	-1.05	-0.95	V
	V <sub>L2</sub>	Connect 1MΩ load resistor between V <sub>DD</sub> and V <sub>L2</sub> (without panel load)	2•V <sub>L1</sub> -0.1		2•V <sub>L1</sub> ×0.85	V
	V <sub>L3</sub>	Connect 1MΩ load resistor between V <sub>DD</sub> and V <sub>L3</sub> (without panel load)	3•V <sub>L1</sub> -0.1		3•V <sub>L1</sub> ×0.85	V
SVD voltage	V <sub>SVD</sub>		-2.55	-2.40	-2.25	V
SVD circuit response time	t <sub>SVD</sub>				100	μS
Current consumption	I <sub>OP</sub>	During HALT		16.0	30.0	μA
		During execution *1	Without panel load	30.0	40.0	μA

\*1: The SVD circuit is turned off.

**E0C62L3A (CR, Normal Mode)**

(Unless otherwise specified: V<sub>DD</sub>=0V, V<sub>SS</sub>=-1.5V, f<sub>OSC</sub>=65kHz, R<sub>CR</sub>=420kΩ, T<sub>a</sub>=25°C, V<sub>S1</sub>/V<sub>L1</sub>-V<sub>L3</sub> are internal voltage, C1-C6=0.1μF)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Internal voltage	V <sub>L1</sub>	Connect 1MΩ load resistor between V <sub>DD</sub> and V <sub>L1</sub> (without panel load)	-1.15	-1.05	-0.95	V
	V <sub>L2</sub>	Connect 1MΩ load resistor between V <sub>DD</sub> and V <sub>L2</sub> (without panel load)	2•V <sub>L1</sub> -0.1		2•V <sub>L1</sub> ×0.9	V
	V <sub>L3</sub>	Connect 1MΩ load resistor between V <sub>DD</sub> and V <sub>L3</sub> (without panel load)	3•V <sub>L1</sub> -0.1		3•V <sub>L1</sub> ×0.9	V
SVD voltage	V <sub>SVD</sub>		-1.30	-1.20	-1.10	V
SVD circuit response time	t <sub>SVD</sub>				100	μS
Current consumption	I <sub>OP</sub>	During HALT		8.0	15.0	μA
		During execution *1	Without panel load	15.0	20.0	μA

\*1: The SVD circuit is turned off.

**E0C62L3A (CR, Heavy Load Protection Mode)**

(Unless otherwise specified: V<sub>DD</sub>=0V, V<sub>SS</sub>=-1.5V, f<sub>OSC</sub>=65kHz, R<sub>CR</sub>=420kΩ, T<sub>a</sub>=25°C, V<sub>S1</sub>/V<sub>L1</sub>-V<sub>L3</sub> are internal voltage, C1-C6=0.1μF)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Internal voltage	V <sub>L1</sub>	Connect 1MΩ load resistor between V <sub>DD</sub> and V <sub>L1</sub> (without panel load)	-1.15	-1.05	-0.95	V
	V <sub>L2</sub>	Connect 1MΩ load resistor between V <sub>DD</sub> and V <sub>L2</sub> (without panel load)	2•V <sub>L1</sub> -0.1		2•V <sub>L1</sub> ×0.85	V
	V <sub>L3</sub>	Connect 1MΩ load resistor between V <sub>DD</sub> and V <sub>L3</sub> (without panel load)	3•V <sub>L1</sub> -0.1		3•V <sub>L1</sub> ×0.85	V
SVD voltage	V <sub>SVD</sub>		-1.30	-1.20	-1.10	V
SVD circuit response time	t <sub>SVD</sub>				100	μS
Current consumption	I <sub>OP</sub>	During HALT		16.0	30.0	μA
		During execution *1	Without panel load	30.0	40.0	μA

\*1: The SVD circuit is turned off.

● Oscillation Characteristics

The oscillation characteristics change depending on the conditions (components used, board pattern, etc.). Use the following characteristics as reference values.

**E0C623A (Crystal oscillation circuit)**

(Unless otherwise specified: V<sub>DD</sub>=0V, V<sub>SS</sub>=-3.0V, Crystal: C-002R (C<sub>I</sub>=35kΩ), C<sub>G</sub>=25pF, C<sub>D</sub>=built-in, T<sub>a</sub>=25°C)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start voltage	V <sub>sta</sub>	t <sub>sta</sub> ≤5sec (V <sub>SS</sub> )	-1.8			V
Oscillation stop voltage	V <sub>stp</sub>	t <sub>stp</sub> ≤10sec (V <sub>SS</sub> )	-1.8			V
Built-in capacitance (drain)	C <sub>D</sub>	Including the parasitic capacity inside the IC		20		pF
Frequency/voltage deviation	∂f/∂V	V <sub>SS</sub> =-1.8 to -3.5V			5	ppm
Frequency/IC deviation	∂f/∂IC		-10		10	ppm
Frequency adjustment range	∂f/∂C <sub>G</sub>	C <sub>G</sub> =5 to 25pF	40			ppm
Harmonic oscillation start voltage	V <sub>hho</sub>	C <sub>G</sub> =5pF (V <sub>SS</sub> )			-3.5	V
Permitted leak resistance	R <sub>leak</sub>	Between OSC1 and V <sub>DD</sub> , V <sub>SS</sub>	200			MΩ

**E0C62L3A (Crystal oscillation circuit)**

(Unless otherwise specified: V<sub>DD</sub>=0V, V<sub>SS</sub>=-1.5V, Crystal: C-002R (C<sub>I</sub>=35kΩ), C<sub>G</sub>=25pF, C<sub>D</sub>=built-in, T<sub>a</sub>=25°C)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start voltage	V <sub>sta</sub>	t <sub>sta</sub> ≤5sec (V <sub>SS</sub> )	-1.1			V
Oscillation stop voltage	V <sub>stp</sub>	t <sub>stp</sub> ≤10sec (V <sub>SS</sub> )	-1.1(-0.9)*1			V
Built-in capacitance (drain)	C <sub>D</sub>	Including the parasitic capacity inside the IC		20		pF
Frequency/voltage deviation	∂f/∂V	V <sub>SS</sub> =-1.1 to -2.0V (-0.9) *1			5	ppm
Frequency/IC deviation	∂f/∂IC		-10		10	ppm
Frequency adjustment range	∂f/∂C <sub>G</sub>	C <sub>G</sub> =5 to 25pF	40			ppm
Harmonic oscillation start voltage	V <sub>hho</sub>	C <sub>G</sub> =5pF (V <sub>SS</sub> )			-2.0	V
Permitted leak resistance	R <sub>leak</sub>	Between OSC1 and V <sub>DD</sub> , V <sub>SS</sub>	200			MΩ

\*1: Items enclosed in parentheses ( ) are those used when operating at heavy load protection mode.

**E0C623A (CR oscillation circuit)**

(Unless otherwise specified: V<sub>DD</sub>=0V, V<sub>SS</sub>=-3.0V, R<sub>CR</sub>=420kΩ, T<sub>a</sub>=25°C)

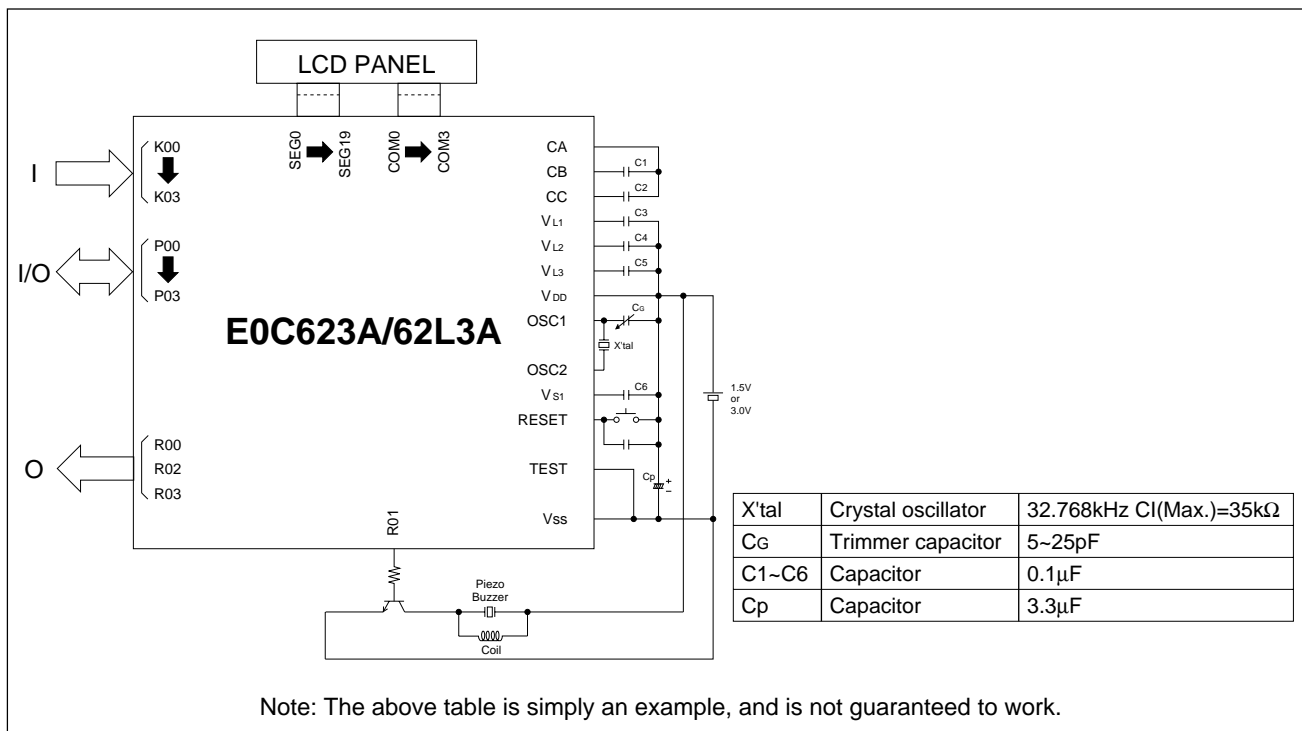
Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation frequency dispersion	f <sub>osc</sub>		-20	65kHz	20	%
Oscillation start voltage	V <sub>sta</sub>	(V <sub>SS</sub> )	-1.8			V
Oscillation start time	t <sub>sta</sub>	V <sub>SS</sub> =-1.8 to -3.5V		3		mS
Oscillation stop voltage	V <sub>stp</sub>	(V <sub>SS</sub> )	-1.8			V

**E0C62L3A (CR oscillation circuit)**

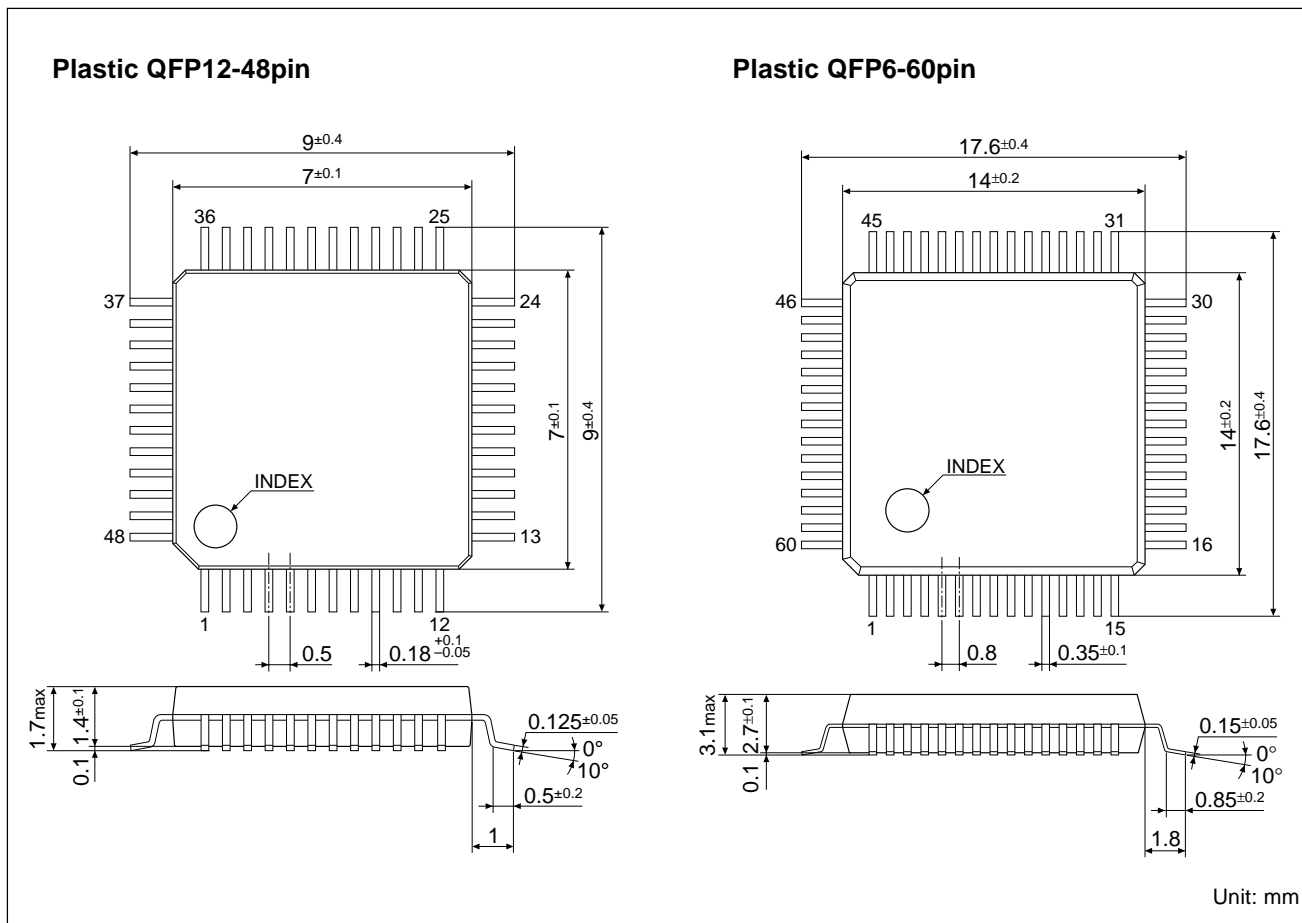
(Unless otherwise specified: V<sub>DD</sub>=0V, V<sub>SS</sub>=-1.5V, R<sub>CR</sub>=420kΩ, T<sub>a</sub>=25°C)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation frequency dispersion	f <sub>osc</sub>		-20	65kHz	20	%
Oscillation start voltage	V <sub>sta</sub>	(V <sub>SS</sub> )	-1.1			V
Oscillation start time	t <sub>sta</sub>	V <sub>SS</sub> =-1.1 to -2.0V		3		mS
Oscillation stop voltage	V <sub>stp</sub>	(V <sub>SS</sub> )	-1.1			V

## ■ BASIC EXTERNAL CONNECTION DIAGRAM



## ■ PACKAGE DIMENSIONS





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