EPSON

E0C623B

4-bit Single Chip Microcomputer

Low Voltage Operation Products

- 4-bit Core CPU
- Low Operating Voltage (0.8V)
- Built-in LCD Driver
- Serial Interface

■ DESCRIPTION

The E0C623B is a single-chip microcomputer for battery-driven products with 7-segment LCD display. It achieves low cost performance, and is suitable for a product added some feature instead of standard IC.
It consists that SEIKO EPSON's original core CPU E0C6200B, LCD driver (20 × 4), 96 words RAM, 1,536 words ROM.

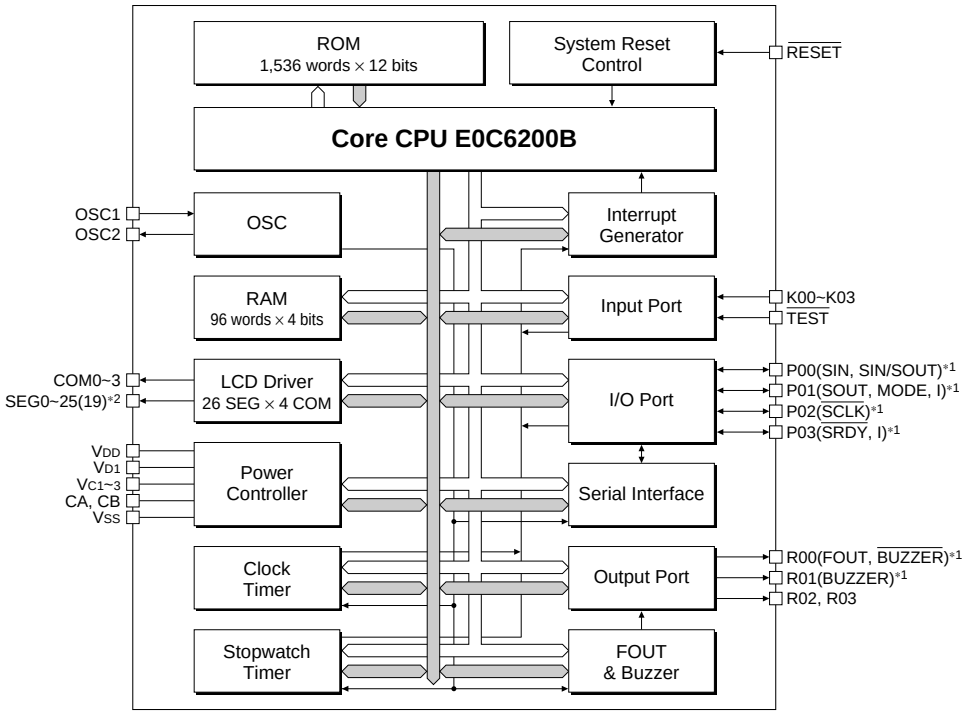
■ FEATURES

- CMOS LSI ..... 4-bit parallel processing
- Clock ..... 32.768kHz (Crystal at 1.5V)
  65kHz (CR at 1.5V)
  250 to 500kHz (CR at 3.0V)
  400 to 1000kHz (Ceramic at 3.0V)
- Instruction set ..... 100 instructions
- Instruction cycle time ..... 153µsec, 214µsec or 366µsec (32kHz)
  5µsec, 7µsec or 12µsec (1MHz)
- ROM capacity ..... 1,536 × 12 bits
- RAM capacity ..... 96 × 4 bits
- Input port ..... 4 bits (pull-up resistors are available by mask option)
- Output port ..... 4 bits (Nch open drain available)
- I/O port ..... 4 bits (Nch open drain available)
- Supply voltage detection (SVD) circuit .. 1.15V ±0.1V (1.5V) / 2.2V ±0.2V (3.0V)
- Clock timer ..... 1 ch.
- Stopwatch timer ..... 1 ch.
- LCD driver ..... 20 segments × 4/3 commons (QFP)
  26 segments × 4/3 commons (Die)
- Serial interface ..... 1 ch. (clock synchronous type)
- Interrupts ..... External : Key interrupt 1 line
  Internal : Timer interrupt 2 lines
  Serial interface interrupt 1 line
- Suppry voltage ..... 0.8 to 3.6V (E0C623B)
  1.8 to 3.6V (E0C62A3B)
- Current consumption ..... HALT mode : TBDµA (32.768kHz Crystal, 3.0V)
  OPERATING mode : TBDµA (32.768kHz Crystal, 3.0V)
- Package ..... QFP12-48pin (plastic), Die form

■ LINE UP

Model	Supply voltage	Clock
E0C623B	0.8V to 3.6V	32.768kHz Crystal or 65kHz CR
E0C62A3B	1.7V to 3.6V	250k~500kHz CR or 400k~1MHz Ceramic

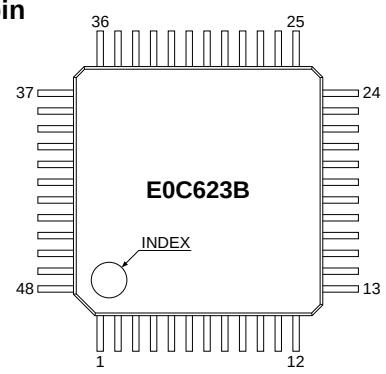
■ BLOCK DIAGRAM



*1: Terminal specifications can be selected by mask option.
*2: SEG0 to 4, 6 and 8 to 19 are only available in the QFP12-48pin package.

■ PIN CONFIGURATION

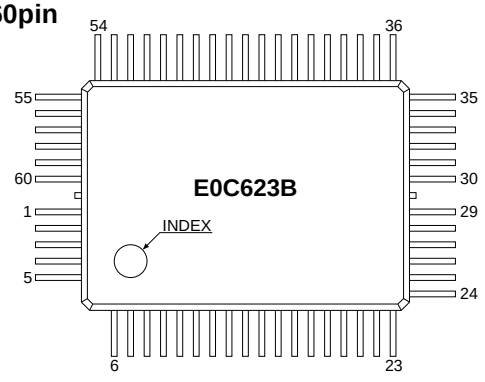
QFP12-48pin



No.	Pin name	No.	Pin name	No.	Pin name	No.	Pin name
1	COM2	13	SEG12	25	P00	37	V_{DD}
2	COM3	14	SEG13	26	N.C.	38	OSC1
3	SEG0	15	SEG14	27	$\overline{RESET}$	39	OSC2
4	SEG1	16	SEG15	28	K00	40	V_{D1}
5	SEG2	17	SEG16	29	K01	41	CA
6	SEG3	18	SEG17	30	K02	42	CB
7	SEG4	19	SEG18	31	K03	43	N.C.
8	SEG6	20	SEG19	32	R00	44	V_{C1}
9	SEG8	21	$\overline{TEST}$	33	R01	45	V_{C2}
10	SEG9	22	P03	34	R02	46	V_{C3}
11	SEG10	23	P02	35	R03	47	COM0
12	SEG11	24	P01	36	V_{SS}	48	COM1

N.C. = No Connection

QFP5-60pin



No.	Pin name	No.	Pin name	No.	Pin name	No.	Pin name
1	V_{C2}	16	SEG9	31	SEG24	46	K02
2	V_{C3}	17	SEG10	32	SEG25	47	K03
3	COM0	18	SEG11	33	$\overline{TEST}$	48	R00
4	COM1	19	SEG12	34	P03	49	R01
5	COM2	20	SEG13	35	P02	50	R02
6	COM3	21	SEG14	36	P01	51	R03
7	SEG0	22	SEG15	37	P00	52	N.C.
8	SEG1	23	SEG16	38	N.C.	53	V_{SS}
9	SEG2	24	SEG17	39	N.C.	54	V_{DD}
10	SEG3	25	SEG18	40	N.C.	55	OSC1
11	SEG4	26	SEG19	41	N.C.	56	OSC2
12	SEG5	27	SEG20	42	N.C.	57	V_{D1}
13	SEG6	28	SEG21	43	$\overline{RESET}$	58	CA
14	SEG7	29	SEG22	44	K00	59	CB
15	SEG8	30	SEG23	45	K01	60	V_{C1}

N.C. = No Connection

■ PIN DESCRIPTION

Pin name	Pin No.		In/Out	Function
	QFP12-48pin	QFP5-60pin		
V_{DD}	37	54	(I)	Power supply pin (+)
V_{SS}	36	53	(I)	Power supply pin (-)
V_{D1}	40	57	–	Oscillation and internal logic system regulated voltage output pin
V_{C1}	44	60	–	LCD system regulated voltage output pin (approx. 1.05 V)
V_{C2}	45	1	–	LCD system booster voltage output pin ($V_{C1} \times 2$)
V_{C3}	46	2	–	LCD system booster voltage output pin ($V_{C1} \times 3$)
CA, CB	41, 42	58, 59	–	Boost capacitor connecting pin
OSC1	38	55	I	Oscillation input pin (crystal, CR or ceramic ∗)
OSC2	39	56	O	Oscillation output pin (crystal, CR or ceramic ∗)
K00–K03	28–31	44–47	I	Input port pin
P00	25	37	I/O	I/O port pin or serial I/F data input/output pin ∗
P01	24	36	I/O	I/O port pin, serial I/F data output pin or input-only pin ∗
P02	23	35	I/O	I/O port pin or serial I/F clock output pin ∗
P03	22	34	I/O	I/O port pin, serial I/F ready signal output pin or input-only pin ∗
R00	32	48	O	Output port pin, buzzer or FOUT output pin ∗
R01	33	49	O	Output port pin or buzzer output pin ∗
R02, R03	34, 35	50, 51	O	Output port pin
SEG0–4	3–7	7–11	O	LCD segment output pin or DC output pin ∗
SEG5	–	12	O	LCD segment output pin or DC output pin ∗ (QFP5-60pin only)
SEG6	8	13	O	LCD segment output pin or DC output pin ∗
SEG7	–	14	O	LCD segment output pin or DC output pin ∗ (QFP5-60pin only)
SEG8–19	9–20	15–26	O	LCD segment output pin or DC output pin ∗
SEG20–25	–	27–32	O	LCD segment output pin or DC output pin ∗ (QFP5-60pin only)
COM0–3	47, 48, 1, 2	3–6	O	LCD common output pin
$\overline{RESET}$	27	43	I	Initial reset input pin
$\overline{TEST}$	21	33	I	Input pin for test

∗ Selected by mask option

■ ELECTRICAL CHARACTERISTICS

● Absolute Maximum Ratings

(V_{SS}=0V)

Rating	Symbol	Value	Unit
Supply voltage	V_{DD}	-0.5 to 7.0	V
Input voltage (1)	V_I	-0.5 to V_{DD} + 0.3	V
Input voltage (2)	V_{IOSC}	-0.5 to V_{D1} + 0.3	V
Permissible total output current ∗1	ΣI_{VDD}	10	mA
Operating temperature	Topr	-20 to 70	°C
Storage temperature	Tstg	-65 to 150	°C
Soldering temperature / time	Tsol	260°C, 10sec (lead section)	–
Permissible dissipation ∗2	P_D	250	mW

∗1: The permissible total output current is the sum total of the current (average current) that simultaneously flows from the output pin (or is drawn in).

∗2: In case of plastic package (QFP12-48pin).

● Recommended Operating Conditions

(Ta=-20 to 70°C)

Condition	Symbol	Remark	Min.	Typ.	Max.	Unit
Supply voltage	V_{DD}	E0C623B (Crystal oscillation)	1.1		3.6	V
		E0C623B (Crystal oscillation + HVLD∗1)	0.8		3.6	V
		E0C623B (CR oscillation)	1.1		3.6	V
		E0C623B (CR oscillation + HVLD∗1)	0.8		3.6	V
		E0C62A3B (CR oscillation)	1.7		3.6	V
		E0C62A3B (Ceramic oscillation)	1.7		3.6	V
Oscillation frequency	f_{OSC}	E0C623B (Crystal oscillation)	–	32.768	–	kHz
		E0C623B (CR oscillation)	30		80	kHz
		E0C62A3B (CR oscillation)			500	kHz
		E0C62A3B (Ceramic oscillation)			1M	Hz

∗1: HVLD = Heavy load protection mode

● DC Characteristics

(Unless otherwise specified: V_{DD}=1.5V, V_{SS}=0V, f_{OSC}=32.768kHz, Ta=25°C, V_{D1}/V_{C1}–V_{C3} are internal voltage, C_1–C_5=0.1µF)

Characteristic	Symbol	Condition		Min.	Typ.	Max.	Unit
High level input voltage (1)	V_{IH1}		K00–K03, P00–P03	0.8•V_{DD}		V_{DD}	V
High level input voltage (2)	V_{IH2}		$\overline{RESET}$, $\overline{TEST}$	0.9•V_{DD}		V_{DD}	V
Low level input voltage (1)	V_{IL1}		K00–K03, P00–P03	0		0.1•V_{DD}	V
Low level input voltage (2)	V_{IL2}		$\overline{RESET}$, $\overline{TEST}$	0		0.1•V_{DD}	V
High level input current	I_{IH}	V_{IH}=1.5V	K00–K03, P00–P03, $\overline{RESET}$, $\overline{TEST}$	0		0.5	µA
Low level input current (1)	I_{IL1}	V_{IL1}=V_{SS} No pull up	K00–K03, P00–P03 $\overline{RESET}$, $\overline{TEST}$	-0.5		0	µA
Low level input current (2)	I_{IL2}	V_{IL2}=V_{SS} With pull up	K00–K03, P00–P03 $\overline{RESET}$, $\overline{TEST}$	-16	-10	-6	µA
High level output current (1)	I_{OH1}	V_{OH1}=0.9•V_{DD}	R00–R03, P00–P03			-0.3	mA
High level output current (2)	I_{OH2}	V_{OH2}=0.9•V_{DD}	BZ, $\overline{BZ}$, FOUT			-0.3	mA
Low level output current (1)	I_{OL1}	V_{OL1}=0.1•V_{DD}	R00–R03, P00–P03	0.7			mA
Low level output current (2)	I_{OL2}	V_{OL2}=0.1•V_{DD}	BZ, $\overline{BZ}$, FOUT	0.7			mA
Common output current	I_{OH3}	V_{OH3}=V_{C3}-0.05V	COM0–COM3			-10	µA
	I_{OL3}	V_{OL3}=V_{SS}+0.05V		10			µA
Segment output current (during LCD output)	I_{OH4}	V_{OH4}=V_{C3}-0.05V	SEG0–SEG25			-10	µA
	I_{OL4}	V_{OL4}=V_{SS}+0.05V		10			µA
Segment output current (during DC output)	I_{OH5}	V_{OH5}=0.9•V_{DD}	SEG0–SEG25			-100	µA
	I_{OL5}	V_{OL5}=0.1•V_{DD}		100			µA

(Unless otherwise specified: V_{DD}=3.0V, V_{SS}=0V, f_{OSC}=32.768kHz, Ta=25°C, V_{D1}/V_{C1}–V_{C3} are internal voltage, C_1–C_5=0.1µF)

Characteristic	Symbol	Condition		Min.	Typ.	Max.	Unit
High level input voltage (1)	V_{IH1}		K00–K03, P00–P03	0.8•V_{DD}		V_{DD}	V
High level input voltage (2)	V_{IH2}		$\overline{RESET}$, $\overline{TEST}$	0.9•V_{DD}		V_{DD}	V
Low level input voltage (1)	V_{IL1}		K00–K03, P00–P03	0		0.1•V_{DD}	V
Low level input voltage (2)	V_{IL2}		$\overline{RESET}$, $\overline{TEST}$	0		0.1•V_{DD}	V
High level input current	I_{IH}	V_{IH}=3.0V	K00–K03, P00–P03, $\overline{RESET}$, $\overline{TEST}$	0		0.5	µA
Low level input current (1)	I_{IL1}	V_{IL1}=V_{SS} No pull up	K00–K03, P00–P03 $\overline{RESET}$, $\overline{TEST}$	-0.5		0	µA
Low level input current (2)	I_{IL2}	V_{IL2}=V_{SS} With pull up	K00–K03, P00–P03 $\overline{RESET}$, $\overline{TEST}$	-32	-20	-12	µA
High level output current (1)	I_{OH1}	V_{OH1}=0.9•V_{DD}	R00–R03, P00–P03			-1.5	mA
High level output current (2)	I_{OH2}	V_{OH2}=0.9•V_{DD}	BZ, $\overline{BZ}$, FOUT			-1.5	mA
Low level output current (1)	I_{OL1}	V_{OL1}=0.1•V_{DD}	R00–R03, P00–P03	6			mA
Low level output current (2)	I_{OL2}	V_{OL2}=0.1•V_{DD}	BZ, $\overline{BZ}$, FOUT	6			mA
Common output current	I_{OH3}	V_{OH3}=V_{C3}-0.05V	COM0–COM3			-10	µA
	I_{OL3}	V_{OL3}=V_{SS}+0.05V		10			µA
Segment output current (during LCD output)	I_{OH4}	V_{OH4}=V_{C3}-0.05V	SEG0–SEG25			-10	µA
	I_{OL4}	V_{OL4}=V_{SS}+0.05V		10			µA
Segment output current (during DC output)	I_{OH5}	V_{OH5}=0.9•V_{DD}	SEG0–SEG25			-300	µA
	I_{OL5}	V_{OL5}=0.1•V_{DD}		300			µA

● Analog Circuit Characteristics and Current Consumption

LCD drive voltage

(Unless otherwise specified: V_{DD}=3.0V, V_{SS}=0V, f_{OSC}=32.768kHz, Ta=25°C, V_{D1}/V_{C1}–V_{C3} are internal voltage, C_1–C_5=0.1µF)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
LCD drive voltage	V_{C1}	Connect 1MΩ load resistor between V_{SS} and V_{C1} (no panel load)	0.95	1.05	1.15	V
	V_{C2}	Connect 1MΩ load resistor between V_{SS} and V_{C2} (no panel load)	2•V_{C1} ×0.9		2•V_{C1} +0.1	V
	V_{C3}	Connect 1MΩ load resistor between V_{SS} and V_{C3} (no panel load)	3•V_{C1} ×0.9		3•V_{C1} +0.1	V

Current consumption

(Unless otherwise specified: V_{DD}=3.0V, V_{SS}=0V, Ta=25°C, V_{D1}/V_{C1}–V_{C3} are internal voltage, C_1–C_5=0.1µF, No panel load)

Characteristic	Symbol	Condition		Min.	Typ.	Max.	Unit
Current consumption	I_{OP}	HALT mode	623B Crystal oscillation (32.768kHz)	–	2.5	5.0	µA
			623B Crystal oscillation (32.768kHz)+HVLD*1	–	6.5	9.0	µA
			623B CR oscillation (40kHz)	–	3.0	6.0	µA
			623B CR oscillation (40kHz)+HVLD*1	–	7.0	10.0	µA
			62A3B CR oscillation (250kHz)	–	55	110	µA
			62A3B Ceramic oscillation (1MHz)	–	80	200	µA
		RUN mode	623B Crystal oscillation (32.768kHz)	–	3.0	6.0	µA
			623B Crystal oscillation (32.768kHz)+HVLD*1	–	7.0	10.0	µA
			623B CR oscillation (40kHz)	–	3.5	7.0	µA
			623B CR oscillation (40kHz)+HVLD*1	–	7.5	11.0	µA
			62A3B CR oscillation (250kHz)	–	60	120	µA
			62A3B Ceramic oscillation (1MHz)	–	100	200	µA
		SLEEP mode	623B CR oscillation	–	–	1.0	µA
			62A3B CR oscillation	–	–	1.0	µA
			62A3B Ceramic oscillation	–	–	1.0	µA

*1: HVLD = Heavy load protection mode

● AC Characteristics

Serial interface

• Master mode 1

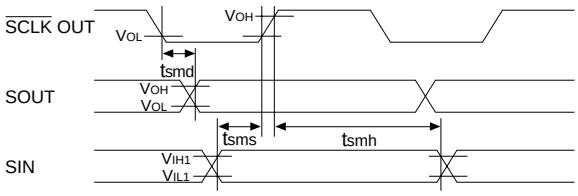
(Unless otherwise specified: V_{DD}=1.5V, V_{SS}=0V, f_{OSC}=32.768kHz, V_{IH1}=0.8V_{DD}, V_{IL1}=0.2V_{DD}, V_{OH}=0.8V_{DD}, V_{OL}=0.2V_{DD}, Ta=-20 to 70°C)

Characteristic	Symbol	Min.	Typ.	Max.	Unit
Transmit data output delay time	tsmd	–	–	5	µS
Receive data input set-up time	tsms	10	–	–	µS
Receive data input hold time	tsmh	5	–	–	µS

• Master mode 2

(Unless otherwise specified: V_{DD}=3.0V, V_{SS}=0V, f_{OSC}=1MHz, V_{IH1}=0.8V_{DD}, V_{IL1}=0.2V_{DD}, V_{OH}=0.8V_{DD}, V_{OL}=0.2V_{DD}, Ta=-20 to 70°C)

Characteristic	Symbol	Min.	Typ.	Max.	Unit
Transmit data output delay time	tsmd	–	–	300	nS
Receive data input set-up time	tsms	200	–	–	nS
Receive data input hold time	tsmh	200	–	–	nS



• Slave mode 1

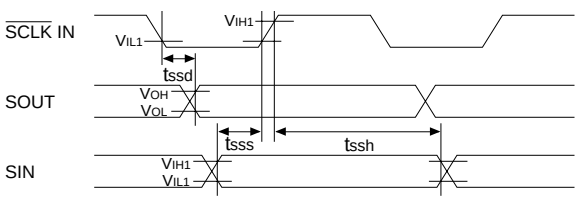
(Unless otherwise specified: V_{DD}=1.5V, V_{SS}=0V, f_{OSC}=32.768kHz, V_{IH1}=0.8V_{DD}, V_{IL1}=0.2V_{DD}, V_{OH}=0.8V_{DD}, V_{OL}=0.2V_{DD}, Ta=-20 to 70°C)

Characteristic	Symbol	Min.	Typ.	Max.	Unit
Transmit data output delay time	tssd	–	–	5	µS
Receive data input set-up time	tsss	10	–	–	µS
Receive data input hold time	tssh	5	–	–	µS

• Slave mode 2

(Unless otherwise specified: V_{DD}=3.0V, V_{SS}=0V, f_{OSC}=1MHz, V_{IH1}=0.8V_{DD}, V_{IL1}=0.2V_{DD}, V_{OH}=0.8V_{DD}, V_{OL}=0.2V_{DD}, Ta=-20 to 70°C)

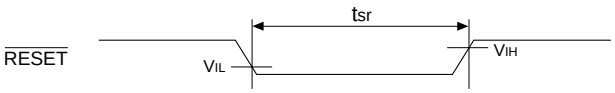
Characteristic	Symbol	Min.	Typ.	Max.	Unit
Transmit data output delay time	tssd	–	–	300	nS
Receive data input set-up time	tsss	200	–	–	nS
Receive data input hold time	tssh	200	–	–	nS



$\overline{\text{RESET}}$ input

(Unless otherwise specified: V_{DD}=1.5/3.0V, V_{SS}=0V, V_{IH}=0.5V_{DD}, V_{IL}=0.1V_{DD}, Ta=-20 to 70°C)

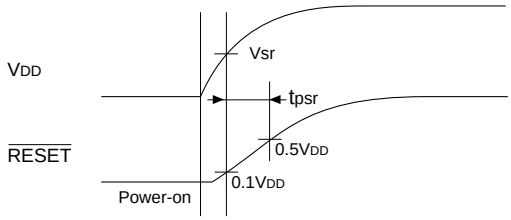
Characteristic	Symbol	Min.	Typ.	Max.	Unit
$\overline{\text{RESET}}$ input time	tsr	5.0			mS

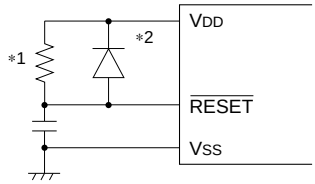


Power-on reset

(Unless otherwise specified: V_{DD}=1.5/3.0V, Ta=-20 to 70°C)

Characteristic	Symbol	Min.	Typ.	Max.	Unit
Operating supply voltage	Vsr	0.8•V_{DD}			V
$\overline{\text{RESET}}$ input time	tsr	5.0			mS





*1 When the built-in pull-up resistor is not used.

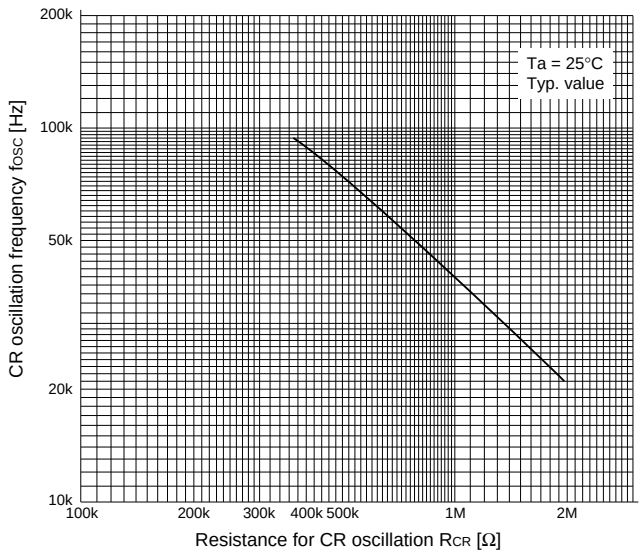
*2 Because the potential of the $\overline{\text{RESET}}$ terminal not reached V_{DD} level or higher.

● Oscillation Characteristics

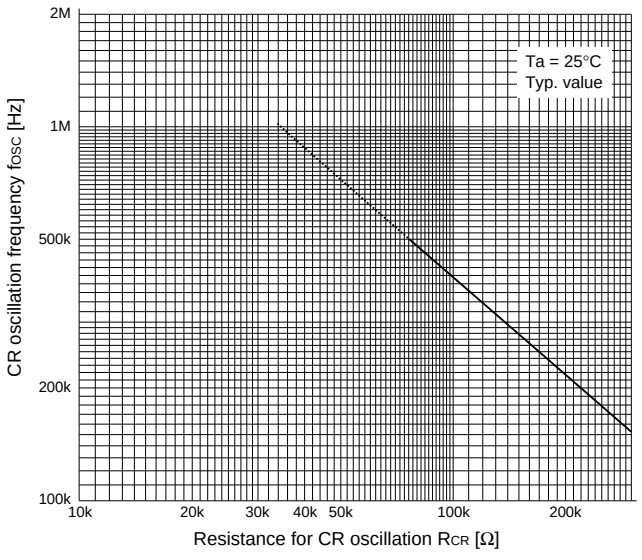
Oscillation characteristics will vary according to different conditions (elements used, board pattern). Use the following characteristics are as reference values.

CR oscillation frequency characteristics (reference value)

E0C623B



E0C62A3B



Crystal oscillation

(Unless otherwise specified: V_{DD}=3.0V, V_{SS}=0V, f_{OSC}=32.768kHz, Crystal: C-002R (C_I=35kΩ), C_G=25pF, C_D=built-in, Ta=25°C)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start voltage	Vsta	tsta≤3sec (Heavy load protection mode ON)	0.8			V
		tsta≤3sec (Heavy load protection mode OFF)	1.1			V
Oscillation stop voltage	Vstp	tstp≤10sec (Heavy load protection mode ON)	0.8			V
		tstp≤10sec (Heavy load protection mode OFF)	1.1			V
Built-in capacitance (drain)	C_D	Including the parasitic capacitance inside the IC (in chip)		14		pF
Frequency/voltage deviation	∂f/∂V	V_{DD}=0.8 to 3.6V (Heavy load protection mode ON)			5	ppm
		V_{DD}=1.1 to 3.6V (Heavy load protection mode OFF)			5	ppm
Frequency/IC deviation	∂f/∂IC		-10		10	ppm
Frequency adjustment range	∂f/∂C_G	C_G=5 to 25pF	30	40		ppm
Harmonic oscillation start voltage	V_{hho}	C_G=5pF (V_{DD})	3.6			V
Permitted leak resistance	R_{leak}	Between OSC1 and V_{DD}, V_{SS}	200			MΩ

CR oscillation

(Unless otherwise specified: V_{DD}=3.0V, V_{SS}=0V, R_{CR}=1MΩ, Ta=25°C)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation frequency dispersion	∂f_{OSCCR}	623B (Heavy load protection ON, V_{DD}=0.8 to 3.6V)	-20	40kHz	+20	%
		623B (Heavy load protection OFF, V_{DD}=1.1 to 3.6V)	-20	40kHz	+20	%
		62A3B (V_{DD}=1.7 to 3.6V)	-30	500kHz	+30	%
Oscillation start voltage	Vsta	623B	0.8			V
		62A3B	1.7			V
Oscillation start time	tsta				3	mS
Oscillation stop voltage	Vstp	623B	0.8			V
		62A3B	1.7			V

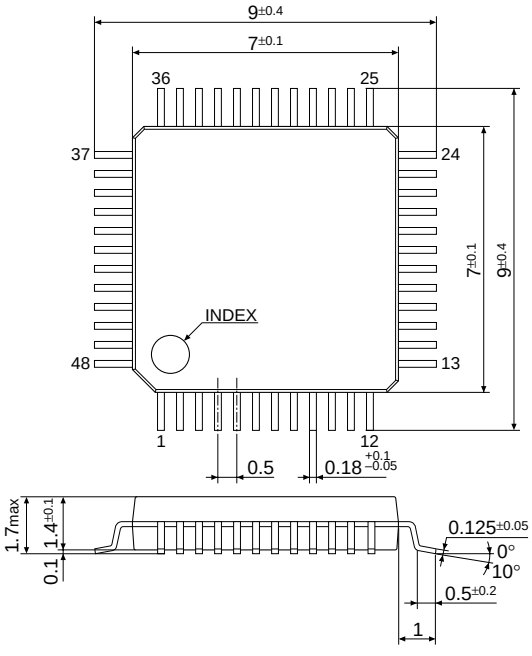
Ceramic oscillation

(Unless otherwise specified: V_{DD}=3.0V, V_{SS}=0V, Ceramic oscillator: CSA1.0MG, C_{GC}=C_{DC}=100pF, Ta=25°C)

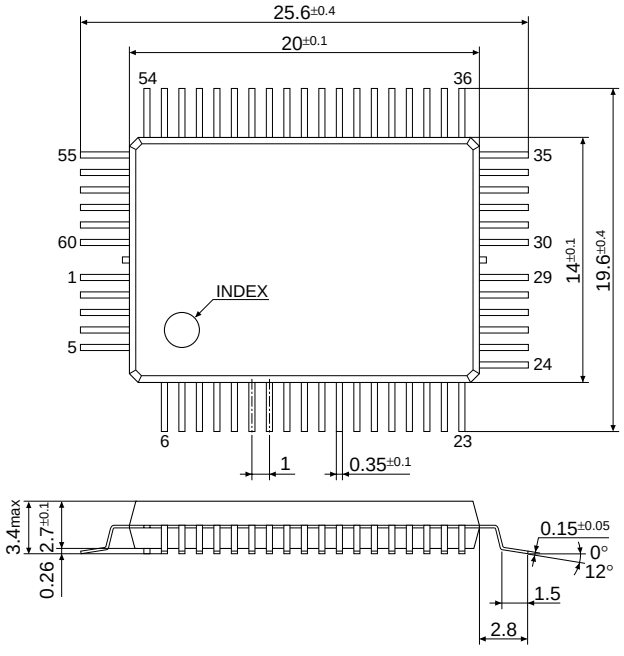
Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start voltage	Vsta		1.7			V
Oscillation start time	tsta				20	mS

■ PACKAGE DIMENSIONS

Plastic QFP12-48pin

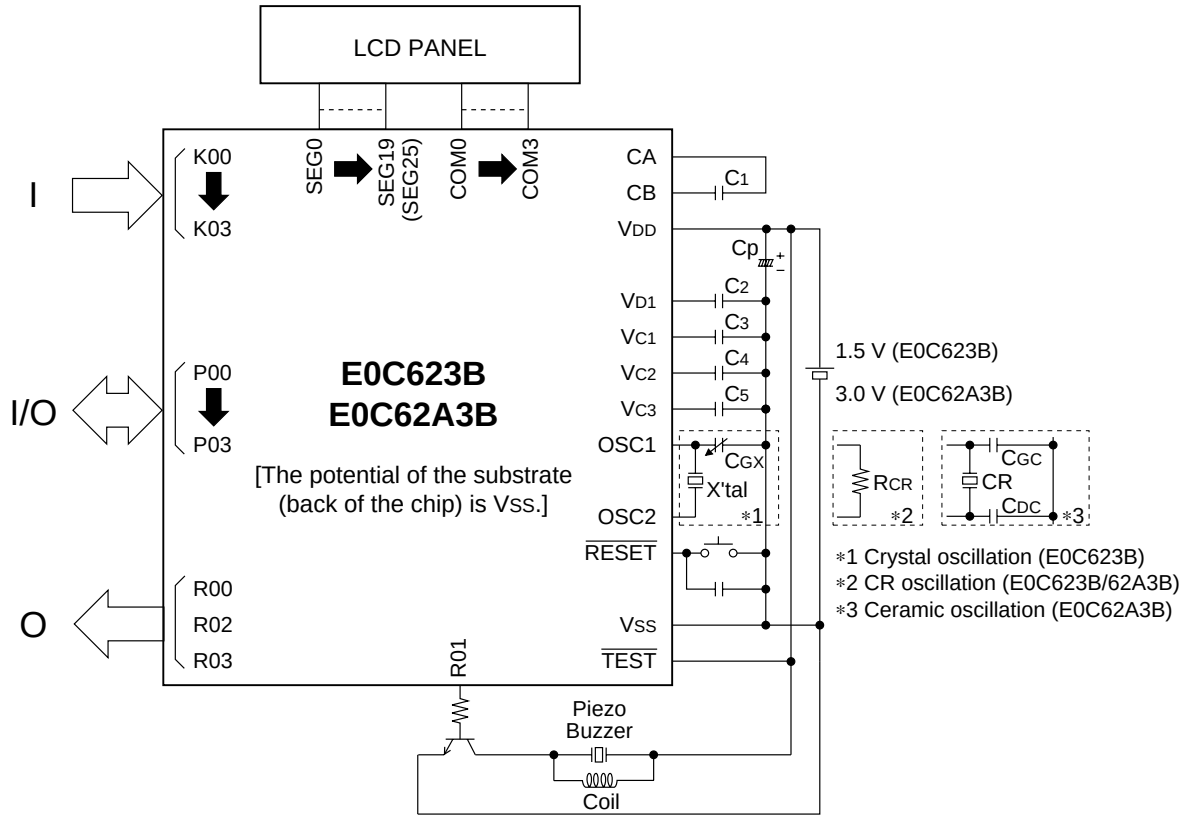


Plastic QFP5-60pin



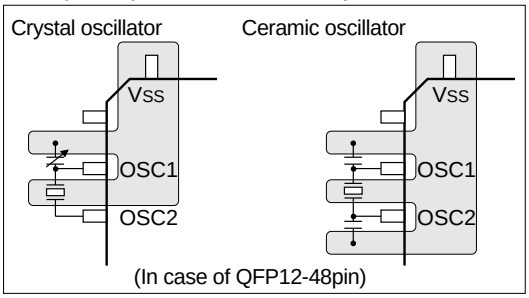
Unit: mm

■ BASIC EXTERNAL CONNECTION DIAGRAM



X'tal	Crystal oscillator	32.768 kHz, CI (Max.)=35 kΩ
CGX	Trimmer capacitor	5~25pF
RCR	Resistor for CR oscillation	See Section 6.6.
CR	Ceramic oscillator	1 MHz
CGC	Capacitor	100 pF
CDC	Capacitor	100 pF
C1–C5	Capacitor	0.1 µF
Cp	Capacitor	3.3 µF

Examples of pattern and oscillator layout



Note: • *The above table is simply an example, and is not guaranteed to work.*

• *When using the crystal oscillation circuit and ceramic oscillation circuit, make a board pattern with noise measure as shown above.*

• *In order to prevent unstable operation of the oscillation circuit due to current leak between OSC1 and VDD, please keep enough distance between VDD and other signals on the board pattern.*

• *Precautions for Visible Radiation*
Visible radiation causes semiconductor devices to change the electrical characteristics. It may cause this IC to malfunction. When developing products which use this IC, consider the following precautions to prevent malfunctions caused by visible radiations.

(1) Design the product and implement the IC on the board so that it is shielded from visible radiation in actual use.

(2) The inspection process of the product needs an environment that shields the IC from visible radiation.

(3) As well as the face of the IC, shield the back and side too.

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