EPSON

E0C6247

4-bit Single Chip Microcomputer

Low Voltage Operation Products

- Core CPU Architecture
- Dot Matrix LCD Driver
- Serial Interface
- Programmable SVD Circuit

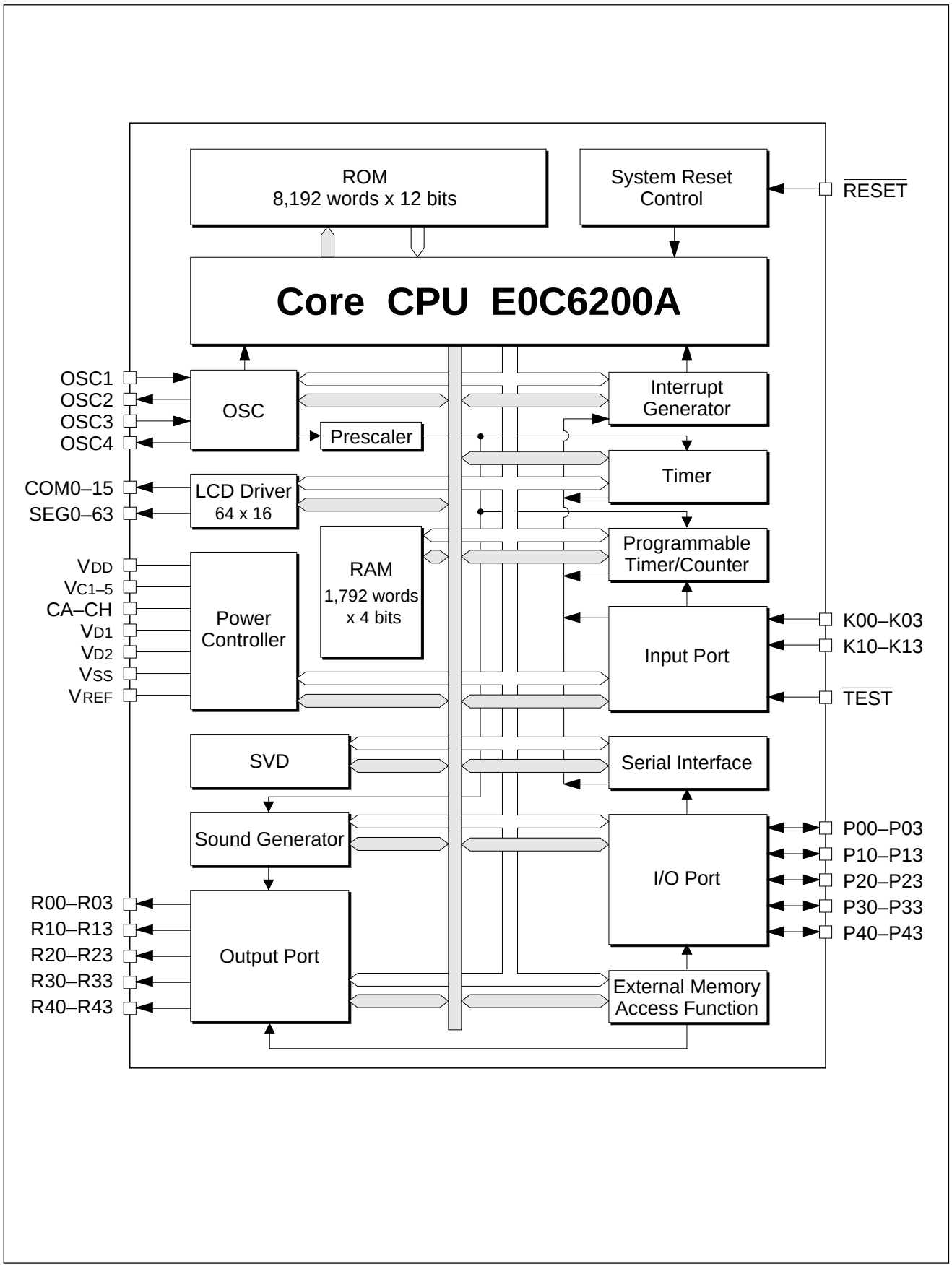
■ DESCRIPTION

The E0C6247 is a CMOS 4-bit single chip microcomputer, built-in Core CPU E0C6200A as main component, ROM, RAM, dot matrix LCD driver, serial interface, time base counter, SVD circuit and others.
The E0C6247 is most suitable for applications with equipment requiring dot matrix display functions.

■ FEATURES

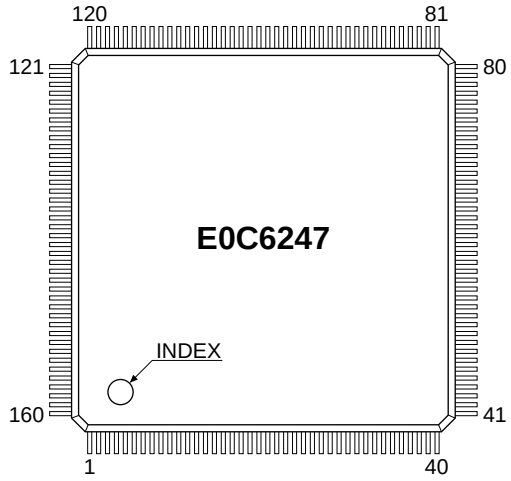
- CMOS LSI 4-bit parallel processing
- Twin clock ..... Crystal oscillation circuit (with built-in drain capacitance)
  32.768kHz, 38.4kHz, 50kHz, 76.8kHz
  Ceramic or CR oscillation circuit
  200kHz (Typ.) / 0.9V, 1MHz (Max.) / 3.0V
- Instruction set ..... 108 instructions
- Instruction cycle time ..... 32.768kHz clock : 153µsec, 214µsec, 366µsec
  38kHz clock : 130µsec, 182µsec, 313µsec
  50kHz clock : 100µsec, 140µsec, 240µsec
  76kHz clock : 65µsec, 91µsec, 156µsec
  200kHz clock : 25µsec, 35µsec, 60µsec
- ROM ..... 8,192 × 12 bits
- RAM ..... Data : 1,792 × 4 bits
  Segment : 256 × 4 bits
- External memory ..... Read/write (RAM) : 512K × 4 bits (Max.)
  Read only (ROM) : 1M × 4 bits (Max.)
- Input port ..... 8 bits (pull-up resistors are available by mask option)
- Output port ..... 20 bits (can be switched to external memory bus and buzzer output by software)
- I/O port ..... 20 bits (can be switched to external memory bus and serial I/O by software)
- Serial interface ..... 8-bit clock synchronous type
  or 8-bit/7-bit asynchronous type can be selected
- Dot matrix LCD driver ..... 64 segments × 8 commons/16 commons
- Time base counter ..... 1 channel for clock use
- Programmable timer ..... 8-bit : 1 channel, with event counter function
- Watchdog timer
- Programmable SVD circuit ..... 16 values programmable (1.05V to 2.60V)
- Sound generator ..... With degital envelope function, volume control function (8 levels)
- Interrupts ..... External : Input port 2 interrupts
  Internal : Clock timer 1 interrupt
  Programmable timer 1 interrupt
  Serial interface 3 interrupts
- Supply voltage ..... 0.9V to 3.6V
- Current consumption ..... HALT mode (32.768kHz or 38kHz/1.5V) : 2.0µA
  OPERATING mode (32.768kHz or 38kHz/3.0V) : 7.0µA
- Package ..... QFP8-160pin (plastic)
  Die form

■ BLOCK DIAGRAM



■ PIN CONFIGURATION

QFP8-160pin



No.	Pin name	No.	Pin name	No.	Pin name	No.	Pin name	No.	Pin name
1	SEG52	33	SEG20	65	K03	97	R01	129	V_{C1}
2	SEG51	34	SEG19	66	K10	98	R02	130	V_{C2}
3	SEG50	35	SEG18	67	K11	99	R03	131	V_{C3}
4	SEG49	36	SEG17	68	K12	100	R10	132	V_{C4}
5	SEG48	37	SEG16	69	K13	101	R11	133	V_{C5}
6	SEG47	38	SEG15	70	P00	102	R12	134	CH
7	SEG46	39	SEG14	71	P01	103	R13	135	CG
8	SEG45	40	SEG13	72	P02	104	R20	136	CF
9	SEG44	41	SEG12	73	P03	105	R21	137	CE
10	SEG43	42	SEG11	74	P10	106	R22	138	CD
11	SEG42	43	SEG10	75	P11	107	R23	139	CC
12	SEG41	44	SEG9	76	P12	108	R30	140	CB
13	SEG40	45	SEG8	77	P13	109	R31	141	CA
14	SEG39	46	SEG7	78	N.C.	110	R32	142	COM0
15	SEG38	47	SEG6	79	N.C.	111	R33	143	COM1
16	SEG37	48	SEG5	80	N.C.	112	R40	144	COM2
17	SEG36	49	SEG4	81	N.C.	113	R41	145	COM3
18	SEG35	50	SEG3	82	N.C.	114	R42	146	COM4
19	SEG34	51	SEG2	83	N.C.	115	R43	147	COM5
20	SEG33	52	SEG1	84	P20	116	N.C.	148	COM6
21	SEG32	53	SEG0	85	P21	117	N.C.	149	COM7
22	SEG31	54	COM15	86	P22	118	$\overline{TEST}$	150	SEG63
23	SEG30	55	COM14	87	P23	119	$\overline{RESET}$	151	SEG62
24	SEG29	56	COM13	88	P30	120	V_{REF}	152	SEG61
25	SEG28	57	COM12	89	P31	121	V_{DD}	153	SEG60
26	SEG27	58	COM11	90	P32	122	OSC4	154	SEG59
27	SEG26	59	COM10	91	P33	123	OSC3	155	SEG58
28	SEG25	60	COM9	92	P40	124	V_{D1}	156	SEG57
29	SEG24	61	COM8	93	P41	125	OSC2	157	SEG56
30	SEG23	62	K00	94	P42	126	OSC1	158	SEG55
31	SEG22	63	K01	95	P43	127	V_{SS}	159	SEG54
32	SEG21	64	K02	96	R00	128	V_{D2}	160	SEG53

N.C. : No Connection

■ PIN DESCRIPTION

Pin name	Pin No.	In/Out	Function
V_{DD}	121	–	Power (+) supply pin
V_{SS}	127	–	Power (-) supply pin
V_{D1}	124	–	Regulated voltage output pin for oscillation/internal logic
V_{D2}	128	–	Boosting/reducing power supply output pin
V_{C1}–V_{C5}	129–133	–	LCD power supply pins, 1/4 bias generated internally, 1/5 bias impressed externally (mask option)
V_{REF}	120	O	LCD power supply test pin
CA–CF	141–136	–	Capacitor connection pins for LCD booster
CG, CH	135, 134	–	Capacitor connection pins for boosting/reducing power supply
OSC1	126	I	Crystal osciration input pin
OSC2	125	O	Crystal oscillation output pin
OSC3	123	I	Ceramic or CR oscillation input pin (selected by mask option)
OSC4	122	O	Ceramic or CR oscillation output pin (selected by mask option)
K00–K03	62–65	I	Input pins
K10–K13	66–69	I	Input pins
P00–P03	70–73	I/O	I/O pins (Switching to external data bus D00–D03 is possible by software)
P10–P13	74–77	I/O	I/O pins (Switching to external data bus D04–D07 is possible by software)
P20–P23	84–87	I/O	I/O pins (Switching to chip select $\overline{CS0}$–$\overline{CS3}$ outputs is possible by software)
P30–P33	88–91	I/O	I/O pins (Switching to special output is possible by software: P30/CR, P31/FR, P32/PTOVF, P33/FOUT)
P40–P43	92–95	I/O	I/O pins (Switching to serial I/F input/output is possible by software)
R00–R03	96–99	O	Output pins (Switching to external address bus A00–A03 is possible by software)
R10–R13	100–103	O	Output pins (Switching to external address bus A04–A07 is possible by software)
R20–R23	104–107	O	Output pins (Switching to external address bus A08–A12 is possible by software)
R30–R33	108–111	O	Output pins (Switching to external address bus A13–A15 is possible by software)
R40	112	O	Output pin (Switching to A16 or $\overline{WR}$ output is posible by software)
R41–R43	113–115	O	Output pins (Switching to special output is possible by software: R41/$\overline{RD}$, R42/$\overline{BZ}$, R43/BZ)
COM0–COM15	142–149, 61–54	O	LCD common output pins (1/8 or 1/16 duty can be selected by software)
SEG0–SEG63	53–1, 160–150	O	LCD segment output pins
$\overline{RESET}$	119	I	Initial reset input pin
$\overline{TEST}$	118	I	Test input pin (connect to V_{DD} in normal operation)

■ ELECTRICAL CHARACTERISTICS

● Absolute Maximum Ratings

(V_{SS}=0V)

Rating	Symbol	Value	Unit
Supply voltage	V_{DD}	-0.5 to 7.0	V
Input voltage (1)	V_I	-0.5 to V_{DD} + 0.3	V
Input voltage (2)	V_{IOSC}	-0.5 to V_{D1} + 0.3	V
Permissible total output current *1	ΣI_{VDD}	10	mA
Operating temperature	Topr	-20 to 70	°C
Storage temperature	Tstg	-65 to 150	°C
Soldering temperature / Time	Tsol	260°C, 10sec (lead section)	–
Allowable dissipation *2	P_D	250	mW

*1 The permissible total output current is the sum total of the current (average current) that simultaneously flows from the output pins (or is drawn in).

*2 In case of plastic package (QFP8-160pin).

● Recommended Operating Conditions

Condition	Symbol	Remark		Min.	Typ.	Max.	Unit
Supply voltage	V_{DD}	V_{SS}=0V	Boost mode (OSC3: OFF)	0.9	1.1	1.25	V
			Boost mode (OSC3: ON *1)	0.9	1.5	2.2	V
			Normal mode (OSC3: OFF)	1.25	3.0	3.6	V
			Normal mode (OSC3: ON *2)	2.2	3.0	3.6	V
			Reduce mode (OSC3: OFF)	2.6	3.0	3.6	V
Oscillation frequency (1)	f_{OSC1}	Any one is selected		–	32.768	–	kHz
				–	38.400	–	kHz
				–	50.000	–	kHz
				–	76.800	–	kHz
Oscillation frequency (2)	f_{OSC3}	Either one is selected	VDC0, 1 = "1"	50	200	260	kHz
		Duty 50±5%	VDC0, 1 = "2" or "3"	50	1,000	1,200	kHz

*1 1MHz oscillation cannot be performed.

*2 200kHz or 1MHz oscillation can be performed.

● DC Characteristics

(Unless otherwise specified, the values listed below are standard values under the following conditions:
V_{DD}=1.5/3.0V, V_{SS}=0V, f_{OSC1}=32.768kHz, Ta=25°C, V_{D1}/V_{C1}/V_{C2}/V_{C4}/V_{C5} are internal voltage, C1–C8=0.2µF, C9–C10=0.4µF)

Characteristic	Symbol	Condition			Min.	Typ.	Max.	Unit
High level input voltage (1)	V_{IH1}		K00–03•10–13, P00–03•10–13 P20–23•30–33•40–43		0.8•V_{DD}		V_{DD}	V
High level input voltage (2)	V_{IH2}		$\overline{RESET}$, $\overline{TEST}$		0.9•V_{DD}		V_{DD}	V
Low level input voltage (1)	V_{IL1}		K00–03•10–13, P00–03•10–13 P20–23•30–33•40–43		0		0.2•V_{DD}	V
Low level input voltage (2)	V_{IL2}		$\overline{RESET}$, $\overline{TEST}$		0		0.1•V_{DD}	V
High level input current	I_{IH}	V_{IH}=1.5V, 3.0V	K00–03•10–13, P00–03•10–13 P20–23•30–33•40–43 $\overline{RESET}$, $\overline{TEST}$		0		0.5	µA
Low level input current (1)	I_{IL1}	V_{IL1}=V_{SS} Without pull up resistor	K00–03•10–13, P00–03•10–13 P20–23•30–33•40–43 $\overline{RESET}$, $\overline{TEST}$		-0.5		0	µA
Low level input current (2)	I_{IL2}	V_{IL2}=V_{SS} With pull up resistor	K00–03•10–13, P00–03•10–13 P20–23•30–33•40–43 $\overline{RESET}$, $\overline{TEST}$	V_{DD}= 1.5V	-8	-5	-3	µA
				3.0V	-16	-10	-6	µA
High level output current	I_{OH1}	V_{OH1}=0.9•V_{DD}	R00–03•10–13•20–23•30–33 R40–43, P00–03•10–13•20–23 P30–33•40–43	V_{DD}= 1.5V			0.3	mA
				3.0V			-1.5	mA
Low level output current	I_{OL1}	V_{OL1}=0.1•V_{DD}	R00–03•10–13•20–23•30–33 R40–43, P00–03•10–13•20–23 P30–33•40–43	V_{DD}= 1.5V	0.7			mA
				3.0V	6			mA
Common output current	I_{OH2}	V_{OH2}=V_{C5}-0.05V	COM0–15				-30	µA
	I_{OL2}	V_{OL2}=V_{SS}+0.05V			30			µA
Segment output current	I_{OH3}	V_{OH3}=V_{C5}-0.05V	SEG0–63				-10	µA
	I_{OL3}	V_{OL3}=V_{SS}+0.05V			10			µA

● Analog Circuit Characteristics and Current Consumption

(Unless otherwise specified, the values listed below are standard values under the following conditions: V_{DD}=1.5V / when V_{C1} standard is selected, V_{DD}=3.0V / when V_{C2} standard is selected, V_{SS}=0V, f_{OSC1}=32.768kHz, C_G=25pF, Ta=25°C, V_{D1}/V_{C1}/V_{C2}/V_{C4}/V_{C5} are internal voltage, C1–C8=0.2µF, C9–C10=0.4µF)

Characteristic	Symbol	Condition		Min.	Typ.	Max.	Unit
LCD drive voltage (when V_{C1} standard is selected)	V_{C1}	Connect 1MΩ load resistor between V_{SS} and V_{C1} (without panel load) V_{DD}=1.5V	LC0–3="0"	Typ.×0.88	0.975	Typ.×1.12	V
			LC0–3="1"		0.990		
			LC0–3="2"		1.005		
			LC0–3="3"		1.020		
			LC0–3="4"		1.035		
			LC0–3="5"		1.050		
			LC0–3="6"		1.065		
			LC0–3="7"		1.080		
			LC0–3="8"		1.095		
			LC0–3="9"		1.110		
			LC0–3="10"		1.125		
			LC0–3="11"		1.140		
			LC0–3="12"		1.155		
			LC0–3="13"		1.170		
			LC0–3="14"		1.185		
			LC0–3="15"		1.200		
	V_{C2}	Connect 1MΩ load resistor between V_{SS} and V_{C2} (without panel load)		2•V_{C1}		2•V_{C1} ×0.9	V
	V_{C4}	Connect 1MΩ load resistor between V_{SS} and V_{C4} (without panel load)		3•V_{C1}		3•V_{C1} ×0.9	V
	V_{C5}	Connect 1MΩ load resistor between V_{SS} and V_{C5} (without panel load)		4•V_{C1}		4•V_{C1} ×0.9	V
LCD drive voltage (when V_{C2} standard is selected)	V_{C1}	Connect 1MΩ load resistor between V_{SS} and V_{C1} (without panel load)		1/2•V_{C2} -0.1		1/2•V_{C2} ×0.95	V
	V_{C2}	Connect 1MΩ load resistor between V_{SS} and V_{C2} (without panel load) V_{DD}=3.0V	LC0–3="0"	Typ.×0.88	1.95	Typ.×1.12	V
			LC0–3="1"		1.98		
			LC0–3="2"		2.01		
			LC0–3="3"		2.04		
			LC0–3="4"		2.07		
			LC0–3="5"		2.10		
			LC0–3="6"		2.13		
			LC0–3="7"		2.16		
			LC0–3="8"		2.19		
			LC0–3="9"		2.22		
			LC0–3="10"		2.25		
			LC0–3="11"		2.28		
			LC0–3="12"		2.31		
			LC0–3="13"		2.34		
			LC0–3="14"		2.37		
			LC0–3="15"		2.40		
	V_{C4}	Connect 1MΩ load resistor between V_{SS} and V_{C4} (without panel load)		3/2•V_{C2}		3/2•V_{C2} ×0.95	V
	V_{C5}	Connect 1MΩ load resistor between V_{SS} and V_{C5} (without panel load)		2•V_{C2}		2•V_{C2} ×0.95	V

(Unless otherwise specified, the values listed below are standard values under the following conditions:
V_{DD}=3.0V, V_{SS}=0V, f_{OSC1}=32.768kHz, C_G=25pF, Ta=25°C, V_{D1}/V_{C1}/V_{C2}/V_{C4}/V_{C5} are internal voltage, C1–C8=0.2µF, C9–C10=0.4µF)

Characteristic	Symbol	Condition		Min.	Typ.	Max.	Unit
SVD voltage	V_{SVD}	SVDS0–3="0"		0.95	1.05	1.15	V
		SVDS0–3="1"		1.05	1.10	1.15	
		SVDS0–3="2"		1.10	1.15	1.20	
		SVDS0–3="3"		1.15	1.20	1.25	
		SVDS0–3="4"		1.20	1.25	1.30	
		SVDS0–3="5"		1.25	1.30	1.35	
		SVDS0–3="6"		1.35	1.40	1.45	
		SVDS0–3="7"		1.55	1.60	1.65	
		SVDS0–3="8"		1.90	1.95	2.00	
		SVDS0–3="9"		1.95	2.00	2.05	
		SVDS0–3="10"		2.00	2.05	2.10	
		SVDS0–3="11"		2.05	2.10	2.15	
		SVDS0–3="12"		2.15	2.20	2.25	
		SVDS0–3="13"		2.25	2.30	2.35	
		SVDS0–3="14"		2.45	2.50	2.55	
		SVDS0–3="15"		2.55	2.60	2.65	
SVD circuit response time	t_{SVD}					100	µsec
Power current consumption	I_{OP}	During HALT Normal mode LCD power OFF	32.768kHz		2.0	4.0	µA
			50.0kHz		2.3	5.0	µA
			76.8kHz		3.0	5.6	µA
		During HALT Normal mode *1 LCD power ON	32.768kHz		6.5	10.0	µA
			50.0kHz		8.0	14.0	µA
			76.8kHz		11.0	18.0	µA
		During HALT Boost mode *1 V_{DD}=1.2V, LCD power ON	32.768kHz		13.5	25.0	µA
			50.0kHz		16.0	30.0	µA
			76.8kHz		22.0	38.0	µA
		During HALT Reduce mode *1 V_{DD}=3.0V, LCD power ON	32.768kHz		5.0	8.0	µA
			50.0kHz		6.5	11.0	µA
			76.8kHz		9.0	14.0	µA
		During execution Normal mode *1 LCD power ON	32.768kHz		10.0	18.0	µA
			50.0kHz		13.0	24.0	µA
			76.8kHz		19.0	32.0	µA
			200kHz(CR oscillation)		40	100	µA
			870kHz(CR oscillation)		330	600	µA
			1MHz(Ceramic oscillation)		300	500	µA
		During execution Boost mode *1 V_{DD}=1.2V, LCD power ON	32.768kHz		20.0	36.0	µA
			50.0kHz		26.0	48.0	µA
			76.8kHz		37.0	64.0	µA
			200kHz(CR oscillation)		80	200	µA
		During execution Reduce mode *1 V_{DD}= 3.0V, LCD power ON	32.768kHz		7.0	14.0	µA
			50.0kHz		10.0	18.0	µA
			76.8kHz		14.0	25.0	µA

*1 Without panel load. The SVD circuit is turned OFF.

● Oscillation Characteristics

The oscillation characteristics change depending on the conditions (components used, board pattern, etc.). Use the following characteristics as reference values.

OSC1 crystal oscillation circuit

(Unless otherwise specified, the values listed below are standard values under the following conditions:
V_{DD}=3.0V, V_{SS}=0V, f_{OSC1}=32.768kHz, C_G=25pF, C_D=built-in, Ta=25°C)

Characteristic	Symbol	Condition		Min.	Typ.	Max.	Unit
Oscillation start voltage	Vsta	tsta≤3sec (V_{DD})		1.1			V
Oscillation stop voltage	Vstp	tstp≤10sec (V_{DD})	Normal mode	1.1			V
			Boost mode	0.9			V
Built-in capacitance (drain)	C_D	Including the parasitic capacitance inside the IC (in chip)			14		pF
Frequency/voltage deviation	f/V	V_{DD}=0.9 to 3.6V	with VDC switching			5	ppm
			without VDC switching			10	ppm
Frequency/IC deviation	f/IC			-10		10	ppm
Frequency adjustment range	f/C_G	C_G=5 to 25pF	32.768, 38.4, 50kHz	35	45		ppm
			76.8kHz	25	35		ppm
Harmonic oscillation start voltage	Vhho	C_G=5pF (V_{DD})		3.6			V
Permitted leak resistance	Rleak	Between OSC1 and V_{DD}, V_{SS}		200			MΩ

OSC3 CR oscillation circuit 1 (200kHz)

(Unless otherwise specified, the values listed below are standard values under the following conditions:
V_{DD}=3.0V, V_{SS}=0V, R_{CR}=160kΩ, Ta=25°C)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation frequency dispersion	f_{OSC3}		-30	200kHz	30	%
Oscillation start voltage	Vsta	Normal mode (V_{DD})	2.2(0.9)*1			V
Oscillation start time	tsta	V_{DD}=2.2 to 3.6V			3	msec
Oscillation stop voltage	Vstp	Normal mode (V_{DD})	2.2(0.9)*1			V

*1 Items enclosed in parentheses ( ) is those used in the boost mode.

OSC3 CR oscillation circuit 2 (1MHz)

(Unless otherwise specified, the values listed below are standard values under the following conditions:
V_{DD}=3.0V, V_{SS}=0V, R_{CR}=33kΩ, Ta=25°C)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation frequency dispersion	f_{OSC3}		-30	870kHz	30	%
Oscillation start voltage	Vsta	Normal mode (V_{DD})	2.2			V
Oscillation start time	tsta	V_{DD}=2.2 to 3.6V			3	msec
Oscillation stop voltage	Vstp	Normal mode (V_{DD})	2.2			V

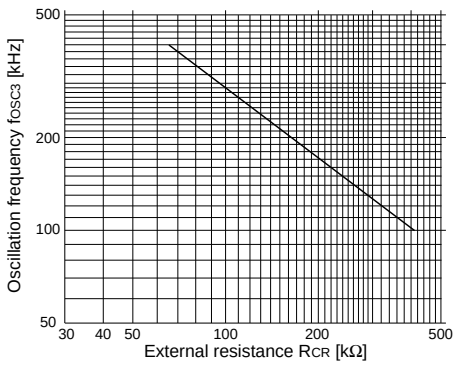
OSC3 ceramic oscillation circuit (1MHz)

(Unless otherwise specified, the values listed below are standard values under the following conditions:
V_{DD}=3.0V, V_{SS}=0V, Ceramic oscillator: 1MHz, C_{GC}=C_{DC}=100pF, Ta=25°C)

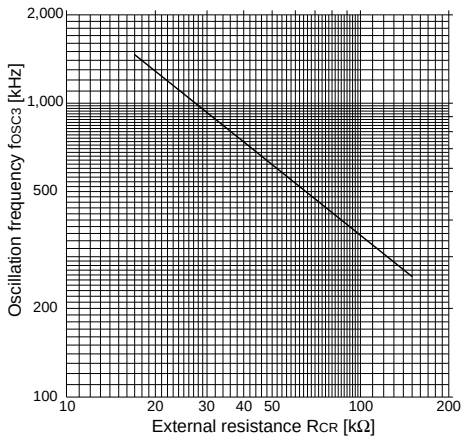
Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start voltage	Vsta	Normal mode (V_{DD})	2.2			V
Oscillation start time	tsta	V_{DD}=2.2 to 3.6V			5	msec
Oscillation stop voltage	Vstp	Normal mode (V_{DD})	2.2			V

CR oscillation frequency - resistance characteristics

<200kHz>



<1MHz>



● External Memory Access AC Characteristics

Read cycle

• During 32kHz (OSC1) operation

(Condition: V_{DD}=1.5V, V_{SS}=0V, Ta=25°C, V_{IH}=0.8V_{DD}, V_{IL}=0.2V_{DD}, V_{OH}=0.8V_{DD}, V_{OL}=0.2V_{DD}, C_L=100pF [load capacitance])

Characteristic	Symbol	Min.	Typ.	Max.	Unit
$\overline{CSx}$ set-up time in read cycle	tras	0.15 × tc			µsec
$\overline{CSx}$ hold time in read cycle	trah	0			µsec
$\overline{RD}$ set-up time in read cycle	trds	0.15 × tc			µsec
$\overline{RD}$ hold time in read cycle	trdh	0			µsec

• During 1MHz (OSC3) operation

(Condition: V_{DD}=3.0V, V_{SS}=0V, Ta=25°C, V_{IH}=0.8V_{DD}, V_{IL}=0.2V_{DD}, V_{OH}=0.8V_{DD}, V_{OL}=0.2V_{DD}, C_L=100pF [load capacitance])

Characteristic	Symbol	Min.	Typ.	Max.	Unit
$\overline{CSx}$ set-up time in read cycle	tras	0.15 × tc			nsec
$\overline{CSx}$ hold time in read cycle	trah	0			nsec
$\overline{RD}$ set-up time in read cycle	trds	0.15 × tc			nsec
$\overline{RD}$ hold time in read cycle	trdh	0			nsec

Write cycle

• During 32kHz (OSC1) operation

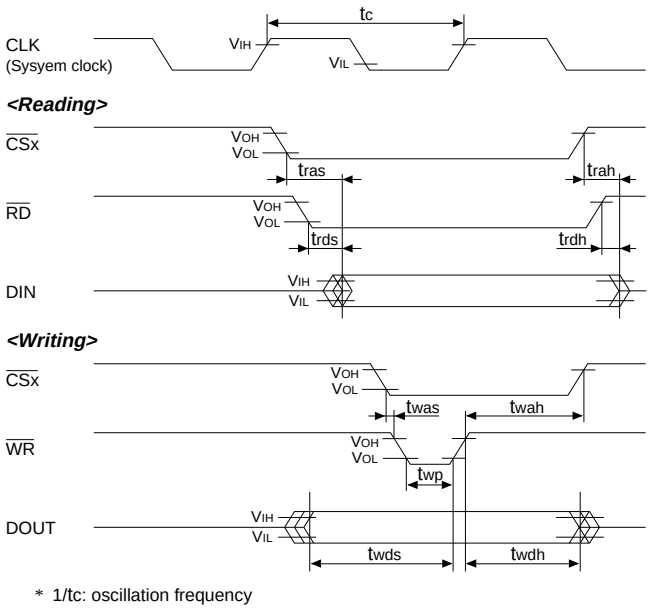
(Condition: V_{DD}=1.5V, V_{SS}=0V, Ta=25°C, V_{IH}=0.8V_{DD}, V_{IL}=0.2V_{DD}, V_{OH}=0.8V_{DD}, V_{OL}=0.2V_{DD}, C_L=100pF [load capacitance])

Characteristic	Symbol	Min.	Typ.	Max.	Unit
Address set-up time in write cycle	twas	0			µsec
Address hold time in write cycle	twah	5			µsec
Write signal pulse width	twp	5			µsec
Data output set-up time in write cycle	twds	5			µsec
Data output hold time in write cycle	twdh	5		30	µsec

• During 1MHz (OSC3) operation

(Condition: V_{DD}=3.0V, V_{SS}=0V, Ta=25°C, V_{IH}=0.8V_{DD}, V_{IL}=0.2V_{DD}, V_{OH}=0.8V_{DD}, V_{OL}=0.2V_{DD}, C_L=100pF [load capacitance])

Characteristic	Symbol	Min.	Typ.	Max.	Unit
Address set-up time in write cycle	twas	0			nsec
Address hold time in write cycle	twah	200			nsec
Write signal pulse width	twp	200			nsec
Data output set-up time in write cycle	twds	200			nsec
Data output hold time in write cycle	twdh	200		1,500	nsec



* 1/tc: oscillation frequency

● Serial Interface AC Characteristics

Clock synchronous master mode

• During 32kHz (OSC1) operation

(Condition: V_{DD}=1.5V, V_{SS}=0V, Ta=25°C, V_{IH1}=0.8V_{DD}, V_{IL1}=0.2V_{DD}, V_{OH}=0.8V_{DD}, V_{OL}=0.2V_{DD})

Characteristic	Symbol	Min.	Typ.	Max.	Unit
Transmitting data output delay time	tsmd			5	µsec
Receiving data input set-up time	tsms	10			µsec
Receiving data input hold time	tsmh	5			µsec

• During 1MHz (OSC3) operation

(Condition: V_{DD}=3.0V, V_{SS}=0V, Ta=25°C, V_{IH1}=0.8V_{DD}, V_{IL1}=0.2V_{DD}, V_{OH}=0.8V_{DD}, V_{OL}=0.2V_{DD})

Characteristic	Symbol	Min.	Typ.	Max.	Unit
Transmitting data output delay time	tsmd			200	nsec
Receiving data input set-up time	tsms	400			nsec
Receiving data input hold time	tsmh	200			nsec

Clock synchronous slave mode

• During 32kHz (OSC1) operation

(Condition: V_{DD}=1.5V, V_{SS}=0V, Ta=25°C, V_{IH1}=0.8V_{DD}, V_{IL1}=0.2V_{DD}, V_{OH}=0.8V_{DD}, V_{OL}=0.2V_{DD})

Characteristic	Symbol	Min.	Typ.	Max.	Unit
Transmitting data output delay time	tsmd			10	µsec
Receiving data input set-up time	tsms	10			µsec
Receiving data input hold time	tsmh	5			µsec

• During 1MHz (OSC3) operation

(Condition: V_{DD}=3.0V, V_{SS}=0V, Ta=25°C, V_{IH1}=0.8V_{DD}, V_{IL1}=0.2V_{DD}, V_{OH}=0.8V_{DD}, V_{OL}=0.2V_{DD})

Characteristic	Symbol	Min.	Typ.	Max.	Unit
Transmitting data output delay time	tsmd			500	nsec
Receiving data input set-up time	tsms	400			nsec
Receiving data input hold time	tsmh	200			nsec

Asynchronous mode

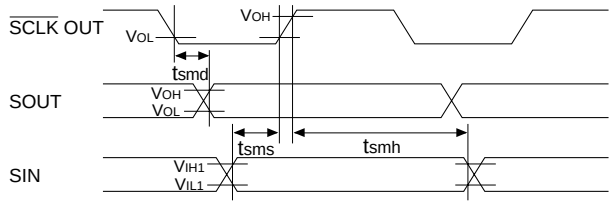
(Condition: V_{DD}=1.5V, V_{SS}=0V, Ta=25°C)

Characteristic	Symbol	Min.	Typ.	Max.	Unit
Start bit detection error time *1	t_{sa1}	0		t/16	sec
Erroneous start bit detection range time *2	t_{sa2}	9t/16		10t/16	sec

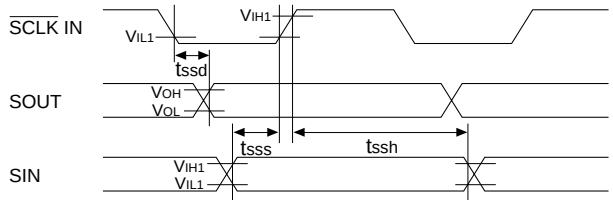
*1 Start bit detection error time is a logical delay time from inputting the start bit until internal sampling begins operating. (Time as far as AC is excluded.)

*2 Erroneous start bit detection range time is a logical range to detect whether a LOW level (start bit) has been input again after a start bit has been detected and the internal sampling clock has started. When a HIGH level is detected, the start bit detection circuit is reset and goes into a wait status until the next start bit. (Time as far as AC is excluded.)

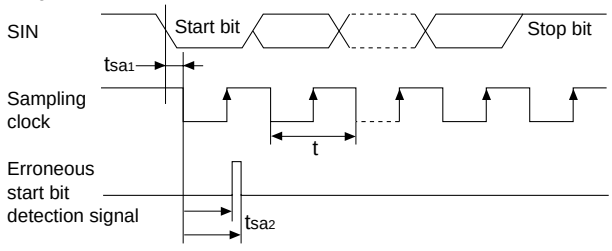
<Clock synchronous master mode>



<Clock synchronous slave mode>

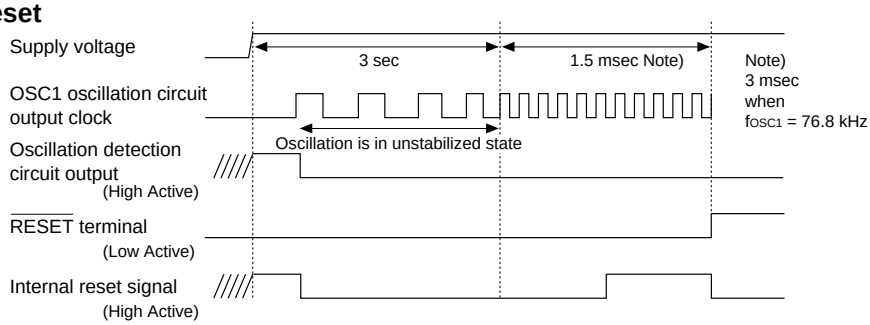


<Asynchronous mode>

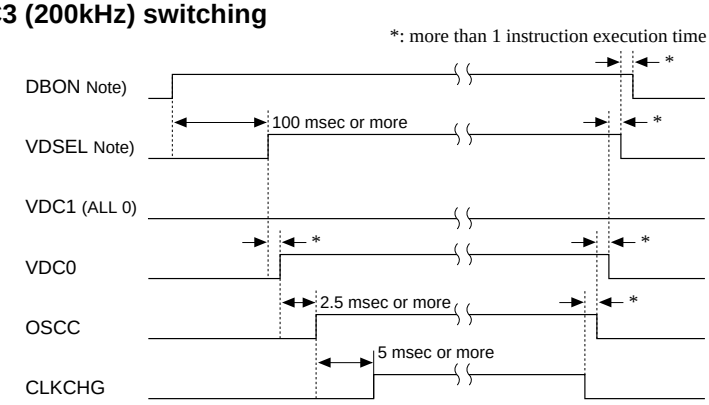


● Timing Chart

1. Initial reset

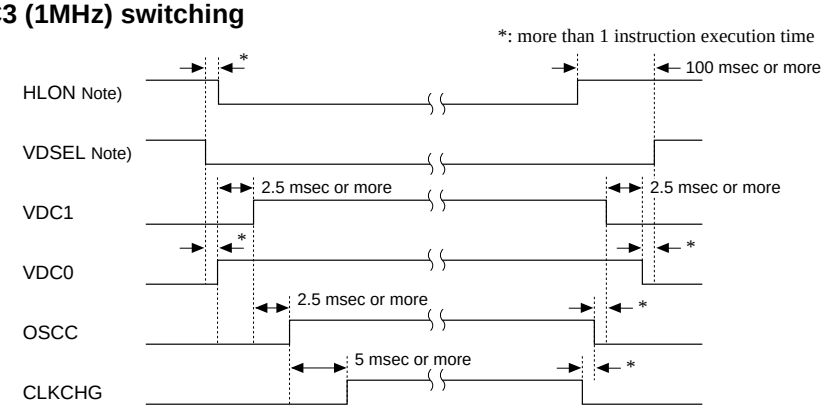


2. OSC1↔OSC3 (200kHz) switching



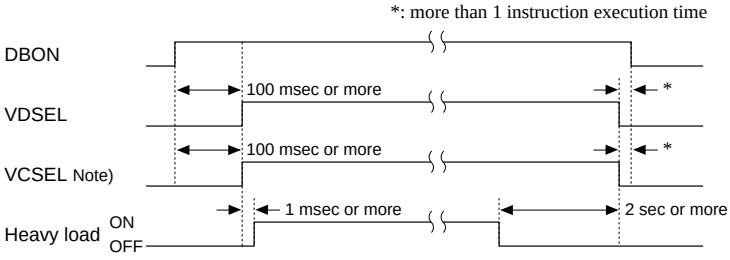
Note) Use DBON and VDSEL only when changes are required.

3. OSC1↔OSC3 (1MHz) switching



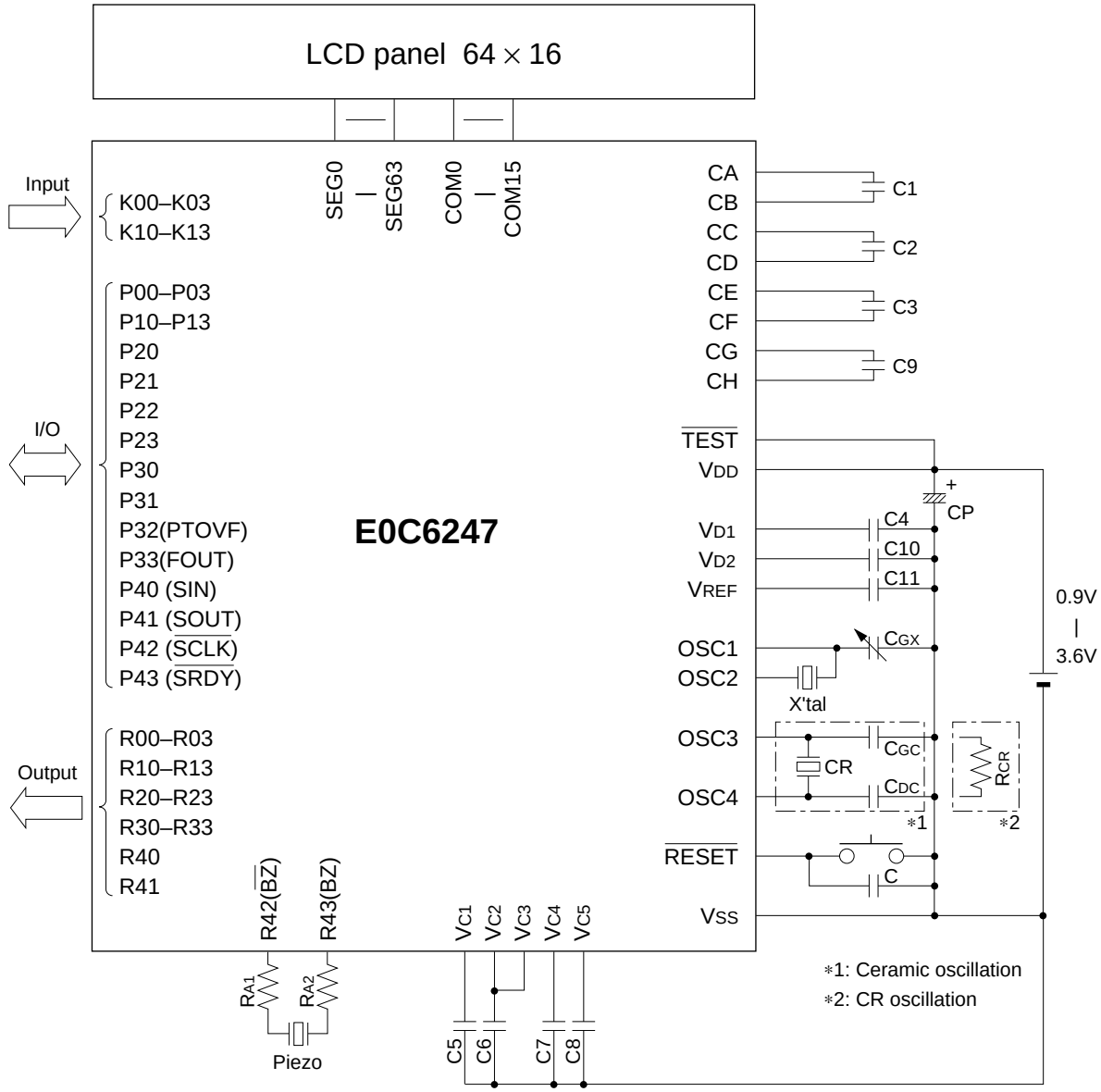
Note) When the reduce mode is used. However, when using the reduce mode in the LCD system voltage circuit (VCSEL = "1"), HLON should be set to "1".

4. Boost mode setting when driving heavy load



Note) VCSEL is used only when it is required.

■ BASIC EXTERNAL CONNECTION DIAGRAM

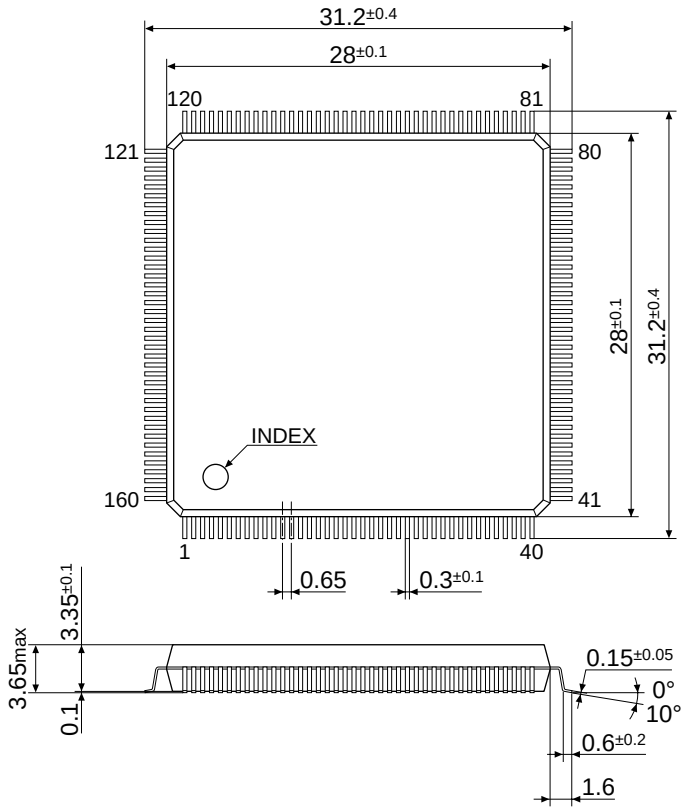


X'tal	Crystal oscillator	32.768kHz / 38.4kHz / 50.0kHz / 76.8kHz, CI (Max.) = 35kΩ
C_{GX}	Trimmer capacitor	5–25pF
CR	Ceramic oscillator	1MHz (3.0V)
C_{GC}	Gate capacitor	100pF
C_{DC}	Drain capacitor	100pF
R_{CR}	Resistor for CR oscillation	160kΩ (200kHz), 33kΩ (1MHz)
R_{A1}, R_{A2}	Protection resistors	100Ω
C1–C8	Capacitors	0.2µF
C9, C10	Capacitors	0.4µF
C11	Capacitor	0.1µF
CP	Capacitor	3.3µF

Note: The above table is simply an example, and is not guaranteed to work.

■ PACKAGE DIMENSIONS

Plastic QFP8-160pin



Unit: mm

NOTICE

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