EPSON

E0C6251

4-bit Single Chip Microcomputer

Low Voltage Operation Products

- Core CPU Architecture
- SVD Circuit
- R/F Converter for Temperature Measuring
- High Quality Display LCD Driver

■ DESCRIPTION

The E0C6251 is a single-chip microcomputer made up of the 4-bit core CPU E0C6200A, ROM, RAM, LCD driver, input ports, output ports, I/O ports, clock timer and A/D converter (R/F conversion type). Because of its low-voltage operation and low power consumption, this series is ideal for a wide range of applications, and is especially suitable for battery-driven systems.

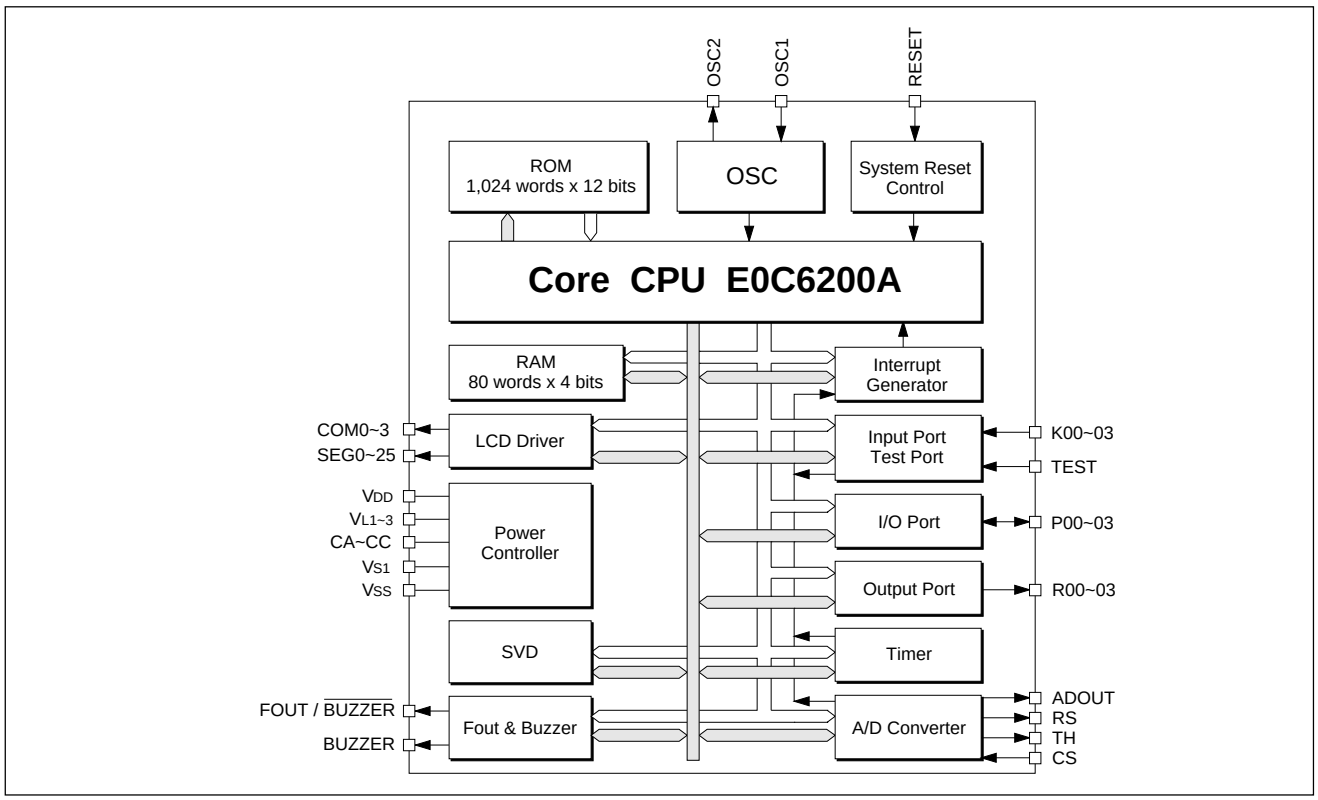
■ FEATURES

- CMOS LSI 4-bit parallel processing
- Clock ..... 32.768kHz (Typ.) (Crystal or CR oscillation)
- Instruction set ..... 100 instructions
- Instruction execution time ..... 153µsec, 214µsec, 366µsec (depending on instruction)
- ROM capacity ..... 1,024 × 12 bits
- RAM capacity ..... 80 × 4 bits
- Input port ..... 4 bits (pull-down resistors are available by mask option)
- Output port ..... 4 bits (common, BZ, $\overline{BZ}$, FOUT and LAMP ports are available by mask option)
- I/O port ..... 4 bits
- Large capacity output port ..... 2 bits
- Buzzer output port ..... 2 bits
- Clock output port ..... 1 bit
- A/D converter ..... R/F (resistance/frequency) conversion type, 1ch.
- LCD driver ..... 26 segments × 2/3/4 commons (Power regulator built-in. DC output available. Selected duty by software setting)
- R/F converter circuit ..... Temperature measurement is possible with the R/F converter in which a external thermistor. Range of temperature measurement and accuracy of temperature measurement changed by thermistor.
- Built-in supply voltage detection (SVD) circuit ..... 1ch.
- Timer ..... Clock timer : 1ch.
- Interrupts ..... External : Input interrupt 1 line
  Internal : Timer interrupt 1 line
  R/F converter interrupt 1 line
- Supply voltage ..... 1.5V (0.9 to 2.0V min. 1.0V: Measurement temperature mode)
  3.0V (1.8 to 3.5V)
- Current consumption ..... HALT mode : 1.0µA (Typ.)
  : 2.5µA (Typ.)
  OPERATING mode : 2.5µA (Typ.)
  : 5.0µA (Typ.)
- Package ..... QFP6-60pin (ceramic), QFP6-64pin (plastic)
  Die form

■ LINE UP

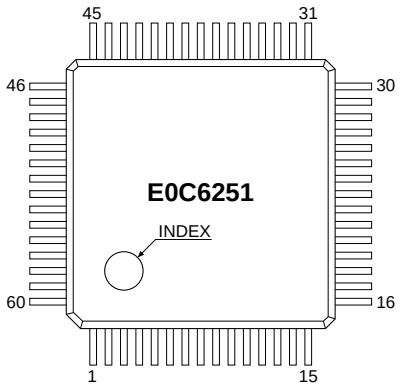
Model	Operating voltage	Clock
E0C62L51	0.9V to 2.0V	32.768kHz (Crystal or CR oscillation)
E0C6251	1.8V to 3.5V	32.768kHz (Crystal or CR oscillation)

■ BLOCK DIAGRAM



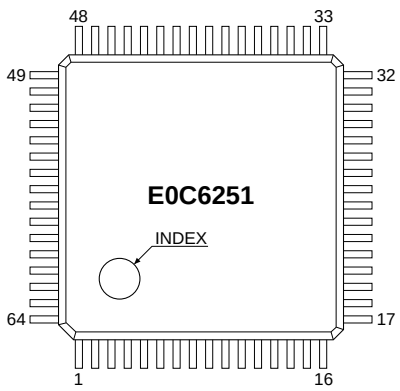
■ PIN CONFIGURATION

QFP6-60pin (ceramic)



No.	Pin name	No.	Pin name	No.	Pin name	No.	Pin name
1	COM3	16	SEG13	31	P00	46	TH
2	SEG0	17	SEG14	32	P01	47	ADOUT
3	SEG1	18	SEG15	33	P02	48	V_{DD}
4	SEG2	19	SEG16	34	P03	49	OSC1
5	SEG3	20	SEG17	35	RESET	50	OSC2
6	SEG4	21	SEG18	36	K00	51	V_{SS}
7	SEG5	22	SEG19	37	K01	52	CA
8	SEG6	23	SEG20	38	K02	53	CB
9	SEG7	24	SEG21	39	K03	54	CC
10	SEG8	25	SEG22	40	R00	55	V_{L1}
11	SEG9	26	SEG23	41	R01	56	V_{L2}
12	SEG10	27	SEG24	42	R02	57	V_{L3}
13	SEG11	28	SEG25	43	R03	58	COM0
14	SEG12	29	V_{DD}	44	CS	59	COM1
15	TEST	30	V_{S1}	45	RS	60	COM2

QFP6-64in (plastic)



No.	Pin name	No.	Pin name	No.	Pin name	No.	Pin name
1	COM2	17	TEST	33	P00	49	CS
2	COM3	18	SEG13	34	P01	50	RS
3	N.C.	19	SEG14	35	P02	51	TH
4	SEG0	20	SEG15	36	P03	52	ADOUT
5	SEG1	21	SEG16	37	RESET	53	V_{DD}
6	SEG2	22	SEG17	38	K00	54	OSC1
7	SEG3	23	SEG18	39	K01	55	OSC2
8	SEG4	24	SEG19	40	K02	56	V_{SS}
9	SEG5	25	SEG20	41	K03	57	CA
10	SEG6	26	SEG21	42	R00	58	CB
11	SEG7	27	SEG22	43	R01	59	CC
12	SEG8	28	SEG23	44	R02	60	V_{L1}
13	SEG9	29	SEG24	45	R03	61	V_{L2}
14	SEG10	30	SEG25	46	N.C.	62	V_{L3}
15	SEG11	31	V_{DD}	47	N.C.	63	COM0
16	SEG12	32	V_{S1}	48	N.C.	64	COM1

N.C. = No Connection

■ PIN DESCRIPTION

Pin name	Pin No.		In/Out	Function
	QFP6-60pin	QFP6-64pin		
V_{DD}	29, 48	31, 53	I	Power source (+) terminal
V_{SS}	51	56	I	Power source (-) terminal
V_{S1}	30	32	O	Oscillation and internal logic system regulated voltage output terminal
V_{L1}	55	60	O	LCD system regulated voltage output terminal (approx. -1.05 V)
V_{L2}	56	61	O	LCD system booster output terminal (V_{L1} x 2)
V_{L3}	57	62	O	LCD system booster output terminal (V_{L1} x 3)
CA–CC	52–54	57–59	–	Booster capacitor connecting terminal
OSC1	49	54	I	Crystal or CR oscillation input terminal
OSC2	50	55	O	Crystal or CR oscillation output terminal
K00–K03	36–39	38–41	I	Input terminal
P00–P03	31–34	33–36	I/O	I/O terminal
R00–R03	40–43	42–45	O	Output terminal
SEG0–25	2–14, 16–28	4–16, 18–30	O	LCD segment output terminal (Convertible to DC output by mask option)
COM0–3	58–60, 1	63, 64, 1, 2	O	LCD common output terminal
CS	44	49	I	A/D converter CR oscillation input terminal
RS	45	50	O	A/D converter CR oscillation output terminal
TH	46	51	O	A/D converter CR oscillation output terminal
ADOUT	47	52	O	A/D converter oscillation frequency output terminal
RESET	35	37	I	Initial reset input terminal
TEST	15	17	I	Test input terminal

■ ELECTRICAL CHARACTERISTICS

● Absolute Maximum Ratings

(V_{DD}=0V)

Rating	Symbol	Value	Unit
Supply voltage	V_{SS}	-5.0 to 0.5	V
Input voltage (1)	V_I	V_{SS} - 0.3 to 0.5	V
Input voltage (2)	V_{IOSC}	V_{SS} - 0.3 to 0.5	V
Operating temperature	Topr	-20 to 70	°C
Storage temperature	Tstg	-65 to 150	°C
Soldering temperature / Time	Tsol	260°C, 10sec (lead section)	–
Permissible dissipation *1	P_D	250	mW

*1: In case of plastic package (QFP6-64pin).

● Recommended Operating Conditions

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(Ta=-20 to 70°C)

Condition	Symbol	Remark	Min.	Typ.	Max.	Unit
Supply voltage	V_{SS}	V_{DD}=0V	-3.5	-3.0	-1.8	V
Oscillation frequency	f_{OSC1}	Crystal oscillation		32.768		kHz
	f_{OSC2}	CR oscillation, R=420kΩ		65	80	kHz
Booster capacitor (1)	C1		0.1			µF
Booster capacitor (2)	C2		0.1			µF
Capacitor between V_{DD} and V_{L1}	C3		0.1			µF
Capacitor between V_{DD} and V_{L2}	C4		0.1			µF
Capacitor between V_{DD} and V_{L3}	C5		0.1			µF
Capacitor between V_{DD} and V_{S1}	C6		0.1			µF

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(Ta=-20 to 70°C)

Condition	Symbol	Remark	Min.	Typ.	Max.	Unit
Supply voltage	V_{SS}	V_{DD}=0V *3	-2.0	-1.5	-1.1	V
		V_{DD}=0V, With software control *1	-2.0	-1.5	-0.9 *2	V
Oscillation frequency	f_{OSC1}	Crystal oscillation		32.768		kHz
	f_{OSC2}	CR oscillation, R=420kΩ		65	80	kHz
Booster capacitor (1)	C1		0.1			µF
Booster capacitor (2)	C2		0.1			µF
Capacitor between V_{DD} and V_{L1}	C3		0.1			µF
Capacitor between V_{DD} and V_{L2}	C4		0.1			µF
Capacitor between V_{DD} and V_{L3}	C5		0.1			µF
Capacitor between V_{DD} and V_{S1}	C6		0.1			µF

*1: When the heavy load protection mode is set by software and the SVD circuit is turned off.
*2: The voltage which can be displayed on the LCD panel will differ according to the characteristics of the LCD panel.
*3: When there is no software control during CR oscillation or crystal oscillation.

● DC Characteristics

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(Unless otherwise specified: V_{DD}=0V, V_{SS}=-3.0V, f_{OSC}=32.768kHz, Ta=25°C, V_{S1}/V_{L1}–V_{L3} are internal voltage, C1–C6=0.1µF)

Characteristic	Symbol	Condition		Min.	Typ.	Max.	Unit
High level input voltage (1)	V_{IH1}		K00–K03, P00–P03	0.2•V_{SS}		0	V
High level input voltage (2)	V_{IH2}		RESET, TEST	0.15•V_{SS}		0	V
Low level input voltage (1)	V_{IL1}		K00–K03, P00–P03	V_{SS}		0.8•V_{SS}	V
Low level input voltage (2)	V_{IL2}		RESET, TEST	V_{SS}		0.85•V_{SS}	V
High level input current (1)	I_{IH1}	V_{IH1}=0V, No pull down resistor	K00–K03, P00–P03	0		0.5	µA
High level input current (2)	I_{IH2}	V_{IH2}=0V, With pull down resistor	K00–K03	5		16	µA
High level input current (3)	I_{IH3}	V_{IH3}=0V, With pull down resistor	P00–P03 RESET, TEST	30		100	µA
Low level input current	I_{IL}	V_{IL}=V_{SS}	K00–K03, P00–P03 RESET, TEST	-0.5		0	µA
High level output current (1)	I_{OH1}	V_{OH1}=0.1•V_{SS}	R02, R03, P00–P03			-1.0	mA
High level output current (2)	I_{OH2}	V_{OH2}=0.1•V_{SS} (built-in protection resistance)	R00, R01			-1.0	mA
High level output current (3)	I_{OH3}	V_{OH3}=-1.0V	ADOUT	-100		-10	µA
Low level output current (1)	I_{OL1}	V_{OL1}=0.9•V_{SS}	R02, R03, P00–P03	3.0			mA
Low level output current (2)	I_{OL2}	V_{OL2}=0.9•V_{SS} (built-in protection resistance)	R00, R01	3.0			mA
Low level output current (3)	I_{OL3}	V_{OL3}=-2.0V	ADOUT	10		100	µA
Common output current	I_{OH4}	V_{OH4}=-0.05V	COM0–COM3			-3	µA
	I_{OL4}	V_{OL4}=V_{L3}+0.05V		3			µA
Segment output current	I_{OH5}	V_{OH5}=-0.05V	SEG0–SEG25			-3	µA
(during LCD output)	I_{OL5}	V_{OL5}=V_{L3}+0.05V		3			µA
Segment output current	I_{OH6}	V_{OH6}=0.1•V_{SS}	SEG0–SEG25			-300	µA
(during DC output)	I_{OL6}	V_{OL6}=0.9•V_{SS}		300			µA

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(Unless otherwise specified: V_{DD}=0V, V_{SS}=-1.5V, f_{OSC}=32.768kHz, Ta=25°C, V_{S1}/V_{L1}–V_{L3} are internal voltage, C1–C6=0.1µF)

Characteristic	Symbol	Condition		Min.	Typ.	Max.	Unit
High level input voltage (1)	V_{IH1}		K00–K03, P00–P03	0.2•V_{SS}		0	V
High level input voltage (2)	V_{IH2}		RESET, TEST	0.15•V_{SS}		0	V
Low level input voltage (1)	V_{IL1}		K00–K03, P00–P03	V_{SS}		0.8•V_{SS}	V
Low level input voltage (2)	V_{IL2}		RESET, TEST	V_{SS}		0.85•V_{SS}	V
High level input current (1)	I_{IH1}	V_{IH1}=0V, No pull down resistor	K00–K03, P00–P03	0		0.5	µA
High level input current (2)	I_{IH2}	V_{IH2}=0V, With pull down resistor	K00–K03	2.0		16	µA
High level input current (3)	I_{IH3}	V_{IH3}=0V, With pull down resistor	P00–P03 RESET, TEST	9.0		100	µA
Low level input current	I_{IL}	V_{IL}=V_{SS}	K00–K03, P00–P03 RESET, TEST	-0.5		0	µA
High level output current (1)	I_{OH1}	V_{OH1}=0.1•V_{SS}	R02, R03, P00–P03			-200	µA
High level output current (2)	I_{OH2}	V_{OH2}=0.1•V_{SS} (built-in protection resistance)	R00, R01			-200	µA
High level output current (3)	I_{OH3}	V_{OH3}=-1.0V	ADOUT	-100		-10	µA
Low level output current (1)	I_{OL1}	V_{OL1}=0.9•V_{SS}	R02, R03, P00–P03	700			µA
Low level output current (2)	I_{OL2}	V_{OL2}=0.9•V_{SS} (built-in protection resistance)	R00, R01	700			µA
Low level output current (3)	I_{OL3}	V_{OL3}=-2.0V	ADOUT	10		100	µA
Common output current	I_{OH4}	V_{OH4}=-0.05V	COM0–COM3			-3	µA
	I_{OL4}	V_{OL4}=V_{L3}+0.05V		3			µA
Segment output current	I_{OH5}	V_{OH5}=-0.05V	SEG0–SEG25			-3	µA
(during LCD output)	I_{OL5}	V_{OL5}=V_{L3}+0.05V		3			µA
Segment output current	I_{OH6}	V_{OH6}=0.1•V_{SS}	SEG0–SEG25			-100	µA
(during DC output)	I_{OL6}	V_{OL6}=0.9•V_{SS}		130			µA

● Analog Circuit Characteristics and Current Consumption

E0C6251 (Normal Mode)

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-3.0V, f_{OSC}=32.768kHz, Ta=25°C, C_G=25pF, V_{S1}/V_{L1}–V_{L3} are internal voltage, C1–C6=0.1µF)
(During A/D conversion: RS=49.8kΩ, TH=50kΩ, CS=2,200pF)

Characteristic	Symbol	Condition		Min.	Typ.	Max.	Unit
Internal voltage	V_{L1}	Connect 1MΩ load resistor between V_{DD} and V_{L1} (without panel load)		-1.15	-1.05	-0.95	V
	V_{L2}	Connect 1MΩ load resistor between V_{DD} and V_{L2} (without panel load)		2•V_{L1} -0.1		2•V_{L1} ×0.9	V
	V_{L3}	Connect 1MΩ load resistor between V_{DD} and V_{L3} (without panel load)		3•V_{L1} -0.1		3•V_{L1} ×0.9	V
SVD voltage	V_{SVD}			-2.55	-2.40	-2.25	V
SVD circuit response time	t_{SVD}					100	µS
Current consumption	I_{OP}	During HALT	Without panel load		1.0	2.5	µA
		During execution *1			2.5	5.0	µA
		During A/D conversion (HALT)			30	40	µA

*1: The SVD circuit is turned off.

E0C6251 (Heavy Load Protection Mode)

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-3.0V, f_{OSC}=32.768kHz, Ta=25°C, C_G=25pF, V_{S1}/V_{L1}–V_{L3} are internal voltage, C1–C6=0.1µF)
(During A/D conversion: RS=49.8kΩ, TH=50kΩ, CS=2,200pF)

Characteristic	Symbol	Condition		Min.	Typ.	Max.	Unit
Internal voltage	V_{L1}	Connect 1MΩ load resistor between V_{DD} and V_{L1} (without panel load)		-1.15	-1.05	-0.95	V
	V_{L2}	Connect 1MΩ load resistor between V_{DD} and V_{L2} (without panel load)		2•V_{L1} -0.1		2•V_{L1} ×0.85	V
	V_{L3}	Connect 1MΩ load resistor between V_{DD} and V_{L3} (without panel load)		3•V_{L1} -0.1		3•V_{L1} ×0.85	V
SVD voltage	V_{SVD}			-2.55	-2.40	-2.25	V
SVD circuit response time	t_{SVD}					100	µS
Current consumption	I_{OP}	During HALT	Without panel load		2.0	5.5	µA
		During execution *1			5.5	10.0	µA
		During A/D conversion (HALT)			31	41.5	µA

*1: The SVD circuit is turned off.

E0C62L51 (Normal Mode)

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-1.5V, f_{OSC}=32.768kHz, Ta=25°C, C_G=25pF, V_{S1}/V_{L1}–V_{L3} are internal voltage, C1–C6=0.1µF)
(During A/D conversion: RS=49.8kΩ, TH=50kΩ, CS=2,200pF)

Characteristic	Symbol	Condition		Min.	Typ.	Max.	Unit
Internal voltage	V_{L1}	Connect 1MΩ load resistor between V_{DD} and V_{L1} (without panel load)		-1.15	-1.05	-0.95	V
	V_{L2}	Connect 1MΩ load resistor between V_{DD} and V_{L2} (without panel load)		2•V_{L1} -0.1		2•V_{L1} ×0.9	V
	V_{L3}	Connect 1MΩ load resistor between V_{DD} and V_{L3} (without panel load)		3•V_{L1} -0.1		3•V_{L1} ×0.9	V
SVD voltage	V_{SVD}			-1.30	-1.20	-1.10	V
SVD circuit response time	t_{SVD}					100	µS
Current consumption	I_{OP}	During HALT	Without panel load		1.0	2.5	µA
		During execution *1			2.5	5.0	µA
		During A/D conversion (HALT)			30	40	µA

*1: The SVD circuit is turned off.

E0C62L51 (Heavy Load Protection Mode)

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-1.5V, f_{OSC}=32.768kHz, Ta=25°C, C_G=25pF, V_{S1}/V_{L1}–V_{L3} are internal voltage, C1–C6=0.1µF)
(During A/D conversion: RS=49.8kΩ, TH=50kΩ, CS=2,200pF)

Characteristic	Symbol	Condition		Min.	Typ.	Max.	Unit
Internal voltage	V_{L1}	Connect 1MΩ load resistor between V_{DD} and V_{L1} (without panel load)		-1.15	-1.05	-0.95	V
	V_{L2}	Connect 1MΩ load resistor between V_{DD} and V_{L2} (without panel load)		2•V_{L1} -0.1		2•V_{L1} ×0.85	V
	V_{L3}	Connect 1MΩ load resistor between V_{DD} and V_{L3} (without panel load)		3•V_{L1} -0.1		3•V_{L1} ×0.85	V
SVD voltage	V_{SVD}			-1.30	-1.20	-1.10	V
SVD circuit response time	t_{SVD}					100	µS
Current consumption	I_{OP}	During HALT	Without panel load		2.0	5.5	µA
		During execution *1			5.5	10.0	µA
		During A/D conversion (HALT)			31	41.5	µA

*1: The SVD circuit is turned off.

E0C6251 (CR, Normal Mode)

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-3.0V, f_{OSC}=65kHz, R_{CR}=420kΩ, Ta=25°C, V_{S1}/V_{L1}–V_{L3} are internal voltage, C1–C6=0.1µF)
(During A/D conversion: RS=49.8kΩ, TH=50kΩ, CS=2,200pF)

Characteristic	Symbol	Condition		Min.	Typ.	Max.	Unit
Internal voltage	V_{L1}	Connect 1MΩ load resistor between V_{DD} and V_{L1} (without panel load)		-1.15	-1.05	-0.95	V
	V_{L2}	Connect 1MΩ load resistor between V_{DD} and V_{L2} (without panel load)		2•V_{L1} -0.1		2•V_{L1} ×0.9	V
	V_{L3}	Connect 1MΩ load resistor between V_{DD} and V_{L3} (without panel load)		3•V_{L1} -0.1		3•V_{L1} ×0.9	V
SVD voltage	V_{SVD}			-2.55	-2.40	-2.25	V
SVD circuit response time	t_{SVD}					100	µS
Current consumption	I_{OP}	During HALT	Without panel load		8.0	15.0	µA
		During execution *1			15.0	20.0	µA
		During A/D conversion (HALT)			37	52.5	µA

*1: The SVD circuit is turned off.

E0C6251 (CR, Heavy Load Protection Mode)

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-3.0V, f_{OSC}=65kHz, R_{CR}=420kΩ, Ta=25°C, V_{S1}/V_{L1}–V_{L3} are internal voltage, C1–C6=0.1µF)
(During A/D conversion: RS=49.8kΩ, TH=50kΩ, CS=2,200pF)

Characteristic	Symbol	Condition		Min.	Typ.	Max.	Unit
Internal voltage	V_{L1}	Connect 1MΩ load resistor between V_{DD} and V_{L1} (without panel load)		-1.15	-1.05	-0.95	V
	V_{L2}	Connect 1MΩ load resistor between V_{DD} and V_{L2} (without panel load)		2•V_{L1} -0.1		2•V_{L1} ×0.85	V
	V_{L3}	Connect 1MΩ load resistor between V_{DD} and V_{L3} (without panel load)		3•V_{L1} -0.1		3•V_{L1} ×0.85	V
SVD voltage	V_{SVD}			-2.55	-2.40	-2.25	V
SVD circuit response time	t_{SVD}					100	µS
Current consumption	I_{OP}	During HALT	Without panel load		16.0	30.0	µA
		During execution *1			30.0	40.0	µA
		During A/D conversion (HALT)			45	57.5	µA

*1: The SVD circuit is turned off.

E0C62L51 (CR, Normal Mode)

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-1.5V, f_{OSC}=65kHz, R_{CR}=420kΩ, Ta=25°C, V_{S1}/V_{L1}–V_{L3} are internal voltage, C1–C6=0.1µF)
(During A/D conversion: RS=49.8kΩ, TH=50kΩ, CS=2,200pF)

Characteristic	Symbol	Condition		Min.	Typ.	Max.	Unit
Internal voltage	V_{L1}	Connect 1MΩ load resistor between V_{DD} and V_{L1} (without panel load)		-1.15	-1.05	-0.95	V
	V_{L2}	Connect 1MΩ load resistor between V_{DD} and V_{L2} (without panel load)		2•V_{L1} -0.1		2•V_{L1} ×0.9	V
	V_{L3}	Connect 1MΩ load resistor between V_{DD} and V_{L3} (without panel load)		3•V_{L1} -0.1		3•V_{L1} ×0.9	V
SVD voltage	V_{SVD}			-1.30	-1.20	-1.10	V
SVD circuit response time	t_{SVD}					100	µS
Current consumption	I_{OP}	During HALT	Without panel load		8.0	15.0	µA
		During execution *1			15.0	20.0	µA
		During A/D conversion (HALT)			37	52.5	µA

*1: The SVD circuit is turned off.

E0C62L51 (CR, Heavy Load Protection Mode)

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-1.5V, f_{OSC}=65kHz, R_{CR}=420kΩ, Ta=25°C, V_{S1}/V_{L1}–V_{L3} are internal voltage, C1–C6=0.1µF)
(During A/D conversion: RS=49.8kΩ, TH=50kΩ, CS=2,200pF)

Characteristic	Symbol	Condition		Min.	Typ.	Max.	Unit
Internal voltage	V_{L1}	Connect 1MΩ load resistor between V_{DD} and V_{L1} (without panel load)		-1.15	-1.05	-0.95	V
	V_{L2}	Connect 1MΩ load resistor between V_{DD} and V_{L2} (without panel load)		2•V_{L1} -0.1		2•V_{L1} ×0.85	V
	V_{L3}	Connect 1MΩ load resistor between V_{DD} and V_{L3} (without panel load)		3•V_{L1} -0.1		3•V_{L1} ×0.85	V
SVD voltage	V_{SVD}			-1.30	-1.20	-1.10	V
SVD circuit response time	t_{SVD}					100	µS
Current consumption	I_{OP}	During HALT	Without panel load		16.0	30.0	µA
		During execution *1			30.0	40.0	µA
		During A/D conversion (HALT)			45	57.5	µA

*1: The SVD circuit is turned off.

● Oscillation Characteristics

The oscillation characteristics change depending on the conditions (components used, board pattern, etc.). Use the following characteristics as reference values.

E0C6251 (Crystal oscillation circuit)

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-3.0V, Crystal: C-002R (C_I=35kΩ), C_G=25pF, C_D=built-in, Ta=25°C)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start voltage	Vsta	tsta≤5sec (Vss)	-1.8			V
Oscillation stop voltage	Vstp	tstp≤10sec (Vss)	-1.8			V
Built-in capacitance (drain)	C_D	Including the parasitic capacity inside the IC		20		pF
Frequency/voltage deviation	∂f/∂V	V_{SS}=-1.8 to -3.5V			5	ppm
Frequency/IC deviation	∂f/∂IC		-10		10	ppm
Frequency adjustment range	∂f/∂C_G	C_G=5 to 25pF	40			ppm
Harmonic oscillation start voltage	V_{hho}	C_G=5pF (Vss)			-3.5	V
Permitted leak resistance	R_{leak}	Between OSC1 and V_{DD}, V_{SS}	200			MΩ

E0C62L51 (Crystal oscillation circuit)

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-1.5V, Crystal: C-002R (C_I=35kΩ), C_G=25pF, C_D=built-in, Ta=25°C)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start voltage	Vsta	tsta≤5sec (Vss)	-1.1			V
Oscillation stop voltage	Vstp	tstp≤10sec (Vss)	-1.1(-0.9)*1			V
Built-in capacitance (drain)	C_D	Including the parasitic capacity inside the IC		20		pF
Frequency/voltage deviation	∂f/∂V	V_{SS}=-1.1 to -2.0V (-0.9) *1			5	ppm
Frequency/IC deviation	∂f/∂IC		-10		10	ppm
Frequency adjustment range	∂f/∂C_G	C_G=5 to 25pF	40			ppm
Harmonic oscillation start voltage	V_{hho}	C_G=5pF (Vss)			-2.0	V
Permitted leak resistance	R_{leak}	Between OSC1 and V_{DD}, V_{SS}	200			MΩ

*1: Items enclosed in parentheses ( ) are those used when operating at heavy load protection mode.

E0C6251 (CR oscillation circuit)

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-3.0V, R_{CR}=420kΩ, Ta=25°C)

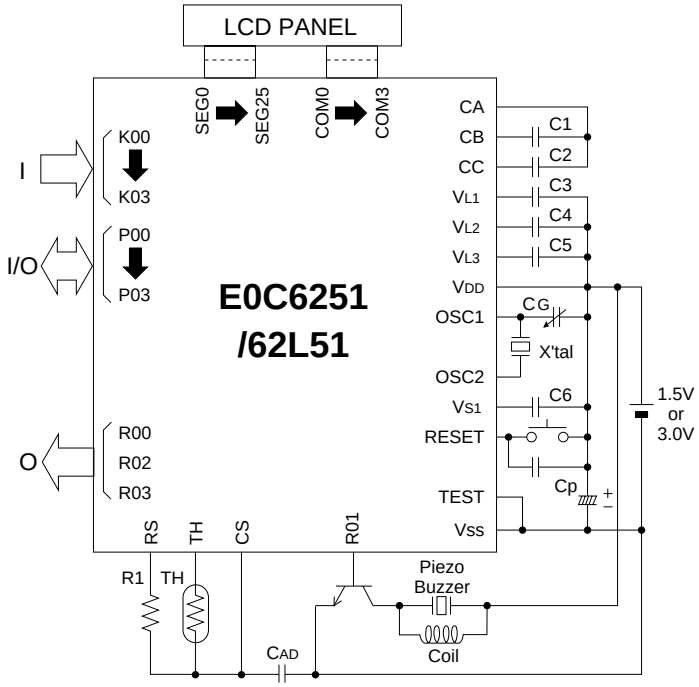
Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation frequency dispersion	fosc		-20	65kHz	20	%
Oscillation start voltage	Vsta	(Vss)	-1.8			V
Oscillation start time	tsta	V_{SS}=-1.8 to -3.5V		3		mS
Oscillation stop voltage	Vstp	(Vss)	-1.8			V

E0C62L51 (CR oscillation circuit)

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-1.5V, R_{CR}=420kΩ, Ta=25°C)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation frequency dispersion	fosc		-20	65kHz	20	%
Oscillation start voltage	Vsta	(Vss)	-1.1			V
Oscillation start time	tsta	V_{SS}=-1.1 to -2.0V		3		mS
Oscillation stop voltage	Vstp	(Vss)	-1.1			V

■ BASIC EXTERNAL CONNECTION DIAGRAM

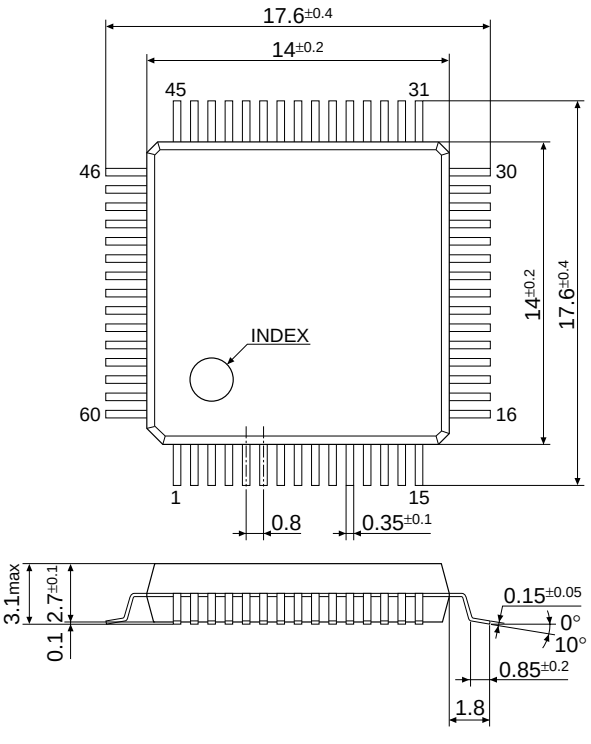


X'tal	Crystal oscillator	32.768kHz CI(Max.)=35kΩ
C_G	Trimmer capacitor	5~25pF
C1~C6	Capacitor	0.1µF
Cp	Capacitor	3.3µF
TH	Thermistor	50kΩ
R1	Resistor	49.8kΩ
C_{AD}	Capacitor	2,200pF

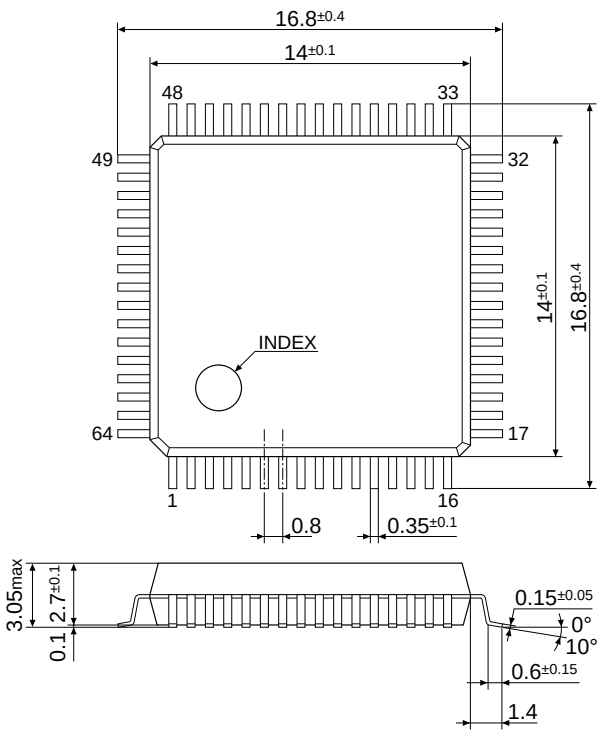
Note: The above table is simply an example, and is not guaranteed to work.

■ PACKAGE DIMENSIONS

Ceramic QFP6-60pin



Plastic QFP6-64pin



Unit: mm

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