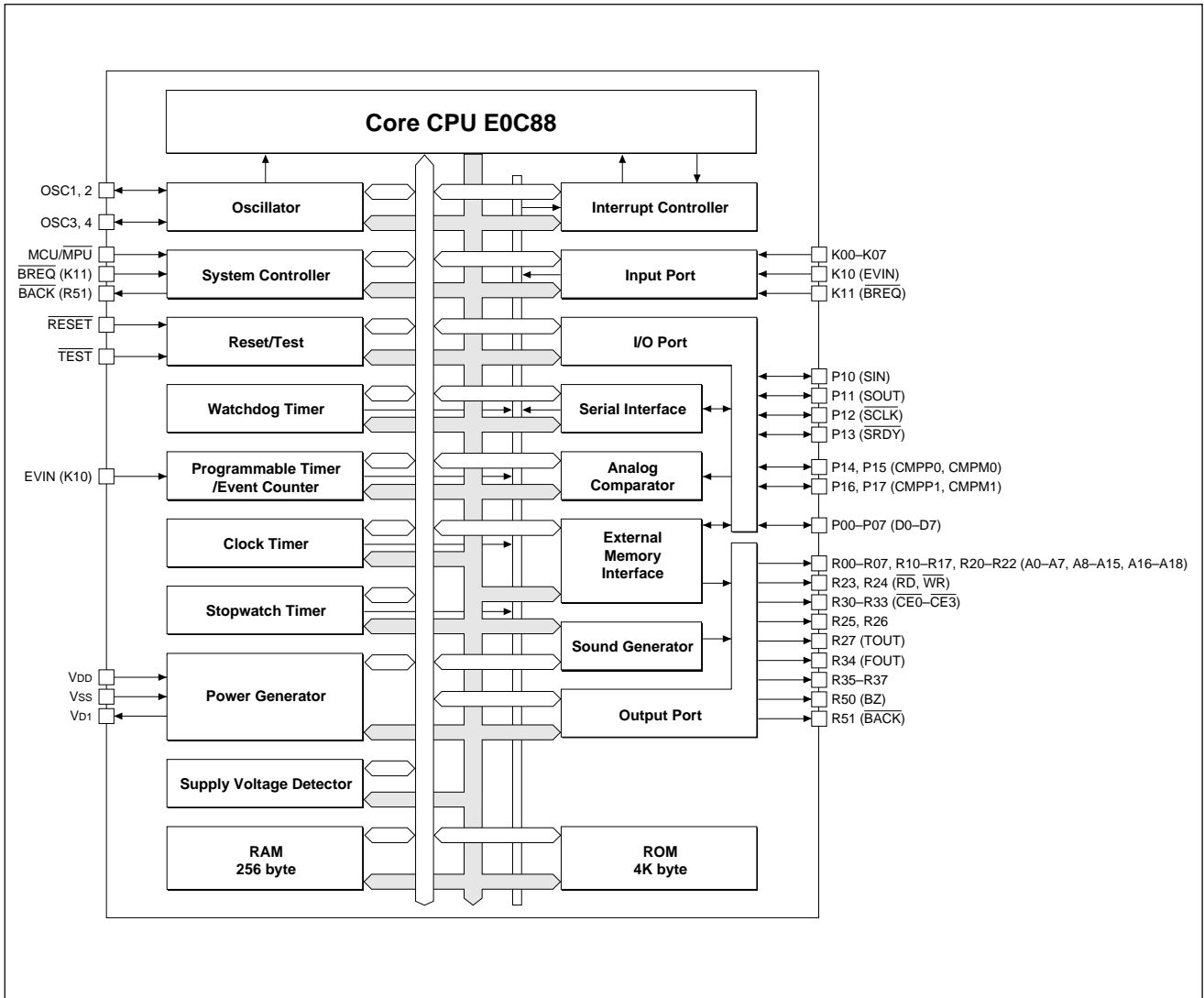
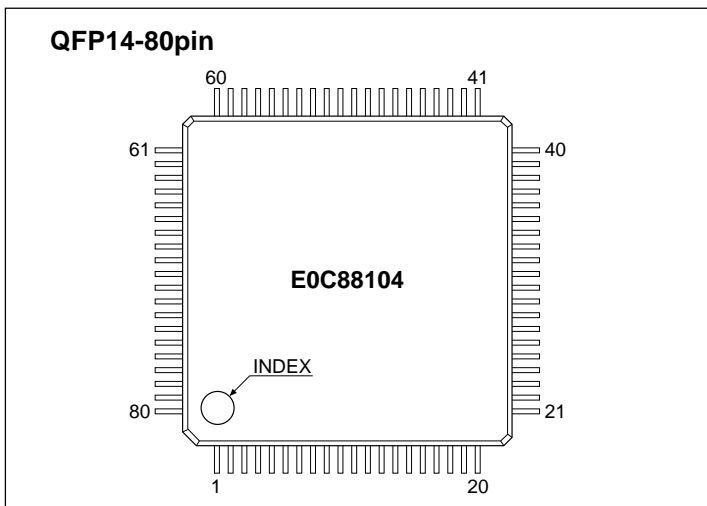


■ BLOCK DIAGRAM

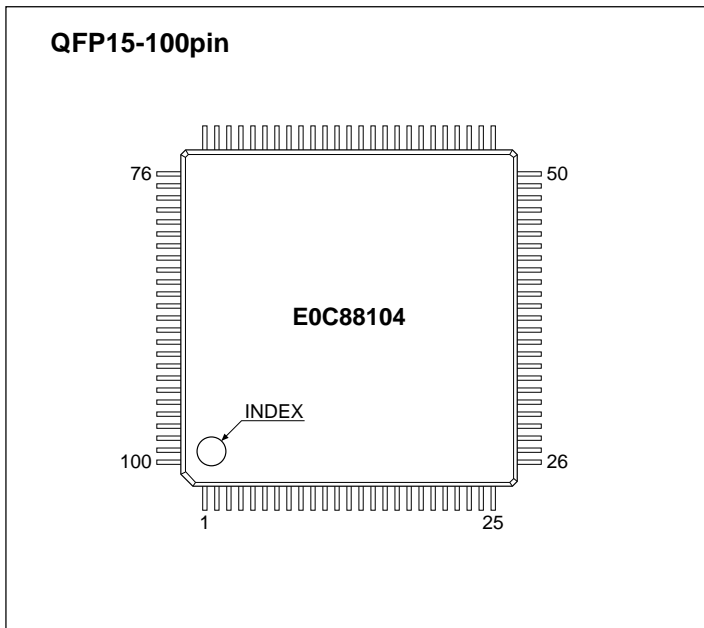


■ PIN CONFIGURATION



Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name
1	R00/A0	21	R24/WR	41	R50/BZ	61	RESET
2	R01/A1	22	R25	42	R51/BACK	62	N.C.
3	R02/A2	23	R26	43	P17/CMPM1	63	K11/BREQ
4	R03/A3	24	R27/TOUT	44	P16/CMPM1	64	K10/EVIN
5	R04/A4	25	R30/CE0	45	P15/CMPM0	65	K07
6	R05/A5	26	R31/CE1	46	P14/CMPM0	66	K06
7	R06/A6	27	R32/CE2	47	P13/SRDY	67	K05
8	R07/A7	28	R33/CE3	48	P12/SCLK	68	K04
9	R10/A8	29	R34/FOUT	49	P11/SOUT	69	K03
10	R11/A9	30	R35	50	P10/SIN	70	K02
11	R12/A10	31	R36	51	P07/D7	71	K01
12	R13/A11	32	R37	52	P06/D6	72	K00
13	R14/A12	33	*	53	P05/D5	73	MCU/MPU
14	R15/A13	34	*	54	P04/D4	74	Vdd
15	R16/A14	35	*	55	P03/D3	75	OSC4
16	R17/A15	36	*	56	P02/D2	76	OSC3
17	R20/A16	37	*	57	P01/D1	77	Vd1
18	R21/A17	38	*	58	P00/D0	78	OSC2
19	R22/A18	39	*	59	N.C.	79	OSC1
20	R23/RD	40	*	60	TEST	80	Vss

* Pins No. 33 to 40 are the pads used for outgoing inspection of the IC. Do not connect anything to these pins.
N.C. : No Connection



Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name
1	N.C.	26	N.C.	51	N.C.	76	N.C.
2	N.C.	27	N.C.	52	N.C.	77	N.C.
3	N.C.	28	R00/A0	53	R24/WR	78	N.C.
4	RESET	29	R01/A1	54	R25	79	R50/BZ
5	N.C.	30	R02/A2	55	R26	80	R51/BACK
6	K11/BREQ	31	R03/A3	56	R27/TOUT	81	P17/CMPM1
7	K10/EVIN	32	R04/A4	57	R30/CE0	82	P16/CMPM1
8	K07	33	R05/A5	58	R31/CE1	83	P15/CMPM0
9	K06	34	R06/A6	59	R32/CE2	84	P14/CMPM0
10	K05	35	R07/A7	60	R33/CE3	85	P13/SRDY
11	K04	36	R10/A8	61	R34/FOUT	86	P12/SCLK
12	K03	37	R11/A9	62	R35	87	P11/SOUT
13	K02	38	R12/A10	63	R36	88	P10/SIN
14	K01	39	R13/A11	64	R37	89	P07/D7
15	K00	40	R14/A12	65	*	90	P06/D6
16	MCU/MPU	41	R15/A13	66	*	91	P05/D5
17	VDD	42	R16/A14	67	*	92	P04/D4
18	OSC4	43	R17/A15	68	*	93	P03/D3
19	OSC3	44	R20/A16	69	*	94	P02/D2
20	Vd1	45	R21/A17	70	*	95	P01/D1
21	OSC2	46	R22/A18	71	*	96	P00/D0
22	OSC1	47	R23/RD	72	*	97	N.C.
23	VSS	48	N.C.	73	N.C.	98	TEST
24	N.C.	49	N.C.	74	N.C.	99	N.C.
25	N.C.	50	N.C.	75	N.C.	100	N.C.

* Pins No. 65 to 72 are the pads used for outgoing inspection of the IC. Do not connect anything to these pins.
N.C. : No Connection

PIN DESCRIPTION

Pin name	Pin No.		In/Out	Function
	QFP14-80	QFP15-100		
VDD	74	17	–	Power supply (+) terminal
VSS	80	23	–	Power supply (GND) terminal
Vd1	77	20	–	Regulated voltage output terminal for oscillators
OSC1	79	22	I	OSC1 oscillation input terminal (crystal oscillation/CR oscillation/external clock input, mask option)
OSC2	78	21	O	OSC2 oscillation output terminal
OSC3	76	19	I	OSC3 oscillation input terminal (crystal/ceramic/CR oscillation/external clock input, mask option)
OSC4	75	18	O	OSC4 oscillation output terminal
MCU/MPU	73	16	I	Terminal for setting MCU or MPU modes
K00–K07	72–65	15–8	I	Input port (K00–K07) terminal
K10/EVIN	64	7	I	Input port (K10) terminal or event counter external clock (EVIN) input terminal
K11/BREQ	63	6	I	Input port (K11) terminal or bus request signal (BREQ) input terminal
R00–R07/A0–A7	1–8	28–35	O	Output port (R00–R07) terminals or address bus (A0–A7)
R10–R17/A8–A15	9–16	36–43	O	Output port (R10–R17) terminals or address bus (A8–A15)
R20–R22/A16–A18	17–19	44–46	O	Output port (R20–R22) terminals or address bus (A16–A18)
R23/RD	20	47	O	Output port (R23) terminal or read signal (RD) output terminal
R24/WR	21	53	O	Output port (R24) terminal or write signal (WR) output terminal
R25	22	54	O	Output port (R25) terminal
R26	23	55	O	Output port (R26) terminal
R27/TOUT	24	56	O	Output port (R27) terminal or programmable timer underflow signal (TOUT) output terminal
R30–R33/CE0–CE3	25–28	57–60	O	Output port (R30–R33) terminals or chip enable (CE0–CE3) output terminals
R34/FOUT	29	61	O	Output port (R34) terminal or clock (FOUT) output terminal
R35–R37	30–32	62–64	O	Output port (R35–R37) terminal
R50/BZ	41	79	O	Output port (R50) terminal or buzzer (BZ) output terminal
R51/BACK	42	80	O	Output port (R51) terminal or bus acknowledge signal (BACK) output terminal
P00–P07/D0–D7	58–51	96–89	I/O	I/O port (P00–P07) terminals or data bus (D0–D7)
P10/SIN	50	88	I/O	I/O port (P10) terminal or serial I/F data input (SIN) terminal
P11/SOUT	49	87	I/O	I/O port (P11) terminal or serial I/F data output (SOUT) terminal
P12/SCLK	48	86	I/O	I/O port (P12) terminal or serial I/F clock (SCLK) I/O terminal
P13/SRDY	47	85	I/O	I/O port (P13) terminal or serial I/F ready signal (SRDY) output terminal
P14/CMPM0	46	84	I/O	I/O port (P14) terminal or comparator 0 non-inverted input terminal
P15/CMPM0	45	83	I/O	I/O port (P15) terminal or comparator 0 inverted input terminal
P16/CMPM1	44	82	I/O	I/O port (P16) terminal or comparator 1 non-inverted input terminal
P17/CMPM1	43	81	I/O	I/O port (P17) terminal or comparator 1 inverted input terminal
RESET	61	4	I	Initial reset input terminal
TEST	*	60	I	Test input terminal

* TEST is the terminal used for outgoing inspection of the IC. For normal operation be sure it is connected to VDD.

■ ELECTRICAL CHARACTERISTICS

● Absolute Maximum Ratings

(V_{SS} = 0V)

Rating	Symbol	Condition	Value	Unit	Note
Power voltage	V _{DD}		-0.3 to +7.0	V	
Input voltage	V _I		-0.3 to V _{DD} + 0.3	V	
Output voltage	V _O		-0.3 to V _{DD} + 0.3	V	1
High level output current	I _{OH}	1 terminal	-5	mA	
		Total of all terminals	-20	mA	
Low level output current	I _{OL}	1 terminal	5	mA	
		Total of all terminals	20	mA	
Permitted loss	P _d		200	mW	2
Operating temperature	T _{opr}		-40 to +85	°C	
Storage temperature	T _{stg}		-65 to +150	°C	

Note) 1 Case that to Nch open drain output by the mask option is included.
 2 In case of plastic package.

● Recommended Operating Conditions

(V_{SS} = 0V, T_a = -40 to 85°C)

Condition	Symbol	Remark	Min.	Typ.	Max.	Unit	Note
Operating power voltage (Normal mode)	V _{DD}		2.4		5.5	V	
Operating power voltage (Low power mode)	V _{DD}		1.8		3.5	V	
Operating power voltage (High speed mode)	V _{DD}		3.5		5.5	V	
Operating frequency (Normal mode)	f _{OSC1}	V _{DD} = 2.4 to 5.5V	30	32.768	50	kHz	3
	f _{OSC3}		0.03		4.2	MHz	3
Operating frequency (Low power mode)	f _{OSC1}	V _{DD} = 1.8 to 3.5V	30	32.768	50	kHz	3
Operating frequency (High speed mode)	f _{OSC1}	V _{DD} = 3.5 to 5.5V	30	32.768	50	kHz	3
	f _{OSC3}		0.03		8.2	MHz	3
Capacitor between V _{D1} and V _{SS}	C1			0.1		μF	

Note) 3 When an external clock is input from the OSC1 terminal by the mask option, do not connect anything to the OSC2 terminal, and when an external clock is input from the OSC3 terminal, do not connect to the OSC4 terminal.

● DC Characteristics

(Unless otherwise specified: V_{DD} = 1.8 to 5.5V, V_{SS} = 0V, T_a = -40 to 85°C)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
High level input voltage (1)	V _{IH1}	Kxx, Pxx, MCU/MPU	0.8V _{DD}		V _{DD}	V	
Low level input voltage (1)	V _{IL1}	Kxx, Pxx, MCU/MPU	0		0.2V _{DD}	V	
High level input voltage (2) (Normal mode)	V _{IH2}	OSC1, OSC3	1.6		V _{DD}	V	4
High level input voltage (2) (Low power mode)	V _{IH2}	OSC1	1.0		V _{DD}	V	4
High level input voltage (2) (High speed mode)	V _{IH2}	OSC1, OSC3	2.4		V _{DD}	V	4
Low level input voltage (2) (Normal mode)	V _{IL2}	OSC1, OSC3	0		0.6	V	4
Low level input voltage (2) (Low power mode)	V _{IL2}	OSC1	0		0.3	V	4
Low level input voltage (2) (High speed mode)	V _{IL2}	OSC1, OSC3	0		0.9	V	4
High level schmitt input voltage	V _{T+}	RESET	0.5V _{DD}		0.9V _{DD}	V	
Low level schmitt input voltage	V _{T-}	RESET	0.1V _{DD}		0.5V _{DD}	V	
High level output current	I _{OH}	Pxx, Rxx, V _{OH} = 0.9V _{DD}			-0.5	mA	
Low level output current	I _{OL}	Pxx, Rxx, V _{OL} = 0.1V _{DD}	0.5			mA	
Input leak current	I _{LI}	Kxx, Pxx, RESET, MCU/MPU	-1		1	μA	
Output leak current	I _{LO}	Pxx, Rxx	-1		1	μA	
Input pull-up resistance	R _{IN}	Kxx, Pxx, RESET, MCU/MPU	100		500	kΩ	5
Input terminal capacitance	C _{IN}	Kxx, Pxx, V _{IN} = 0 V, f = 1MHz, T _a = 25°C			15	pF	

Note) 4 When external clock is selected by mask option.
 5 When addition of pull-up resistor is selected by mask option.

● SVD Circuit

(Unless otherwise specified: VDD = 1.8 to 5.5V, VSS = 0V, Ta = 25°C)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
SVD voltage	VsVD	Level 1 → Level 0		1.82		V	
		Level 2 → Level 1		2.00		V	
		Level 3 → Level 2		2.18		V	
		Level 4 → Level 3		2.36		V	
		Level 5 → Level 4	Typ×0.92	2.54	Typ×1.08	V	
		Level 6 → Level 5		2.72		V	
		Level 7 → Level 6		2.90		V	
		Level 8 → Level 7		3.08		V	
		Level 9 → Level 8		3.26		V	
		Level 10 → Level 9		3.45		V	
		Level 11 → Level 10		3.65		V	
		Level 12 → Level 11	Typ×0.88	3.85	Typ×1.12	V	
		Level 13 → Level 12		4.05		V	
		Level 14 → Level 13		4.25		V	
		Level 15 → Level 14		4.50		V	

● Analog Comparator Circuit

(Unless otherwise specified: VDD = 1.8 to 5.5V, VSS = 0V, Ta = 25°C)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Analog comparator operating voltage input range	VCMIP	Non-inverted input (CMPP)	0.7		VDD - 0.7	V	6
	VCMIM	Inverted input (CMPM)	0.7		VDD - 0.7	V	6
Analog comparator offset voltage	VCMOF	VCMIP = 0.7V to VDD - 0.7V VCMIM = 0.7V to VDD - 0.7V			20	mV	6
Analog comparator stability time	tCMP1				1	mS	7
Analog comparator response time	tCMP2	VCMIP = 0.7V to VDD - 0.7V VCMIM = 0.7V to VDD - 0.7V			2	mS	6
		VCMIP = VCMIM ± 0.025V					8

- Note) 6 When "without pull-up resistor" (comparator input terminal) is selected by mask option.
 7 Stability time is the time from turning the circuit ON until the circuit is stabilized.
 8 Response time is the time that the output result responds to the input signal.

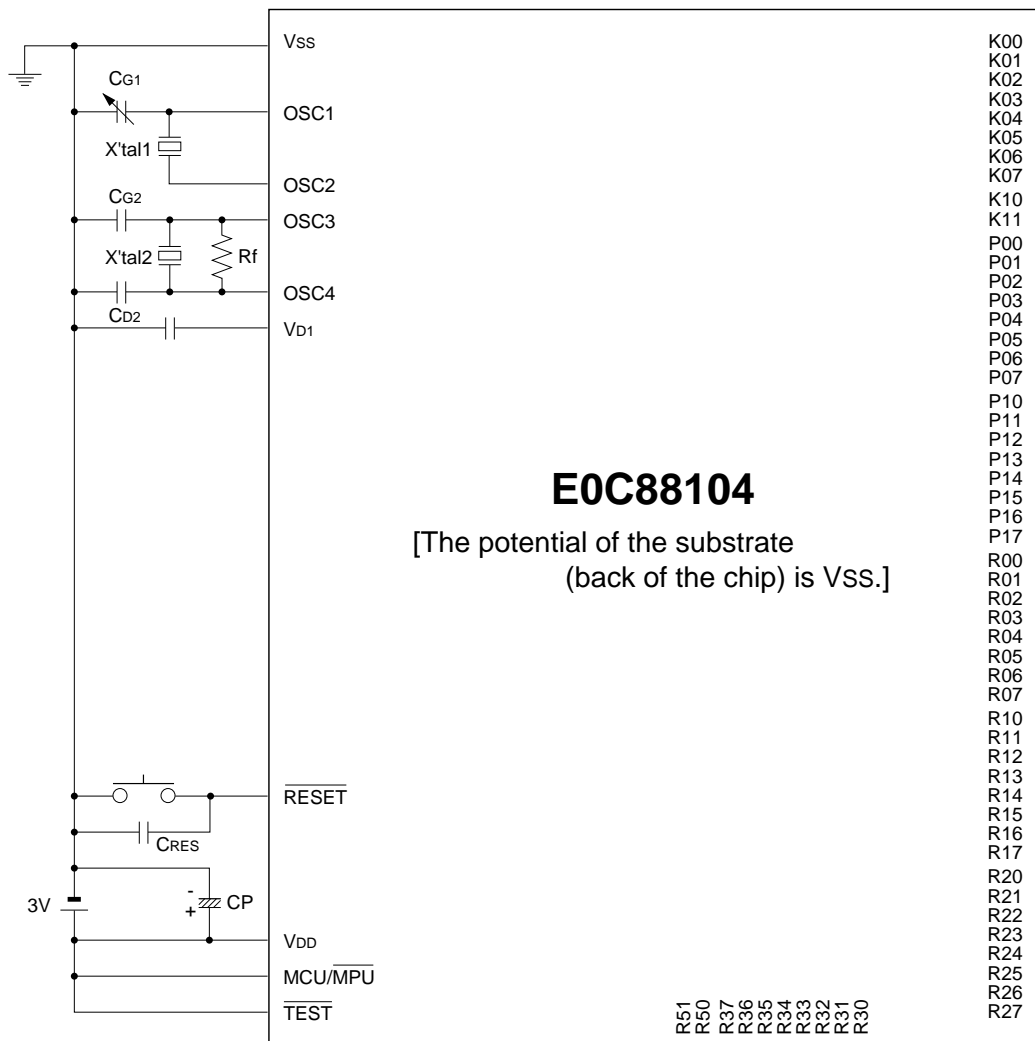
● Current Consumption

(Unless otherwise specified: VDD = Within the operating voltage in each operating mode, VSS = 0V, Ta = 25°C, OSC1 = 32.768kHz crystal oscillation, Cg = 10pF, OSC3 = External clock input, Non heavy load protection mode, C1 = 0.1μF)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Power current (Normal mode)	IDD1	In SLEEP status *1		0.3	1	μA	
	IDD2	In HALT status *2		2	5	μA	
	IDD3	CPU is in operating (32.768kHz) *3		14	18	μA	
	IDD4	CPU is in operating (1MHz) *4		0.45	0.60	mA	
	IHVL	In heavy load protection mode		25	50	μA	9
Power current (Low power mode)	IDD1	In SLEEP status *1		0.2	1	μA	
	IDD2	In HALT status *2		1	5	μA	
	IDD3	CPU is in operating (32.768kHz) *3		8	12	μA	
	IHVL	In heavy load protection mode		15	30	μA	9
	Power current (High speed mode)	IDD1	In SLEEP status *1		1	3	μA
IDD2		In HALT status *2		5	10	μA	
IDD3		CPU is in operating (32.768kHz) *3		24	30	μA	
IDD4		CPU is in operating (1MHz) *4		0.70	1.00	mA	
IHVL		In heavy load protection mode		35	70	μA	9
SVD circuit current	ISVDN	VDD = 3.0V		30	60	μA	10
	ISVDH	In heavy load protection mode		25	75	μA	9
Analog comparator circuit current	ICMP1	CMPXDT = "1"		40	100	μA	
	ICMP2	CMPXDT = "0"		4	10	μA	
OSC1 CR oscillation current	ICR1			20	50	μA	11

- *1 OSC1: Stop, OSC3: Stop, CPU, ROM, RAM: SLEEP status, Clock timer: Stop, Others: Stop status
 *2 OSC1: Oscillating, OSC3: Stop, CPU, ROM, RAM: HALT status, Clock timer: Operating, Others: Stop status
 *3 OSC1: Oscillating, OSC3: Stop, CPU, ROM, RAM: Operating in 32.768kHz, Clock timer: Operating, Others: Stop status
 *4 OSC1: Oscillating, OSC3: Oscillating, CPU, ROM, RAM: Operating in 1MHz, Clock timer: Operating, Others: Stop status
 Note) 9 It is the value of current which flows in the heavy load protection circuit when in the heavy load protection mode (OSC3 ON or buzzer ON).
 10 The value in x V can be found by the following expression:
 ISVDN (VDD = x V) = (x × 20) - 30 (Typ. value), ISVDN (VDD = x V) = (x × 30) - 30 (Max. value)
 11 When OSC1 CR oscillation circuit is selected by the mask option.

■ BASIC EXTERNAL CONNECTION DIAGRAM

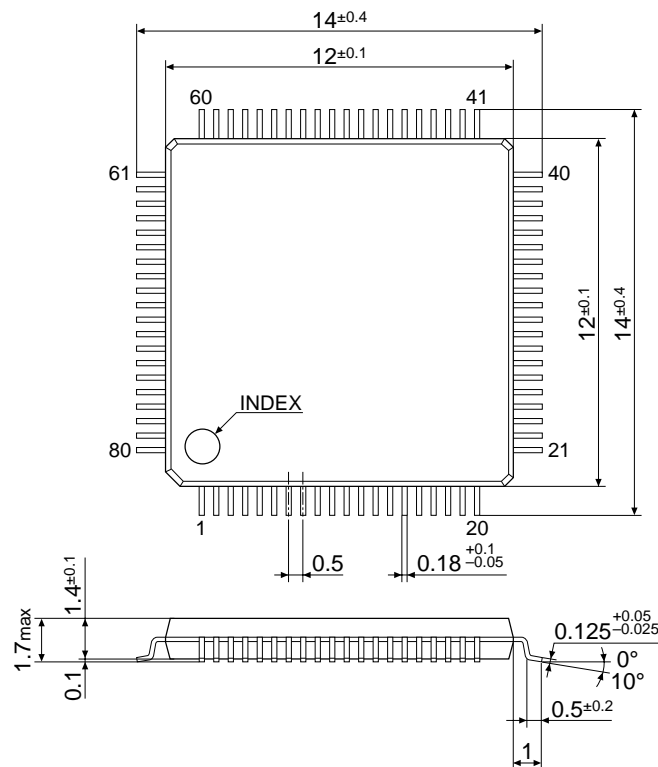


Recommended values for external parts

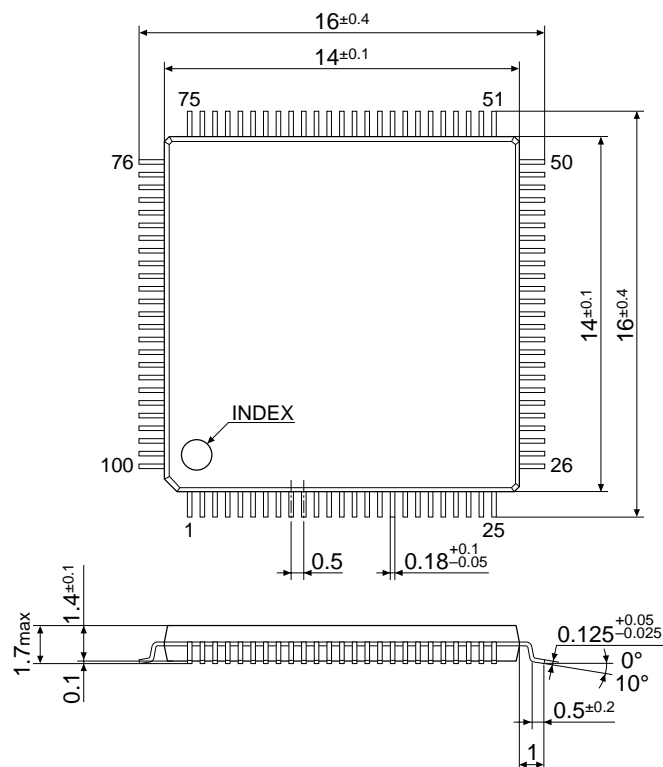
Symbol	Name	Recommended value
X'tal1	Crystal oscillator	32.768kHz, CI(Max.) = 35kΩ
X'tal2	Crystal oscillator	4.2MHz
Rf	Feedback resistor	1MΩ
CG1	Trimmer capacitor	5–25pF
CG2	Gate capacitor	15pF
CD2	Drain capacitor	15pF
CP	Capacitor for power supply	3.3μF
CRES	Capacitor for RESET terminal	0.47μF

■ PACKAGE DIMENSIONS

Plastic QFP14-80pin



Plastic QFP15-100pin



Unit: mm

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SEIKO EPSON CORPORATION**ELECTRONIC DEVICES MARKETING DIVISION****Electronic Device Marketing Department
IC Marketing & Engineering Group**

421-8, Hino, Hino-shi, Tokyo 191-8501, JAPAN
Phone: +81-(0)42-587-5816 Fax: +81-(0)42-587-5624

ED International Marketing Department I (Europe & U.S.A.)

421-8, Hino, Hino-shi, Tokyo 191-8501, JAPAN
Phone: +81-(0)42-587-5812 Fax: +81-(0)42-587-5564

ED International Marketing Department II (Asia)

421-8, Hino, Hino-shi, Tokyo 191-8501, JAPAN
Phone: +81-(0)42-587-5814 Fax: +81-(0)42-587-5110

Electric Device Information of EPSON WWW server

<http://www.epson.co.jp>

