MF1114-01

EPSON

CMOS 4-BIT SINGLE CHIP MICROCOMPUTER

E0C6006 TECHNICAL MANUAL

E0C6006 Technical Hardware

ENERGY SAVING EPSON

SEIKO EPSON CORPORATION

CONTENTS

CHAPTER 1 INTRODUCTION

The E0C6006 is a single-chip microcomputer which uses an E0C6200B CMOS 4-bit CPU as the core. It contains a 2,048 (words) × 12 (bits) ROM, 128 (words) × 4 (bits) RAM, LCD driver circuit, remote-control carrier output circuit, time base counter and watchdog timer.
The E0C6006 offers a superb solution to infrared remote controller and other applications requiring low power consumption.

1.1 Features

Core CPU E0C6200B

ROM size ..... 2,048 words × 12 bits

RAM size ..... 128 words × 4 bits

Clock ..... 32.768 kHz crystal oscillation circuit
455 kHz ceramic or CR oscillation circuit (selectable by mask option)

Instruction execution time ..... 32 kHz operation: 153, 214 or 366 µsec (depending on instructions)
455 kHz operation: 11, 15 or 26 µsec (depending on instructions)

Instruction set ..... 100 instructions

Input port ..... 8 ports (with or without pull-up resistor)

Output ports ..... 4 ports (clock and buzzer outputs are possible by mask option)

I/O port ..... 4 ports

Infrared remote-control output .... 1 output

LCD driver ..... 20 segments × 3 or 4 commons
(1/3 or 1/4 duty are selectable by mask option)

Clock timer ..... Built-in

Watchdog timer ..... Built-in

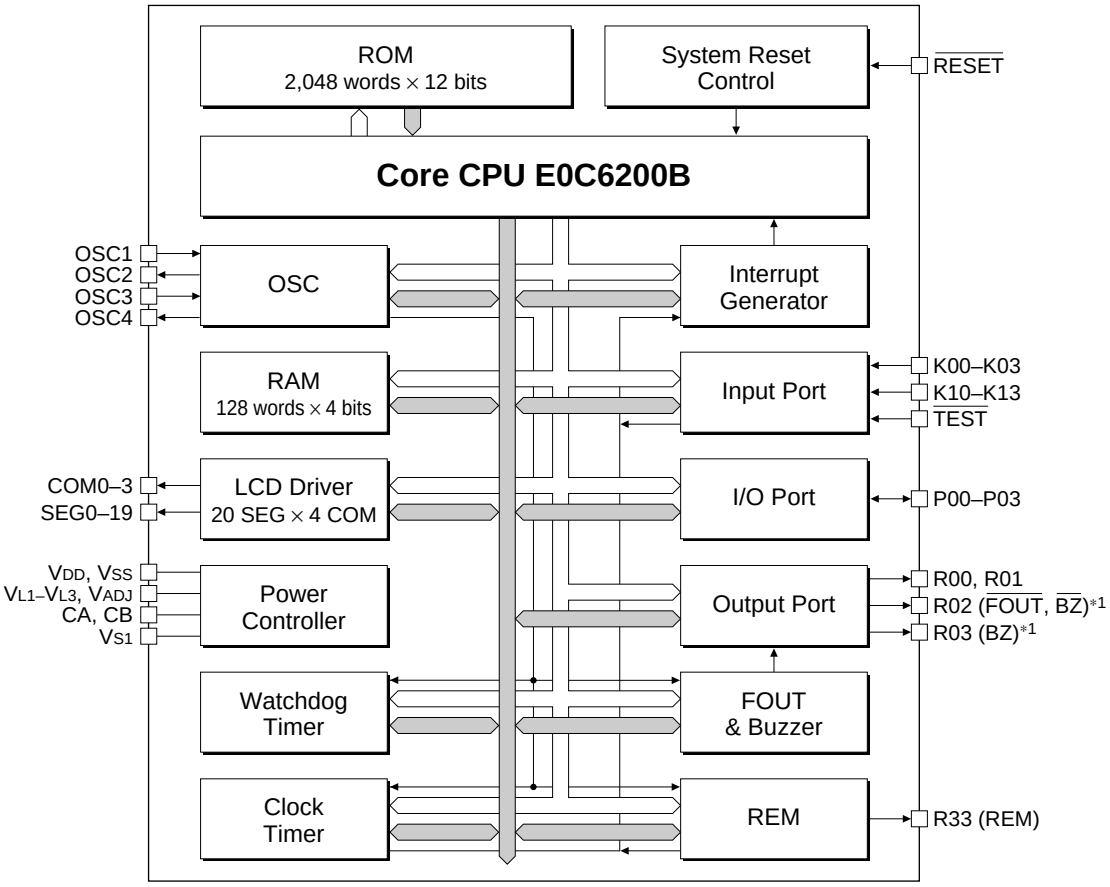
Interrupt ..... External: 2 input interrupts
Internal: 3 timer interrupts (32 Hz, 8 Hz or 2 Hz)
1 remote control output control interrupt

Supply voltage ..... 3 V (2.2 V to 3.5 V)

Current consumption (Typ.) ..... 32 kHz operation: 2 µA in halt mode
9 µA in full run mode
455 kHz operation: 130 µA

Supply form ..... Die form, QFP6-60pin plastic package or QFP13-64pin plastic package

1.2 Block Diagram

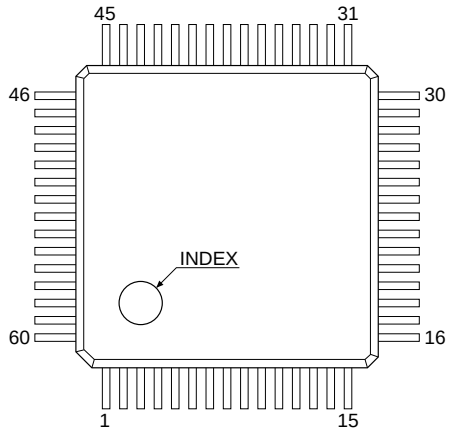


*1: Terminal specifications can be selected by mask option.

Fig. 1.2.1 E0C6006 block diagram

1.3 Pin Layout

QFP6-60pin

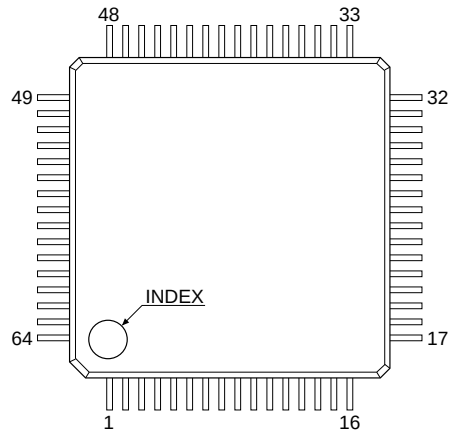


No.	Pin name	No.	Pin name	No.	Pin name	No.	Pin name
1	N.C.	16	R33(REM)	31	$\overline{\text{RESET}}$	46	V_{L3}
2	N.C.	17	SEG0	32	SEG12	47	V_{ADJ}
3	N.C.	18	SEG1	33	SEG13	48	CA
4	K00	19	SEG2	34	SEG14	49	CB
5	K01	20	SEG3	35	SEG15	50	V_{SS}
6	K02	21	SEG4	36	SEG16	51	OSC4
7	K03	22	SEG5	37	SEG17	52	OSC3
8	K10	23	SEG6	38	SEG18	53	V_{S1}
9	K11	24	SEG7	39	SEG19	54	OSC2
10	K12	25	SEG8	40	COM3	55	OSC1
11	K13	26	SEG9	41	COM2	56	V_{DD}
12	R00	27	SEG10	42	COM1	57	P03
13	R01	28	N.C.	43	COM0	58	P02
14	R02	29	SEG11	44	V_{L1}	59	P01
15	R03	30	$\overline{\text{TEST}}$	45	V_{L2}	60	P00

N.C. = No connection

Fig. 1.3.1 E0C6006 pin layout (QFP6-60pin)

QFP13-64pin



No.	Pin name	No.	Pin name	No.	Pin name	No.	Pin name
1	N.C.	17	N.C.	33	$\overline{\text{RESET}}$	49	N.C.
2	N.C.	18	R33(REM)	34	SEG12	50	V_{ADJ}
3	N.C.	19	SEG0	35	SEG13	51	CA
4	N.C.	20	SEG1	36	SEG14	52	CB
5	K00	21	SEG2	37	SEG15	53	V_{SS}
6	K01	22	SEG3	38	SEG16	54	OSC4
7	K02	23	SEG4	39	SEG17	55	OSC3
8	K03	24	SEG5	40	SEG18	56	V_{S1}
9	K10	25	SEG6	41	SEG19	57	OSC2
10	K11	26	SEG7	42	COM3	58	OSC1
11	K12	27	SEG8	43	COM2	59	V_{DD}
12	K13	28	SEG9	44	COM1	60	P03
13	R00	29	SEG10	45	COM0	61	P02
14	R01	30	SEG11	46	V_{L1}	62	P01
15	R02	31	N.C.	47	V_{L2}	63	P00
16	R03	32	$\overline{\text{TEST}}$	48	V_{L3}	64	N.C.

N.C. = No connection

Fig. 1.3.2 E0C6006 pin layout (QFP13-64pin)

1.4 Pin Description

Table 1.4.1 Pin description

Pin name	Pin No.		I/O	Function
	QFP6-60	QFP13-64		
V_{DD}	56	59	(I)	Power supply pin (+)
V_{SS}	50	53	(I)	Power supply pin (-)
V_{S1}	53	56	–	Oscillation and internal logic system voltage output pin
V_{L1}	44	46	–	LCD drive voltage output pin
V_{L2}	45	47	–	LCD drive voltage output pin
V_{L3}	46	48	–	LCD drive voltage output pin
CA, CB	48, 49	51, 52	–	Boost capacitor connecting pin
V_{ADJ}	47	50	I	V_{L1} adjustment input pin
OSC1	55	58	I	Oscillation input pin (crystal)
OSC2	54	57	O	Oscillation output pin (crystal)
OSC3	52	55	I	Oscillation input pin (ceramic or CR *)
OSC4	51	54	O	Oscillation output pin (ceramic or CR *)
K00–K03	4–7	5–8	I	Input port pin
K10–K13	8–11	9–12	I	Input port pin
P00–P03	60–57	63–60	I/O	I/O port pin
R00, R01	12, 13	13, 14	O	Output port pin
R02	14	15	O	Output port pin, $\overline{BZ}$ or $\overline{FOUT}$ output pin *
R03	15	16	O	Output port pin or BZ output pin *
R33(REM)	16	18	O	Remote control carrier output port pin
SEG0–19	17–27, 29, 32–39	19–30, 34–41	O	LCD segment output pin or DC output pin *
COM0–3	43–40	45–42	O	LCD common output pin (1/3 duty or 1/4 duty are selectable *)
$\overline{RESET}$	31	33	I	Initial reset input pin
$\overline{TEST}$	30	32	I	Input pin for test

∗ Can be selected by mask option

CHAPTER 2 POWER SUPPLY AND INITIAL RESET

2.1 Power Supply

With a single external power supply (*) supplied to VDD through VSS, the E0C6006 generates the necessary internal voltages with the regulated voltage circuit (<VS1> for oscillator and internal circuit) and the LCD voltage circuit (<VL2 and VL3 or VL1 and VL3> for LCD).

* Supply voltage: 3 V (2.2 to 3.5 V)

Note: External loads cannot be driven by the output voltage of the regulated voltage circuit and LCD voltage circuit.

2.1.1 Voltage <VS1> for oscillation circuit and internal circuits

VS1 is a voltage for the oscillation circuit and the internal logic circuits, and is generated by the voltage regulator for stabilizing the oscillation.

2.1.2 Voltage <VL1–VL3> for LCD driving

The on-chip LCD voltage circuit generates the voltage levels (VDD, VL1, VL2 and VL3) needed to drive the LCD panel.
Figure 2.1.2.1 shows the external connection diagram.

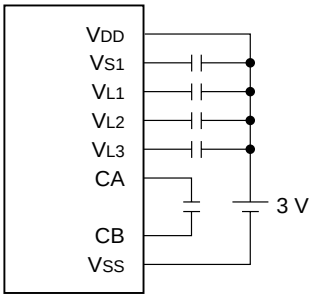


Fig. 2.1.2.1 External connection in each LCD operation mode

For LCD driving, the internal voltage regulator generates the VL1 voltage. The VL2 and VL3 voltage levels are generated by boosting the VL1 voltage.
The VL1 voltage can be adjusted by feeding it back to the VADJ pin through RA1 and RA2 as shown in Figure 2.1.2.2. VL (≈ VDD - VL1) is defined by following equation:

$$V_L \approx 1 \times (R_{A1} + R_{A2}) / R_{A1}$$

Example:

VL	RA1	RA2
≈ 1 V	∞	0 Ω
≈ 1.5 V	2 MΩ	1 MΩ

An LCD driving voltage suited to each LCD panel can be obtained by adjusting VL at the VADJ pin.

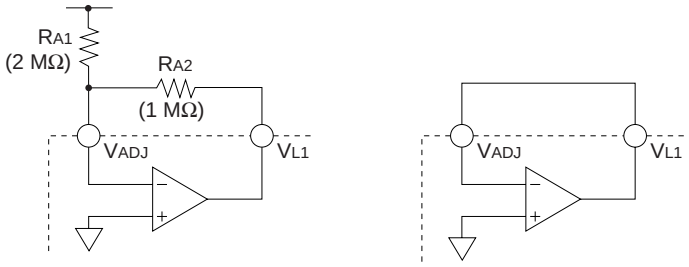


Fig. 2.1.2.2 LCD voltage adjustment circuit

2.2 Initial Reset

The E0C6006 must be initially reset to initialize its circuits. Initial reset is triggered by an external reset ($\overline{\text{RESET}}$) signal, oscillation detector signal, or watchdog timer signal. The $\overline{\text{RESET}}$ input is needed for initialization at power-on.

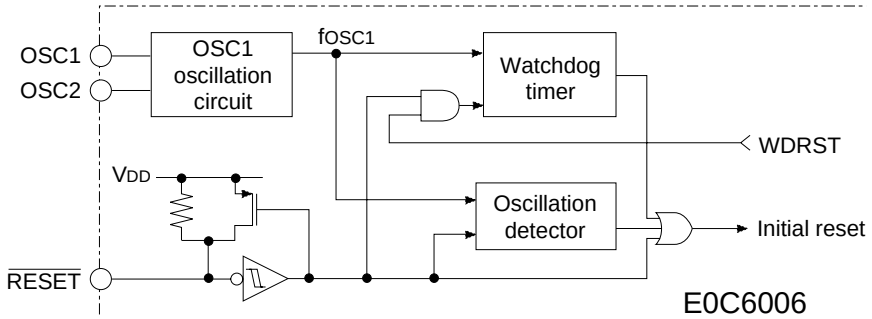


Fig. 2.2.1 Initial reset circuit configuration

2.2.1 Reset at power-on

At power-on, the initial reset signal has two functions. One function is to initialize a circuit and the other to sustain the initializing function until the OSC3 oscillation is stabilized. Thus, the $\overline{\text{RESET}}$ input must be held at low level for at least 0.5 second after power-on.
After the $\overline{\text{RESET}}$ input reaches the high level and the OSC1 oscillation circuit starts operating, several milliseconds later, the system is released from internal reset and starts to operate.

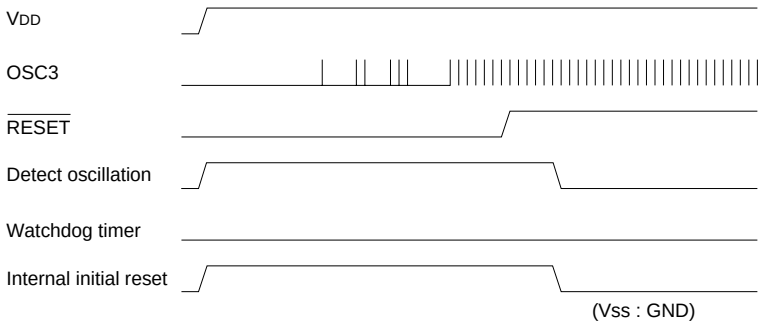


Fig. 2.2.1.1 Initial reset sequence at power-on

2.2.2 $\overline{\text{RESET}}$ pin

The $\overline{\text{RESET}}$ signal directly initializes the E0C6006. The system is reset when $\overline{\text{RESET}}$ = L, and released from the reset state when $\overline{\text{RESET}}$ = H. As the $\overline{\text{RESET}}$ pin is pulled up and receives a schmitt trigger input, it can be used as a power-on reset circuit if the $\overline{\text{RESET}}$ pin is connected with the VSS pin via a capacitor as shown in Figure 2.2.2.1. A reset switch must be provided to obtain an assured reset effect at power-on without being influenced by possible power. This is especially important for a reset operation without the use of the OSC3 oscillation circuit, in which case the system clock (OSC1) must be ON before the system is released from the reset state.

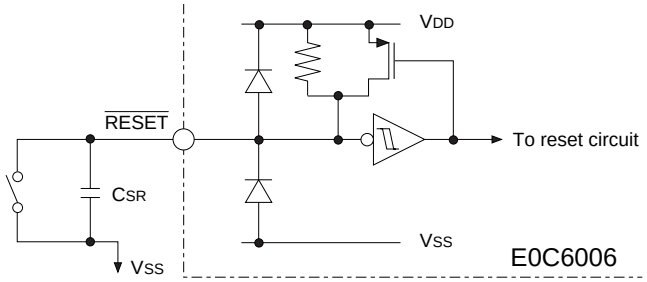


Fig. 2.2.2.1 Power-on reset circuit

2.2.3 Oscillation detection circuit

With $\overline{\text{RESET}}$ = H, the oscillation detection circuit receives f_{OSC1} and makes a f-V conversion. If the OSC1 frequency is greater than a certain value, the oscillation output goes to L to clear the reset state. The time required for f-V conversion depends on f_{OSC1}, and is several milliseconds with f_{OSC1} = 32 kHz. This time gives a delay for clearing the reset state from the $\overline{\text{RESET}}$ input going to H.

The oscillation detection circuit may sometimes not operate normally with the initial resetting due to the circuit, depending on the method of making the power, you should utilize the initial resetting method by the $\overline{\text{RESET}}$ pin.

2.2.4 Watchdog timer

The watchdog timer guards the CPU against an unexpected overrun. It uses the OSC1 clock as the source oscillation frequency to perform the increment operation. If the watchdog timer fails to be reset in 3–4 seconds with f_{OSC1} = 32 kHz, the CPU will be initialized at initial reset.
See Section 4.2, "Watchdog Timer", for details.

2.2.5 Initialization by initial reset

When the E0C6006 is initially reset, its internal registers are set as follows:

Table 2.2.5.1 Initial status

CPU Core			
Name	Symbol	Bit size	Initial value
Program counter step	PCS	8	00H
Program counter page	PCP	4	1H
New page pointer	NPP	4	1H
Stack pointer	SP	8	Undefined
Index register X	X	8	Undefined
Index register Y	Y	8	Undefined
Register pointer	RP	4	Undefined
General-purpose register A	A	4	Undefined
General-purpose register B	B	4	Undefined
Interrupt flag	I	1	0
Decimal flag	D	1	0
Zero flag	Z	1	Undefined
Carry flag	C	1	Undefined

Peripheral Circuits		
Name	Bit size	Initial value
RAM	128×4	Undefined
Display memory	20×4	Undefined
Other peripheral circuits	–	*

* See Section 4.1, "Memory Map".

2.3 Test Input Pin ($\overline{\text{TEST}}$)

This pin is used when IC is inspected for shipment.
During normal operation connect it to V_{DD}.

CHAPTER 3 CPU, ROM, RAM

3.1 CPU

The E0C6006 employs the E0C6200B core CPU, so that register configuration, instructions, and so forth are virtually identical to those in other processors in the family using the E0C6200/6200A/6200B. Refer to the "E0C6200/6200A Core CPU Manual" for details of the E0C6200B.

Note the following points with regard to the E0C6006:

(1) The E0C6006 does not support the SLEEP function, therefore the SLP instruction cannot be used.

(2) Because the ROM capacity is 2,048 words, 12 bits per word, bank bits are unnecessary, and PCB and NBP are not used.

(3) The RAM page is set to 0 only, so the page part (XP, YP) of the index register that specifies addresses is invalid.

```
PUSH XP    POP XP    LD XP,r    LD r,XP
PUSH YP    POP YP    LD YP,r    LD r,YP
```

3.2 ROM

The built-in ROM, a mask ROM for the program, has a capacity of 2,048 × 12-bit steps. The program area is 8 pages (0–7), each consisting of 256 steps (00H–FFH). After an initial reset, the program start address is set to page 1, step 00H. The interrupt vectors are allocated to page 1, steps 01H–07H.

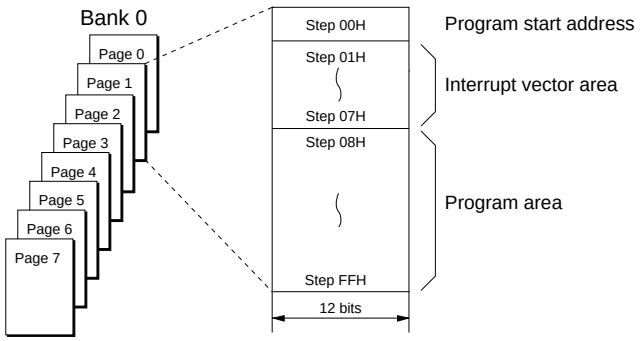


Fig. 3.2.1 ROM configuration

3.3 RAM

The RAM, a data memory for storing a variety of data, has a capacity of 128 words, 4-bit words. When programming, keep the following points in mind:

(1) Part of the data memory is used as stack area when saving subroutine return addresses and registers, so be careful not to overlap the data area and stack area.

(2) Subroutine calls and interrupts take up three words on the stack.

(3) Data memory 000H–00FH is the memory area pointed by the register pointer (RP).

CHAPTER 4 PERIPHERAL CIRCUITS AND OPERATION

Peripheral circuits (timer, I/O, and so on) of the E0C6006 are memory mapped. Thus, all the peripheral circuits can be controlled by using memory operations to access the I/O memory. The following sections describe how the peripheral circuits operate.

4.1 Memory Map

The data memory of the E0C6006 has an address space of 175 words, of which 32 words are allocated to display memory and 15 words, to I/O memory. Figure 4.1.1 show the overall memory map for the E0C6006, and Table 4.1.1, the memory maps for the peripheral circuits (I/O space).

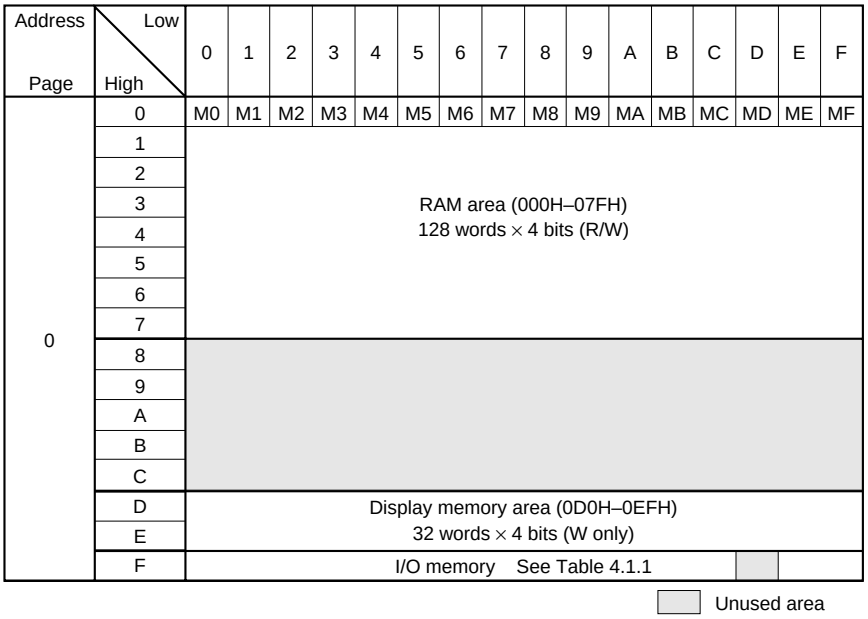


Fig. 4.1.1 Memory map

Note: Memory is not mounted in unused area within the memory map and in memory area not indicated in this chapter. For this reason, normal operation cannot be assured for programs that have been prepared with access to these areas.

Table 4.1.1 I/O memory map

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
0F0H	REMSO	IREM	IK1	IK0	REMSO	0	On	Off	Forced REM output (on/off)
					IREM *4	– *5	Yes	No	Interrupt factor flag (REM)
	R/W	R			IK1 *4	0	Yes	No	Interrupt factor flag (K10–K13)
					IK0 *4	0	Yes	No	Interrupt factor flag (K00–K03)
0F1H	WDRST	IT2	IT8	IT32	WDRST	Reset	Reset	–	Watchdog timer reset
					IT2 *4	0	Yes	No	Interrupt factor flag (clock timer 2 Hz)
	W	R			IT8 *4	0	Yes	No	Interrupt factor flag (clock timer 8 Hz)
					IT32 *4	0	Yes	No	Interrupt factor flag (clock timer 32 Hz)
0F2H	REMC	EIREM	EIK1	EIK0	REMC	1	On	Off	REM carrier generation on/off
					EIREM	0	Enable	Mask	Interrupt mask register (REM)
	R/W				EIK1	0	Enable	Mask	Interrupt mask register (K10–K13)
					EIK0	0	Enable	Mask	Interrupt mask register (K00–K03)
0F3H	TMRUN	EIT2	EIT8	EIT32	TMRUN	0	Run	Reset,Stop	Timer run/reset & stop
					EIT2	0	Enable	Mask	Interrupt mask register (clock timer 2 Hz)
	R/W				EIT8	0	Enable	Mask	Interrupt mask register (clock timer 8 Hz)
					EIT32	0	Enable	Mask	Interrupt mask register (clock timer 32 Hz)
0F4H	TM03	TM02	TM01	TM00	TM03	0			Timer data (16 Hz)
					TM02	0			Timer data (32 Hz)
	R				TM01	0			Timer data (64 Hz)
					TM00	0			Timer data (128 Hz)
0F5H	TM13	TM12	TM11	TM10	TM13	0			Timer data (1 Hz)
					TM12	0			Timer data (2 Hz)
	R				TM11	0			Timer data (4 Hz)
					TM10	0			Timer data (8 Hz)
0F6H	0	0	CLKCHG	OSCC	0 *3	– *2	–	–	Unused
					0 *3	– *2	–	–	Unused
	R		R/W		CLKCHG	0	OSC1	OSC3	CPU clock change
					OSCC	1	On	Off	OSC3 oscillation on/off
0F7H	RCDIV	RCDUTY	RT1	RT0	RCDIV	– *5			REM carrier interval and duty ratio setting → D3 D2 Div. ratio Duty: 0 0 1/8 1/4; 0 1 1/8 3/8; 1 0 1/12 1/3; 1 1 1/12 1/4
					RCDUTY	– *5			
	R/W				RT1	– *5			τ cycle (division ratio) setting
					RT0	– *5			0: 1/12, 1: 1/16, 2: 1/20, 3: 1/32
0F8H	RIC3	RIC2	RIC1	RIC0	RIC3	– *5			REM interrupt counter (0τ to 14τ)
					RIC2	– *5			
	W				RIC1	– *5			
					RIC0	– *5			
0F9H	ROUT1	ROUT0	MF91	MF90	ROUT1	0			REM output duration setting (0τ to 3τ)
					ROUT0	0			
	R/W				MF91	– *5			General-purpose register
					MF90	– *5			General-purpose register
0FAH	K03	K02	K01	K00	K03	– *2	High	Low	K0 input port data
					K02	– *2	High	Low	
	R				K01	– *2	High	Low	
					K00	– *2	High	Low	
0FBH	K13	K12	K11	K10	K13	– *2	High	Low	K1 input port data
					K12	– *2	High	Low	
	R				K11	– *2	High	Low	
					K10	– *2	High	Low	
0FCH	R03 BZ	R02 $\overline{BZ}$ $\overline{FOUT}$	R01	R00	R03	0	High	Low	R03 output port data
					BZ	0	On	Low	Signal on/off when BZ is selected. (mask option)
					R02	0	High	Low	R02 output port data
	R/W				$\overline{BZ}$/$\overline{FOUT}$	0	On	Low	Signal on/off when $\overline{BZ}$/$\overline{FOUT}$ is selected. (mask option)
					R01	0	High	Low	R01 output port data
					R00	0	High	Low	R00 output port data
0FEH	P03	P02	P01	P00	P03	– *2	High	Low	P0 I/O port data
					P02	– *2	High	Low	
	R/W				P01	– *2	High	Low	
					P00	– *2	High	Low	
0FFH	0	0	IOC	0	0 *3	– *2	–	–	Unused
					0 *3	– *2	–	–	Unused
	R		R/W	R	IOC	0	Output	Input	I/O port I/O control
					0 *3	– *2	–	–	Unused

*1 Initial value at initial reset
*2 Not set in the circuit
*3 Always "0" being read
*4 Reset (0) immediately after being read
*5 Undefined

4.2 Watchdog Timer

4.2.1 Configuration of watchdog timer

The E0C6006 has a built-in watchdog timer that operates with a divided clock from the OSC1 as the source clock. The watchdog timer must be reset cyclically by the software while it operates. If the watchdog timer is not reset in at least 3–4 seconds (when fOSC1 is 32.768 kHz), it resets the CPU.
Figure 4.2.1.1 is the block diagram of the watchdog timer.

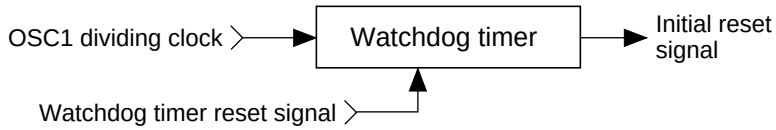


Fig. 4.2.1.1 Watchdog timer block diagram

Watchdog timer reset processing in the program's main routine enables detection of program overrun, such as when the main routine's watchdog timer processing is bypassed. Ordinarily this routine is incorporated where periodic processing takes place, just as for the timer interrupt routine.
The watchdog timer operates in the HALT mode. If a HALT status continues for 3–4 seconds, the watchdog timer generates a CPU reset signal.

The watchdog timer function can be nullified by using the mask option.

4.2.2 I/O memory of watchdog timer

Table 4.2.2.1 shows the I/O address and control bit for the watchdog timer.

Table 4.2.2.1 Control bit of watchdog timer

Address	Register								Comment
	D3	D2	D1	D0	Name	Init *1	1	0	
0F1H	WDRST	IT2	IT8	IT32	WDRST	Reset	Reset	–	Watchdog timer reset
					IT2 *4	0	Yes	No	Interrupt factor flag (clock timer 2 Hz)
	W	R			IT8 *4	0	Yes	No	Interrupt factor flag (clock timer 8 Hz)
					IT32 *4	0	Yes	No	Interrupt factor flag (clock timer 32 Hz)

*1 Initial value at initial reset
*2 Not set in the circuit
*3 Always "0" being read
*4 Reset (0) immediately after being read
*5 Undefined

WDRST: Watchdog timer reset (0F1H•D3)
Resets the watchdog timer.

When "1" is written: Watchdog timer is reset
When "0" is written: No operation
Reading: Always "0"

When "1" is written to WDRST, the watchdog timer is reset and restarts immediately after that. When "0" is written, no operation results.
This bit is dedicated for writing, and is always "0" for reading.

4.2.3 Programming note

When the watchdog timer is being used, the software must reset it within 3-second cycles.

4.3 Oscillation Circuit

4.3.1 Configuration of oscillation circuit

The E0C6006 has two oscillation circuits (OSC1 and OSC3). OSC1 is a crystal oscillation circuit that supplies the operating clock to the CPU and peripheral circuits. OSC3 is either a CR or a ceramic oscillation circuit. When processing with the E0C6006 requires high-speed operation, the CPU operating clock can be switched from OSC1 to OSC3 by the software. Figure 4.3.1.1 is the block diagram of this oscillation system.

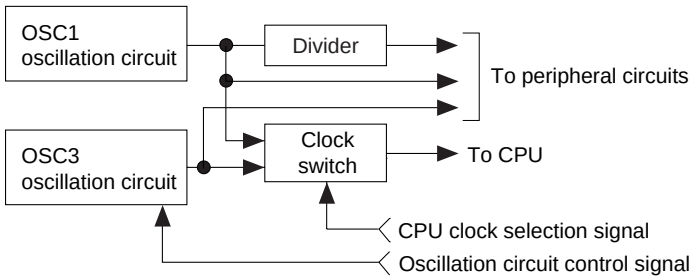


Fig. 4.3.1.1 Oscillation system block diagram

4.3.2 OSC1 oscillation circuit

The OSC1 crystal oscillation circuit generates the main clock for the CPU and the peripheral circuits. The oscillation frequency is 32.768 kHz (Typ.). Figure 4.3.2.1 is the block diagram of the OSC1 oscillation circuit.

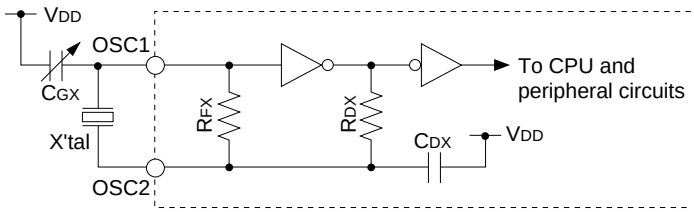
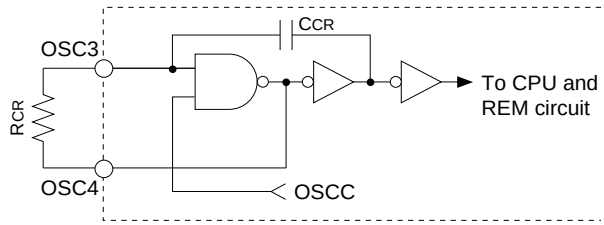


Fig. 4.3.2.1 OSC1 oscillation circuit (crystal)

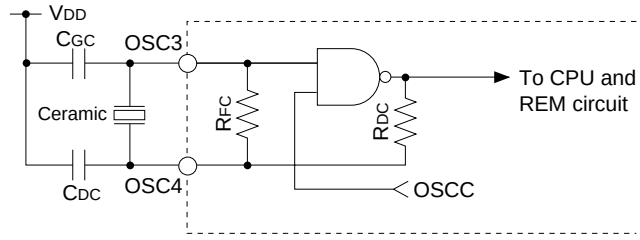
As shown in Figure 4.3.2.1, the crystal oscillation circuit can be configured simply by connecting the crystal oscillator (X'tal) of 32.768 kHz (Typ.) between the OSC1 and OSC2 terminals and the trimmer capacitor (CGX) between the OSC1 and VDD terminals.

4.3.3 OSC3 oscillation circuit

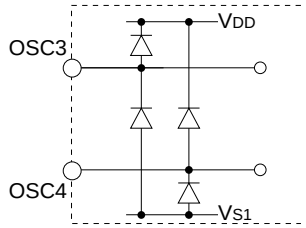
The E0C6006 has built-in the OSC3 oscillation circuit that generates the CPU's sub-clock (Typ. 455 kHz) for high speed operation and the source clock for peripheral circuits needing a high speed clock (REM circuit). The mask option enables selection of either the CR or ceramic oscillation circuit. When CR oscillation is selected, only a resistance is required as an external element. When ceramic oscillation is selected, a ceramic oscillator and two capacitors (gate and drain capacitance) are required.
Figure 4.3.3.1 is the block diagram of the OSC3 oscillation circuit.



(a) CR oscillation circuit



(b) Ceramic oscillation circuit



(c) When "Not Use" is selected by mask option

Fig. 4.3.3.1 OSC3 oscillation circuit

As shown in Figure 4.3.3.1, the CR oscillation circuit can be configured simply by connecting the resistor RCR between the OSC3 and OSC4 terminals when CR oscillation is selected. See Chapter 6, "Electrical Characteristics" for resistance value of RCR.
When ceramic oscillation is selected, the ceramic oscillation circuit can be configured by connecting the ceramic oscillator (Typ. 455 kHz) between the OSC3 and OSC4 terminals, capacitor CGC between the OSC3 and VDD terminals, and capacitor CDC between the OSC4 and VDD terminals. For both CGC and CDC, connect capacitors that are about 100 pF.
The OSC3 ocsillation circuit can be controlled (on and off) using the OSCC register. To reduce current consumption, the OSC3 oscillation circuit should be stopped by the software (OSCC register) if unnecessary.
When "Not Use" is selected by mask option, do not connect anything to the OSC3 and OSC4 terminals.

4.3.4 Switching the system clock

The CPU system clock is switched to OSC1 or OSC3 by the software (CLKCHG register).
When OSC3 is to be used as the CPU clock, it should be done as the following procedure using the software: turn the OSC3 oscillation ON and wait at least 5 msec for oscillation stabilization, then switch the CPU clock after waiting 5 msec or more.
When switching from OSC3 to OSC1, switch the CPU clock, then turn the OSC3 oscillation circuit off.

OSC1 → OSC3

1. Set OSCC to "1" (OSC3 oscillation ON).
2. Maintain 5 msec or more.
3. Set CLKCHG to "1" (OSC1 → OSC3).

OSC3 → OSC1

1. Set CLKCHG to "0" (OSC3 → OSC1).
2. Set OSCC to "0" (OSC3 oscillation OFF).

4.3.5 Clock frequency and instruction execution time

Table 4.3.5.1 shows the instruction execution time according to each frequency of the system clock.

Table 4.3.5.1 Clock frequency and instruction execution time

Clock frequency	Instruction execution time (µsec)		
	5-clock instruction	7-clock instruction	12-clock instruction
OSC1: 32.768 kHz	152.6	213.6	366.2
OSC3: 455 kHz	11.0	15.4	26.4

4.3.6 I/O memory of oscillation circuit

Table 4.3.6.1 shows the I/O address and the control bits for the oscillation circuit.

Table 4.3.6.1 Control bits of oscillation circuit

Address	Register								Comment
	D3	D2	D1	D0	Name	Init *1	1	0	
0F6H	0	0	CLKCHG	OSCC	0 *3	– *2	–	–	Unused
					0 *3	– *2	–	–	Unused
	R		R/W		CLKCHG	0	OSC1	OSC3	CPU clock change
					OSCC	1	On	Off	OSC3 oscillation on/off

*1 Initial value at initial reset
*2 Not set in the circuit
*3 Always "0" being read
*4 Reset (0) immediately after being read
*5 Undefined

OSCC: OSC3 oscillation control register (0F6H•D0)

Controls oscillation for the OSC3 oscillation circuit.

When "1" is written: OSC3 oscillation ON
When "0" is written: OSC3 oscillation OFF
Reading: Valid

When it is necessary to operate the CPU at high speed or output a remote control carrier signal, set OSCC to "1". At other times, set it to "0" to reduce current consumption.
At initial reset, this register is set to "1".

CLKCHG: CPU system clock switching register (0F6H•D1)

The CPU's operation clock is selected with this register.

When "1" is written: OSC1 clock is selected
When "0" is written: OSC3 clock is selected
Reading: Valid

When the CPU clock is to be OSC3, set CLKCHG to "0"; for OSC1, set CLKCHG to "1".
After turning the OSC3 oscillation ON (OSCC = "1"), switching of the clock should be done after waiting 5 msec or more.
At initial reset, this register is set to "0".

4.3.7 Programming notes

(1) It takes at least 5 msec from the time the OSC3 oscillation circuit goes on until the oscillation stabilizes. Consequently, when switching the CPU operation clock from OSC1 to OSC3, do this after a minimum of 5 msec have elapsed since the OSC3 oscillation went on.
Further, the oscillation stabilization time varies depending on the external oscillator characteristics and conditions of use, so allow ample margin when setting the wait time.

(2) When switching the clock from OSC3 to OSC1, use a separate instruction for switching the OSC3 oscillation off. An error in the CPU operation can result if this processing is performed at the same time by the one instruction.

4.4 Input Ports (K00–K03, K10–K13)

4.4.1 Configuration of input port

The E0C6006 has two 4-bit general-purpose input ports (K00–K03 and K10–K13). As shown in Figure 4.4.1.1, each input port terminal is provided with a pull-up and a feedback pull-up so that the port is suitable for push switch or key matrix switch input. As the pull-up can be removed by using mask option, the input port can also be used for slide switch input or interface with another LSI.

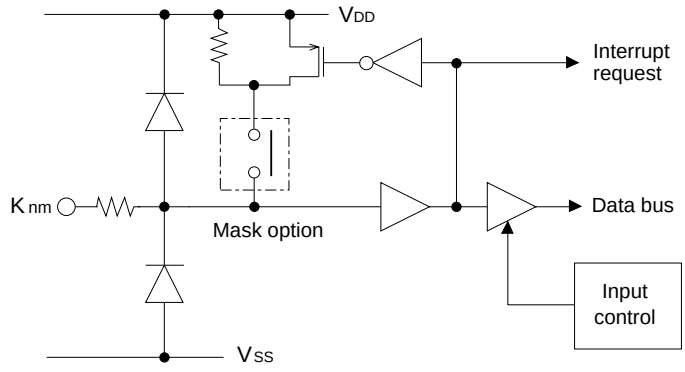


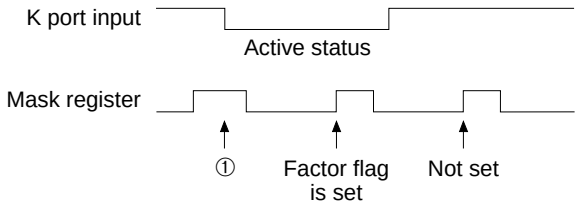
Fig. 4.4.1.1 Configuration of input port

Input port data can be read on a 4-bit basis (K00–K03, K10–K13) addressed 0FAH and 0FBH.

4.4.2 Interrupt function

All input port bits (K00–K03, K10–K13) provide the interrupt function.
The interrupt mask registers (EIK0, EIK1) enable the interrupt mask to be selected individually for K0 and K1 terminal groups. An interrupt occurs at the falling edge of an input signal which is not masked and the interrupt factor flags (IK0, IK1) is set to "1".

Input interrupt programming related precautions



When the content of the mask register is rewritten, while the port K input is in the active status. The input interrupt factor flag is set at ①.

Fig. 4.4.2.1 Input interrupt timing

When using an input interrupt, if you rewrite the content of the mask register, when the value of the input terminal which becomes the interrupt input is in the active status (input terminal = low status), the factor flag for input interrupt may be set.
For example, a factor flag is set with the timing of ① shown in Figure 4.4.2.1. However, when clearing the content of the mask register with the input terminal kept in the low status and then setting it, the factor flag of the input interrupt is again set at the timing that has been set.
Consequently, when the input terminal is in the active status (low status), do not rewrite the mask register (clearing, then setting the mask register), so that a factor flag will only set at the falling edge in this case. When clearing, then setting the mask register, set the mask register, when the input terminal is not in the active status (high status).

4.4.3 Mask option

An internal pull-up resistor can be selected for each of the eight bits of the input ports (K00–K03, K10–K13). Having selected "pull-up resistor disabled", take care that the input does not float. Select "pull-up resistor enabled" for input ports that are not being used.

4.4.4 I/O memory of input port

Table 4.4.4.1 shows the I/O addresses and the control bits for the input port.

Table 4.4.4.1 Control bits of input port

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
0F0H	REMSO	IREM	IK1	IK0	REMSO	0	On	Off	Forced REM output (on/off)
					IREM *4	– *5	Yes	No	Interrupt factor flag (REM)
	R/W	R			IK1 *4	0	Yes	No	Interrupt factor flag (K10–K13)
					IK0 *4	0	Yes	No	Interrupt factor flag (K00–K03)
0F2H	REMC	EIREM	EIK1	EIK0	REMC	1	On	Off	REM carrier generation on/off
					EIREM	0	Enable	Mask	Interrupt mask register (REM)
	R/W				EIK1	0	Enable	Mask	Interrupt mask register (K10–K13)
					EIK0	0	Enable	Mask	Interrupt mask register (K00–K03)
0FAH	K03	K02	K01	K00	K03	– *2	High	Low	K0 input port data
					K02	– *2	High	Low	
	R				K01	– *2	High	Low	
					K00	– *2	High	Low	
0FBH	K13	K12	K11	K10	K13	– *2	High	Low	K1 input port data
					K12	– *2	High	Low	
	R				K11	– *2	High	Low	
					K10	– *2	High	Low	

*1 Initial value at initial reset
*2 Not set in the circuit
*3 Always "0" being read
*4 Reset (0) immediately after being read
*5 Undefined

K00–K03: Input port data (0FAH)
K10–K13: Input port data (0FBH)

The input data of the input port terminals can be read with these registers.

When "1" is read: High level
When "0" is read: Low level
Writing: Invalid

The value read is "1" when the terminal voltage of the input port (K00–K03, K10–K13) goes high (V_{DD}), and "0" when the voltage goes low (V_{SS}). These bits are reading only, so writing cannot be done.

EIK0, EIK1: Interrupt mask registers (0F2H•D0, D1)

Masking the interrupt of the input port terminal groups can be done with these registers.

When "1" is written: Enabled
When "0" is written: Masked
Reading: Valid

With these registers, masking of the input port bits can be done for each of the four-bit terminal groups. At initial reset, these registers are all set to "0".

IK0, IK1: Interrupt factor flags (0F0H•D0, D1)

These flags indicate the occurrence of an input interrupt.

When "1" is read: Interrupt has occurred
When "0" is read: Interrupt has not occurred
Writing: Invalid

IK0 and IK1 are the interrupt factor flags corresponding to the input ports K00–K03 and K10–K13, respectively. They are set to "1" at the falling edge of the input signal. From the status of this flag, the software can decide whether an input interrupt has occurred or not.
These flags are reset when the software has read them.
Reading of interrupt factor flag is available at EI, but be careful in the following cases.
If the interrupt mask register value corresponding to the interrupt factor flag to be read is set to "1", an interrupt request will be generated by the interrupt factor flag set timing, or an interrupt request will not be generated. Be very careful when interrupt factor flags are in the same address.
At initial reset, this flag is set to "0".

4.4.5 Programming notes

(1) When modifying the input port from low level to high level with pull-up resistor, a delay will occur at the rise of the waveform due to time constant of the pull-up resistor and input gate capacities. Provide appropriate waiting time in the program when reading an input port.

(2) Reading of the interrupt factor flag is available at EI, but be careful in the following cases.
If the interrupt mask register value corresponding to the interrupt factor flag to be read is set to "1", an interrupt request will be generated by the interrupt factor flag set timing, or an interrupt request will not be generated. Be very careful when interrupt factor flags are in the same address.

4.5 Output Ports (R00–R03)

4.5.1 Configuration of output port

The E0C6006 has 4 bits of general output ports (R00–R03).
Output specifications of the output ports can be selected individually with the mask option. Two kinds of output specifications are available: complementary output and Nch open drain output. Also, the mask option enables the output ports R02 and R03 to be used as special output ports. Figure 4.5.1.1 shows the configuration of the output port.

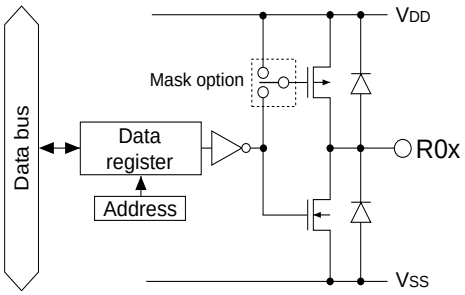


Fig. 4.5.1.1 Configuration of output ports

In the DC output mode, the output terminal goes high (VDD) when "1" is written to the data register and goes low (VSS) when "0" is written. At initial reset, the output terminal goes low.

4.5.2 Mask option

The mask option enables the following output port selection.

(1) Output specifications of output ports

The output specifications for the output port (R00–R03) can be selected from complementary output and Nch open drain output for each of the four bits. However, even when Nch open drain output is selected, a voltage exceeding the power voltage must not be supplied to the output port.

(2) Special output

In addition to the regular DC output, special output clock signal can be selected for output ports R02 and R03, as shown in Table 4.5.2.1.

Table 4.5.2.1 Special output

Output port	Special output
R02	$\overline{FOUT}$ or $\overline{BZ}$ output
R03	BZ output

The signal frequencies can also be selected by mask option.

4.5.3 Special output

Figure 4.5.3.1 shows the structure of output ports R00–R03.
As shown in the previous section, the R02 terminal and the R03 terminal can be used as special output ports by selecting mask option.

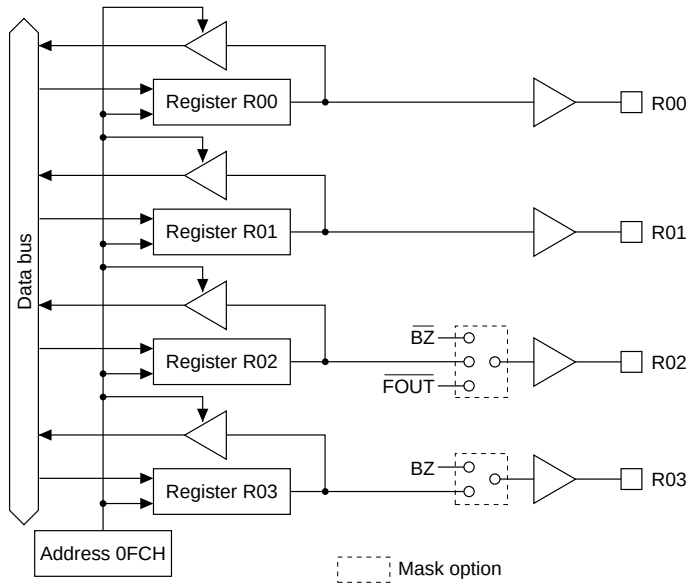


Fig. 4.5.3.1 Structure of output port R00–R03

$\overline{\text{FOUT}}$ (R02)

When the output port R02 is set as the $\overline{\text{FOUT}}$ output port, the R02 will output the clock generated from the OSC1 oscillation clock (f_{OSC1}). The clock frequency can be selected from among 8 types by mask option

Table 4.5.3.1 $\overline{FOUT}$ clock frequency

No.	Dividing ratio	Frequency *
1	f_{OSC1}	32768 Hz
2	f_{OSC1}/2	16384 Hz
3	f_{OSC1}/4	8192 Hz
4	f_{OSC1}/8	4096 Hz
5	f_{OSC1}/16	2048 Hz
6	f_{OSC1}/32	1024 Hz
7	f_{OSC1}/64	512 Hz
8	f_{OSC1}/128	256 Hz

∗ When f_{OSC1} = 32.768 kHz

When "1" is written to the $\overline{\text{FOUT}}$ (R02) register, the $\overline{\text{FOUT}}$ (R02) terminal outputs the clock with the selected frequency. When "0" is written, the $\overline{\text{FOUT}}$ (R02) terminal goes low.
Figure 4.5.3.2 shows the output waveform of the $\overline{\text{FOUT}}$ output.

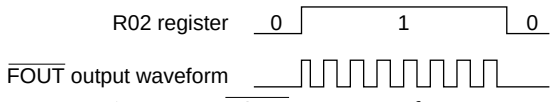


Fig. 4.5.3.2 $\overline{FOUT}$ output waveform

Note: A hazard may occur when the $\overline{FOUT}$ signal is turned on or off.

BZ, $\overline{BZ}$ (R03, R02)

The output ports R03 and R02 can be set to BZ output port and $\overline{BZ}$ output (BZ reverse output) port, respectively. However, when $\overline{FOUT}$ output is selected for the R02 terminal, $\overline{BZ}$ output cannot be selected.

Direct driving of piezo-electric buzzer

By setting the R03 to the BZ output port and the R02 to the $\overline{BZ}$ output port, these two terminals can directly drive a piezo-electric buzzer. The $\overline{BZ}$ output (R02) can only be set if the R03 is set to the BZ output.
At initial reset, the output terminals go low.
When "1" is written to the BZ (R03)/$\overline{BZ}$ (R02) registers, the output terminals output the buzzer signals.
When "0" is written, the terminals go low.
Figure 4.5.3.3 shows the buzzer direct drive waveform.

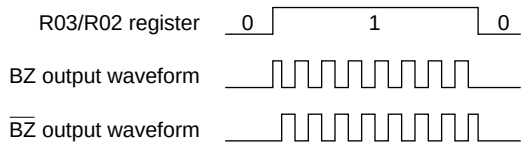


Fig. 4.5.3.3 Buzzer output waveform (direct driving)

Single terminal driving of piezo-electric buzzer

The piezo-electric buzzer can be driven with one terminal by setting the R03 to the BZ output terminal.
At initial reset, the BZ output goes off and the output terminal (R03) is set to low level.
When "1" is written to the BZ (R03) register, the output terminal output the BZ signal.
Figure 4.5.3.4 shows the BZ output waveform in single terminal driving.

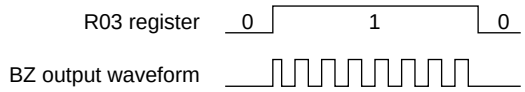


Fig. 4.5.3.4 Buzzer output waveform (single terminal driving)

Busser signal frequency

The buzzer signal frequency can be selected from 2 types ($f_{OSC1}/8$, $f_{OSC1}/16$) by the mask option. When the OSC1 oscillation frequency is 32.768 kHz, they becomes 4 kHz and 2 kHz, respectively.

4.5.4 I/O memory of output ports

Table 4.5.4.1 shows the I/O address and the control bits for the output port.

Table 4.5.4.1 Control bits of output port

Address	Register								Comment
	D3	D2	D1	D0	Name	Init *1	1	0	
0FCH	R03 / BZ	R02 / $\overline{BZ}$ / $\overline{FOUT}$	R01	R00	R03	0	High	Low	R03 output port data
					BZ	0	On	Low	Signal on/off when BZ is selected. (mask option)
					R02	0	High	Low	R02 output port data
					$\overline{BZ}$/$\overline{FOUT}$	0	On	Low	Signal on/off when $\overline{BZ}$/$\overline{FOUT}$ is selected. (mask option)
	R/W				R01	0	High	Low	R01 output port data
					R00	0	High	Low	R00 output port data

*1 Initial value at initial reset
*2 Not set in the circuit
*3 Always "0" being read
*4 Reset (0) immediately after being read
*5 Undefined

R00–R03: Output port data (0FCH)

Sets the output data for the output ports.

When "1" is written: High output
When "0" is written: Low output
Reading: Valid

The output port terminals output the data written to the corresponding registers (R00–R03) without changing it. When "1" is written to the register, the output port terminal goes high (V_{DD}), and when "0" is written, the output port terminal goes low (V_{SS}).
At initial reset, these registers are all set to "0".

R02 (when $\overline{FOUT}$ is selected): Special output control (0FCH•D2)

Controls the $\overline{FOUT}$ (clock) output.

When "1" is written: Clock output
When "0" is written: Low level (DC) output
Reading: Valid

When "1" is written to the $\overline{FOUT}$ (R02) register, the $\overline{FOUT}$ (R02) terminal outputs the $\overline{FOUT}$ signal. When "0" is written, the terminal goes low.
At initial reset, this register is set to "0".

R02, R03 (when buzzer output is selected): Special output port data (0FCH•D2, D3)

Controls the buzzer output.

When "1" is written: Buzzer output
When "0" is written: Low level (DC) output
Reading: Valid

The $\overline{BZ}$ and BZ outputs can be controlled by writing data to the R02 and R03 registers.
At initial reset, these registers are set to "0".

4.5.5 Programming note

The $\overline{FOUT}$ and buzzer output signals may produce hazards when the output ports R02 and R03 are turned on or off.

4.6 I/O Ports (P00–P03)

4.6.1 Configuration of I/O port

The E0C6006 has 4 bits of general-purpose I/O ports. Figure 4.6.1.1 shows the configuration of the I/O ports. The I/O ports P00–P03 can be set to either input mode or output mode by writing data to the I/O control register (IOC).

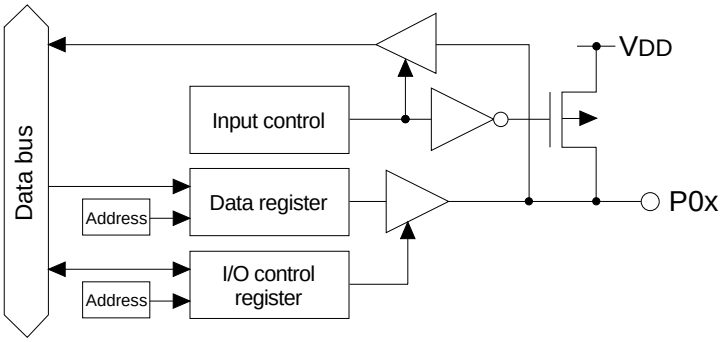


Fig. 4.6.1.1 Configuration of I/O port

4.6.2 I/O control register and I/O mode

Input or output mode can be set for the I/O ports P00–P03 by writing data to the I/O control register IOC.

To set the input mode, write "0" to the I/O control register (IOC). When the I/O ports are set to the input mode, the terminals become high impedance and they work as input ports. The input line is pulled up during read operation.

The output mode is set when "1" is written to the I/O control register (IOC). When the I/O ports are set to the output mode, they work as output ports and output a high signal (V_{DD}) when the port output data is "1", and a low signal (V_{SS}) when the port output data is "0". If perform the read out in each mode; when output mode, the register value is read out, and when input mode, the port value is read out.

At initial reset, the I/O control register is set to "0", and the I/O ports enter the input mode.

4.6.3 I/O memory of I/O port

Table 4.6.3.1 shows the I/O addresses and the control bits for the I/O port.

Table 4.6.3.1 Control bits of I/O port

Address	Register								Comment
	D3	D2	D1	D0	Name	Init *1	1	0	
0FEH	P03	P02	P01	P00	P03	– *2	High	Low	P0 I/O port data
					P02	– *2	High	Low	
	R/W				P01	– *2	High	Low	
					P00	– *2	High	Low	
0FFH	0	0	IOC	0	0 *3	– *2	–	–	Unused
					0 *3	– *2	–	–	Unused
	R		R/W	R	IOC	0	Output	Input	I/O port I/O control
					0 *3	– *2	–	–	Unused

*1 Initial value at initial reset
*2 Not set in the circuit
*3 Always "0" being read
*4 Reset (0) immediately after being read
*5 Undefined

P00–P03: I/O port data register (0FEH)

I/O port data can be read and output data can be written through this register.

• ***Writing***

When "1" is written: High level
When "0" is written: Low level

When the I/O port is set to the output mode, the written data is output from the I/O port terminal unchanged. When "1" is written as the port data, the port terminal goes high (V_{DD}), and when "0" is written, the level goes low (V_{SS}). Port data can also be written in the input mode.

• ***Reading***

When "1" is read: High level
When "0" is read: Low level

The terminal voltage level of the I/O port is read. When the I/O port is in the input mode the voltage level being input to the port terminal can be read; in the output mode the output voltage level can be read. When the terminal voltage is high (V_{DD}) the port data read is "1", and when the terminal voltage is low (V_{SS}) the data is "0".
When the port data is read, the built-in pull-up resistors go on and the I/O port terminals are pulled up.

IOC: I/O control register (0FFH•D1)

The input or output mode can be set with this register.

When "1" is written: Output mode
When "0" is written: Input mode
Reading: Valid

When "1" is written to the I/O control register, the I/O ports enter the output mode, and when "0" is written, the I/O ports enter the input mode.
At initial reset, this register is set to "0".

4.6.4 Programming notes

(1) When the I/O port is set to the output mode and a low-impedance load is connected to the port terminal, the data written to the register may differ from the data read.

(2) When the I/O port is set to the input mode and the input level changed from low (V_{SS}) to high (V_{DD}) through the built-in pull-up resistor, an erroneous input results if the time constant of the capacitive load of the input line and the built-in pull-up resistor is greater than the read-out time. When the input data is being read, the time that the input line is pulled up is equivalent to 0.5 cycles of the CPU system clock. Hence, the electric potential of the terminals must settle within 0.5 cycles. If this condition cannot be met, some measure must be devised, such as arranging a pull-up resistor externally, or performing multiple read-outs.

4.7 LCD Driver

4.7.1 Configuration of LCD driver

The E0C6006 has four common terminals (COM0–COM3) and 20 segment terminals (SEG0–SEG19), so that an LCD with a maximum of 80 (20 × 4) segments can be driven.
The driving method is 1/4 duty (1/3 duty can also be selected by mask option) dynamic drive, adopting the four types of potential, V_{DD}, V_{L1}, V_{L2} and V_{L3}.
The power for driving the LCD is generated by the internal circuit so that there is no need to apply power especially from outside.
The frame frequency is 32 Hz for 1/4 duty and 42.7 Hz for 1/3 duty (in the case of f_{OSC1} = 32.768 kHz).
Figures 4.7.1.1 and 4.7.1.2 show the drive waveform for 1/3 duty and 1/4 duty.

Table 4.7.1.1 LCD drive mode options

Duty	COM used	Max. number of segments	Frame frequency *
1/4	COM0–COM3	80 (20 × 4)	32 Hz
1/3	COM0–COM2	60 (20 × 3)	42.7 Hz

* When f_{OSC1} = 32 kHz

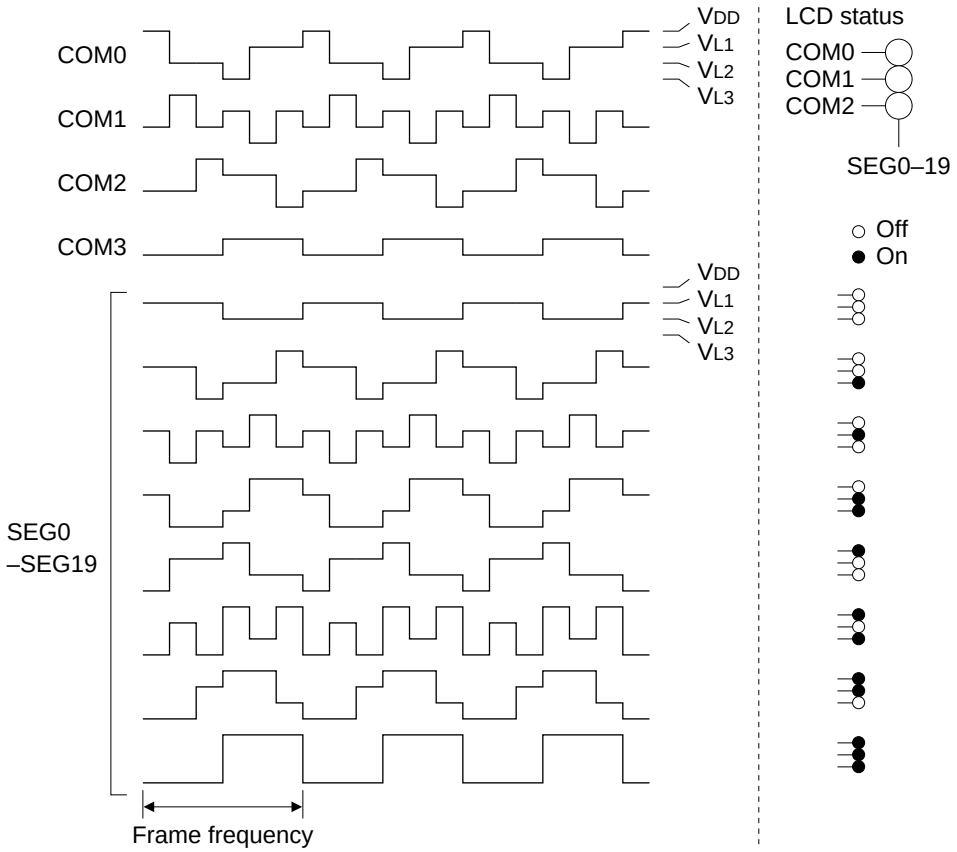


Fig. 4.7.1.1 Drive waveform for 1/3 duty

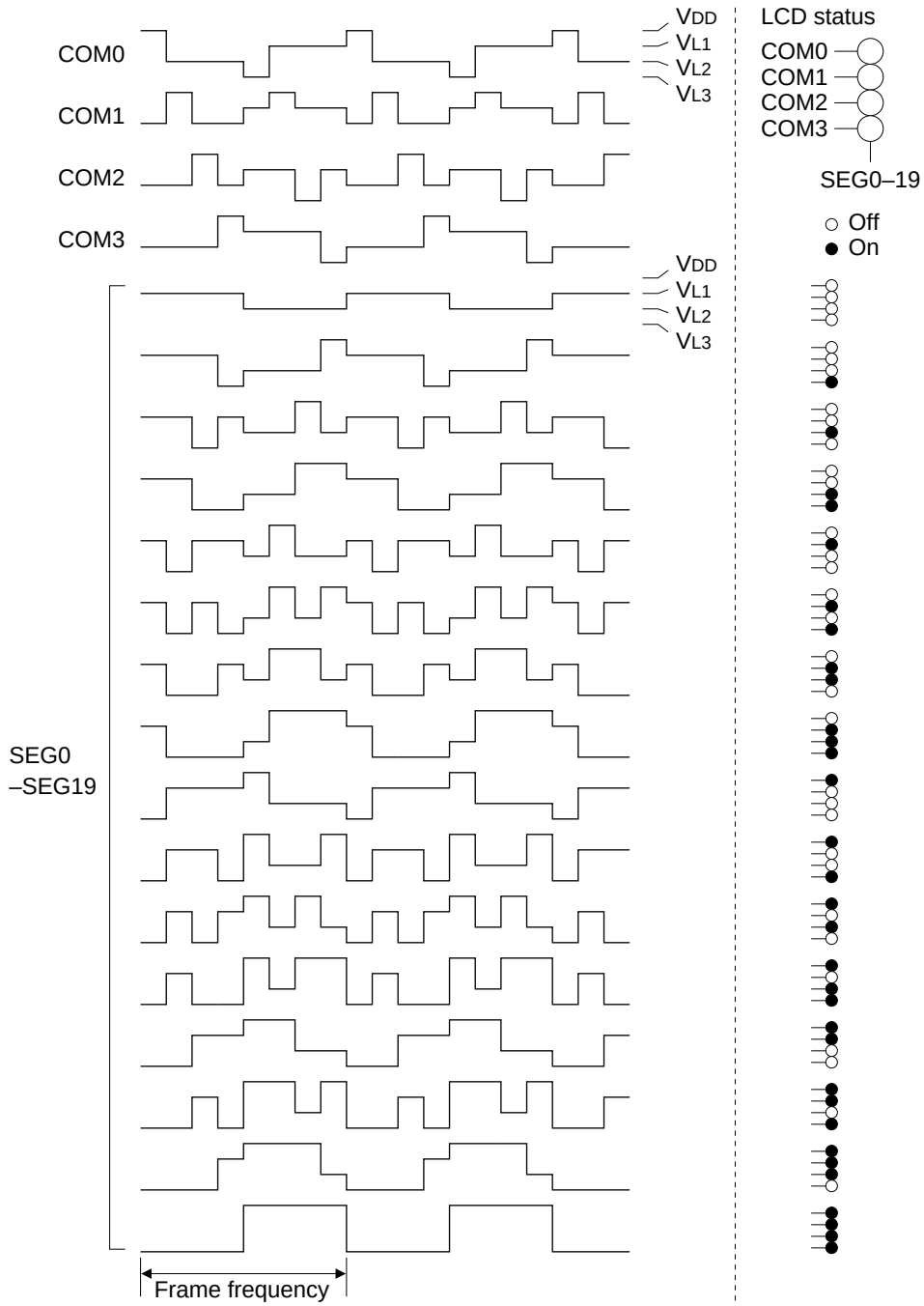


Fig. 4.7.1.2 Drive waveform for 1/4 duty

4.7.2 Mask option

(1) Segment allocation

The segment data is decided by the display data written to the display memory at address "0D0H–0EFH". Writing "1" to the display memory turns the associated LCD segment on, and writing "0" turns the LCD segment off.

The addresses and bits of the display memory can be made to correspond to the segment terminals (SEG0–SEG19) in any combination by mask option. This simplifies design by increasing the degree of freedom with which the liquid crystal panel can be designed.

Figure 4.7.2.1 shows an example of the relationship between the LCD segments (on the panel) and the display memory in the case of 1/3 duty.

Address	Data			
	D3	D2	D1	D0
0ECH	d	c	b	a
0EDH	p	g	f	e
0EEH	d'	c'	b'	a'
0EFH	p'	g'	f'	e'

Display memory allocation

	Common 0	Common 1	Common 2
SEG10	EC, D0 (a)	ED, D1 (f)	ED, D0 (e)
SEG11	EC, D1 (b)	ED, D2 (g)	EC, D3 (d)
SEG12	EF, D1 (f')	EC, D2 (c)	ED, D3 (p)

Pin address allocation

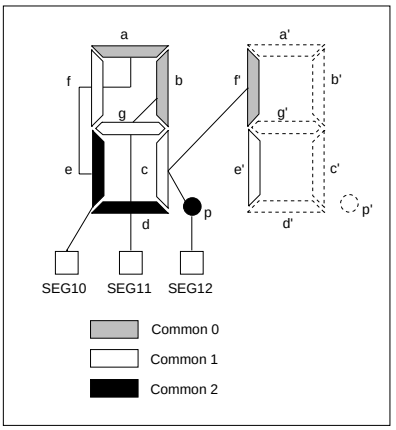


Fig. 4.7.2.1 Segment allocation

(2) Drive duty

Either 1/4 or 1/3 duty can be selected as the LCD drive duty.

4.7.3 Programming note

Because the display memory is for writing only, re-writing the contents with logical instructions (e.g., AND, OR, etc.) which come with read-out operations is not possible. To perform bit operations, a buffer to hold the display data is required on the RAM.

4.8 Clock Timer

4.8.1 Configuration of clock timer

The E0C6006 has a built-in clock timer that uses the OSC1 oscillation circuit as the clock source. The clock timer is configured as a 8-bit binary counter that counts with a 256 Hz source clock from the divider. The 8 bits of the counter (128 Hz–1 Hz) can be read by the software in 4-bit units.
Figure 4.8.1.1 is the block diagram of the clock timer.

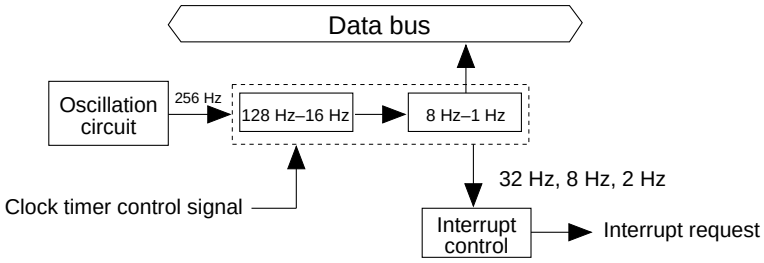


Fig. 4.8.1.1 Block diagram of clock timer

Normally, this clock timer is used for all kinds of timing purpose, such as clocks.

Note: The information given in this section is based on fOSC1 = 32.768 kHz. For a system which uses an oscillator having any other frequency at OSC1, substitute the appropriate value for 32.768 kHz throughout this section.

4.8.2 Interrupt function

The clock timer can generate interrupts at the falling edge of the 32 Hz, 8 Hz, and 2 Hz signals. The software can mask any of these interrupt signals.
Figure 4.8.2.1 is the timing chart of the clock timer.

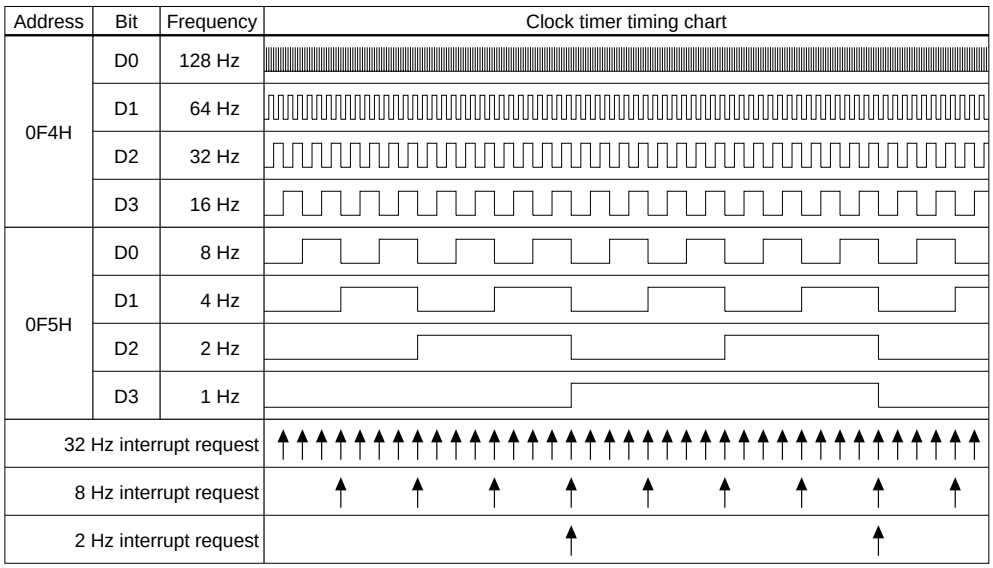


Fig. 4.8.2.1 Timing chart of the clock timer

As shown in Figure 4.8.2.1, an interrupt is generated at the falling edge of the 32 Hz, 8 Hz, and 2 Hz signals. At this point, the corresponding interrupt factor flag (IT32, IT8, IT2) is set to "1". The interrupts can be masked individually with the interrupt mask register (EIT32, EIT8, EIT2). However, regardless of the interrupt mask register setting, the interrupt factor flags will be set to "1" at the falling edge of their corresponding signal (e.g. the falling edge of the 2 Hz signal sets the 2 Hz interrupt factor flag to "1").

4.8.3 I/O memory of clock timer

Table 4.8.3.1 shows the I/O addresses and the control bits for the clock timer.

Table 4.8.3.1 Control bits of clock timer

Address	Register								Comment
	D3	D2	D1	D0	Name	Init *1	1	0	
0F1H	WDRST	IT2	IT8	IT32	WDRST	Reset	Reset	–	Watchdog timer reset
					IT2 *4	0	Yes	No	Interrupt factor flag (clock timer 2 Hz)
	W	R			IT8 *4	0	Yes	No	Interrupt factor flag (clock timer 8 Hz)
					IT32 *4	0	Yes	No	Interrupt factor flag (clock timer 32 Hz)
0F3H	TMRUN	EIT2	EIT8	EIT32	TMRUN	0	Run	Reset,Stop	Timer run/reset & stop
					EIT2	0	Enable	Mask	Interrupt mask register (clock timer 2 Hz)
	R/W				EIT8	0	Enable	Mask	Interrupt mask register (clock timer 8 Hz)
					EIT32	0	Enable	Mask	Interrupt mask register (clock timer 32 Hz)
0F4H	TM03	TM02	TM01	TM00	TM03	0			Timer data (16 Hz)
					TM02	0			Timer data (32 Hz)
	R				TM01	0			Timer data (64 Hz)
					TM00	0			Timer data (128 Hz)
0F5H	TM13	TM12	TM11	TM10	TM13	0			Timer data (1 Hz)
					TM12	0			Timer data (2 Hz)
	R				TM11	0			Timer data (4 Hz)
					TM10	0			Timer data (8 Hz)

*1 Initial value at initial reset
*2 Not set in the circuit
*3 Always "0" being read
*4 Reset (0) immediately after being read
*5 Undefined

TM00–TM03: Timer low-order data (0F4H)
TM10–TM13: Timer high-order data (0F5H)

The l28 Hz to 16 Hz timer data of the clock timer can be read from the TM00–TM03 register and 8 Hz to 1 Hz data can be read from the TM10–TM13 register. These eight bits are read-only, and write operations are invalid.
At initial reset, the timer data is initialized to "00H".

TMRUN: Clock timer control (0F3H•D3)

Starts, stops and resets the clock timer.

When "1" is written: Run
When "0" is written: Reset and stop
Reading: Valid

The clock timer starts counting by writing "1" to the TMRUN register. When "0" is written, the clock timer clears the count data and stops counting.
At initial reset, this register is set to "0".

EIT32, EIT8, EIT2: Interrupt mask registers (0F3H•D0–D2)

These registers are used to mask the clock timer interrupt.

When "1" is written: Enabled
When "0" is written: Masked
Reading: Valid

The interrupt mask registers (EIT32, EIT8, EIT2) mask the corresponding interrupt frequencies (32 Hz, 8 Hz, 2 Hz).
At initial reset, these registers are all set to "0".

IT32, IT8, IT2: Interrupt factor flags (0F1H•D0–D2)
These flags indicate the status of the clock timer interrupt.

When "1" is read: Interrupt has occurred
When "0" is read: Interrupt has not occurred
Writing: Invalid

The interrupt factor flags (IT32, IT8, IT2) correspond to the clock timer interrupts (32 Hz, 8 Hz, 2 Hz). The software can determine from these flags whether there is a clock timer interrupt. However, even if the interrupt is masked, the flags are set to "1" at the falling edge of the signal. These flags can be reset when the register is read by the software.
Reading of interrupt factor flags is available at EI, but be careful in the following cases.
If the interrupt mask register value corresponding to the interrupt factor flag to be read is set to "1", an interrupt request will be generated by the interrupt factor flag set timing, or an interrupt request will not be generated. Be very careful when interrupt factor flags are in the same address.
At initial reset, these flags are set to "0".

4.8.4 Programming notes

(1) Note that the frequencies and times differ from the description in this section when the oscillation frequency is not 32.768 kHz.

(2) Reading of interrupt factor flags is available at EI, but be careful in the following cases.
If the interrupt mask register value corresponding to the interrupt factor flag to be read is set to "1", an interrupt request will be generated by the interrupt factor flag set timing, or an interrupt request will not be generated. Be very careful when interrupt factor flags are in the same address.

4.9 Remote Controller (REM)

4.9.1 Configuration of remote controller

The E0C6006 has a remote controller (REM circuit) built-in. It can easily adapt to various remote controllers by connecting an infrared remote LED and a transistor as shown in Figure 4.9.1.1.

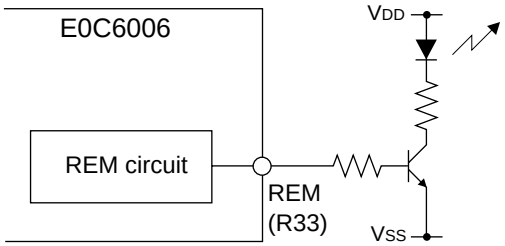


Fig. 4.9.1.1 Remote LED control circuit

Figure 4.9.1.2 shows the configuration of the REM circuit.

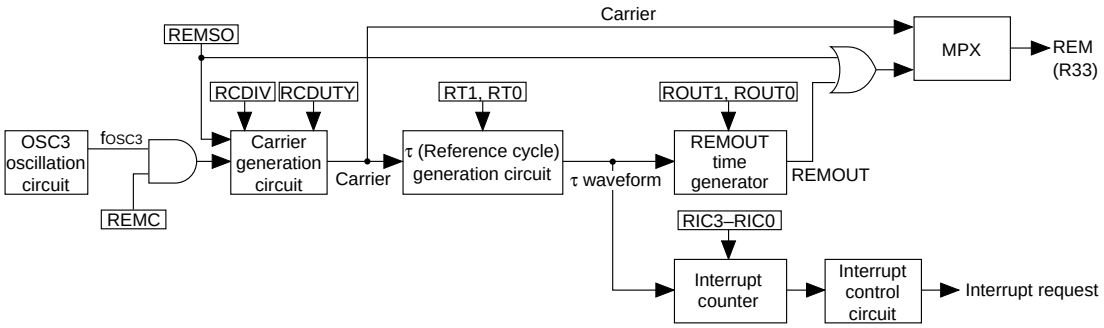


Fig. 4.9.1.2 Configuration of REM circuit

The generally used infrared remote controllers employ a method that generates transmission waveforms in pulse modulation as shown in Figure 4.9.1.3 and transmits the signal.
First the transmission code is modulated in a pulse phase modulation (PPM) method to generate the modulation signal, and the carrier that has constant frequency is amplitude-modulated (AM) using the modulation signal. As a result, transmission waveforms are generated. Transmission is done by driving the infrared LED using the transmission waveform.

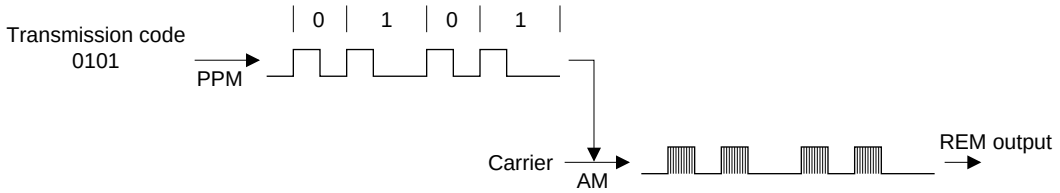


Fig. 4.9.1.3 Remote transmission method

In this remote controller, the carrier generated from the carrier generation circuit is controlled to turn the output ON and OFF and the transmission waveform is generated. This transmission waveform can be output from the REM (R33) terminal. At initial reset and while remote output stops, the REM terminal goes low level (VSS).
The carrier frequency and duty ratio can be selected by the software from among 4 types. (details are explained later)

This remote controller supports the following two modes for controlling the modulation signal (carrier ON/OFF).

- Soft-timer mode (Software timer control mode)
- Hard-timer mode (Hardware timer control mode)

In the soft-timer mode, the carrier ON/OFF timing and the time are controlled by the software. The optional ON/OFF time can be set within the range that is controlled by the software.
In the hard-timer mode, the carrier ON/OFF timing and the output time are controlled by the REMOUT time generator based on the reference cycle (τ) that is generated by the τ (reference cycle) generation circuit dividing the carrier. For the reference cycle (τ), the carrier dividing ratio can be selected by the software from 4 types. The REMOUT (REM output) time can be selected by the software from 4 types, 0 to 3 times as long as the reference cycle (τ). The ON/OFF time is limited to some extent in comparison with the soft-timer mode, but the software's share is decreased because the interrupt can be used.
Features of the soft-timer mode and hard-timer mode are shown in Table 4.9.1.1.

Table 4.9.1.1 Features of soft-timer mode and hard-timer mode

Item	Soft-timer mode	Hard-timer mode
Processing of other routines during REM output	Difficult	Possible
Reference cycle (τ) sway during REM transmission	Source oscillation sway and errors caused by instruction cycles	Source oscillation sway only
Setting of REM output width	Variable to any width	Fixed to several widths
Relation between REM reference cycle and modulation frequency cycle	Variable	Fixed to several cycles
Carrier waveform	Duty slightly disturbed before and after ON time	Stabilized at setting

4.9.2 Carrier

The carrier is generated by the carrier generation circuit using the OSC3 clock as the source clock.

Note: If an option is selected without use of OSC3, the OSC1 clock (instead of the OSC3 clock) is introduced into the REM circuit. For an option selected without using OSC3, the term "OSC3" should read "OSC1" in the description that follows.

The carrier cycle and duty ratio selections and the carrier generation circuit ON/OFF control can be done by the software.
The control for the carrier is same procedure for both the soft-timer mode and the hard-timer mode. Perform the carrier settings before starting the transmission in each mode.

The carrier cycle (selection as the dividing ratio of the OSC3 clock) and the duty ratio can be set using the RCDIV register (F7H•D3) and RCDUTY register (F7H•D2) as shown in Table 4.9.2.1.

Table 4.9.2.1 Carrier dividing ratio and duty ratio

RCDIV	RCDUTY	Carrier dividing ratio	Carrier duty ratio
0	0	f_{OSC3} / 8	1/4
0	1	f_{OSC3} / 8	3/8
1	0	f_{OSC3} / 12	1/3
1	1	f_{OSC3} / 12	1/4

f_{OSC3}: OSC3 oscillation frequency

Carrier settings can be done even when the OSC3 oscillation circuit is in OFF status. Furthermore, when these are set once, the set contents are maintained until an initial reset is performed.

Note: The setting of the RCDIV register and the RCDUTY register should be done when the REM circuit is OFF (REMC = "0") before starting remote transmission. If changing the contents when the REM circuit is ON, it may cause a malfunction.

The carrier generation circuit is switched to ON/OFF by the REMC register. By writing "1" to the register, the carrier generation circuit goes ON and generates the carrier. When the register is set to "0" by writing, the carrier generation circuit goes OFF and the carrier generation stops.
The OSC3 clock is divided to generate the carrier. Therefore, the OSC3 oscillation circuit must be ON before starting remote output. Remote output should be done when the OSC3 oscillation has stabilized.

Note: It takes at least 5 msec from the time the OSC3 oscillation circuit goes ON until the oscillation stabilizes. Consequently, when starting a remote output, secure 5 msec or more waiting time for oscillation stabilization after turning the OSC3 oscillation ON.

Further, the oscillation stabilization time varies depending on the external oscillator characteristics and conditions of use, so allow ample margin when setting the waiting time.

Figure 4.9.2.1 shows the carrier waveform.

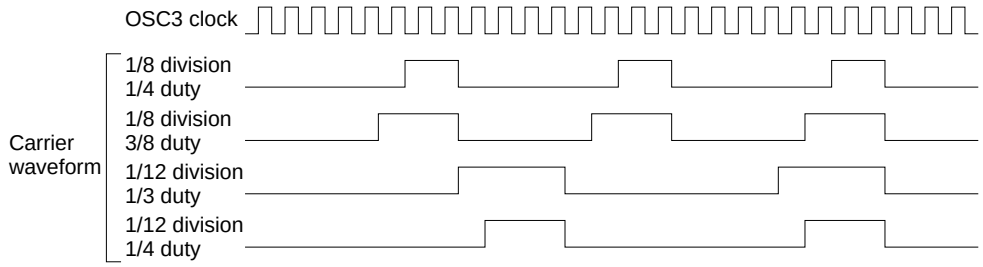


Fig. 4.9.2.1 Carrier waveform

The carrier generation circuit starts carrier output by writing "1" to the REMC register. When the REMC register is set to "0", the carrier output stops.

Note: Except when outputting the remote control waveform, REMC register should be fixed at "0" to prevent outputting unnecessary waveforms and to reduce current consumption. However at initial reset, the REMC register is set to "1" for initializing the carrier generation circuit. The register must not be set to "0" until after initialization (within 32 machine cycles).

4.9.3 Soft-timer mode

In the soft-timer mode, software controls the ON/OFF time and timing of the carrier output. This mode does not use the τ (reference cycle) generation circuit, REMOUT time generator and interrupt control circuit that are used in the hard-timer mode, and operates with the configuration as shown in Figure 4.9.3.1.

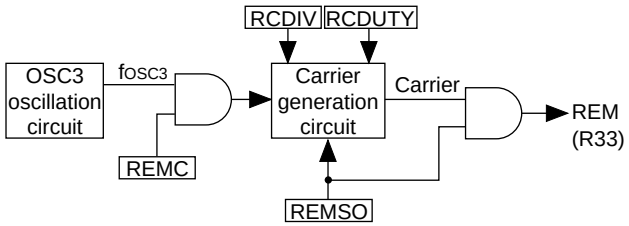


Fig. 4.9.3.1 REM circuit configuration in soft-timer mode

The ON/OFF control of the carrier output is done using the REMSO register (F0H•D3). By writing "1" to the REMSO register, the carrier is output to the REM terminal and when "0" is written, the REM terminal goes low level (VSS). However, the carrier must be generated by writing "1" to the REMC register before writing "1" to the REMSO register.
Figure 4.9.3.2 shows the timing chart in the soft-timer mode.

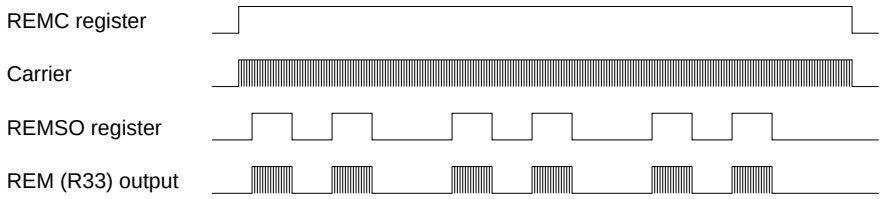


Fig. 4.9.3.2 Timing chart (soft-timer mode)

Note: • Writing to the REMSO register without synchronization with the carrier generation circuit, therefore when turning the carrier output ON/OFF using the REMSO register, the duty ratio of the carrier will not be the value set by the software. (Figure 4.9.3.3)

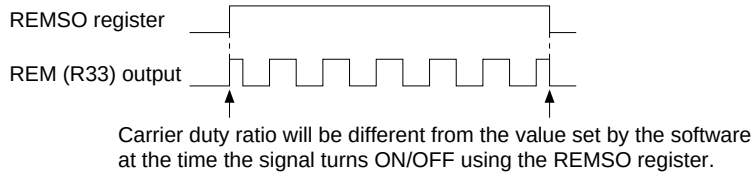


Fig. 4.9.3.3 Carrier ON/OFF by REMSO register

• Be sure to control the carrier output using the REMSO register. Do not control the carrier output using the REMC register by setting the REMSO register to "1".

4.9.4 Hard-timer mode and REM interrupt

In the soft-timer mode, the CPU is occupied for the remote output processing so that it has no flexibility for execution of other routines. To alleviate this problem, the E0C6006 supports the hard-timer mode explained below.

In the hard-timer mode, the carrier ON/OFF, that is controlled using the REMSO register in the soft-timer mode, is done in the hardware by using the τ (reference cycle) generation circuit and the REMOUT time generator. τ (reference cycle) is generated from the carrier by dividing, and is used for reference of the carrier ON/OFF time in the hard-timer mode. The dividing ratio of τ (reference cycle) is selected from 4 types by the software. The carrier ON/OFF time can be set for each transmission data bit by the software using τ (reference cycle) as reference. Furthermore, the interrupt function is provided so that the setting can be done without synchronizing with the timing of the carrier output.
The interrupt timing can also be set by the software using τ (reference cycle) as the reference same as the ON/OFF time.
The circuit in the hard-timer mode is configured as shown in Figure 4.9.1.2, and all the REM circuit is used. However, the REMSO register that is used to control the carrier output in the soft-timer mode should be fixed at "0". If "1" is written to the REMSO register, REM output are forcibly done regardless of the control of the hard-timer mode.

(1) τ (reference cycle)

τ (reference cycle) is used as reference for the carrier output ON time and interrupt timing specified by the software, and is generated by the τ (reference cycle) generation circuit by dividing carrier. This dividing ratio can be selected using the RT1–RT0 register (F7H•D1, D0) from 4 types as shown in Table 4.9.4.1.

Table 4.9.4.1 τ (reference cycle) setting

RT1	RT0	τ dividing ratio
0	0	fcarrier / 12
0	1	fcarrier / 16
1	0	fcarrier / 20
1	1	fcarrier / 32

* fcarrier indicates carrier frequency. It is selected with the RCDIV register (F7H•D3).

The actual time of τ (reference cycle) can be found using the following expression according to the OSC3 oscillation frequency, carrier cycle selection and the above selection.

τ (reference cycle) [sec] = 1 / (f_{OSC3} × DIV1 × DIV2)

f_{OSC3}: OSC3 oscillation frequency
DIV1: Content of carrier dividing ratio set with the RCDIV register (1/8 or 1/12)
DIV2: Content of τ dividing ratio set with the RT1 and RT0 registers (1/12, 1/16, 1/20 or 1/32)

Table 4.9.4.2 shows the examples of τ (reference cycle) when f_{OSC3} is 455 kHz.

Table 4.9.4.2 τ (reference cycle) examples

Register settings			τ (reference cycle)
RCDIV	RT1	RT0	f_{OSC3} = 455 kHz
0	0	0	0.211 msec (4739.6 Hz)
0	0	1	0.281 msec (3554.7 Hz)
0	1	0	0.352 msec (2843.8 Hz)
0	1	1	0.563 msec (1777.3 Hz)
1	0	0	0.316 msec (3159.7 Hz)
1	0	1	0.422 msec (2369.8 Hz)
1	1	0	0.527 msec (1895.8 Hz)
1	1	1	0.844 msec (1184.9 Hz)

The carrier output ON time can be set to 4 types (0τ to 3τ) based on the τ (reference cycle) set, so set the τ (reference cycle) after due consideration.

Figure 4.9.4.1 shows the τ waveform when fcarrier /12 has been selected.
τ waveform is kept on outputting from the τ (reference cycle) generation circuit according to the set dividing ratio while the REMC register is "1".

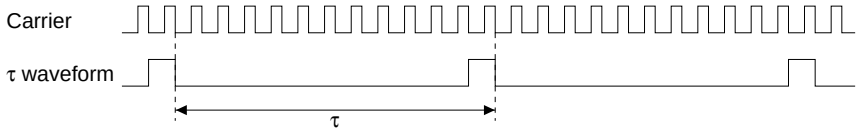


Fig. 4.9.4.1 τ waveform (when fcarrier /12 is selected)

It is possible to set τ (reference cycle) even if the OSC3 oscillation circuit is in OFF status. Furthermore, when it is set once, the set contents are maintained until an initial reset is performed.

When the REMC is set to "0", the REM circuit stops synchronously with τ. This timing is shown in Figure 4.9.4.2.

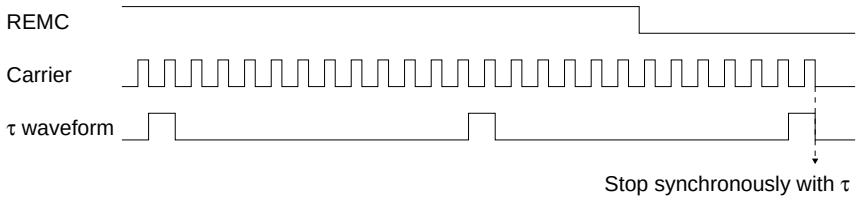


Fig. 4.9.4.2 REM circuit stop timing

Maximum of 384 machine cycles* are required until the REM circuit stops after the REMC is set to "0". Even if the CPU clock is changed from OSC3 to OSC1 after the REMC = "0", OSC3 must not be turned OFF before the REM circuit stops.

* This time depends on the value of the set τ cycle. If a shorter τ cycle is set, the maximum time required for the REM circuit to stop after REMC = "0" is shortened.

If the REM circuit is restarted from OFF state with REMC = "0", the timing of the τ waveform rises one carrier before the set division ratio.

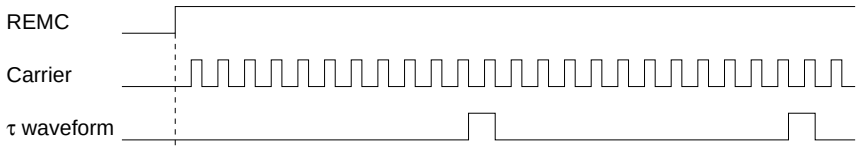


Fig. 4.9.4.3 τ generation circuit restart timing

Note: The setting of the RT register should be done when the REM circuit is OFF (REMC = "0") before starting remote transmission. Changing the contents when the REM circuit is ON may cause a malfunction.

(2) Setting of carrier output width

In the soft-timer mode, the carrier output width (carrier output ON time) is controlled by writing to the REMSO register, but in the hard-timer mode, it can be specified with values 0 to 3, which mean the number of τ cycles described above, in each transmission data bit. Since the carrier output ON/OFF is controlled by the hardware in synchronizing with τ waveform, it is unnecessary to watch the ON time and to specify the OFF timing by the software.
The carrier output width can be selected by writing data to the ROUT1–ROUT0 register (F9H•D3, D2) from among 4 types as shown in Table 4.9.4.3.

Table 4.9.4.3 Setting of carrier output width

ROUT1	ROUT0	Carrier output width
0	0	0τ
0	1	1τ
1	0	2τ
1	1	3τ

The carrier is output in synchronizing with the rising edge of the τ waveform after writing data to ROUT register. Data written to the ROUT register is maintained while the REM circuit is ON until the next data is written. The carrier output starts using the write signal for this register and the carrier output will be ON from the rising edge of the τ waveform immediately after that until the period set in the register has passed. In other words, the register data is valid only one time after writing. Consequently, data must be written every time even when outputting the same data successively.
The ROUT register is set to "0H" at initial reset and when the REMC register is set to "0". Consequently, after turning the REM circuit ON ("1" is written to the REMC register), REM output becomes low level (VSS) until a value other than "0H" is written to the ROUT register.
Figure 4.9.4.4 shows the timing of data writing to the ROUT register and the carrier output.

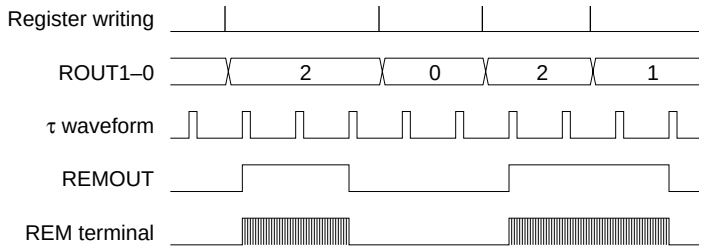


Fig. 4.9.4.4 Carrier output timing

Note: The values set in the ROUT register is taken into the REMOUT time generator synchronously with the rise of a τ waveform. For this reason, avoid writing data into the ROUT register during one carrier cycle immediately before and after the rise of the τ waveform.

(3) Remote controller (REM) interrupt

The carrier output ON time for one transmission data bit is controlled by writing data to the above mentioned ROUT register. The OFF time is from when the output is turned OFF to when the next carrier output starts by writing to the same register. Since the carrier output is turned ON at the rising edge of the τ waveform after writing data, the next data must be written during the last τ cycle in the carrier OFF period of the current transmission data. To decide its timing, an interrupt is used in the hard-timer mode.
By using the interrupt, the CPU is released from the processing such as a timing watch, and can execute other processing.

The timing to generate interrupt can be set by the software using τ cycle as reference the same as the carrier output width. The interrupt timing can be selected by writing data to the RIC3–RIC0 register (F8H).

The time until an interrupt request occurs (t_{RI}) is given by:

$t_{RI} = t_{RIC} + (1 \pm 1$ instruction cycle)

Where t_{RIC} is the time set by the RIC register. The relation between the RIC register and t_{RIC} is:

$t_{RIC} = (RIC3 \times 2^3 + RIC2 \times 2^2 + RIC1 \times 2 + RIC0) \times \tau$

As with the REMOUT time generator, the REM interrupt counter starts counting synchronously with the rising edge of the τ waveform. The interrupt control circuit generates a REM interrupt synchronously with the τ pulse when the count is completed.

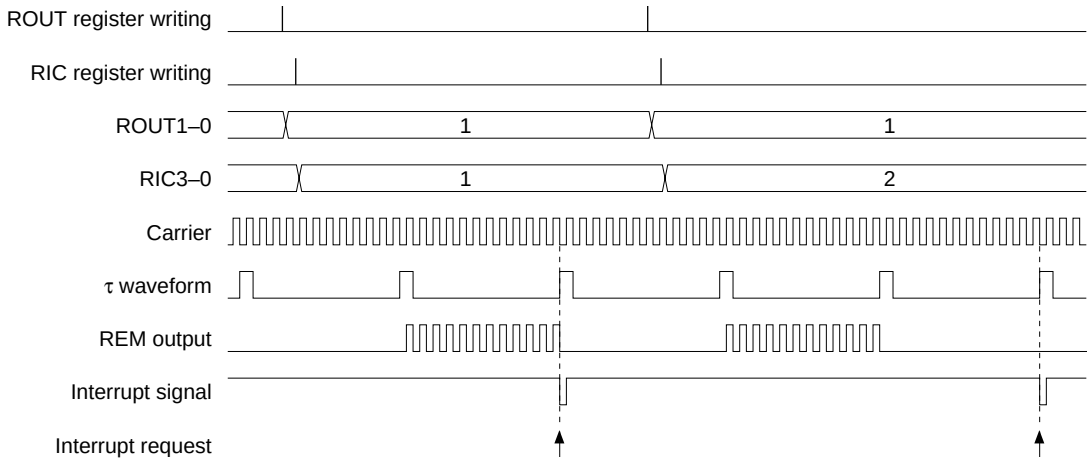


Fig. 4.9.4.5 REM interrupt timing

The τ waveform is counted at every rising edge. When the count becomes the number set in the RIC register, the interrupt factor flag IREM (F0H•D2) is set to "1" and an interrupt occurs in synchronization with that riging edge.
Set the next carrier output width and the interrupt timing using this interrupt.
The REM interrupt can be masked through the interrupt mask register EIREM (F2H•D2). However, regardless of the setting of the interrupt mask register, the interrupt factor flag IREM is set to "1" when the counting of the interrupt τ cycles are completed.
The interrupt factor flag is reset to "0" by the reading.

Data written to the RIC register is maintained while the REM circuit is ON until the next data is written. However, the counting of τ waveform starts using the write signal for the RIC register the same as the ROUT register, so this register data is valid only one time after writing. Consequently, data must be written every time even when generating the next interrupt in the same cycle count.
The RIC register is undefined at initial reset. However, the counting of τ cycles is not performed until the RIC register is written after that.

Note: • Once data has been written in the RIC register, avoid writing other data into the register before a REM interrupt occurs (which would otherwise cause an invalid interrupt).

• The values allowed for the RIC register are 0 to 0EH.

• Reading of the interrupt factor flag is available at EI, but be careful in the following cases.
If the interrupt mask register value corresponding to the interrupt factor flag to be read is set to "1", an interrupt request will be generated by the interrupt factor flag set timing, or an interrupt request will not be generated.

4.9.5 I/O memory of remote controller

Table 4.9.5.1 shows the I/O addresses and the control bits for the remote controller.

Table 4.9.5.1 Control bits of remote controller

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
0F0H	REMSO	IREM	IK1	IK0	REMSO	0	On	Off	Forced REM output (on/off)
					IREM *4	– *5	Yes	No	Interrupt factor flag (REM)
	R/W		R		IK1 *4	0	Yes	No	Interrupt factor flag (K10–K13)
					IK0 *4	0	Yes	No	Interrupt factor flag (K00–K03)
0F2H	REMC	EIREM	EIK1	EIK0	REMC	1	On	Off	REM carrier generation on/off
					EIREM	0	Enable	Mask	Interrupt mask register (REM)
	R/W				EIK1	0	Enable	Mask	Interrupt mask register (K10–K13)
					EIK0	0	Enable	Mask	Interrupt mask register (K00–K03)
0F7H	RCDIV	RCDUTY	RT1	RT0	RCDIV	– *5			REM carrier interval and duty ratio setting → D3 D2 Div. ratio Duty: 0 0 1/8 1/4; 0 1 1/8 3/8; 1 0 1/12 1/3; 1 1 1/12 1/4
					RCDUTY	– *5			
	R/W				RT1	– *5			τ cycle (division ratio) setting
					RT0	– *5			0: 1/12, 1: 1/16, 2: 1/20, 3: 1/32
0F8H	RIC3	RIC2	RIC1	RIC0	RIC3	– *5			REM interrupt counter (0τ to 14τ)
					RIC2	– *5			
	W				RIC1	– *5			
					RIC0	– *5			
0F9H	ROUT1	ROUT0	MF91	MF90	ROUT1	0			REM output duration setting (0τ to 3τ)
					ROUT0	0			
	R/W				MF91	– *5			General-purpose register
					MF90	– *5			General-purpose register

*1 Initial value at initial reset
*2 Not set in the circuit
*3 Always "0" being read
*4 Reset (0) immediately after being read
*5 Undefined

REMC: REM carrier generation control (0F2H•D3)

Turns the carrier generation on and off.

When "1" is written: On
When "0" is written: Off
Reading: Valid

When "1" is written to the REMC register, the carrier generation circuit turns ON.
Writing "0" turns the carrier generation circuit OFF.
At initial reset, this register is set to "1".

REMSO: Soft-timer output control (0F0H•D3)

Controls the carrier output in the soft-timer mode.

When "1" is written: Carrier output ON
When "0" is written: Carrier output OFF
Reading: Valid

By writing "1" to the REMSO register when the REMC registre has been set to "1", carrier is output from the REM (R33) terminal. When "0" is written, the REM (R33) terminal goes to low level (V_{SS}).
At initial reset, this register is set to "0".

Note: The REMSO register is for the exclusive use of the soft-timer mode. When controlling with the hard-timer mode, the REMSO register should be fixed at "0".

RCDIV: Carrier cycle selection (0F7H•D3)

Selects the carrier cycle.

When "1" is written: $f_{OSC3}/12$
When "0" is written: $f_{OSC3}/8$
Reading: Valid

When "1" is written to the RCDIV register, the carrier frequency is set to $f_{OSC3}/12$. When "0" is written, it is set to $f_{OSC3}/8$. This setting must be done when the remote controller is OFF (REMC = "0") status.
At initial reset, this register is undefined.

RCDUTY: Carrier duty ratio selection (0F7H•D2)

Selects the duty ratio of the carrier.
Duty ratio set by RCDUTY varies according to the carrier cycle set by RCDIV as the follows:

Table 4.9.5.2 Selection of carrier duty ratio

RCDIV	RCDUTY	Carrier dividing ratio	Carrier duty ratio
0	0	fOSC3 / 8	1/4
0	1	fOSC3 / 8	3/8
1	0	fOSC3 / 12	1/3
1	1	fOSC3 / 12	1/4

fOSC3: OSC3 oscillation frequency

This setting must be done when the remote controller is OFF (REMC = "0") status.
At initial reset, this register is undefined.

RT1, RT0: τ cycle selection (0F7H•D1, D0)

Selects the τ (reference cycle).
When controlling in the hard-timer mode, select the τ (reference cycle) that is used as a reference for the timing generation.

Table 4.9.5.3 τ (reference cycle) setting

RT1	RT0	τ dividing ratio
0	0	fcarrier / 12
0	1	fcarrier / 16
1	0	fcarrier / 20
1	1	fcarrier / 32

* fcarrier indicates carrier frequency. It is selected by RCDIV (F7H•D3).

This setting must be done when the remote controller is in OFF (REMC = "0") status.
At initial reset, this register is undefined.

ROUT1, ROUT0: Carrier output width selection (0F9H•D3, D2)

When controlling in the hard-timer mode, select the carrier output width.

Table 4.9.5.4 Setting of carrier output width

ROUT1	ROUT0	Carrier output width
0	0	0τ
0	1	1τ
1	0	2τ
1	1	3τ

By writing data to this register, the carrier for set τ cycles is output from the REM (R33) terminal in synchronization with the rising edge of the τ waveform immediately after that.
The setting (writing) of carrier output width must be done at every bit of the transmission data.
At initial reset and when the REMC register is set to "0", this register is set to "0".

Note: The ROUT register is for the exclusive use of the hard-timer mode. When controlling with the soft-timer mode, be sure not to write data to this register to prevent malfunction.

RIC3–RIC0: Interrupt τ cycle selection (0F8H)

The τ cycle count for generating a REM interrupt is set to this register.
By writing data to this register when the REM circuit has been ON (REMC = "1"), the counting of τ waveform is started by synchronizing with the rising edge of the τ waveform immediately after that. When the count becomes the number set in this register, an interrupt occurs. Set the next transmission data and interrupt timing using this interrupt.
Do not set "0FH" in this register.
The setting (writing) of interrupt τ cycle must be done at every bit of the transmission data.
At initial reset, this register is undefined.

Note: The RIC register is for the exclusive use of the hard-timer mode. When controlling with the soft-timer mode, be sure not to write data to this register to prevent malfunction.

EIREM: Interrupt mask register (0F2H•D2)

This register is used to select whether to mask the remote controller interrupt.

When "1" is written: Enabled
When "0" is written: Masked
Reading: Valid

When "1" is written to EIREM, the remote controller interrupt is enabled. When "0" is written, it is masked.
At initial reset, this register is set to "0".

IREM: Interrupt factor flag (0F0H•D2)

This is the interrupt factor flag of the remote controller.

When "1" is read: Interrupt has occurred
When "0" is read: Interrupt has not occurred
Writing: Invalid

This flag is set to "1" when the interrupt τ cycle set with the RIC register has passed (counting of the τ waveform has completed).
From the status of this flag, the software can decide the remote controller interrupt. Note, however, that even if the interrupt is masked, this flag will be set to "1" when the counting of the interrupt τ cycle is completed.
This flag is reset when read out by the software.
Reading of the interrupt factor flag is available at EI, but be careful in the following cases.
If the interrupt mask register value corresponding to the interrupt factor flag to be read is set to "1", an interrupt request will be generated by the interrupt factor flag set timing, or an interrupt request will not be generated.
At initial reset, this flag is set to "0".

4.9.6 Programming notes

(1) The following programming steps are needed to initialize the REM circuit (τ clock, REM interrupt circuit):

- Write data at addresses 0F7H and 0F8H in that order within 80 machine clocks (equivalent to eleven 7-clock instructions) after release from initial reset.
- With REMC = "0" (0F2H•D3), the REM circuit must not be stopped within cycle of 1τ after data has been written at address 0F8H.
- To initialize the REM interrupt circuit, read the REM interrupt factor flag (address 0F0H) to clear it at least an interval of 2τ after data has been written at address 0F8H.

(2) After initial reset, the REMC register stays at "1" to initialize the carrier generation circuit. The REMC register can only be reset to "0" after initialization (at least 32 machine cycles later).

(3) The REM circuit does not stop immediately after the REMC register is reset to "0". It stops synchronously with the interval τ, during which OSC3 must be held ON.

(4) With the REM circuit in operation, do not write data at addresses 0F8H and 0F9H (REM interrupt counter and REMOUT time setting register) during an interval of one carrier before and after the rise of τ.

(5) With the REM circuit in operation, do not write data at addresses 0F7H (τ-setting register).

(6) During the operation under hard-timer mode, the REMSO register must be fixed at "0".

(7) Reading of interrupt factor flag is available at EI, but be careful in the following cases.
If the interrupt mask register value corresponding to the interrupt factor flag to be read is set to "1", an interrupt request will be generated by the interrupt factor flag set timing, or an interrupt request will not be generated. Be very careful when interrupt factor flags are in the same address.

(8) If the RIC register is set again before a REM interrupt occurs with the RIC register set, an invalid interrupt may occur.

(9) The values that can be set in the REM interrupt counter (0F8H) are from 0 to 0EH. Remember, writing 0FH into the counter may cause an error.

(10) Soft-timer mode cannot coexist with hard-timer mode.
To use them in combination, stop the REM circuit before selecting either.

4.10 Interrupt and HALT

The E0C6006 has a total of six interrupt functions: two external input interrupts, three internal timer interrupts, and one remote control (REM) interrupt. Each of them can be masked. To enable an interrupt, the interrupt flag must be enabled (set to "1"). Upon occurrence of an interrupt, the flag is disabled (set to "0").

When an interrupt occurs, the address of the next program to execute is saved into the stack (RAM) and the program counter is set to the interrupt vector (page 1, steps 01H to 0FH) depending on the interrupt factor. (These processes require a time of 12 clocks.) All subsequent processing is controlled by the software written in the interrupt vector.

Execution of the HALT instruction stops the CPU clock of the E0C6006 to halt the CPU. An interrupt enables it to restart from the halt state. If the CPU can not restart, because dose not detect an interrupt, it restarts from initial reset state under watchdog timer control.

Table 4.10.1 I/O memory map

Address	Register								Comment
	D3	D2	D1	D0	Name	Init *1	1	0	
0F0H	REMSO	IREM	IK1	IK0	REMSO	0	On	Off	Forced REM output (on/off)
					IREM *4	– *5	Yes	No	Interrupt factor flag (REM)
	R/W	R			IK1 *4	0	Yes	No	Interrupt factor flag (K10–K13)
					IK0 *4	0	Yes	No	Interrupt factor flag (K00–K03)
0F1H	WDRST	IT2	IT8	IT32	WDRST	Reset	Reset	–	Watchdog timer reset
					IT2 *4	0	Yes	No	Interrupt factor flag (clock timer 2 Hz)
	W	R			IT8 *4	0	Yes	No	Interrupt factor flag (clock timer 8 Hz)
					IT32 *4	0	Yes	No	Interrupt factor flag (clock timer 32 Hz)
0F2H	REMC	EIREM	EIK1	EIK0	REMC	1	On	Off	REM carrier generation on/off
					EIREM	0	Enable	Mask	Interrupt mask register (REM)
	R/W				EIK1	0	Enable	Mask	Interrupt mask register (K10–K13)
					EIK0	0	Enable	Mask	Interrupt mask register (K00–K03)
0F3H	TMRUN	EIT2	EIT8	EIT32	TMRUN	0	Run	Reset,Stop	Timer run/reset & stop
					EIT2	0	Enable	Mask	Interrupt mask register (clock timer 2 Hz)
	R/W				EIT8	0	Enable	Mask	Interrupt mask register (clock timer 8 Hz)
					EIT32	0	Enable	Mask	Interrupt mask register (clock timer 32 Hz)

*1 Initial value at initial reset
*2 Not set in the circuit
*3 Always "0" being read
*4 Reset (0) immediately after being read
*5 Undefined

4.10.1 Interrupt request

An interrupt request is caused by one of the following factors:

Table 4.10.1.1 Interrupt factor and interrupt factor flag

Interrupt factor	Interrupt factor flag	
Falling edge of 2 Hz timer signal	TI2	(0F1H•D2)
Falling edge of 8 Hz timer signal	TI8	(0F1H•D1)
Falling edge of 32 Hz timer signal	TI32	(0F1H•D0)
REM control	IREM	(0F0H•D2)
Falling edge of input (K10–K13)	IK1	(0F0H•D1)
Falling edge of input (K00–K03)	IK0	(0F0H•D0)

An interrupt factor sets the corresponding interrupt factor flag (read-only register) to "1". When its data is read, the register is reset to "0". At initial reset, it is reset to "0". (However, the value of the REM interrupt factor flag (IREM) is undefined at initial reset.)

When the interrupt factor flag is set to "1" with both the corresponding interrupt mask register and interrupt flag set at "1", an interrupt request to the CPU is generated.

Reading of interrupt factor flags is available at EI, but be careful in the following cases.
If the interrupt mask register value corresponding to the interrupt factor flag to be read is set to "1", an interrupt request will be generated by the interrupt factor flag set timing, or an interrupt request will not be generated. Be very careful when interrupt factor flags are in the same address.

• Timer Interrupt

As described in section 4.8 "Clock Timer", the timer signal of 2 Hz, 8 Hz or 32 Hz can request a timer interrupt (when fOSC1 = 32.768 kHz). As the timer continues to operate even with the CPU in the halt state, the CPU can be restarted under timer control.

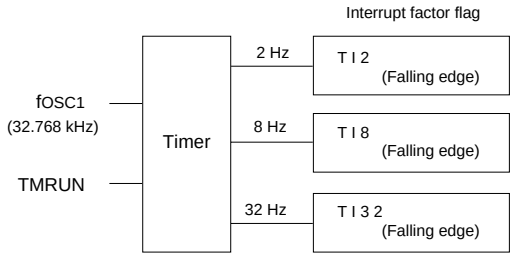


Fig. 4.10.1.1 Timer interrupt request circuit

• REM Interrupt

As described in section 4.9 "Remote Controller", a REM interrupt can be invoked during operation of the REM circuit or synchronously with a REM carrier. Note that the operation of the REM circuit is assured only with a CPU clock being supplied from OSC3.

• Input Interrupt

An input interrupt can be invoked by the IK1 group (K10–K13) or the IK0 group (K00–K03). As each pin contains an fOSC1/8 (4 kHz) clock noise reject circuit, the input must be held at low level for at least 16/fOSC1 (0.5 msec) to assure an input interrupt.

For the K10–K13 group, the interrupt factor flag can be set with the noise reject circuit bypassed by using the mask option. In this case, the input must be held at low level for at least 5 machine clocks (equivalent to 0.16 msec in the 32 kHz mode or 11 µsec in the 455 kHz mode) to get an assured input interrupt.

Since the noise reject circuit continues operating with the CPU in the halt state, the CPU can be restarted by an input interrupt. Note that, if this is impossible, initial resetting under watchdog timer control is required.

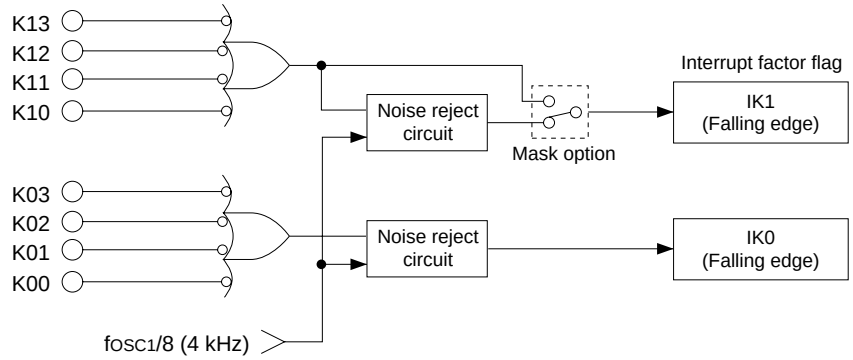
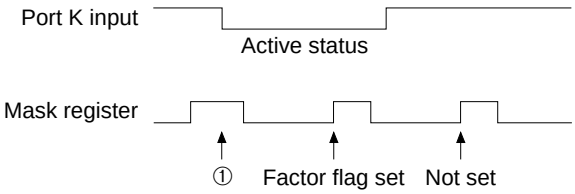


Fig. 4.10.1.2 Input interrupt circuit

<Input interrupt programming related precautions>



When the content of the mask register is rewritten, while the port K input is in the active status. The input interrupt factor flag is set at ①.

Fig. 4.10.1.3 Input interrupt timing

When using an input interrupt, if you rewrite the content of the mask register, when the value of the input terminal which becomes the interrupt input is in the active status (input terminal = low status), the factor flag for input interrupt may be set.
For example, a factor flag is set with the timing of ① shown in Figure 4.10.1.3. However, when clearing the content of the mask register with the input terminal kept in the low status and then setting it, the factor flag of the input interrupt is again set at the timing that has been set.
Consequently, when the input terminal is in the active status (low status), do not rewrite the mask register (clearing, then setting the mask register), so that a factor flag will only set at the falling edge in this case. When clearing, then setting the mask register, set the mask register, when the input terminal is not in the active status (high status).

4.10.2 Interrupt mask register

One interrupt mask register is available to each interrupt factor flag to mask an interrupt request. Data can be written to or read from the mask register. An interrupt request is enabled with "1" set in the register, and masked with "0" set in the register. At initial reset, the mask register is reset to "0".

Table 4.10.2.1 Interrupt mask register

Interrupt mask register		Interrupt factor flag	
ETI2	(0F3H•D2)	TI2	(0F1H•D2)
ETI8	(0F3H•D1)	TI8	(0F1H•D1)
ETI32	(0F3H•D0)	TI32	(0F1H•D0)
EIREM	(0F2H•D2)	IREM	(0F0H•D2)
EIK1	(0F2H•D1)	IK1	(0F0H•D1)
EIK0	(0F2H•D0)	IK0	(0F0H•D0)

4.10.3 Interrupt vector

In response to an interrupt request, the CPU starts interrupt processing. The CPU saves the PC into the stack and makes a jump to the interrupt address, that is the interrupt handling routine. The interrupt address is indirectly specified by an interrupt factor. Interrupt addresses are assigned to page 1, steps 01H to 0FH of the PC. In other words, the low-order 4 bits of the PC are indirectly addressed by interrupt factors, as follows:

Table 4.10.3.1 Interrupt vector

PC	Value	Interrupt factor
PCS3	1	Timer interrupt requested
	0	Timer interrupt not requested
PCS2	1	REM interrupt requested
	0	REM interrupt not requested
PCS1	1	K10–K13 interrupt requested
	0	K10–K13 interrupt not requested
PCS0	1	K00–K03 interrupt requested
	0	K00–K03 interrupt not requested

Examples:
- Only timer interrupt requested — Jump to page 1, step 08H
- Both timer interrupt and REM interrupt requested — Jump to page 1, step 0CH

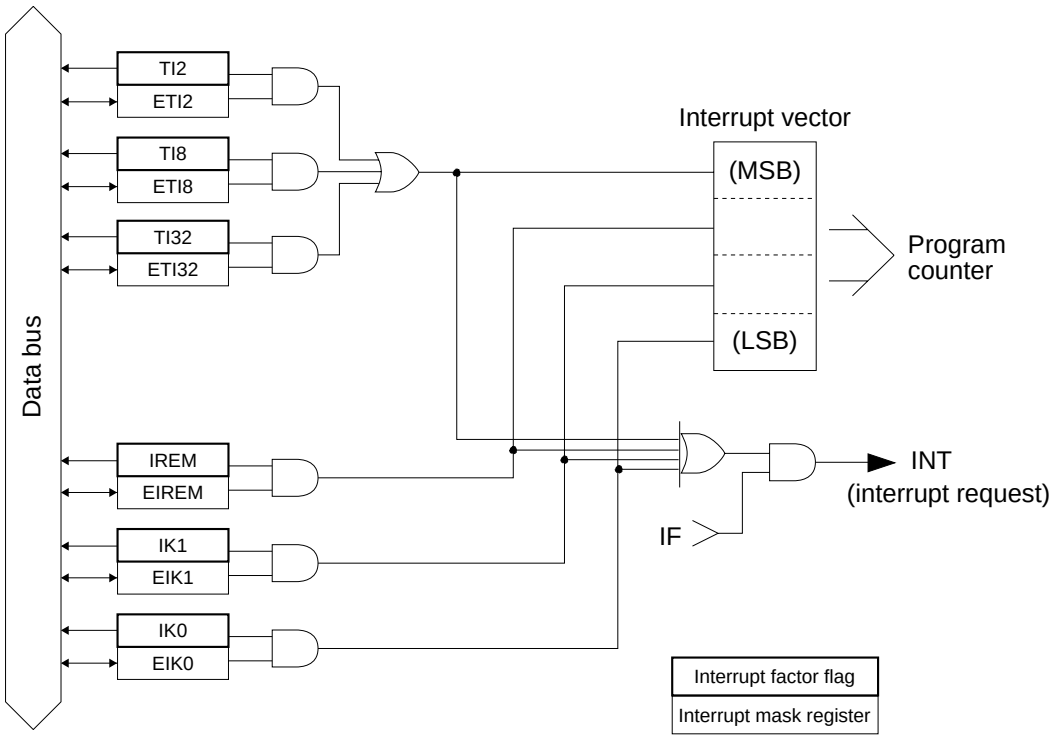


Fig. 4.10.3.1 Interrupt request/interrupt vector generation circuit

4.10.4 Programming notes

(1) Restart from the HALT mode is performed by an interrupt. The return address after completion of the interrupt processing will be the address following the HALT instruction.

(2) When an interrupt occurs, the interrupt flag will be reset by the hardware and it will become DI status. After completion of the interrupt processing, set to the EI status through the software as needed.
Moreover, the nesting level may be set to be programmable by setting to the EI state at the beginning of the interrupt processing routine.

(3) The interrupt factor flags must always be reset before setting the EI status. When the interrupt mask register has been set to "1", the same interrupt will occur again if the EI status is set unless of resetting the interrupt factor flag.

(4) The interrupt factor flag will be reset by reading through the software. Because of this, when multiple interrupt factor flags are to be assigned to the same address, perform the flag check after the contents of the address has been stored in the RAM. Direct checking with the FAN instruction will cause all the interrupt factor flag to be reset.

(5) Reading of interrupt factor flag is available at EI, but be careful in the following cases.
If the interrupt mask register value corresponding to the interrupt factor flag to be read is set to "1", an interrupt request will be generated by the interrupt factor flag set timing, or an interrupt request will not be generated. Be very careful when interrupt factor flags are in the same address.

4.11 Lower Current Dissipation

The E0C6006 contains a control register for each circuit block to realize lower current consumption. The registers are programmed so as to operate each circuit with a minimum current. For reference in programming, the following table summarizes the circuits that can be controlled for lower current consumption and the in associated registers:

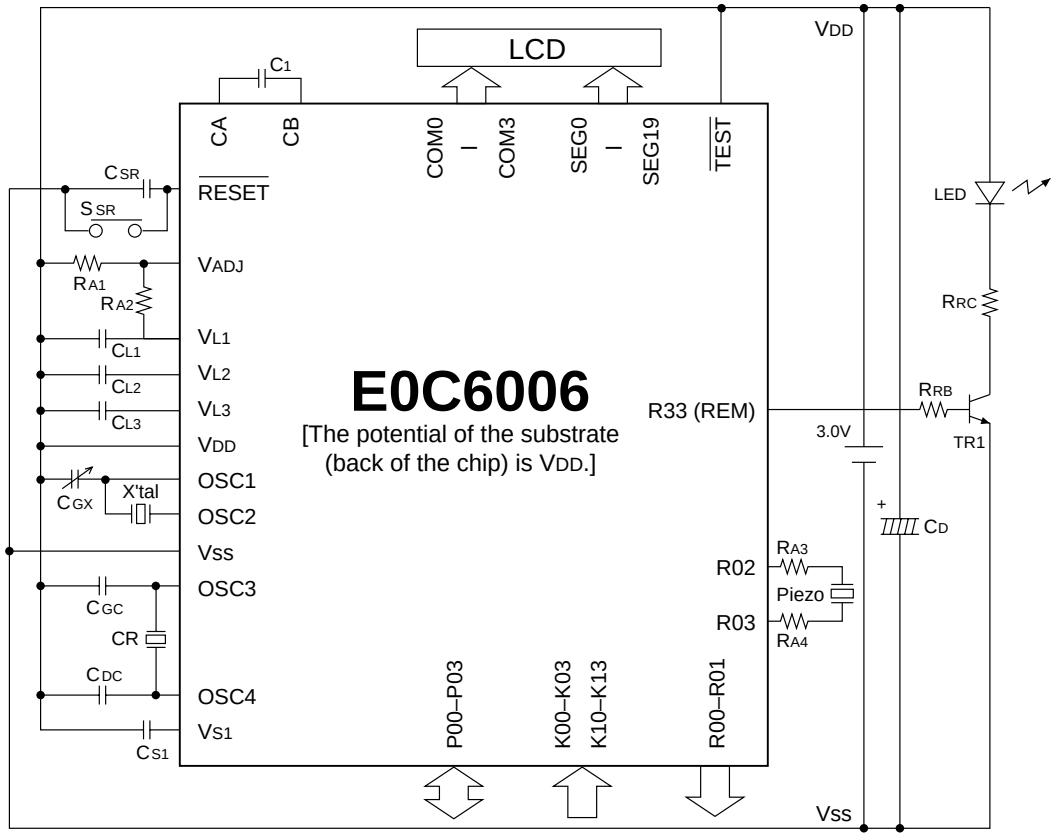
Table 4.11.1 Order of current consumption

Circuit system	Control register	Order of current consumption
CPU	HALT instruction	See Capter 6, "Electrical Characteristics"
CPU operating frequency	CLKCHG	
Ceramic (CR) oscillation circuit	OSCC	Several tens µA
REM circuit	REMC	Several µA (in OSC3 mode) Several hundreds nA ("OSC3 not used" selected)
Clock timer	TMRUN	Several hundreds nA

At initial setting with the CPU in operation mode, the CPU is ready with OSC3 clock (CLKCHG = "0", in high-speed mode), the ceramic (CR) oscillation circuit is ON (OSCC = 1), the REM circuit is ON (REMC = "1"), and the timer is OFF (TMRUN = "0").

It should be noted that various factors affecting current consumption. For example, a system in which a resistor is connected to the V_{ADJ} pin to control the LCD power (V_{L1}) differ from a system in which the V_{ADJ} pin is shorted to V_{L1}. Also, characteristics of the LCD panel used will produce a difference in power consumption to the order of several micro-amperes.

CHAPTER 5 BASIC EXTERNAL WIRING DIAGRAM



X'tal	Crystal oscillator	32.768kHz, CI(Max.)=35kΩ
CGX	Trimmer capacitor	5–25pF
CR	Ceramic oscillator	455kHz
CGC	Capacitor	100pF
CDC	Capasitor	100pF
CSR	Capacitor	0.33µF
RA1	Resistor	Open(VL=1.0V), 2MΩ (VL=1.5V)
RA2	Resistor	Short(VL=1.0V), 1MΩ (VL=1.5V)
RA3, RA4	Resistor	100Ω
C1	Capacitor	0.1µF
CS1	Capacitor	0.1µF
CL1–CL3	Capacitor	0.1µF

Note: The above table is simply an example, and is not guaranteed to work.

CHAPTER 6 ELECTRICAL CHARACTERISTICS

6.1 Absolute Maximum Rating

(V_{DD}=0V)

Item	Symbol	Rated value	Unit
Supply voltage	V_{SS}	-5.2 to 0.5	V
Input voltage (1)	V_I	V_{SS} - 0.3 to 0.3	V
Input voltage (2)	V_{IOSC}	V_{S1} - 0.3 to 0.3	V
Operating temperature	Topr	-20 to 70	°C
Storage temperature	Tstg	-65 to 150	°C
Soldering temperature / time	Tsol	260°C, 10sec (lead section)	–
Permissible dissipation *1	P_D	250	mW

*1 In case of plastic package (QFP6-60pin, QFP13-64pin).

6.2 Recommended Operating Conditions

(Ta=-20 to 70°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply voltage	V_{SS}	V_{DD}=0V	-3.5	-3.0	-2.2	V
Oscillation frequency	f_{OSC1}		–	32.768	–	kHz
	f_{OSC3}	Duty: 50±5%	50	455	600	kHz
LCD drive voltage	V_{L1}		-1.6	-1.03	–	V
CR oscillation external resistor	R_{CR}		100	140	500	kΩ

6.3 DC Characteristics

Unless otherwise specified:
V_{DD}=0V, V_{SS}=-2.2 to -3.5V, V_{L3}=-3.0V, Ta=-20 to 70°C

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
High level input voltage (1)	V_{IH1}		K00–03, K10–13, P00–03	0.2·V_{SS}		0	V
Low level input voltage (1)	V_{IL1}		K00–03, K10–13, P00–03	V_{SS}		0.8·V_{SS}	V
High level input voltage (2)	V_{IH2}		$\overline{RESET}$	0.1·V_{SS}		0	V
Low level input voltage (2)	V_{IL2}		$\overline{RESET}$	V_{SS}		0.9·V_{SS}	V
High level input current	I_{IH}	V_{IH}=V_{DD}				1	µA
Low level input current	I_{IL1}	V_{IL1}=V_{SS}	K00–03, K10–13, No pull-up	-1			µA
	I_{IL2}	V_{IL2}=V_{SS}	K00–03, K10–13, Pull-up	-5		-0.35	µA
	I_{IL3}	V_{IL3}=V_{SS}	$\overline{RESET}$	-5		-0.35	µA
	I_{IL4}	V_{IL4}=0.2·V_{SS}	K00–03, K10–13, Pull-up	-50			µA
	I_{IL5}	V_{IL5}=0.2·V_{SS}	$\overline{RESET}$	-50			µA
	I_{IL6}	V_{IL6}=V_{SS}	P00–03 *1	-13		-2	µA
High level output current (1)	I_{OH1}	V_{OH1}=0.1·V_{SS}	R00–03			-250	µA
Low level output current (1)	I_{OL1}	V_{OL1}=0.9·V_{SS}	R00–03	1.0			mA
High level output current (2)	I_{OH2}	V_{OH2}=0.1·V_{SS}	P00–03			-250	µA
Low level output current (2)	I_{OL2}	V_{OL2}=0.9·V_{SS}	P00–03	1.0			mA
High level output current (3)	I_{OH3}	V_{OH3}=0.1·V_{SS}	R33(REM)			-1.8	mA
Low level output current (3)	I_{OL3}	V_{OL3}=0.9·V_{SS}	R33(REM)	1.0			mA
Common output current	I_{OH4}	V_{OH4}=-0.05V	COM0–3			-3.0	µA
	I_{OL4}	V_{OL4}=V_{L3}+0.05V		3.0			µA
Segment output current	I_{OH5}	V_{OH5}=-0.05V	SEG0–19			-3.0	µA
(during LCD output)	I_{OL5}	V_{OL5}=V_{L3}+0.05V		3.0			µA

*1 Only at read cycle using internal program.

6.4 Analog Circuit Characteristics and Power Current Consumption

Unless otherwise specified:
V_{DD}=0V, V_{SS}=-2.2 to -3.5V, Ta=25°C

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
LCD drive voltage	V_{L1}	V_{ADJ}=V_{L1}, I_{L1}=5µA		-1.11	-1.03	-0.95	V
	V_{L2}	1 MΩ load connected between V_{DD} and V_{L2} (no panel load)		2·V_{L1}		2·V_{L1} +0.1	V
	V_{L3}	1 MΩ load connected between V_{DD} and V_{L3} (no panel load)		3·V_{L1}		3·V_{L1} +0.3	V
Current consumption	I_{OP}	HALT mode, OSCC=0	V_{ADJ}=V_{L1} no panel load		2	5	µA
		OSC1 mode, OSCC=0			9	18	µA
		OSC3 mode *1			130	250	µA

*1 Ceramic oscillation (455 kHz) or CR oscillation (R_{CR}=140 kΩ)

6.5 Oscillation Characteristics

Oscillation characteristics will vary according to different conditions (elements used, board pattern). Use the following characteristics are as reference values.

OSC1 (Crystal Oscillation)

Unless otherwise specified:
V_{DD}=0V, V_{SS}=-3.0V, Crystal oscillator: C-002R (C_I=35kΩ), C_G=25pF, C_D=built-in, Ta=25°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start time	tsta	V_{SS}=-2.2 to -3.5V	–	–	3	sec
Built-in capacitance (drain)	C_D	Package as assembled	–	20	–	pF
		Bare chip	–	19	–	pF
Frequency/voltage deviation	∂f/∂V	V_{SS}=-2.2 to -3.5V	–	–	5	ppm
Frequency/IC deviation	∂f/∂IC		-10	–	10	ppm
Frequency adjustment range	∂f/∂C_G	C_G=5 to 25pF	40	–	–	ppm
Harmonic oscillation start voltage	V_{hho}	C_G=5pF (V_{SS})	–	–	-3.5	V
Permitted leak resistance	R_{leak}	Between OSC1 and other pins	200	–	–	MΩ

OSC3 (Ceramic Oscillation)

Unless otherwise specified:
V_{DD}=0V, V_{SS}=-3.0V, Ceramic oscillator: CSB455E*1, C_{GC}=C_{DC}=100pF, Ta=25°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start voltage	Vsta	(V_{DD})	-2.2		–	V
Oscillation start time	tsta	V_{SS}=-2.2 to -3.5V	–	3	–	mS
Oscillation stop voltage	Vstp	(V_{DD})	-2.2		–	V

*1 CSB455E: made by Murata Mfg.Co.

OSC3 (CR Oscillation)

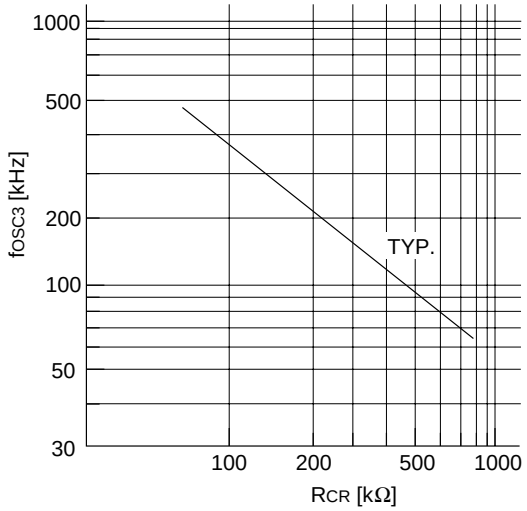
Unless otherwise specified:
V_{DD}=0V, V_{SS}=-3.0V, R_{CR}=140kΩ, Ta=25°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation frequency	f_{OSC3}		–	280	–	kHz
Oscillation start voltage	Vsta	(V_{DD})	-2.2	–	–	V
Oscillation start time	tsta	V_{SS}=-2.2 to -3.5V	–	3	–	mS
Oscillation stop voltage	Vstp	(V_{DD})	-2.2	–	–	V

E0C6006 oscillation characteristics — f_{OSC3} vs R_{CR} — (for reference)

Condition: Ta = 25°C, V_{DD} = GND, V_{SS} = -3.0 V,
Non board and package capacitance

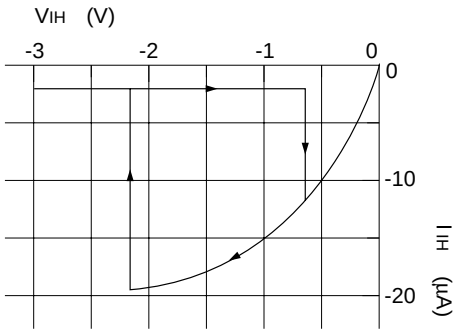
Note: Oscillation characteristics are affected by various conditions (board pattern, parts used, etc.).



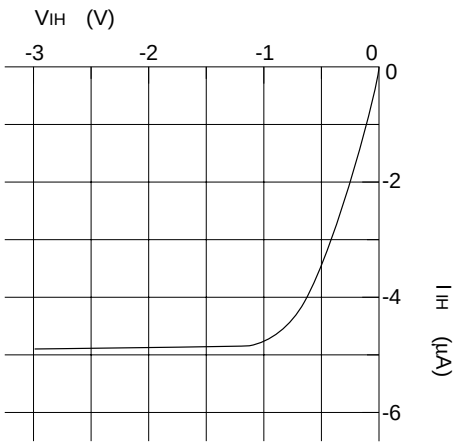
6.6 Input Current Characteristics *(For Reference)*

Condition: Ta = 25°C, V_{DD} = 0 V, V_{SS} = -3.0 V

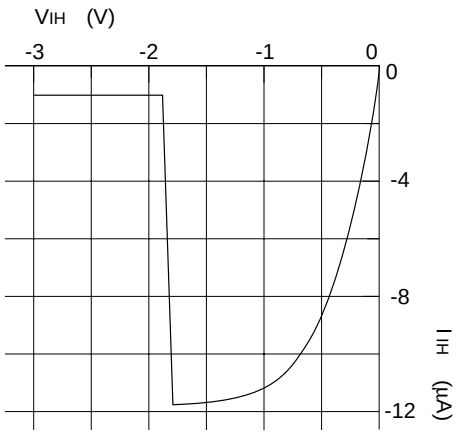
$\overline{\text{RESET}}$



P**



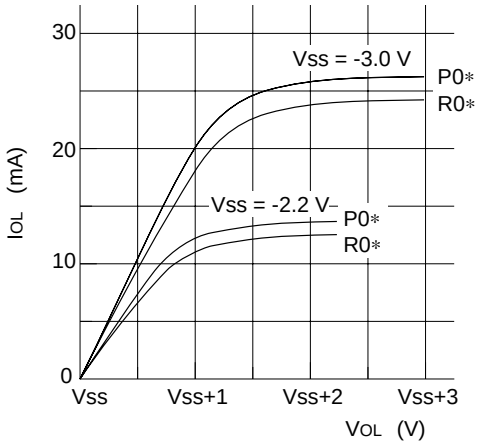
K**



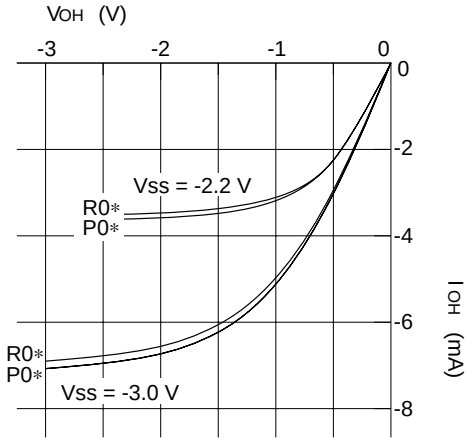
6.7 Output Current Characteristics *(For Reference)*

Condition: Ta = 25°C, V_{DD} = 0 V

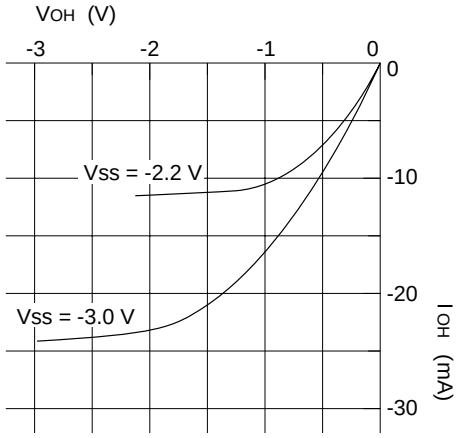
R0∗, P∗∗



R0∗, P∗∗



R33 (REM)

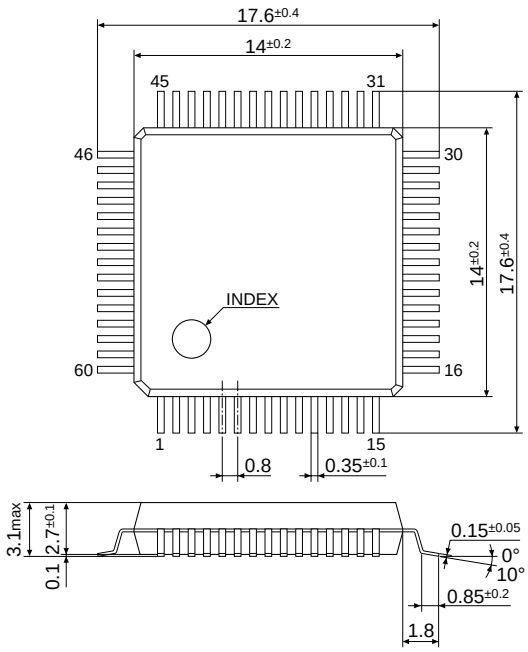


CHAPTER 7 PACKAGE

7.1 Plastic Package

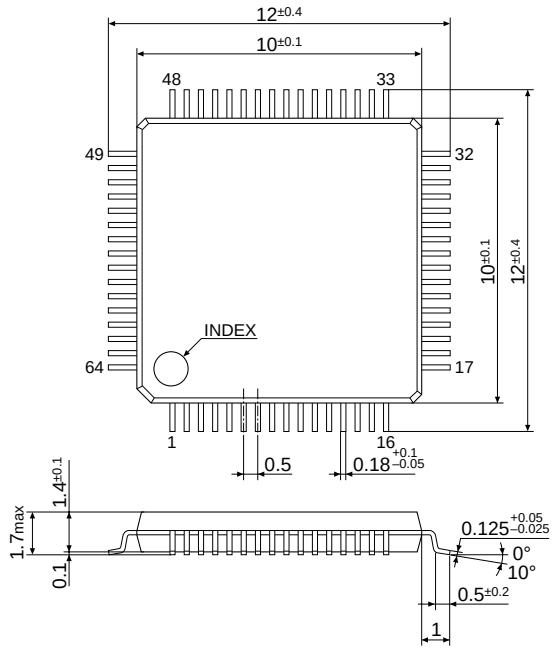
QFP6-60pin

(Unit: mm)



QFP13-64pin

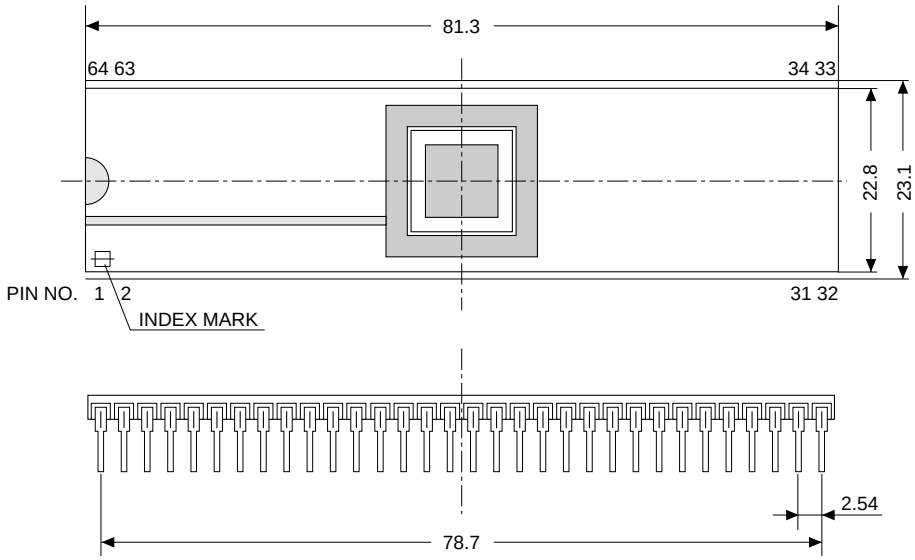
(Unit: mm)



The dimensions are subjected to change without notice.

7.2 Ceramic Package for Test Samples

(Unit: mm)

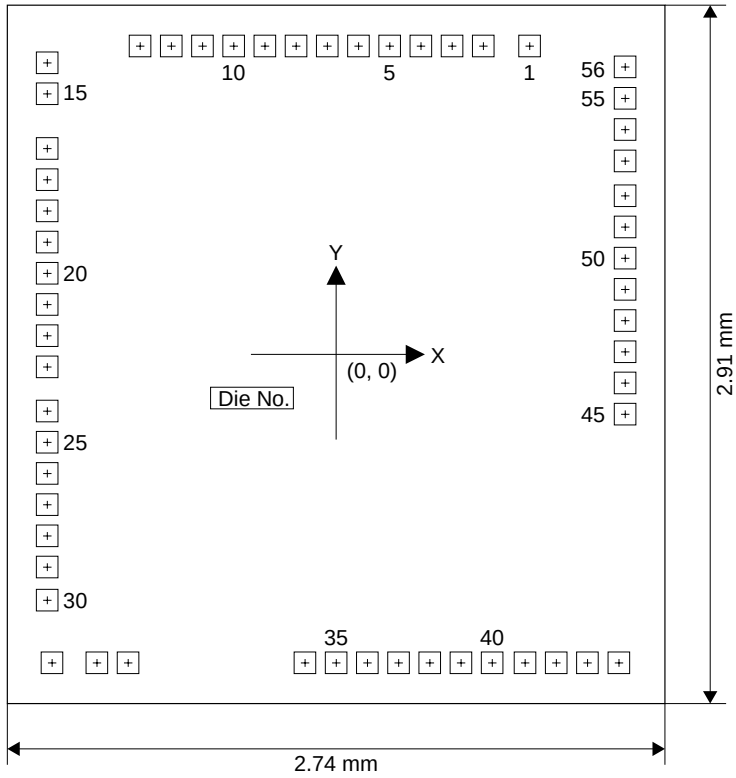


No.	Pin name	No.	Pin name	No.	Pin name	No.	Pin name
1	SEG19	17	OSC2	33	K12	49	SEG6
2	COM3	18	OSC1	34	K13	50	SEG7
3	COM2	19	V_{DD}	35	R00	51	SEG8
4	COM1	20	P03	36	R01	52	SEG9
5	COM0	21	P02	37	R02	53	SEG10
6	V_{L1}	22	P01	38	R03	54	SEG11
7	V_{L2}	23	P00	39	N.C.	55	N.C.
8	V_{L3}	24	N.C.	40	N.C.	56	TEST
9	N.C.	25	N.C.	41	N.C.	57	RESET
10	VADJ	26	N.C.	42	R33(REM)	58	SEG12
11	CA	27	K00	43	SEG0	59	SEG13
12	CB	28	K01	44	SEG1	60	SEG14
13	V_{SS}	29	K02	45	SEG2	61	SEG15
14	OSC4	30	K03	46	SEG3	62	SEG16
15	OSC3	31	K10	47	SEG4	63	SEG17
16	V_{S1}	32	K11	48	SEG5	64	SEG18

N.C. = No Connection

CHAPTER 8 PAD LAYOUT

8.1 Diagram of Pad Layout



8.2 Pad Coordinates

Unit: µm

No.	Pad name	X	Y	No.	Pad name	X	Y	No.	Pad name	X	Y
1	R33(REM)	806	1285	20	SEG16	-1204	338	39	OSC1	520	-1285
2	SEG0	613	1285	21	SEG17	-1204	208	40	V_{DD}	650	-1285
3	SEG1	483	1285	22	SEG18	-1204	78	41	P03	787	-1285
4	SEG2	353	1285	23	SEG19	-1204	-52	42	P02	917	-1285
5	SEG3	223	1285	24	COM3	-1204	-236	43	P01	1047	-1285
6	SEG4	93	1285	25	COM2	-1204	-366	44	P00	1178	-1285
7	SEG5	-37	1285	26	COM1	-1204	-496	45	K00	1204	-249
8	SEG6	-167	1285	27	COM0	-1204	-626	46	K01	1204	-119
9	SEG7	-297	1285	28	V_{L1}	-1204	-756	47	K02	1204	11
10	SEG8	-427	1285	29	V_{L2}	-1204	-886	48	K03	1204	141
11	SEG9	-557	1285	30	V_{L3}	-1204	-1024	49	K10	1204	271
12	SEG10	-687	1285	31	V_{ADJ}	-1184	-1285	50	K11	1204	401
13	SEG11	-817	1285	32	CA	-997	-1285	51	K12	1204	531
14	$\overline{\text{TEST}}$	-1204	1215	33	CB	-867	-1285	52	K13	1204	661
15	$\overline{\text{RESET}}$	-1204	1086	34	V_{SS}	-130	-1285	53	R00	1204	806
16	SEG12	-1204	858	35	OSC4	0	-1285	54	R01	1204	937
17	SEG13	-1204	728	36	OSC3	130	-1285	55	R02	1204	1067
18	SEG14	-1204	598	37	V_{S1}	260	-1285	56	R03	1204	1198
19	SEG15	-1204	468	38	OSC2	390	-1285	–			

CHAPTER 9 PRECAUTIONS ON MOUNTING

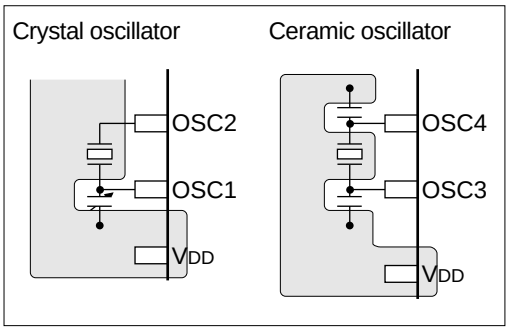
<Oscillation Circuit>

- Oscillation characteristics change depending on conditions (board pattern, components used, etc.). In particular, when a ceramic oscillator or crystal oscillator is used, use the oscillator manufacturer's recommended values for constants such as capacitance and resistance.
- Disturbances of the oscillation clock due to noise may cause a malfunction. Consider the following points to prevent this:

  (1) Components which are connected to the OSC1, OSC2, OSC3 and OSC4 terminals, such as oscillators, resistors and capacitors, should be connected in the shortest line.

  (2) As shown in the right hand figure, make a VDD pattern as large as possible at circumscription of the OSC1/OSC3 and OSC2/OSC4 terminals and the components connected to these terminals. Furthermore, do not use this VDD pattern for any purpose other than the oscillation system.

Examples of pattern and oscillator layout



- In order to prevent unstable operation of the oscillation circuit due to current leak between OSC1/OSC3 and VSS, please keep enough distance between OSC1/OSC3 and VSS or other signals on the board pattern.

<Reset Circuit>

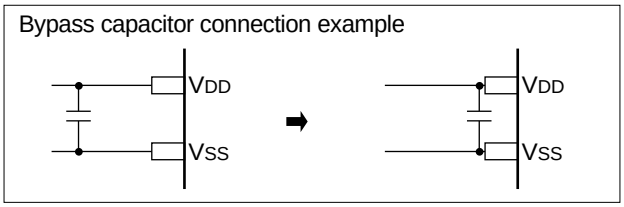
- The power-on reset signal which is input to the $\overline{\text{RESET}}$ terminal changes depending on conditions (power rise time, components used, board pattern, etc.).
  Decide the time constant of the capacitor and resistor after enough tests have been completed with the application product.
  When the built-in pull-up resistor of the $\overline{\text{RESET}}$ terminal, take into consideration dispersion of the resistance for setting the constant.
- In order to prevent any occurrences of unnecessary resetting caused by noise during operating, components such as capacitors and resistors should be connected to the $\overline{\text{RESET}}$ terminal in the shortest line.

<Power Supply Circuit>

- Sudden power supply variation due to noise may cause malfunction. Consider the following points to prevent this:

  (1) The power supply should be connected to the VDD and VSS terminal with patterns as short and large as possible.

  (2) When connecting between the VDD and VSS terminals with a bypass capacitor, the terminals should be connected as short as possible.

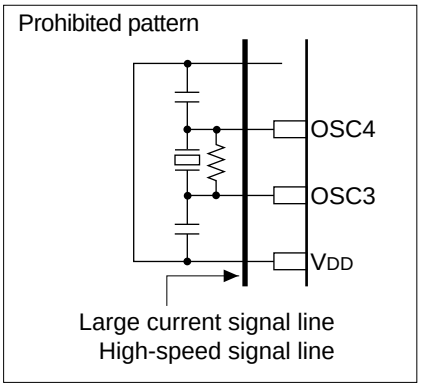


(3) Components which are connected to the V_{S1}, V_{L1}, V_{L2} and V_{L3} terminals, such as capacitors and resistors, should be connected in the shortest line.
In particular, the V_{L1}, V_{L2} and V_{L3} voltages affect the display quality.

- Do not connect anything to the V_{L1}, V_{L2} and V_{L3} terminals when the LCD driver is not used.

<Arrangement of Signal Lines>

- In order to prevent generation of electromagnetic induction noise caused by mutual inductance, do not arrange a large current signal line near the circuits that are sensitive to noise such as the oscillation unit.
- When a signal line is parallel with a high-speed line in long distance or intersects a high-speed line, noise may generated by mutual interference between the signals and it may cause a malfunction. Do not arrange a high-speed signal line especially near circuits that are sensitive to noise such as the oscillation unit.



<Precautions for Visible Radiation (when bare chip is mounted)>

- Visible radiation causes semiconductor devices to change the electrical characteristics. It may cause this IC to malfunction. When developing products which use this IC, consider the following precautions to prevent malfunctions caused by visible radiations.

(1) Design the product and implement the IC on the board so that it is shielded from visible radiation in actual use.

(2) The inspection process of the product needs an environment that shields the IC from visible radiation.

(3) As well as the face of the IC, shield the back and side too.

EPSON International Sales Operations

AMERICA

S-MOS SYSTEMS, INC.
150 River Oaks Parkway
San Jose, CA 95134, U.S.A.
Phone: +1-408-922-0200 Fax: +1-408-922-0238
Telex: 176079 SMOS SNJUD

S-MOS SYSTEMS, INC.
EASTERN AREA SALES AND TECHNOLOGY CENTER
301 Edgewater Place, Suite 120
Wakefield, MA 01880, U.S.A.
Phone: +1-617-246-3600 Fax: +1-617-246-5443

S-MOS SYSTEMS, INC.
SOUTH EASTERN AREA SALES AND TECHNOLOGY CENTER
4300 Six Forks Road, Suite 430
Raleigh, NC 27609, U.S.A.
Phone: +1-919-781-7667 Fax: +1-919-781-6778

S-MOS SYSTEMS, INC.
CENTRAL AREA SALES AND TECHNOLOGY CENTER
1450 E.American Lane, Suite 1550
Schaumburg, IL 60173, U.S.A.
Phone: +1-847-517-7667 Fax: +1-847-517-7601

EUROPE

- HEADQUARTERS -

EPSON EUROPE ELECTRONICS GmbH
Riesstrasse 15
80992 Muenchen, GERMANY
Phone: +49-(0)89-14005-0 Fax: +49-(0)89-14005-110

- GERMANY -

EPSON EUROPE ELECTRONICS GmbH
SALES OFFICE
Breidenbachstrasse 46
D-51373 Leverkusen, GERMANY
Phone: +49-(0)214-83070-0 Fax: +49-(0)214-83070-10

- UNITED KINGDOM -

EPSON EUROPE ELECTRONICS GmbH
UK BRANCH OFFICE
G6 Doncastle House, Doncastle Road
Bracknell, Berkshire RG12 8PE, ENGLAND
Phone: +44-(0)1344-381700 Fax: +44-(0)1344-381701

- FRANCE -

EPSON EUROPE ELECTRONICS GmbH
FRENCH BRANCH OFFICE
1 Avenue de l' Atlantique, LP 915 Les Conquerants
Z.A. de Courtaboeuf 2, F-91976 Les Ulis Cedex, FRANCE
Phone: +33-(0)1-64862350 Fax: +33-(0)1-64862355

ASIA

- HONG KONG, CHINA -

EPSON HONG KONG LTD.
20/F., Harbour Centre, 25 Harbour Road
Wanchai, HONG KONG
Phone: +852-2585-4600 Fax: +852-2827-4346
Telex: 65542 EPSCO HX

- CHINA -

SHANGHAI EPSON ELECTRONICS CO., LTD.
4F, Bldg., 27, No. 69, Gui Jing Road
Caohejing, Shanghai, CHINA
Phone: 21-6485-5552 Fax: 21-6485-0775

- TAIWAN, R.O.C. -

EPSON TAIWAN TECHNOLOGY & TRADING LTD.
10F, No. 287, Nanking East Road, Sec. 3
Taipei, TAIWAN, R.O.C.
Phone: 02-2717-7360 Fax: 02-2712-9164
Telex: 24444 EPSONTB

EPSON TAIWAN TECHNOLOGY & TRADING LTD.
HSINCHU OFFICE
13F-3, No. 295, Kuang-Fu Road, Sec. 2
HsinChu 300, TAIWAN, R.O.C.
Phone: 03-573-9900 Fax: 03-573-9169

- SINGAPORE -

EPSON SINGAPORE PTE., LTD.
No. 1 Temasek Avenue, #36-00
Millenia Tower, SINGAPORE 039192
Phone: +65-337-7911 Fax: +65-334-2716

- KOREA -

SEIKO EPSON CORPORATION
KOREA OFFICE
10F, KLI 63 Bldg., 60 Yoido-Dong
Youngdeungpo-Ku, Seoul, 150-010, KOREA
Phone: 02-784-6027 Fax: 02-767-3677

- JAPAN -

SEIKO EPSON CORPORATION
ELECTRONIC DEVICES MARKETING DIVISION

Electronic Device Marketing Department
IC Marketing & Engineering Group
421-8, Hino, Hino-shi, Tokyo 191-8501, JAPAN
Phone: +81-(0)42-587-5816 Fax: +81-(0)42-587-5624

ED International Marketing Department I
(Europe & U.S.A.)
421-8, Hino, Hino-shi, Tokyo 191-8501, JAPAN
Phone: +81-(0)42-587-5812 Fax: +81-(0)42-587-5564

ED International Marketing Department II (Asia)
421-8, Hino, Hino-shi, Tokyo 191-8501, JAPAN
Phone: +81-(0)42-587-5814 Fax: +81-(0)42-587-5110

In pursuit of **“Saving” Technology**, Epson electronic devices.
Our lineup of semiconductors, liquid crystal displays and quartz devices
assists in creating the products of our customers’ dreams.
Epson IS energy savings.

EPSON

SEIKO EPSON CORPORATION
ELECTRONIC DEVICES MARKETING DIVISION

■ Electronic devices information on the Epson WWW server

http://www.epson.co.jp

Issue SEPTEMBER 1998, Printed in Japan Ⓜ A