MF977-01a

EPSON

CMOS 4-BIT SINGLE CHIP MICROCOMPUTER

E0C623B TECHNICAL MANUAL

E0C623B Technical Hardware

ENERGY SAVING EPSON

SEIKO EPSON CORPORATION

CONTENTS

CHAPTER 1 INTRODUCTION

Each member of the E0C623B Series of single chip microcomputer features a 4-bit E0C6200B core CPU, 1,536 words of ROM (12 bits per word), 96 words of RAM (4 bits per word), an LCD driver, 4-bit input port (K00–K03), 4-bit output port (R00–R03), 4-bit I/O port (P00–P03), two timers (clock timer and stopwatch timer) and serial interface. Because of their low voltage operation and low power consumption, the E0C623B Series are ideal for a wide range of applications.

1.1 Configuration

The E0C623B Series is configured as follows, depending on the supply voltage and the oscillation circuit.

Table 1.1.1 Configuration of the E0C623B Series

Model	Supply voltage	Oscillation circuit	SLEEP
E0C623B	0.8–3.6 V	Crystal (32.768 kHz, Typ.) or CR (65 kHz, Typ.)	Available only for CR oscillation
E0C62A3B	1.7–3.6 V	CR (250 kHz–500 kHz) or Ceramic (400 kHz–1 MHz)	Available

1.2 Features

Oscillation circuit ..... E0C623B: Crystal oscillation circuit 32.768 kHz (Typ.)
or CR oscillation circuit 65 kHz (Typ.)
E0C62A3B: CR oscillation circuit 250 kHz to 500 kHz
or Ceramic oscillation circuit 400 kHz to 1 MHz

Instruction set ..... 100 instructions (Crystal oscillation)
101 instructions
(The SLP instruction is available with mask option except for crystal oscillation.)

Instruction execution time . With 32 kHz clock: 153 µsec, 214 µsec, 366 µsec (E0C623B)
With 65 kHz clock: 77 µsec, 108 µsec, 185 µsec (E0C623B)
With 500 kHz clock: 10 µsec, 14 µsec, 24 µsec (E0C62A3B)
With 1 MHz clock: 5 µsec, 7 µsec, 12 µsec (E0C62A3B)

ROM capacity ..... 1,536 words × 12 bits

RAM capacity ..... 96 words × 4 bits

Input port ..... 4 bits (Pull-up resistors are available with mask option)

Output port ..... 4 bits (Piezo buzzer and programmable frequency output can be driven directly by mask option)

I/O port ..... 4 bits (Serial interface data input and data output are available with mask option)

LCD driver ..... 26 segments × 4, 3 or 2 common duty (QFP5-60pin or chip)
20 segments × 4, 3 or 2 common duty (QFP12-48pin)

Serial interface ..... Clock synchronous system (Terminal pecificasion can be selected by mask option)

Time base counter ..... 2 systems (Clock timer/stopwatch timer)

Interrupts ..... External interrupt: Input port interrupt 1 system
I/O port interrupt 1 system
(Available when "input-only" is selected by mask option.)
Internal interrupt: Clock timer interrupt 1 system
Stopwatch timer interrupt 1 system
Serial interface interrupt 1 system

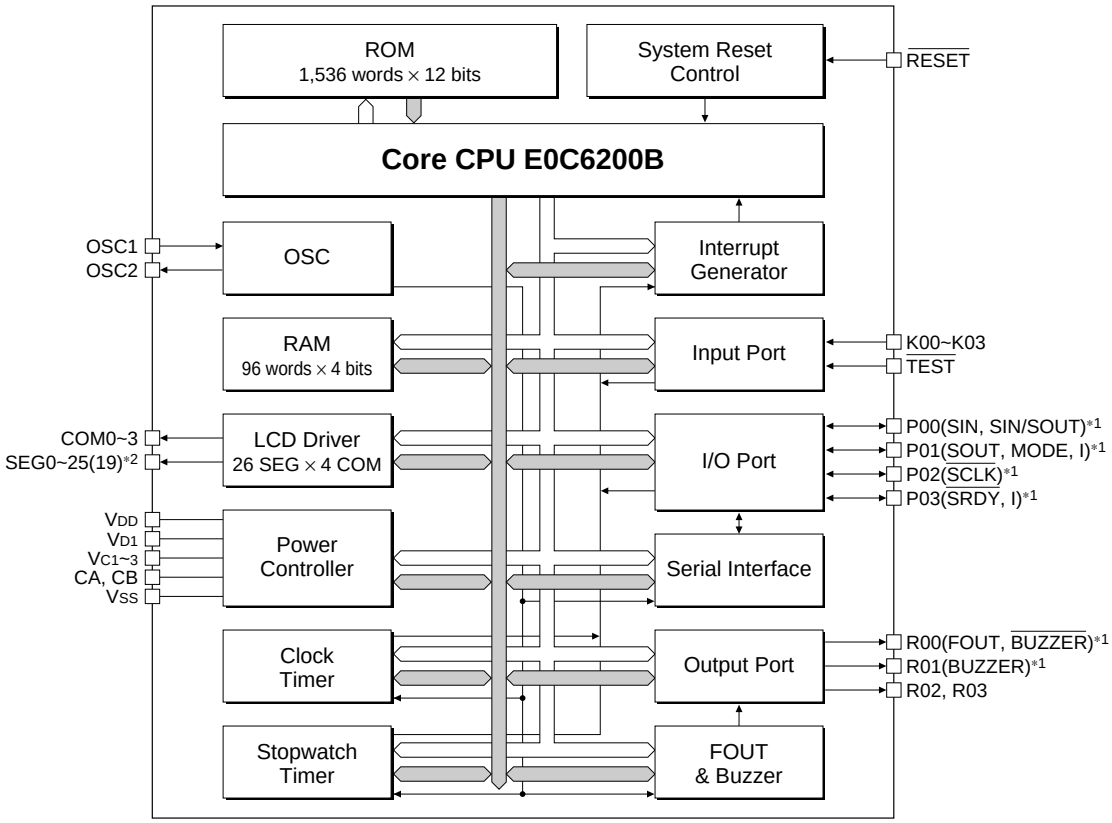
Supply voltage ..... E0C623B: 0.8 to 3.6 V, Oscillation start voltage: 0.8 V
E0C62A3B: 1.7 to 3.6 V

Operating temperature ..... -20°C to +70°C

Current consumption (Typ.) .. 2.5 µA (E0C623B, 32.768 kHz, HALT mode)
3.0 µA (E0C623B, 32.768 kHz, RUN)
1.0 µA (E0C62A3B, SLEEP mode)
80 µA (E0C62A3B, 1 MHz, HALT mode)
100 µA (E0C62A3B, 1 MHz, RUN)

Supply form ..... QFP12-48pin, QFP5-60pin (plastic) or chip

1.3 Block Diagram

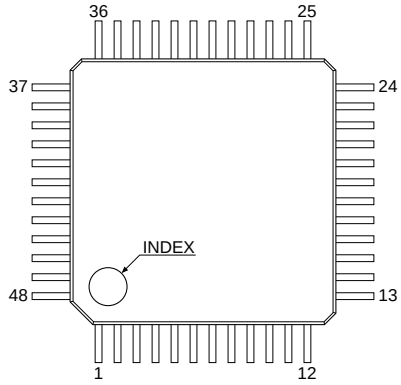


*1: Terminal specifications can be selected by mask option.
*2: SEG0 to 4, 6 and 8 to 19 are only available in the QFP12-48pin package.

Fig. 1.3.1 Block diagram

1.4 Pin Layout Diagram

QFP12-48pin

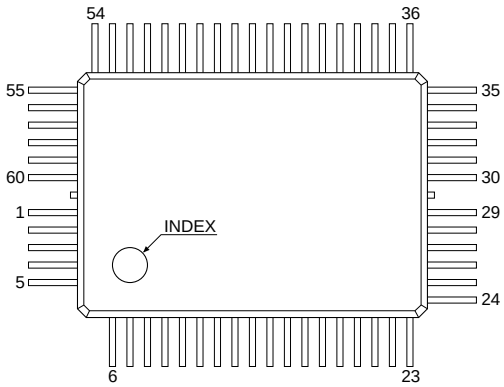


No.	Pin name	No.	Pin name	No.	Pin name	No.	Pin name
1	COM2	13	SEG12	25	P00	37	V_{DD}
2	COM3	14	SEG13	26	N.C.	38	OSC1
3	SEG0	15	SEG14	27	$\overline{\text{RESET}}$	39	OSC2
4	SEG1	16	SEG15	28	K00	40	V_{D1}
5	SEG2	17	SEG16	29	K01	41	CA
6	SEG3	18	SEG17	30	K02	42	CB
7	SEG4	19	SEG18	31	K03	43	N.C.
8	SEG6	20	SEG19	32	R00	44	V_{C1}
9	SEG8	21	$\overline{\text{TEST}}$	33	R01	45	V_{C2}
10	SEG9	22	P03	34	R02	46	V_{C3}
11	SEG10	23	P02	35	R03	47	COM0
12	SEG11	24	P01	36	V_{SS}	48	COM1

N.C. : No Connection

Fig. 1.4.1 Pin assignment (QFP12-48pin)

QFP5-60pin



No.	Pin name	No.	Pin name	No.	Pin name	No.	Pin name
1	V_{C2}	16	SEG9	31	SEG24	46	K02
2	V_{C3}	17	SEG10	32	SEG25	47	K03
3	COM0	18	SEG11	33	$\overline{\text{TEST}}$	48	R00
4	COM1	19	SEG12	34	P03	49	R01
5	COM2	20	SEG13	35	P02	50	R02
6	COM3	21	SEG14	36	P01	51	R03
7	SEG0	22	SEG15	37	P00	52	N.C.
8	SEG1	23	SEG16	38	N.C.	53	V_{SS}
9	SEG2	24	SEG17	39	N.C.	54	V_{DD}
10	SEG3	25	SEG18	40	N.C.	55	OSC1
11	SEG4	26	SEG19	41	N.C.	56	OSC2
12	SEG5	27	SEG20	42	N.C.	57	V_{D1}
13	SEG6	28	SEG21	43	$\overline{\text{RESET}}$	58	CA
14	SEG7	29	SEG22	44	K00	59	CB
15	SEG8	30	SEG23	45	K01	60	V_{C1}

N.C. : No Connection

Fig. 1.4.2 Pin assignment (QFP5-60pin)

1.5 Pin Description

Table 1.5.1 Pin description

Pin name	Pin No.		I/O	Function
	QFP12-48	QFP5-60		
V_{DD}	37	54	(I)	Power supply pin (+)
V_{SS}	36	53	(I)	Power supply pin (-)
V_{D1}	40	57	–	Oscillation and internal logic system regulated voltage output pin
V_{C1}	44	60	–	LCD system regulated voltage output pin (approx. 1.05 V)
V_{C2}	45	1	–	LCD system booster voltage output pin (V_{C1}×2)
V_{C3}	46	2	–	LCD system booster voltage output pin (V_{C1}×3)
CA, CB	41, 42	58, 59	–	Boost capacitor connecting pin
OSC1	38	55	I	Oscillation input pin (crystal, CR or ceramic *)
OSC2	39	56	O	Oscillation output pin (crystal, CR or ceramic *)
K00–K03	28–31	44–47	I	Input port pin
P00	25	37	I/O	I/O port pin or serial I/F data input/output pin *
P01	24	36	I/O	I/O port pin, serial I/F data output pin or input-only pin *
P02	23	35	I/O	I/O port pin or serial I/F clock output pin *
P03	22	34	I/O	I/O port pin, serial I/F ready signal output pin or input-only pin *
R00	32	48	O	Output port pin, buzzer or FOUT output pin *
R01	33	49	O	Output port pin or buzzer output pin *
R02, R03	34, 35	50, 51	O	Output port pin
SEG0–4	3–7	7–11	O	LCD segment output pin or DC output pin *
SEG5	–	12	O	LCD segment output pin or DC output pin * (QFP5-60pin only)
SEG6	8	13	O	LCD segment output pin or DC output pin *
SEG7	–	14	O	LCD segment output pin or DC output pin * (QFP5-60pin only)
SEG8–19	9~20	15–26	O	LCD segment output pin or DC output pin *
SEG20–25	–	27–32	O	LCD segment output pin or DC output pin * (QFP5-60pin only)
COM0–3	47, 48, 1, 2	3–6	O	LCD common output pin
$\overline{\text{RESET}}$	27	43	I	Initial reset input pin
$\overline{\text{TEST}}$	21	33	I	Input pin for test

* Selected by mask option

CHAPTER 2 POWER SUPPLY AND INITIAL RESET

2.1 Power Supply

With a single external power supply (*) supplied to VDD through VSS, the E0C623B Series generates the necessary internal voltages with the regulated voltage circuit (<VD1> for oscillator and internal circuit, <VC1> for LCD) and the voltage booster circuit (<VC2, VC3> for LCD).
Figure 2.1.1 shows the power supply configuration.

* Supply voltage: 623B...0.8 to 3.6 V, 62A3B...1.7 to 3.6 V

Note: • *External loads cannot be driven by the output voltage of the regulated voltage circuit and voltage booster circuit.*
• *See Chapter 6, "Electrical Characteristics", for voltage values.*

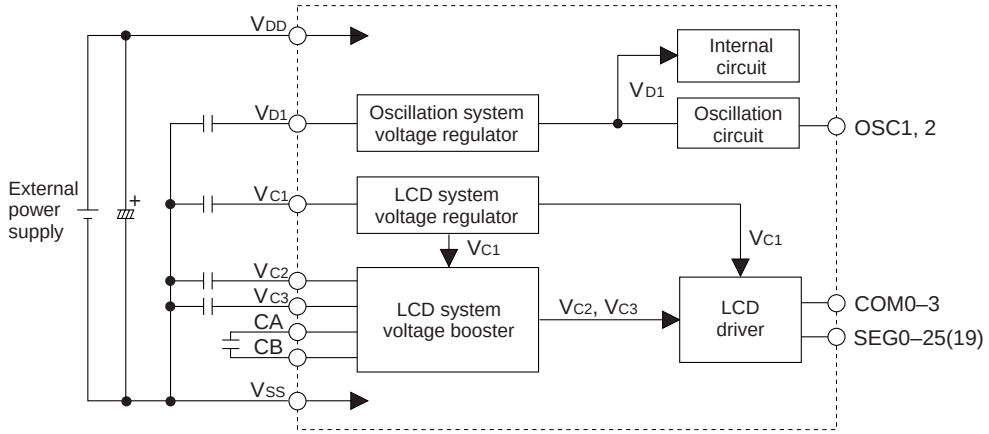


Fig. 2.1.1 Configuration of power supply (when internal voltage regulator is selected as LCD power by mask option)

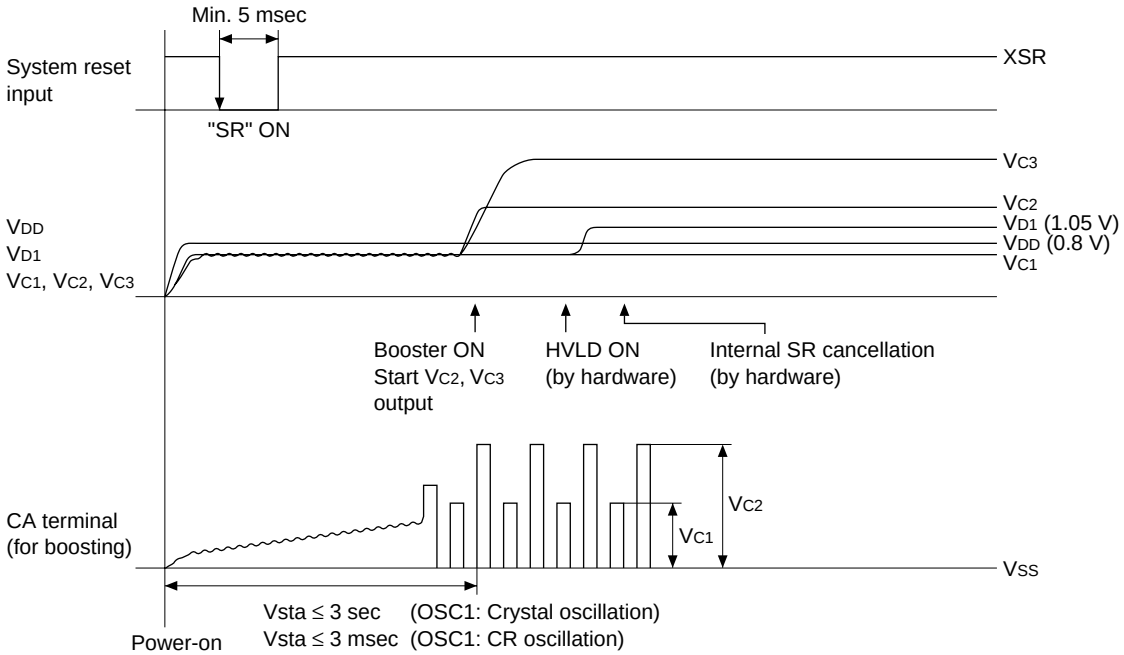


Fig. 2.1.2 Sequence after power on (E0C623B, VDD = 0.8 V)

2.1.1 Voltage <V_{D1}> for oscillation circuit and internal circuits

V_{D1} is a voltage for the oscillation circuit and the internal logic circuits.
V_{D1} is driven with the supply voltage V_{DD} in the normal operating mode.
The E0C623B can be set in the heavy load protection mode to protect the IC operation from voltage variation when heavy loads such as a buzzer is driven and to operate in a condition of $V_{DD} \leq 1.1$ V (see Section 4.10 for detail). In the heavy protection mode, the E0C623B drives V_{D1} with the boosted voltage V_{C2} (explained in the next section) for stabilizing operation in low supply voltage.
The E0C62A3B always drives V_{D1} with the supply voltage V_{DD}.

2.1.2 Voltage <V_{C1}–V_{C3}> for LCD driving

V_{C1}–V_{C3} are the LCD drive voltages. They can be generated by the internal LCD system power supply circuit or can be supplied from outside by selecting mask option.
The LCD system power supply circuit consists of two voltage circuits: a voltage regulator that generates the V_{C1} voltage and a voltage booster circuit that generates the V_{C2} and V_{C3} voltages by doubling and tripling the V_{C1} (when the internal voltage regulator is selected as the LCD power source by mask option).
The LCD system power supply circuit stops operating in the SLEEP mode (available for the CR oscillation model of the E0C623B and E0C62A3B). The voltages V_{C1} to V_{C3} go to V_{SS} level when it stops. (The SLEEP function cannot be used when an external LCD power supply is selected.)

In the heavy load protection mode in the E0C623B, the V_{C2} is also used for driving the oscillation system voltage regulator.

2.2 Initial Reset

To initialize the E0C623B Series circuits, an initial reset must be executed. There are three ways of doing this.

(1) External initial reset by simultaneous low input to terminals K00–K03 (depending on mask option)
(2) External initial reset via the $\overline{\text{RESET}}$ terminal
(3) Initial reset by the oscillation detection circuit

Figure 2.2.1 shows the configuration of the initial reset circuit.

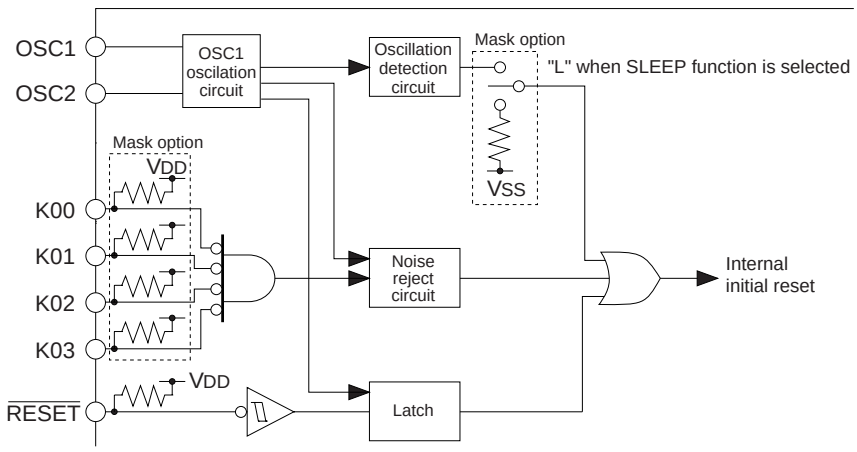


Fig. 2.2.1 Configuration of initial reset circuit

2.2.1 Simultaneous low input to input ports (K00–K03)

An initial reset can be performed by inputting low signals simultaneously to the input ports (K00–K03) selected with the mask option. The specified input port terminals must be kept low for at least a time shown in Table 2.2.1.1, because the signals pass through the noise rejection circuit. Table 2.2.1.2 shows the combinations of the input ports (K00–K03) that can be selected with the mask option.

Table 2.2.1.1 Simultaneous low input time

Model	Oscillation frequency	Simultaneous LOW set-up time (Min.)
E0C623B	32.768 kHz (crystal)	3 sec
	65 kHz (CR)	1.5 sec
E0C62A3B	500 kHz (CR, dividing ratio: 1/6)	1.2 sec
	1 MHz (ceramic, dividing ratio: 1/12)	1.2 sec

Table 2.2.1.2 Input port combinations

Selection	Combination
A	Not used
B	K00∗K01
C	K00∗K01∗K02
D	K00∗K01∗K02∗K03

When, for instance, mask option D (K00∗K01∗K02∗K03) is selected, an initial reset is executed when the signals input to the four ports K00–K03 are all low at the same time. If you use this function, make sure that the specified ports do not go low at the same time during normal operation.

2.2.2 Reset terminal ($\overline{RESET}$)

Initial reset can be executed externally by setting the reset terminal to a low level (VSS). After that the initial reset is released by setting the reset terminal to a high level (VDD) and the CPU starts operation. The reset input signal is maintained by the latch and becomes the internal initial reset signal. The latch is designed to be released by the signal that is divided by the oscillation clock. In normal operation, a reset release time shown in Table 2.2.2.1 is needed until the internal initial reset is released after the reset terminal goes to high level. Be sure to maintain the reset terminal at a low level for at least the reset input time shown in Table 2.2.2.1.
However, when turning the power on, the reset terminal should be set at a low level as in the timing shown in Figure 2.2.2.1.

Table 2.2.2.1 Reset time

Model	Oscillation frequency	Reset input pulse width (Min.)	Reset cancelation time by hardware inside of IC (Max.)
E0C623B	32.768 kHz (crystal)	5 msec	Reset terminal ↑ → 250 msec
	65 kHz (CR)	5 msec	Reset terminal ↑ → 125 msec
E0C62A3B	500 kHz (CR, division ratio: 1/6)	5 msec	Reset terminal ↑ → 98 msec
	1 MHz (ceramic, division ratio: 1/12)	5 msec	Reset terminal ↑ → 98 msec

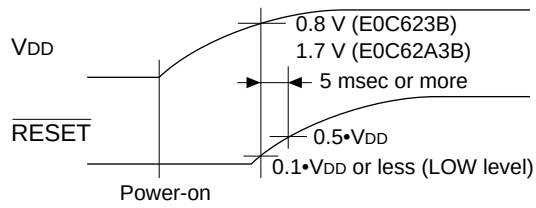


Fig. 2.2.2.1 Initial reset at power on

The reset terminal should be set to 0.1•VDD or less (low level) until the supply voltage becomes 0.8 V (E0C623B) or 1.7 V (E0C62A3B) or more. After that, a level of 0.5•VDD or less should be maintained more than 5 msec.

2.2.3 Oscillation detection circuit

The oscillation detection circuit outputs the initial reset signal at power-on until the oscillation circuit starts oscillating, or when the oscillation circuit stops oscillating for some reason.

Note:
- *Use the reset terminal or K00–K03 simultaneous low input for power-on reset because the circuit may not work due to chattering when the power is turned on.*
- *The oscillation detection function cannot be used when the mask option is selected as follows:*
  - When CR oscillation circuit and the SLEEP function are selected in the E0C623B.
  - When the SLEEP function is selected in the E0C62A3B.

2.2.4 Internal register following initialization

An initial reset initializes the CPU as shown in the table below.

Table 2.2.4.1 Initial setting values

CPU Core			
Name	Symbol	Bit size	Initial value
Program counter step	PCS	8	00H
Program counter page	PCP	4	1H
New page pointer	NPP	4	1H
Stack pointer	SP	8	Undefined
Index register X	X	8	Undefined
Index register Y	Y	8	Undefined
Register pointer	RP	4	Undefined
General-purpose register A	A	4	Undefined
General-purpose register B	B	4	Undefined
Interrupt flag	I	1	0
Decimal flag	D	1	0
Zero flag	Z	1	Undefined
Carry flag	C	1	Undefined

Peripheral Circuits		
Name	Bit size	Initial value
RAM	96 × 4	Undefined
Display memory	26 × 4	Undefined
Other peripheral circuits	–	*

* See Section 4.1, "Memory Map".

2.3 Test Terminal ($\overline{TEST}$)

This terminal is used when IC is inspected for shipment.
During normal operation connect it to VDD.

CHAPTER 3 CPU, ROM, RAM

3.1 CPU

The E0C623B Series employs the E0C6200B core CPU, so that register configuration, instructions, and so forth are virtually identical to those in other processors in the family using the E0C6200/6200A/6200B. Refer to the "E0C6200/6200A Core CPU Manual" for details of the E0C6200B.

Note the following points with regard to the E0C623B Series:

(1) The crystal oscillator model of the E0C623B does not support the SLEEP function, therefore the SLP instruction cannot be used.
The SLP instruction is only available for the E0C623B CR oscillation model and E0C62A3B which have the SLEEP function selected by mask option.

(2) Because the ROM capacity is 1,536 words, 12 bits per word, bank bits are unnecessary, and PCB and NBP are not used.

(3) The RAM page is set to 0 only, so the page part (XP, YP) of the index register that specifies addresses is invalid.

```
PUSH XP    POP XP    LD XP,r    LD r,XP
PUSH YP    POP YP    LD YP,r    LD r,YP
```

3.2 ROM

The built-in ROM, a mask ROM for the program, has a capacity of 1,536 × 12-bit steps. The program area is 6 pages (0–5), each consisting of 256 steps (00H–FFH). After an initial reset, the program start address is set to page 1, step 00H. The interrupt vectors are allocated to page l, steps 01H–08H.

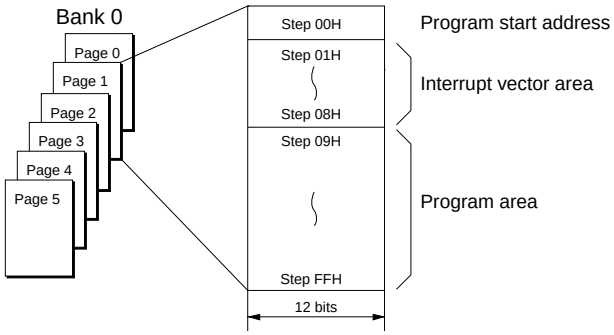


Fig. 3.2.1 ROM configuration

3.3 RAM

The RAM, a data memory for storing a variety of data, has a capacity of 96 words, 4-bit words. When programming, keep the following points in mind:

(1) Part of the data memory is used as stack area when saving subroutine return addresses and registers, so be careful not to overlap the data area and stack area.

(2) Subroutine calls and interrupts take up three words on the stack.

(3) Data memory 00H–0FH is the memory area pointed by the register pointer (RP).

CHAPTER 4 PERIPHERAL CIRCUITS AND OPERATION

Peripheral circuits (timer, I/O, and so on) of the E0C623B Series are memory mapped. Thus, all the peripheral circuits can be controlled by using memory operations to access the I/O memory. The following sections describe how the peripheral circuits operate.

4.1 Memory Map

The data memory of the E0C623B Series has an address space of 150 words, of which 32 words are allocated to display memory and 22 words, to I/O memory. Figure 4.1.1 show the overall memory map for the E0C623B Series, and Tables 4.1.1(a)–(b), the memory maps for the peripheral circuits (I/O space).

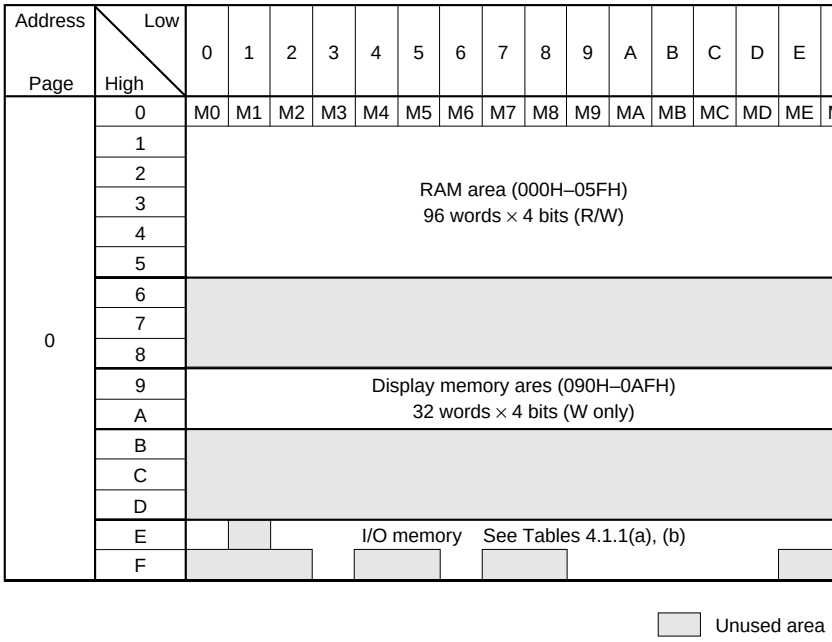


Fig. 4.1.1 Memory map

Note: Memory is not mounted in unused area within the memory map and in memory area not indicated in this chapter. For this reason, normal operation cannot be assured for programs that have been prepared with access to these areas.

Table 4.1.1(a) I/O memory map (0E0H–0EFH)

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
0E0H	K03	K02	K01	K00	K03	– *2	High	Low	K0 input port data
					K02	– *2	High	Low	
	R				K01	– *2	High	Low	
					K00	– *2	High	Low	
0E2H	SWL3	SWL2	SWL1	SWL0	SWL3	0			MSB
					SWL2	0			Stopwatch timer data
	R				SWL1	0			1/100sec (BCD)
					SWL0	0			LSB
0E3H	SWH3	SWH2	SWH1	SWH0	SWH3	0			MSB
					SWH2	0			Stopwatch timer data
	R				SWH1	0			1/10sec (BCD)
					SWH0	0			LSB
0E4H	TM3	TM2	TM1	TM0	TM3	0			Clock timer data (2 Hz)
					TM2	0			Clock timer data (4 Hz)
	R				TM1	0			Clock timer data (8 Hz)
					TM0	0			Clock timer data (16 Hz)
0E5H	SD3	SD2	SD1	SD0	SD3	– *2	High	Low	Serial interface
					SD2	– *2	High	Low	
	R/W				SD1	– *2	High	Low	data register (low-order 4 bits)
					SD0	– *2	High	Low	LSB
0E6H	SD7	SD6	SD5	SD4	SD7	– *2	High	Low	MSB
					SD6	– *2	High	Low	Serial interface
	R/W				SD5	– *2	High	Low	data register (high-order 4 bits)
					SD4	– *2	High	Low	
0E7H	SCTRG	SEN	SCS1	SCS0	SCTRG	– *2	Trigger	–	Serial interface trigger (writing)
	SCRUN				SCRUN	– *2	Run	Stop	Serial interface status (reading)
	W	R/W			SEN	0	↓	↑	Serial interface clock edge selection
	R				SCS1	0			Serial interface clock mode selection
					SCS0	0			0: Slave, 2: Master (CLK), 3: Master (CLK/2)
0E8H	EIK03	EIK02	EIK01	EIK00	EIK03	0	Enable	Mask	Interrupt mask register (K03)
					EIK02	0	Enable	Mask	Interrupt mask register (K02)
	R/W				EIK01	0	Enable	Mask	Interrupt mask register (K01)
					EIK00	0	Enable	Mask	Interrupt mask register (K00)
0E9H	0	EIP0	SIOMODE	EISIO	0 *3	– *2	–	–	Unused
					EIP0	0	Enable	Mask	Interrupt mask register (P0)
	R	R/W			SIOMODE	0	Output	Input	SIO terminal input/output control
					EISIO	0	Enable	Mask	Interrupt mask register (serial interface)
0EAH	0	0	EISW1	EISW0	0 *3	– *2	–	–	Unused
					0 *3	– *2	–	–	Unused
	R		R/W		EISW1	0	Enable	Mask	Interrupt mask register (stopwatch 1 Hz)
					EISW0	0	Enable	Mask	Interrupt mask register (stopwatch 10 Hz)
0EBH	0	EIT2	EIT8	EIT32	0 *3	– *2	–	–	Unused
					EIT2	0	Enable	Mask	Interrupt mask register (clock timer 2 Hz)
	R	R/W			EIT8	0	Enable	Mask	Interrupt mask register (clock timer 8 Hz)
					EIT32	0	Enable	Mask	Interrupt mask register (clock timer 32 Hz)
0ECH	0	0	0	ISIO	0 *3	– *2	–	–	Unused
					0 *3	– *2	–	–	Unused
	R				0 *3	– *2	–	–	Unused
					ISIO *4	0	Yes	No	Interrupt factor flag (serial interface)
0EDH	0	0	IP0	IK0	0 *3	– *2	–	–	Unused
					0 *3	– *2	–	–	Unused
	R				IP0 *4	0	Yes	No	Interrupt factor flag (P0)
					IK0 *4	0	Yes	No	Interrupt factor flag (K00–K03)
0EEH	0	0	ISW1	ISW0	0 *3	– *2	–	–	Unused
					0 *3	– *2	–	–	Unused
	R				ISW1 *4	– *2	Yes	No	Interrupt factor flag (stopwatch 1 Hz)
					ISW0 *4	0	Yes	No	Interrupt factor flag (stopwatch 10 Hz)
0EFH	0	IT2	IT8	IT32	0 *3	– *2	–	–	Unused
					IT2 *4	0	Yes	No	Interrupt factor flag (clock timer 2 Hz)
	R				IT8 *4	0	Yes	No	Interrupt factor flag (clock timer 8 Hz)
					IT32 *4	0	Yes	No	Interrupt factor flag (clock timer 32 Hz)

*1 Initial value at initial reset
*2 Not set in the circuit
*3 Always "0" being read
*4 Reset (0) immediately after being read

Table 4.1.1(b) I/O memory map (0F3H–0FDH)

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
0F3H	R03	R02	R01	R00	R03	1	High	Low	R03 output port data
					R02	1	High	Low	R02 output port data
			BUZZER	FOUT	R01	1	High	Low	R01 output port data
				BUZZER	BUZZER	1	Off	On	Buzzer output On/Off control
	R/W				R00	1	High	Low	R00 output port data
					FOUT	1	Off	On	FOUT output On/Off control
					$\overline{\text{BUZZER}}$	1	Off	On	Buzzer inverted output On/Off control
0F6H	P03	P02	P01	P00	P03	– *2	High	Low	P0 I/O port data
					P02	– *2	High	Low	
	R/W				P01	– *2	High	Low	
					P00	– *2	High	Low	
0F9H	0	TMRST	SWRUN	SWRST	0 *3	– *2	–	–	Unused
					TMRST*3	Reset	Reset	–	Clock timer reset
	R	W	R/W	W	SWRUN	0	Run	Stop	Stopwatch timer Run/Stop
					SWRST*3	Reset	Reset	–	Stopwatch timer reset
0FAH	HLMOD	0	0	0	HLMOD	1	Heavy	Normal	Heavy load protection mode (E0C623B)
					HLMOD	0	–	–	Fixed at "0" in the E0C62A3B
	R/W	R			0 *3	– *2	–	–	Unused
					0 *3	– *2	–	–	Unused
					0 *3	– *2	–	–	Unused
0FBH	CSDC	ALLOFF	ALLON	0	CSDC	0	Static	Dynamic	LCD drive mode switch
					ALLOFF	1	All Off	Normal	LCD all-off control
	R/W			R	ALLON	0	All On	Normal	LCD all-on control
					0 *3	– *2	–	–	Unused
0FCH	0	0	PLON	IOC	0 *3	– *2	–	–	Unused
					0 *3	– *2	–	–	Unused
	R		R/W		PLON	0	On	Off	I/O port pull-up control
					IOC	0	Output	Input	I/O port I/O control
0FDH	XBZR	0	XFOUT1	XFOUT0	XBZR	0	f_{BZL}	f_{BZH}	Buzzer frequency control (in 32 kHz: f_{BZL}=2 kHz, f_{BZH}=4 kHz)
					0 *3	– *2	–	–	Unused
	R/W	R	R/W		XFOUT1	0			FOUT frequency control
					XFOUT0	0			0: F1, 1: F2, 2: F3, 3: F4

*1 Initial value at initial reset
*2 Not set in the circuit
*3 Always "0" being read
*4 Reset (0) immediately after being read

4.2 Oscillation Circuit

4.2.1 Oscillator type

The E0C623B Series has a built-in oscillation circuit that generates the operating clock of the CPU and the peripheral circuit. The oscillator type can be selected by mask option. Table 4.2.1.1 shows the oscillator type and oscillation frequency available for each model. See Chapter 6, "Electrical Characteristics" for the oscillation start time and other characteristics.

Table 4.2.1.1 Oscillator type

Model	Oscillation circuit (selected by mask option)	Supply voltage
E0C623B	Crystal (32.768 kHz, Typ.) or CR (65 kHz, Typ.)	0.8–3.6 V
E0C62A3B	CR (250 kHz–500 kHz) or Ceramic (400 kHz–1 MHz)	1.7–3.6 V

4.2.2 Mask option

(1) Oscillator type

The oscillator can be selected from the two types shown in Table 4.2.1.1 for each of the E0C623B and the E0C62A3B models.

(2) Dividing ratio of the prescaler (E0C62A3B)

The high-speed CPU E0C62A3B has a built-in prescaler for making the source clock of the frequency divider that generates the operating clocks of the peripheral circuits. The prescaler outputs fosc/12 clock when ceramic oscillation is selected and fosc/6 clock when CR oscillation is selected.
The E0C623B delivers the oscillation clock (32 kHz or 65 kHz) directly to the frequency divider for the peripheral circuits.

4.2.3 Crystal oscillation circuit

The crystal oscillation circuit can be selected in the E0C623B by mask option. The oscillation frequency (fosc) is 32.768 kHz (Typ.).
Figure 4.2.3.1 shows the configuration of the crystal oscillation circuit.

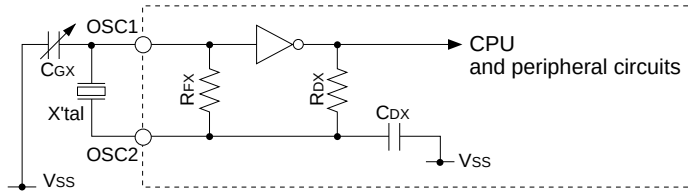


Fig. 4.2.3.1 Configuration of crystal oscillation circuit

As Figure 4.2.3.1 indicates, the crystal oscillation circuit can be configured simply by connecting the crystal oscillator X'tal (Typ. 32.768 kHz) between the OSC1 and OSC2 terminals and the trimmer capacitor CGX (5–25pF) between the OSC1 and VSS terminals.

4.2.4 CR oscillation circuit

The CR oscillation circuit can be selected for all the E0C623B models by mask option. The oscillation frequency (fosc) of the E0C623B is 65 kHz (Typ.) and the E0C62A3B is 250 kHz to 500 kHz.
Figure 4.2.4.1 shows the configuration of the CR oscillation circuit.

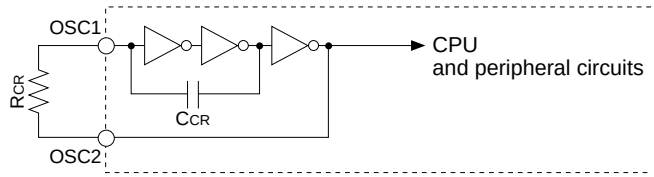


Fig. 4.2.4.1 Configuration of CR oscillation circuit

As Figure 4.2.4.1 indicates, the CR oscillation circuit can be configured simply by connecting the resistor RCR between terminals OSC1 and OSC2 since capacity (CCR) is built-in.
See Chapter 6, "Electrical Characteristics" for RCR value.

4.2.5 Ceramic oscillation circuit

The ceramic oscillation circuit can be selected in the E0C62A3B by mask option. The oscillation frequency (fosc) is 400 kHz to 1MHz.
Figure 4.2.5.1 shows the configuration of the ceramic oscillation circuit.

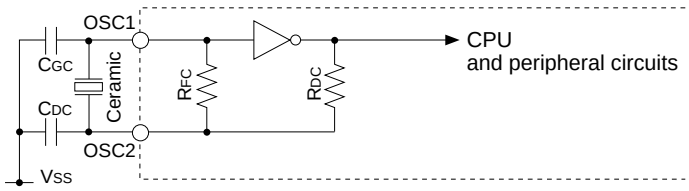
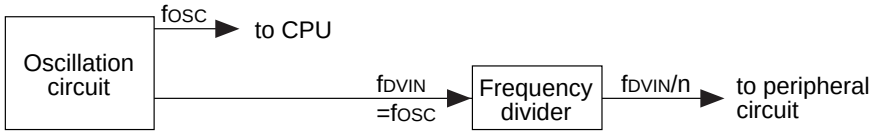


Fig. 4.2.5.1 Configuration of ceramic oscillation circuit

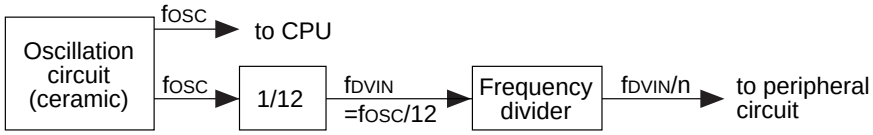
As Figure 4.2.5.1 indicates, the ceramic oscillation circuit can be configured by connecting the ceramic oscillator (400 kHz–1 MHz) between the OSC1 and OSC2 terminals, the gate capacitor CGC between the OSC1 and VSS terminals, and the drain capacitor CDC between the OSC2 and VSS terminals.
For both CGC and CDC, connect capacitors that are about 100 pF.

4.2.6 Frequency divider

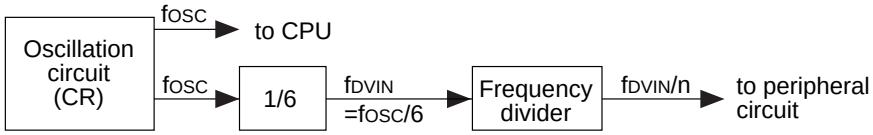
The CPU operates by inputting the oscillation clock directly.
The operating clocks for the peripheral circuits are generated by the frequency divider at the post stage of the oscillation circuit.



E0C623B



E0C62A3B (when ceramic oscillation is selected)



E0C62A3B (when CR oscillation is selected)

Fig. 4.2.6.1 Configuration of divider

In the E0C623B, the oscillation clock is directly input to the divider for the peripheral circuits.
Since the E0C62A3B is a high-speed model, the oscillation clock is divided by 12 (ceramic) or 6 (CR) with the prescaler and then the divided clock is input to the divider for the peripheral circuits.

Table 4.2.6.1 shows the frequencies of the clocks/signals used in the peripheral circuits.

Table 4.2.6.1 Frequency of peripheral circuit clocks/signals

Clocks and signals	Frequency			
	E0C623B Crystal oscillation (32.768 kHz)	E0C623B CR oscillation (65 kHz)	E0C62A3B Ceramic oscillation (f_{DVIN}=f_{OSC}/12)	E0C62A3B CR oscillation (f_{DVIN}=f_{OSC}/6)
CPU operating clock	f_{OSC}=32kHz	f_{OSC}=65kHz	f_{OSC}	f_{OSC}
Input port noise rejection clock	f_{OSC}/8=4kHz	f_{OSC}/8=8kHz	f_{OSC}/96	f_{OSC}/48
Buzzer signal (f_{BZL})	f_{OSC}/16=2kHz	f_{OSC}/16=4kHz	f_{OSC}/192	f_{OSC}/96
Buzzer signal (f_{BZH})	f_{OSC}/8=4kHz	f_{OSC}/8=8kHz	f_{OSC}/96	f_{OSC}/48
FOUT signal (F1-1)	f_{OSC}/128=256Hz	f_{OSC}/128=512Hz	f_{OSC}/1536	f_{OSC}/768
FOUT signal (F1-2,F2-1)	f_{OSC}/64=512Hz	f_{OSC}/64=1kHz	f_{OSC}/768	f_{OSC}/384
FOUT signal (F1-3,F2-2,F3-1)	f_{OSC}/32=1kHz	f_{OSC}/32=2kHz	f_{OSC}/384	f_{OSC}/192
FOUT signal (F1-4,F2-3,F3-2,F4-1)	f_{OSC}/16=2kHz	f_{OSC}/16=4kHz	f_{OSC}/192	f_{OSC}/96
FOUT signal (F1-5,F2-4,F3-3,F4-2)	f_{OSC}/8=4kHz	f_{OSC}/8=8kHz	f_{OSC}/96	f_{OSC}/48
FOUT signal (F2-5,F3-4,F4-3)	f_{OSC}/4=8kHz	f_{OSC}/4=16kHz	f_{OSC}/48	f_{OSC}/24
FOUT signal (F3-5,F4-4)	f_{OSC}/2=16kHz	f_{OSC}/2=32kHz	f_{OSC}/24	f_{OSC}/12
FOUT signal (F4-5)	f_{OSC}/1=32kHz	f_{OSC}/1=65kHz	f_{OSC}/12	f_{OSC}/6
LCD FR signal (1/4 duty)	f_{OSC}/1024=32Hz	f_{OSC}/1024=64Hz	f_{OSC}/12288	f_{OSC}/6144
LCD FR signal (1/3 duty)	f_{OSC}/768=42.7Hz	f_{OSC}/768=85.3Hz	f_{OSC}/9216	f_{OSC}/4608
LCD FR signal (1/2 duty)	f_{OSC}/1024=32Hz	f_{OSC}/1024=64Hz	f_{OSC}/12288	f_{OSC}/6144
Clock timer input clock	f_{OSC}/128=256Hz	f_{OSC}/128=512Hz	f_{OSC}/1536	f_{OSC}/768
Clock timer data (D3)	f_{OSC}/16384=2Hz	f_{OSC}/16384=4Hz	f_{OSC}/196608	f_{OSC}/98304
Clock timer data (D2)	f_{OSC}/8192=4Hz	f_{OSC}/8192=8Hz	f_{OSC}/98304	f_{OSC}/49152
Clock timer data (D1)	f_{OSC}/4096=8Hz	f_{OSC}/4096=16Hz	f_{OSC}/49152	f_{OSC}/24576
Clock timer data (D0)	f_{OSC}/2048=16Hz	f_{OSC}/2048=32Hz	f_{OSC}/24576	f_{OSC}/12288
Clock timer interrupt (IT32)	f_{OSC}/1024=32Hz	f_{OSC}/1024=64Hz	f_{OSC}/12288	f_{OSC}/6144
Clock timer interrupt (IT8)	f_{OSC}/4096=8Hz	f_{OSC}/4096=16Hz	f_{OSC}/49152	f_{OSC}/24576
Clock timer interrupt (IT2)	f_{OSC}/16384=2Hz	f_{OSC}/16384=4Hz	f_{OSC}/196608	f_{OSC}/196608
Stopwatch timer input clock	f_{OSC}/128=256Hz	f_{OSC}/128=512Hz	f_{OSC}/1536	f_{OSC}/768
Serial I/F input clock (CLK)	f_{OSC}=32kHz	f_{OSC}=65kHz	f_{OSC}	f_{OSC}

f_{OSC}: Oscillation frequency
f_{DVIN}: Input clock frequency of divider for peripheral circuits

Note: This manual describes frequencies and times when the crystal oscillation circuit (32.768 kHz) of the E0C623B has been selected unless there has been a special description. Be aware that the frequencies and times vary when the E0C623B CR oscillator model or the E0C62A3B is used.

4.2.7 Operation in SLEEP mode

The E0C623B CR oscillator model and the E0C62A3B can incorporate the SLEEP function that reduces current consumption in the standby mode with mask option selection.
The oscillation circuit stops oscillating when the SLEEP mode is set by the SLP instruction.
The oscillation circuit resumes oscillating when an input interrupt cancels the SLEEP mode, however some startup time is required for stabilizing oscillation (See Chapter 6, "Electrical Characteristics"). Therefore be sure the interval is long enough before controlling the peripheral circuits that use the oscillation clock as the source clock.
Note that the oscillation detection function cannot be used when the SLEEP function is selected by mask option.

4.3 Input Port (K00–K03)

4.3.1 Configuration of input port

The E0C623B Series has 4 bits of general-purpose input port. Each of the input port terminals (K00–K03) has an internal pull-up resistor. The pull-up resistor can be selected for each bit with the mask option. Figure 4.3.1.1 shows the configuration of input port.

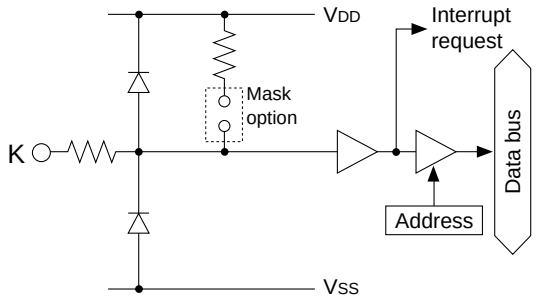


Fig. 4.3.1.1 Configuration of input port

Selecting "pull-up resistor enabled" with the mask option allows input from a push button, key matrix, and so forth. When "pull-up resistor disabled" is selected, the port can be used for slide switch input and interfacing with other LSIs.

4.3.2 Interrupt function

All four input port bits (K00–K03) provide the interrupt function.
Figure 4.3.2.1 shows the configuration of K00–K03.

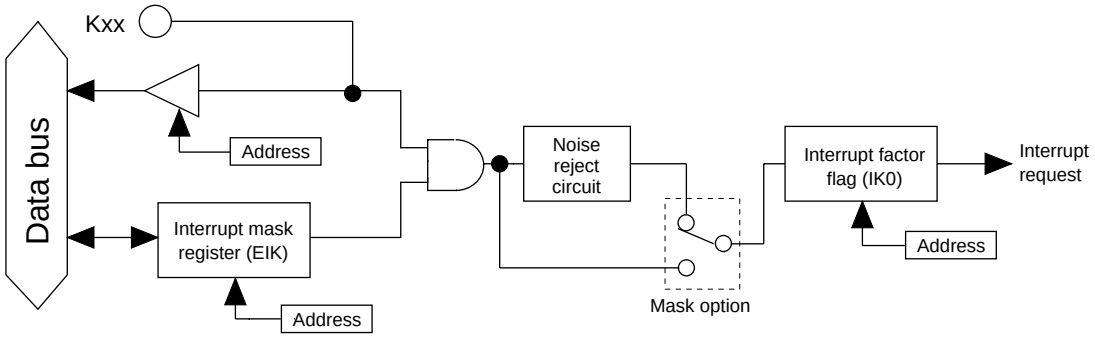
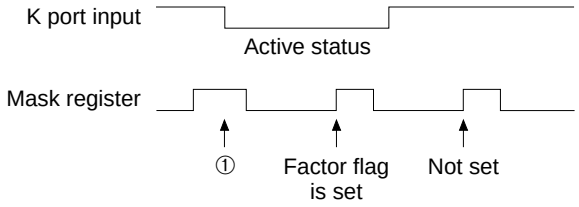


Fig. 4.3.2.1 Input interrupt circuit configuration (K00–K03)

The interrupt mask registers (EIK00–EIK03) enable the interrupt mask to be selected individually for K00–K03. An interrupt occurs at the falling edge of the input signal which is not masked and the interrupt factor flag (IK0) is set to "1".

Input interrupt programming related precautions



- When the content of the mask register is rewritten, while the port K input is in the active status.
- The input interrupt factor flag is set at ①.

Fig. 4.3.2.2 Input interrupt timing

When using an input interrupt, if you rewrite the content of the mask register, when the value of the input terminal which becomes the interrupt input is in the active status (input terminal = low status), the factor flag for input interrupt may be set.
For example, a factor flag is set with the timing of ① shown in Figure 4.3.2.2. However, when clearing the content of the mask register with the input terminal kept in the low status and then setting it, the factor flag of the input interrupt is again set at the timing that has been set.
Consequently, when the input terminal is in the active status (low status), do not rewrite the mask register (clearing, then setting the mask register), so that a factor flag will only set at the falling edge in this case. When clearing, then setting the mask register, set the mask register, when the input terminal is not in the active status (high status).

4.3.3 Mask option

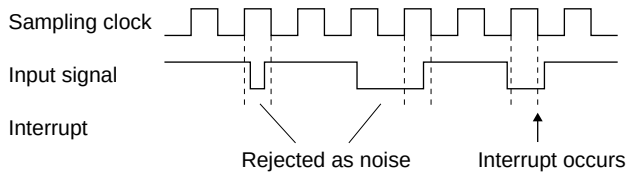
The contents that can be selected with the input port mask option are as follows:

(1) Pull-up resistor

An internal pull-up resistor can be selected for each of the four bits of the input ports (K00–K03). Having selected "pull-up resistor disabled", take care that the input does not float. Select "pull-up resistor enabled" for input ports that are not being used.

(2) Noise rejection circuit

The input interrupt circuit contains a noise rejection circuit to prevent interrupts form occurring through noise. The mask option enables selection of the noise rejection circuit for each terminals. When the noise rejection circuit is used, pulses shorter than 0.5 cycles of the sampling clock are rejected as noise. To be certain interrupts are generated the input signal must have at least 1.5 cycles of low width. Be aware that pulses between 0.5 and 1.5 cycles may or may not be regarded as noise depending on the input timing.



Sampling clock frequency: E0C623B fosc/8 4 kHz when fosc = 32 kHz
E0C62A3B fDVIN/8 fDVIN: fosc/12 (ceramic oscillation) or fosc/6 (CR oscillation)

Fig. 4.3.3.1 Noise rejection

4.3.4 Control of input ports

Table 4.3.4.1 shows the input port control bits and their addresses.

Table 4.3.4.1 I/O memory (Input port)

Address	Register								Comment
	D3	D2	D1	D0	Name	Init *1	1	0	
0E0H	K03	K02	K01	K00	K03	– *2	High	Low	K0 input port data
					K02	– *2	High	Low	
	R				K01	– *2	High	Low	
					K00	– *2	High	Low	
0E8H	EIK03	EIK02	EIK01	EIK00	EIK03	0	Enable	Mask	Interrupt mask register (K03)
					EIK02	0	Enable	Mask	Interrupt mask register (K02)
	R/W				EIK01	0	Enable	Mask	Interrupt mask register (K01)
					EIK00	0	Enable	Mask	Interrupt mask register (K00)
0EDH	0	0	IP0	IK0	0 *3	– *2	–	–	Unused
					0 *3	– *2	–	–	Unused
	R				IP0 *4	0	Yes	No	Interrupt factor flag (P0)
					IK0 *4	0	Yes	No	Interrupt factor flag (K00–K03)

*1 Initial value at initial reset
*2 Not set in the circuit
*3 Always "0" being read
*4 Reset (0) immediately after being read

K00–K03: Input port data (0E0H)

The input data of the input port terminals can be read with these registers.

When "1" is read: High level
When "0" is read: Low level
Writing: Invalid

The value read is "1" when the terminal voltage of the input port (K00–K03) goes high (V_{DD}), and "0" when the voltage goes low (V_{SS}). These bits are reading, so writing cannot be done.

EIK00–EIK03: Interrupt mask registers (0E8H)

Masking the interrupt of the input port terminals can be done with these registers.

When "1" is written: Enabled
When "0" is written: Masked
Reading: Valid

With these registers, masking of the input port bits can be done for each of the four bits.
At initial reset, these registers are all set to "0".

IK0: Interrupt factor flag (0EDH D0)

This flag indicates the occurrence of an input interrupt.

When "1" is read: Interrupt has occurred
When "0" is read: Interrupt has not occurred
Writing: Invalid

IK0 is the interrupt factor flag corresponding to the input ports K00–K03 and is set to "1" at the falling edge of the input signal. From the status of this flag, the software can decide whether an input interrupt has occurred or not.
This flag is reset when the software has read it.
Reading of interrupt factor flag is available at EI, but be careful in the following cases.
If the interrupt mask register value corresponding to the interrupt factor flag to be read is set to "1", an interrupt request will be generated by the interrupt factor flag set timing, or an interrupt request will not be generated. Be very careful when interrupt factor flags are in the same address.
At initial reset, this flag is set to "0".

4.3.5 Programming notes

(1) When modifying the input port from low level to high level with pull-up resistor, a delay will occur at the rise of the waveform due to time constant of the pull-up resistor and input gate capacities. Provide appropriate waiting time in the program when reading an input port.

(2) Reading of the interrupt factor flag is available at EI, but be careful in the following cases.
If the interrupt mask register value corresponding to the interrupt factor flag to be read is set to "1", an interrupt request will be generated by the interrupt factor flag set timing, or an interrupt request will not be generated. Be very careful when interrupt factor flags are in the same address.

4.4 Output Port (R00–R03)

4.4.1 Configuration of output port

The E0C623B Series has 4 bits of general output ports (R00–R03).
Output specifications of the output ports can be selected individually with the mask option. Two kinds of output specifications are available: complementary output and Nch open drain output. Also, the mask option enables the output ports R00 and R01 to be used as special output ports. Figure 4.4.1.1 shows the configuration of the output ports.

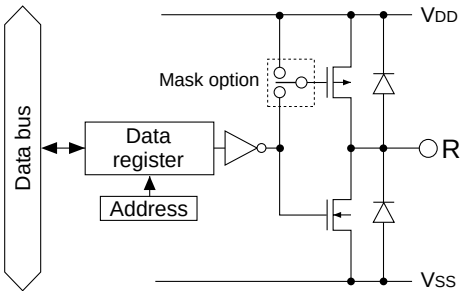


Fig. 4.4.1.1 Configuration of output ports

In the DC output mode, the output terminal goes high (V_{DD}) when "1" is written to the data register and goes low (V_{SS}) when "0" is written. At initial reset, the output terminal goes high.

4.4.2 Mask option

The mask option enables the following output port selection.

(1) Output specifications of output ports

The output specifications for the output ports (R00–R03) can be selected from complementary output and Nch open drain output for each of the four bits. However, even when Nch open drain output is selected, a voltage exceeding the power voltage must not be supplied to the output port.

(2) Special output

In addition to the regular DC output, special output can be selected for output ports R00 and R01, as shown in Table 4.4.2.1.

Table 4.4.2.1 Special output

Output port	Special output
R00	FOUT or $\overline{\text{BUZZER}}$ output
R01	BUZZER output

(3) BUZZER signal polarity

When driving a buzzer using the BUZZER (R01) output terminal only, the polarity of the BUZZER signal off status can be selected.

4.4.3 Special output

Figure 4.4.3.1 shows the structure of output ports R00–R03.
As shown in the previous section, the R00 terminal and the R01 terminal can be used as special output ports by selecting with mask option.

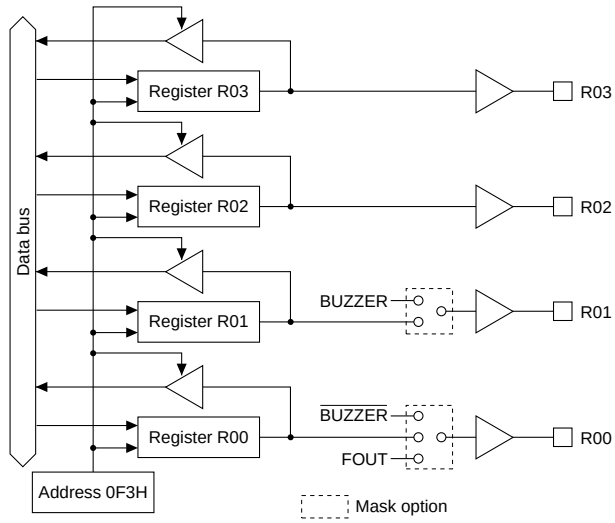


Fig. 4.4.3.1 Structure of output port R00–R03

FOUT (R00)

When the output port R00 is set as the FOUT output port, the R00 will output the fosc (CPU operating clock frequency) clock or the clock that is generated by dividing the fosc clock. The clock frequency can be selected individually for F1–F4, from among 5 types by mask option; one among F1–F4 is selected by software (XFOUT register) and used.
The types of frequency which can be selected are shown in Table 4.4.3.1.

Table 4.4.3.1 FOUT clock frequency

Setting value	Clock frequency (Hz)			
	F1 (XFOUT)=(0, 0)	F2 (XFOUT)=(0, 1)	F3 (XFOUT)=(1, 0)	F4 (XFOUT)=(1, 1)
1	f/128	f/64	f/32	f/16
2	f/64	f/32	f/16	f/8
3	f/32	f/16	f/8	f/4
4	f/16	f/8	f/4	f/2
5	f/8	f/4	f/2	f/1

E0C623B: f=fOSC 32 kHz or 65 kHz Typ.
E0C62A3B: f=fDVIN fDVIN=fOSC/12 (ceramic oscillation) or fOSC/6 (CR oscillation)

When "0" is written to the FOUT (R00) register, the FOUT (R00) terminal outputs the clock with the specified frequency. When "1" is written, the FOUT terminal goes high.
Figure 4.4.3.2 shows the output waveform of the FOUT output.

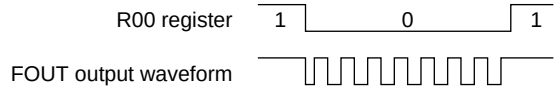


Fig. 4.4.3.2 FOUT output waveform

Note: A hazard may occur when the FOUT signal is turned on or off.

BUZZER, $\overline{\text{BUZZER}}$ (R01, R00)

The output ports R01 and R00 can be set to BUZZER output port and $\overline{\text{BUZZER}}$ output (BUZZER reverse output) port, respectively.

Direct driving of piezo-electric buzzer

By setting the R01 to the BUZZER output port and the R00 to the $\overline{\text{BUZZER}}$ output port, these two terminals can directly drive a piezo-electric buzzer. The $\overline{\text{BUZZER}}$ output (R00) can only be set if the R01 is set to the BUZZER output.
The output signal polarity is a high level while the buzzer signal is off.
At initial reset, the output terminals go high.
When "0" is written to the BUZZER (R01)/$\overline{\text{BUZZER}}$ (R00) registers, the output terminals output the buzzer signals. When "1" is written, the terminals go high.
Figure 4.4.3.3 shows the buzzer direct drive waveform.

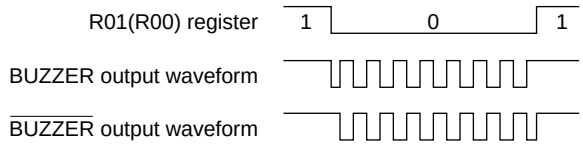


Fig. 4.4.3.3 BUZZER output waveform (direct driving)

Single terminal driving of piezo-electric buzzer

The piezo-electric buzzer can be driven with one terminal by setting the R01 to the BUZZER output terminal. In this case, the polarity of the buzzer off signal can also be selected from high level and low level by mask option.
At initial reset, the buzzer output goes off and the output terminal (R01) is set to the level that is selected by mask option.
When "0" is written to the BUZZER (R01) register, the output terminal outputs the buzzer signal.
Figure 4.4.3.4 shows the buzzer output waveform in single terminal driving.

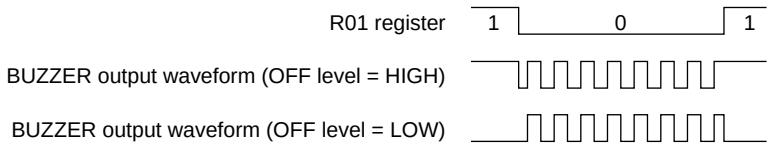


Fig. 4.4.3.4 BUZZER output waveform (single terminal driving)

BUZZER frequency

The buzzer signal frequency can be selected from 2 types (f_{BZL}, f_{BZH}) using the XBZR register. The frequencies are set as in Table 4.4.3.2 according to the model.

Table 4.4.3.2 BUZZER frequency

Buzzer frequency	Frequency			
	E0C623B Crystal oscillation (32.768 kHz)	E0C623B CR oscillation (65 kHz)	E0C62A3B Ceramic oscillation	E0C62A3B CR oscillation
f_{BZL} (XBZR="1")	f_{OSC}/16=2kHz	f_{OSC}/16=4kHz	f_{OSC}/192	f_{OSC}/96
f_{BZH} (XBZR="0")	f_{OSC}/8=4kHz	f_{OSC}/8=8kHz	f_{OSC}/96	f_{OSC}/48

4.4.4 Control of output ports

Table 4.4.4.1 shows the output port control bits and their addresses.

Table 4.4.4.1 I/O memory (Output port)

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
0F3H	R03	R02	R01	R00	R03	1	High	Low	R03 output port data
			FOUT		R02	1	High	Low	R02 output port data
			BUZZER	BUZZER	R01	1	High	Low	R01 output port data
	R/W				BUZZER	1	Off	On	Buzzer output On/Off control
					R00	1	High	Low	R00 output port data
					FOUT	1	Off	On	FOUT output On/Off control
					BUZZER	1	Off	On	Buzzer inverted output On/Off control
0FDH	XBZR	0	XFOUT1	XFOUT0	XBZR	0	f_{BZL}	f_{BZH}	Buzzer frequency control (in 32 kHz: f_{BZL}=2 kHz, f_{BZH}=4 kHz)
					0 *3	– *2	–	–	Unused
	R/W	R	R/W		XFOUT1	0			FOUT frequency control
					XFOUT0	0			0: F1, 1: F2, 2: F3, 3: F4

*1 Initial value at initial reset
*2 Not set in the circuit
*3 Always "0" being read
*4 Reset (0) immediately after being read

R00–R03: Output port data (0F3H)

Sets the output data for the output ports.

When "1" is written: High output
When "0" is written: Low output
Reading: Valid

The output port terminals output the data written to the corresponding registers (R00–R03) without changing it. When "1" is written to the register, the output port terminal goes high (V_{DD}), and when "0" is written, the output port terminal goes low (V_{SS}).
At initial reset, these registers are all set to "1".

R00 (when FOUT is selected): Special output control (0F3H D0)

Controls the FOUT (clock) output.

When "1" is written: High level (DC) output
When "0" is written: Clock output
Reading: Valid

When "0" is written to the FOUT (R00) register, the FOUT (R00) terminal outputs the FOUT signal.
At initial reset, this register is set to "1".

XFOUT0, XFOUT1: FOUT frequency control (0FDH D0 and D1)

Selects the output frequency when the R00 port is set for FOUT output.

Table 4.4.4.2 FOUT frequency selection

XFOUT1	XFOUT0	Frequency selected
0	0	F1
0	1	F2
1	0	F3
1	1	F4

At initial reset, these registers are set to "0".

R00, R01 (when buzzer output is selected): Special output port data (0F3H D0 and D1)

Controls the buzzer output.

When "1" is written:	OFF	High level (DC) output (R00 can output High level only) High level (DC) output (when "OFF level = High" is selected for R01) Low level (DC) output (when "OFF level = Low" is selectedfot R01)
When "0" is written:	ON	Buzzer output
Reading:	Valid	

The $\overline{\text{BUZZER}}$ and BUZZER outputs can be controlled by writing data to the R00 and R01 registers.
At initial reset, these registers are set to "1".

XBZR: Buzzer frequency control (0FDH D3)

Selects the frequency of the buzzer signal.

When "1" is written:	f_{BZL}	(2 kHz when the oscillation frequency is 32 kHz)
When "0" is written:	f_{BZH}	(4 kHz when the oscillation frequency is 32 kHz)
Reading:	Valid	

When the R01 and/or R00 ports are set as the buzzer output port, the frequency of the buzzer signal can be selected by this register.
When "1" is written to this register, the frequency is set to f_{BZL} (E0C623B: $f_{OSC}/16$, E0C62A3B: $f_{DVIN}/16$), and f_{BZH} (E0C623B: $f_{OSC}/8$, E0C62A3B: $f_{DVIN}/8$) when "0" is written.
At initial reset, this register is set to "0".

4.4.5 Programming note

The FOUT and buzzer output signals may produce hazards when the output ports R00 and R01 are turned on or off.

4.5 I/O Port (P00–P03)

4.5.1 Configuration of I/O port

The E0C623B Series has 4 bits of general-purpose I/O ports. Figure 4.5.1.1 shows the configuration of the I/O ports. The four bits of the I/O ports P00–P03 can be set to either input mode or output mode by writing data to the I/O control register (IOC).
Furthermore, the I/O port that is selected by mask option can generate input interrupts.

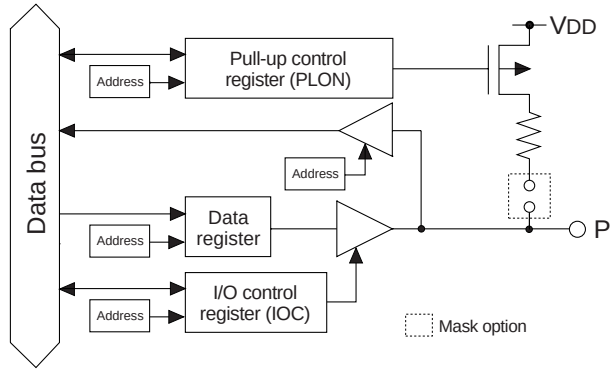


Fig. 4.5.1.1 Configuration of I/O port

Note: The I/O port terminals (P00–P03) are shared with the input/output terminals of the serial interface and the terminals that are not used for the serial interface can only be used as general-purpose I/O ports or input-only ports. This section explains only the control of the I/O port and input-only port.

4.5.2 Mask option

The following specifications of the I/O port can be selected by mask option:

(1) Terminal configuration

The terminal functions can be selected. The terminal configuration varies according to the serial interface setting.

Table 4.5.2.1 Terminal configuration of P00–P03

No.	P00	P01	P02	P03	No.	P00	P01	P02	P03
1	I/O	I/O	I/O	I/O	8	SIO	MODE	$\overline{\text{SCLK}}$	$\overline{\text{SRDY}}$
2	I/O	I/O	I/O	I	9	SIO	MODE	$\overline{\text{SCLK}}$	I/O
3	SIN	SOUT	$\overline{\text{SCLK}}$	$\overline{\text{SRDY}}$	10	SIO	MODE	$\overline{\text{SCLK}}$	I
4	SIN	SOUT	$\overline{\text{SCLK}}$	I/O	11	SIO	I/O	$\overline{\text{SCLK}}$	$\overline{\text{SRDY}}$
5	SIN	SOUT	$\overline{\text{SCLK}}$	I	12	SIO	I	$\overline{\text{SCLK}}$	$\overline{\text{SRDY}}$
6	SIN	I/O	$\overline{\text{SCLK}}$	I/O	13	SIO	I/O	$\overline{\text{SCLK}}$	I/O
7	SIN	I/O	$\overline{\text{SCLK}}$	I	14	SIO	I/O	$\overline{\text{SCLK}}$	I

I/O: I/O port terminal (input interrupt is disabled)
I: Input-only terminal (input interrupt is enabled)
SIN, SOUT, SIO, $\overline{\text{SCLK}}$, $\overline{\text{SRDY}}$, MODE: Terminal for serial interface

See Section 4.9, "Serial Interface", for the serial interface terminals.

(2) Output specifications

The output specification during output mode (IOC = "1") of the I/O port can be set with the mask option for either complementary output or Nch open drain output. This setting can be performed for each bit of the I/O port. However, when Nch open drain output has been selected, voltage in excess of the supply voltage must not be applied to the port.

(3) Pull-up resistor

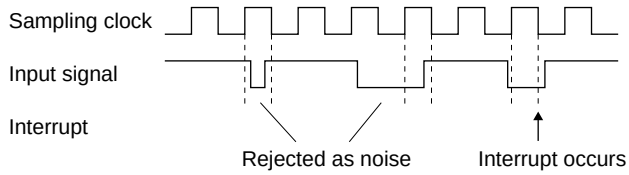
Whether or not the I/O port terminal will use built-in pull-up resistor which is turned on during input mode can be selected.

(4) Interrupt port

When the P01 or the P03 is set as an input-only port, the port can generate an input interrupt. This function cannot be selected for the I/O ports and the serial interface ports.

(5) Noise rejection circuit

The input interrupt circuit contains a noise rejection circuit to prevent interrupts form occurring through noise. The mask option enables selection of the noise rejection circuit for each terminals. When the noise rejection circuit is used, pulses shorter than 0.5 cycles of the sampling clock are rejected as noise. To be certain interrupts are generated the input signal must have at least 1.5 cycles of low width. Be aware that pulses between 0.5 and 1.5 cycles may or may not be regarded as noise depending on the input timing.



Sampling clock frequency: E0C623B fOSC/8 4 kHz when fOSC = 32 kHz
E0C62A3B fDVIN/8 fDVIN: fOSC/12 (ceramic oscillation) or fOSC/6 (CR oscillation)

Fig. 4.5.2.1 Noise rejection

4.5.3 I/O control register and I/O mode

Input or output mode can be set for the I/O ports P00–P03 by writing data to the I/O control register IOC.

To set the input mode, write "0" to the I/O control register (IOC). When the I/O ports are set to the input mode, the terminals become high impedance and they work as input ports. However, when the pull-up explained in the following section has been set by software, the input line is pulled up only during this input mode.

The output mode is set when "1" is written to the I/O control register (IOC). When the I/O ports are set to the output mode, thet work as output ports and output a high signal (VDD) when the port output data is "1", and a low signal (VSS) when the port output data is "0". If perform the read out in each mode; when output mode, the register value is read out, and when input mode, the port value is read out.

At initial reset, the I/O control register is set to "0", and the I/O ports enter the input mode.
The ports that are set for the serial interface or set as input only cannot be controlled by the IOC register.

4.5.4 Control of pull-up

Pull-up resistors can be added to the I/O port and input-only port by mask option.

The pull-up resistors of the I/O port turn on when "1" is written to the pull-up control register PLON and the ports are pulled up. When "0" is written, the ports are not pulled-up. At initial reset, the pull-up control register is set to "0". However, the ports will not be pulled up even if the PLON is set to "1" when the I/O ports are set in the output mode.
The pull-up resistor of the input-only port is always turned on regardless of the PLON setting.

4.5.5 Interrupt function

The I/O ports P01 or P03 can generate an input interrupt. To use this function set the P01 or P03 to input only and select the interrupt function by mask option.
Figure 4.5.5.1 shows the configuration of the interrupt circuit.

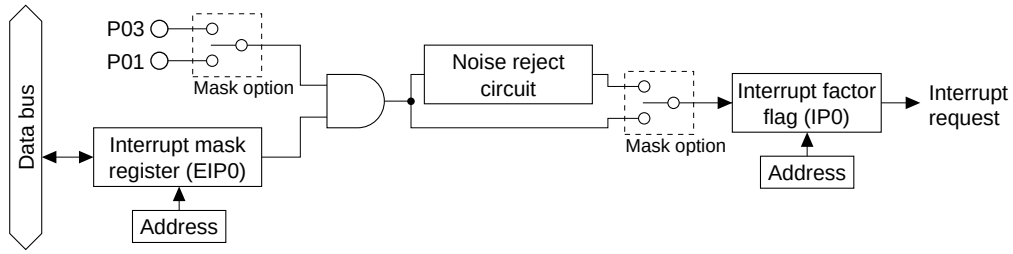


Fig. 4.5.5.1 Configuration of interrupt circuit

The input interrupt can be masked using the interrupt mask register EIP0. The input interrupt occurs at the falling edge of the signal input to the selected port only when the interrupt has been enabled by the interrupt mask register. When an input interrupt occurs, the interrupt factor flag IP0 is set to "1".

4.5.6 Control of I/O port

Table 4.5.6.1 shows the I/O port control bits and their addresses.

Table 4.5.6.1 I/O memory (I/O port)

Address	Register								Comment
	D3	D2	D1	D0	Name	Init *1	1	0	
0E9H	0	EIP0	SIOMODE	EISIO	0 *3	– *2	–	–	Unused
					EIP0	0	Enable	Mask	Interrupt mask register (P0)
	R	R/W			SIOMODE	0	Output	Input	SIO terminal input/output control
					EISIO	0	Enable	Mask	Interrupt mask register (serial interface)
0EDH	0	0	IP0	IK0	0 *3	– *2	–	–	Unused
					0 *3	– *2	–	–	Unused
	R				IP0 *4	0	Yes	No	Interrupt factor flag (P0)
					IK0 *4	0	Yes	No	Interrupt factor flag (K00–K03)
0F6H	P03	P02	P01	P00	P03	– *2	High	Low	P0 I/O port data
					P02	– *2	High	Low	
	R/W				P01	– *2	High	Low	
					P00	– *2	High	Low	
0FCH	0	0	PLON	IOC	0 *3	– *2	–	–	Unused
					0 *3	– *2	–	–	Unused
	R		R/W		PLON	0	On	Off	I/O port pull-up control
					IOC	0	Output	Input	I/O port I/O control

*1 Initial value at initial reset
*2 Not set in the circuit
*3 Always "0" being read
*4 Reset (0) immediately after being read

P00–P03: I/O port data (0F6H)

I/O port data can be read and output data can be written through these registers.

• ***Writing***

When "1" is written: High level
When "0" is written: Low level

When the I/O port is set to the output mode, the written data is output from the I/O port terminal unchanged. When "1" is written as the port data, the port terminal goes high (V_{DD}), and when "0" is written, the level goes low (V_{SS}). Port data can also be written in the input mode.

• ***Reading***

When "1" is read: High level
When "0" is read: Low level

The terminal voltage level of the I/O port is read. When the I/O port is in the input mode the voltage level being input to the port terminal can be read; in the output mode the output voltage level can be read. When the terminal voltage is high (V_{DD}) the port data read is "1", and when the terminal voltage is low (V_{SS}) the data is "0".
When "1" is written to the PLON register, the built-in pull-up resistors go on and the I/O port terminals are pulled up.

Note:
- *When the I/O port is set to the output mode and a low-impedance load is connected to the port terminal, the data written to the register may differ from the data read.*
- *When the I/O port is set to the input mode and the input level changed from low (V_{SS}) to high (V_{DD}) through the built-in pull-up resistor, an erroneous input results if the time constant of the capacitive load of the input line and the built-in pull-up resistor is greater than the read-out time. When the input data is being read, the time that the input line is pulled up is equivalent to 0.5 cycles of the CPU system clock. Hence, the electric potential of the terminals must settle within 0.5 cycles. If this condition cannot be met, some measure must be devised, such as arranging a pull-up resistor externally, or performing multiple read-outs.*

IOC: I/O control register (0FCH D0)

The input or output mode can be set with this register.

When "1" is written: Output mode
When "0" is written: Input mode
Reading: Valid

When "1" is written to the I/O control register, the I/O ports enter the output mode, and when "0" is written, the I/O ports enter the input mode (except for the ports that are set as the serial interface ports or input only).
At initial reset, this register is set to "0".

PLON: Pull-up control register (0FCH D1)

Controls the pull-up on/off.

When "1" is written: Pull-up ON
When "0" is written: Pull-up OFF
Reading: Valid

Turns the pull-up resistors built into the I/O ports on and off. (The pull-up resistor is supplemented to the ports selected by mask option.)
When "1" is written to the PLON register, the I/O ports are pulled up.
This control is invalid when the I/O ports are set in the output mode (IOC = "1"). In the output mode, the pull-up resistor is turned off even if the PLON register is set to "1".
At initial reset, this register is set to "0".
The pull-up resistor of the input-only port is always turned on regardless of the PLON setting.

EIP0: Interrupt mask register (0E9H D2)

Sets the mask for the input interrupt.

When "1" is written: Enabled
When "0" is written: Masked
Reading: Valid

Enables or masks the input interrupt of the input-only port set by mask option.
At initial reset, this register is set to "0".

IP0: Interrupt factor flag (0EDH D1)

This flag indicates the occurrence of an input interrupt.

When "1" is read: Interrupt has occurred
When "0" is read: Interrupt has not occurred
Writing: Invalid

IP0 is the interrupt factor flag corresponding to the input-only port input interrupt, and is set to "1" at the falling edge of the signal input to the port that has been selected by mask option.
From the status of this flag, the software can decide whether an input interrupt has occurred.
This flag is reset when the software has read it.
Reading of interrupt factor flag is available at EI, but be careful in the following cases.
If the interrupt mask register value corresponding to the interrupt factor flag to be read is set to "1", an interrupt request will be generated by the interrupt factor flag set timing, or an interrupt request will not be generated. Be very careful when interrupt factor flags are in the same address.
At initial reset, this flag is set to "0".

4.5.7 Programming notes

(1) When the I/O port is set to the output mode and a low-impedance load is connected to the port terminal, the data written to the register may differ from the data read.

(2) When the I/O port is set to the input mode and the input level changed from low (V_{SS}) to high (V_{DD}) through the built-in pull-up resistor, an erroneous input results if the time constant of the capacitive load of the input line and the built-in pull-up resistor is greater than the read-out time. When the input data is being read, the time that the input line is pulled up is equivalent to 0.5 cycles of the CPU system clock. Hence, the electric potential of the terminals must settle within 0.5 cycles. If this condition cannot be met, some measure must be devised, such as arranging a pull-up resistor externally, or performing multiple read-outs.

(3) Reading of interrupt factor flag is available at EI, but be careful in the following cases.
If the interrupt mask register value corresponding to the interrupt factor flag to be read is set to "1", an interrupt request will be generated by the interrupt factor flag set timing, or an interrupt request will not be generated. Be very careful when interrupt factor flags are in the same address.

4.6 LCD Driver

4.6.1 Configuration of LCD driver

The E0C623B Series has four common terminals (COM0–COM3) and 26 segment terminals (SEG0–SEG25), so that an LCD with a maximum of 104 (26 × 4) segments can be driven.
When using the QFP12-48pin package, only 18 segment terminals (SEG0–4, 6, 8–19) are available and up to 72 (18 × 4) segments can be driven.
The driving method is 1/4 duty (1/3 or 1/2 duty can also be selected by mask option) dynamic drive, adopting the four types of potential, V_{SS}, V_{C1}, V_{C2} and V_{C3}.
The power for driving the LCD is generated by the internal circuit so that there is no need to apply power especially from outside.
The LCD drive voltage can also be supplied from outside by selecting mask option ($V_{DD} = V_{C1}$, $V_{DD} = V_{C2}$ or $V_{DD} = V_{C3}$).
When using the internal LCD drive voltage (V_{C1} to V_{C3}), the LCD power supply circuit goes off in the SLEEP mode (E0C62A3B and the CR oscillator model of the E0C623B) and V_{C1} to V_{C3} voltages go to V_{SS} level.

Note: When the LCD drive voltage is supplied externally, the SLEEP function cannot be used.

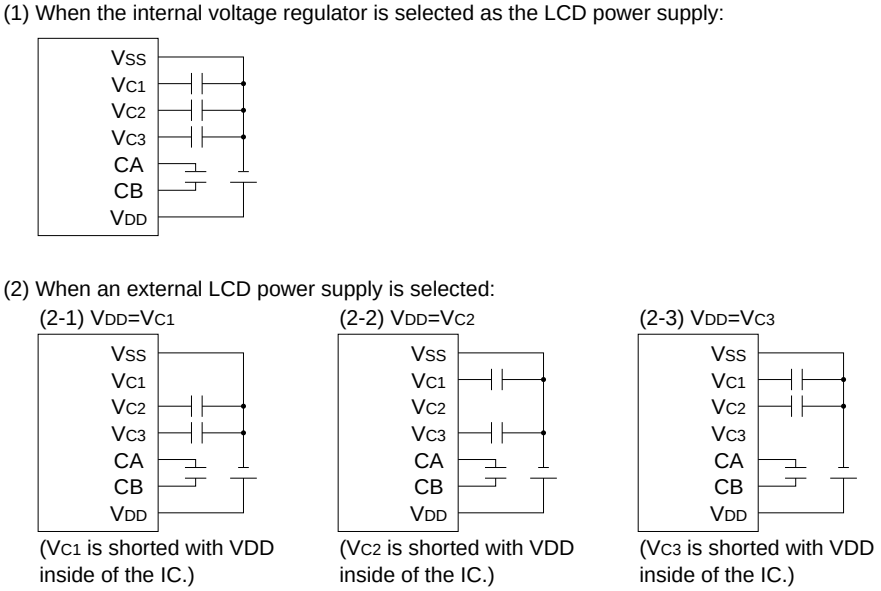


Fig. 4.6.1.1 External connection diagram

The frame frequency is set as shown in Table 4.6.1.1 according to the oscillation frequency.

Table 4.6.1.1 Frame frequency

Model	Oscillation frequency	FR frequency (Hz)		
		1/4 duty	1/3 duty	1/2 duty
E0C623B	32.768 kHz (crystal)	fosc/1024=32	fosc/768=42.7	fosc/1024=32
	65 kHz (CR)	fosc/1024≈64	fosc/768≈85	fosc/1024≈64
E0C62A3B	250 kHz–500 kHz (CR)	fosc/6144	fosc/4608	fosc/6144
	400 kHz–1 MHz (ceramic)	fosc/12288	fosc/9216	fosc/12288

fosc: Oscillation frequency

Figures 4.6.1.2 to 4.6.1.4 show the drive waveform for 1/4 duty, 1/3 duty and 1/2 duty.

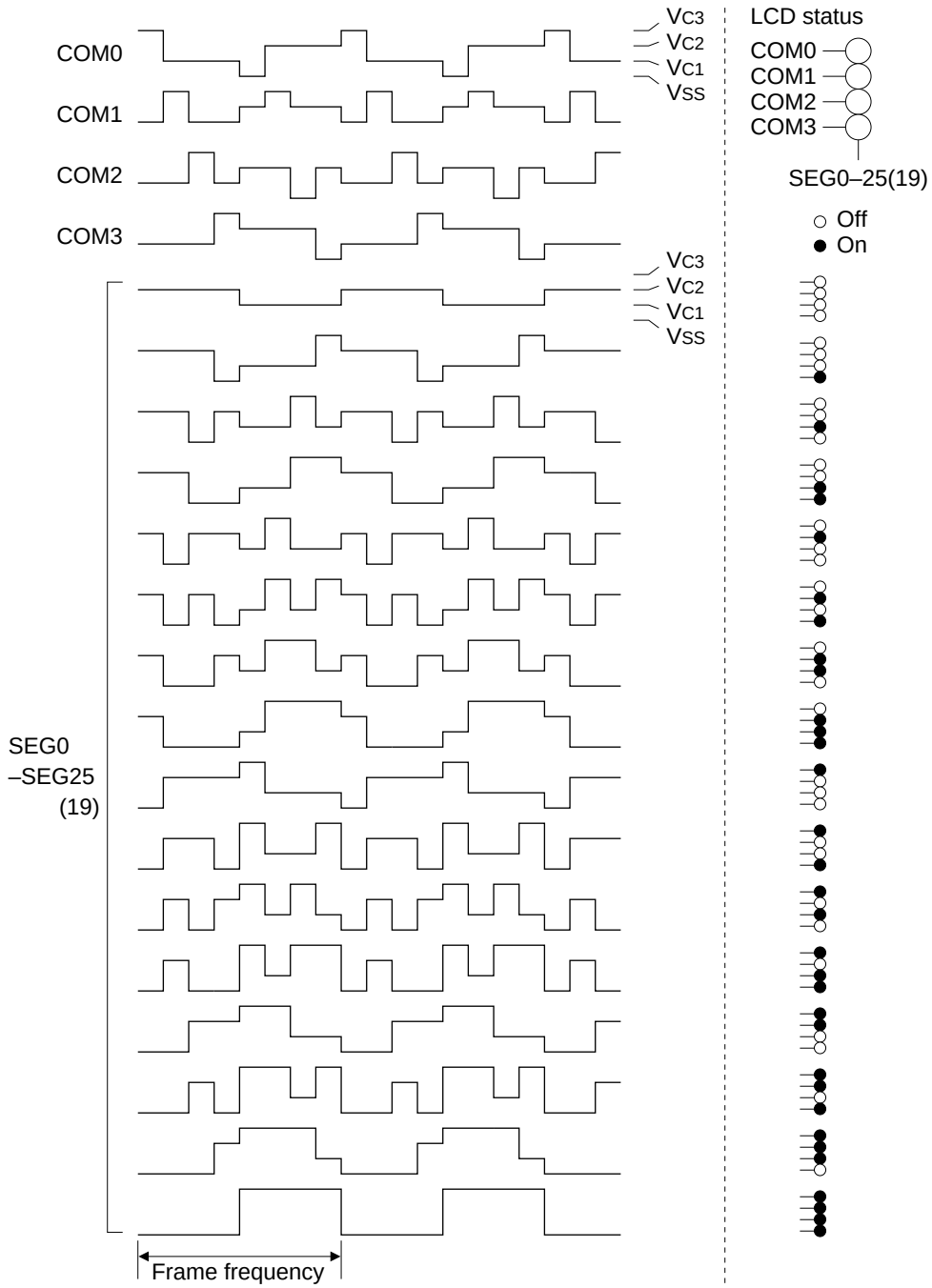


Fig. 4.6.1.2 Drive waveform for 1/4 duty

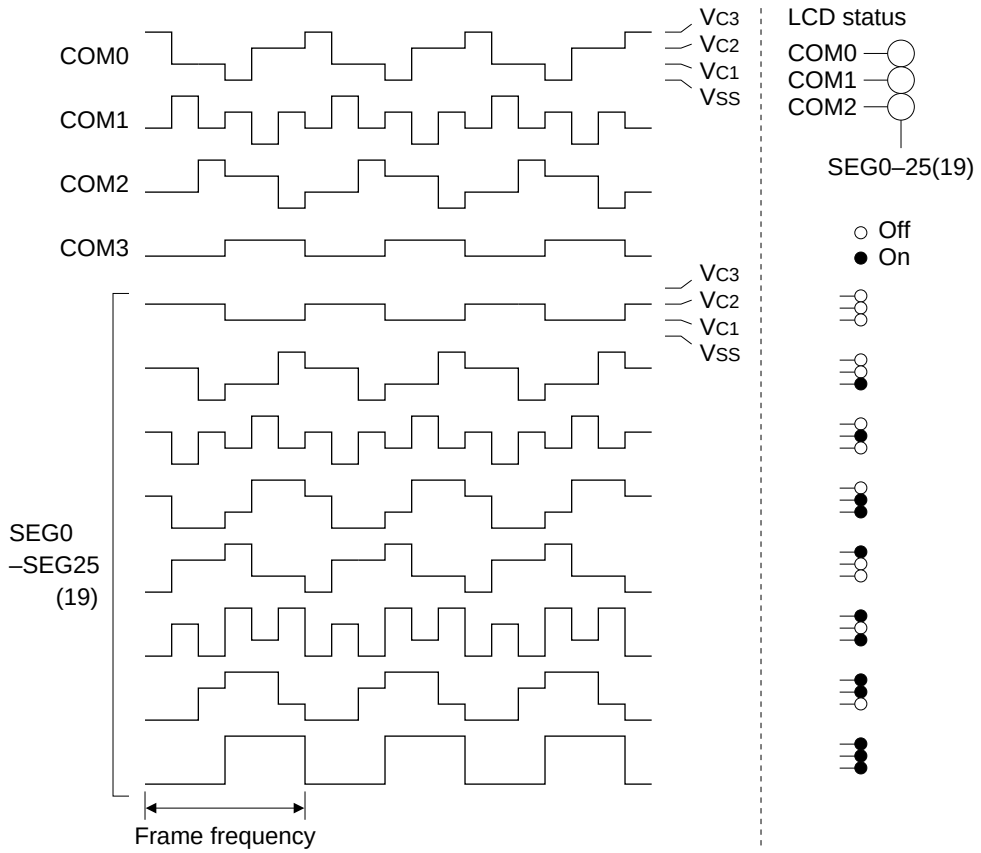


Fig. 4.6.1.3 Drive waveform for 1/3 duty

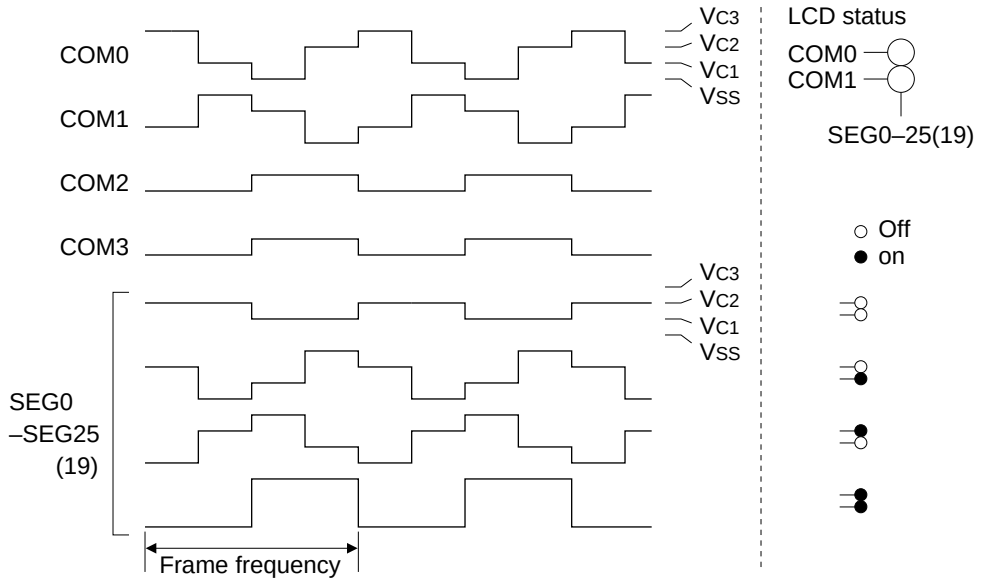


Fig. 4.6.1.4 Drive waveform for 1/2 duty

4.6.2 Switching between dynamic and static drive

The E0C623B Series allows software setting of the LCD static drive.
The procedure for executing of the LCD static drive is as follows:

① Write "1" to the CSDC register at address "0FBH D3".

② Write the same value to the display memory corresponding to COM0–COM3.

Note: Even when l/3 duty is selected, the display data corresponding to COM3 is valid for static drive. Hence, for static drive, set the same value to all display memory corresponding COM0–COM3.

Figure 4.6.2.1 shows the drive waveform for static drive.

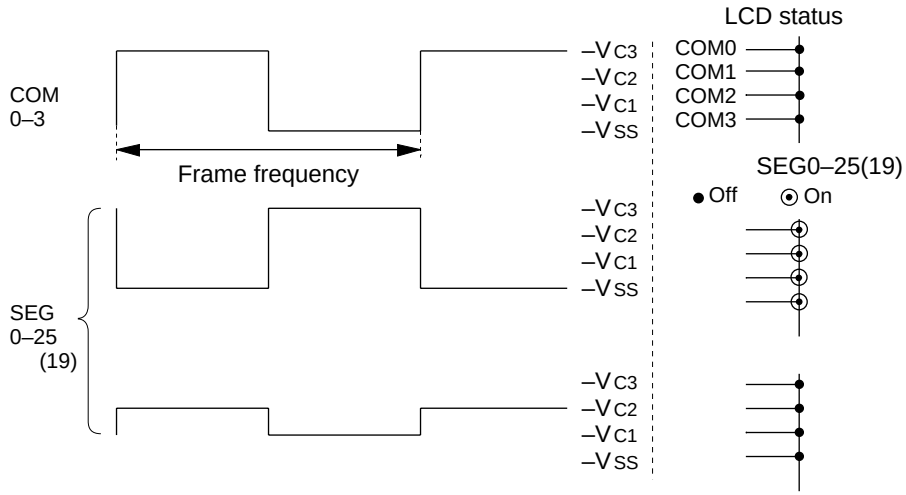


Fig. 4.6.2.1 LCD static drive waveform

4.6.3 Display control

The ALLOFF register is provided to turn all the LCD dots off. At initial reset, the ALLOFF register is set to "1" and the LCD display goes off because the contents of the display memory are undefined. To start display, write "0" to the ALLOFF register after writing display data to the display memory. In the LCD all-off status, the OFF waveform shown in Figure 4.6.2.1 is output.

Similarly, the ALLON register is also provided to turn all the LCD dots on. This register allows the software to control blinking in the display. In the LCD all-on status, the ON waveform shown in Figure 4.6.2.1 is output.

These controls do not affect display memory data.

4.6.4 Mask option

(1) Segment allocation

The segment data is decided by the display data written to the display memory at address "090H–0AFH".

The addresses and bits of the display memory can be made to correspond to the segment terminals (SEG0–SEG25/19) in any combination by mask option. This simplifies design by increasing the degree of freedom with which the liquid crystal panel can be designed.

Figure 4.6.4.1 shows an example of the relationship between the LCD segments (on the panel) and the display memory in the case of 1/3 duty.

Address	Data			
	D3	D2	D1	D0
09AH	d	c	b	a
09BH	p	g	f	e
09CH	d'	c'	b'	a'
09DH	p'	g'	f'	e'

Display memory allocation

	Common 0	Common 1	Common 2
SEG10	9A, D0 (a)	9B, D1 (f)	9B, D0 (e)
SEG11	9A, D1 (b)	9B, D2 (g)	9A, D3 (d)
SEG12	9D, D1 (f')	9A, D2 (c)	9B, D3 (p)

Pin address allocation

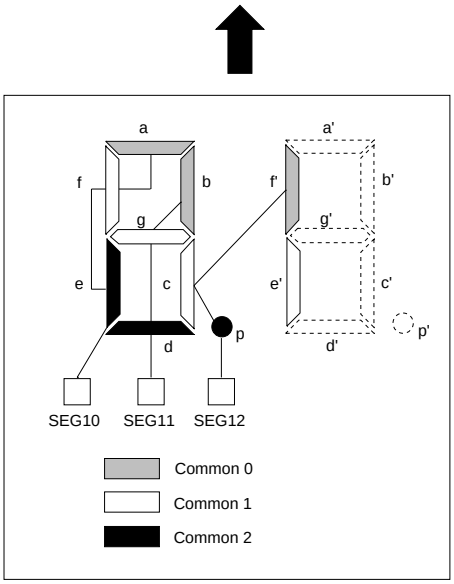


Fig. 4.6.4.1 Segment allocation

(2) Drive duty

Either 1/4, 1/3 or 1/2 duty can be selected as the LCD drive duty.

(3) Output specification

① The segment terminals (SEG0–SEG25/19) are selected by mask option in pairs for either segment signal output or DC output (V_{DD} and V_{SS} binary output). When DC output is selected, the data corresponding to COM0 of each segment terminal is output.
At initial reset, the display memory corresponding to the DC output terminals are set to "1" and the display memory corresponding to the segment output terminals are undefined.

② When DC output is selected, either complementary output or Nch open drain output can be selected for each terminal by mask option.

*Note: The terminal pairs are the combination of SEG (2*n) and SEG (2*n + 1) (where n is an integer from 0 to 12).*

4.6.5 Control of LCD driver

Table 4.6.5.1 shows the control bits of the LCD driver and their addresses. Figure 4.6.5.1 shows the display memory map.

Table 4.6.5.1 I/O memory (LCD driver)

Address	Register								Comment
	D3	D2	D1	D0	Name	Init *1	1	0	
0FBH	CSDC	ALLOFF	ALLON	0	CSDC	0	Static	Dynamic	LCD drive mode switch
					ALLOFF	1	All Off	Normal	LCD all-off control
	R/W			R	ALLON	0	All On	Normal	LCD all-on control
					0 *3	– *2	–	–	Unused

*1 Initial value at initial reset
*2 Not set in the circuit
*3 Always "0" being read
*4 Reset (0) immediately after being read

Address	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
090	Display memory (W only) 32 words × 4 bits															
0A0																

Fig. 4.6.5.1 Display memory map

CSDC: LCD drive switch (0FBH D3)

Selects the LCD drive method.

When "1" is written: Static drive
When "0" is written: Dynamic drive
Reading: Valid

At initial reset, this register is set to "0".

ALLOFF: LCD all OFF control register (0FBH D2)

Fade outs the all LCD segments.

When "1" is written: All LCD segments fade out
When "0" is written: Normal display
Reading: Valid

By writing "1" to the ALLOFF register, all the LCD segments goes off, and when "0" is written, it returns to normal display. This function does not affect the contents of the display memory.
At initial reset, this register is set to "1".

ALLON: LCD all ON control register (0FBH D1)

Displays the all LCD segments on.

When "1" is written: All LCD segments displayed
When "0" is written: Normal display
Reading: Valid

By writing "1" to the ALLON register, all the LCD segments goes on, and when "0" is written, it returns to normal display. This function does not affect the contents of the display memory.
At initial reset, this register is set to "0".

Display memory (090H–0AFH)

The LCD segments are turned on or off according to this data.

When "1" is written: On
When "0" is written: Off
Reading: Invalid

By writing data into the display memory allocated to the LCD segment (on the panel), the segment can be turned on or off.
At initial reset, the contents of the display memory are undefined. The display memory corresponding to the DC output terminals are set to "1".

4.6.6 Programming notes

(1) Because the display memory is for writing only, re-writing the contents with logical instructions (e.g., AND, OR, etc.) which come with read-out operations is not possible. To perform bit operations, a buffer to hold the display data is required on the RAM.

(2) Even when 1/3 duty is selected, the display data corresponding to COM3 is valid for static drive. Hence, for static drive set the same value to all display memory corresponding COM0–COM3.

4.7 Clock Timer

4.7.1 Configuration of clock timer

The E0C623B Series has a built-in clock timer that uses the oscillation circuit as the clock source. The clock timer is configured as a 7-bit binary counter that counts with a 256 Hz source clock from the divider. The high-order 4 bits of the counter (16 Hz–2 Hz) can be read by the software.
Figure 4.7.1.1 is the block diagram of the clock timer.

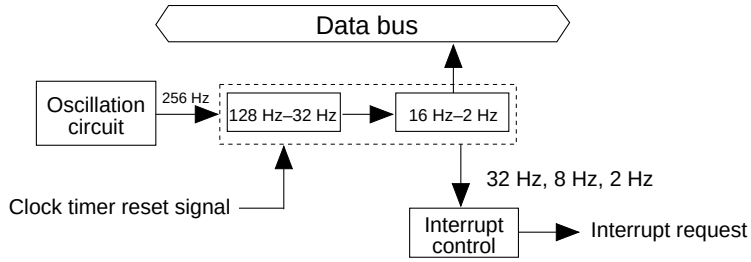


Fig. 4.7.1.1 Block diagram of clock timer

Normally, this clock timer is used for all kinds of timing purpose, such as clocks.

Note: This manual describes frequencies and times when the crystal oscillation circuit (32.768 kHz) of the E0C623B has been selected. Be aware that the frequencies and times vary when the E0C623B CR oscillator model or the E0C62A3B is used.
See Section 4.2.6, "Frequency divider", for the input clock.

4.7.2 Interrupt function

The clock timer can generate interrupts at the falling edge of the 32 Hz, 8 Hz, and 2 Hz signals. The software can mask any of these interrupt signals.
Figure 4.7.2.1 is the timing chart of the clock timer.

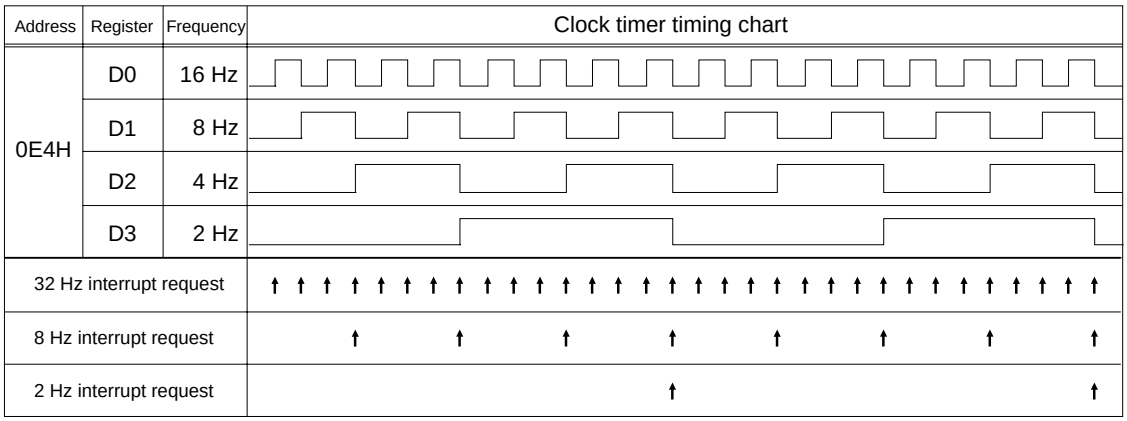


Fig. 4.7.2.1 Timing chart of the clock timer

As shown in Figure 4.7.2.1, an interrupt is generated at the falling edge of the 32 Hz, 8 Hz, and 2 Hz signals. At this point, the corresponding interrupt factor flag (IT32, IT8, IT2) is set to "1". The interrupts can be masked individually with the interrupt mask register (EIT32, EIT8, EIT2). However, regardless of the interrupt mask register setting, the interrupt factor flags will be set to "1" at the falling edge of their corresponding signal (e.g. the falling edge of the 2 Hz signal sets the 2 Hz interrupt factor flag to "1").

4.7.3 Control of clock timer

Table 4.7.3.1 shows the clock timer control bits and their addresses.

Table 4.7.3.1 I/O memory (Clock timer)

Address	Register								Comment
	D3	D2	D1	D0	Name	Init *1	1	0	
0E4H	TM3	TM2	TM1	TM0	TM3	0			Clock timer data (2 Hz)
					TM2	0			Clock timer data (4 Hz)
	R				TM1	0			Clock timer data (8 Hz)
					TM0	0			Clock timer data (16 Hz)
0EBH	0	EIT2	EIT8	EIT32	0 *3	– *2	–	–	Unused
					EIT2	0	Enable	Mask	Interrupt mask register (clock timer 2 Hz)
	R	R/W			EIT8	0	Enable	Mask	Interrupt mask register (clock timer 8 Hz)
					EIT32	0	Enable	Mask	Interrupt mask register (clock timer 32 Hz)
0EFH	0	IT2	IT8	IT32	0 *3	– *2	–	–	Unused
					IT2 *4	0	Yes	No	Interrupt factor flag (clock timer 2 Hz)
	R				IT8 *4	0	Yes	No	Interrupt factor flag (clock timer 8 Hz)
					IT32 *4	0	Yes	No	Interrupt factor flag (clock timer 32 Hz)
0F9H	0	TMRST	SWRUN	SWRST	0 *3	– *2	–	–	Unused
					TMRST*3	Reset	Reset	–	Clock timer reset
	R	W	R/W	W	SWRUN	0	Run	Stop	Stopwatch timer Run/Stop
					SWRST*3	Reset	Reset	–	Stopwatch timer reset

*1 Initial value at initial reset
*2 Not set in the circuit
*3 Always "0" being read
*4 Reset (0) immediately after being read

TM0–TM3: Timer data (0E4H)

The l6 Hz to 2 Hz timer data of the clock timer can be read from this register. These four bits are read-only, and write operations are invalid.
At initial reset, the timer data is initialized to "0H".

EIT32, EIT8, EIT2: Interrupt mask registers (0EBH D0–D2)

These registers are used to mask the clock timer interrupt.

When "1" is written: Enabled
When "0" is written: Masked
Reading: Valid

The interrupt mask registers (EIT32, EIT8, EIT2) mask the corresponding interrupt frequencies (32 Hz, 8 Hz, 2 Hz).
At initial reset, these registers are all set to "0".

IT32, IT8, IT2: Interrupt factor flags (0EFH D0–D2)

These flags indicate the status of the clock timer interrupt.

When "1" is read: Interrupt has occurred
When "0" is read: Interrupt has not occurred
Writing: Invalid

The interrupt factor flags (IT32, IT8, IT2) correspond to the clock timer interrupts (32 Hz, 8 Hz, 2 Hz). The software can determine from these flags whether there is a clock timer interrupt. However, even if the interrupt is masked, the flags are set to "1" at the falling edge of the signal. These flags can be reset when the register is read by the software.
Reading of interrupt factor flags is available at EI, but be careful in the following cases.
If the interrupt mask register value corresponding to the interrupt factor flag to be read is set to "1", an interrupt request will be generated by the interrupt factor flag set timing, or an interrupt request will not be generated. Be very careful when interrupt factor flags are in the same address.
At initial reset, these flags are all set to "0".

TMRST: Clock timer reset (0F9H D2)

This bit resets the clock timer.

When "1" is written: Clock timer reset
When "0" is written: No operation
Reading: Always "0"

The clock timer is reset by writing "1" to TMRST. The clock timer starts immediately after this. No operation results when "0" is written to TMRST.
This bit is write-only, and so is always "0" when read.

4.7.4 Programming notes

(1) Note that the frequencies and times differ from the description in this section when the oscillation frequency is not 32.768 kHz.

(2) Reading of interrupt factor flags is available at EI, but be careful in the following cases.
If the interrupt mask register value corresponding to the interrupt factor flag to be read is set to "1", an interrupt request will be generated by the interrupt factor flag set timing, or an interrupt request will not be generated. Be very careful when interrupt factor flags are in the same address.

4.8 Stopwatch Timer

4.8.1 Configuration of stopwatch timer

The E0C623B Series has a built-in 1/100 sec and 1/10 sec stopwatch timer. The stopwatch timer is configured as a two-stage, four-bit BCD timer serving as the clock source for an approximately 100 Hz signal (obtained by approximately dividing the 256 Hz signal output from the divider). Data can be read out four bits at a time by the software.
Figure 4.8.1.1 is the block diagram of the stopwatch timer.

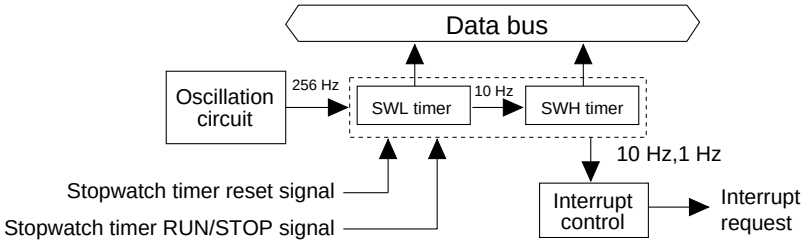


Fig. 4.8.1.1 Block diagram of stopwatch timer

The stopwatch timer can be used separately from the clock timer. In particular, digital stopwatch functions can be easily realized by software.

Note: This manual describes frequencies and times when the crystal oscillation circuit (32.768 kHz) of the E0C623B has been selected. Be aware that the frequencies and times vary when the E0C623B CR oscillator model or the E0C62A3B is used.
See Section 4.2.6, "Frequency divider", for the input clock.

4.8.2 Count-up pattern

The stopwatch timer is configured as two four-bit BCD timers, SWL and SWH. The SWL timer, at the stage preceding the stopwatch timer, has an approximate l00 Hz signal as its input clock. It counts up every 1/100 sec and generates an approximate 10 Hz signal. The SWH timer has an approximate 10 Hz signal generated by the SWL timer for its input clock. It counts up every 1/10 sec and generates a 1 Hz signal.
Figure 4.8.2.1 shows the count-up pattern of the stopwatch timer.

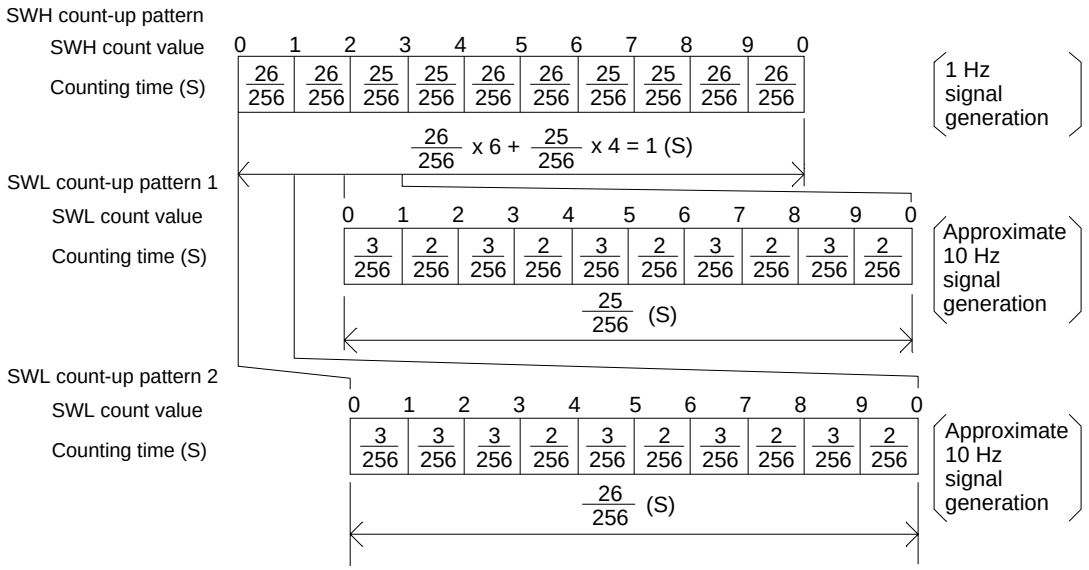


Fig. 4.8.2.1 Count-up pattern of stopwatch timer

SWL generates an approximate 10 Hz signal from the 256 Hz based signal. The count-up intervals are 2/256 sec and 3/256 sec, so that two final patterns are generated: a 25/256 sec interval and a 26/256 sec interval. Consequently, the count-up intervals are 2/256 sec and 3/256 sec, which do not amount to an accurate 1/100 sec. SWH counts the approximate 10 Hz signals generated by the 25/256 sec and 26/256 sec intervals in the ratio of 4:6 to generate a l Hz signal. The count-up intervals are 25/256 sec and 26/256 sec, which do not amount to an accurate 1/10 sec.

4.8.3 Interrupt function

The 10 Hz (approximate 10 Hz) and 1 Hz interrupts can be generated by the overflow of the SWL and SWH stopwatch timers, respectively. Also, software can separately mask the frequencies as described earlier.
Figure 4.8.3.1 is the timing chart for the stopwatch timer.

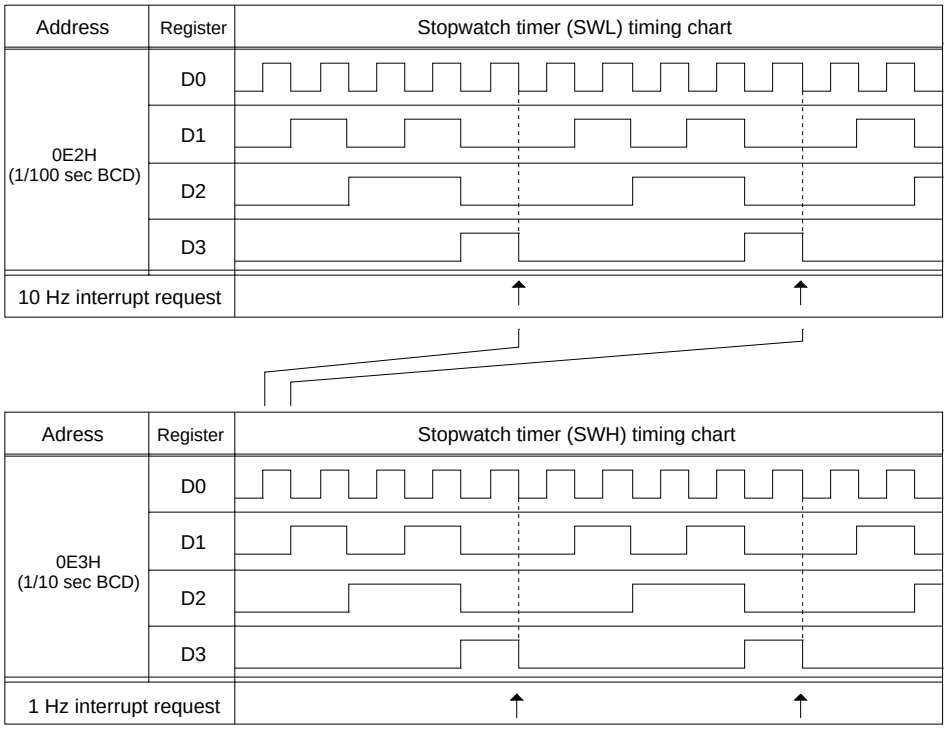


Fig. 4.8.3.1 Timing chart for stopwatch timer

As shown in Figure 4.8.3.1, the interrupts are generated by the overflow of the respective timers ("9" changing to "0"). Also at this point, the corresponding interrupt factor flags (ISW0, ISW1) are set to "1". The respective interrupts can be masked separately with the interrupt mask registers (EISW0, EISW1). However, regardless of the setting of the interrupt mask registers, the interrupt factor flags are set to "1" by the overflow of the corresponding timers.

4.8.4 Control of stopwatch timer

Table 4.8.4.1 shows the stopwatch timer control bits and their addresses.

Table 4.8.4.1 I/O memory (Stopwatch timer)

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
0E2H	SWL3	SWL2	SWL1	SWL0	SWL3	0			MSB
					SWL2	0			Stopwatch timer data
	R				SWL1	0			1/100sec (BCD)
					SWL0	0			LSB
0E3H	SWH3	SWH2	SWH1	SWH0	SWH3	0			MSB
					SWH2	0			Stopwatch timer data
	R				SWH1	0			1/10sec (BCD)
					SWH0	0			LSB
0EAH	0	0	EISW1	EISW0	0 *3	– *2	–	–	Unused
					0 *3	– *2	–	–	Unused
	R		R/W		EISW1	0	Enable	Mask	Interrupt mask register (stopwatch 1 Hz)
					EISW0	0	Enable	Mask	Interrupt mask register (stopwatch 10 Hz)
0EEH	0	0	ISW1	ISW0	0 *3	– *2	–	–	Unused
					0 *3	– *2	–	–	Unused
	R				ISW1 *4	– *2	Yes	No	Interrupt factor flag (stopwatch 1 Hz)
					ISW0 *4	0	Yes	No	Interrupt factor flag (stopwatch 10 Hz)
0F9H	0	TMRST	SWRUN	SWRST	0 *3	– *2	–	–	Unused
					TMRST*3	Reset	Reset	–	Clock timer reset
	R	W	R/W	W	SWRUN	0	Run	Stop	Stopwatch timer Run/Stop
					SWRST*3	Reset	Reset	–	Stopwatch timer reset

*1 Initial value at initial reset
*2 Not set in the circuit
*3 Always "0" being read
*4 Reset (0) immediately after being read

SWL0–SWL3: 1/100 sec stopwatch timer (0E2H)

Data (BCD) of the 1/100 sec column of the stopwatch timer can be read. These four bits are read-only, and cannot be written.
At initial reset, the timer data is set to "0H".

SWH0–SWH3: 1/10 sec stopwatch timer (0E3H)

Data (BCD) of the 1/10 sec column of the stopwatch timer can be read. These four bits are read-only, and cannot be written.
At initial reset, the timer data is set to "0H".

EISW0, EISW1: Interrupt mask registers (0EAH D0 and D1)

These registers mask the stopwatch timer interrupt.

When "1" is written: Enabled
When "0" is written: Masked
Reading: Valid

The interrupt mask registers (EISW0, EISW1) are used to mask the 10 Hz and 1 Hz interrupts, respectively.
At initial reset, these registers are both set to "0".

ISW0, ISW1: Interrupt factor flags (0EEH D0 and D1)

These flags indicate the status of the stopwatch timer interrupt.

When "1" is read: Interrupt has occurred
When "0" is read: Interrupt has not occurred
Writing: Invalid

The interrupt factor flags (ISW0, ISW1) correspond to the 10 Hz and 1 Hz interrupts, respectively. With these flags, the software can determine whether a stopwatch timer interrupt has occurred. However, regardless of the interrupt mask register setting, these flags are set to "1" by the timer overflow.
They are reset by reading with the software.
Reading of interrupt factor flags are available at EI, but be careful in the following cases.
If the interrupt mask register value corresponding to the interrupt factor flag to be read is set to "1", an interrupt request will be generated by the interrupt factor flag set timing, or an interrupt request will not be generated. Be very careful when interrupt factor flags are in the same address.
At initial reset, these flags are set to "0".

SWRST: Stopwatch timer reset (0F9H D0)

This bit resets the stopwatch timer.

When "1" is written: Stopwatch timer reset
When "0" is written: No operation
Reading: Always "0"

The stopwatch timer is reset when "1" is written to SWRST. When the stopwatch timer is reset while running, operation restarts immediately. Also, while stopped, the reset data is maintained.
This bit is write-only, and is always "0" when read.

SWRUN: Stopwatch timer run/stop (0F9H D1)

This bit controls run/stop of the stopwatch timer.

When "1" is written: Run
When "0" is written: Stop
Reading: Valid

The stopwatch timer runs when "1" is written to SWRUN, and stops when "0" is written.
When stopped, the timer data is maintained until the timer next Run or is reset. Also, when the timer runs after being stopped, the data that was maintained can be used to resume the count.
If the timer data is read while running, a correct read may be impossible because of the carry from the low-order bit (SWL) to the high-order bit (SWH). This occurs if reading has extended over the SWL and SWH bits when the carry occurs. To prevent this, read after stopping, and then continue running. Also, the stopped duration must be within 976 μsec (256 Hz, 1/4 cycle).
At initial reset, this register is set to "0".

4.8.5 Programming notes

(1) Note that the frequencies and times differ from the description in this section when the oscillation frequency is not 32.768 kHz.

(2) If the timer data is read while running, a correct read may be impossible because of the carry from the low-order bit (SWL) to the high-order bit (SWH). This occurs if reading has extended over the SWL and SWH bits when the carry occurs. To prevent this, read after stopping, and then continue running. Also, the stopped duration must be within 976 μsec (256 Hz, 1/4 cycle).

(3) Reading of interrupt factor flags are available at EI, but be careful in the following cases.
If the interrupt mask register value corresponding to the interrupt factor flag to be read is set to "1", an interrupt request will be generated by the interrupt factor flag set timing, or an interrupt request will not be generated. Be very careful when interrupt factor flags are in the same address.

4.9 Serial Interface

4.9.1 Configuration of serial interface

The E0C623B Series has a built-in 8-bit synchronous clock type serial interface.
The configuration of the serial interface is shown in Figure 4.9.1.1.
The serial input/output ports SIN, SOUT, $\overline{SCLK}$ and $\overline{SRDY}$ are common used with the I/O ports P00, P01, P02 and P03. The port (terminal) configuration can be selected by mask option. The serial input and output can also be shared using the P00 terminal as the SIO terminal.
The CPU, via the 8-bit shift register, can read the serial input data from the SIN/SIO terminal. Moreover, via the same 8-bit shift register, it can convert parallel data into serial data and output it to the SOUT/SIO terminal.
The synchronous clock for serial data input/output can be selected by software any one of 2 types of master mode (internal clock mode: when the E0C623B Series is to be the master for serial input/output) and a type of slave mode (external clock mode: when the E0C623B Series is to be the slave for serial input/output).

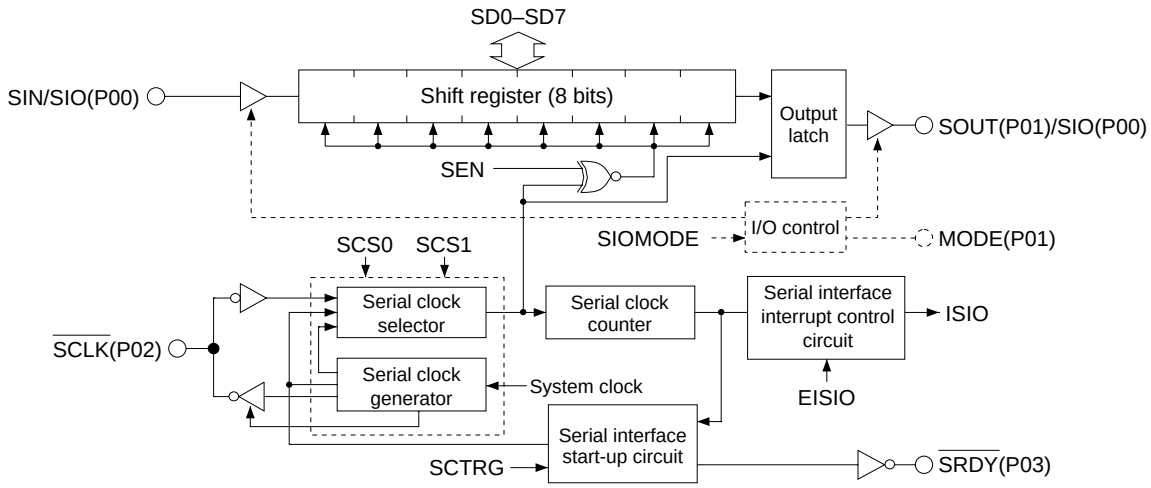


Fig. 4.9.1.1 Configuration of serial interface

4.9.2 Mask option

The following mask options are provided for the serial interface.

(1) Terminal configuration

The input/output terminals of the serial interface are shared with the I/O port terminals P00–P03. The terminal configuration can be selected from 14 types shown in Table 4.9.2.1 according to the serial input/output specification.

Table 4.9.2.1 Terminal configuration of serial interface

No.	P00	P01	P02	P03	No.	P00	P01	P02	P03
1	I/O	I/O	I/O	I/O	8	SIO	MODE	$\overline{\text{SCLK}}$	$\overline{\text{SRDY}}$
2	I/O	I/O	I/O	I	9	SIO	MODE	$\overline{\text{SCLK}}$	I/O
3	SIN	SOUT	$\overline{\text{SCLK}}$	$\overline{\text{SRDY}}$	10	SIO	MODE	$\overline{\text{SCLK}}$	I
4	SIN	SOUT	$\overline{\text{SCLK}}$	I/O	11	SIO	I/O	$\overline{\text{SCLK}}$	$\overline{\text{SRDY}}$
5	SIN	SOUT	$\overline{\text{SCLK}}$	I	12	SIO	I	$\overline{\text{SCLK}}$	$\overline{\text{SRDY}}$
6	SIN	I/O	$\overline{\text{SCLK}}$	I/O	13	SIO	I/O	$\overline{\text{SCLK}}$	I/O
7	SIN	I/O	$\overline{\text{SCLK}}$	I	14	SIO	I/O	$\overline{\text{SCLK}}$	I

SIN: Serial data input terminal. The P00 terminal is set as the SIN terminal when the serial interface is used.

SOUT: Serial data output terminal. The SOUT terminal can be omitted when only the serial input function is used.

SIO: Serial data I/O terminal. The P00 terminal can be set to this shared terminal.

$\overline{\text{SCLK}}$: Synchronous clock I/O terminal. It functions as the internal clock output terminal in the master mode and the input terminal of the clock from the external serial device in the slave mode.

$\overline{\text{SRDY}}$: Ready signal output terminal. This terminal outputs the signal indicating that the serial interface is in ready status when used in the slave mode. It is not necessary to select the $\overline{\text{SRDY}}$ terminal when using the serial interface in the master mode.

MODE: I/O status output terminal. It can be selected when using the P00 terminal as the SIO terminal. When SIO is selected, the input/output direction is set by the SIOMODE register. The MODE terminal outputs the signal indicating the direction, thus the signal can be used for direction control of the serial data line.

I/O: General-purpose I/O port terminal. See Section 4.5, "I/O port", for details.

I: General-purpose input terminal. The input interrupt function is available by mask option. See Section 4.5, "I/O port", for details.

(2) Pull-up resistor

The pull-up resistor can be added to the terminal used for input (SIN/SIO, $\overline{\text{SCLK}}$ in the slave mode). When "pull-up disabled" is selected, take care that floating status does not occur. Normally select "pull-up enabled".

(3) Output specifications

For the output terminals (SOUT/SIO, $\overline{\text{SCLK}}$ in the master mode, $\overline{\text{SRDY}}$ in the slave mode), either complementary output or Nch open drain output can be selected as the output specification. However, even when Nch open drain output is selected, a voltage exceeding the power voltage must not be supplied to the terminal.

(4) Data input/output permutation

Either LSB first or MSB first can be selected as the input/output permutation of serial data.

4.9.3 Master mode and slave mode

The serial interface of the E0C623B Series has two types of operation mode: master mode and slave mode. In the master mode, it uses an internal clock as the synchronous clock of the built-in shift register and outputs this internal clock to the $\overline{SCLK}$ terminal to control the external (slave side) serial interface.
In the slave mode, the synchronous clock output from the external (master side) serial device is input from the $\overline{SCLK}$ terminal and is used as the synchronous clock to the built-in shift register. Furthermore the $\overline{SRDY}$ signal that indicates whether the serial interface is in ready status or not is output from the $\overline{SRDY}$ terminal (when the $\overline{SRDY}$ terminal is set).
The master mode or slave mode is selected using the SCS0 and SCS1 registers; when the master mode is selected, a synchronous clock may be selected from among 2 types as shown in Table 4.9.3.1.

Table 4.9.3.1 Synchronous clock selection

SCS1	SCS0	Mode	Synchronous clock
1	1	Master mode	CLK/2
1	0	Master mode	CLK
0	1	–	–
0	0	Slave mode	External clock

CLK: CPU system clock fosc
CLK/2: CLK divided by 2

At initial reset, the slave mode (external clock mode) is selected.
Moreover, the synchronous clock, along with the input/output of the 8 bits serial data, is controlled as follows:

- In the master mode, after output of 8 clocks from the $\overline{SCLK}$ terminal, clock output is automatically suspended.
- In the slave mode, after input of 8 clocks to the $\overline{SCLK}$ terminal, subsequent clock inputs are masked.

4.9.4 Data input/output and interrupt function

The serial interface of the E0C623B Series can input/output data via the internal 8-bit shift register. The shift register operates by synchronizing with either the synchronous clock output from $\overline{SCLK}$ terminal (master mode), or the synchronous clock input to $\overline{SCLK}$ terminal (slave mode).
The serial interface generates interrupt on completion of the 8-bit serial daata input/output. Detection of serial data input/output is done by the counting of the synchronous clock ($\overline{SCLK}$); the clock completes input/output operation when 8 counts (equivalent to 8 cycles) have been made and then generates interrupt.
The serial data input/output procedure data is explained below:

(1) Serial data output procedure

The E0C623B Series serial interface is capable of outputting parallel data as serial data, in units of 8 bits.
By setting the parallel data to data registers SD0–SD3 (0E5H) and SD4–SD7 (0E6H) individually and writing "1" to SCTRG (0E7H D3), it synchronizes with the synchronous clock and serial data is output at the SOUT/SIO terminal.
When the P00 terminal is used as SIO, it is necessary to set the serial interface to the output mode by writing "1" to the SIOMODE register (0E9H D1) before transmitting. In the output mode, the MODE terminal goes high level (when the MODE terminal has been set). This control is not necessary when the P01 terminal is used as SOUT.
The synchronous clock used here is as follows: in the master mode, internal clock which is output to the $\overline{SCLK}$ terminal while in the slave mode, external clock which is input from the $\overline{SCLK}$ terminal.
The serial data output from the SOUT/SIO terminal changes at the rising edge of the synchronous clock.
When the output of the 8-bit data from SD0 to SD7 is completed, the interrupt factor flag ISIO is set to "1" and interrupt is generated. Moreover, the interrupt can be masked by the interrupt mask register EISIO. Note, however, that regardless of the setting of the interrupt mask register, the interrupt factor flag is set to "1" after output of the 8-bit data.

(2) Serial data input procedure

The E0C623B Series serial interface is capable of inputting serial data as parallel data, in units of 8 bits.
By writing "1" to SCTRG, the serial data is input from the SIN/SIO terminal, synchronizes with the synchronous clock, and is sequentially read in the 8-bit shift register.
When the P00 terminal is used as SIO, it is necessary to set the serial interface to the input mode by writing "0" to the SIOMODE register before receiving. In the output mode, the MODE terminal goes low level (when the MODE terminal has been set). This control is not necessary when the P01 terminal is used as SOUT.
As in the above item (1), the synchronous clock used here is as follows: in the master mode, internal clock which is output to the $\overline{SCLK}$ terminal while in the slave mode, external clock which is input from the $\overline{SCLK}$ terminal.
The serial data is read to the built-in shift register at the falling edge of the synchronous clock when SEN bit is "1" and is read at the rising edge of the synchronous clock when SEN bit is "0". Moreover, the shift register is sequentially shifted as the data is fetched.

When the input of the 8-bit data from SD0 to SD7 is completed, the interrupt factor flag ISIO is set to "1" and interrupt is generated. Moreover, the interrupt can be masked by the interrupt mask register EISIO. Note, however, that regardless of the setting of the interrupt mask register, the interrupt factor flag is set to "1" after input of the 8 bits data.

The data in the shift register can be read from data registers SD0–SD7 by software.

(3) Serial data input/output permutation

E0C623B Series allows the input/output permutation of serial data to be selected by mask option as to either LSB first or MSB first. The block diagram showing input/output permutation in case of LSB first and MSB first is provided in Figure 4.9.4.1.

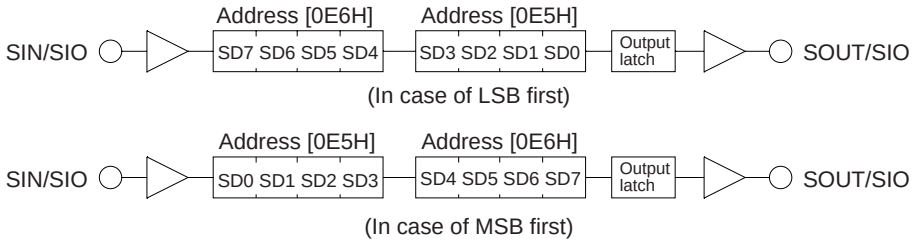


Fig. 4.9.4.1 Serial data input/output permutation

(4) $\overline{\text{SRDY}}$ signal

When the serial interface is used in the slave mode (external clock mode), $\overline{\text{SRDY}}$ is used to indicate whether the serial interface is available to transmit or receive data for the master side (external) serial device. The $\overline{\text{SRDY}}$ signal is output from the $\overline{\text{SRDY}}$ terminal (when the $\overline{\text{SRDY}}$ terminal is selected by mask option).

The $\overline{\text{SRDY}}$ signal goes to "0" (low) when the serial interface becomes available to transmit or receive data; normally, it is at "1" (high).

The $\overline{\text{SRDY}}$ signal changes from "1" to "0" immediately after "1" is written to SCTRG and returns from "0" to "1" when "0" is input to the $\overline{\text{SCLK}}$ terminal (i.e., when the serial input/output begins transmitting or receiving data). Moreover, when data is read from or written to SD4–SD7, the $\overline{\text{SRDY}}$ signal returns to "1".

(5) Timing chart

The serial interface timing chart is shown in Figure 4.9.4.2.

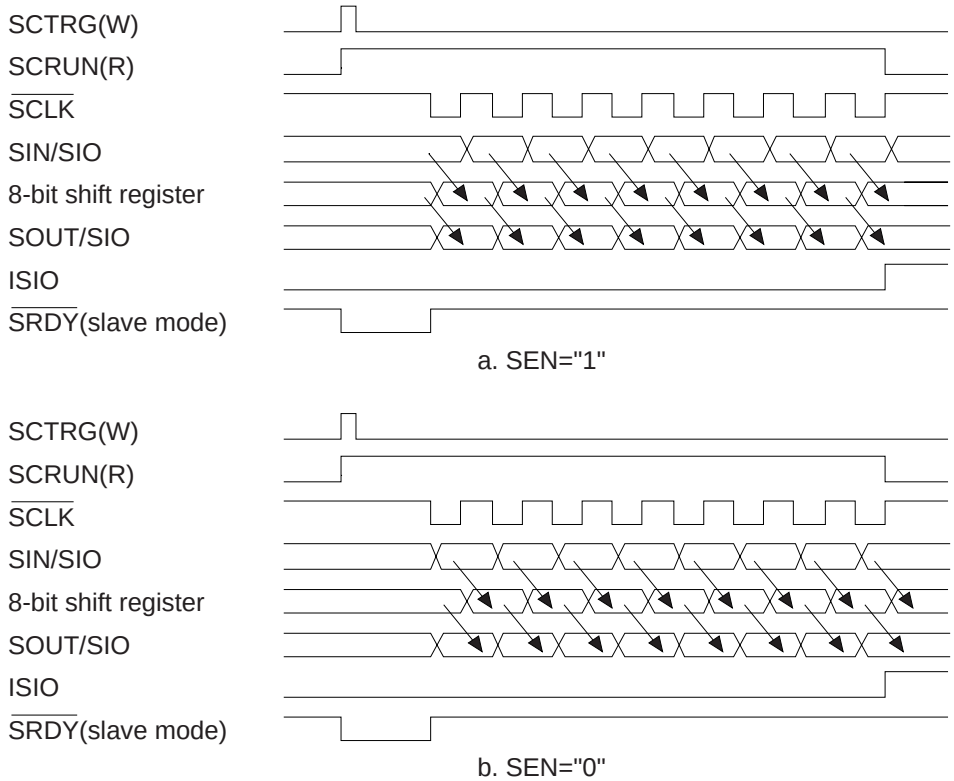


Fig. 4.9.4.2 Serial interface timing chart

4.9.5 Control of serial interface

Table 4.9.5.1 shows the serial interface control bits and their addresses.

Table 4.9.5.1 I/O memory (Serial interface)

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
0E5H	SD3	SD2	SD1	SD0	SD3	– *2	High	Low	Serial interface data register (low-order 4 bits) LSB
					SD2	– *2	High	Low	
	R/W				SD1	– *2	High	Low	
					SD0	– *2	High	Low	
0E6H	SD7	SD6	SD5	SD4	SD7	– *2	High	Low	MSB Serial interface data register (high-order 4 bits)
					SD6	– *2	High	Low	
	R/W				SD5	– *2	High	Low	
					SD4	– *2	High	Low	
0E7H	SCTRG / SCRUN	SEN	SCS1	SCS0	SCTRG	– *2	Trigger	–	Serial interface trigger (writing)
					SCRUN	– *2	Run	Stop	Serial interface status (reading)
					SEN	0	↓	↑	Serial interface clock edge selection
	W / R	R/W			SCS1	0			Serial interface clock mode selection
					SCS0	0			0: Slave, 2: Master (CLK), 3: Master (CLK/2)
0E9H	0	EIP0	SIOMODE	EISIO	0 *3	– *2	–	–	Unused
					EIP0	0	Enable	Mask	Interrupt mask register (P0)
	R	R/W			SIOMODE	0	Output	Input	SIO terminal input/output control
					EISIO	0	Enable	Mask	Interrupt mask register (serial interface)
0ECH	0	0	0	ISIO	0 *3	– *2	–	–	Unused
					0 *3	– *2	–	–	Unused
	R				0 *3	– *2	–	–	Unused
					ISIO *4	0	Yes	No	Interrupt factor flag (serial interface)

*1 Initial value at initial reset
*2 Not set in the circuit
*3 Always "0" being read
*4 Reset (0) immediately after being read

SD0–SD3, SD4–SD7: Serial interface data registers (0E5H, 0E6H)

These are the data registers of the serial interface.

• ***Writing***

When "1" is written: High level
When "0" is written: Low level

Write serial data will be output to SOUT/SIO terminal. From the SOUT/SIO terminal, the data converted into serial data as high (V_{DD}) level bit for bits set at "1" and as low (V_{SS}) level bit for bits set at "0".
Perform data writing only while the serial interface is standby status (i.e., the synchronous clock is neither being input or output).
At initial reset, these registers will be undefined.

• ***Reading***

When "1" is read: High level
When "0" is read: Low level

The serial data input from the SOUT/SIO terminal can be read by this register.
The data converted into parallel data, as high (V_{DD}) level bit "1" and as low (V_{SS}) level bit "0" input from SOUT/SIO terminal. Perform data reading only while the serial interface is standby status (i.e., the synchronous clock is neither being input or output).
At initial reset, these registers will be undefined.

SCS1, SCS0: Synchronous clock selection (0E7H D1 and D0)

Selects the synchronous clock for the serial interface ($\overline{SCLK}$).

Table 4.9.5.2 Synchronous clock selection

SCS1	SCS0	Mode	Synchronous clock
1	1	Master mode	CLK/2
1	0	Master mode	CLK
0	1	–	–
0	0	Slave mode	External clock

Synchronous clock ($\overline{SCLK}$) is selected from among the above 3 types: 2 types of internal clock and an external clock.
At initial reset, external clock is selected.

SEN: Clock edge selection (0E7H D2)

Selects the timing for reading in the serial data input.

When "1" is written: Falling edge of $\overline{SCLK}$
When "0" is written: Rising edge of $\overline{SCLK}$
Reading: Valid

Selects whether the fetching for the serial input data to the registers (SD0–SD7) at the falling edge (at "1" writing) or rising edge (at "0" writing) of the $\overline{SCLK}$ signal.
The input data fetching timing may be selected but output timing for output data is fixed at $\overline{SCLK}$ falling edge.
At initial reset, rising edge of $\overline{SCLK}$ (SEN = "0") is selected.

SIOMODE: SIO terminal input/output control (0E9H D1)

Controls the I/O direction of the serial data line (P00).

When "1" is written: Output mode
When "0" is written: Input mode
Reading: Valid

The SIOMODE register is used to control the serial data direction when the P00 terminal is shared with input and output as SIO. When "1" is written to the SIOMODE register, the serial interface is set to the output mode and the SIO terminal becomes the serial data output terminal. When "0" is written, the serial interface is set to the input mode and the SIO terminal becomes the serial data input terminal. The content of the SIOMODE register is output to outside the IC via the MODE terminal (when the MODE terminal has been set).
This control is not necessary when the SIN and SOUT terminals are provided separately.
At initial reset, input mode (SIOMODE = "0") is selected.

SCTRG, SCRUN: Clock trigger, Clock Run/Stop monitor (0E7H D3)

This is a trigger to start input/output of synchronous clock.

When "1" is written: Trigger
When "0" is written: No operation
Reading: Valid

When this trigger is supplied to the serial interface activating circuit, the synchronous clock ($\overline{SCLK}$) input/output is started.
As a trigger condition, it is required that data writing or reading on data registers SD0–SD7 be performed prior to writing "1" to SCTRG. (The internal circuit of the serial interface is initiated through data writing/reading on data registers SD0–SD7.)
Supply trigger only once every time the serial interface is placed in the RUN state.
Moreover, when the synchronous clock $\overline{SCLK}$ is external clock, start to input the external clock after the trigger.

When read out this bit, it indicates the status of serial interface clock.
After "1" is written in SCTRG, this value is latched till serial interface clock stops (8 clock counts). So during this period, reading this bit SCRUN causes "1". Other time it is "0".

EISIO: Interrupt mask register (0E9H D0)

This is the interrupt mask register of the serial interface.

When "1" is written: Enabled
When "0" is written: Masked
Reading: Valid

With interrupt mask register (EISIO), masking of the serial interface interrupt can be selected.
At initial reset, this register is set to "0" (mask).

ISIO: Interrupt factor flag (0ECH D0)

This is the interrupt factor flag of the serial interface.

When "1" is read: Interrupt has occurred
When "0" is read: Interrupt has not occurred
Writing: Invalid

From the status of this flag, the software can decide whether the serial interface interrupt has been occurred or not. Note, however, that even if the interrupt is masked, this flag will be set to "1" after the 8 bits data input/output.
This flag is reset by reading with software.
Reading of interrupt factor flag is available at EI, but be careful in the following cases.
If the interrupt mask register value corresponding to the interrupt factor flag to be read is set to "1", an interrupt request will be generated by the interrupt factor flag set timing, or an interrupt request will not be generated.
At initial reset, this flag is set to "0".

4.9.6 Programming notes

(1) Perform data writing/reading to data registers SD0–SD7 only while the serial interface is standby status (i.e., the synchronous clock is neither being input or output).

(2) As a trigger condition, it is required that data writing or reading on data registers SD0–SD7 be performed prior to writing "1" to SCTRG. (The internal circuit of the serial interface is initiated through data writing/reading on data registers SD0–SD7.) Supply trigger only once every time the serial interface is placed in the RUN state. Moreover, when the synchronous clock $\overline{\text{SCLK}}$ is external clock, start to input the external clock after the trigger.

(3) Reading of interrupt factor flag is available at EI, but be careful in the following cases.
If the interrupt mask register value corresponding to the interrupt factor flag to be read is set to "1", an interrupt request will be generated by the interrupt factor flag set timing, or an interrupt request will not be generated.

4.10 Heavy Load Protection Circuit (E0C623B)

4.10.1 Heavy load protection function

The E0C623B has a heavy load protection function for when the battery load becomes heavy and the source voltage changes, such as when an external buzzer sounds or an external lamp lights. The state where the heavy load protection function is in effect is called the heavy load protection mode. Compared with the normal operation mode, the IC can operate in low voltage.
The heavy load protection function allows the E0C623B to operate with 0.8 V supply voltage.
This function is not available in the E0C62A3B.

The normal mode changes to the heavy load protection mode in the following case:

- When the software changes the mode to the heavy load protection mode (HLMOD = "1")

In the heavy load protection mode, the internal regulated voltage for the internal circuits is generated from the LCD system booster voltage V_{C2}. Consequently, more current is consumed in the heavy load protection mode than in the normal mode. Unless it is necessary, be careful not to set the heavy load protection mode with the software.
At initial reset, the E0C623B is set in the heavy load protection mode to be certain oscillation starts. Return to the normal mode by writing "0" to the HLMOD register after stabilizing oscillation.

4.10.2 Control of heavy load protection circuit

Table 4.10.2.1 shows the heavy load protection circuit control bit and the address.

Table 4.10.2.1 I/O memory (Heavy load protection circuit)

Address	Register								Comment
	D3	D2	D1	D0	Name	Init *1	1	0	
0FAH	HLMOD	0	0	0	HLMOD	1	Heavy	Normal	Heavy load protection mode (E0C623B)
					HLMOD	0	–	–	Fixed at "0" in the E0C62A3B
	R/W	R			0 *3	– *2	–	–	Unused
					0 *3	– *2	–	–	Unused
					0 *3	– *2	–	–	Unused

*1 Initial value at initial reset
*2 Not set in the circuit
*3 Always "0" being read
*4 Reset (0) immediately after being read

HLMOD: Heavy load protection mode on/off (0FAH D3)

Controls the heavy load protection mode.

When "1" is written: Heavy load protection mode on
When "0" is written: Heavy load protection mode off
Reading: Valid

When HLMOD is set to "1", the E0C623B enters the heavy load protection mode.
In the heavy load protection mode, the consumed current becomes larger. Unless necessary, do not select the heavy load protection mode with the software.
The heavy load protection function is not available in the E0C62A3B.
At initial reset, this register is set to "1" (heavy load protection mode) in the E0C623B, and "0" in the E0C62A3B.

4.10.3 Programming note

In the heavy load protection mode, the consumed current becomes larger. Unless necessary, do not select the heavy load protection mode with the software.

4.11 Interrupt and HALT/SLEEP

The E0C623B Series provides the following interrupt settings, each of which is maskable.

External interrupt: Input port interrupt (one)
I/O port interrupt (one) - available when "input-only" is selected by mask option
Internal interrupt: Timer interrupt (three)
Stopwatch interrupt (two)
Serial interface interrupt (one)

To enable interrupts, the interrupt flag must be set to "1" (EI) and the necessary related interrupt mask registers must be set to "1" (enable). When an interrupt occurs, the interrupt flag is automatically reset to "0" (DI) and interrupts after that are inhibited.
Figure 4.11.1 shows the configuration of the interrupt circuit.

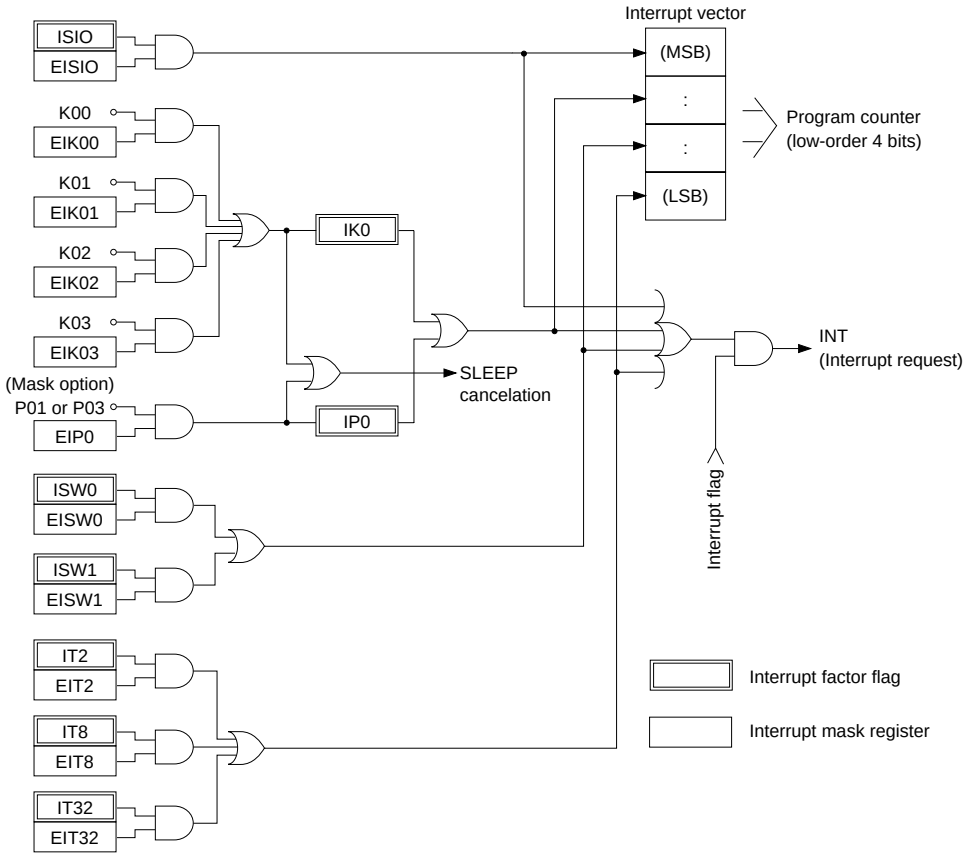


Fig. 4.11.1 Configuration of interrupt circuit

HALT mode

When the HALT instruction is executed, the CPU stops operating and enters the HALT mode. The oscillation circuit and the peripheral circuits operate in the HALT mode. By an interrupt, the CPU exits the HALT mode and resumes operating.

SLEEP mode (E0C623B CR oscillator model, E0C62A3B)

The SLEEP function can be selected in the E0C623B CR oscillator model and the E0C62A3B by mask option. When the SLEEP function has been selected, executing the SLP instruction sets the IC in the SLEEP mode and stops operation of the CPU, oscillation circuit and LCD power supply circuit. The SLEEP mode will be canceled by an input interrupt request from the input port or the I/O port selected by mask option.

4.11.1 Interrupt factors

Table 4.11.1.1 shows the factors that generate interrupt requests.

The interrupt factor flags are set to "1" depending on the corresponding interrupt factors.
The CPU is interrupted when the following two conditions occur and an interrupt factor flag is set to "1".

- The corresponding mask register is "1" (enabled)
- The interrupt flag is "1" (EI)

The interrupt factor flag is a read-only register, but can be reset to "0" when the register data is read.
At initial reset, the interrupt factor flags are reset to "0".

Note: Reading of interrupt factor flag is available at EI, but be careful in the following cases.
If the interrupt mask register value corresponding to the interrupt factor flag to be read is set to "1", an interrupt request will be generated by the interrupt factor flag set timing, or an interrupt request will not be generated. Be very careful when interrupt factor flags are in the same address.

Table 4.11.1.1 Interrupt factors

Interrupt factor	Interrupt factor flag	
Clock timer 2 Hz falling edge	IT2	(0EFH D2)
Clock timer 8 Hz falling edge	IT8	(0EFH D1)
Clock timer 32 Hz falling edge	IT32	(0EFH D0)
Stopwatch timer 1 Hz falling edge	ISW1	(0EEH D1)
Stopwatch timer 10 Hz falling edge	ISW0	(0EEH D0)
I/O (P) port falling edge	IP0	(0EDH D1)
Input (K) port falling edge	IK0	(0EDH D0)
Serial I/F data transfer completion	ISIO	(0ECH D0)

4.11.2 Specific masks for interrupt

The interrupt factor flags can be masked by the corresponding interrupt mask registers. The interrupt mask registers are read/write registers. The interrupts are enabled when "1" is written to them, and masked (interrupt disabled) when "0" is written to them.
At initial reset, the interrupt mask register is set to "0".
Table 4.11.2.1 shows the correspondence between interrupt mask registers and interrupt factor flags.

Table 4.11.2.1 Interrupt mask registers and interrupt factor flags

Interrupt mask register		Interrupt factor flag	
EIT2	(0EBH D2)	IT2	(0EFH D2)
EIT8	(0EBH D1)	IT8	(0EFH D1)
EIT32	(0EBH D0)	IT32	(0EFH D0)
EISW1	(0EAH D1)	ISW1	(0EEH D1)
EISW0	(0EAH D0)	ISW0	(0EEH D0)
EIP0	(0E9H D2)	IP0	(0EDH D1)
EIK03*	(0E8H D3)	IK0	(0EDH D0)
EIK02*	(0E8H D2)		
EIK01*	(0E8H D1)		
EIK00*	(0E8H D0)		
ISIO	(0E9H D0)	ISIO	(0ECH D0)

∗ There is an interrupt mask register for each input port terminal.

4.11.3 Interrupt vectors

When an interrupt request is input to the CPU, the CPU starts interrupt processing. After the program being executed is suspended, interrupt processing is executed in the following order:

① The address data (value of the program counter) of the program step to be executed next is saved on the stack (RAM).

② The interrupt request causes the value of the interrupt vector (page 1, 01H–08H) to be loaded into the program counter.

③ The program at the specified address is executed (execution of interrupt processing routine).

Note: The processing in steps 1 and 2, above, takes 12 cycles of the CPU system clock.

Table 4.11.3.1 Interrupt vector addresses

Page	Step	Interrupt vector
1	00H	Initial reset
	01H	Clock timer interrupt
	02H	Stopwatch timer interrupt
	03H	Clock timer + Stopwatch timer interrupt
	04H	Input (K00–K03, P0n) interrupt
	05H	Input + Clock timer interrupt
	06H	Input + Stopwatch timer interrupt
	07H	Input + Clock timer + Stopwatch timer interrupt
	08H	Serial interface interrupt

4.11.4 Control of interrupt

Tables 4.11.4.1 show the interrupt control bits and their addresses.

Table 4.11.4.1 I/O memory (Interrupt)

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
0E8H	EIK03	EIK02	EIK01	EIK00	EIK03	0	Enable	Mask	Interrupt mask register (K03)
					EIK02	0	Enable	Mask	Interrupt mask register (K02)
	R/W				EIK01	0	Enable	Mask	Interrupt mask register (K01)
					EIK00	0	Enable	Mask	Interrupt mask register (K00)
0E9H	0	EIP0	SIOMODE	EISIO	0 *3	– *2	–	–	Unused
					EIP0	0	Enable	Mask	Interrupt mask register (P0)
	R	R/W			SIOMODE	0	Output	Input	SIO terminal input/output control
					EISIO	0	Enable	Mask	Interrupt mask register (serial interface)
0EAH	0	0	EISW1	EISW0	0 *3	– *2	–	–	Unused
					0 *3	– *2	–	–	Unused
	R		R/W		EISW1	0	Enable	Mask	Interrupt mask register (stopwatch 1 Hz)
					EISW0	0	Enable	Mask	Interrupt mask register (stopwatch 10 Hz)
0EBH	0	EIT2	EIT8	EIT32	0 *3	– *2	–	–	Unused
					EIT2	0	Enable	Mask	Interrupt mask register (clock timer 2 Hz)
	R	R/W			EIT8	0	Enable	Mask	Interrupt mask register (clock timer 8 Hz)
					EIT32	0	Enable	Mask	Interrupt mask register (clock timer 32 Hz)
0ECH	0	0	0	ISIO	0 *3	– *2	–	–	Unused
					0 *3	– *2	–	–	Unused
	R				0 *3	– *2	–	–	Unused
					ISIO *4	0	Yes	No	Interrupt factor flag (serial interface)
0EDH	0	0	IP0	IK0	0 *3	– *2	–	–	Unused
					0 *3	– *2	–	–	Unused
	R				IP0 *4	0	Yes	No	Interrupt factor flag (P0)
					IK0 *4	0	Yes	No	Interrupt factor flag (K00–K03)
0EEH	0	0	ISW1	ISW0	0 *3	– *2	–	–	Unused
					0 *3	– *2	–	–	Unused
	R				ISW1 *4	– *2	Yes	No	Interrupt factor flag (stopwatch 1 Hz)
					ISW0 *4	0	Yes	No	Interrupt factor flag (stopwatch 10 Hz)
0EFH	0	IT2	IT8	IT32	0 *3	– *2	–	–	Unused
					IT2 *4	0	Yes	No	Interrupt factor flag (clock timer 2 Hz)
	R				IT8 *4	0	Yes	No	Interrupt factor flag (clock timer 8 Hz)
					IT32 *4	0	Yes	No	Interrupt factor flag (clock timer 32 Hz)

*1 Initial value at initial reset
*2 Not set in the circuit
*3 Always "0" being read
*4 Reset (0) immediately after being read

EIK00–EIK03: Interrupt mask registers (0E8H)
IK0: Interrupt factor flag (0EDH D0)

...See Section 4.3.4, "Control of input ports".

EIP0: Interrupt mask register (0E9H D2)
IP0: Interrupt factor flag (0EDH D1)

...See Section 4.5.6, "Control of I/O port".

EISIO: Interrupt mask register (0E9H D0)
ISIO: Interrupt factor flag (0ECH D0)

...See Section 4.9.5, "Control of serial interface".

EISW0, EISW1: Interrupt mask registers (0EAH D0 and D1)
ISW0, ISW1: Interrupt factor flags (0EEH D0 and D1)

...See Section 4.8.4, "Control of stopwatch timer".

EIT32, EIT8, EIT2: Interrupt mask registers (0EBH D0–D2)
IT32, IT8, IT2: Interrupt factor flags (0EFH D0–D2)

...See Section 4.7.3, "Control of clock timer".

4.11.5 Programming notes

(1) Restart from the HALT mode is performed by an interrupt. The return address after completion of the interrupt processing will be the address following the HALT instruction.

(2) Restart from the SLEEP mode is performed by an input interrupt from the input port (K00–K03) or the input-only port (P01 or P03 selected by mask option). The return address after completion of the interrupt processing will be the address following the SLP instruction.
The SLEEP function can only be selected in the E0C623B CR oscillator model and the E0C62A3B by mask option. It is not available in the E0C623B crystal oscillator model.

(3) When an interrupt occurs, the interrupt flag will be reset by the hardware and it will become DI status. After completion of the interrupt processing, set to the EI status through the software as needed.
Moreover, the nesting level may be set to be programmable by setting to the EI state at the beginning of the interrupt processing routine.

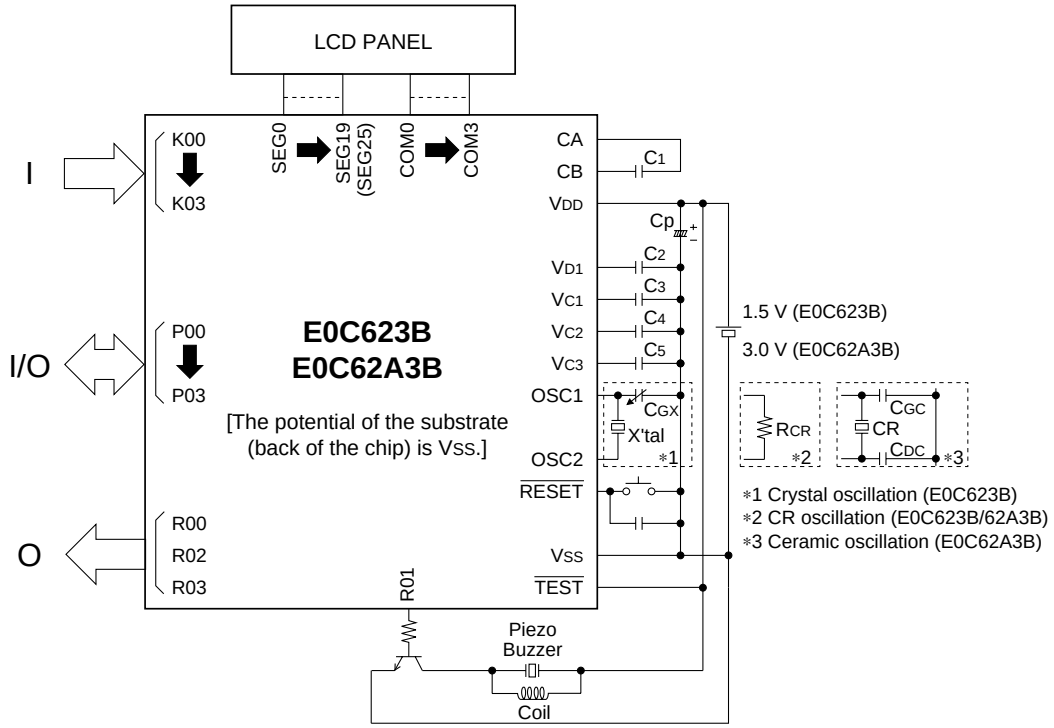
(4) The interrupt factor flags must always be reset before setting the EI status. When the interrupt mask register has been set to "1", the same interrupt will occur again if the EI status is set unless the interrupt factor flag has been reset.

(5) The interrupt factor flag will be reset by reading through the software. Because of this, when multiple interrupt factor flags are to be assigned to the same address, perform the flag check after the contents of the address has been stored in the RAM. Direct checking with the FAN instruction will cause all the interrupt factor flag to be reset.

(6) Reading of interrupt factor flag is available at EI, but be careful in the following cases.
If the interrupt mask register value corresponding to the interrupt factor flag to be read is set to "1", an interrupt request will be generated by the interrupt factor flag set timing, or an interrupt request will not be generated. Be very careful when interrupt factor flags are in the same address.

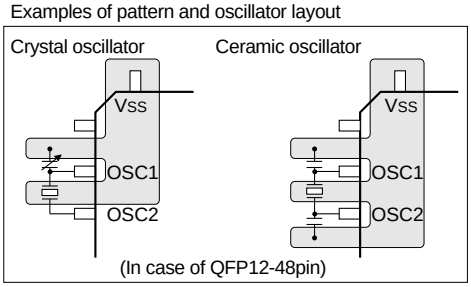
CHAPTER 5 BASIC EXTERNAL WIRING DIAGRAM

(1) Piezo Buzzer Single Terminal Driving
(when "Buzzer OFF level = High" and "LCD internal voltage regurator" are selected)



X'tal	Crystal oscilator	32.768 kHz, C_I (Max.)=35 kΩ
C_{GX}	Trimmer capacitor	5~25pF
R_{CR}	Resistor for CR oscillation	See Section 6.6.
CR	Ceramic oscillator	1 MHz
C_{GC}	Capacitor	100 pF
C_{DC}	Capacitor	100 pF
C_1–C_5	Capacitor	0.1 µF
Cp	Capacitor	3.3 µF

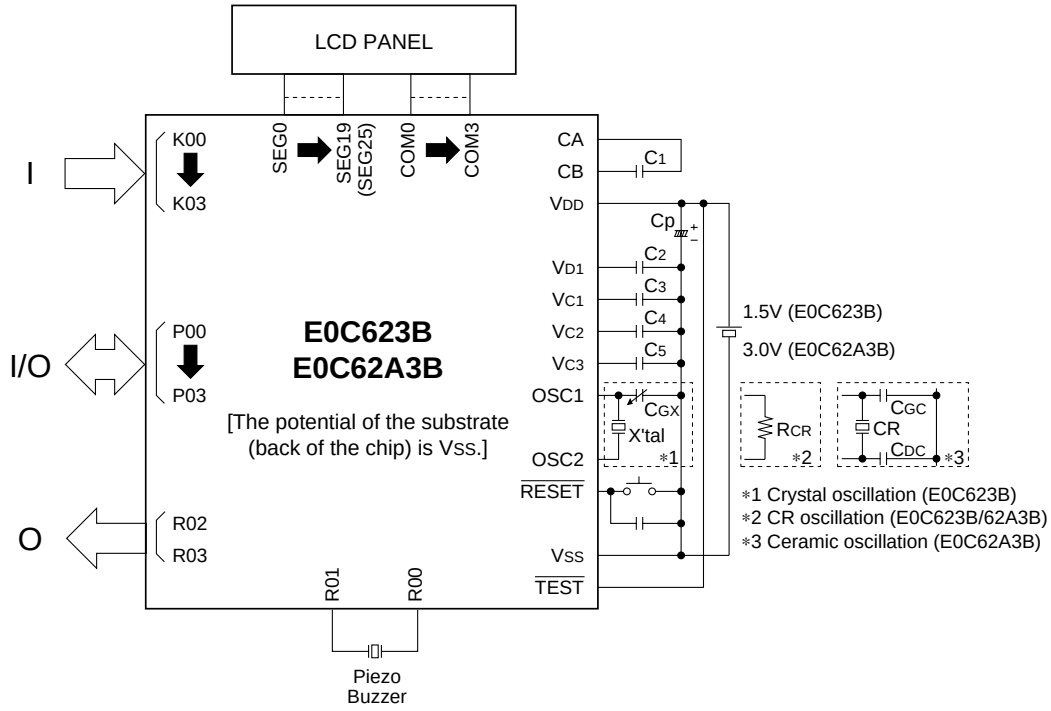
Examples of pattern and oscillator layout



Note: • *The above table is simply an example, and is not guaranteed to work.*

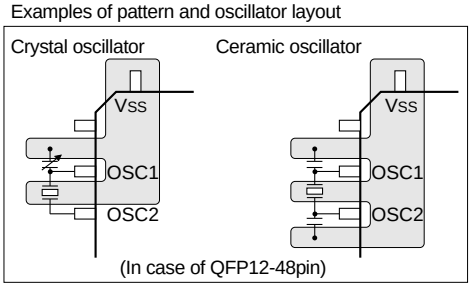
- *When using the crystal oscillation circuit and ceramic oscillation circuit, make a board pattern with noise measure as shown above.*
- *In order to prevent unstable operation of the oscillation circuit due to current leak between OSC1 and V_{DD}, please keep enough distance between V_{DD} and other signals on the board pattern.*
- *Precautions for Visible Radiation*
  Visible radiation causes semiconductor devices to change the electrical characteristics. It may cause this IC to malfunction. When developing products which use this IC, consider the following precautions to prevent malfunctions caused by visible radiations.
  (1) Design the product and implement the IC on the board so that it is shielded from visible radiation in actual use.
  (2) The inspection process of the product needs an environment that shields the IC from visible radiation.
  (3) As well as the face of the IC, shield the back and side too.

(2) Piezo Buzzer Direct Driving
(when "LCD internal voltage regurator" is selected)



X'tal	Crystal oscillator	32.768 kHz, C_I (Max.)=35 kΩ
C_{GX}	Trimmer capacitor	5~25pF
R_{CR}	Resistor for CR oscillation	See Section 6.6.
CR	Ceramic oscillator	1 MHz
C_{GC}	Capacitor	100 pF
C_{DC}	Capacitor	100 pF
C_1–C_5	Capacitor	0.1 µF
Cp	Capacitor	3.3 µF

Examples of pattern and oscillator layout



Note: • *The above table is simply an example, and is not guaranteed to work.*

- *When using the crystal oscillation circuit and ceramic oscillation circuit, make a board pattern with noise measure as shown above.*
- *In order to prevent unstable operation of the oscillation circuit due to current leak between OSC1 and V_{DD}, please keep enough distance between V_{DD} and other signals on the board pattern.*
- *Precautions for Visible Radiation*
  Visible radiation causes semiconductor devices to change the electrical characteristics. It may cause this IC to malfunction. When developing products which use this IC, consider the following precautions to prevent malfunctions caused by visible radiations.
  (1) Design the product and implement the IC on the board so that it is shielded from visible radiation in actual use.
  (2) The inspection process of the product needs an environment that shields the IC from visible radiation.
  (3) As well as the face of the IC, shield the back and side too.

CHAPTER 6 ELECTRICAL CHARACTERISTICS

6.1 Absolute Maximum Rating

(VSS=0V)

Item	Symbol	Rated value	Unit
Supply voltage	VDD	-0.5 to 7.0	V
Input voltage (1)	VI	-0.5 to VDD + 0.3	V
Input voltage (2)	VIOSC	-0.5 to VD1 + 0.3	V
Permissible total output current *1	ΣIVDD	10	mA
Operating temperature	Topr	-20 to 70	°C
Storage temperature	Tstg	-65 to 150	°C
Soldering temperature / time	Tsol	260°C, 10sec (lead section)	–
Permissible dissipation *2	PD	250	mW

*1 The permissible total output current is the sum total of the current (average current) that simultaneously flows from the output pin (or is drawn in).

*2 In case of plastic package (QFP12-48pin).

6.2 Recommended Operating Conditions

(Ta=-20 to 70°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply voltage	VDD	E0C623B (Crystal oscillation)	1.1		3.6	V
		E0C623B (Crystal oscillation + HVLD*1)	0.8		3.6	V
		E0C623B (CR oscillation)	1.1		3.6	V
		E0C623B (CR oscillation + HVLD*1)	0.8		3.6	V
		E0C62A3B (CR oscillation)	1.7		3.6	V
		E0C62A3B (Ceramic oscillation)	1.7		3.6	V
Oscillation frequency	fOSC	E0C623B (Crystal oscillation)	–	32.768	–	kHz
		E0C623B (CR oscillation)	30		80	kHz
		E0C62A3B (CR oscillation)			500	kHz
		E0C62A3B (Ceramic oscillation)			1M	Hz

*1 HVLD = Heavy load protection mode

6.3 DC Characteristics

Unless otherwise specified:
V_{DD}=1.5V, V_{SS}=0V, f_{OSC}=32.768kHz, Ta=25°C, V_{D1}/V_{C1}/V_{C2}/V_{C3} are internal voltage, C_1–C_5=0.1µF

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
High level input voltage (1)	V_{IH1}		K00–03, P00–03	0.8·V_{DD}		V_{DD}	V
High level input voltage (2)	V_{IH2}		$\overline{RESET}$, $\overline{TEST}$	0.9·V_{DD}		V_{DD}	V
Low level input voltage (1)	V_{IL1}		K00–03, P00–03	0		0.1·V_{DD}	V
Low level input voltage (2)	V_{IL2}		$\overline{RESET}$, $\overline{TEST}$	0		0.1·V_{DD}	V
High level input current	I_{IH}	V_{IH}=1.5V	K00–03, P00–03, $\overline{RESET}$, $\overline{TEST}$	0		0.5	µA
Low level input current (1)	I_{IL1}	V_{IL1}=V_{SS} No Pull-up	K00–03, P00–03 $\overline{RESET}$, $\overline{TEST}$	-0.5		0	µA
Low level input current (2)	I_{IL2}	V_{IL2}=V_{SS} With Pull-up	K00–03, P00–03 $\overline{RESET}$, $\overline{TEST}$	-16	-10	-6	µA
High level output current (1)	I_{OH1}	V_{OH1}=0.9·V_{DD}	R00–03, P00–03			-0.3	mA
High level output current (2)	I_{OH2}	V_{OH2}=0.9·V_{DD}	BZ, $\overline{BZ}$, FOUT			-0.3	mA
Low level output current (1)	I_{OL1}	V_{OL1}=0.1·V_{DD}	R00–03, P00–03	0.7			mA
Low level output current (2)	I_{OL2}	V_{OL2}=0.1·V_{DD}	BZ, $\overline{BZ}$, FOUT	0.7			mA
Common output current	I_{OH3}	V_{OH3}=V_{C3}-0.05V	COM0–3			-10	µA
	I_{OL3}	V_{OL3}=V_{SS}+0.05V		10			µA
Segment output current	I_{OH4}	V_{OH4}=V_{C3}-0.05V	SEG0–25			-10	µA
(during LCD output)	I_{OL4}	V_{OL4}=V_{SS}+0.05V		10			µA
Segment output current	I_{OH5}	V_{OH5}=0.9·V_{DD}	SEG0–25			-100	µA
(during DC output)	I_{OL5}	V_{OL5}=0.1·V_{DD}		100			µA

Unless otherwise specified:
V_{DD}=3.0V, V_{SS}=0V, f_{OSC}=32.768kHz, Ta=25°C, V_{D1}/V_{C1}/V_{C2}/V_{C3} are internal voltage, C_1–C_5=0.1µF

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
High level input voltage (1)	V_{IH1}		K00–03, P00–03	0.8·V_{DD}		V_{DD}	V
High level input voltage (2)	V_{IH2}		$\overline{RESET}$, $\overline{TEST}$	0.9·V_{DD}		V_{DD}	V
Low level input voltage (1)	V_{IL1}		K00–03, P00–03	0		0.1·V_{DD}	V
Low level input voltage (2)	V_{IL2}		$\overline{RESET}$, $\overline{TEST}$	0		0.1·V_{DD}	V
High level input current	I_{IH}	V_{IH}=3.0V	K00–03, P00–03, $\overline{RESET}$, $\overline{TEST}$	0		0.5	µA
Low level input current (1)	I_{IL1}	V_{IL1}=V_{SS} No Pull-up	K00–03, P00–03 $\overline{RESET}$, $\overline{TEST}$	-0.5		0	µA
Low level input current (2)	I_{IL2}	V_{IL2}=V_{SS} With Pull-up	K00–03, P00–03 $\overline{RESET}$, $\overline{TEST}$	-32	-20	-12	µA
High level output current (1)	I_{OH1}	V_{OH1}=0.9·V_{DD}	R00–03, P00–03			-1.5	mA
High level output current (2)	I_{OH2}	V_{OH2}=0.9·V_{DD}	BZ, $\overline{BZ}$, FOUT			-1.5	mA
Low level output current (1)	I_{OL1}	V_{OL1}=0.1·V_{DD}	R00–03, P00–03	6			mA
Low level output current (2)	I_{OL2}	V_{OL2}=0.1·V_{DD}	BZ, $\overline{BZ}$, FOUT	6			mA
Common output current	I_{OH3}	V_{OH3}=V_{C3}-0.05V	COM0–3			-10	µA
	I_{OL3}	V_{OL3}=V_{SS}+0.05V		10			µA
Segment output current	I_{OH4}	V_{OH4}=V_{C3}-0.05V	SEG0–25			-10	µA
(during LCD output)	I_{OL4}	V_{OL4}=V_{SS}+0.05V		10			µA
Segment output current	I_{OH5}	V_{OH5}=0.9·V_{DD}	SEG0–25			-300	µA
(during DC output)	I_{OL5}	V_{OL5}=0.1·V_{DD}		300			µA

6.4 Analog Circuit Characteristics and Power Current Consumption

LCD drive voltage

Unless otherwise specified:

V_{DD}=3.0V, V_{SS}=0V, f_{OSC}=32.768kHz, Ta=25°C, V_{D1}/V_{C1}/V_{C2}/V_{C3} are internal voltage, C_1–C_5=0.1µF

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
LCD drive voltage	V_{C1}	Connect 1 MΩ load resistor between V_{SS} and V_{C1} (no panel load)	0.95	1.05	1.15	V
	V_{C2}	Connect 1 MΩ load resistor between V_{SS} and V_{C2} (no panel load)	2·V_{C1} ×0.9		2·V_{C1} +0.1	V
	V_{C3}	Connect 1 MΩ load resistor between V_{SS} and V_{C3} (no panel load)	3·V_{C1} ×0.9		3·V_{C1} +0.1	V

Current consumption

Unless otherwise specified:

V_{DD}=3.0V, V_{SS}=0V, Ta=25°C, V_{D1}/V_{C1}/V_{C2}/V_{C3} are internal voltage, C_1–C_5=0.1µF, No panel load

Item	Symbol		Condition	Min.	Typ.	Max.	Unit
Current consumption	I_{OP}	HALT mode	623B Crystal oscillation (32.768kHz)	–	2.5	5.0	µA
			623B Crystal oscillation (32.768kHz)+HVLD*1	–	6.5	9.0	µA
			623B CR oscillation (40kHz)	–	3.0	6.0	µA
			623B CR oscillation (40kHz)+HVLD*1	–	7.0	10.0	µA
			62A3B CR oscillation (250kHz)	–	55	110	µA
			62A3B Ceramic oscillation (1MHz)	–	80	200	µA
		RUN mode	623B Crystal oscillation (32.768kHz)	–	3.0	6.0	µA
			623B Crystal oscillation (32.768kHz)+HVLD*1	–	7.0	10.0	µA
			623B CR oscillation (40kHz)	–	3.5	7.0	µA
			623B CR oscillation (40kHz)+HVLD*1	–	7.5	11.0	µA
			62A3B CR oscillation (250kHz)	–	60	120	µA
			62A3B Ceramic oscillation (1MHz)	–	100	200	µA
		SLEEP mode	623B CR oscillation	–	–	1.0	µA
			62A3B CR oscillation	–	–	1.0	µA
			62A3B Ceramic oscillation	–	–	1.0	µA

*1 HVLD = Heavy load protection mode

6.5 AC Characteristics

6.5.1 Serial interface

Master mode 1

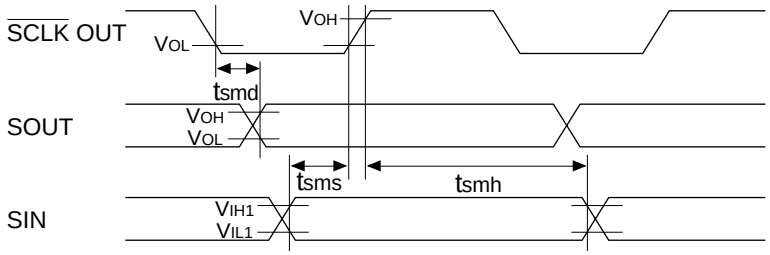
Condition: V_{DD}=1.5V, V_{SS}=0V, fosc=32.768kHz, V_{IH1}=0.8V_{DD}, V_{IL1}=0.2V_{DD}, V_{OH}=0.8V_{DD}, V_{OL}=0.2V_{DD}, Ta=-20 to 70°C

Item	Symbol	Min.	Typ.	Max.	Unit
Transmit data output delay time	tsmd	–	–	5	µS
Receive data input set-up time	tsms	10	–	–	µS
Receive data input hold time	tsmh	5	–	–	µS

Master mode 2

Condition: V_{DD}=3.0V, V_{SS}=0V, fosc=1MHz, V_{IH1}=0.8V_{DD}, V_{IL1}=0.2V_{DD}, V_{OH}=0.8V_{DD}, V_{OL}=0.2V_{DD}, Ta=-20 to 70°C

Item	Symbol	Min.	Typ.	Max.	Unit
Transmit data output delay time	tsmd	–	–	300	nS
Receive data input set-up time	tsms	200	–	–	nS
Receive data input hold time	tsmh	200	–	–	nS



Slave mode 1

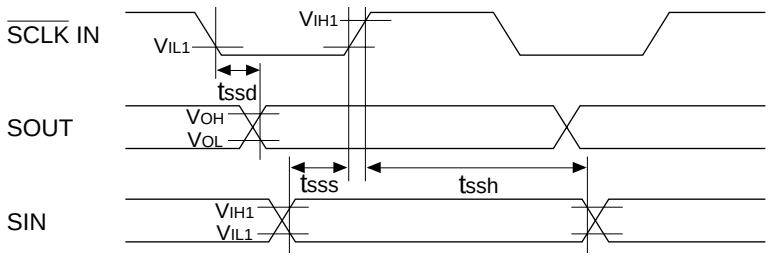
Condition: V_{DD}=1.5V, V_{SS}=0V, fosc=32.768kHz, V_{IH1}=0.8V_{DD}, V_{IL1}=0.2V_{DD}, V_{OH}=0.8V_{DD}, V_{OL}=0.2V_{DD}, Ta=-20 to 70°C

Item	Symbol	Min.	Typ.	Max.	Unit
Transmit data output delay time	tssd	–	–	5	µS
Receive data input set-up time	tsss	10	–	–	µS
Receive data input hold time	tssh	5	–	–	µS

Slave mode 2

Condition: V_{DD}=3.0V, V_{SS}=0V, fosc=1MHz, V_{IH1}=0.8V_{DD}, V_{IL1}=0.2V_{DD}, V_{OH}=0.8V_{DD}, V_{OL}=0.2V_{DD}, Ta=-20 to 70°C

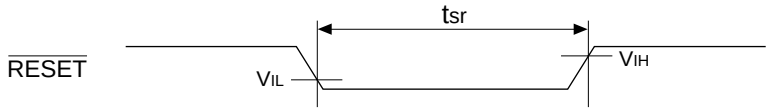
Item	Symbol	Min.	Typ.	Max.	Unit
Transmit data output delay time	tssd	–	–	300	nS
Receive data input set-up time	tsss	200	–	–	nS
Receive data input hold time	tssh	200	–	–	nS



6.5.2 $\overline{RESET}$ input

Condition: V_{DD}=1.5V/3.0V, V_{SS}=0V, V_{IH}=0.5V_{DD}, V_{IL}=0.1V_{DD}, Ta=-20 to 70°C

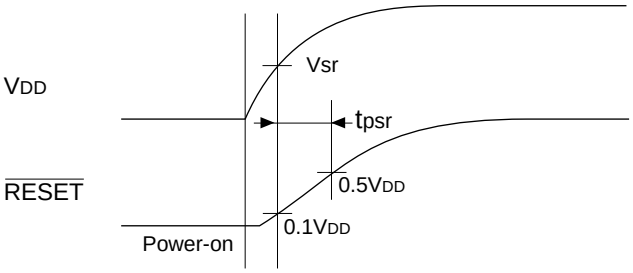
Item	Symbol	Min.	Typ.	Max.	Unit
$\overline{RESET}$ input time	tsr	5.0			mS

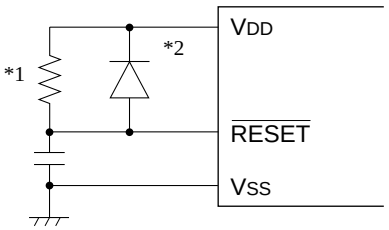


6.5.3 Power-on reset

Condition: V_{DD}=1.5V/3.0V, V_{SS}=0V, Ta=-20 to 70°C

Item	Symbol	Min.	Typ.	Max.	Unit
Operating supply voltage	Vsr	0.8·V_{DD}			V
$\overline{RESET}$ input time	tpsr	5.0			mS





*1 When the built-in pull-up resistor is not used.

*2 Because the potential of the $\overline{RESET}$ terminal not reached V_{DD} level or higher.

6.6 Oscillation Characteristics

Oscillation characteristics will vary according to different conditions (elements used, board pattern). Use the following characteristics are as reference values.

Crystal oscillation

Unless otherwise specified:

V_{DD}=3.0V, V_{SS}=0V, f_{OSC}=32.768kHz, Crystal: C-002R (C_I=35kΩ), C_G=25pF, C_D=built-in, Ta=25°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start voltage	Vsta	tsta≤3sec (Heavy load protection mode ON)	0.8			V
		tsta≤3sec (Heavy load protection mode OFF)	1.1			V
Oscillation stop voltage	Vstp	tstp≤10sec (Heavy load protection mode ON)	0.8			V
		tstp≤10sec (Heavy load protection mode OFF)	1.1			V
Built-in capacitance (drain)	C_D	Including the parasitic capacitance inside the IC (in chip)		14		pF
Frequency/voltage deviation	∂f/∂V	V_{DD}=0.8 to 3.6V (Heavy load protection mode ON)			5	ppm
		V_{DD}=1.1 to 3.6V (Heavy load protection mode OFF)			5	ppm
Frequency/IC deviation	∂f/∂IC		-10		10	ppm
Frequency adjustment range	∂f/∂C_G	C_G=5 to 25pF	30	40		ppm
Harmonic oscillation start voltage	V_{hho}	C_G=5pF (V_{DD})	3.6			V
Permitted leak resistance	R_{leak}	Between OSC1 and V_{DD}, V_{SS}	200			MΩ

CR oscillation

Unless otherwise specified:

V_{DD}=3.0V, V_{SS}=0V, R_{CR}=1MΩ, Ta=25°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation frequency dispersion	∂f_{OSCCR}	623B (Heavy load protection ON, V_{DD}=0.8 to 3.6V)	-20	40kHz	+20	%
		623B (Heavy load protection OFF, V_{DD}=1.1 to 3.6V)	-20	40kHz	+20	%
		62A3B (V_{DD}=1.7 to 3.6V)	-30	500kHz	+30	%
Oscillation start voltage	Vsta	623B	0.8			V
		62A3B	1.7			V
Oscillation start time	tsta				3	mS
Oscillation stop voltage	Vstp	623B	0.8			V
		62A3B	1.7			V

Ceramic oscillation

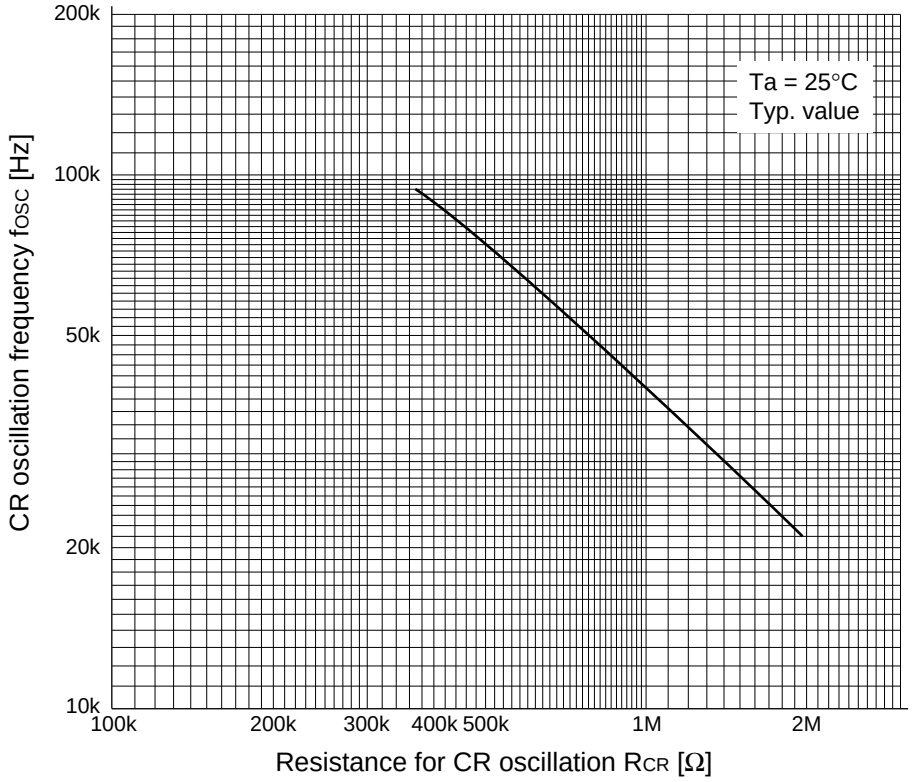
Unless otherwise specified:

V_{DD}=3.0V, V_{SS}=0V, Ceramic oscillator: CSA1.0MG, C_{GC}=C_{DC}=100pF, Ta=25°C

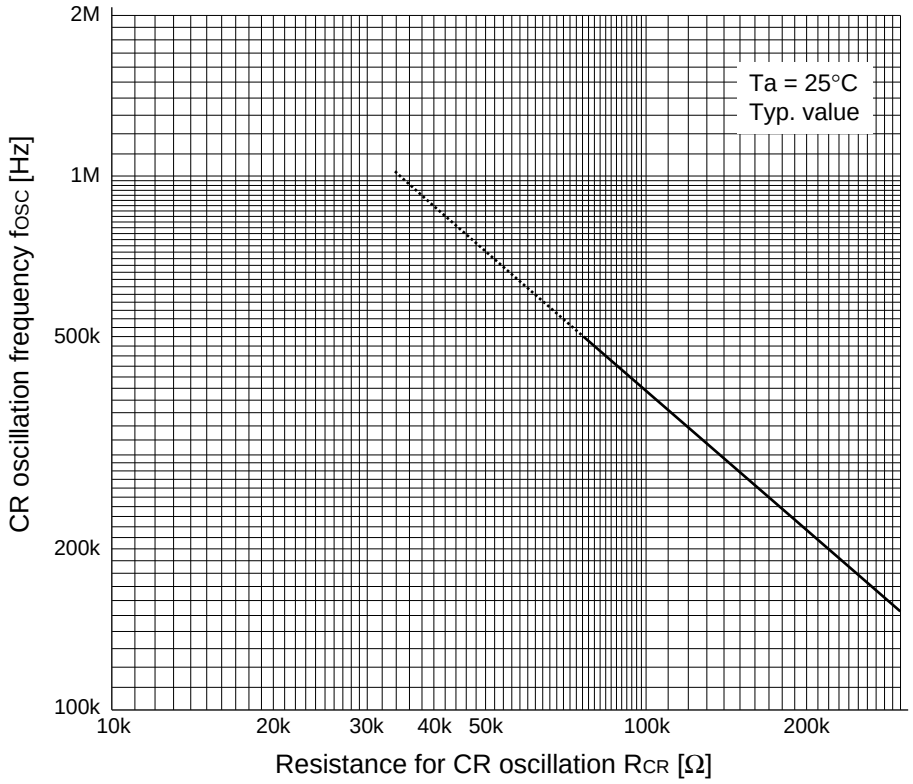
Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start voltage	Vsta		1.7			V
Oscillation start time	tsta				20	mS

CR oscillation frequency characteristic (reference value)

E0C623B



E0C62A3B

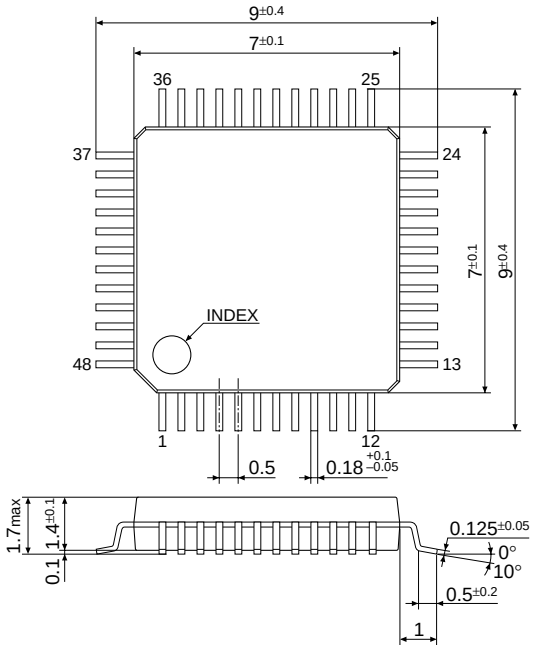


CHAPTER 7 PACKAGE

7.1 Plastic Package

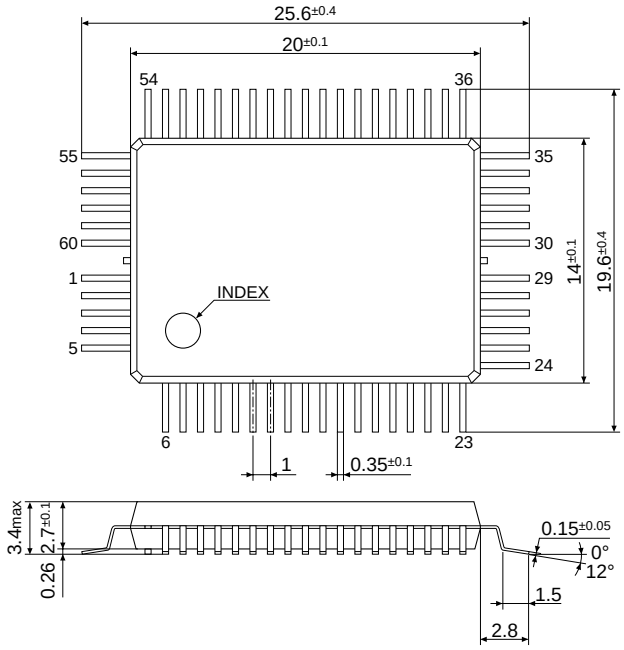
QFP12-48 pin

(Unit: mm)



QFP5-60 pin

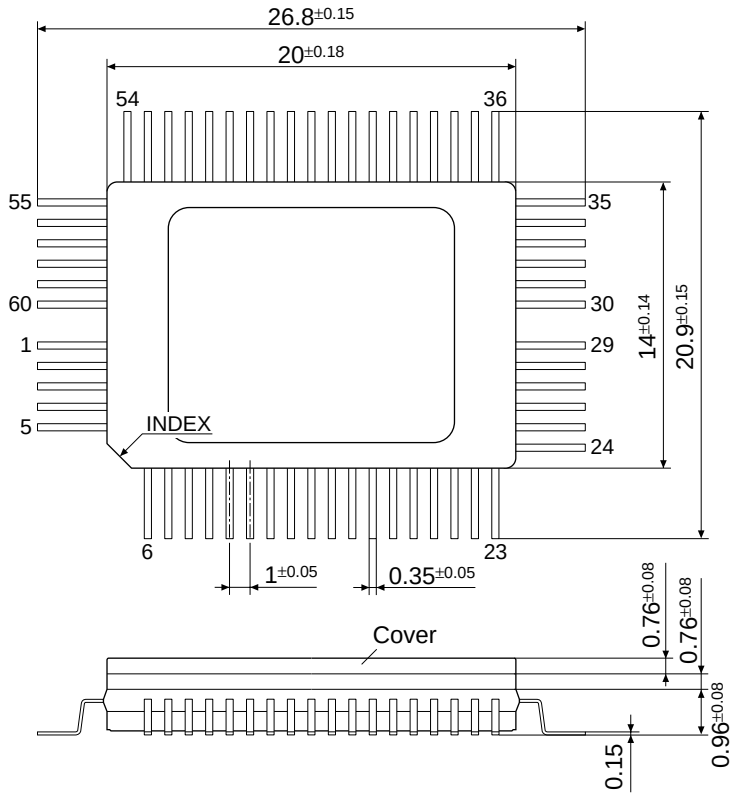
(Unit: mm)



7.2 Ceramic Package for Test Samples

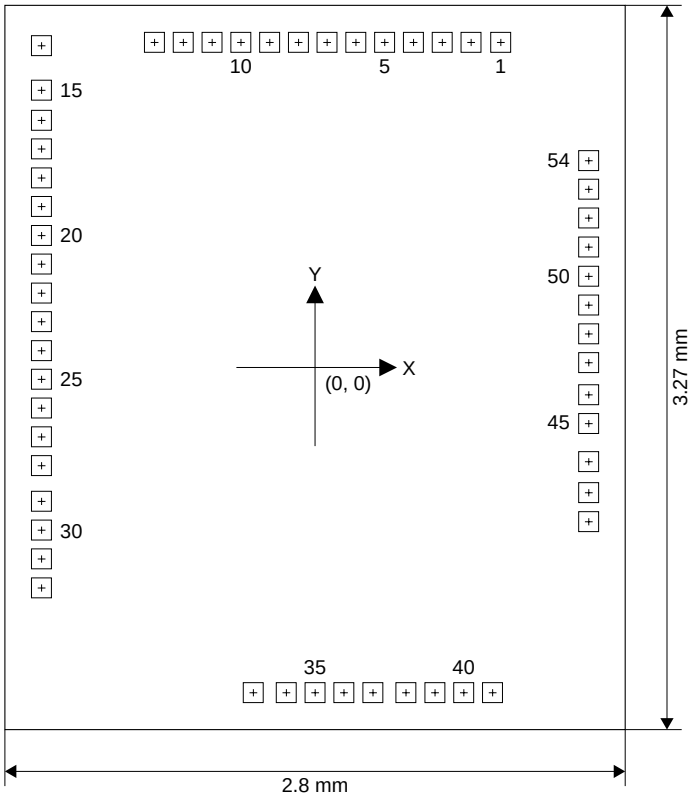
QFP5-60 pin

(Unit: mm)



CHAPTER 8 PAD LAYOUT

8.1 Diagram of Pad Layout



Chip thickness: 400 (μm)
Pad opening: 90 (μm)

8.2 Pad Coordinates

Unit: mm

No.	Pad name	X	Y	No.	Pad name	X	Y	No.	Pad name	X	Y
1	COM3	0.838	1.468	19	SEG17	-1.235	0.727	37	K03	0.261	-1.468
2	SEG0	0.704	1.468	20	SEG18	-1.235	0.596	38	R00	0.410	-1.468
3	SEG1	0.574	1.468	21	SEG19	-1.235	0.467	39	R01	0.541	-1.468
4	SEG2	0.444	1.468	22	SEG20	-1.235	0.336	40	R02	0.671	-1.468
5	SEG3	0.314	1.468	23	SEG21	-1.235	0.207	41	R03	0.801	-1.468
6	SEG4	0.184	1.468	24	SEG22	-1.235	0.076	42	V_{SS}	1.235	-0.696
7	SEG5	0.054	1.468	25	SEG23	-1.235	-0.053	43	V_{DD}	1.235	-0.565
8	SEG6	-0.075	1.468	26	SEG24	-1.235	-0.183	44	OSC1	1.235	-0.425
9	SEG7	-0.205	1.468	27	SEG25	-1.235	-0.313	45	OSC2	1.235	-0.253
10	SEG8	-0.335	1.468	28	$\overline{TEST}$	-1.235	-0.443	46	V_{D1}	1.235	-0.123
11	SEG9	-0.465	1.468	29	P03	-1.235	-0.604	47	CA	1.235	0.022
12	SEG10	-0.595	1.468	30	P02	-1.235	-0.734	48	CB	1.235	0.152
13	SEG11	-0.725	1.468	31	P01	-1.235	-0.864	49	V_{C1}	1.235	0.282
14	SEG12	-1.235	1.453	32	P00	-1.235	-0.995	50	V_{C2}	1.235	0.412
15	SEG13	-1.235	1.252	33	$\overline{RESET}$	-0.279	-1.468	51	V_{C3}	1.235	0.544
16	SEG14	-1.235	1.116	34	K00	-0.130	-1.468	52	COM0	1.235	0.674
17	SEG15	-1.235	0.987	35	K01	0	-1.468	53	COM1	1.235	0.805
18	SEG16	-1.235	0.856	36	K02	0.130	-1.468	54	COM2	1.235	0.934

EPSON International Sales Operations

AMERICA

EPSON ELECTRONICS AMERICA, INC.

- HEADQUARTERS -
1960 E. Grand Avenue
El Segundo, CA 90245, U.S.A.
Phone: +1-310-955-5300 Fax: +1-310-955-5400

- SALES OFFICES -

West
150 River Oaks Parkway
San Jose, CA 95134, U.S.A.
Phone: +1-408-922-0200 Fax: +1-408-922-0238

Central
101 Virginia Street, Suite 290
Crystal Lake, IL 60014, U.S.A.
Phone: +1-815-455-7630 Fax: +1-815-455-7633

Northeast
301 Edgewater Place, Suite 120
Wakefield, MA 01880, U.S.A.
Phone: +1-781-246-3600 Fax: +1-781-246-5443

Southeast
3010 Royal Blvd. South, Suite 170
Alpharetta, GA 30005, U.S.A.
Phone: +1-877-EEA-0020 Fax: +1-770-777-2637

EUROPE

EPSON EUROPE ELECTRONICS GmbH

- HEADQUARTERS -
Riesstrasse 15
80992 Muenchen, GERMANY
Phone: +49-(0)89-14005-0 Fax: +49-(0)89-14005-110

- GERMANY -
SALES OFFICE
Altstadtstrasse 176
51379 Leverkusen, GERMANY
Phone: +49-(0)217-15045-0 Fax: +49-(0)217-15045-10

- UNITED KINGDOM -
UK BRANCH OFFICE
2.4 Doncastle House, Doncastle Road
Bracknell, Berkshire RG12 8PE, ENGLAND
Phone: +44-(0)1344-381700 Fax: +44-(0)1344-381701

- FRANCE -
FRENCH BRANCH OFFICE
1 Avenue de l' Atlantique, LP 915 Les Conquerants
Z.A. de Courtaboeuf 2, F-91976 Les Ulis Cedex, FRANCE
Phone: +33-(0)1-64862350 Fax: +33-(0)1-64862355

ASIA

- CHINA -
EPSON (CHINA) CO., LTD.
28F, Beijing Silver Tower 2# North RD DongSanHuan
ChaoYang District, Beijing, CHINA
Phone: 64106655 Fax: 64107320

SHANGHAI BRANCH
4F, Bldg., 27, No. 69, Gui Jing Road
Caohejing, Shanghai, CHINA
Phone: 21-6485-5552 Fax: 21-6485-0775

- HONG KONG, CHINA -
EPSON HONG KONG LTD.
20/F., Harbour Centre, 25 Harbour Road
Wanchai, HONG KONG
Phone: +852-2585-4600 Fax: +852-2827-4346
Telex: 65542 EPSCO HX

- TAIWAN, R.O.C. -
EPSON TAIWAN TECHNOLOGY & TRADING LTD.
10F, No. 287, Nanking East Road, Sec. 3
Taipei, TAIWAN, R.O.C.
Phone: 02-2717-7360 Fax: 02-2712-9164
Telex: 24444 EPSONTB

HSINCHU OFFICE
13F-3, No. 295, Kuang-Fu Road, Sec. 2
HsinChu 300, TAIWAN, R.O.C.
Phone: 03-573-9900 Fax: 03-573-9169

- SINGAPORE -
EPSON SINGAPORE PTE., LTD.
No. 1 Temasek Avenue, #36-00
Millenia Tower, SINGAPORE 039192
Phone: +65-337-7911 Fax: +65-334-2716

- KOREA -
SEIKO EPSON CORPORATION KOREA OFFICE
50F, KLI 63 Bldg., 60 Yoido-Dong
Youngdeungpo-Ku, Seoul, 150-010, KOREA
Phone: 02-784-6027 Fax: 02-767-3677

- JAPAN -
SEIKO EPSON CORPORATION
ELECTRONIC DEVICES MARKETING DIVISION

Electronic Device Marketing Department
IC Marketing & Engineering Group
421-8, Hino, Hino-shi, Tokyo 191-8501, JAPAN
Phone: +81-(0)42-587-5816 Fax: +81-(0)42-587-5624

ED International Marketing Department I (Europe & U.S.A.)
421-8, Hino, Hino-shi, Tokyo 191-8501, JAPAN
Phone: +81-(0)42-587-5812 Fax: +81-(0)42-587-5564

ED International Marketing Department II (Asia)
421-8, Hino, Hino-shi, Tokyo 191-8501, JAPAN
Phone: +81-(0)42-587-5814 Fax: +81-(0)42-587-5110

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