

CMOS 4-BIT SINGLE CHIP MICROCOMPUTER
E0C63256 TECHNICAL MANUAL

E0C63256 Technical Hardware



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CONTENTS

CHAPTER 1	OUTLINE	1
1.1	Features	1
1.2	Block Diagram	2
1.3	Pin Layout Diagram	3
1.4	Pin Description	3
1.5	Mask Option	4
CHAPTER 2	POWER SUPPLY AND INITIAL RESET	6
2.1	Power Supply	6
2.1.1	Voltage <VD1> for oscillation circuit and internal circuits	6
2.1.2	Voltage <VC1, VC2, VC3> for LCD driving	6
2.2	Initial Reset	8
2.2.1	Reset terminal (RESET)	8
2.2.2	Simultaneous low input to terminals K00–K03	9
2.2.3	Internal register at initial resetting	10
2.2.4	Terminal settings at initial resetting	11
2.3	Test Terminal ($\overline{\text{TEST}}$)	11
CHAPTER 3	CPU, ROM, RAM	12
3.1	CPU	12
3.2	Code ROM	12
3.3	RAM	13
CHAPTER 4	PERIPHERAL CIRCUITS AND OPERATION	14
4.1	Memory Map	14
4.2	Oscillation Circuit and Prescaler	19
4.2.1	Configuration of oscillation circuit	19
4.2.2	Kind of oscillation circuit	19
4.2.3	Prescaler	20
4.2.4	Clock frequency and instruction execution time	21
4.2.5	I/O memory of prescaler	21
4.2.6	Programming note	21
4.3	Input Ports (K00–K03)	22
4.3.1	Configuration of input ports	22
4.3.2	Interrupt function	22
4.3.3	Mask option	23
4.3.4	I/O memory of input ports	24
4.3.5	Programming notes	26
4.4	Output Ports (R00–R03)	27
4.4.1	Configuration of output ports	27
4.4.2	Mask option	27
4.4.3	High impedance control	28
4.4.4	Special output	28
4.4.5	I/O memory of output ports	30
4.4.6	Programming notes	31

- 4.5 I/O Ports (P20–P23 and P40–P43) 32
 - 4.5.1 Configuration of I/O ports 32
 - 4.5.2 Mask option 33
 - 4.5.3 I/O control registers and input/output mode 33
 - 4.5.4 Pull-up during input mode 33
 - 4.5.5 I/O memory of I/O ports 34
 - 4.5.6 Programming note 36
- 4.6 LCD Driver (COM0–COM3, SEG0–SEG19) 37
 - 4.6.1 Configuration of LCD driver 37
 - 4.6.2 Power supply for LCD driving/LCD drive bias 37
 - 4.6.3 Control of LCD display and drive waveform 38
 - 4.6.4 Mask option 44
 - 4.6.5 I/O memory of LCD driver 45
 - 4.6.6 Programming note 47
- 4.7 Clock Timer and Watchdog Timer 48
 - 4.7.1 Configuration of clock timer and watchdog timer 48
 - 4.7.2 Clock timer operation 48
 - 4.7.3 Watchdog timer operation 49
 - 4.7.4 I/O memory of clock timer and watchdog timer 50
 - 4.7.5 Programming notes 51
- 4.8 Programmable Timer 52
 - 4.8.1 Configuration of programmable timer 52
 - 4.8.2 8-/16-bit mode 53
 - 4.8.3 Programmable timer operation 53
 - 4.8.4 Interrupt function 56
 - 4.8.5 Event counter function 56
 - 4.8.6 Setting of PTOUT output 58
 - 4.8.7 I/O memory of programmable timer 59
 - 4.8.8 Programming notes 64
- 4.9 Buzzer Output Circuit 65
 - 4.9.1 Configuration of buzzer output circuit 65
 - 4.9.2 Mask option 65
 - 4.9.3 Control of buzzer output 66
 - 4.9.4 I/O memory of buzzer output circuit 67
 - 4.9.5 Programming note 67
- 4.10 A/D Converter 68
 - 4.10.1 Characteristics and configuration of A/D converter 68
 - 4.10.2 Terminal configuration of A/D converter 68
 - 4.10.3 Mask option 69
 - 4.10.4 Control of A/D converter 69
 - 4.10.5 Interrupt function 71
 - 4.10.6 I/O memory of A/D converter 71
 - 4.10.7 Programming notes 73
- 4.11 Interrupt and HALT/SLEEP 74
 - 4.11.1 Interrupt factor 76
 - 4.11.2 Interrupt mask 76
 - 4.11.3 Interrupt vector 77
 - 4.11.4 I/O memory of interrupt 78
 - 4.11.5 Programming notes 79

CHAPTER 5	SUMMARY OF NOTES	80
CHAPTER 6	BASIC EXTERNAL WIRING DIAGRAM	83
CHAPTER 7	ELECTRICAL CHARACTERISTICS	84
7.1	Absolute Maximum Rating	84
7.2	Recommended Operating Conditions	84
7.3	DC Characteristics	85
7.3.1	Input characteristics	85
7.3.2	Output characteristics	85
7.4	Analog Circuit Characteristics	86
7.4.1	LCD drive voltage characteristics	86
7.4.2	A/D conversion characteristics	86
7.5	Current Consumption	87
7.6	AC Characteristics	88
7.6.1	Operating range	88
7.6.2	Input clock	88
7.6.3	Power-on reset	89
7.6.4	A/D conversion characteristics	89
7.7	Oscillation Characteristics	90
7.7.1	Crystal oscillation circuit	90
7.7.2	Ceramic oscillation circuit	90
7.7.3	CR oscillation circuit	90
7.8	Characteristic Curves (reference value)	91
7.8.1	Output current characteristics	91
7.8.2	Power current - frequency characteristics	93
7.8.3	Analog system operating current - voltage characteristic	95
7.8.4	CR oscillation frequency characteristics	96
CHAPTER 8	PACKAGE	97
8.1	Plastic Package	97
8.2	Ceramic Package for Test Samples	98
CHAPTER 9	PAD LAYOUT	99
9.1	Diagram of Pad Layout	99
9.2	Pad Coordinates	99
CHAPTER 10	PRECAUTIONS ON MOUNTING	100

CHAPTER 1 OUTLINE

The E0C63256 is a microcomputer which has a high-performance 4-bit CPU E0C63000 as the core CPU, ROM (6,144 words × 13 bits), RAM (256 words × 4 bits), clock timer, watchdog timer, programmable timer, an LCD driver that can drive a maximum 20 segments × 4 commons and A/D converter built-in. It features a wide operating voltage (2.7 to 5.5 V) and operating frequency (0.5 to 4.5 MHz), and is most suitable for applications such as control units for the household electric appliances which need A/D conversion and liquid crystal display.

1.1 Features

Oscillation circuit	0.5 to 4.5 MHz Crystal, ceramic, CR oscillation circuit or external clock input (*1)
Instruction set	Basic instruction: 47 types (411 instructions with all) Addressing mode: 8 types
Instruction execution time	During operation at 2 MHz: 1 μsec 2 μsec 3 μsec During operation at 4.194304 MHz: 0.48 μsec 0.95 μsec 1.43 μsec
ROM capacity	Code ROM: 6,144 words × 13 bits
RAM capacity	Data memory: 256 words × 4 bits Display memory: 20 words × 4 bits
Input port	4 bits (Pull-up resistors may be supplemented *1)
Output port	4 bits (It is possible to switch the 2 bits to clock output *2)
I/O port	8 bits (It is possible to switch the 4 bits to A/D converter input *2)
LCD driver	20 segments × 4, 3 or 2 commons (*2) 1/3 or 1/2 bias drive (*1)
Time base counter	Clock timer (when 4.194304 MHz oscillation clock is used)
Programmable timer	Built-in 8 bits × 4 ch, with event counter and clock output function Usable for 8 bits × 4 ch, 8 bits × 2 ch & 16 bits × 1 ch or 16 bits × 2 ch
Watchdog timer	Built-in
Buzzer output	Buzzer frequency: 2 kHz or 4 kHz (*2)
A/D converter	Resolution: 8 bits, analog input: 4 ch
External interrupt	Input port interrupt: 1 system
Internal interrupt	Clock timer interrupt: 1 system Programmable timer interrupt: 4 systems A/D converter interrupt: 1 system
Power supply voltage	2.7 V to 5.5 V
Operating temperature range	-20°C to 85°C
Current consumption (Typ.)	During SLEEP 0.3 μA During HALT (*3) 4.194304 MHz: 3.0 V 620 μA (Crystal oscillation) 5.0 V 660 μA 4 MHz: 3.0 V 670 μA (Ceramic oscillation) 5.0 V 710 μA 2 MHz: 3.0 V 740 μA (CR oscillation) 5.0 V 780 μA During operation (*3) 4.194304 MHz: 3.0 V 1.5 mA (Crystal oscillation) 5.0 V 1.5 mA 4 MHz: 3.0 V 1.5 mA (Ceramic oscillation) 5.0 V 1.5 mA 2 MHz: 3.0 V 1.2 mA (CR oscillation) 5.0 V 1.2 mA
Package	QFP13-64pin (plastic) or chip

*1: Can be selected with mask option.

*2: Can be selected with software.

*3: A/D converter operating current is not included.

1.2 Block Diagram

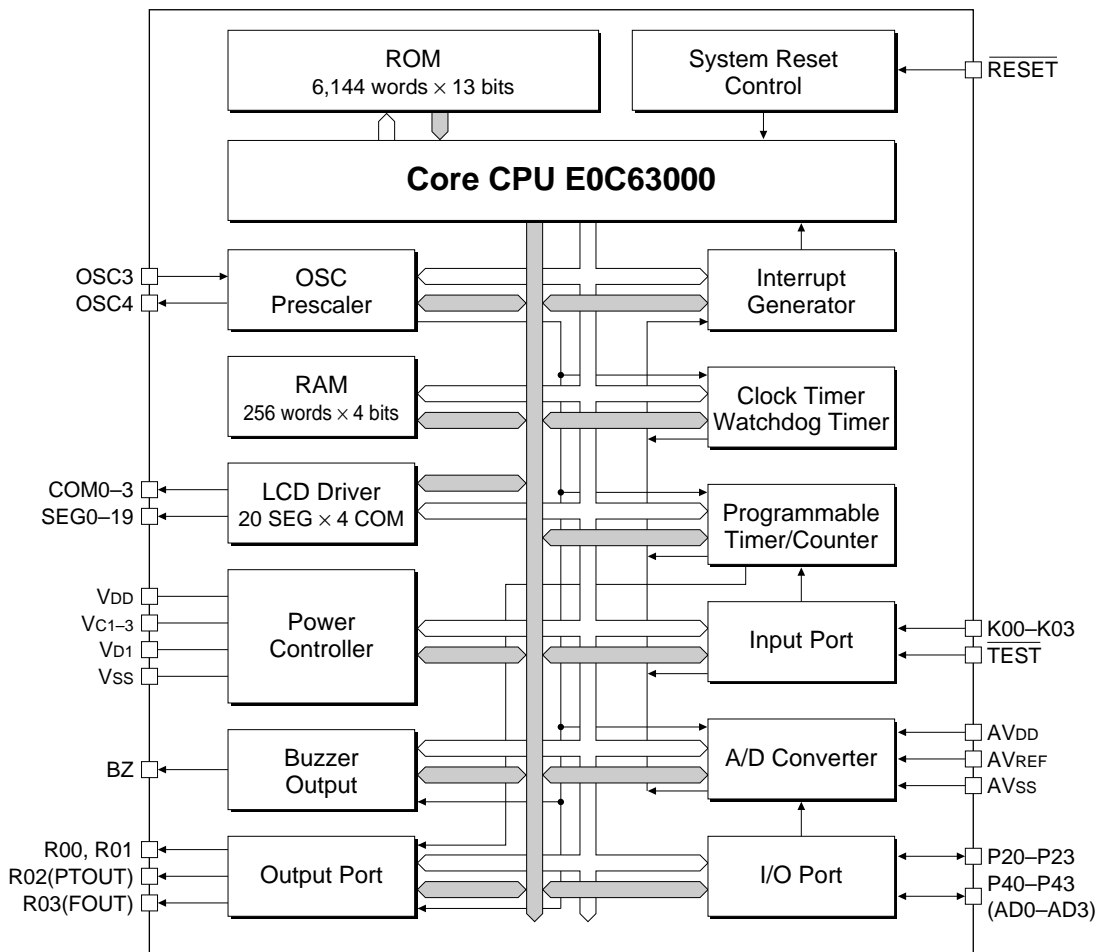
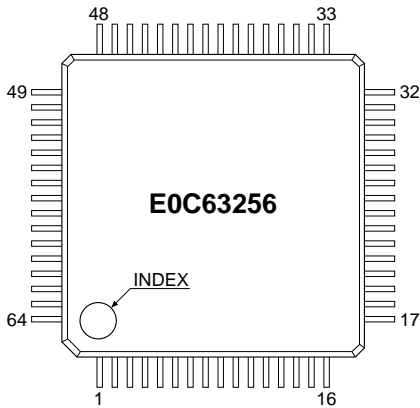


Fig. 1.2.1 Block diagram

1.3 Pin Layout Diagram

QFP13-64pin



No.	Name	No.	Name	No.	Name	No.	Name
1	SEG13	17	RESET	33	N.C.	49	COM2
2	SEG14	18	TEST	34	BZ	50	COM3
3	SEG15	19	VSS	35	R00	51	SEG0
4	SEG16	20	OSC3	36	R01	52	SEG1
5	SEG17	21	OSC4	37	R02	53	SEG2
6	SEG18	22	VD1	38	R03	54	SEG3
7	SEG19	23	VDD	39	P20	55	SEG4
8	N.C.	24	AVDD	40	P21	56	SEG5
9	N.C.	25	AVREF	41	P22	57	SEG6
10	N.C.	26	AVSS	42	P23	58	SEG7
11	N.C.	27	N.C.	43	K00	59	SEG8
12	N.C.	28	N.C.	44	K01	60	SEG9
13	N.C.	29	P40	45	K02	61	SEG10
14	Vc1	30	P41	46	K03	62	SEG11
15	Vc2	31	P42	47	COM0	63	SEG12
16	Vc3	32	P43	48	COM1	64	N.C.

N.C. : No Connection

Fig. 1.3.1 Pin layout diagram

1.4 Pin Description

Table 1.4.1 Pin description

Pin name	Pin No.	In/Out	Function
VDD	23	–	Power (+) supply pin
VSS	19	–	Power (–) supply pin
AVDD	24	–	Power (+) supply pin for analog circuit system
AVSS	26	–	Power (–) supply pin for analog circuit system
AVREF	25	I	Reference voltage input pin for analog circuit system
VD1	22	–	Oscillation/internal logic system regulated voltage output pin
Vc1, Vc2, Vc3	14, 15, 16	–	LCD system power supply pin 1/3 or 1/2 bias (selected by mask option)
OSC3	20	I	Crystal/ceramic/CR oscillation/external clock input pin (selected by mask option)
OSC4	21	O	Crystal/ceramic/CR oscillation output pin (selected by mask option)
K00–K03	43–46	I	Input port
P20–P23	39–42	I/O	I/O port
P40–P43	29–32	I/O	I/O port (switching to A/D converter input is possible by software)
R00	35	O	Output port
R01	36	O	Output port
R02	37	O	Output port (switching to PTOUT signal output is possible by software)
R03	38	O	Output port (switching to FOUT signal output is possible by software)
COM0–COM3	47–50	O	LCD common output pin (1/4, 1/3, 1/2 duty can be selected by software)
SEG0–SEG19	51–63, 1–7	O	LCD segment output pin
BZ	34	O	Buzzer output pin
RESET	17	I	Initial reset input pin
TEST	18	I	Testing input pin

1.5 Mask Option

Mask options shown below are provided for the E0C63256. Several hardware specifications are prepared in each mask option, and one of them can be selected according to the application. The function option generator FOG63256 and the segment option generator SOG63256, that have been prepared as the development software tool of E0C63256, are used for this selection. Mask pattern of the IC is finally generated based on the data created by the FOG63256 and the SOG63256. Refer to the "E0C63256 Development Tool Manual" for the FOG63256 and the SOG63256.

<Functions selectable with E0C63256 mask options>

(1) *External reset by simultaneous LOW input to the input port (K00–K03)*

This function resets the IC when several keys are pressed simultaneously. The mask option is used to select whether this function is used or not. Further when the function is used, a combination of the input ports (K00–K03), which are connected to the keys to be pressed simultaneously, can be selected. Refer to Section 2.2.2, "Simultaneous low input to terminals K00–K03", for details.

(2) *Time authorize circuit for the simultaneous LOW input reset function*

When using the external reset function (shown in 1 above), using the time authorize circuit or not can be selected by the mask option. The reset function works only when the input time of simultaneous LOW is more than the rule time if the time authorize circuit is being used. Refer to Section 2.2.2, "Simultaneous low input to terminals K00–K03", for details.

(3) *Input port pull-up resistor*

The mask option is used to select whether the pull-up resistor is supplemented to the input ports or not. It is possible to select for each bit of the input ports. Refer to Section 4.3.3, "Mask option", for details.

(4) *Output specification of the output port*

Either complementary output or N-channel open drain output can be selected as the output specification for the output ports. It is possible to select for each bit of the output ports. Refer to Section 4.4.2, "Mask option", for details.

(5) *Output specification / pull-up resistor of the I/O ports*

Either complementary output or N-channel open drain output can be selected as the output specification when the I/O port is in the output mode. Further, whether or not the pull-up resistors working in the input mode are supplemented can be selected. It is possible to select for each bit of the I/O ports. Refer to Section 4.5.2, "Mask option", for details.

(6) *Power supply for LCD driving/LCD drive bias*

Either the internal power supply or an external power supply can be selected as the LCD system power supply. Further the LCD drive method can be selected from a 1/3 bias drive or a 1/2 bias drive. Refer to Section 2.1.2, "Voltage <V_{C1}, V_{C2}, V_{C3}> for LCD driving", for details.

(7) *LCD segment specification*

The display memory can be allocated to the optional SEG terminal. It is also possible to set the optional SEG terminal for DC output. Refer to Section 4.6.4, "Mask option", for details.

(8) *Polarity of the buzzer output signal*

It is possible to select the polarity of the buzzer signal output from the BZ terminal. Select either positive polarity or negative polarity according to the external drive transistor to be used. Refer to Section 4.9.2, "Mask option", for details.

(9) Oscillation circuit

The specification of the oscillation circuit can be selected from either crystal/ceramic oscillation , CR oscillation or external clock input.

Refer to Section 4.2.2, "Kind of oscillation circuit", for details.

(10) $\overline{\text{RESET}}$ terminal pull-up resistor

This mask option can select whether the pull-up resistor for the $\overline{\text{RESET}}$ terminal is used or not.

CHAPTER 2 POWER SUPPLY AND INITIAL RESET

2.1 Power Supply

The E0C63256 operating power voltage is as follows:

2.7 V to 5.5 V

The E0C63256 operates by applying a single power supply within the above range between VDD and VSS. The E0C63256 itself generates the voltage necessary for all the internal circuits by the built-in power supply circuits shown in Table 2.1.1.

Table 2.1.1 Power supply circuits

Circuit	Power supply circuit	Input voltage	Output voltage
Oscillation and internal circuits	Oscillation system voltage regulator	VDD	VD1
LCD driver	LCD system voltage circuit	VC3	VC1, VC2

Besides the power supply terminals mentioned above, two power supply terminals, AVDD and AVSS for the built-in A/D converter, are also provided.

- Note:
- Do not drive external loads with the output voltage from the internal power supply circuits.
 - Short-circuit between VC1 and VC2 when 1/2-bias LCD drive is selected.
 - Short-circuit between AVSS and VSS.

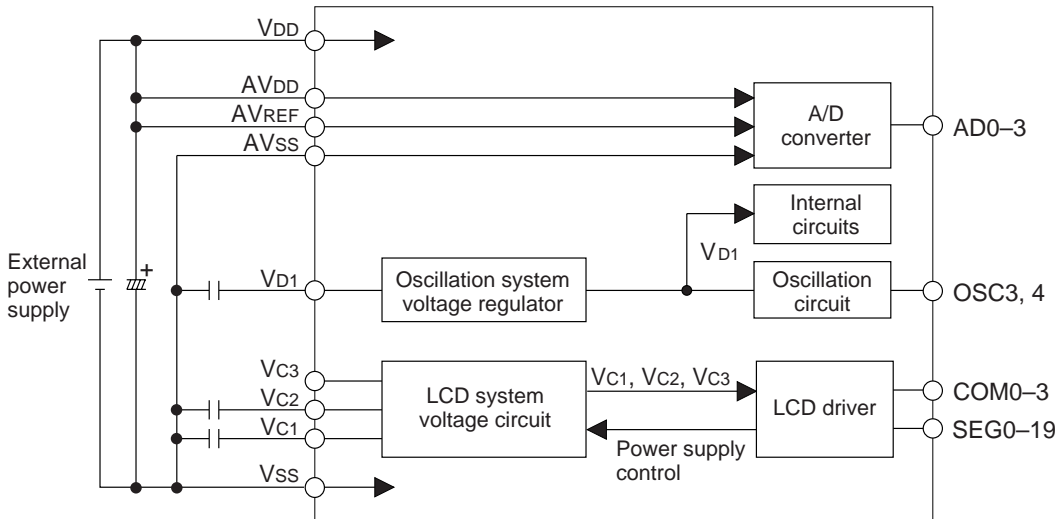


Fig. 2.1.1 Configuration of power supply

2.1.1 Voltage <VD1> for oscillation circuit and internal circuits

VD1 is a voltage for the oscillation circuit and the internal logic circuits, and is generated by the oscillation system voltage regulator for stabilizing the oscillation.

VD1 that is output from the oscillation system voltage regulator is 2.4 V (Typ.).

2.1.2 Voltage <VC1, VC2, VC3> for LCD driving

VC1-VC3 are the LCD drive voltage. For driving LCD, either 1/3 bias or 1/2 bias can be selected by mask option, and each LCD drive voltage is set as shown below according to the selection.

When 1/3 bias is selected: VC1 = VC3 × 1/3, VC2 = VC3 × 2/3

When 1/2 bias is selected: VC1 = VC2 = VC3 × 1/2

The power source of VC_1 – VC_3 can also be selected from either the internal LCD system voltage circuit or an external power supply. This mask option allows selection of the following three conditions.

(1) Internal power supply (external V_{C3} is used)

When this option is selected, VC_3 should be supplied from outside the IC. VC_1 and VC_2 are generated by dividing the VC_3 with resistors inside the IC. It enlarges the selection range of the LCD panel because VC_3 can be controlled using the external power supply. It also enables adjustment contrast of the LCD panel by varying the VC_3 .

However, be sure to supply a voltage in the range of $2.7\text{ V} \leq V_{C3} \leq 5.5\text{ V}$ to the VC_3 terminal. Do not supply a voltage out of the range.

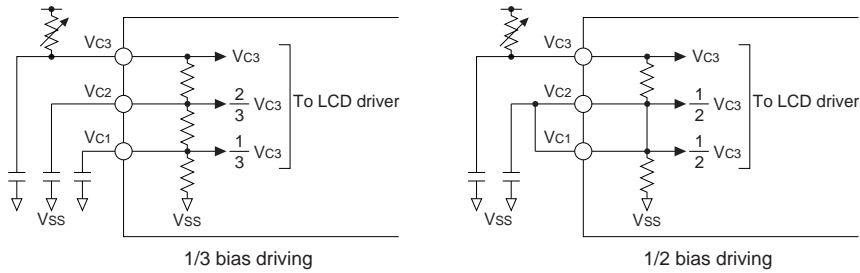


Fig. 2.1.2.1 Option 1 (Internal power supply/external V_{C3} used)

(2) Internal power supply (external V_{C3} is not used, $V_{C3} = V_{DD}$)

When this option is selected VC_1 – VC_3 are all generated inside the IC. It reduces the number of external parts. In this case, open the VC_3 terminal because the terminal is connected to the V_{DD} inside the IC.

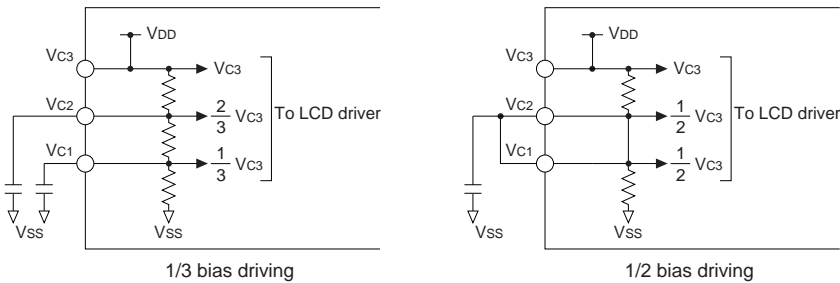


Fig. 2.1.2.2 Option 2 (Internal power supply/ $V_{C3} = V_{DD}$)

(3) External power supply

When this option is selected, supply all the VC_1 – VC_3 voltage from outside the IC. This option should be selected when the system requires better display quality. The voltage to be supplied must meet the following conditions: $2.7\text{ V} \leq V_{C3} \leq 5.5\text{ V}$ and $V_{SS} < V_{C1} \leq V_{C2} < V_{C3}$.

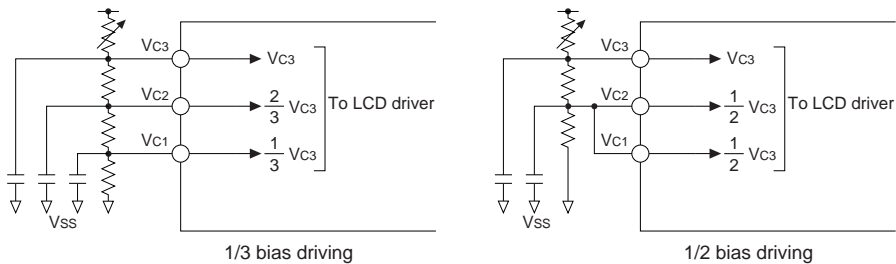


Fig. 2.1.2.3 Option 3 (External power supply)

When using the internal LCD voltage circuit, write "1" to the power control register LPWR to generate the LCD drive voltage. When the register is set to "0", VC_1 and VC_2 become the V_{SS} level, and all the SEG and COM terminals go to the V_{SS} level.

Note: It is necessary to write "1" to the LPWR register even if external power supply is selected.

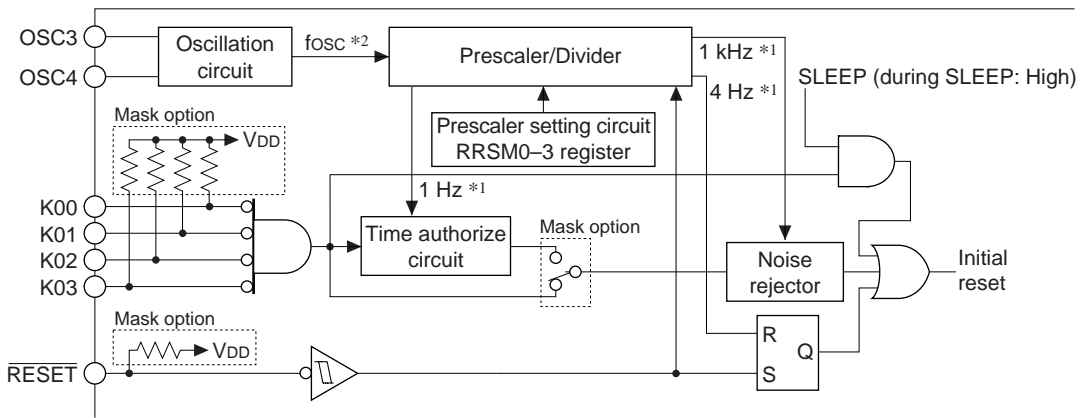
2.2 Initial Reset

To initialize the E0C63256 circuits, initial reset must be executed. There are two ways of doing this.

- (1) External initial reset by the $\overline{\text{RESET}}$ terminal
- (2) External initial reset by simultaneous low input to terminals K00–K03 (mask option setting)

Be sure to initialize the IC securely using one of the above reset functions when the power is turned on. Proper operation is not guaranteed if starting the IC with the power-on only.

Figure 2.2.1 shows the configuration of the initial reset circuit.



*1 The frequencies shown in the figure will differ according to the oscillation clock frequency and prescaler settings.
 *2 Oscillation clock frequency

Fig. 2.2.1 Configuration of initial reset circuit

2.2.1 Reset terminal ($\overline{\text{RESET}}$)

Initial reset can be executed externally by setting the reset terminal to a low level (V_{SS}). After that the initial reset is released by setting the reset terminal to a high level (V_{DD}) and the CPU starts operation. A pull-up resistor is available for the reset terminal. It can be added by mask option.

(1) Latch for reset signal

The reset input signal is maintained by the RS latch and becomes the internal initial reset signal. The RS latch is designed to release the latched signal at the rising edge of the f_{OSC} divided clock signal. The frequency of the latch release signal is $f_{OSC} / 1048576$.

Example of latch cancellation clock

- $f_{OSC} = 4.194304 \text{ MHz}$: 4 Hz
- $f_{OSC} = 2 \text{ MHz}$: 1.9 Hz

Therefore this example, a maximum of 125 msec and 264 msec are needed respectively until the internal initial reset is released after the reset terminal goes to high level.

(2) Power-on reset

To initially reset the IC securely at power-on, the reset terminal should be set the to low level as shown in Figure 2.2.1.1.

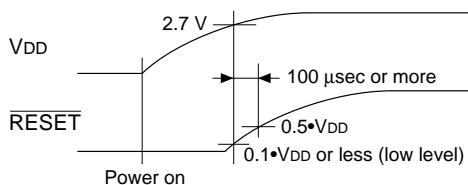


Fig. 2.2.1.1 Initial reset at power on

The reset terminal should be set to $0.1 \cdot V_{DD}$ or less (low level) until the supply voltage becomes 2.7 V or more. After that, a level of $0.5 \cdot V_{DD}$ or less should be maintained more than 100 μsec . After the reset terminal goes high, the internal initial reset will be released by the above mentioned latch.

(3) Reset during operating

To initially reset the IC securely during operating, be sure to maintain the reset terminal to low for at least 0.1 msec.

After the reset terminal goes high, the internal initial reset will be released by the above mentioned latch.

2.2.2 Simultaneous low input to terminals K00–K03

Another way of executing initial reset externally is to input a low signal simultaneously to the input ports (K00–K03) selected with the mask option. This initial reset signal passes through the noise rejector. The noise rejector removes reset pulses shorter than $256 \cdot n / f_{OSC}$ as noise (n is a prescaler parameter for dividing the oscillation clock and indicates the value of the PRSM register [FF02H] + 1). Therefore when the IC is operating, the specified input port terminals should be set to low to at least triple the reject pulse width.

The noise rejector does not operate at power-on since the oscillation has also stopped. Therefore, maintain the input port terminals at low until the above mentioned amount of time passes after oscillation starts. Table 2.2.2.1 shows the combinations of input ports (K00–K03) that can be selected with the mask option.

Table 2.2.2.1 Combinations of input ports

1	Not used
2	K00*K01*K02*K03
3	K00*K01*K02
4	K00*K01

When, for instance, mask option 2 (K00*K01*K02*K03) is selected, initial reset is executed when the signals input to the four ports K00–K03 are all low at the same time. When 3 or 4 is selected, the initial reset is done when a key entry including a combination of selected input ports is made.

If using this function, make sure that the specified ports do not go low at the same time during ordinary operation.

Further, the time authorize circuit can be selected with the mask option. The time authorize circuit checks the input time of the simultaneous low input and performs initial reset if that time is the defined time or more.

The authorization time becomes $[524288 \cdot n / f_{OSC}]$ to $[1048576 \cdot n / f_{OSC}]$ by setting the prescaler (n : PRSM setting value + 1).

Example of authorization time

In case of $f_{OSC} = 4.194304\text{MHz}$ and PRSM = 7: Min. $524288 \cdot 8 / 4194304 = 1 \text{ sec}$

Max. $1048576 \cdot 8 / 4194304 = 2 \text{ sec}$

In case of $f_{OSC} = 2\text{MHz}$ and PRSM = 3: Min. $524288 \cdot 4 / 2000000 = 1.0 \text{ sec}$

Max. $1048576 \cdot 4 / 2000000 = 2.1 \text{ sec}$

In the SLEEP status, the noise rejector and the time authorize circuit are bypassed since the oscillation circuit is off.

2.2.3 Internal register at initial resetting

Initial reset initializes the CPU as shown in Table 2.2.3.1.

The registers and flags which are not initialized by initial reset should be initialized in the program if necessary. In particular, the stack pointers SP1 and SP2 must be set as a pair because all the interrupts including NMI are masked after initial reset until both the SP1 and SP2 stack pointers are set with software.

When data is written to the EXT register, the E flag is set and the following instruction will be executed in the extended addressing mode. If an instruction which does not permit extended operation is used as the following instruction, the operation is not guaranteed. Therefore, do not write data to the EXT register for initialization only.

Refer to the "E0C63000 Core CPU Manual" for extended addressing and usable instructions.

Table 2.2.3.1 Initial values

CPU core			
Name	Symbol	Number of bits	Setting value
Data register A	A	4	Undefined
Data register B	B	4	Undefined
Extension register EXT	EXT	8	Undefined
Index register X	X	16	Undefined
Index register Y	Y	16	Undefined
Program counter	PC	16	0110H
Stack pointer SP1	SP1	8	Undefined
Stack pointer SP2	SP2	8	Undefined
Zero flag	Z	1	Undefined
Carry flag	C	1	Undefined
Interrupt flag	I	1	0
Extension flag	E	1	0
Queue register	Q	16	Undefined

Peripheral circuits		
Name	Number of bits	Setting value
RAM	4	Undefined
Display memory	4	Undefined
Other peripheral circuits	—	*

* See Section 4.1, "Memory Map".

2.2.4 Terminal settings at initial resetting

The output port (R) terminals and I/O port (P) terminals are shared with special output terminals and input terminals of the A/D converter. These functions are selected by the software. At initial reset, these terminals are set to the general purpose output port terminals and I/O port terminals. Set them according to the system in the initial routine. In addition, take care of the initial status of output terminals when designing a system.

Table 2.2.4.1 shows the list of the shared terminal settings.

Table 2.2.4.1 List of shared terminal settings

Terminal name	Terminal status at initial reset	Special output		When A/D converter is used
		PTOUT	FOUT	
R00	R00 (High output)			
R01	R01 (High output)			
R02	R02 (High output)	PTOUT		
R03	R03 (High output)		FOUT	
R20–R23	P20–P23 (Input & Pull-up *)			
P40	P40 (Input & Pull-up *)			AD0 (I)
P41	P41 (Input & Pull-up *)			AD1 (I)
P42	P42 (Input & Pull-up *)			AD2 (I)
P43	P43 (Input & Pull-up *)			AD3 (I)

* When "with pull-up" is selected by mask option (high impedance when "gate direct" is selected)

For setting procedure of the functions, see explanations for each of the peripheral circuits.

2.3 Test Terminal ($\overline{\text{TEST}}$)

This is the terminal used for the factory inspection of the IC. During normal operation, connect the $\overline{\text{TEST}}$ terminal to VDD.

CHAPTER 3 CPU, ROM, RAM

3.1 CPU

The E0C63256 has a 4-bit core CPU E0C63000 built-in as its CPU part. Refer to the "E0C63000 Core CPU Manual" for the E0C63000.

3.2 Code ROM

The built-in code ROM is a mask ROM for loading programs, and has a capacity of 6,144 steps × 13 bits. The core CPU can linearly access the program space up to step FFFFH from step 0000H, however, the program area of the E0C63256 is step 0000H to step 17FFH. The program start address after initial reset is assigned to step 0110H. The non-maskable interrupt (NMI) vector and hardware interrupt vectors are allocated to step 0100H and steps 0102H–010EH, respectively.

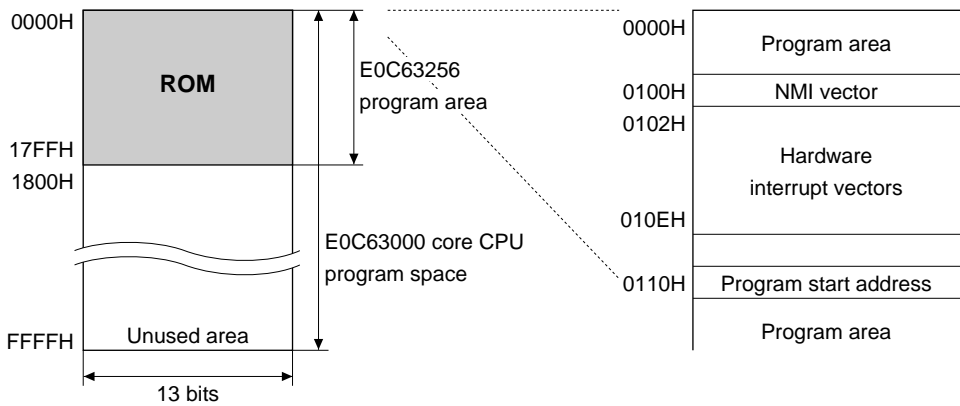


Fig. 3.2.1 Configuration of code ROM

3.3 RAM

The RAM is a data memory for storing various kinds of data, and has a capacity of 256 words \times 4 bits. The RAM area is assigned to addresses 0000H to 00FFH on the data memory map.

4-bit/16-bit data access is possible for the entire area.

When programming, keep the following points in mind.

(1) All of the RAM area is used as a stack area for subroutine call and register evacuation, so pay attention not to overlap the data area and stack area.

(2) The E0C63000 core CPU handles the stack using the stack pointer for 4-bit data (SP2) and the stack pointer for 16-bit data (SP1).

The stack pointers SP1 and SP2 change cyclically within their respective range: the range of SP1 is 0000H to 03FFH and the range of SP2 is 0000H to 00FFH. Therefore, pay attention to the SP1 value because it may be set to 0100H or more exceeding the RAM area in the E0C63256. Memory accesses except for stack operations by SP1 are 4-bit data access.

After initial reset, all the interrupts including NMI are masked until both the stack pointers SP1 and SP2 are set by software. Further, if either SP1 or SP2 is re-set when both are set already, the interrupts including NMI are masked again until the other is re-set. Therefore, the settings of SP1 and SP2 must be done as a pair.

(3) Subroutine calls use 4 words (for PC evacuation) in the stack area for 16-bit data (SP1). Interrupts use 4 words (for PC evacuation) in the stack area for 16-bit data (SP1) and 1 word (for F register evacuation) in the stack area for 4-bit data.

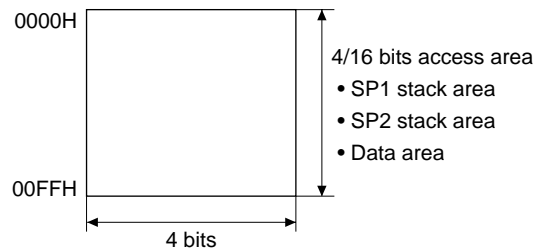


Fig. 3.3.1 Configuration of data RAM

CHAPTER 4 PERIPHERAL CIRCUITS AND OPERATION

The peripheral circuits of E0C63256 (timer, I/O, etc.) are interfaced with the CPU in the memory mapped I/O method. Thus, all the peripheral circuits can be controlled by accessing the I/O memory on the memory map using the memory operation instructions.

The following sections explain the detailed operation of each peripheral circuit.

4.1 Memory Map

The E0C63256 data memory consists of 256-word RAM, 20-word display memory and 52-word peripheral I/O memory area.

Figure 4.1.1 shows the overall memory map of the E0C63256, and Tables 4.1.1(a)–(d) the peripheral circuits' (I/O space) memory maps.

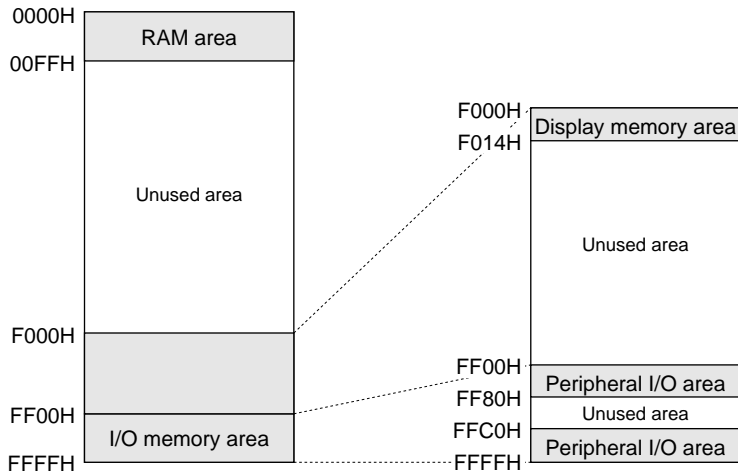


Fig. 4.1.1 Memory map

Note: Memory is not implemented in unused areas within the memory map. Further, some non-implementation areas and unused (access prohibition) areas exist in the peripheral I/O area. If the program that accesses these areas is generated, its operation cannot be guaranteed. Refer to the I/O memory maps shown in Tables 4.1.1 (a)–(d) for the peripheral I/O area.

Table 4.1.1 (a) I/O memory map (FF02H–FF52H)

Address	Register				Name	Init *1	1	0	Comment
	D3	D2	D1	D0					
FF02H	PRSM3	PRSM2	PRSM1	PRSM0	PRSM3	1			Prescaler setting Prescaler output $f_{PRS} = \frac{f_{OSC}}{2 \cdot (PRSM + 1)}$ PRSM setting condition: $240 \text{ Hz} < f_{OSC} / (2048 \cdot (PRSM + 1)) < 530 \text{ Hz}$
					PRSM2	1			
	R/W				PRSM1	1			
					PRSM0	1			
FF06H	FOUT	0	FOFQ1	FOFQ0	FOUT	0	Enable	Disable	FOUT output enable Unused [FOFQ1, 0] FOUT frequency selection $f_{OSC} = 4.19 \text{ MHz} \rightarrow 262 \text{ kHz}$ $\frac{f_{PRS}}{64}$ $\frac{f_{PRS}}{512}$
					0 *3	- *2			
	R/W	R	R/W		FOFQ1	0			
					FOFQ0	0			
FF07H	0	0	WDEN	WDRST	0 *3	- *2			Unused Unused Watchdog timer enable Watchdog timer reset (writing)
					0 *3	- *2			
	R		R/W	W	WDEN	1	Enable	Disable	
					WDRST*3	Reset	Reset	Invalid	
FF20H	SIK03	SIK02	SIK01	SIK00	SIK03	0	Enable	Disable	K00–K03 interrupt selection register
					SIK02	0	Enable	Disable	
	R/W				SIK01	0	Enable	Disable	
					SIK00	0	Enable	Disable	
FF21H	K03	K02	K01	K00	K03	- *2	High	Low	K00–K03 input port data
					K02	- *2	High	Low	
	R				K01	- *2	High	Low	
					K00	- *2	High	Low	
FF22H	KCP03	KCP02	KCP01	KCP00	KCP03	1			K00–K03 input comparison register
					KCP02	1			
	R/W				KCP01	1			
					KCP00	1			
FF30H	R03HIZ	R02HIZ	R01HIZ	R00HIZ	R03HIZ	0	High-Z	Output	R03/FOUT output high impedance control R02/PTOUT output high impedance control R01 output high impedance control R00 output high impedance control
					R02HIZ	0	High-Z	Output	
	R/W				R01HIZ	0	High-Z	Output	
					R00HIZ	0	High-Z	Output	
FF31H	R03	R02	R01	R00	R03	1	High	Low	R03 output port data (FOUTE=0) Fix at "1" when FOUT is used R02 output port data (PTOUT=0) Fix at "1" when PTOUT is used R01 output port data R00 output port data
					R02	1	High	Low	
	R/W				R01	1	High	Low	
					R00	1	High	Low	
FF48H	IOC23	IOC22	IOC21	IOC20	IOC23	0	Output	Input	P20–P23 I/O control register
					IOC22	0	Output	Input	
	R/W				IOC21	0	Output	Input	
					IOC20	0	Output	Input	
FF49H	PUL23	PUL22	PUL21	PUL20	PUL23	1	On	Off	P20–P23 pull-up control register
					PUL22	1	On	Off	
	R/W				PUL21	1	On	Off	
					PUL20	1	On	Off	
FF4AH	P23	P22	P21	P20	P23	- *2	High	Low	P20–P23 I/O port data
					P22	- *2	High	Low	
	R/W				P21	- *2	High	Low	
					P20	- *2	High	Low	
FF50H	IOC43	IOC42	IOC41	IOC40	IOC43	0	Output	Input	P43 I/O control (PAD3=0), general-purpose register (PAD3=1) P42 I/O control (PAD2=0), general-purpose register (PAD2=1) P41 I/O control (PAD1=0), general-purpose register (PAD1=1) P40 I/O control (PAD0=0), general-purpose register (PAD0=1)
					IOC42	0	Output	Input	
	R/W				IOC41	0	Output	Input	
					IOC40	0	Output	Input	
FF51H	PUL43	PUL42	PUL41	PUL40	PUL43	1	On	Off	P43 pull-up control (PAD3=0), general-purpose register (PAD3=1) P42 pull-up control (PAD2=0), general-purpose register (PAD2=1) P41 pull-up control (PAD1=0), general-purpose register (PAD1=1) P40 pull-up control (PAD0=0), general-purpose register (PAD0=1)
					PUL42	1	On	Off	
	R/W				PUL41	1	On	Off	
					PUL40	1	On	Off	
FF52H	P43	P42	P41	P40	P43	- *2	High	Low	P43 port data (PAD3=0), general-purpose register (PAD3=1) P42 port data (PAD2=0), general-purpose register (PAD2=1) P41 port data (PAD1=0), general-purpose register (PAD1=1) P40 port data (PAD0=0), general-purpose register (PAD0=1)
					P42	- *2	High	Low	
	R/W				P41	- *2	High	Low	
					P40	- *2	High	Low	

Remarks

- *1 Initial value at initial reset
- *2 Not set in the circuit
- *3 Constantly "0" when being read

Table 4.1.1 (b) I/O memory map (FF60H–FFD0H)

Address	Register				Name	Init *1	1	0	Comment
	D3	D2	D1	D0					
FF60H	LDUTY1	LDUTY0	0	LPWR	LDUTY1	0			LCD drive duty switch [LDUTY1, 0] 0 1 2, 3 Duty 1/4 1/3 1/2
	R/W		R	R/W	LDUTY0	0			
FF61H	0	ALOFF	ALON	STCD	LPWR	0	On	Off	LCD power On/Off
	R	R/W			ALOFF	0 *3	- *2		Unused
FF64H	0	ENON	BZFQ	BZON	ALON	0	All Off	Normal	LCD all OFF control
	R	R/W			STCD	0	All On	Normal	LCD all ON control
FF68H	ADRUN	ADCLK	CHS1	CHS0	ADRUN*3	0	Start	Invalid	A/D conversion control
	W	R/W			ADCLK	0	fosc/2	fprs	Input clock selection
FF69H	PAD3	PAD2	PAD1	PAD0	CHS1	0			Input channel selection [CHS1, 0] 0 1 2 3 Ch AD0 AD1 AD2 AD3
	R/W				CHS0	0			
FF6AH	ADDR3	ADDR2	ADDR1	ADDR0	PAD3	0	A/D	I/O	A/D-Ch3 enable (P43 terminal)
	R				PAD2	0	A/D	I/O	
FF6BH	ADDR7	ADDR6	ADDR5	ADDR4	PAD1	0	A/D	I/O	A/D-Ch1 enable (P41 terminal)
	R				PAD0	0	A/D	I/O	A/D-Ch0 enable (P40 terminal)
FFC0H	0	0	MODE1	MODE0	ADDR3	- *2			A/D conversion data (low-order 4 bits)
	R		R/W		ADDR2	- *2			
FFC1H	0	EVCNT	FCSEL	PLPOL	ADDR1	- *2			MSB
	R	R/W			ADDR0	- *2			
FFC2H	0	PTOUT	CHSEL1	CHSEL0	ADDR7	- *2			A/D conversion data (high-order 4 bits)
	R	R/W			ADDR6	- *2			
FFC4H	PTPS01	PTPS00	PTRST0	PTRUN0	ADDR5	- *2			A/D conversion data (high-order 4 bits)
	R/W		W	R/W	ADDR4	- *2			
FFC5H	PTPS11	PTPS10	PTRST1	PTRUN1	MODE1	0	16 bit	8 bit x 2	8/16 bits mode selection (Programmable timer 2, 3)
	R/W		W	R/W	MODE0	0	16 bit	8 bit x 2	
FFC6H	PTPS21	PTPS20	PTRST2	PTRUN2	MODE0	0	16 bit	8 bit x 2	8/16 bits mode selection (Programmable timer 0, 1)
	R/W		W	R/W	PTOUT	0	On	Off	
FFC7H	PTPS31	PTPS30	PTRST3	PTRUN3	CHSEL1	0			PTOUT output channel selection [CHSEL1, 0] 0 1 2 3 Output Ch Timer 0 Timer 1 Timer 2 Timer 3
	R/W		W	R/W	CHSEL0	0			
FFD0H	RLD03	RLD02	RLD01	RLD00	PTPS01	0			Timer 0 clock division ratio selection [PTPS01, 00] 0 1 2 3 Division ratio fosc/1 fosc/4 fosc/32 fosc/256
	R/W				PTPS00	0			
FFD0H	RLD03	RLD02	RLD01	RLD00	PTRST0*3	- *2	Reset	Invalid	Timer 0 reset (reload)
	R/W				PTRUN0	0	Run	Stop	Timer 0 Run/Stop
FFD0H	RLD03	RLD02	RLD01	RLD00	PTPS11	0			Timer 1 clock division ratio selection [PTPS11, 10] 0 1 2 3 Division ratio fosc/1 fosc/4 fosc/32 fosc/256
	R/W		W	R/W	PTPS10	0			
FFD0H	RLD03	RLD02	RLD01	RLD00	PTRST1*3	- *2	Reset	Invalid	Timer 1 reset (reload)
	R/W		W	R/W	PTRUN1	0	Run	Stop	Timer 1 Run/Stop
FFD0H	RLD03	RLD02	RLD01	RLD00	PTPS21	0			Timer 2 clock division ratio selection [PTPS21, 20] 0 1 2 3 Division ratio fosc/1 fosc/4 fosc/32 fosc/256
	R/W		W	R/W	PTPS20	0			
FFD0H	RLD03	RLD02	RLD01	RLD00	PTRST2*3	- *2	Reset	Invalid	Timer 2 reset (reload)
	R/W		W	R/W	PTRUN2	0	Run	Stop	Timer 2 Run/Stop
FFD0H	RLD03	RLD02	RLD01	RLD00	PTPS31	0			Timer 3 clock division ratio selection [PTPS31, 30] 0 1 2 3 Division ratio fosc/1 fosc/4 fosc/32 fosc/256
	R/W		W	R/W	PTPS30	0			
FFD0H	RLD03	RLD02	RLD01	RLD00	PTRST3*3	- *2	Reset	Invalid	Timer 3 reset (reload)
	R/W		W	R/W	PTRUN3	0	Run	Stop	Timer 3 Run/Stop
FFD0H	RLD03	RLD02	RLD01	RLD00	MSB				Programmable timer 0 reload data (low-order 4 bits)
	R/W				LSB				

Table 4.1.1 (c) I/O memory map (FFD1H–FFDFH)

Address	Register				Name	Init *1	1	0	Comment
	D3	D2	D1	D0					
FFD1H	RLD07	RLD06	RLD05	RLD04	RLD07	0			MSB Programmable timer 0 reload data (high-order 4 bits) LSB
	R/W				RLD06	0			
					RLD05	0			
					RLD04	0			
FFD2H	RLD13	RLD12	RLD11	RLD10	RLD13	0			MSB Programmable timer 1 reload data (low-order 4 bits) LSB
	R/W				RLD12	0			
					RLD11	0			
					RLD10	0			
FFD3H	RLD17	RLD16	RLD15	RLD14	RLD17	0			MSB Programmable timer 1 reload data (high-order 4 bits) LSB
	R/W				RLD16	0			
					RLD15	0			
					RLD14	0			
FFD4H	RLD23	RLD22	RLD21	RLD20	RLD23	0			MSB Programmable timer 2 reload data (low-order 4 bits) LSB
	R/W				RLD22	0			
					RLD21	0			
					RLD20	0			
FFD5H	RLD27	RLD26	RLD25	RLD24	RLD27	0			MSB Programmable timer 2 reload data (high-order 4 bits) LSB
	R/W				RLD26	0			
					RLD25	0			
					RLD24	0			
FFD6H	RLD33	RLD32	RLD31	RLD30	RLD33	0			MSB Programmable timer 3 reload data (low-order 4 bits) LSB
	R/W				RLD32	0			
					RLD31	0			
					RLD30	0			
FFD7H	RLD37	RLD36	RLD35	RLD34	RLD37	0			MSB Programmable timer 3 reload data (high-order 4 bits) LSB
	R/W				RLD36	0			
					RLD35	0			
					RLD34	0			
FFD8H	PTD03	PTD02	PTD01	PTD00	PTD03	0			MSB Programmable timer 0 data (low-order 4 bits) LSB
	R				PTD02	0			
					PTD01	0			
					PTD00	0			
FFD9H	PTD07	PTD06	PTD05	PTD04	PTD07	0			MSB Programmable timer 0 data (high-order 4 bits) LSB
	R				PTD06	0			
					PTD05	0			
					PTD04	0			
FFDAH	PTD13	PTD12	PTD11	PTD10	PTD13	0			MSB Programmable timer 1 data (low-order 4 bits) LSB
	R				PTD12	0			
					PTD11	0			
					PTD10	0			
FFDBH	PTD17	PTD16	PTD15	PTD14	PTD17	0			MSB Programmable timer 1 data (high-order 4 bits) LSB
	R				PTD16	0			
					PTD15	0			
					PTD14	0			
FFDCH	PTD23	PTD22	PTD21	PTD20	PTD23	0			MSB Programmable timer 2 data (low-order 4 bits) LSB
	R				PTD22	0			
					PTD21	0			
					PTD20	0			
FFDDH	PTD27	PTD26	PTD25	PTD24	PTD27	0			MSB Programmable timer 2 data (high-order 4 bits) LSB
	R				PTD26	0			
					PTD25	0			
					PTD24	0			
FFDEH	PTD33	PTD32	PTD31	PTD30	PTD33	0			MSB Programmable timer 3 data (low-order 4 bits) LSB
	R				PTD32	0			
					PTD31	0			
					PTD30	0			
FFDFH	PTD37	PTD36	PTD35	PTD34	PTD37	0			MSB Programmable timer 3 data (high-order 4 bits) LSB
	R				PTD36	0			
					PTD35	0			
					PTD34	0			

Table 4.1.1 (d) I/O memory map (FFE2H–FFF7H)

Address	Register				Name	Init *1	1	0	Comment
	D3	D2	D1	D0					
FFE2H	EIPT3	EIPT2	EIPT1	EIPT0	EIPT3	0	Enable	Mask	Interrupt mask register (Programmable timer 3)
	R/W				EIPT2	0	Enable	Mask	Interrupt mask register (Programmable timer 2)
	R/W				EIPT1	0	Enable	Mask	Interrupt mask register (Programmable timer 1)
	R/W				EIPT0	0	Enable	Mask	Interrupt mask register (Programmable timer 0)
FFE4H	0	0	0	EIK0	0 *3	– *2			Unused
	R				0 *3	– *2			Unused
	R				0 *3	– *2			Unused
	R				EIK0	0	Enable	Mask	Interrupt mask register (K00–K03)
FFE6H	0	0	0	EIT0	0 *3	– *2			Unused
	R				0 *3	– *2			Unused
	R				0 *3	– *2			Unused
	R				EIT0	0	Enable	Mask	Interrupt mask register (Clock timer 1 Hz)
FFE7H	0	0	0	EIAD	0 *3	– *2			Unused
	R				0 *3	– *2			Unused
	R				0 *3	– *2			Unused
	R				EIAD	0	Enable	Mask	Interrupt mask register (A/D converter)
FFF2H	IPT3	IPT2	IPT1	IPT0	IPT3	0	(R)	(R)	Interrupt factor flag (Programmable timer 3)
	R/W				IPT2	0	Yes	No	Interrupt factor flag (Programmable timer 2)
	R/W				IPT1	0	(W)	(W)	Interrupt factor flag (Programmable timer 1)
	R/W				IPT0	0	Reset	Invalid	Interrupt factor flag (Programmable timer 0)
FFF4H	0	0	0	IK0	0 *3	– *2	(R)	(R)	Unused
	R				0 *3	– *2	Yes	No	Unused
	R				0 *3	– *2	(W)	(W)	Unused
	R				IK0	0	Reset	Invalid	Interrupt factor flag (K00–K03)
FFF6H	0	0	0	IT0	0 *3	– *2	(R)	(R)	Unused
	R				0 *3	– *2	Yes	No	Unused
	R				0 *3	– *2	(W)	(W)	Unused
	R				IT0	0	Reset	Invalid	Interrupt factor flag (Clock timer 1 Hz)
FFF7H	0	0	0	IAD	0 *3	– *2	(R)	(R)	Unused
	R				0 *3	– *2	Yes	No	Unused
	R				0 *3	– *2	(W)	(W)	Unused
	R				IAD	0	Reset	Invalid	Interrupt factor flag (A/D converter)

4.2 Oscillation Circuit and Prescaler

4.2.1 Configuration of oscillation circuit

The E0C63256 has a built-in oscillation circuit that supplies the operation clock to the CPU and peripheral circuits.

As a kind of oscillation circuit, either crystal/ceramic oscillation, CR oscillation or external clock input can be selected by mask option. The oscillation circuit supports 0.5 MHz to 4.5 MHz (Max. 2.5 MHz in CR oscillation) of oscillation frequency. To generate the operation clocks for the peripheral circuit from this wide frequency range, a prescaler is provided at the last stage of the oscillation circuit. The division ratio of the prescaler can be set according to the oscillation frequency with software. Figure 4.2.1.1 is the block diagram of this oscillation system.

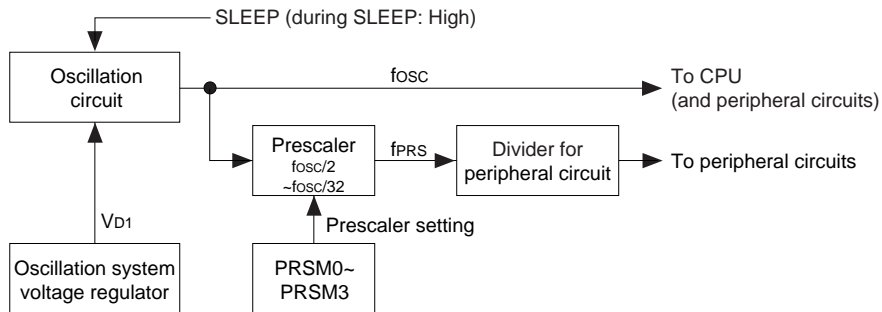


Fig. 4.2.1.1 Oscillation system block diagram

4.2.2 Kind of oscillation circuit

As a kind of oscillation circuit, either crystal/ceramic oscillation, CR oscillation or external clock input can be selected by mask option. The oscillation frequency range is 0.5 MHz to 2.5 MHz in CR oscillation and 0.5 MHz to 4.5 MHz in other types. This oscillation circuit stops in the SLEEP mode.

Note: A 4.194304 MHz crystal oscillator is recommended when using as a clock function.

(1) Crystal/ceramic oscillation circuit

As shown in Figure 4.2.2.1, the crystal oscillation circuit can be configured simply by connecting a crystal oscillator (X'tal) and a feedback resistor (R_f) between the OSC3 and OSC4 terminals, the gate capacitor (C_G) between the OSC3 and VSS terminals, and the drain capacitor (C_D) between the OSC4 and VSS terminals.

In the case of ceramic oscillation, connect a ceramic oscillator between the OSC3 and OSC4 terminals instead of a crystal oscillator.

See Chapter 7, "Electrical Characteristic" for the recommended values of each element.

(2) CR oscillation circuit

As shown in Figure 4.2.2.2, the CR oscillation circuit can be configured simply by connecting the resistor R_{CR} between the OSC3 and OSC4 terminals. See Chapter 7, "Electrical Characteristics" for resistance value of R_{CR} .

(3) External clock input

When external clock input is selected, open the OSC4 terminal and input a square wave clock to the OSC3 terminal.

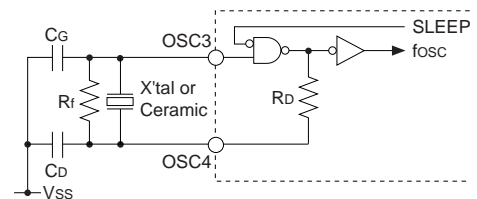


Fig. 4.2.2.1 Crystal/ceramic oscillation circuit

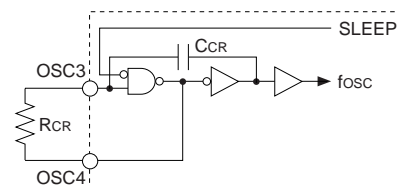


Fig. 4.2.2.2 CR oscillation circuit

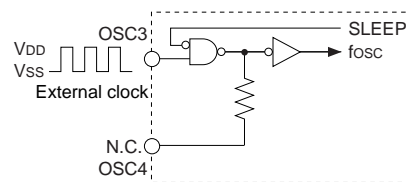


Fig. 4.2.2.3 External clock input

4.2.3 Prescaler

To adopt 0.5 MHz to 4.5 MHz of oscillation frequency, a prescaler is provided at the last stage of the oscillation circuit. The prescaler sets the operating clocks of the peripheral circuits in a fixed range. The division ratio of the prescaler can be set using the PRSM register as shown in Table 4.2.3.1.

Table 4.2.3.1 Division ratio of prescaler

PRSM3	PRSM2	PRSM1	PRSM0	fPRS	PRSM3	PRSM2	PRSM1	PRSM0	fPRS
1	1	1	1	fosc/32	0	1	1	1	fosc/16
1	1	1	0	fosc/30	0	1	1	0	fosc/14
1	1	0	1	fosc/28	0	1	0	1	fosc/12
1	1	0	0	fosc/26	0	1	0	0	fosc/10
1	0	1	1	fosc/24	0	0	1	1	fosc/8
1	0	1	0	fosc/22	0	0	1	0	fosc/6
1	0	0	1	fosc/20	0	0	0	1	fosc/4
1	0	0	0	fosc/18	0	0	0	0	fosc/2

fPRS: Prescaler output clock frequency = fosc/2n (n: PRSM setting value + 1)
 fosc: Oscillation clock frequency

The division ratio should be set so that it meets the following condition.

$$240 \text{ Hz} < \frac{f_{osc}}{2048 \cdot n} < 530 \text{ Hz} \quad (n: \text{PRSM setting value} + 1)$$

Examples

In case of fosc = 4.194304 MHz: fosc / (2048 • 8) = 256 Hz PRSM = 7 fPRS = 262.144 kHz

In case of fosc = 2 MHz: fosc / (2048 • 4) = 244 Hz PRSM = 3 fPRS = 250 kHz

Note: It is necessary to take into consideration frequency deviation of fosc. The examples do not. See Chapter 7, "Electrical Characteristic" for frequency deviation.

The peripheral circuits that are affected with the setting of the prescaler are as follows:

- Clock timer and watchdog timer (Count clock)
- LCD driver (Frame frequency)
- Buzzer output circuit (Buzzer frequency, 2 Hz interval)
- Special output of output port (FOUT frequency)
- Initial reset circuit (Time authorize circuit, noise rejector)
- Programmable timer (Noise rejector, data hold time)
- A/D conversion clock

The operation clocks of these peripheral circuits are generated by dividing the output clock of the prescaler (fPRS). Table 4.2.3.2 shows examples of division ratio and clock frequency of each peripheral circuit. Examples of 4.19 MHz are showing the PRSM set to 7, and examples of 2 MHz are showing the PRSM set to 3.

Table 4.2.3.2 Clock frequency for peripheral circuit

Peripheral circuit/Signal	Division ratio	Frequency/Time	
		fosc=4.194304 MHz	fosc=2 MHz
Clock timer count clock	fPRS/1024	256 Hz	244 Hz
Clock timer 1 Hz interrupt (WDT clock)	fPRS/262144	1 Hz	0.95 Hz
Watchdog timer reset cycle Min.	786432/fPRS	3 sec	3.15 sec
Watchdog timer reset cycle Max.	1048576/fPRS	4 sec	4.19 sec
LCD driver frame frequency (1/4, 1/2 duty)	fPRS/4096	64 Hz	61.0 Hz
LCD driver frame frequency (1/3 duty)	fPRS/3072	85.3 Hz	81.4 Hz
Buzzer signal (2 kHz)	fPRS/128	2048 Hz	1953 Hz
Buzzer signal (4 kHz)	fPRS/64	4096 Hz	3906 Hz
Buzzer 2 Hz interval signal	fPRS/131072	2 Hz	1.9 Hz
FOUT frequency 0	fosc	4.194304 MHz	2 MHz
FOUT frequency 1	fPRS	262.144 kHz	250 kHz
FOUT frequency 2	fPRS/64	4096 Hz	3906 Hz
FOUT frequency 3	fPRS/512	512 Hz	488 Hz
Initial reset noise rejection pulse width	128/fPRS	0.49 msec	0.51 msec
Authorization time for simultaneous input reset Min.	262144/fPRS	1 sec	1.05 sec
Authorization time for simultaneous input reset Max.	524288/fPRS	2 sec	2.1 sec
Programmable timer noise rejection pulse width	128/fPRS	0.49 msec	0.51 msec
Programmable timer data hold time (8 bits)	128/fPRS	0.49 msec	0.51 msec
Programmable timer data hold time (16 bits)	256/fPRS	0.98 msec	1.02 msec
A/D converter clock	fPRS	262.144 kHz	250 kHz

4.2.4 Clock frequency and instruction execution time

The CPU operates with the oscillation clock f_{osc} .

Table 4.2.4.1 shows the instruction execution time according to frequency.

Table 4.2.4.1 Clock frequency and instruction execution time

Clock frequency	Instruction execution time (μsec)		
	1-cycle instruction	2-cycle instruction	3-cycle instruction
4.194304 MHz	0.48	0.95	1.43
2 MHz	1	2	3

4.2.5 I/O memory of prescaler

Table 4.2.5.1 shows the I/O addresses and the control bits for the prescaler.

Table 4.2.5.1 Control bits of prescaler

Address	Register				Name	Init *1	1	0	Comment
	D3	D2	D1	D0					
FF02H	PRSM3	PRSM2	PRSM1	PRSM0	PRSM3	1			Prescaler setting Prescaler output $f_{PRS} = \frac{f_{osc}}{2 \cdot (\text{PRSM} + 1)}$ PRSM setting condition: $240 \text{ Hz} < f_{osc}/(2048 \cdot (\text{PRSM} + 1)) < 530 \text{ Hz}$
					PRSM2	1			
	R/W				PRSM1	1			
					PRSM0	1			

*1 Initial value at initial reset

*2 Not set in the circuit

*3 Constantly "0" when being read

PRSM3–PRSM0: Prescaler setting register (FF02H)

Sets a division ratio of the prescaler.

Table 4.2.5.2 Prescaler setting

PRSM3	PRSM2	PRSM1	PRSM0	f_{PRS}	PRSM3	PRSM2	PRSM1	PRSM0	f_{PRS}
1	1	1	1	$f_{osc}/32$	0	1	1	1	$f_{osc}/16$
1	1	1	0	$f_{osc}/30$	0	1	1	0	$f_{osc}/14$
1	1	0	1	$f_{osc}/28$	0	1	0	1	$f_{osc}/12$
1	1	0	0	$f_{osc}/26$	0	1	0	0	$f_{osc}/10$
1	0	1	1	$f_{osc}/24$	0	0	1	1	$f_{osc}/8$
1	0	1	0	$f_{osc}/22$	0	0	1	0	$f_{osc}/6$
1	0	0	1	$f_{osc}/20$	0	0	0	1	$f_{osc}/4$
1	0	0	0	$f_{osc}/18$	0	0	0	0	$f_{osc}/2$

Select one according to the oscillation frequency.

When the oscillation frequency is 4.194304 MHz, set to 7 (0111B) to use the clock timer as a clock function.

Refer to Section 4.2.3 for details.

At initial reset, this register is set to "1111B".

4.2.6 Programming note

The peripheral circuits may not operate normally if the prescaler is not set properly.

4.3 Input Ports (K00–K03)

4.3.1 Configuration of input ports

The E0C63256 has four bits general-purpose input ports. Each of the input port terminals (K00–K03) provides internal pull-up resistor. Pull-up resistor can be selected for each bit with the mask option. Figure 4.3.1.1 shows the configuration of input port.

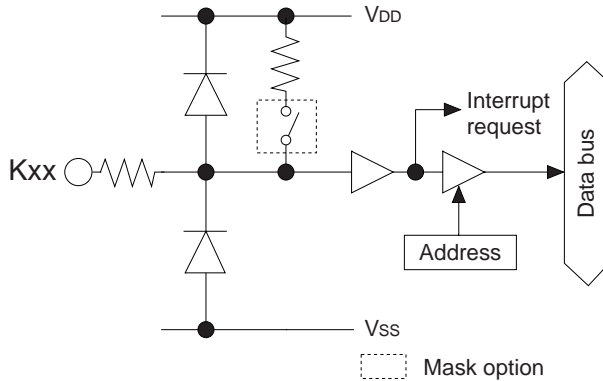


Fig. 4.3.1.1 Configuration of input port

Selection of "With pull-up resistor" with the mask option suits input from the push switch, key matrix, and so forth. When "Gate direct" is selected, the port can be used for slide switch input and interfacing with other LSIs.

4.3.2 Interrupt function

All four bits of the input ports (K00–K03) provide the interrupt function. The conditions for issuing an interrupt can be set by the software. Further, whether to mask the interrupt function can be selected by the software. The input port interrupts are also used for releasing the SLEEP mode.

Figure 4.3.2.1 shows the configuration of K00–K03 interrupt circuit.

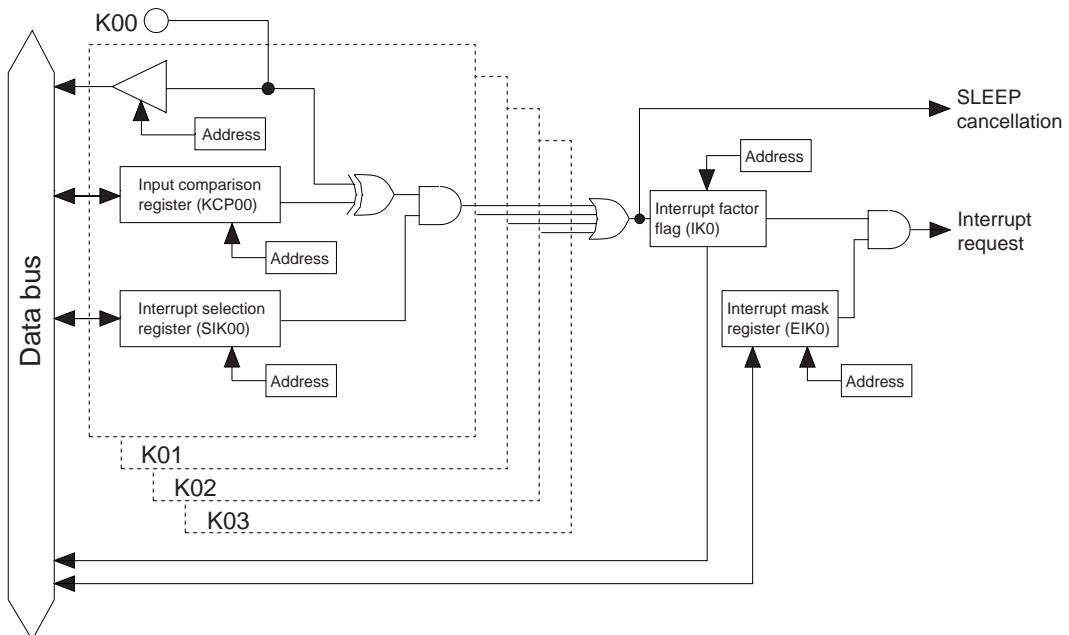


Fig. 4.3.2.1 Input interrupt circuit configuration

The interrupt selection register (SIK) and input comparison register (KCP) are individually set for the input ports K00–K03, and can specify the terminals for generating interrupt and interrupt timing. The interrupt selection registers (SIK00–SIK03) select what input of K00–K03 to use for the interrupt. Writing "1" into an interrupt selection register incorporates that input port into the interrupt generation conditions. The changing the input port where the interrupt selection register has been set to "0" does not affect the generation of the interrupt.

The input interrupt timing can select that the interrupt be generated at the rising edge of the input or that it be generated at the falling edge according to the set value of the input comparison registers (KCP00–KCP03).

By setting these two conditions, the interrupt for K00–K03 is generated when input ports in which an interrupt has been enabled by the input selection registers and the contents of the input comparison registers have been changed from matching to no matching.

The interrupt mask register (EIK0) enable the interrupt mask to be selected for K00–K03.

When the interrupt is generated, the interrupt factor flag (IK0) is set to "1".

Figure 4.3.2.2 shows an example of an interrupt for K00–K03.

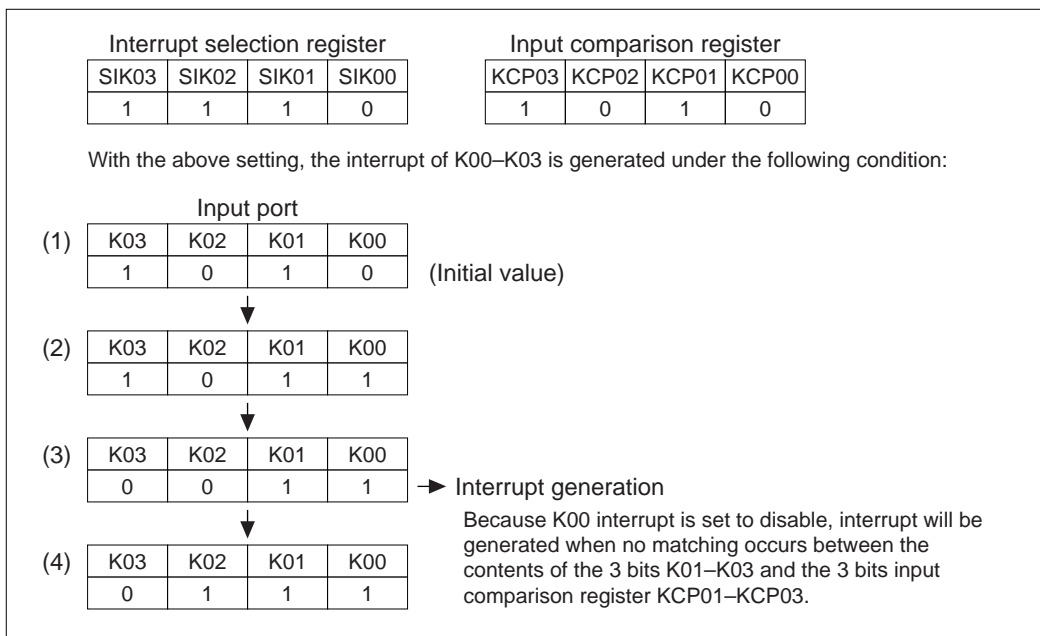


Fig. 4.3.2.2 Example of interrupt of K00–K03

K00 interrupt is disabled by the interrupt selection register (SIK00), so that an interrupt does not occur at (2). At (3), K03 changes to "0"; the data of the terminals that are interrupt enabled no longer match the data of the input comparison registers, so that interrupt occurs. As already explained, the condition for the interrupt to occur is the change in the port data and contents of the input comparison registers from matching to no matching. Hence, in (4), when the no matching status changes to another no matching status, an interrupt does not occur. Further, terminals that have been masked for interrupt do not affect the conditions for interrupt generation.

4.3.3 Mask option

Internal pull-up resistor can be selected for each of the four bits of the input ports (K00–K03) with the input port mask option.

When "Gate direct" is selected, take care that the floating status does not occur for the input. Select "With pull-up resistor" for input ports that are not being used.

4.3.4 I/O memory of input ports

Table 4.3.4.1 shows the I/O addresses and the control bits for the input ports.

Table 4.3.4.1 Control bits of input ports

Address	Register								Comment
	D3	D2	D1	D0	Name	Init *1	1	0	
FF20H	SIK03	SIK02	SIK01	SIK00	SIK03	0	Enable	Disable	K00–K03 interrupt selection register
					SIK02	0	Enable	Disable	
	R/W				SIK01	0	Enable	Disable	
	R/W				SIK00	0	Enable	Disable	
FF21H	K03	K02	K01	K00	K03	– *2	High	Low	K00–K03 input port data
					K02	– *2	High	Low	
	R				K01	– *2	High	Low	
	R				K00	– *2	High	Low	
FF22H	KCP03	KCP02	KCP01	KCP00	KCP03	1	↓	↑	K00–K03 input comparison register
					KCP02	1	↓	↑	
	R/W				KCP01	1	↓	↑	
	R/W				KCP00	1	↓	↑	
FFE4H	0	0	0	EIK0	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R				0 *3	– *2			Unused
	R/W				EIK0	0	Enable	Mask	Interrupt mask register (K00–K03)
FFF4H	0	0	0	IK0	0 *3	– *2	(R)	(R)	Unused
					0 *3	– *2	Yes	No	Unused
	R				0 *3	– *2	(W)	(W)	Unused
	R/W				IK0	0	Reset	Invalid	Interrupt factor flag (K00–K03)

*1 Initial value at initial reset
 *2 Not set in the circuit
 *3 Constantly "0" when being read

K00–K03: K0 port input port data (FF21H)

Input data of the input port terminals can be read with these registers.

- When "1" is read: High level
- When "0" is read: Low level
- Writing: Invalid

The reading is "1" when the terminal voltage of the four bits of the input ports (K00–K03) goes high (VDD), and "0" when the voltage goes low (VSS).

These bits are dedicated for reading, so writing cannot be done.

SIK00–SIK03: K0 port interrupt selection register (FF20H)

Selects the ports to be used for the K00–K03 input interrupts.

- When "1" is written: Enable
- When "0" is written: Disable
- Reading: Valid

Enables the interrupt for the input ports (K00–K03) for which "1" has been written into the interrupt selection registers (SIK00–SIK03). The input port set for "0" does not affect the interrupt generation condition.

At initial reset, this register is set to "0".

Note: The interrupt of the input port that is used for releasing SLEEP mode must be enabled by writing "1" to the interrupt selection register before executing the SLP instruction.

KCP00–KCP03: K0 port input comparison register (FF22H)

Interrupt conditions for terminals K00–K03 can be set with these registers.

When "1" is written: Falling edge

When "0" is written: Rising edge

Reading: Valid

The interrupt conditions can be set for the rising or falling edge of input for each of the four bits (K00–K03), through the input comparison registers (KCP00–KCP03).

Comparison is done only with the ports that are enabled by the interrupt among K00–K03 by means of the SIK00–SIK03 registers.

At initial reset, this register is set to "1111B".

EIK0: K0 input interrupt mask register (FFE4H•D0)

Masking the interrupt of the input port can be selected with this register.

When "1" is written: Enable

When "0" is written: Mask

Reading: Valid

With this register, masking of the input port interrupt can be selected.

At initial reset, this register is set to "0".

Note: Since an input port interrupt is used to release SLEEP mode, the input interrupt must be enabled by this register before executing the SLP instruction.

IK0: K0 input interrupt factor flag (FFF4H•D0)

This flag indicates the occurrence of input interrupt.

When "1" is read: Interrupt has occurred

When "0" is read: Interrupt has not occurred

When "1" is written: Flag is reset

When "0" is written: Invalid

The interrupt factor flag IK0 is associated with K00–K03. From the status of this flag, the software can decide whether an input interrupt has occurred.

The interrupt factor flag is set to "1" when the interrupt condition is established regardless of the interrupt mask register setting. However, the interrupt does not occur to the CPU when the interrupt is masked.

This flag is reset to "0" by writing "1".

After an interrupt occurs, the same interrupt will occur again if the interrupt enabled state (I flag = "1") is set or the RETI instruction is executed unless the interrupt factor flag is reset. Therefore, be sure to reset (write "1" to) the interrupt factor flag in the interrupt service routine before shifting to the interrupt enabled state.

At initial reset, this flag is set to "0".

4.3.5 Programming notes

- (1) When input ports are changed from low to high by pull-up resistors, the rise of the waveform is delayed on account of the time constant of the pull-up resistor and input gate capacitance. Hence, when fetching input ports, set an appropriate waiting time.

Particular care needs to be taken of the key scan during key matrix configuration.

Make this waiting time the amount of time or more calculated by the following expression.

Waiting time = $R_{IN} \times (C_{IN} + C_L) \times 1.6$ [sec]

R_{IN}: Pull-up resistance Max. value

C_{IN}: Terminal capacitance Max. value

C_L: Load capacitance on the board

- (2) The K03 terminal functions as the clock input terminal for the programmable timer, and the input signal is shared with the input port and the programmable timer. Therefore, when the K03 terminal is set to the clock input terminal for the programmable timer, take care of the interrupt setting.
- (3) After an interrupt occurs, the same interrupt will occur again if the interrupt enabled state (I flag = "1") is set or the RETI instruction is executed unless the interrupt factor flag is reset. Therefore, be sure to reset (write "1" to) the interrupt factor flag in the interrupt service routine before shifting to the interrupt enabled state.

4.4 Output Ports (R00–R03)

4.4.1 Configuration of output ports

The E0C63256 has 4 bits general output ports.

Output specifications of the output ports can be selected individually with the mask option. Two kinds of output specifications are available: complementary output and N-channel open drain output.

Figure 4.4.1.1 shows the configuration of the output port.

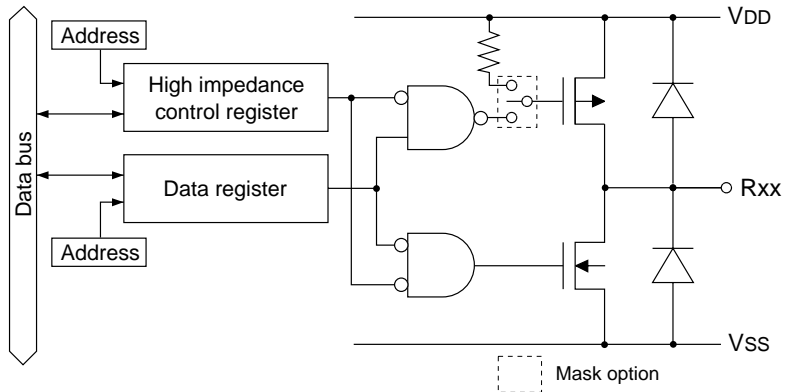


Fig. 4.4.1.1 Configuration of output port

The R02 and R03 output terminals are shared with special output terminals (PTOUT, FOUT), and this function is selected by the software.

At initial reset, these are all set to the general purpose output port.

Table 4.4.1.1 shows the setting of the output terminals by function selection.

Table 4.4.1.1 Function setting of output terminals

Terminal name	Terminal status at initial reset	Special output	
		PTOUT	FOUT
R00	R00 (High output)	R00	R00
R01	R01 (High output)	R01	R01
R02	R02 (High output)	PTOUT	
R03	R03 (High output)		FOUT

When using the output port (R02, R03) as the special output port, the data register must be fixed at "1" and the high impedance control register must be fixed at "0" (data output).

4.4.2 Mask option

Output specifications of the output ports can be selected with the mask option.

The output specifications of the output ports R00–R03 can be selected from either complementary output or N-channel open drain output individually (in 1-bit units).

This mask option is effective even when the output port (R02, R03) is used for special output port.

However, when N-channel open drain output is selected, do not apply a voltage exceeding the power supply voltage to the output port.

4.4.3 High impedance control

The terminal output status of each output port can be set to a high impedance status using the high impedance control register.

When "1" is written to the high impedance control register, the corresponding output port terminal goes to high impedance status. When "0" is written, the port outputs a signal according to the data register.

4.4.4 Special output

In addition to the regular DC output, special output can be selected for the output ports R02 and R03 as shown in Table 4.4.4.1 with the software.

Figure 4.4.4.1 shows the configuration of the R02 and R03 output ports.

Table 4.4.4.1 Special output

Terminal	Special output	Output control register
R03	FOUT	FOUT
R02	PTOUT	PTOUT

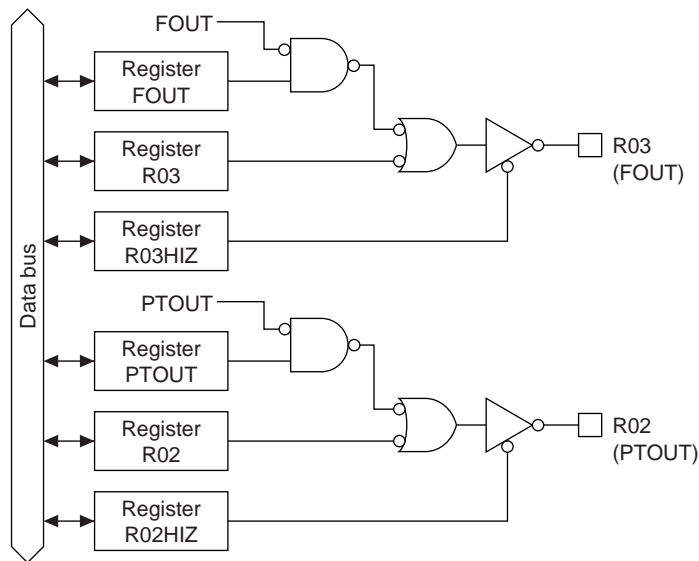


Fig. 4.4.4.1 Configuration of R02 and R03 output ports

At initial reset, the output port data register is set to "1" and the high impedance control register is set to "0". Consequently, the output terminal goes high (VDD).

When using the output port (R02, R03) as the special output port, fix the data register (R02, R03) at "1" and the high impedance control register (R02HIZ, R03HIZ) at "0" (data output). The respective signal should be turned ON and OFF using the special output control register.

- Note:
- Be aware that the output terminal is fixed at a low (Vss) level the same as the DC output if "0" is written to the R02 and R03 registers when the special output has been selected.
 - Be aware that the output terminal shifts into high impedance status when "1" is written to the high impedance control register (R02HIZ, R03HIZ).

• **PTOUT (R02)**

The R02 terminal can output the PTOUT signal.

The PTOUT signal is the clock that is output from the programmable timer, and can be used to provide a clock signal to an external device.

To output the PTOUT signal, fix the R02 register at "1" and the R02HIZ register at "0", and turn the signal ON and OFF using the PTOUT register. It is, however, necessary to control the programmable timer.

Refer to Section 4.8, "Programmable Timer" for details of the programmable timer.

Note: A hazard may occur when the PTOUT signal is turned ON and OFF.

Figure 4.4.4.2 shows the output waveform of the PTOUT signal.

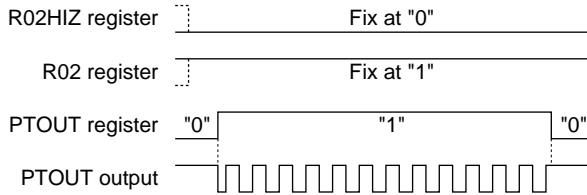


Fig. 4.4.4.2 Output waveform of PTOUT signal

• **FOUT (R03)**

The R03 terminal can output the FOUT signal.

The FOUT signal is the oscillation clock (fosc) or a clock that the prescaler output (fPRS) has divided, and can be used to provide a clock signal to external devices.

To output the FOUT signal, fix the R03 register at "1" and the R03HIZ register at "0", and turn the signal ON and OFF using the FOUT register.

The frequency of the output clock may be selected from among 4 types shown in Table 4.4.4.2 by setting the FOFQ0 and FOFQ1 registers.

Table 4.4.4.2 FOUT clock frequency

FOFQ1	FOFQ0	Clock frequency		
		Division ratio	fosc = 4.194304 MHz PRSM = 7	fosc = 2 MHz PRSM = 3
1	1	fosc	4.194304 MHz	2 MHz
1	0	fPRS	262.144 kHz	250 kHz
0	1	fPRS/64	4096 Hz	3906 Hz
0	0	fPRS/512	512 Hz	488 Hz

fosc: Oscillation clock
fPRS: Prescaler output clock

The FOUT frequency varies according to the oscillation frequency and setting of the prescaler (PRSM register). Refer to Section 4.2, "Oscillation Circuit and Prescaler", for setting of the prescaler.

Note: A hazard may occur when the FOUT signal is turned ON and OFF.

Figure 4.4.4.3 shows the output waveform of the FOUT signal.

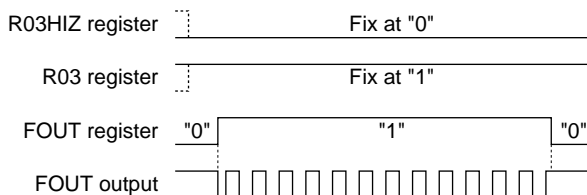


Fig. 4.4.4.3 Output waveform of FOUT signal

4.4.5 I/O memory of output ports

Table 4.4.5.1 shows the I/O addresses and control bits for the output ports.

Table 4.4.5.1 Control bits of output ports

Address	Register								Comment
	D3	D2	D1	D0	Name	Init *1	1	0	
FF06H	FOUT	0	FOFQ1	FOFQ0	FOUT 0 *3	0 - *2	Enable	Disable	FOUT output enable Unused [FOFQ1, 0] 0 1 2 3 FOUT Frequency fosc fPRS $\frac{fPRS}{64}$ $\frac{fPRS}{512}$ frequency selection fosc = 4.19 MHz → 262 kHz 4 kHz 512 Hz
	R/W	R	R/W		FOFQ1 FOFQ0	0 0			
FF30H	R03HIZ	R02HIZ	R01HIZ	R00HIZ	R03HIZ	0	High-Z	Output	R03/FOUT output high impedance control R02/PTOUT output high impedance control R01 output high impedance control R00 output high impedance control
	R/W				R02HIZ	0	High-Z	Output	
	R/W				R01HIZ	0	High-Z	Output	
	R/W				R00HIZ	0	High-Z	Output	
FF31H	R03	R02	R01	R00	R03	1	High	Low	R03 output port data (FOUTE=0) Fix at "1" when FOUT is used R02 output port data (PTOUT=0) Fix at "1" when PTOUT is used R01 output port data R00 output port data
	R/W				R02	1	High	Low	
	R/W				R01	1	High	Low	
	R/W				R00	1	High	Low	
FFC2H	0	PTOUT	CHSEL1	CHSEL0	0 *3	- *2			Unused PTOUT output control PTOUT output [CHSEL1, 0] 0 1 2 3 channel selection Output Ch Timer 0 Timer 1 Timer 2 Timer 3
	R/W				PTOUT	0	On	Off	
	R/W				CHSEL1	0			
	R/W				CHSEL0	0			

- *1 Initial value at initial reset
- *2 Not set in the circuit
- *3 Constantly "0" when being read

R00HIZ–R03HIZ: R0 port high impedance control register (FF30H)

Controls high impedance output of the output port.

- When "1" is written: High impedance
- When "0" is written: Data output
- Reading: Valid

By writing "0" to the high impedance control register, the corresponding output terminal outputs according to the data register. When "1" is written, it shifts into high impedance status.

When the output ports R02 and R03 are used for special output (PTOUT, FOUT), fix the R02HIZ register and the R03HIZ register at "0" (data output).

At initial reset, these registers are set to "0".

R00–R03: R0 output port data register (FF31H)

Set the output data for the output ports.

- When "1" is written: High level output
- When "0" is written: Low level output
- Reading: Valid

The output port terminals output the data written in the corresponding data registers without changing it. When "1" is written to the register, the output port terminal goes high (VDD), and when "0" is written, the output port terminal goes low (VSS).

When the output ports R02 and R03 are used for special output (PTOUT, FOUT), fix the R02 register and the R03 register at "1".

At initial reset, these registers are all set to "1".

FOUT: FOUT output control register (FF06H•D3)

Controls the FOUT output.

When "1" is written: FOUT output ON
 When "0" is written: FOUT output OFF
 Reading: Valid

By writing "1" to the FOUT register when the R03 register has been set to "1" and the R03HIZ register has been set to "0", the FOUT signal is output from the R03 terminal. When "0" is written, the R03 terminal goes high (VDD).

When using the R03 output port for DC output, fix this register at "0".

At initial reset, this register is set to "0".

FOFQ0, FOFQ1: FOUT frequency selection register (FF06H•D0, D1)

Selects a frequency of the FOUT signal.

Table 4.4.5.2 FOUT clock frequency

FOFQ1	FOFQ0	Clock frequency		
		Division ratio	fosc = 4.194304 MHz PRSM = 7	fosc = 2 MHz PRSM = 3
1	1	fosc	4.194304 MHz	2 MHz
1	0	fPRS	262.144 kHz	250 kHz
0	1	fPRS/64	4096 Hz	3906 Hz
0	0	fPRS/512	512 Hz	488 Hz

The FOUT frequency varies according to the oscillation frequency and setting of the prescaler (PRSM register). Refer to Section 4.2, "Oscillation Circuit and Prescaler", for setting of the prescaler.

At initial reset, this register is set to "0".

PTOUT: PTOUT output control register (FFC2H•D2)

Controls the PTOUT output.

When "1" is written: PTOUT output ON
 When "0" is written: PTOUT output OFF
 Reading: Valid

By writing "1" to the PTOUT register when the R02 register has been set to "1" and the R02HIZ register has been set to "0", the PTOUT signal is output from the R02 terminal. When "0" is written, the R02 terminal goes high (VDD). However, it is necessary that the programmable timer has output the PTOUT signal.

When using the R02 output port for DC output, fix this register at "0".

At initial reset, this register is set to "0".

4.4.6 Programming notes

- (1) When using the output port (R02, R03) as the special output port, fix the data register (R02, R03) at "1" and the high impedance control register (R02HIZ, R03HIZ) at "0" (data output).
 Be aware that the output terminal is fixed at a low (Vss) level the same as the DC output if "0" is written to the R02 and R03 registers when the special output has been selected.
 Be aware that the output terminal shifts into high impedance status when "1" is written to the high impedance control register (R02HIZ, R03HIZ).
- (2) A hazard may occur when the FOUT signal and the PTOUT signal are turned ON and OFF.
- (3) The FOUT frequency varies according to the oscillation frequency and setting of the prescaler (PRSM register). Refer to Section 4.2, "Oscillation Circuit and Prescaler", for setting of the prescaler.

4.5 I/O Ports (P20–P23 and P40–P43)

4.5.1 Configuration of I/O ports

The E0C63256 has 8 bits general-purpose I/O ports. Figure 4.5.1.1 shows the configuration of the I/O port.

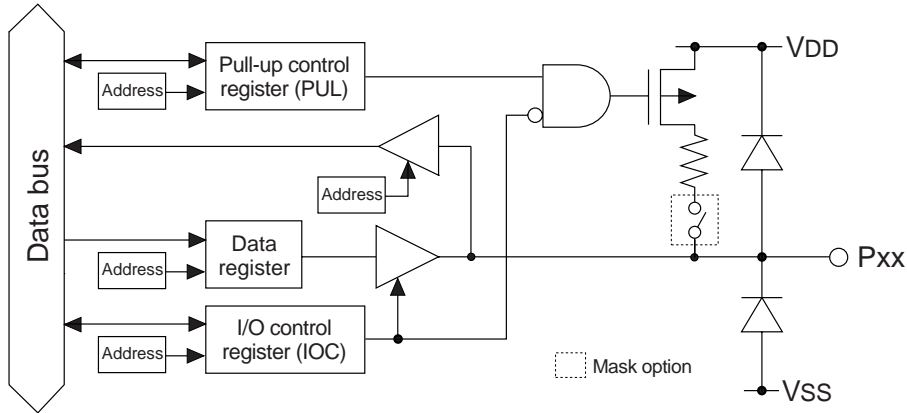


Fig. 4.5.1.1 Configuration of I/O port

The P40–P43 I/O port terminals are shared with the A/D converter input terminals and this function is selected by the software.

At initial reset, these are all set to the I/O port.

Table 4.5.1.1 shows the setting of the input/output terminals by function selection.

Table 4.5.1.1 Function setting of input/output terminals

Terminal name	Terminal status at initial reset	When A/D converter is used
P20–P23	P20–P23 (Input & pull-up *)	P20–P23
P40	P40 (Input & pull-up *)	AD0 (I)
P41	P41 (Input & pull-up *)	AD1 (I)
P42	P42 (Input & pull-up *)	AD2 (I)
P43	P43 (Input & pull-up *)	AD3 (I)

* When "with pull-up resistor" is selected by the mask option (high impedance when "gate direct" is set)

When these ports are used as I/O ports, the ports can be set to either input mode or output mode (in 1-bit unit). Modes can be set by writing data to the I/O control registers.

Refer to Section 4.10, "A/D Converter", for control of the A/D converter.

4.5.2 Mask option

Output specification for the output mode and addition of pull-up resistors can be selected as the terminal specification of the I/O port. Two selection items are available: complementary output and N-channel open drain output.

When N-channel open drain output is selected, do not supply a voltage exceeding the power supply voltage to the port.

Furthermore, a pull-up resistor can be added to each terminal by mask option.

When "without pull-up" is selected, take care that the floating status does not occur in the input mode. Select "Gate Direct" for the terminals that are used for A/D input among P40–P43.

These options can be selected individually in each port.

4.5.3 I/O control registers and input/output mode

Input or output mode can be set for the I/O ports by writing data into the I/O control registers IOCxx. This setting can be done individually in each port.

To set the input mode, write "0" to the I/O control register. When an I/O port is set to input mode, it becomes high impedance status and works as an input port.

However, when the pull-up explained in the following section has been set by software, the input line is pulled up only during this input mode.

To set the output mode, write "1" to the I/O control register. When an I/O port is set to output mode, it works as an output port, it outputs a high level (VDD) when the port output data is "1", and a low level (Vss) when the port output data is "0".

If perform the read out in each mode; when output mode, the register value is read out, and when input mode, the port value is read out.

At initial reset, the I/O control registers are set to "0", and the I/O ports enter the input mode.

Ports set as the inputs of the A/D converter (P40–P43) are fixed as input. In this case, the I/O control registers can be used as general purpose registers that do not affect the I/O control.

4.5.4 Pull-up during input mode

For the I/O ports of the E0C63256, pull-up resistors that are effective in the input mode can be added by mask option.

The pull-up resistor becomes effective by writing "1" to the pull-up control register PULxx that corresponds to each port, and the input line is pulled up during the input mode. When "0" has been written, no pull-up is done.

At initial reset, the pull-up control registers are set to "1".

The pull-up control registers of the ports in which "without pull-up" have been selected can be used as general purpose registers.

4.5.5 I/O memory of I/O ports

Table 4.5.5.1 show the I/O addresses and the control bits for the I/O ports.

Table 4.5.5.1 Control bits of I/O ports

Address	Register								Comment
	D3	D2	D1	D0	Name	Init *1	1	0	
FF48H	IOC23	IOC22	IOC21	IOC20	IOC23	0	Output	Input	P20–P23 I/O control register
	R/W				IOC22	0	Output	Input	
					IOC21	0	Output	Input	
					IOC20	0	Output	Input	
FF49H	PUL23	PUL22	PUL21	PUL20	PUL23	1	On	Off	P20–P23 pull-up control register
	R/W				PUL22	1	On	Off	
					PUL21	1	On	Off	
					PUL20	1	On	Off	
FF4AH	P23	P22	P21	P20	P23	– *2	High	Low	P20–P23 I/O port data
	R/W				P22	– *2	High	Low	
					P21	– *2	High	Low	
					P20	– *2	High	Low	
FF50H	IOC43	IOC42	IOC41	IOC40	IOC43	0	Output	Input	P43 I/O control (PAD3=0), general-purpose register (PAD3=1) P42 I/O control (PAD2=0), general-purpose register (PAD2=1) P41 I/O control (PAD1=0), general-purpose register (PAD1=1) P40 I/O control (PAD0=0), general-purpose register (PAD0=1)
	R/W				IOC42	0	Output	Input	
					IOC41	0	Output	Input	
					IOC40	0	Output	Input	
FF51H	PUL43	PUL42	PUL41	PUL40	PUL43	1	On	Off	P43 pull-up control (PAD3=0), general-purpose register (PAD3=1) P42 pull-up control (PAD2=0), general-purpose register (PAD2=1) P41 pull-up control (PAD1=0), general-purpose register (PAD1=1) P40 pull-up control (PAD0=0), general-purpose register (PAD0=1)
	R/W				PUL42	1	On	Off	
					PUL41	1	On	Off	
					PUL40	1	On	Off	
FF52H	P43	P42	P41	P40	P43	– *2	High	Low	P43 port data (PAD3=0), general-purpose register (PAD3=1) P42 port data (PAD2=0), general-purpose register (PAD2=1) P41 port data (PAD1=0), general-purpose register (PAD1=1) P40 port data (PAD0=0), general-purpose register (PAD0=1)
	R/W				P42	– *2	High	Low	
					P41	– *2	High	Low	
					P40	– *2	High	Low	
FF69H	PAD3	PAD2	PAD1	PAD0	PAD3	0	A/D	I/O	A/D-Ch3 enable (P43 terminal) A/D-Ch2 enable (P42 terminal) A/D-Ch1 enable (P41 terminal) A/D-Ch0 enable (P40 terminal)
	R/W				PAD2	0	A/D	I/O	
					PAD1	0	A/D	I/O	
					PAD0	0	A/D	I/O	

*1 Initial value at initial reset
 *2 Not set in the circuit
 *3 Constantly "0" when being read

PAD0–PAD3: A/D channel enable register (FF69H)

Selects the function for P40–P43.

- When "1" is written: A/D converter input
- When "0" is written: I/O port
- Reading: Valid

The PAD0 to PAD3 registers correspond to the P40 to P43 terminals. They set the terminals as the analog signal input terminal used in the A/D converter.

Write "1" to the register when using the terminal as the input channel of the A/D converter. When using the I/O port, write "0".

At initial reset, this register is set to "0".

P20–P23: P2 I/O port data register (FF4AH) P40–P43: P4 I/O port data register (FF52H)

I/O port data can be read and output data can be set through these registers.

• When writing data

- When "1" is written: High level
- When "0" is written: Low level

When an I/O port is set to the output mode, the written data is output unchanged from the I/O port terminal. When "1" is written as the port data, the port terminal goes high (VDD), and when "0" is written, the terminal goes low (VSS).

Port data can be written also in the input mode.

- **When reading data**

When "1" is read: High level

When "0" is read: Low level

The terminal voltage level of the I/O port is read out. When the I/O port is in the input mode the voltage level being input to the port terminal can be read out; in the output mode the register value can be read. When the terminal voltage is high (V_{DD}) the port data that can be read is "1", and when the terminal voltage is low (V_{SS}) the data is "0".

When "with pull-up resistor" has been selected with the mask option and the PUL register is set to "1", the built-in pull-up resistor goes ON during input mode, so that the I/O port terminal is pulled up.

The data registers of the ports (P40–P43) that are set as input for the A/D converter can be used as general purpose registers that do not affect the input/output.

Note: When the I/O port terminal is changed from low to high by pull-up resistor, the rise of the waveform is delayed on account of the time constant of the pull-up resistor and input gate capacitance.

Hence, when fetching input ports, set an appropriate wait time.

Particular care needs to be taken of the key scan during key matrix configuration.

Make this waiting time the amount of time or more calculated by the following expression.

Waiting time = $R_{IN} \times (C_{IN} + C_L) \times 1.6$ [sec]

R_{IN} : Pull-up resistance Max. value

C_{IN} : Terminal capacitance Max. value

C_L : Load capacitance on the board

IOC20–IOC23: P2 port I/O control register (FF48H)

IOC40–IOC43: P4 port I/O control register (FF50H)

The input and output modes of the I/O ports are set with these registers.

When "1" is written: Output mode

When "0" is written: Input mode

Reading: Valid

The input and output modes of the I/O ports are set in 1-bit unit.

Writing "1" to the I/O control register makes the corresponding I/O port enter the output mode, and writing "0" induces the input mode.

At initial reset, these registers are all set to "0", so the I/O ports are in the input mode.

The I/O control registers of the ports (P40–P43) that are set as input for the A/D converter can be used as general purpose registers that do not affect the input/output.

PUL20–PUL23: P2 port pull-up control register (FF49H)

PUL40–PUL43: P4 port pull-up control register (FF51H)

The pull-up during the input mode are set with these registers.

When "1" is written: Pull-up ON

When "0" is written: Pull-up OFF

Reading: Valid

The built-in pull-up resistor which is turned ON during input mode is set to enable in 1-bit units. (The pull-up resistor is included into the ports selected by the mask option.)

By writing "1" to the pull-up control register, the corresponding I/O ports are pulled up (during input mode), while writing "0" turns the pull-up function OFF.

At initial reset, these registers are all set to "1", so the pull-up function is set to ON.

The pull-up control registers of the ports (P40–P43) that are set as input for the A/D converter can be used as general purpose registers that do not affect the pull-up control.

4.5.6 Programming note

When the I/O port terminal is changed from low to high by the pull-up resistor in the input mode, the rise of the waveform is delayed on account of the time constant of the pull-up resistor and input gate capacitance. Hence, when fetching input ports, set an appropriate wait time.

Particular care needs to be taken of the key scan during key matrix configuration.

Make this waiting time the amount of time or more calculated by the following expression.

Waiting time = $R_{IN} \times (C_{IN} + C_L) \times 1.6$ [sec]

R_{IN}: Pull-up resistance Max. value

C_{IN}: Terminal capacitance Max. value

C_L: Load capacitance on the board

4.6 LCD Driver (COM0–COM3, SEG0–SEG19)

4.6.1 Configuration of LCD driver

The E0C63256 has 4 common terminals (COM0–COM3) and 20 segment terminals (SEG0–SEG19), so that it can drive an LCD with a maximum of 80 (20×4) segments.

In this LCD driver, the following drive methods can be selected with software.

- Duty: 1/4 duty, 1/3 duty or 1/2 duty
- Driving method: Dynamic drive or Static drive

4.6.2 Power supply for LCD driving/LCD drive bias

For the LCD drive power source, either the internal power supply or an external power supply can be selected by mask option.

Furthermore, when the internal power supply is selected, it is possible to choose whether the V_{C3} is supplied from outside of the IC or connected to V_{DD} inside the IC.

The internal LCD system voltage circuit generates V_{C2} and V_{C1} by dividing the V_{C3} or V_{DD} with resistors. See Section 2.1.2, "Voltage < V_{C1} , V_{C2} , V_{C3} > for LCD driving" for more information on the mask option for the LCD drive voltage.

The drive bias can also be selected from 1/3 bias and 1/2 bias by mask option.

Relationship of the voltages is as follows:

When 1/3 bias is selected: $V_{C1} = V_{C3} \times 1/3$, $V_{C2} = V_{C3} \times 2/3$ or $V_{C1} = V_{DD} \times 1/3$, $V_{C2} = V_{DD} \times 2/3$

When 1/2 bias is selected: $V_{C1} = V_{C2} = V_{C3} \times 1/2$ or $V_{C1} = V_{C2} = V_{DD} \times 1/2$

When an external power supply is selected, supply the above voltages to the V_{C1} , V_{C2} and V_{C3} terminals from the external power circuit.

The LCD system voltage circuit is turned ON and OFF by the LCD power control register LPWR.

When using the internal LCD voltage circuit, the LCD system voltage circuit generates V_{C1} and V_{C2} by setting LPWR to "1". When LPWR is set to "0", V_{C1} and V_{C2} become V_{SS} level. In this case, all outputs from the COM terminals and SEG terminals go to V_{SS} level. Therefore to display the LCD, the LCD drive power must be ON by previously setting LPWR to "1". SEG output ports that are set for DC output by the mask option operate same as the output (R) port regardless of the power ON/OFF control.

Note: It is necessary to write "1" to the LPWR register even if external power supply is selected.

4.6.3 Control of LCD display and drive waveform

(1) Display ON/OFF control

The E0C63256 incorporates the ALON and ALOFF registers to blink display. When "1" is written to ALON, all the segments go ON, and when "1" is written to ALOFF, all the segments go OFF. At such a time, an ON waveform or an OFF waveform is output from the SEG terminals. When "0" is written to these registers, normal display is performed. Furthermore, when "1" is written to both of the ALON and ALOFF, ALON (all ON) has priority over the ALOFF (all OFF). At initial reset, both the registers are set to "0" (normal display). However, the LCD power is OFF at initial reset, so the display is actually performed when the LCD power is turned ON (LPWR = "1").

(2) Setting of drive duty

In the E0C63256, the drive duty can be set to 1/4, 1/3 or 1/2 by the software. This setting is done using the LDUTY1 and LDUTY0 registers as shown in Table 4.6.3.1.

Table 4.6.3.1 LCD drive duty setting

LDUTY1	LDUTY0	Drive duty	Common terminal used	Maximum segment number
1	*	1/2	COM0, COM1	40 (20 × 2)
0	1	1/3	COM0–COM2	60 (20 × 3)
0	0	1/4	COM0–COM3	80 (20 × 4)

The frame frequency (f_{FR}) varies according to the oscillation frequency and setting of the prescaler (PRSM register). Refer to Section 4.2, "Oscillation Circuit and Prescaler", for setting of the prescaler.

- **When 1/4 duty, 1/2 duty driving**

$$f_{FR} = f_{PRS}/4096$$

Examples

In case of $f_{OSC} = 4.194304$ MHz and PRSM = 7: $f_{FR} = 64$ Hz

In case of $f_{OSC} = 2$ MHz and PRSM = 3: $f_{FR} = 61.0$ Hz

- **When 1/3 duty driving**

$$f_{FR} = 4/3 \times f_{PRS}/4096$$

Examples

In case of $f_{OSC} = 4.194304$ MHz and PRSM = 7: $f_{FR} = 85.3$ Hz

In case of $f_{OSC} = 2$ MHz and PRSM = 3: $f_{FR} = 81.4$ Hz

Figures 4.6.3.1 to 4.6.3.6 show the dynamic drive waveform according to the drive bias and duty.

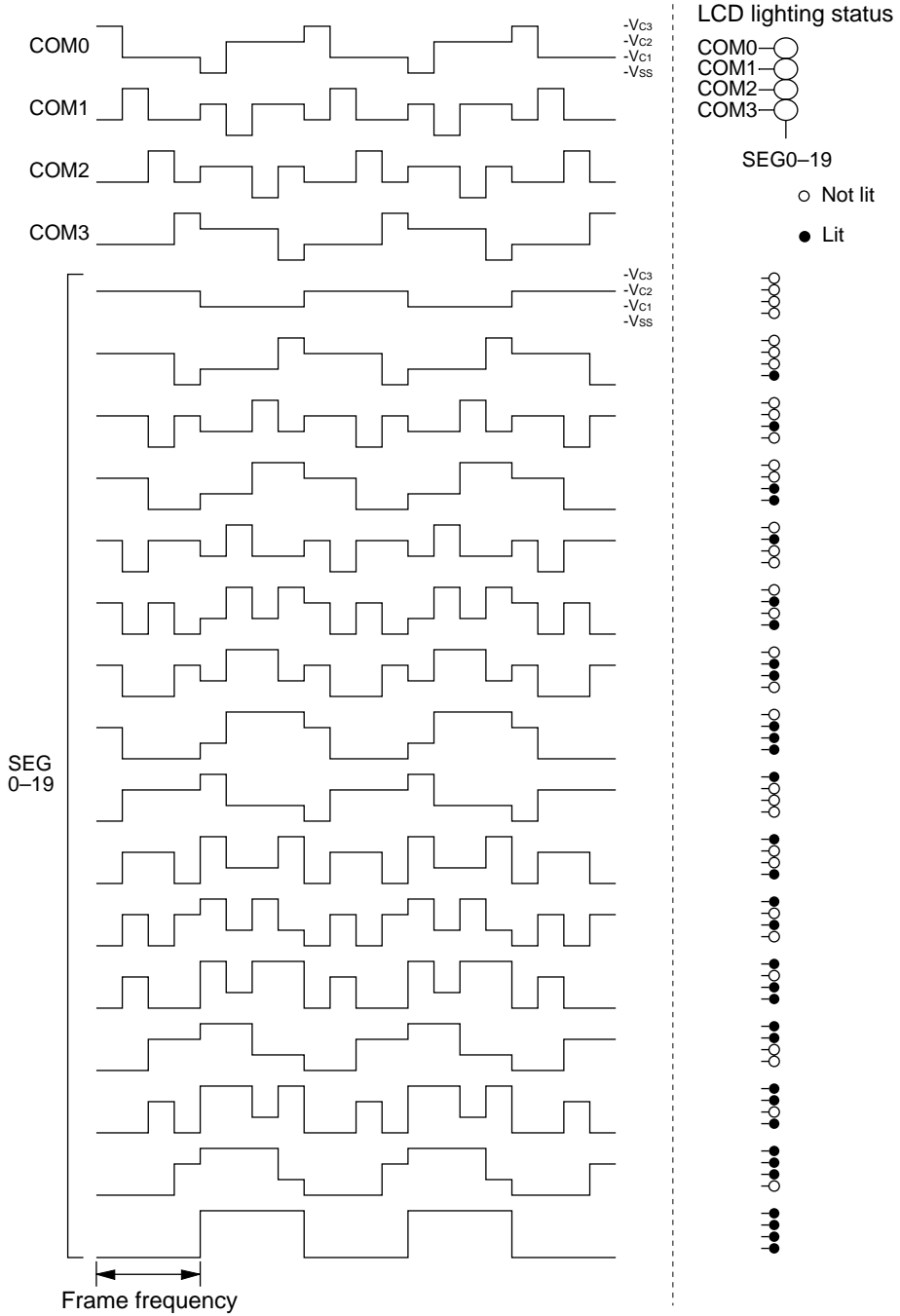


Fig. 4.6.3.1 Dynamic drive waveform for 1/4 duty (1/3 bias)

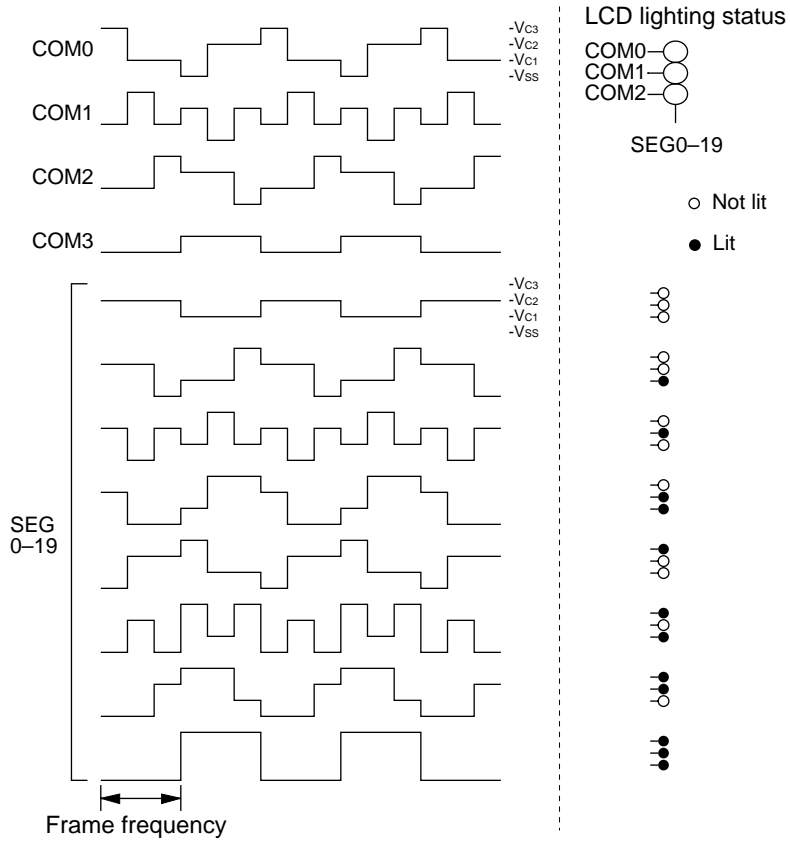


Fig. 4.6.3.2 Dynamic drive waveform for 1/3 duty (1/3 bias)

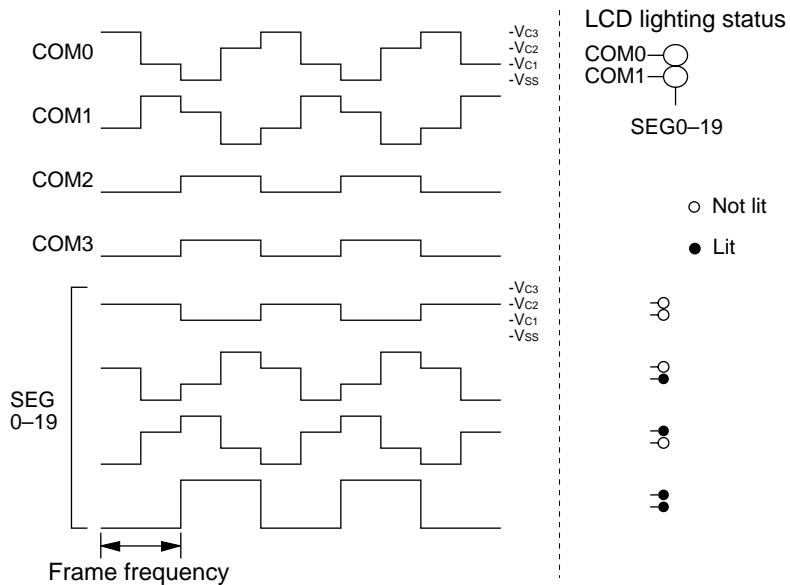


Fig. 4.6.3.3 Dynamic drive waveform for 1/2 duty (1/3 bias)

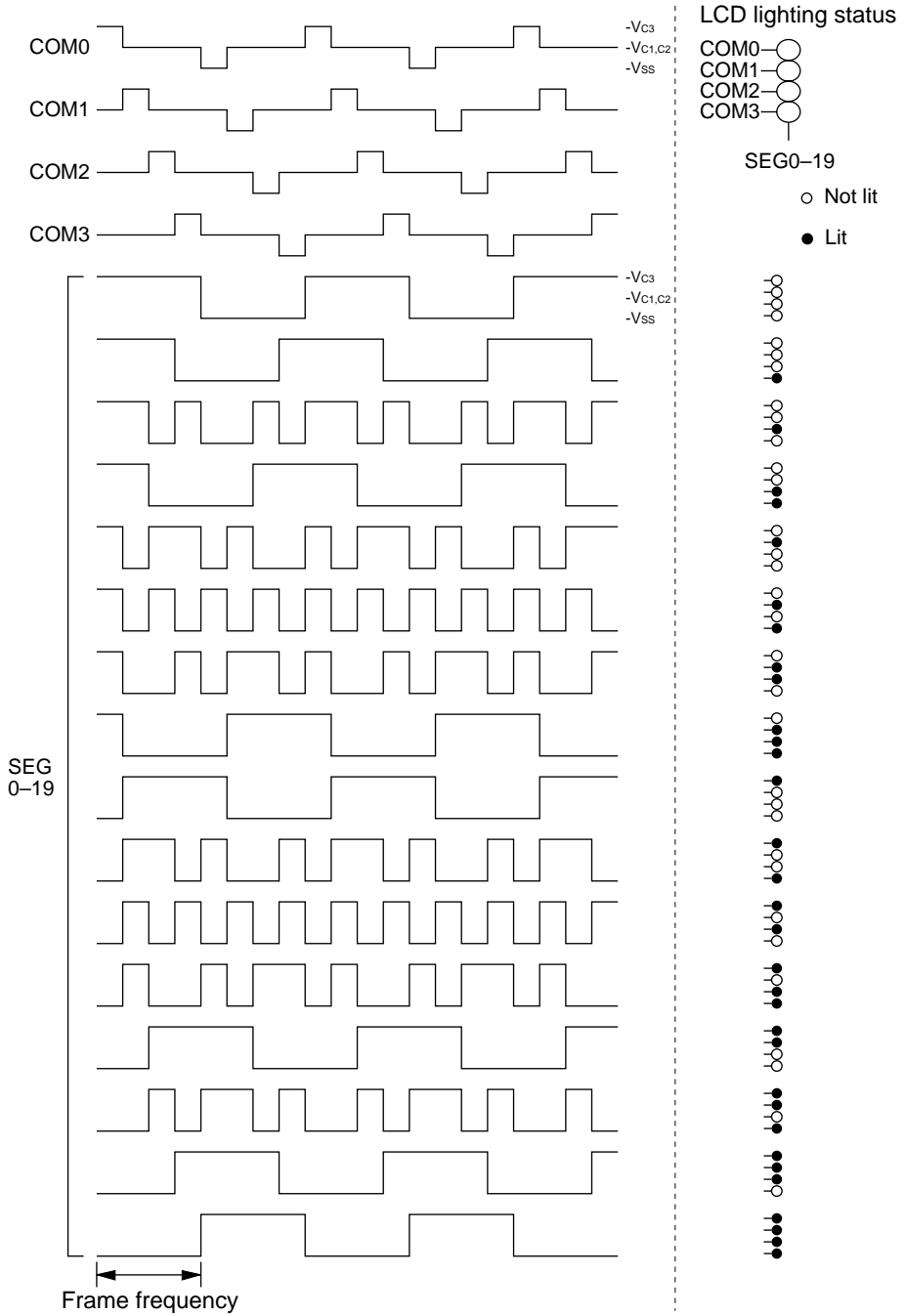


Fig. 4.6.3.4 Dynamic drive waveform for 1/4 duty (1/2 bias)

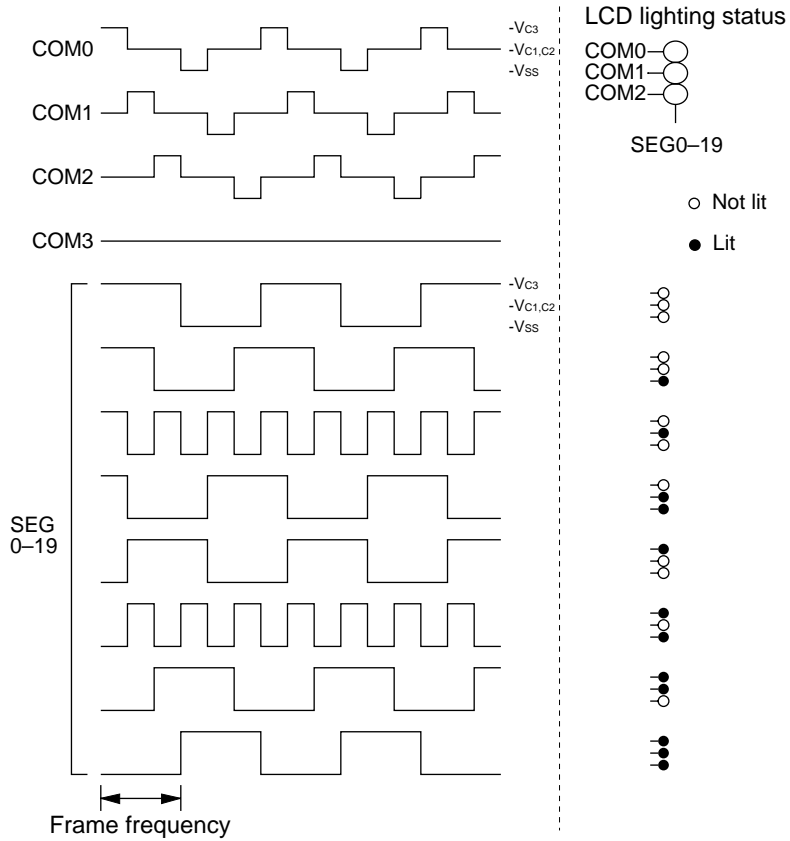


Fig. 4.6.3.5 Dynamic drive waveform for 1/3 duty (1/2 bias)

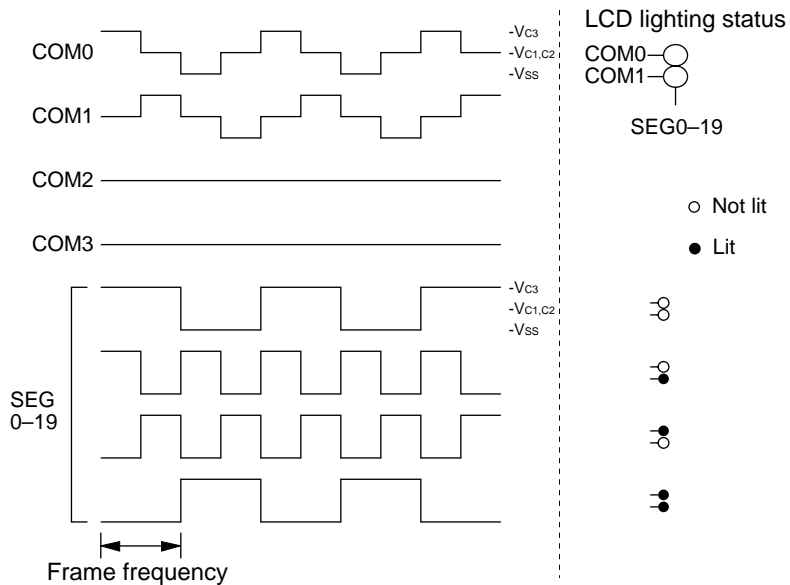


Fig. 4.6.3.6 Dynamic drive waveform for 1/2 duty (1/2 bias)

(3) Static drive

The E0C63256 provides software setting of the LCD static drive.

To set in static drive, write "1" to the common output signal control register STCD. Then, by writing "1" to any one of COM0 to COM3 (display memory) corresponding to the SEG terminal, the SEG terminal outputs a static ON waveform. When all the COM0 to COM3 bits are set to "0", the SEG terminal outputs a dynamic OFF waveform.

Figures 4.6.3.7 and 4.6.3.8 show the static drive waveform for 1/3 bias and 1/2 bias.

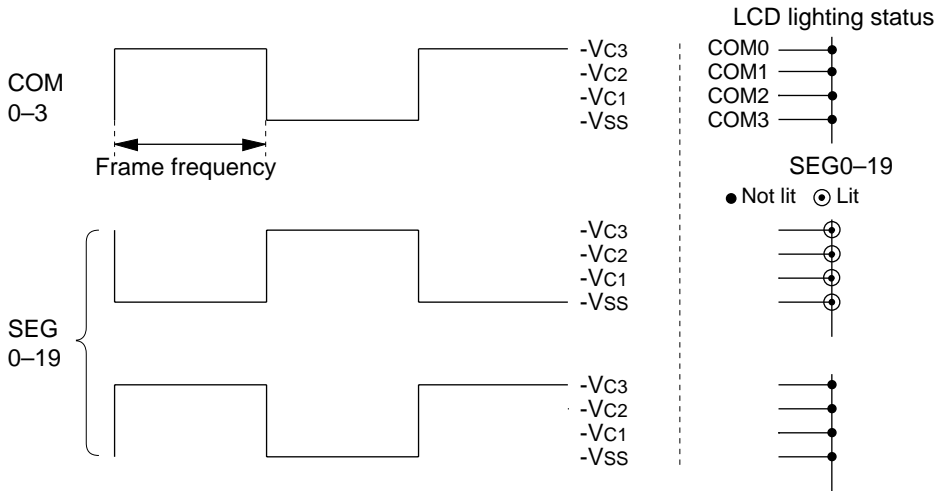


Fig. 4.6.3.7 Static drive waveform (1/3 bias)

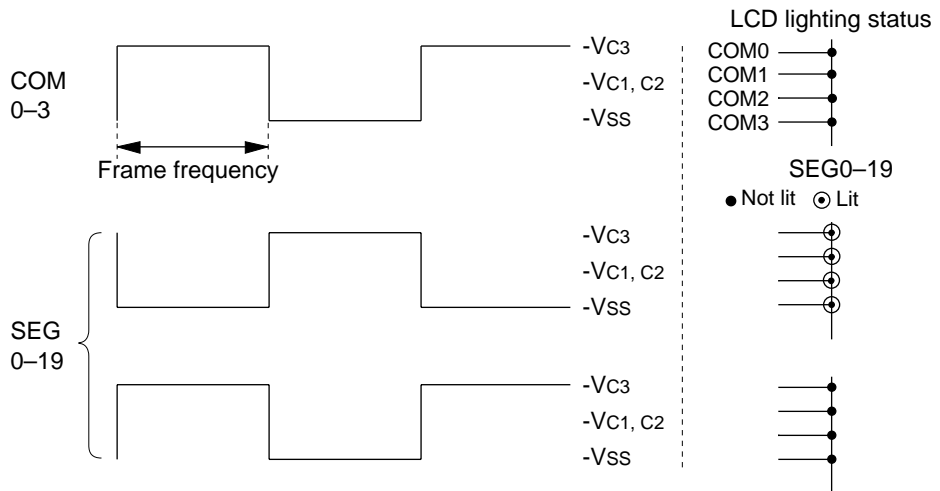


Fig. 4.6.3.8 Static drive waveform (1/2 bias)

4.6.4 Mask option

(1) Segment allocation

The display memory is arranged from addresses F000H to F013H in the data memory space. The LCD driver has a segment decoder built-in, and the data bit (D0–D3) of the optional address in the display memory area (F000H–F013H) can be allocated to the optional segment. This makes design easy by increasing the degree of freedom with which the liquid crystal panel can be designed.

The allocated segment displays when the bit for the display memory is set to "1", and goes out when bit is set to "0".

Figure 4.6.4.1 shows an example of the relationship between the LCD segments (on the panel) and the display memory for the case of 1/3 duty.

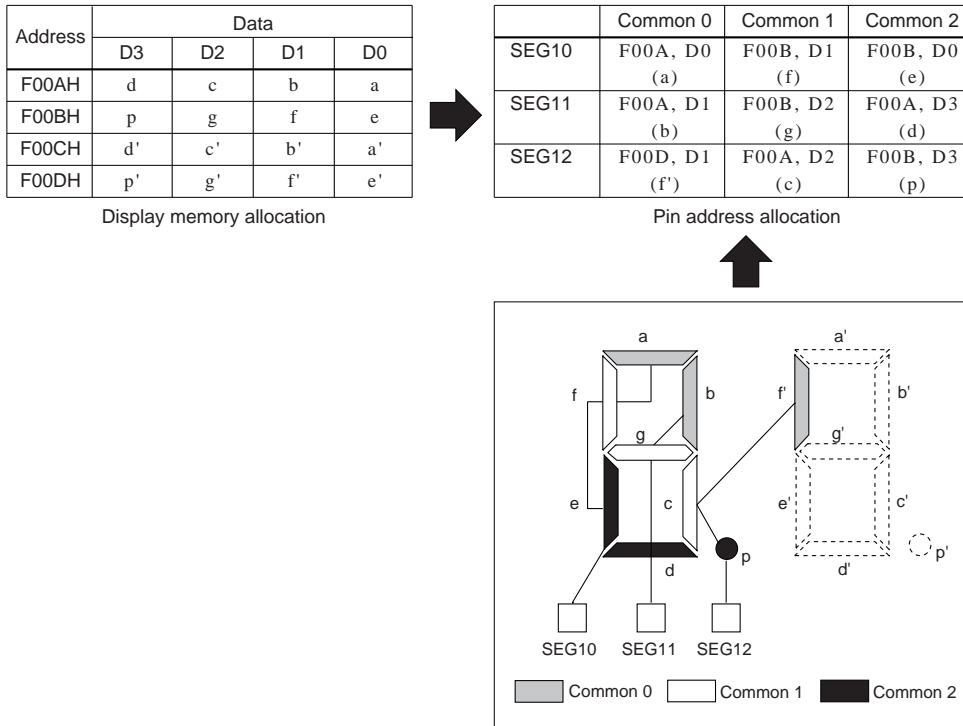


Fig. 4.6.4.1 Segment allocation

At initial reset, the contents of the display memory are undefined, therefore it is necessary to initialize by software. Since the display memory permits reading and writing, the addresses/bits that are not used on the LCD display can be used as general-purpose registers.

(2) Output specification

- ① The segment terminals (SEG0–SEG19) can be selected with the mask option in pairs* for either segment signal output or DC output (VDD and VSS binary output).
When DC output is selected, the data corresponding to COM0 of each segment terminal is output.
 - ② When DC output is selected, either complementary output or N-channel open drain output can be selected for each terminal with the mask option.
- * The terminal pairs are combination of $SEG2 \times n$ and $SEG2 \times n + 1$ (where n is an integer from 0 to 9).

Figure 4.6.4.2 shows the configuration of the segment terminal when DC output is selected.

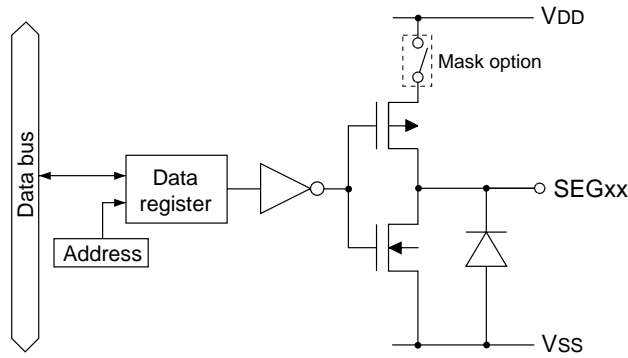


Fig. 4.6.4.2 Configuration of LCD driver (for DC output)

(3) Power supply for driving LCD/LCD drive bias

Either the internal power supply (external VC3 is used), internal power supply (external VC3 is not used) or an external power supply can be selected as the LCD system power supply. Further the LCD drive method can be selected from 1/3 bias drive or 1/2 bias drive. Refer to Section 2.1.2, "Voltage <VC1, VC2, VC3> for LCD driving", for details.

4.6.5 I/O memory of LCD driver

Table 4.6.5.1 shows the I/O addresses and the control bits for the LCD driver. Figure 4.6.5.1 shows the display memory map.

Table 4.6.5.1 Control bits of LCD driver

Address	Register				Name	Init *1	1	0	Comment
	D3	D2	D1	D0					
FF60H	LDUTY1	LDUTY0	0	LPWR	LDUTY1	0			LCD drive duty switch Duty [LDUTY1, 0] 0 1 2, 3 1/4 1/3 1/2
					LDUTY0	0			
	R/W		R	R/W	0 *3	- *2			Unused
					LPWR	0	On	Off	LCD power On/Off
FF61H	0	ALOFF	ALON	STCD	0 *3	- *2			Unused
					ALOFF	1	All Off	Normal	LCD all OFF control
					ALON	0	All On	Normal	LCD all ON control
	R	R/W			STCD	0	Static	Dynamic	Common output signal control

*1 Initial value at initial reset
 *2 Not set in the circuit
 *3 Constantly "0" when being read

Base address	Low	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
F000	Display memory (20 words × 4 bits) R/W																
F010	Unused area																

Fig. 4.6.5.1 Display memory map

LPWR: LCD power control (ON/OFF) register (FF60H•D0)

Turns the LCD system voltage circuit ON and OFF.

- When "1" is written: ON
- When "0" is written: OFF
- Reading: Valid

When "1" is written to the LPWR register, the LCD system voltage circuit goes ON and generate the LCD drive voltage (Vc1, Vc2). When "0" is written, the LCD drive voltage (Vc1, Vc2) goes to Vss level. It is necessary to write "1" to the LPWR register even if external power is selected by mask option. This control does not affect to SEG terminals that have been set for DC output. At initial reset, this register is set to "0".

Note: When the SLP instruction is executed when the LCD power is turned on (LPWR = "1"), the LCD drive voltages Vc1 and Vc2, COM outputs and SEG outputs go low the same when "0" is written to the LPWR register. However, since the SLEEP status does not affect the LPWR register, the LCD power turns on and the display resumes when the SLEEP status is released.

LDUTY0, LDUTY1: LCD drive duty switching register (FF60H•D2, D3)

Selects the LCD drive duty.

Table 4.6.5.2 Drive duty setting

LDUTY1	LDUTY0	Drive duty	Common terminal used	Maximum segment number
1	*	1/2	COM0, COM1	40 (20 × 2)
0	1	1/3	COM0–COM2	60 (20 × 3)
0	0	1/4	COM0–COM3	80 (20 × 4)

At initial reset, this register is set to "0".

STCD: Common output signal control register (FF61H•D0)

Switches the LCD driving method.

- When "1" is written: Static drive
- When "0" is written: Dynamic drive
- Reading: Valid

By writing "1" to STCD, static drive is selected, and dynamic drive is selected when "0" is written. At initial reset, this register is set to "0".

ALON: LCD all ON control register (FF61H•D1)

Displays the all LCD segments ON.

- When "1" is written: All LCD segments displayed
- When "0" is written: Normal display
- Reading: Valid

By writing "1" to the ALON register, all the LCD segments goes ON, and when "0" is written, it returns to normal display.

This function outputs an ON waveform to the SEG terminals, and segments not affect the content of the display memory.

ALON has priority over ALOFF.

At initial reset, this register is set to "0".

ALOFF: LCD all OFF control register (FF61H•D2)

Fade outs the all LCD segments.

When "1" is written: All LCD segments fade out

When "0" is written: Normal display

Reading: Valid

By writing "1" to the ALOFF register, all the LCD segments goes OFF, and when "0" is written, it returns to normal display.

This function outputs an OFF waveform to the SEG terminals, and does not affect the content of the display memory.

At initial reset, this register is set to "0".

Display memory (F000H–F013H)

The LCD segments are lit or turned off depending on this data.

When "1" is written: Lit

When "0" is written: Not lit

Reading: Invalid

By writing data into the display memory allocated to the LCD segment (on the panel), the segment can be lit or put out.

At initial reset, the contents of the display memory are undefined, therefore it is necessary to initialize by software. Since the display memory permits reading and writing, the addresses/bits that are not used on the LCD display can be used as general-purpose registers.

4.6.6 Programming note

The contents of the display memory are undefined until the area is initialized (through, for instance, memory clear processing by the CPU). Initialize the display memory by executing initial processing.

4.7 Clock Timer and Watchdog Timer

4.7.1 Configuration of clock timer and watchdog timer

The E0C63256 has a built-in clock timer that has a 1 Hz interrupt function and a watchdog timer that detects program overrun.

Figure 4.7.1.1 is the block diagram of the clock timer and watchdog timer.

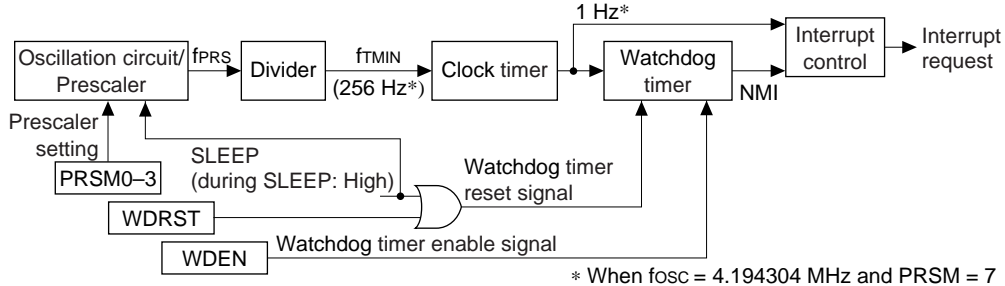


Fig. 4.7.1.1 Block diagram of clock timer and watchdog timer

4.7.2 Clock timer operation

The clock timer consists of an 8-bit binary counter that counts up with a divided f_{PRS} clock (256 Hz) output from the prescaler. The last stage of the counter generates a 1 Hz clock and it generates an interrupt.

(1) Input clock

When using the clock timer for clock function, a 256 Hz clock must be input to the timer. For this purpose, use a 4.194304 MHz crystal oscillator and set the PRSM register of the prescaler to 7. An accurate 1 Hz signal cannot be obtained in other conditions.

When using an oscillation frequency other than 4.194304 MHz, the frequency of the clock input to the clock timer is calculated by the expression below.

$$f_{TMIN} = \frac{f_{OSC}}{2048 \cdot n} \text{ [Hz]}$$

f_{TMIN} : Frequency of clock timer input clock [Hz]

f_{OSC} : Oscillation clock frequency [Hz]

n : PRSM register setting value + 1

For example, when the oscillation frequency is 2 MHz and the PRSM register is set to 3, the clock timer inputs a 244 Hz clock and generates a 0.95 Hz signal from the last stage of its counter.

Refer to Section 4.2, "Oscillation Circuit and Prescaler", for setting of the prescaler.

(2) Count operation

The clock timer always operates (counts up) when the IC is being operated even in HALT status. However, it stops counting in SLEEP status because the oscillation stops.

(3) 1 Hz interrupt

The clock timer sets the interrupt factor flag IT0 to "1" at the falling edge of its 1 Hz signal (when $f_{OSC} = 4.194304$ MHz) to generate an interrupt. The interrupt request to the CPU can be masked using the interrupt mask register EIT0. However, regardless of the interrupt mask register setting, the interrupt factor flag is set to "1" at the falling edge of the 1 Hz signal.

4.7.3 Watchdog timer operation

The watchdog timer is a 2-bit binary counter that counts up with the clock timer output signal (1 Hz). The watchdog timer must be reset periodically by software during operation. If the watchdog timer is not reset, it will generate a non-maskable interrupt when an overflow occurs in the last stage of the counter (0.25 Hz).

Watchdog timer reset processing in the program's main routine enables detection of program overrun, such as when the main routine's watchdog timer processing is bypassed. Ordinarily this routine is incorporated where periodic processing takes place, just as for the timer interrupt routine.

(1) Controlling watchdog timer

The watchdog timer starts counting after an initial reset, but it can be stopped by software. When the watchdog timer is not used, write "0" to the WDEN register (FF07H•D1) to stop the operation. This writing must be performed before a NMI occurs.

(2) Resetting watchdog timer

When the watchdog timer is being operated, reset it by writing "1" to WDRST (FF07H•D0) before the counter overflows. If the watchdog timer is not reset, a non-maskable interrupt (NMI) request will occur to the CPU.

The interval between resetting and an overflow occurring is calculated by the expression below.

$$\text{Min.} = \frac{524288 \cdot n}{f_{\text{OSC}}} \times 3 \text{ [sec]}$$

$$\text{Min.} = \frac{524288 \cdot n}{f_{\text{OSC}}} \times 4 \text{ [sec]}$$

f_{OSC} : Oscillation clock frequency [Hz]

n : PRSM register setting value + 1

Examples

In case of $f_{\text{OSC}} = 4.194304 \text{ MHz}$ and $\text{PRSM} = 7$: 3–4 seconds

In case of $f_{\text{OSC}} = 2 \text{ MHz}$ and $\text{PRSM} = 3$: 3.15–4.19 seconds

Refer to Section 4.2, "Oscillation Circuit and Prescaler", for setting of the prescaler.

The watchdog timer operates in HALT status. If the HALT status continues for the above time, the non-maskable interrupt will release the HALT status.

However, SLEEP period is not included in the reset cycle because the watchdog timer is placed in reset status in SLEEP mode (when the oscillation stops). Resume periodical resetting after the SLEEP mode is released.

(3) Interrupt

If the watchdog timer is not reset periodically, a non-maskable interrupt (NMI) is generated to the core CPU. Since this interrupt cannot be masked, it is accepted even in the interrupt disable status (I flag = "1"). However, it is not accepted when the CPU is in the interrupt mask state until SP1 and SP2 are set as a pair, such as after initial reset or during re-setting the stack pointer. The interrupt vector of NMI is assigned to 0100H in the program memory.

4.7.4 I/O memory of clock timer and watchdog timer

Table 4.7.4.1 shows the I/O addresses and the control bits for the clock timer and watchdog timer.

Table 4.7.4.1 Control bits of clock timer and watchdog timer

Address	Register								Comment
	D3	D2	D1	D0	Name	Init *1	1	0	
FF07H	0	0	WDEN	WDRST	0 *3	- *2			Unused
					0 *3	- *2			Unused
	R		R/W	W	WDEN	1	Enable	Disable	Watchdog timer enable
FFE6H				EITO	0 *3	- *2			Unused
					0 *3	- *2			Unused
	R			R/W	0 *3	- *2			Unused
					EITO	0	Enable	Mask	Interrupt mask register (Clock timer 1 Hz)
FFF6H	0	0	0	ITO	0 *3	- *2	(R)	(R)	Unused
					0 *3	- *2	Yes	No	Unused
	R			R/W	0 *3	- *2	(W)	(W)	Unused
					ITO	0	Reset	Invalid	Interrupt factor flag (Clock timer 1 Hz)

*1 Initial value at initial reset

*2 Not set in the circuit

*3 Constantly "0" when being read

WDEN: Watchdog timer enable register (FF07H•D1)

Selects whether the watchdog timer is used (enabled) or not (disabled).

- When "1" is written: Enabled
- When "0" is written: Disabled
- Reading: Valid

When "1" is written to the WDEN register, the watchdog timer starts count operation. When "0" is written, the watchdog timer does not count and does not generate an interrupt (NMI).

At initial reset, this register is set to "1".

WDRST: Watchdog timer reset (FF07H•D0)

Resets the watchdog timer.

- When "1" is written: Watchdog timer is reset
- When "0" is written: No operation
- Reading: Always "0"

When "1" is written to WDRST, the watchdog timer is reset and restarts immediately after that. When "0" is written, no operation results.

This bit is dedicated for writing, and is always "0" for reading.

EITO: 1 Hz interrupt mask register (FFE6H•D0)

Masks the clock timer interrupt.

- When "1" is written: Enabled
- When "0" is written: Masked
- Reading: Valid

This register is used to select whether the 1 Hz interrupt of the clock timer is masked or not. At initial reset, this register is set to "0".

IT0: 1 Hz interrupt factor flag (FFF6H•D0)

This flag indicates the status of the clock timer interrupt.

When "1" is read: Interrupt has occurred

When "0" is read: Interrupt has not occurred

When "1" is written: Flag is reset

When "0" is written: Invalid

The interrupt factor flag (IT0) corresponds to the 1 Hz clock timer interrupt. The software can judge from this flag whether it is a clock timer interrupt. However, even if the interrupt is masked, the flag is set to "1" at the falling edge of the 1 Hz signal.

This flag is reset to "0" by writing "1" to it.

After an interrupt occurs, the same interrupt will occur again if the interrupt enabled state (I flag = "1") is set or the RETI instruction is executed unless the interrupt factor flag is reset. Therefore, be sure to reset (write "1" to) the interrupt factor flag in the interrupt service routine before shifting to the interrupt enabled state.

At initial reset, this flag is set to "0".

4.7.5 Programming notes

- (1) To operate the clock timer accurately, the prescaler must be set correctly.
When using the clock timer for clock function, use a 4.194304 MHz crystal oscillator and set the PRSM register of the prescaler to 7. An accurate 1 Hz signal cannot be obtained in other conditions.
- (2) After an interrupt occurs, the same interrupt will occur again if the interrupt enabled state (I flag = "1") is set or the RETI instruction is executed unless the interrupt factor flag is reset. Therefore, be sure to reset (write "1" to) the interrupt factor flag in the interrupt service routine before shifting to the interrupt enabled state.
- (3) When the watchdog timer is used, the software must reset the watchdog timer before an overflow occurs.
- (4) Because the watchdog timer is set in operation state by initial reset, set the watchdog timer to disabled state (not used) before generating an interrupt (NMI) if it is not used.

4.8.2 8-/16-bit mode

Each pair of timers (timers 0 and 1 and timers 2 and 3) can be used as an 8-bit × 2 ch. of timer or a 16-bit × 1 ch. timer, respectively. The MODE0 register (timers 0, 1) and the MODE1 register (timers 2, 3) are used for this setting.

Table 4.8.2.1 Setting of 8/16-bit mode

MODE1	MODE0	Timer 3	Timer 2	Timer 1	Timer 0
0	0	8 bits	8 bits	8 bits	8 bits
0	1	8 bits	8 bits	16 bits	
1	0	16 bits		8 bits	8 bits
1	1	16 bits		16 bits	

In the 8-bit mode, each timer can be controlled individually.

In the 16-bit mode, the underflow signal of timer 0 (or timer 2) is used as the input clock of timer 1 (or timer 3) so that the down counters operate as a 16-bit counter.

The timer in the 16-bit mode is controlled with the control registers for low-order 8-bit side (timer 0, timer 2).

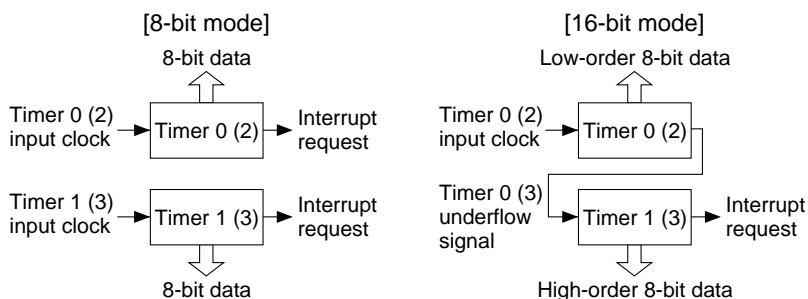


Fig. 4.8.2.1 Counter configuration in 8- and 16-bit mode

4.8.3 Programmable timer operation

(1) Count clock

The programmable timer generates four types of count clocks by dividing the oscillation clock (f_{osc}). One of among the four types can be selected as the input clock for the counter. This selection can be done in each timer individually using the division ratio selection register PTPS for each timer.

Table 4.8.3.1 Selection of count clock

PTPS01	PTPS00	Timer 0 input clock
PTPS11	PTPS10	Timer 1 input clock
PTPS21	PTPS20	Timer 2 input clock
PTPS31	PTPS30	Timer 3 input clock
1	1	$f_{osc}/256$
1	0	$f_{osc}/32$
0	1	$f_{osc}/4$
0	0	$f_{osc}/1$

f_{osc} : Oscillation clock

Timer 0 has an event counter function and can use the signal input to the K03 input port as the count clock. Refer to Section 4.8.5 for information on the event counter function and the input clock.

(2) Reload data register and initial value setting

Each timer contains an 8-bit reload data register RLD that is used to set a counter initial value.

Timer 0: RLD07–RLD00 (used as the low-order 8-bit data in the 16-bit mode)

Timer 1: RLD17–RLD10 (used as the high-order 8-bit data in the 16-bit mode)

Timer 2: RLD27–RLD20 (used as the low-order 8-bit data in the 16-bit mode)

Timer 3: RLD37–RLD30 (used as the high-order 8-bit data in the 16-bit mode)

The reload data register can be read and written, and the each registers are set to 00H at initial reset. Data written in this register is loaded into the down counter, and a down counting starts from the value.

The preset of the down counter is done in the following two cases:

1. When software presets

The software preset can be done using the reset bit PTRST of each timer.

Timer 0: PTRST0

Timer 1: PTRST1

Timer 2: PTRST2

Timer 3: PTRST3

When the reset bit is set to "1", the content of the reload data register is loaded into the down counter at that point.

In the 16-bit mode, a 16-bit reload data is loaded all at a time by PTRST (PTRST0, PTRST2) of the low-order 8-bit side. In this case, writing to PTRST (PTRST1, PTRST3) of the high-order 8-bit side is invalid.

2. When down counter has underflown during a count

Since each down counter is preset with the reload data by the underflow, the underflow period is decided according to the value set in the reload data register. This underflow generates an interrupt, and controls the clock (PTOUT signal) output.

(3) Reload data register and setting of initial value

The register PTRUN is provided to control the RUN/STOP for each timer.

Timer 0: PTRUN0

Timer 1: PTRUN1

Timer 2: PTRUN2

Timer 3: PTRUN3

By writing "1" to the register after presetting the reload data to the down counter, the down counter starts counting down. Writing "0" stops the input count clock and the down counter stops counting. This control (RUN/STOP) does not affect the counter data. The counter maintains its data while stopped, and can restart counting continuing from that data.

In the 16-bit mode, the counter is controlled by the PTRUN register of the low-order 8-bit side (PTRUN0, PTRUN2). In this case, writing to the PTRUN register of the high-order 8-bit side (PTRUN1, PTRUN3) is invalid.

Each counter reloads the initial value set in the reload data register RLD when an underflow occurs through the count down. It continues counting down from the initial value after reloading.

In addition to reloading the counter, this underflow signal controls the interrupt generation and pulse (PTOUT signal) output.

Figure 4.8.3.1 shows the basic operation timing of the down counter.

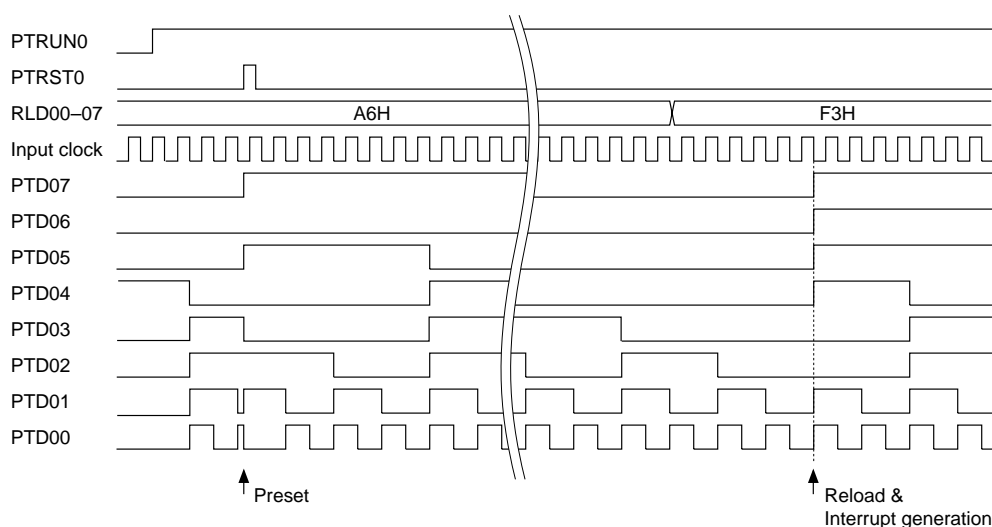


Fig. 4.8.3.1 Basic operation timing of down counter (example of timer 0)

(4) Counter data reading and hold function

The counter data can be read via the data buffer PTD of each timer.

Timer 0: PTD07–PTD00 (used as the low-order 8-bit data in the 16-bit mode)

Timer 1: PTD17–PTD10 (used as the high-order 8-bit data in the 16-bit mode)

Timer 2: PTD27–PTD20 (used as the low-order 8-bit data in the 16-bit mode)

Timer 3: PTD37–PTD30 (used as the high-order 8-bit data in the 16-bit mode)

The count data in the data buffer can be read in 4-bit units. Note, however to be sure to read the least significant data first because the data buffer is designed so that reading of the least significant data holds the high-order data in order to prevent the borrowing operation between low- and high-order reading.

In the 16-bit mode, read data in order of low-order 4 bits and high-order 4 bits of timer 0 (timer 2) then low-order 4 bits and high-order 4 bits of timer 1 (timer 3)

The data hold function uses the prescaler as the clock source, therefore, the data hold time varies according to the oscillation frequency and setting of the prescaler (PRSM). The data hold time is calculated by the expression below.

$$\text{8-bit mode: } t_{\text{HOLD}} = \frac{256 \cdot n}{f_{\text{OSC}}} \text{ [sec]}$$

$$\text{16-bit mode: } t_{\text{HOLD}} = \frac{512 \cdot n}{f_{\text{OSC}}} \text{ [sec]}$$

t_{HOLD} : Count data hold time

f_{OSC} : Oscillation clock frequency

n : PRSM register setting value + 1

Examples

	8-bit mode	16-bit mode
In case of $f_{\text{OSC}} = 4.194304 \text{ MHz}$ and $\text{PRSM} = 7$:	0.49 msec	0.98 msec
In case of $f_{\text{OSC}} = 2 \text{ MHz}$ and $\text{PRSM} = 3$:	0.51 msec	1.02 msec

Refer to Section 4.2, "Oscillation Circuit and Prescaler", for setting of the prescaler.

Note that the counter data hold function will be released if the high-order data is not read in this data hold period.

4.8.4 Interrupt function

The programmable timer can generate an interrupt due to an underflow of each timer. See Figure 4.8.3.1 for the interrupt timing.

In the 16-bit mode, the high-order 8-bit counter (timer 1, timer 3) generates an interrupt by its underflow. In this case, the low-order 8-bit counter (timer 0, timer 2) does not generate an interrupt even if the counter underflows.

An underflow of each timer sets the corresponding interrupt factor flag IPT to "1", and generates an interrupt. The interrupt can also be masked by setting the corresponding interrupt mask register EIPT. However, the interrupt factor flag is set to "1" by an underflow of the corresponding timer regardless of the interrupt mask register setting.

Interrupt factor flag	Interrupt mask register
Timer 0: IPT0 (invalid in the 16-bit mode)	EIPT0
Timer 1: IPT1	EIPT1
Timer 2: IPT2 (invalid in the 16-bit mode)	EIPT2
Timer 3: IPT3	EIPT3

4.8.5 Event counter function

The timer 0 has an event counter function that counts an external clock input to the input port K03. This function is selected by writing "1" to the timer 0 counter mode selection register EVCNT.

When the pair of timers 0 and 1 are set in the 16-bit mode, they become a 16-bit event counter. The timers 2 and 3 cannot be used as an event counter.

In the event counter mode, the clock is supplied to timer 0 from outside of the IC, therefore, the settings of the timer 0 division ratio selection register PTPS0 become invalid.

Count down timing can be selected from either the falling or rising edge of the input clock using the timer 0 pulse polarity selection register PLPOL. When "0" is written to the PLPOL register, the falling edge is selected, and when "1" is written, the rising edge is selected. The count down timing is shown in Figure 4.8.5.1.

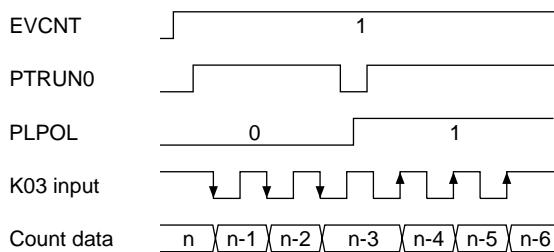


Fig. 4.8.5.1 Timing chart in event counter mode

The event counter mode also includes a noise reject function to eliminate noise such as chattering on the external clock (K03 input signal). This function is selected by writing "1" to the timer 0 function selection register FCSEL.

The noise rejection clock is generated using the prescaler as the clock source, therefore, the frequency varies according to the oscillation frequency and setting of the prescaler (PRSM). The noise rejection clock frequency is calculated by the expression below.

$$f_{PTNR} = \frac{f_{OSC}}{256 \cdot n} \text{ [Hz]}$$

f_{PTNR} : Noise rejection clock frequency

f_{OSC} : Oscillation clock frequency

n : PRSM register setting value + 1

Examples

In case of $f_{OSC} = 4.194304$ MHz and PRSM = 7: 2048 Hz

In case of $f_{OSC} = 2$ MHz and PRSM = 3: 1953 Hz

The noise rejector allows the counter to input the clock at the second falling edge of the noise rejection clock (f_{PTNR}) after changing the input level of the K03 input port terminal. Consequently, the pulse width of noise that can reliably be rejected is $1/f_{PTNR}$ or less.

Examples: Pulse width of noise that can reliably be rejected

In case of $f_{OSC} = 4.194304$ MHz and PRSM = 7: 0.49 msec or less

In case of $f_{OSC} = 2$ MHz and PRSM = 3: 0.51 msec or less

When the noise rejector is used, the input pulse width (for both low level and high level) must be longer than the doubled noise rejection pulse for reliable counting.

Examples: Input pulse width that can reliably be counted

In case of $f_{OSC} = 4.194304$ MHz and PRSM = 7: 0.98 msec or more

In case of $f_{OSC} = 2$ MHz and PRSM = 3: 1.01 msec or more

Refer to Section 4.2, "Oscillation Circuit and Prescaler", for setting of the prescaler.

Figure 4.8.5.2 shows the count down timing with noise rejector.

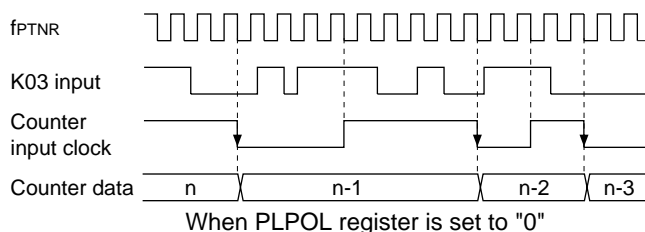


Fig. 4.8.5.2 Count down timing with noise rejector

The operation of the event counter mode is the same as the timer mode except it uses the K03 input as the clock.

Refer to Section 4.8.3, "Programmable timer operation" for basic operation and control.

4.8.6 Setting of PTOUT output

The programmable timer can generate a PTOUT signal due to an underflow of each timer. The PTOUT signal is generated by dividing the underflows in 1/2. It is possible to select which timer's underflow is to be used by the PTOUT output channel selection register CHSEL.

Table 4.8.6.1 Selection of PTOUT output channel

CHSEL1	CHSEL0	PTOUT output Ch
1	1	Timer 3
1	0	Timer 2
0	1	Timer 1
0	0	Timer 0

In the 16-bit mode, the PTOUT signal is generated using underflow from the high-order 8-bit counter. Therefore, the PTOUT output channel selection register CHSEL must be set to timer 1 or timer 3. Figure 4.8.6.1 shows the PTOUT signal waveform when the channel is changed.

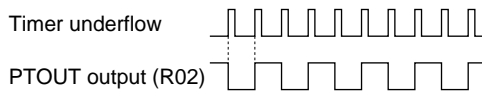


Fig. 4.8.6.1 PTOUT signal waveform at channel change

The PTOUT signal can be output from the R02 output port terminal. Programmable clocks can be supplied to external devices.

Figure 4.8.6.2 shows the configuration of the output port R02.

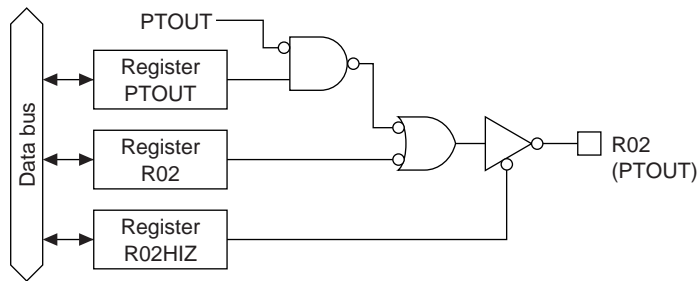


Fig. 4.8.6.2 Configuration of R02

The output of a PTOUT signal is controlled by the PTOUT register. When "1" is written to the PTOUT register, the PTOUT signal is output from the R02 output port terminal and when "0" is written, the terminal goes to a high (VDD) level. However, the data register R02 must always be "1" and the high impedance control register R02HIZ must always be "0" (data output state).

Since the PTOUT signal is generated asynchronously from the PTOUT register, a hazard within 1/2 cycle is generated when the signal is turned ON and OFF by setting the register.

Figure 4.8.6.3 shows the output waveform of the PTOUT signal.

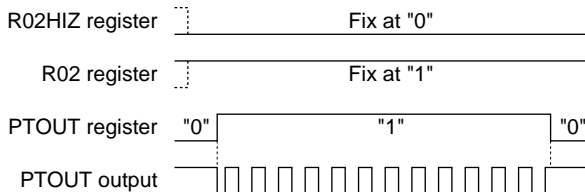


Fig. 4.8.6.3 Output waveform of the PTOUT signal

4.8.7 I/O memory of programmable timer

Table 4.8.7.1 shows the I/O addresses and the control bits for the programmable timer.

Table 4.8.7.1(a) Control bits of programmable timer

Address	Register				Name	Init *1	1	0	Comment
	D3	D2	D1	D0					
FFC0H	0	0	MODE1	MODE0	0 *3	- *2			Unused
					0 *3	- *2			Unused
	R		R/W		MODE1	0	16 bit	8 bit x 2	8/16 bits mode selection (Programmable timer 2, 3)
FFC1H	0	EVCNT	FCSEL	PLPOL	0 *3	- *2			Unused
					EVCNT	0	Event ct.	Timer	Timer 0 counter mode selection
	R	R/W			FCSEL	0	With NR	No NR	Timer 0 function selection (for event counter mode)
FFC2H	0	PTOUT	CHSEL1	CHSEL0	0 *3	- *2			Unused
					PTOUT	0	On	Off	PTOUT output control
	R	R/W			CHSEL1	0			PTOUT output channel selection
				CHSEL0	0			Output Ch Timer 0 Timer 1 Timer 2 Timer 3	
FFC4H	PTPS01	PTPS00	PTRST0	PTRUN0	PTPS01	0			Timer 0 clock division ratio selection
					PTPS00	0			
	R/W		W	R/W	PTRST0*3	- *2	Reset	Invalid	Timer 0 reset (reload)
FFC5H	PTPS11	PTPS10	PTRST1	PTRUN1	PTPS11	0			Timer 1 clock division ratio selection
					PTPS10	0			
	R/W		W	R/W	PTRST1*3	- *2	Reset	Invalid	Timer 1 reset (reload)
FFC6H	PTPS21	PTPS20	PTRST2	PTRUN2	PTPS21	0			Timer 2 clock division ratio selection
					PTPS20	0			
	R/W		W	R/W	PTRST2*3	- *2	Reset	Invalid	Timer 2 reset (reload)
FFC7H	PTPS31	PTPS30	PTRST3	PTRUN3	PTPS31	0			Timer 3 clock division ratio selection
					PTPS30	0			
	R/W		W	R/W	PTRST3*3	- *2	Reset	Invalid	Timer 3 reset (reload)
FFD0H	RLD03	RLD02	RLD01	RLD00	RLD03	0			MSB
					RLD02	0			
	R/W				RLD01	0			LSB
FFD1H	RLD07	RLD06	RLD05	RLD04	RLD07	0			MSB
					RLD06	0			
	R/W				RLD05	0			LSB
FFD2H	RLD13	RLD12	RLD11	RLD10	RLD13	0			MSB
					RLD12	0			
	R/W				RLD11	0			LSB
FFD3H	RLD17	RLD16	RLD15	RLD14	RLD17	0			MSB
					RLD16	0			
	R/W				RLD15	0			LSB
FFD4H	RLD23	RLD22	RLD21	RLD20	RLD23	0			MSB
					RLD22	0			
	R/W				RLD21	0			LSB
FFD5H	RLD27	RLD26	RLD25	RLD24	RLD27	0			MSB
					RLD26	0			
	R/W				RLD25	0			LSB
FFD6H	RLD33	RLD32	RLD31	RLD30	RLD33	0			MSB
					RLD32	0			
	R/W				RLD31	0			LSB
				RLD30	0				

*1 Initial value at initial reset

*2 Not set in the circuit

*3 Constantly "0" when being read

Table 4.8.1(b) Control bits of programmable timer

Address	Register				Name	Init *1	1	0	Comment
	D3	D2	D1	D0					
FFD7H	RLD37	RLD36	RLD35	RLD34	RLD37	0			MSB Programmable timer 3 reload data (high-order 4 bits) LSB
	R/W				RLD36	0			
					RLD35	0			
					RLD34	0			
FFD8H	PTD03	PTD02	PTD01	PTD00	PTD03	0			MSB Programmable timer 0 data (low-order 4 bits) LSB
	R				PTD02	0			
					PTD01	0			
					PTD00	0			
FFD9H	PTD07	PTD06	PTD05	PTD04	PTD07	0			MSB Programmable timer 0 data (high-order 4 bits) LSB
	R				PTD06	0			
					PTD05	0			
					PTD04	0			
FFDAH	PTD13	PTD12	PTD11	PTD10	PTD13	0			MSB Programmable timer 1 data (low-order 4 bits) LSB
	R				PTD12	0			
					PTD11	0			
					PTD10	0			
FFDBH	PTD17	PTD16	PTD15	PTD14	PTD17	0			MSB Programmable timer 1 data (high-order 4 bits) LSB
	R				PTD16	0			
					PTD15	0			
					PTD14	0			
FFDCH	PTD23	PTD22	PTD21	PTD20	PTD23	0			MSB Programmable timer 2 data (low-order 4 bits) LSB
	R				PTD22	0			
					PTD21	0			
					PTD20	0			
FFDDH	PTD27	PTD26	PTD25	PTD24	PTD27	0			MSB Programmable timer 2 data (high-order 4 bits) LSB
	R				PTD26	0			
					PTD25	0			
					PTD24	0			
FFDEH	PTD33	PTD32	PTD31	PTD30	PTD33	0			MSB Programmable timer 3 data (low-order 4 bits) LSB
	R				PTD32	0			
					PTD31	0			
					PTD30	0			
FFDFH	PTD37	PTD36	PTD35	PTD34	PTD37	0			MSB Programmable timer 3 data (high-order 4 bits) LSB
	R				PTD36	0			
					PTD35	0			
					PTD34	0			
FFE2H	EIPT3	EIPT2	EIPT1	EIPT0	EIPT3	0	Enable	Mask	Interrupt mask register (Programmable timer 3)
					EIPT2	0	Enable	Mask	Interrupt mask register (Programmable timer 2)
					EIPT1	0	Enable	Mask	Interrupt mask register (Programmable timer 1)
					EIPT0	0	Enable	Mask	Interrupt mask register (Programmable timer 0)
FFF2H	IPT3	IPT2	IPT1	IPT0	IPT3	0	(R)	(R)	Interrupt factor flag (Programmable timer 3)
					IPT2	0	Yes	No	Interrupt factor flag (Programmable timer 2)
					IPT1	0	(W)	(W)	Interrupt factor flag (Programmable timer 1)
	R/W				IPT0	0	Reset	Invalid	Interrupt factor flag (Programmable timer 0)

*1 Initial value at initial reset
 *2 Not set in the circuit
 *3 Constantly "0" when being read

MODE0: Timer 0, 1 8-/16-bit mode selection register (FFC0H•D0)

MODE1: Timer 2, 3 8-/16-bit mode selection register (FFC0H•D1)

Selects either the 8-bit or 16-bit mode.

- When "1" is written: 16 bits × 1 channel
- When "0" is written: 8 bits × 2 channels
- Reading: Valid

Select whether timers 0 and 1 or timers 2 and 3 are used as 2 channels independent 8-bit timers or as 1 channel combined 16-bit timer. When "0" is written to the MODE0 (timers 0 and 1) or MODE1 (timers 2 and 3) register, 8-bit × 2 channels is selected and when "1" is written, 16-bit × 1 channel is selected. At initial reset, these registers are set to "0".

PTPS00, PTPS01: Timer 0 clock division ratio selection register (FFC4H•D2, D3)

PTPS10, PTPS11: Timer 1 clock division ratio selection register (FFC5H•D2, D3)

PTPS20, PTPS21: Timer 2 clock division ratio selection register (FFC6H•D2, D3)

PTPS30, PTPS31: Timer 3 clock division ratio selection register (FFC7H•D2, D3)

Selects the division ratio of the clock to be input to each timer.

Table 4.8.7.2 shows the selectable division ratios.

Table 4.8.7.2 Selection of clock division ratio

PTPS01	PTPS00	Timer 0 input clock
PTPS11	PTPS10	Timer 1 input clock
PTPS21	PTPS20	Timer 2 input clock
PTPS31	PTPS30	Timer 3 input clock
1	1	fosc/256
1	0	fosc/32
0	1	fosc/4
0	0	fosc/1

fosc: Oscillation clock

In the 16-bit mode, the division ratio should be selected using the low-order 8-bit side PTPS (PTPS0, PTPS2). Writing to the high-order side will be invalid.

When timer 0 is set in the event counter mode, settings of PTPS00 and PTPS01 are invalid.

At initial reset, these registers are set to "0".

EVCNT: Timer 0 counter mode selection register (FFC1H•D2)

Selects a counter mode for timer 0.

When "1" is written: Event counter

When "0" is written: Timer

Reading: Valid

Selects whether timer 0 is used as an event counter that counts with the external clock or a timer that counts with the internal clock. When "1" is written to the EVCNT register, the event counter is selected and when "0" is written, the timer is selected.

At initial reset, this register is set to "0".

FCSEL: Timer 0 function selection register (FFC1H•D1)

Selects whether the noise rejector will be used or not in the event counter.

When "1" is written: With noise rejector

When "0" is written: Without noise rejector

Reading: Valid

When "1" is written to the FCSEL register, the external clock that is input from the K03 terminal passes through the noise rejector. When "0" is written, the K03 input clock bypasses the noise rejector and directly counts up the event counter. See Section 4.8.5 for pulse width regarded as noise by the noise rejector and pulse width that can be used as count pulse.

Setting of this register is effective only when timer 0 is used in the event counter.

At initial reset, this register is set to "0".

PLPOL: Timer 0 pulse polarity selection register (FFC1H•D0)

Selects the count pulse polarity in the event counter.

When "1" is written: Rising edge

When "0" is written: Falling edge

Reading: Valid

The count timing in the event counter mode (timer 0) is selected from either the falling edge of the external clock input to the K03 input port terminal or the rising edge. When "0" is written to the PLPOL register, the falling edge is selected and when "1" is written, the rising edge is selected.

Setting of this register is effective only when timer 0 is used in the event counter.

At initial reset, this register is set to "0".

RLD00–RLD07: Timer 0 reload data register (FFD0H, FFD1H)

RLD10–RLD17: Timer 1 reload data register (FFD2H, FFD3H)

RLD20–RLD27: Timer 2 reload data register (FFD4H, FFD5H)

RLD30–RLD37: Timer 3 reload data register (FFD6H, FFD7H)

Sets the initial value for the counter.

The reload data written in this register is loaded to the respective counters. The counter counts down using the data as the initial value for counting.

Reload data is loaded to the counter when the counter is reset by writing "1" to the PTRST register of each timer, or when counter underflow occurs.

At initial reset, these registers are set to "00H".

PTD00–PTD07: Timer 0 counter data (FFD8H, FFD9H)

PTD10–PTD17: Timer 1 counter data (FFDAH, FFDBH)

PTD20–PTD27: Timer 2 counter data (FFDCH, FFDDH)

PTD30–PTD37: Timer 3 counter data (FFDEH, FPDFH)

Count data in the programmable timer can be read from these latches.

Be sure to read the low-order 4 bits first.

In the 16-bit mode, read data in order of low-order 4 bits and high-order 4 bits of timer 0 (timer 2) then low-order 4 bits and high-order 4 bits of timer 1 (timer 3).

Since these latches are exclusively for reading, the writing operation is invalid.

At initial reset, these counter data are set to "00H".

PTRST0: Timer 0 reset (reload) (FFC4H•D1)

PTRST1: Timer 1 reset (reload) (FFC5H•D1)

PTRST2: Timer 2 reset (reload) (FFC6H•D1)

PTRST3: Timer 3 reset (reload) (FFC7H•D1)

Resets the timer and presets reload data to the counter.

When "1" is written: Reset

When "0" is written: No operation

Reading: Always "0"

By writing "1" to PTRST, the reload data in the reload register RLD is preset to the counter.

When the counter is preset in the RUN status, the counter restarts immediately after presetting. In the case of STOP status, the reload data is preset to the counter and is maintained.

No operation results when "0" is written.

In the 16-bit mode, a 16-bit reload data is loaded all at a time by PTRST (PTRST0, PTRST2) of the low-order 8-bit side. In this case, writing to PTRST (PTRST1, PTRST3) of the high-order 8-bit side is invalid.

Since these bits are exclusively for writing, always set to "0" during reading.

PTRUN0: Timer 0 RUN/STOP control register (FFC4H•D0)

PTRUN1: Timer 1 RUN/STOP control register (FFC5H•D0)

PTRUN2: Timer 2 RUN/STOP control register (FFC6H•D0)

PTRUN3: Timer 3 RUN/STOP control register (FFC7H•D0)

Controls the RUN/STOP of the counter.

When "1" is written: RUN

When "0" is written: STOP

Reading: Valid

The counter of each timer starts counting down by writing "1" to the PTRUN register and stops by writing "0". In STOP status, the counter data is maintained until the counter is reset or is set in the next RUN status. When STOP status changes to RUN status, the data that has been maintained can be used for resuming the count.

In the 16-bit mode, the counter is controlled by the PTRUN register of the low-order 8-bit side (PTRUN0, PTRUN2). In this case, writing to the PTRUN register of the high-order 8-bit side (PTRUN1, PTRUN3) is invalid.

At initial reset, these registers are set to "0".

CHSEL0, CHSEL1: PTOUT output channel selection register (FFC2H•D0, D1)

Selects the channel used for PTOUT signal output.

Table 4.8.7.3 Selection of PTOUT output channel

CHSEL1	CHSEL0	PTOUT output Ch
1	1	Timer 3
1	0	Timer 2
0	1	Timer 1
0	0	Timer 0

The specified timer generates the PTOUT signal by its underflow.

In the 16-bit mode, the PTOUT signal is generated using underflow from the high-order 8-bit counter.

Therefore, CHSEL must be set to timer 1 or timer 3.

At initial reset, these registers are set to "0".

PTOUT: PTOUT output control register (FFC2H•D2)

Turns PTOUT signal output ON and OFF.

When "1" is written: ON

When "0" is written: OFF

Reading: Valid

PTOUT is the output control register for the PTOUT signal. When "1" is written to the register, the PTOUT signal is output from the output port terminal R02 and when "0" is written, the terminal goes to a high (VDD) level. However, the data register R02 must always be "1" and the high impedance control register R02HIZ must always be "0" (data output state).

At initial reset, this register is set to "0".

EIPT0: Timer 0 interrupt mask register (FFE2H•D0)**EIPT1: Timer 1 interrupt mask register (FFE2H•D1)****EIPT2: Timer 2 interrupt mask register (FFE2H•D2)****EIPT3: Timer 3 interrupt mask register (FFE2H•D3)**

Masks the the programmable timer interrupt.

When "1" is written: Enabled

When "0" is written: Masked

Reading: Valid

Timer interrupts can be masked individually by the interrupt mask register EIPT.

At initial reset, these registers are set to "0".

IPT0: Timer 0 interrupt factor flag (FFF2H•D0)**IPT1: Timer 1 interrupt factor flag (FFF2H•D1)****IPT2: Timer 2 interrupt factor flag (FFF2H•D2)****IPT3: Timer 3 interrupt factor flag (FFF2H•D3)**

These flags indicate the status of the programmable timer interrupt.

When "1" is read: Interrupt has occurred

When "0" is read: Interrupt has not occurred

When "1" is written: Flag is reset

When "0" is written: Invalid

The interrupt factor flags IPT0–IPT3 correspond to timers 0–3 interrupts, respectively. The software can judge from these flags whether there is a programmable timer interrupt. However, even if the interrupt is masked, the flags are set to "1" by the underflows of the corresponding counters.

In the 16-bit mode, the high-order 8-bit counter (timer 1, timer 3) generates an interrupt by its underflow.

In this case, the interrupt factor flag of low-order 8-bit side (timer 0, timer 2) is not set.

These flags are reset to "0" by writing "1" to them.

After an interrupt occurs, the same interrupt will occur again if the interrupt enabled state (I flag = "1") is set or the RETI instruction is executed unless the interrupt factor flag is reset. Therefore, be sure to reset (write "1" to) the interrupt factor flag in the interrupt service routine before shifting to the interrupt enabled state.

At initial reset, these flags are set to "0".

4.8.8 Programming notes

- (1) When reading the counter data, be sure to read the low-order 4 bits first.
In the 16-bit mode, read data in order of low-order 4 bits and high-order 4 bits of timer 0 (timer 2) then low-order 4 bits and high-order 4 bits of timer 1 (timer 3).
- (2) The programmable timer actually enters RUN/STOP status in synchronization with the falling edge of the input clock after writing to the PTRUN register. Consequently, when "0" is written to the PTRUN register, the timer enters STOP status at the point where the counter is decremented (-1). The PTRUN register maintains "1" for reading until the timer actually stops.
Figure 4.8.8.1 shows the timing chart for the RUN/STOP control.

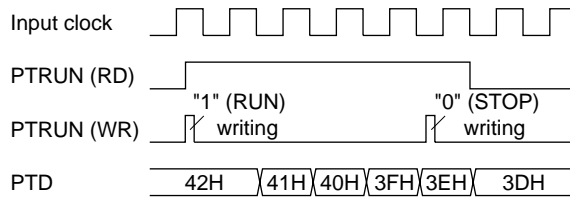


Fig. 4.8.8.1 Timing chart for RUN/STOP control

It is the same even in the event counter mode. Therefore, be aware that the counter does not enter RUN/STOP status if a clock is not input after setting the RUN/STOP control register (PTRUN0).

- (3) Since the PTOUT signal is generated asynchronously from the PTOUT register, a hazard within 1/2 cycle is generated when the signal is turned ON and OFF by setting the register.
- (4) After an interrupt occurs, the same interrupt will occur again if the interrupt enabled state (I flag = "1") is set or the RETI instruction is executed unless the interrupt factor flag is reset. Therefore, be sure to reset (write "1" to) the interrupt factor flag in the interrupt service routine before shifting to the interrupt enabled state.

4.9 Buzzer Output Circuit

4.9.1 Configuration of buzzer output circuit

The E0C63256 is capable of generating buzzer signal to drive a piezo-electric buzzer. The buzzer signal is output from the BZ terminal by software control. Furthermore, the buzzer signal frequency can be set to 2 kHz or 4 kHz by software.

Figure 4.9.1.1 shows the configuration of the buzzer output circuit.

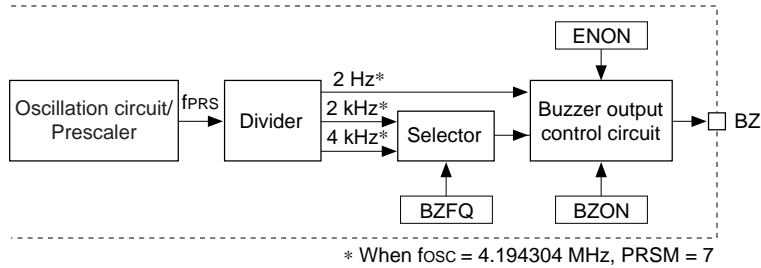
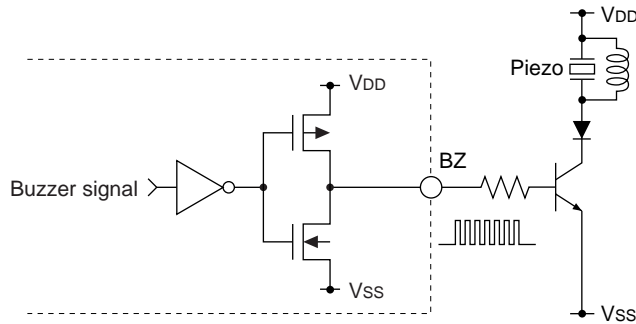


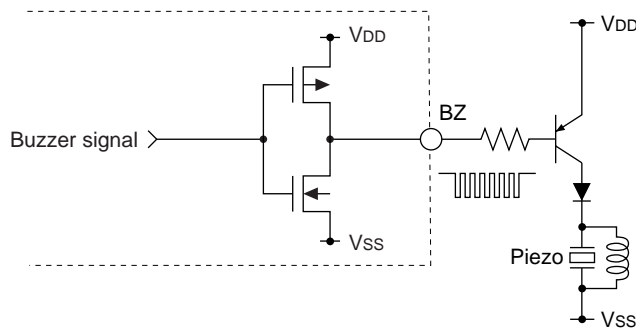
Fig. 4.9.1.1 Configuration of buzzer output circuit

4.9.2 Mask option

Polarity of the buzzer signal output from the BZ terminal can be selected as either positive polarity or negative polarity. Figure 4.9.2.1 shows each output circuit configuration and the output waveform. When positive polarity is selected, the BZ terminal goes to a low (Vss) level when the buzzer signal is not output. Select positive polarity when driving a piezo buzzer by externally connecting an NPN transistor. When negative polarity is selected, the BZ terminal goes to a high (VDD) level when the buzzer signal is not output. Select negative polarity when driving a piezo buzzer by externally connecting a PNP transistor.



(a) When positive polarity is selected



(b) When negative polarity is selected

Fig. 4.9.2.1 Configuration of output circuit

4.9.3 Control of buzzer output

(1) Buzzer frequency

The buzzer signal frequency is selected by the buzzer frequency selection register BZFQ. When "1" is written to the BZFQ register, the frequency is set to 2 kHz. When "0" is written, it is set to 4 kHz. The buzzer signal frequency varies according to the oscillation frequency and setting of the prescaler (PRSM). It is calculated by the expression below.

$$f_{BZL} = \frac{f_{OSC}}{256 \cdot n} \text{ [Hz]} \quad f_{BZL}: \text{ Buzzer frequency when BZFQ} = "1"$$

$$f_{BZH} = \frac{f_{OSC}}{128 \cdot n} \text{ [Hz]} \quad f_{BZH}: \text{ Buzzer frequency when BZFQ} = "0"$$

f_{OSC} : Oscillation clock frequency
 n : PRSM register setting value + 1

Examples

In case of $f_{OSC} = 4.194304 \text{ MHz}$ and $PRSM = 7$: $f_{BZL} = 2048 \text{ Hz}$, $f_{BZH} = 4096 \text{ Hz}$
 In case of $f_{OSC} = 2 \text{ MHz}$ and $PRSM = 3$: $f_{BZL} = 1953 \text{ Hz}$, $f_{BZH} = 3906 \text{ Hz}$

Refer to Section 4.2, "Oscillation Circuit and Prescaler", for setting of the prescaler.

(2) Buzzer output control

The buzzer signal is output from the BZ terminal by writing "1" to the buzzer output control register BZON. When negative polarity is selected, the BZ terminal goes to a high (V_{DD}) level by writing "0" to the BZON register. When positive polarity is selected, the BZ terminal goes to a low (V_{SS}) level by writing "0".

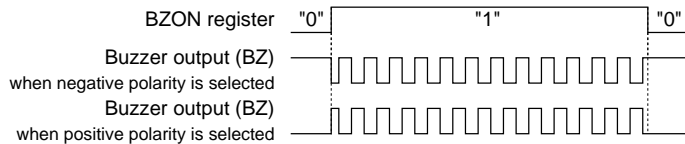


Fig. 4.9.3.1 Timing chart of buzzer signal output

Note: Since it generates a buzzer signal that is out of synchronization with the BZON register, hazards may at times be produced when the signal goes ON/OFF due to the setting of the BZON register.

(3) 2 Hz interval

Besides the normal consecutive output, the buzzer output circuit can generate an intermittent buzzer sound by modulating the buzzer signal with a 2 Hz signal. Write "1" to the ENON register when using the 2 Hz interval function. The ENON register only switches the 2 Hz interval function ON and OFF. To output the buzzer signal, control of the BZON register is necessary.

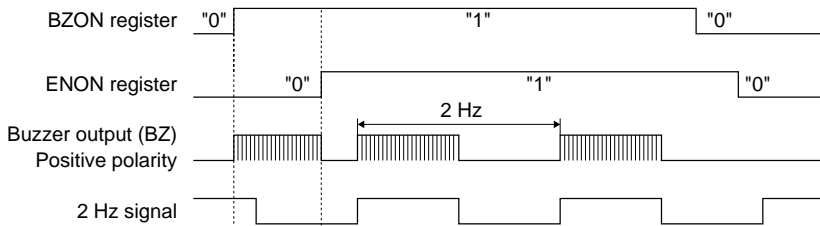


Fig. 4.9.3.2 2 Hz interval

The 2 Hz signal also varies according to the oscillation frequency and setting of the prescaler (PRSM).

$$f_{IVL} = \frac{f_{OSC}}{262144 \cdot n} \text{ [Hz]} \quad f_{IVL}: \text{ Interval frequency}$$

$$f_{OSC}: \text{ Oscillation clock frequency}$$

n : PRSM register setting value + 1

Examples

In case of $f_{OSC} = 4.194304 \text{ MHz}$ and $PRSM = 7$: $f_{IVL} = 2 \text{ Hz}$
 In case of $f_{OSC} = 2 \text{ MHz}$ and $PRSM = 3$: $f_{IVL} = 1.9 \text{ Hz}$

Refer to Section 4.2, "Oscillation Circuit and Prescaler", for setting of the prescaler.

4.9.4 I/O memory of buzzer output circuit

Table 4.9.4.1 shows the I/O address and the control bits for the buzzer output circuit.

Table 4.9.4.1 Control bits of buzzer output circuit

Address	Register								Comment
	D3	D2	D1	D0	Name	Init *1	1	0	
FF64H	0	ENON	BZFQ	BZON	0 *3	- *2			Unused
					ENON	0	On	Off	2 Hz interval On/Off
					BZFQ	0	2 kHz	4 kHz	Buzzer frequency selection
	R	R/W			BZON	0	On	Off	Buzzer output On/Off

*1 Initial value at initial reset

*2 Not set in the circuit

*3 Constantly "0" when being read

ENON: 2 Hz interval control (ON/OFF) register (FF64H•D2)

Turns the 2 Hz interval function ON and OFF.

When "1" is written: ON

When "0" is written: OFF

Reading: Valid

When "1" is written to ENON, 2 Hz intermittent buzzer signal output mode is set. When "0" is written, normal consecutive output mode is set.

The 2 Hz signal varies according to the oscillation frequency and setting of the prescaler (see Section 4.9.3).

At initial reset, this register is set to "0".

BZFQ: Buzzer frequency selection register (FF64H•D1)

Selects the buzzer signal frequency.

When "1" is written: 2 kHz

When "0" is written: 4 kHz

Reading: Valid

When "1" is written to BZFQ, the frequency is set to 2 kHz. When "0" is written, it is set to 4 kHz.

The buzzer frequency varies according to the oscillation frequency and setting of the prescaler (see Section 4.9.3).

At initial reset, this register is set to "0".

BZON: Buzzer output control (ON/OFF) register (FF64H•D0)

Controls the buzzer signal output.

When "1" is written: Buzzer output ON

When "0" is written: Buzzer output OFF

Reading: Valid

When "1" is written to BZON, the buzzer signal is output from the BZ terminal. When "0" is written, the BZ terminal goes to a high (VDD) level (when negative polarity is selected by mask option) or to a low (Vss) level (when positive polarity is selected by mask option).

At initial reset, this register is set to "0".

4.9.5 Programming note

Since it generates a buzzer signal that is out of synchronization with the BZON register, hazards may at times be produced when the signal goes ON/OFF due to the setting of the BZON register.

4.10 A/D Converter

4.10.1 Characteristics and configuration of A/D converter

The E0C63256 has a built-in A/D converter with the following characteristics.

- Conversion method: Successive-approximation type
- Resolution: 8 bits
- Input channels: Maximum 4 channels
- Conversion time: Minimum 8 μ sec ($f_{AD} = 2.5$ MHz)
- Setting of analog conversion voltage range is possible with reference voltage terminal (AV_{REF})
- A/D conversion result is possible to read from 8-bit data register
- Sample & hold circuit built-in
- A/D conversion completion generates an interrupt

Figure 4.10.1.1 shows the configuration of the A/D converter.

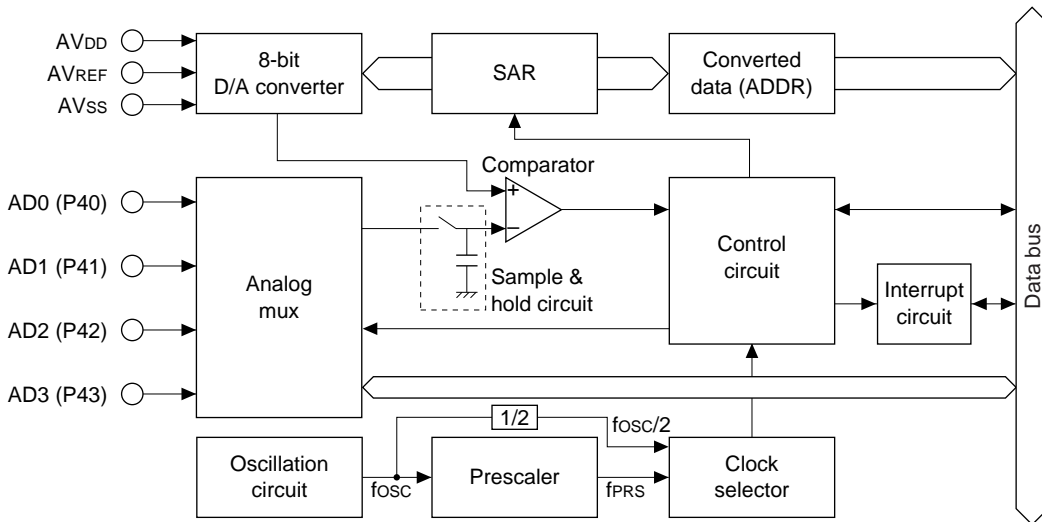


Fig. 4.10.1.1 Configuration of A/D converter

4.10.2 Terminal configuration of A/D converter

The terminals used with the A/D converter are as follows:

AV_{DD} , AV_{SS} (power supply terminal)

The AV_{DD} and AV_{SS} terminals are power supply terminals for the A/D converter. The voltage should be input as $AV_{DD} \leq V_{DD}$ and $AV_{SS} = V_{SS}$.

AV_{REF} (reference voltage input terminal)

The AV_{REF} terminal is the reference voltage terminal of the analog block. Input voltage range of the A/D conversion is decided by this input ($AV_{SS} - AV_{REF}$). The voltage should be input as $AV_{REF} \leq AV_{DD}$.

AD0–AD3 (analog input terminal)

The analog input terminals AD0–AD3 are shared with the I/O port terminals P40–P43. Therefore, it is necessary to set them for the A/D converter by software when using them as analog input terminals. This setting can be done for each terminal. (Refer to Section 4.10.4 for setting.)

At initial reset, all the terminals are set in the I/O port terminals.

Analog voltage value AV_{IN} that can be input is in the range of $AV_{SS} \leq AV_{IN} \leq AV_{REF}$.

4.10.3 Mask option

The input terminals of the A/D converter are shared with the I/O port terminals P40–P43. Therefore, the terminal specification of the A/D converter is decided by setting the I/O port mask option. Select "Without pull-up" for the port corresponding to the channel to be used to obtain the conversion precision.

4.10.4 Control of A/D converter

(1) Setting of A/D input terminal

When using the A/D converter, it is necessary to set up the terminals used for analog input from the P40–P43 initialized as the I/O port terminals. Four terminals can all be used as analog input terminals.

The PAD (PAD0–PAD3) register is used to set analog input terminals. When the PAD register bits are set to "1", the corresponding terminals function as the analog input terminals.

At initial reset, these terminals are all set in the I/O port terminals, and each terminal goes to a high impedance.

Table 4.10.4.1 Correspondence between A/D input terminal and PAD register

Terminal	A/D input enable register	Comment
P40 (AD0)	PAD0	Terminals can be used for analog input by setting PADx to "1".
P41 (AD1)	PAD1	
P42 (AD2)	PAD2	
P43 (AD3)	PAD3	

(2) Setting of input clock

Two types of A/D conversion clock are available: a prescaler output clock (f_{PRS}) or a clock ($f_{OSC}/2$) that has a halved oscillation frequency. One or the other can be selected using the ADCLK register as shown in Table 4.10.4.2.

Table 4.10.4.2 Input clock selection

ADCLK	Input clock
0	f_{PRS}
1	$f_{OSC}/2$

The clock selector outputs the selected clock to the A/D converter by writing "1" to the ADRUN register.

When f_{PRS} is selected, the clock that is output from the prescaler according to the PRSM register value is input to the A/D converter as the A/D conversion clock.

$$f_{PRS} = f_{OSC}/(PRSM + 1) \text{ [Hz]}$$

Examples

In case of $f_{OSC} = 4.194304 \text{ MHz}$ and $PRSM = 7$: 262.144 kHz

In case of $f_{OSC} = 2 \text{ MHz}$ and $PRSM = 3$: 250 kHz

Refer to Section 4.2, "Oscillation Circuit and Prescaler", for setting of the prescaler.

- Note:**
- Stop A/D conversion before changing the ADCLK register. Switching the input clock during A/D conversion may cause a malfunction.
 - When f_{PRS} is selected as the input clock, do not change the setting of the prescaler during A/D conversion. It may cause a malfunction.

(3) Input signal selection

The analog signals from the AD0 (P40)–AD3 (P43) terminals are input to the multiplexer, and the analog input channel for A/D conversion is selected by software. This selection can be done using the CHS register as shown in Table 4.10.4.3.

Table 4.10.4.3 Selection of analog input channel

CHS1	CHS0	Input channel
1	1	AD3 (P43)
1	0	AD2 (P42)
0	1	AD1 (P41)
0	0	AD0 (P40)

(4) A/D conversion operation

An A/D conversion starts by writing to the ADRUN register.

For example, when performing A/D conversion using AD1 as the analog input, write "1" (0, 1) to the CHS register (CHS1, CHS0). The A/D input channel is selected by this operation. However, it is necessary that the P41 terminal has been set as an analog input terminal.

Then write "1" to the ADRUN register. The built-in sample/hold circuit starts sampling of the analog input specified from t_{AD} after writing. When the sampling is completed, the held analog input voltage is converted into a 8-bit digital value in successive-approximation architecture.

The conversion result is loaded into the ADDR register (ADDR0–ADDR7) register. ADDR0 is the LSB and ADDR7 is the MSB.

Note: If the CHS register selects an input channel which is not included in the analog input terminals set by the PAD register (the PAD register can select several terminals simultaneously), the A/D conversion does not result in a correct converted value.

Example

Terminal setting: PAD3=1, PAD2–PAD0=0 (AD3 terminal is used)

Selection of input channel: CHS1=0, CHS0=0 (AD0 is selected)

In a setting like this, the A/D conversion result will be invalid because the contents of the settings are not matched.

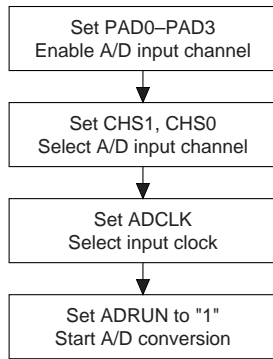


Fig. 4.10.4.1 Flowchart for starting A/D conversion

An A/D conversion is completed when the conversion result is loaded into the ADDR register. At that point, the A/D converter generates an interrupt (explained in the next section).

Figure 4.10.4.2 shows the timing chart of A/D conversion.

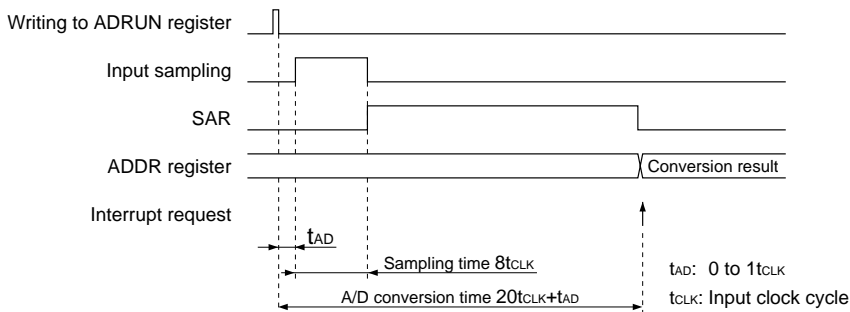


Fig. 4.10.4.2 Timing chart of A/D conversion

CHS0, CHS1: Analog input channel selection register (FF68H•D0, D1)

Selects an analog input channel.

Table 4.10.6.3 Selection of analog input channel

CHS1	CHS0	Input channel
1	1	AD3 (P43)
1	0	AD2 (P42)
0	1	AD1 (P41)
0	0	AD0 (P40)

At initial reset, this register is set to "0".

ADCLK: A/D converter clock source selection register (FF68H•D2)

Selects the clock source for the A/D converter.

When "1" is written: Oscillation clock frequency / 2 ($f_{OSC} / 2$)

When "0" is written: Prescaler output clock (f_{PRS})

Reading: Valid

When "1" is written to ADCLK, a halved oscillation clock is selected as the A/D conversion clock. When "0" is written, a prescaler output clock is selected.

At initial reset, ADCLK register is set to "0" (f_{PRS}).

ADRUN: A/D conversion control (FF68H•D3)

Starts an A/D conversion.

When "1" is written: Start

When "0" is written: No operation

Reading: Invalid

When "1" is written to ADRUN, the channel that has been specified by the CHS register starts A/D conversion. See Figure 4.10.4.2 for A/D conversion time (from starting A/D conversion until the conversion result is loaded to the ADDR register). When "0" is written, no operation results.

This bit is dedicated for writing, and is always "0" for reading.

ADDR0–ADDR7: A/D conversion result (FF6AH, FF6BH)

8-bit A/D conversion results are stored.

ADDR0 is the LSB and ADDR7 is the MSB.

At initial reset, data is undefined.

EIAD: A/D converter interrupt mask register (FFE7H•D0)

Masks the A/D converter interrupt.

When "1" is written: Enabled

When "0" is written: Masked

Reading: Valid

This register is used to select whether the A/D converter interrupt is masked or not.

At initial reset, this register is set to "0".

IAD: A/D converter interrupt factor flag (FFF7H•D0)

This flag indicates the status of the A/D converter interrupt.

When "1" is read: Interrupt has occurred

When "0" is read: Interrupt has not occurred

When "1" is written: Flag is reset

When "0" is written: Invalid

From the status of the interrupt factor flag IAD, the software can decide whether an A/D converter interrupt has occurred or not.

The interrupt factor flag is set to "1" when an A/D conversion has finished regardless of the interrupt mask register setting. However, the interrupt does not occur to the CPU when the interrupt is masked. This flag is reset to "0" by writing "1".

After an interrupt occurs, the same interrupt will occur again if the interrupt enabled state (I flag = "1") is set or the RETI instruction is executed unless the interrupt factor flag is reset. Therefore, be sure to reset (write "1" to) the interrupt factor flag in the interrupt service routine before shifting to the interrupt enabled state.

At initial reset, this flag is set to "0".

4.10.7 Programming notes

- (1) When using the prescaler as the clock source of the A/D converter, A/D conversion time will vary according to the setting of the prescaler.
- (2) The analog input terminals should be set when the A/D converter stops. Changing during A/D conversion may cause malfunction.
- (3) If the CHS register selects an input channel which is not included in the analog input terminals set by the PAD register (the PAD register can select several terminals simultaneously), the A/D conversion does not result in a correct converted value.
- (4) During A/D conversion, do not operate the P4n terminals which are not used for analog inputs of the A/D converter (for input/output of digital signals). It affects the A/D conversion precision.
- (5) Stop A/D conversion before changing the ADCLK register. Switching the input clock during A/D conversion may cause malfunction.
- (6) When fPRS is selected as the input clock, do not change the setting of the prescaler during A/D conversion. It may cause a malfunction.
- (7) After an interrupt occurs, the same interrupt will occur again if the interrupt enabled state (I flag = "1") is set or the RETI instruction is executed unless the interrupt factor flag is reset. Therefore, be sure to reset (write "1" to) the interrupt factor flag in the interrupt service routine before shifting to the interrupt enabled state.

4.11 Interrupt and HALT/SLEEP

<Interrupt types>

The E0C63256 provides the following interrupt functions.

External interrupt:	• Input interrupt	(1 system)
Internal interrupt:	• Watchdog timer interrupt	(NMI, 1 system)
	• Programmable timer interrupt	(4 systems)
	• Clock timer interrupt	(1 system)
	• A/D converter interrupt	(1 system)

To authorize interrupt, the interrupt flag must be set to "1" (EI) and the necessary related interrupt mask registers must be set to "1" (enable).

When an interrupt occurs the interrupt flag is automatically reset to "0" (DI), and interrupts after that are inhibited.

The watchdog timer interrupt is an NMI (non-maskable interrupt), therefore, the interrupt is generated regardless of the interrupt flag setting. Also the interrupt mask register is not provided. However, it is possible to not generate NMI since software can stop the watchdog timer operation.

Figure 4.11.1 shows the configuration of the interrupt circuit.

Note: After an initial reset, all the interrupts including NMI are masked until both the stack pointers SP1 and SP2 are set with the software. Be sure to set the SP1 and SP2 in the initialize routine. Further, when re-setting the stack pointer, the SP1 and SP2 must be set as a pair. When one of them is set, all the interrupts including NMI are masked and interrupts cannot be accepted until the other one is set.

<HALT/SLEEP>

The E0C63256 has HALT and SLEEP functions that considerably reduce current consumption when it is not necessary.

The CPU enters HALT status when the HALT instruction is executed.

In HALT status, the operation of the CPU is stopped. However, timers continue counting since the oscillation circuit operates. Reactivating the CPU from HALT status is done by generating a hardware interrupt request including NMI.

When shifted into SLEEP status as the result of a SLP instruction, the operation of the CPU is stopped, the same as for HALT status, and the oscillation circuit also stops.

Reactivating from SLEEP status can only be done by generation of a K0 port input interrupt request. Therefore, it is necessary to set the interrupt selection register (SIK0x = "1") of the input port to be used for releasing SLEEP status, the K0 system interrupt mask register (EIK0x = "1") and the interrupt flag (I flag = "1") to enabled status before executing the SLP instruction.

When the SLEEP status is canceled by a K0 port input interrupt, wait for oscillation to stabilize, then restart the CPU operation (K0 port input interrupt processing).

Refer to the "E0C63000 Core CPU Manual" for transition to the HALT/SLEEP status and timing of its cancellation.

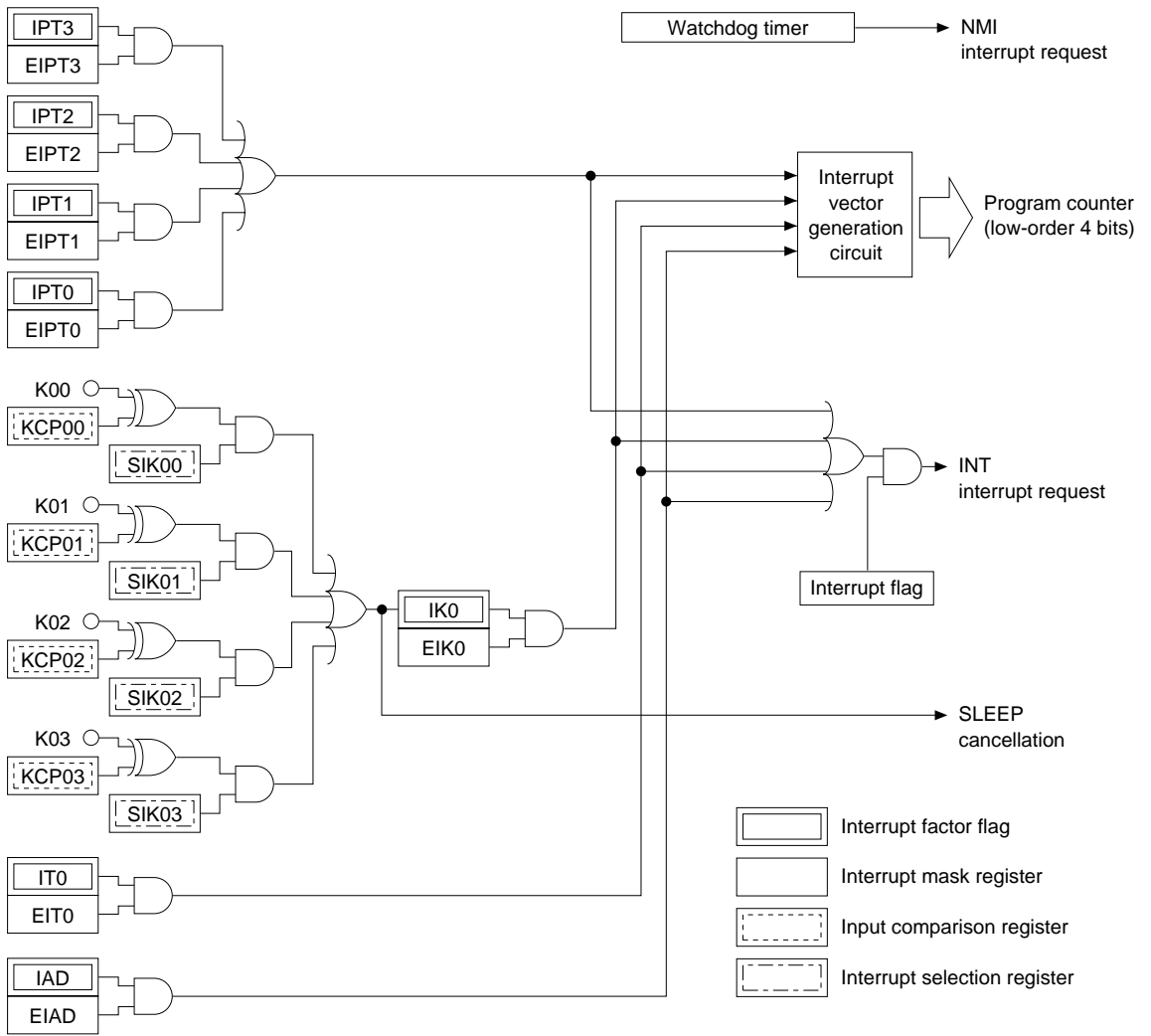


Fig. 4.11.1 Configuration of the interrupt circuit

4.11.1 Interrupt factor

Table 4.11.1.1 shows the factors for generating interrupt requests.

The interrupt flags are set to "1" depending on the corresponding interrupt factors.

The CPU operation is interrupted when an interrupt factor flag is set to "1" if the following conditions are established.

- The corresponding mask register is "1" (enabled)
- The interrupt flag is "1" (EI)

The interrupt factor flag is reset to "0" when "1" is written.

At initial reset, the interrupt factor flags are reset to "0".

* Since the watchdog timer's interrupt is NMI, the interrupt is generated regardless of the setting above, and no interrupt factor flag is provided.

Table 4.11.1.1 Interrupt factors

Interrupt factor	Interrupt factor flag
Programmable timer 3 (counter = 0)	IPT3 (FFF2H•D3)
Programmable timer 2 (counter = 0)	IPT2 (FFF2H•D2)
Programmable timer 1 (counter = 0)	IPT1 (FFF2H•D1)
Programmable timer 0 (counter = 0)	IPT0 (FFF2H•D0)
K00–K03 input (falling edge or rising edge)	IK0 (FFF4H•D0)
Clock timer 1 Hz (falling edge)	IT0 (FFF6H•D0)
A/D converter (A/D conversion completion)	IAD (FFF7H•D0)

Note: After an interrupt occurs, the same interrupt will occur again if the interrupt enabled state (I flag = "1") is set or the RETI instruction is executed unless the interrupt factor flag is reset. Therefore, be sure to reset (write "1" to) the interrupt factor flag in the interrupt service routine before shifting to the interrupt enabled state.

4.11.2 Interrupt mask

The interrupt factor flags can be masked by the corresponding interrupt mask registers.

The interrupt mask registers are read/write registers. They are enabled (interrupt authorized) when "1" is written to them, and masked (interrupt inhibited) when "0" is written to them.

At initial reset, the interrupt mask register is set to "0".

Table 4.11.2.1 shows the correspondence between interrupt mask registers and interrupt factor flags.

Table 4.11.2.1 Interrupt mask registers and interrupt factor flags

Interrupt mask register	Interrupt factor flag
EIPT3 (FFE2H•D3)	IPT3 (FFF2H•D3)
EIPT2 (FFE2H•D2)	IPT2 (FFF2H•D2)
EIPT1 (FFE2H•D1)	IPT1 (FFF2H•D1)
EIPT0 (FFE2H•D0)	IPT0 (FFF2H•D0)
EIK0 (FFE4H•D0)	IK0 (FFF4H•D0)
EIT0 (FFE6H•D0)	IT0 (FFF6H•D0)
EIAD (FFE7H•D0)	IAD (FFF7H•D0)

4.11.3 Interrupt vector

When an interrupt request is input to the CPU, the CPU begins interrupt processing. After the program being executed is terminated, the interrupt processing is executed in the following order.

- 1 The content of the flag register is evacuated, then the I flag is reset.
- 2 The address data (value of program counter) of the program to be executed next is saved in the stack area (RAM).
- 3 The interrupt request causes the value of the interrupt vector (0100H–010EH) to be set in the program counter.
- 4 The program at the specified address is executed (execution of interrupt processing routine by software).

Table 4.11.3.1 shows the correspondence of interrupt requests and interrupt vectors.

Table 4.11.3.1 Interrupt request and interrupt vectors

Interrupt vector	Interrupt factor	Priority
0100H	Watchdog timer	High ↑
0102H	–	
0104H	Programmable timer	↓ Low
0106H	–	
0108H	K00–K03 input	
010AH	–	
010CH	Clock timer	
010EH	A/D converter	

The four low-order bits of the program counter are indirectly addressed through the interrupt request.

4.11.4 I/O memory of interrupt

Table 4.11.4.1 shows the I/O addresses and the control bits for controlling interrupts.

Table 4.11.4.1 Control bits of interrupt

Address	Register				Name	Init *1	1	0	Comment
	D3	D2	D1	D0					
FF20H	SIK03	SIK02	SIK01	SIK00	SIK03	0	Enable	Disable	K00–K03 interrupt selection register
					SIK02	0	Enable	Disable	
	R/W				SIK01	0	Enable	Disable	
	R/W				SIK00	0	Enable	Disable	
FF22H	KCP03	KCP02	KCP01	KCP00	KCP03	1	↓	↑	K00–K03 input comparison register
					KCP02	1	↓	↑	
	R/W				KCP01	1	↓	↑	
	R/W				KCP00	1	↓	↑	
FFE2H	EIPT3	EIPT2	EIPT1	EIPT0	EIPT3	0	Enable	Mask	Interrupt mask register (Programmable timer 3)
					EIPT2	0	Enable	Mask	Interrupt mask register (Programmable timer 2)
	R/W				EIPT1	0	Enable	Mask	Interrupt mask register (Programmable timer 1)
	R/W				EIPT0	0	Enable	Mask	Interrupt mask register (Programmable timer 0)
FFE4H	0	0	0	EIK0	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R			R/W	0 *3	– *2			Unused
	R			R/W	EIK0	0	Enable	Mask	Interrupt mask register (K00–K03)
FFE6H	0	0	0	EIT0	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R			R/W	0 *3	– *2			Unused
	R			R/W	EIT0	0	Enable	Mask	Interrupt mask register (Clock timer 1 Hz)
FFE7H	0	0	0	EIAD	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R			R/W	0 *3	– *2			Unused
	R			R/W	EIAD	0	Enable	Mask	Interrupt mask register (A/D converter)
FFF2H	IPT3	IPT2	IPT1	IPT0	IPT3	0	(R)	(R)	Interrupt factor flag (Programmable timer 3)
					IPT2	0	Yes	No	Interrupt factor flag (Programmable timer 2)
	R/W				IPT1	0	(W)	(W)	Interrupt factor flag (Programmable timer 1)
	R/W				IPT0	0	Reset	Invalid	Interrupt factor flag (Programmable timer 0)
FFF4H	0	0	0	IK0	0 *3	– *2	(R)	(R)	Unused
					0 *3	– *2	Yes	No	Unused
	R			R/W	0 *3	– *2	(W)	(W)	Unused
	R			R/W	IK0	0	Reset	Invalid	Interrupt factor flag (K00–K03)
FFF6H	0	0	0	IT0	0 *3	– *2	(R)	(R)	Unused
					0 *3	– *2	Yes	No	Unused
	R			R/W	0 *3	– *2	(W)	(W)	Unused
	R			R/W	IT0	0	Reset	Invalid	Interrupt factor flag (Clock timer 1 Hz)
FFF7H	0	0	0	IAD	0 *3	– *2	(R)	(R)	Unused
					0 *3	– *2	Yes	No	Unused
	R			R/W	0 *3	– *2	(W)	(W)	Unused
	R			R/W	IAD	0	Reset	Invalid	Interrupt factor flag (A/D converter)

*1 Initial value at initial reset

*2 Not set in the circuit

*3 Constantly "0" when being read

EIPT3, EIPT2, EIPT1, EIPT0: Interrupt mask registers (FFE2H)

IPT3, IPT2, IPT1, IPT0: Interrupt factor flags (FFF2H)

Refer to Section 4.8, "Programmable Timer".

KCP03–KCP00: Input comparison registers (FF22H)

SIK03–SIK00: Interrupt selection registers (FF20HH)

EIK0: Interrupt mask register (FFE4H•D0)

IK0: Interrupt factor flag (FFF4H•D0)

Refer to Section 4.3, "Input Ports".

EIT0: Interrupt mask register (FFE6H•D0)

IT0: Interrupt factor flag (FFF6H•D0)

Refer to Section 4.7, "Clock Timer and Watchdog Timer".

EIAD: Interrupt mask register (FFE7H•D0)

IAD: Interrupt factor flag (FFF7H•D0)

Refer to Section 4.10, "A/D Converter".

4.11.5 Programming notes

- (1) The interrupt factor flags are set when the interrupt condition is established, even if the interrupt mask registers are set to "0".
- (2) After an interrupt occurs, the same interrupt will occur again if the interrupt enabled state (I flag = "1") is set or the RETI instruction is executed unless the interrupt factor flag is reset. Therefore, be sure to reset (write "1" to) the interrupt factor flag in the interrupt service routine before shifting to the interrupt enabled state.
- (3) After an initial reset, all the interrupts including NMI are masked until both the stack pointers SP1 and SP2 are set with the software. Be sure to set the SP1 and SP2 in the initialize routine. Further, when re-setting the stack pointer, the SP1 and SP2 must be set as a pair. When one of them is set, all the interrupts including NMI are masked and interrupts cannot be accepted until the other one is set.
- (4) The input interrupt must be enabled before shifting to SLEEP status.

CHAPTER 5 SUMMARY OF NOTES

Here, the cautionary notes are summed up by function category. Keep these notes well in mind when programming.

Memory and stack

- (1) Memory is not implemented in unused areas within the memory map. Further, some non-implementation areas and unused (access prohibition) areas exist in the peripheral I/O area. If the program that accesses these areas is generated, its operation cannot be guaranteed. Refer to the I/O memory maps shown in Tables 4.1.1 (a)–(d) for the peripheral I/O area.
- (1) All of the RAM area is used as a stack area for subroutine call and register evacuation, so pay attention not to overlap the data area and stack area.
- (2) The E0C63000 core CPU handles the stack using the stack pointer for 4-bit data (SP2) and the stack pointer for 16-bit data (SP1).
The stack pointers SP1 and SP2 change cyclically within their respective range: the range of SP1 is 0000H to 03FFH and the range of SP2 is 0000H to 00FFH. Therefore, pay attention to the SP1 value because it may be set to 0100H or more exceeding the RAM area in the E0C63256. Memory accesses except for stack operations by SP1 are 4-bit data access.
After initial reset, all the interrupts including NMI are masked until both the stack pointers SP1 and SP2 are set by software. Further, if either SP1 or SP2 is re-set when both are set already, the interrupts including NMI are masked again until the other is re-set. Therefore, the settings of SP1 and SP2 must be done as a pair.

Oscillation circuit and prescaler

The peripheral circuits may not operate normally if the prescaler is not set properly.

Input port

- (1) When input ports are changed from low to high by pull-up resistors, the rise of the waveform is delayed on account of the time constant of the pull-up resistor and input gate capacitance. Hence, when fetching input ports, set an appropriate waiting time.
Particular care needs to be taken of the key scan during key matrix configuration.
Make this waiting time the amount of time or more calculated by the following expression.
Waiting time = $R_{IN} \times (C_{IN} + C_L) \times 1.6$ [sec]
 R_{IN} : Pull-up resistance Max. value
 C_{IN} : Terminal capacitance Max. value
 C_L : Load capacitance on the board
- (2) The K03 terminal functions as the clock input terminal for the programmable timer, and the input signal is shared with the input port and the programmable timer. Therefore, when the K03 terminal is set to the clock input terminal for the programmable timer, take care of the interrupt setting.

Output port

- (1) When using the output port (R02, R03) as the special output port, fix the data register (R02, R03) at "1" and the high impedance control register (R02HIZ, R03HIZ) at "0" (data output).
Be aware that the output terminal is fixed at a low (V_{SS}) level the same as the DC output if "0" is written to the R02 and R03 registers when the special output has been selected.
Be aware that the output terminal shifts into high impedance status when "1" is written to the high impedance control register (R02HIZ, R03HIZ).
- (2) A hazard may occur when the FOUT signal and the PTOUT signal are turned ON and OFF.
- (3) The FOUT frequency varies according to the oscillation frequency and setting of the prescaler (PRSM register). Refer to Section 4.2, "Oscillation Circuit and Prescaler", for setting of the prescaler.

I/O port

When the I/O port terminal is changed from low to high by the pull-up resistor in the input mode, the rise of the waveform is delayed on account of the time constant of the pull-up resistor and input gate capacitance. Hence, when fetching input ports, set an appropriate wait time.

Particular care needs to be taken of the key scan during key matrix configuration.

Make this waiting time the amount of time or more calculated by the following expression.

Waiting time = $R_{IN} \times (C_{IN} + C_L) \times 1.6$ [sec]

R_{IN} : Pull-up resistance Max. value

C_{IN} : Terminal capacitance Max. value

C_L : Load capacitance on the board

LCD driver

The contents of the display memory are undefined until the area is initialized (through, for instance, memory clear processing by the CPU). Initialize the display memory by executing initial processing.

Clock timer and watchdog timer

(1) To operate the clock timer accurately, the prescaler must be set correctly.

When using the clock timer for clock function, use a 4.194304 MHz crystal oscillator and set the PRSM register of the prescaler to 7. An accurate 1 Hz signal cannot be obtained in other conditions.

(2) When the watchdog timer is used, the software must reset the watchdog timer before an overflow occurs.

(3) Because the watchdog timer is set in operation state by initial reset, set the watchdog timer to disabled state (not used) before generating an interrupt (NMI) if it is not used.

Programmable timer

(1) When reading the counter data, be sure to read the low-order 4 bits first.

In the 16-bit mode, read data in order of low-order 4 bits and high-order 4 bits of timer 0 (timer 2) then low-order 4 bits and high-order 4 bits of timer 1 (timer 3).

(2) The programmable timer actually enters RUN/STOP status in synchronization with the falling edge of the input clock after writing to the PTRUN register. Consequently, when "0" is written to the PTRUN register, the timer enters STOP status at the point where the counter is decremented (-1). The PTRUN register maintains "1" for reading until the timer actually stops.

Figure 5.1 shows the timing chart for the RUN/STOP control.

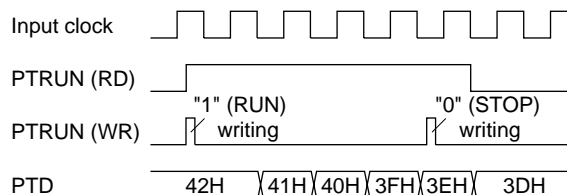


Fig. 5.1 Timing chart for RUN/STOP control

It is the same even in the event counter mode. Therefore, be aware that the counter does not enter RUN/STOP status if a clock is not input after setting the RUN/STOP control register (PTRUN0).

(3) Since the PTOUT signal is generated asynchronously from the PTOUT register, a hazard within 1/2 cycle is generated when the signal is turned ON and OFF by setting the register.

Buzzer output circuit

Since it generates a buzzer signal that is out of synchronization with the BZON register, hazards may at times be produced when the signal goes ON/OFF due to the setting of the BZON register.

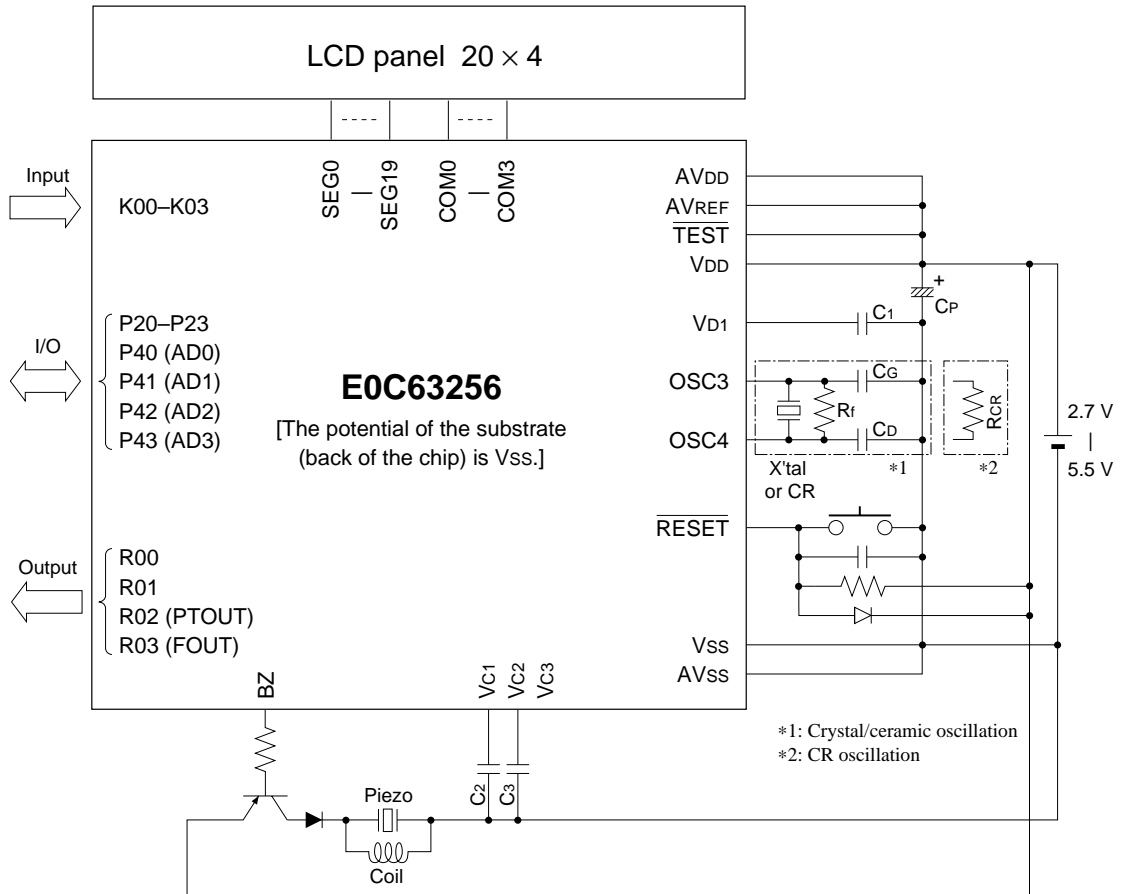
A/D converter

- (1) When using the prescaler as the clock source of the A/D converter, A/D conversion time will vary according to the setting of the prescaler.
- (2) The analog input terminals should be set when the A/D converter stops. Changing during A/D conversion may cause malfunction.
- (3) If the CHS register selects an input channel which is not included in the analog input terminals set by the PAD register (the PAD register can select several terminals simultaneously), the A/D conversion does not result in a correct converted value.
- (4) During A/D conversion, do not operate the P4n terminals which are not used for analog inputs of the A/D converter (for input/output of digital signals). It affects the A/D conversion precision.
- (5) Stop A/D conversion before changing the ADCLK register. Switching the input clock during A/D conversion may cause malfunction.
- (6) When fPRS is selected as the input clock, do not change the setting of the prescaler during A/D conversion. It may cause a malfunction.

Interrupt

- (1) The interrupt factor flags are set when the interrupt condition is established, even if the interrupt mask registers are set to "0".
- (2) After an interrupt occurs, the same interrupt will occur again if the interrupt enabled state (I flag = "1") is set or the RETI instruction is executed unless the interrupt factor flag is reset. Therefore, be sure to reset (write "1" to) the interrupt factor flag in the interrupt service routine before shifting to the interrupt enabled state.
- (3) After an initial reset, all the interrupts including NMI are masked until both the stack pointers SP1 and SP2 are set with the software. Be sure to set the SP1 and SP2 in the initialize routine. Further, when re-setting the stack pointer, the SP1 and SP2 must be set as a pair. When one of them is set, all the interrupts including NMI are masked and interrupts cannot be accepted until the other one is set.
- (4) The input interrupt must be enabled before shifting to SLEEP status.

CHAPTER 6 BASIC EXTERNAL WIRING DIAGRAM



X'tal	Crystal oscillator	4.194304 MHz
CR	Ceramic oscillator	4.0 MHz
CG	Gate capacitor	15 pF (Crystal oscillation) 30 pF (Ceramic oscillation)
CD	Drain capacitor	15 pF (Crystal oscillation) 30 pF (Ceramic oscillation)
Rf	Feedback resistor	1 MΩ
RCR	Resistor for CR oscillation	20 kΩ (2 MHz)
C1	Capacitor	0.1 μF
C2, C3	Capacitor	0.1 μF
CP		3.3 μF

- * The connection diagram shown above is an example of when mask option settings are as follows:
 Buzzer signal: Negative polarity
 LCD power source: Internal LCD power supply (external Vc3 not used)

- Note:
- The above table is simply an example. Refer to Chapter 7, "Electrical Characteristics", for detailed characteristics.
 - Capacitors should be connected to the Vc1, Vc2 and Vc3 terminals for noise measure and to prevent reduction in LCD display quality. (These terminals do not necessarily have to be connected to a capacitor.)
 - To interrupt current that flows in the resistor (analog reference resistor) connected between the AVREF and AVSS terminals, use a switching transistor from outside the IC.

CHAPTER 7 ELECTRICAL CHARACTERISTICS

7.1 Absolute Maximum Rating

(Vss=0V)						
Item	Symbol	Condition	Rated value	Unit	Note	
Supply voltage	VDD		-0.3 to +7.0	V		
LCD supply voltage	Vc		-0.3 to +7.0	V		
Input voltage	VI		-0.3 to VDD+0.3	V		
Output voltage	Vo		-0.3 to VDD+0.3	V	1	
High-level output current	IOH	1 terminal	-5	mA		
		Total of all terminals	-20	mA		
Low-level output current	IOL	1 terminal	5	mA		
		Total of all terminals	20	mA		
Operating temperature	Topr		-20 to +85	°C		
Storage temperature	Tstg		-65 to +150	°C		
Soldering temperature / time	Tsol		260°C, 10sec (lead section)	-		
Permissible dissipation	PD		250	mW	2	

- Note) 1. It is applied to the output voltage when Nch open drain is selected by mask option.
2. In case of plastic package.

7.2 Recommended Operating Conditions

(Vss=AVss=0V, Ta=-20 to 85°C)								
Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note	
Supply voltage	VDD	VDD	2.7	3.0/5.0	5.5	V		
LCD supply voltage	VC3I	VC3	2.7		5.5	V	1	
	VC3E	VC3	2.7		5.5	V	2	
	VC2E	1/3 bias	VC2	Typ. - 0.2	VC3:2/3	Typ. + 0.2	V	2
		1/2 bias	VC2	Typ. - 0.2	VC3:1/2	Typ. + 0.2	V	2
	VC1E	1/3 bias	VC1	Typ. - 0.2	VC3:1/3	Typ. + 0.2	V	2
		1/2 bias	VC1	Typ. - 0.2	VC3:1/2	Typ. + 0.2	V	2
Analog supply voltage	VAVDD	AVDD	2.7		VDD	V		
Analog reference voltage range	VREF	AVREF	2.7		AVDD	V		
Analog input voltage range	VIN	AD0 to AD3 (P40 to P43)	AVss		AVREF	V		
Operating frequency	fosc	VDD=2.7 to 5.5V	Crystal oscillation circuit	0.5	4.194	4.5	MHz	3,4
			Ceramic oscillation circuit	0.5	4.0	4.5	MHz	3
			CR oscillation circuit	0.5	2.0	2.5	MHz	3
			External clock input	0.5	4.0	4.5	MHz	3,5

- Note) 1. When "Internal power (external VC3 is used)" is selected by mask option.
2. When "External power" is selected by mask option.
3. The CPU uses the clock output from the oscillation circuit as the operating clock.
4. Crystal oscillator = 4.194304 MHz
5. When an external clock is input from the OSC3 terminal by setting the mask option, do not connect anything to the OSC4 terminal.

7.3 DC Characteristics

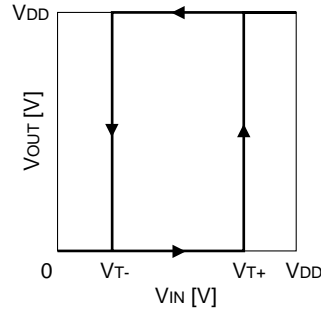
7.3.1 Input characteristics

Unless otherwise specified: $V_{DD}=2.7$ to $5.5V$, $V_{SS}=0V$, $T_a=-20$ to $85^{\circ}C$

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
High-level input voltage	V_{IH1}	Kxx, Pxx	$0.7 \cdot V_{DD}$		V_{DD}	V	
	V_{IH2}	OSC3	1.7		V_{DD}	V	1
Low-level input voltage	V_{IL1}	Kxx, Pxx	0		$0.3 \cdot V_{DD}$	V	
	V_{IL2}	OSC3	0		0.7	V	1
High-level schmitt input voltage	V_{T+}	\overline{RESET}	$0.5 \cdot V_{DD}$		$0.9 \cdot V_{DD}$	V	
Low-level schmitt input voltage	V_{T-}		$0.1 \cdot V_{DD}$		$0.5 \cdot V_{DD}$	V	
Input leak current	I_{LIH}	$V_{LIH}=V_{DD}$	0		1.0	μA	
	I_{LIL}	$V_{LIL}=V_{SS}$					
Input pull-up resistance	R_{IN}	Kxx, Pxx	100	250	400	$k\Omega$	
		\overline{RESET}	250	450	650	$k\Omega$	
Input terminal capacitance	C_{IN}	$V_{IN}=0V$, $f=1MHz$		10	15	pF	

Note) 1. When "External clock" is selected by mask option.

2. When "with pull-up resistor" is selected by mask option.



7.3.2 Output characteristics

Unless otherwise specified: $V_{DD}=2.7$ to $5.5V$, $V_{SS}=0V$, $V_{C3}=2.7$ to $5.5V$, V_{C2}/V_{C1} are internal voltage, $T_a=-20$ to $85^{\circ}C$, $C_2=C_3=0.1\mu F$

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
High-level output voltage	I_{OH1}	$V_{OH1}=0.9 \cdot V_{DD}$, $V_{DD}=5.0V$	Pxx, Rxx	5.3		mA	3
		$V_{OH1}=0.9 \cdot V_{DD}$, $V_{DD}=3.0V$		2.5		mA	3
	I_{OH2}	$V_{OH2}=0.9 \cdot V_{DD}$, $V_{DD}=5.0V$	BZ	5.3		mA	3
		$V_{OH2}=0.9 \cdot V_{DD}$, $V_{DD}=3.0V$		2.5		mA	3
	I_{OH3}	$V_{OH3}=0.9 \cdot V_{DD}$, $V_{DD}=5.0V$	SEGxx (during DC output)	1.2		mA	1,3
		$V_{OH3}=0.9 \cdot V_{DD}$, $V_{DD}=3.0V$		0.6		mA	1,3
Low-level output voltage	I_{OL1}	$V_{OL1}=0.1 \cdot V_{DD}$, $V_{DD}=5.0V$	Pxx, Rxx	8.5		mA	4
		$V_{OL1}=0.1 \cdot V_{DD}$, $V_{DD}=3.0V$		4.1		mA	4
	I_{OL2}	$V_{OL2}=0.1 \cdot V_{DD}$, $V_{DD}=5.0V$	BZ	8.5		mA	4
		$V_{OL2}=0.1 \cdot V_{DD}$, $V_{DD}=3.0V$		4.1		mA	4
	I_{OL3}	$V_{OL3}=0.1 \cdot V_{DD}$, $V_{DD}=5.0V$	SEGxx (during DC output)	1.4		mA	1,4
		$V_{OL3}=0.1 \cdot V_{DD}$, $V_{DD}=3.0V$		0.7		mA	1,4
Output leak current	I_{LOH}	$V_{LOH}=V_{DD}$	0		1.0	μA	
	I_{LOL}	$V_{LOL}=V_{SS}$	-1.0		0	μA	
Common output current	I_{COMH}	$V_{COMH}=V_{C3}-0.05V$	COMx			-5	μA
	I_{COML}	$V_{COML}=V_{SS}+0.05V$		5		μA	
Segment output current	I_{SEGH}	$V_{SEGH}=V_{C3}-0.05V$	SEGxx (during LCD output)			-5	μA
	I_{SEGL}	$V_{SEGL}=V_{SS}+0.05V$		5		μA	2

Note) 1. When "DC output" is selected by mask option.

2. When "LCD output" is selected by mask option.

3. See Section 7.8, "Characteristic curves", for the maximum values.

4. See Section 7.8, "Characteristic curves", for the minimum values.

7.4 Analog Circuit Characteristics

7.4.1 LCD drive voltage characteristics

Unless otherwise specified: $V_{DD}=2.7$ to $5.5V$, $V_{SS}=0V$, V_{C2}/V_{C1} are internal voltage, $T_a=-20$ to $85^{\circ}C$, $C_2=C_3=0.1\mu F$

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
LCD supply voltage	VC31	VC3	2.7		5.5	V	1
LCD drive voltage (when 1/3 bias is selected)	VC1	Connect 1 MΩ load resistor between VSS or VDD and VC1 (without panel load)	Typ. - 0.2	VC3:1/3	Typ. + 0.2	V	2
	VC2	Connect 1 MΩ load resistor between VSS or VDD and VC2 (=VC2) (without panel load)	Typ. - 0.2	VC3:2/3	Typ. + 0.2	V	2
LCD drive voltage (when 1/2 bias is selected)	VC1&2	Connect 1 MΩ load resistor between VSS or VDD and VC1(=VC2)(without panel load), VC1 and VC2 are shorted	Typ. - 0.2	VC3:1/2	Typ. + 0.2	V	2
Built-in resistance	RLCD	Resistance between VC3 and VSS	30	50	100	kΩ	2

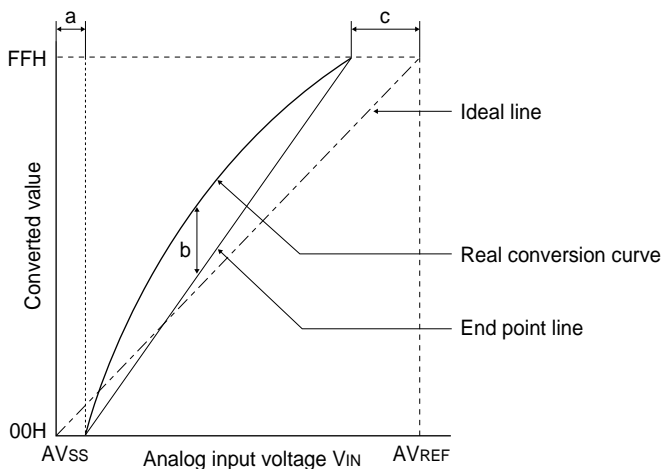
- Note) 1. When "Internal power (external VC3 is used)" is selected by mask option.
 2. VC3 = VDD when "Internal power (external VC3 is not used)" is selected by mask option.

7.4.2 A/D conversion characteristics

Unless otherwise specified: $V_{DD}=2.7$ to $5.5V$, $V_{SS}=AV_{SS}=0V$, $T_a=-20$ to $85^{\circ}C$

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Analog supply voltage	VAVDD	AVDD	2.7		VDD	V	
Analog reference voltage range	VREF	AVREF	2.7		AVDD	V	
Analog input voltage range	VIN	AD0 to AD3 (P40 to P43)	AVSS		AVREF	V	
Analog input capacitance	CAIN	During sampling AD0 to AD3 (P40 to P43)		35	60	pF	
Analog reference resistance	RREF	Resistance for AVREF-AVSS	10	20	30	kΩ	
Resolution	-				8	bit	
Offset error	E _{OFF}	AVDD=2.7V to VDD	-1		1	LSB	1
Full scale error	E _{FS}	AVREF=2.7V to AVDD	-1		1	LSB	1
Non-linearity error	E _{LI}	f _{AD} =240kHz to 2.5MHz	-2		4	LSB	1,2
Overall error	E _T		-2		4	LSB	1,2
A/D conversion time	t _{ADC}	f _{AD} =240kHz to 2.5MHz	20		21	clock	1
Sampling time	t _{SMP}	f _{AD} =240kHz to 2.5MHz		8		clock	1

- Note) 1. $f_{AD}=f_{PRS}=f_{OSC}/2n$ or $f_{AD}=f_{OSC}/2$ (f_{AD}: A/D conversion clock frequency, f_{OSC}: oscillation clock frequency, n=1-16: PRSM setting value + 1)
 2. The best straight line within a ±3LSB of error can be obtained by correcting the conversion result with -1LSB by software.



- Offset error : $E_{OFF} = a$ (the deviation from the ideal value at zero point)
 Non-linearity error : $E_{LI} = b$ (the deviation of the real conversion curve from the end point line)
 Full scale error : $E_{FS} = c$ (the deviation from the ideal value at the full scale point)
- Total error : $E_T = \max(E_{OFF}, E_{LI}, E_{ABS})$
 E_{ABS} = the deviation from the ideal line (including quantizing error)

7.5 Current Consumption

Unless otherwise specified: $V_{DD}=AV_{DD}=AV_{REF}=2.7$ to $5.5V$, $V_{SS}=AV_{SS}=0V$, $T_a=25^{\circ}C$, $C_1=0.1\mu F$, $C_2=C_3=0.1\mu F$

Item	Symbol	Condition		Min.	Typ.	Max.	Unit	Note
Power current during SLEEP	ISLP				0.3	1.0	μA	
Power current during HALT	IHALT	LCD system circuit and A/D converter are not used	Crystal oscillation (4.194304MHz)		560	1200	μA	1,4,7
			Ceramic oscillation (4.0MHz)		610	1400	μA	2,4,7
			CR oscillation (2MHz)		680	1400	μA	3,4,7
			External clock input (4.0MHz)		220	420	μA	4,7
Power current during execution	IEXE	LCD system circuit and A/D converter are not used Software duty = 100%	Crystal oscillation (4.194304MHz)		1400	2600	μA	1,5,7
			Ceramic oscillation (4.0MHz)		1400	2600	μA	2,5,7
			CR oscillation (2MHz)		1100	2100	μA	3,5,7
			External clock input (4.0MHz)		1000	1700	μA	5,7
LCD system operating current	ILCD	$V_{DD}=V_{C3}=3.0V$, no panel load			60	100	μA	8
		$V_{DD}=V_{C3}=5.0V$, no panel load			100	170	μA	8
A/D conversion operating current	IADC	$V_{DD}=AV_{DD}=AV_{DD}=3.0V$, $f_{AD}=TBDkHz$			600	1000	μA	6
		$V_{DD}=AV_{DD}=AV_{DD}=5.0V$, $f_{AD}=TBDkHz$			1800	3000	μA	6

Note) 1. $R_f=1M\Omega$, $C_G=C_D=15pF$

2. $R_f=1M\Omega$, $C_G=C_D=30pF$

3. $R_{CR}=20k\Omega$

4. OSC: oscillated (except for external clock input) CPU, ROM, RAM: HALT status Others: stopped

5. OSC: oscillated (except for external clock input) CPU, ROM, RAM: operating Others: stopped

6. $f_{AD}=f_{PRS}=f_{OSC}/2n$ (f_{AD} : A/D conversion clock frequency, f_{OSC} : oscillation clock frequency, $n=1-16$: PRSM setting value + 1)
 $f_{OSC}=4.194304MHz$, $PRSM=7$

7. Current consumption when the LCD system circuit or A/D converter is used is found by adding the LCD system operating current or the A/D conversion current.

8. When "Internal power" is selected by mask option.

7.6 AC Characteristics

7.6.1 Operating range

Unless otherwise specified: $V_{DD}=2.7$ to $5.5V$, $V_{SS}=0V$, $T_a=-20$ to $85^{\circ}C$

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Operating clock frequency	fosc	Crystal oscillation circuit	0.5		4.5	MHz	1
		Ceramic oscillation circuit	0.5		4.5	MHz	1
		CR oscillation circuit	0.5		2.5	MHz	1
		External clock input	0.5		4.5	MHz	1,2
Instruction execution time	tcy	1-cycle instruction	0.44 (0.8)		4.0	μS	3
		2-cycle instruction	0.89 (1.6)		8.0	μS	3
		3-cycle instruction	1.33 (2.4)		12.0	μS	3

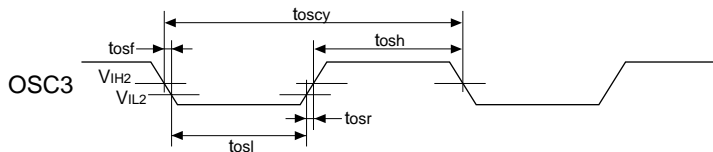
- Note) 1. The CPU uses the clock output from the oscillation circuit as the operating clock.
 2. When an external clock is input from the OSC3 terminal by setting the mask option, do not connect anything to the OSC4 terminal.
 3. The values enclosed with () indicate the execution time when the CR oscillation circuit is used.

7.6.2 Input clock

OSC3 external clock

Unless otherwise specified: $V_{DD}=2.7$ to $5.5V$, $V_{SS}=0V$, $T_a=-20$ to $85^{\circ}C$, $V_{IH2}=1.7V$, $V_{IL2}=0.7V$

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Input clock cycle time	toscy		230		2,000	nS	
Input clock "H" pulse width	tosh		115		1,000	nS	
Input clock "L" pulse width	tosl		115		1,000	nS	
Input clock rising time	tosr				25	nS	
Input clock falling time	tosf				25	nS	

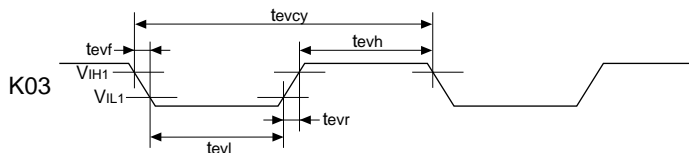


K03 external clock (event counter external clock)

Unless otherwise specified: $V_{DD}=2.7$ to $5.5V$, $V_{SS}=0V$, $T_a=-20$ to $85^{\circ}C$, $V_{IH1}=0.8 \cdot V_{DD}$, $V_{IL1}=0.2 \cdot V_{DD}$

Item	Symbol	Condition	Min.	Max.	Unit	Note
Input clock cycle time	tevcy	With noise rejecter	$512 \cdot n / f_{osc}$		S	1
Input clock "H" pulse width	tevh		$256 \cdot n / f_{osc}$		S	1
Input clock "L" pulse width	tevl		$256 \cdot n / f_{osc}$		S	1
Input clock cycle time	tevcy	Without noise rejecter	4		μS	
Input clock "H" pulse width	tevh		2		μS	
Input clock "L" pulse width	tevl		2		μS	
Input clock rising time	tsr			25	nS	
Input clock falling time	tsf			25	nS	

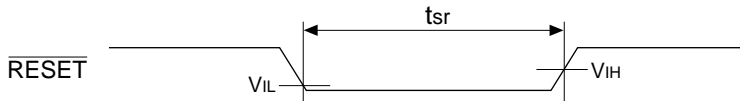
- Note) 1. fosc: oscillation clock frequency, n=1-16: PRSM setting value + 1



RESET input clock

Unless otherwise specified: $V_{DD}=2.7$ to $5.5V$, $V_{SS}=0V$, $T_a=-20$ to $85^{\circ}C$, $V_{IH}=0.5 \cdot V_{DD}$, $V_{IL}=0.1 \cdot V_{DD}$

Item	Symbol	Condition	Min.	Max.	Unit	Note
RESET input time	tsr		100		μS	



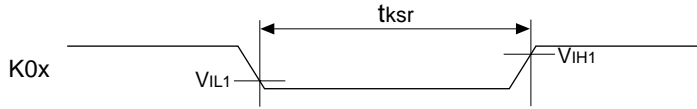
K00–K03 simultaneous low input clock

Unless otherwise specified: $V_{DD}=2.7$ to $5.5V$, $V_{SS}=0V$, $T_a=-20$ to $85^{\circ}C$, $V_{IH}=0.8 \cdot V_{DD}$, $V_{IL}=0.2 \cdot V_{DD}$

Item	Symbol	Condition	Min.	Max.	Unit	Note
Simultaneous low input time	tksr	Time authorize circuit is used	524288-n/fosc		S	1
		Time authorize circuit is not used	768-n/fosc		S	1

Note) 1. fosc: oscillation clock frequency, n=1–16: PRSM setting value + 1

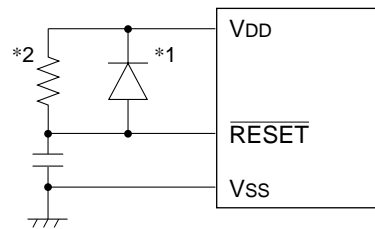
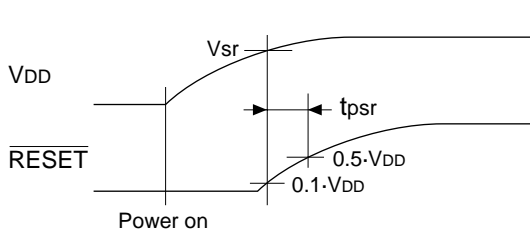
When the simultaneous low input reset function is selected by mask option.



7.6.3 Power-on reset

Unless otherwise specified: $V_{SS}=0V$, $T_a=-20$ to $85^{\circ}C$, $V_{IH}=0.5 \cdot V_{DD}$, $V_{IL}=0.1 \cdot V_{DD}$

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Operating power voltage	Vsr	RESET=0.1·VDD	2.7			V	
RESET input time	tpsr		100			μS	



*1 Because the potential of the RESET terminal not reached VDD level or higher.

*2 When the built-in pull-up resistor is not used.

7.6.4 A/D conversion characteristics

Unless otherwise specified: $V_{DD}=2.7$ to $5.5V$, $V_{SS}=AV_{SS}=0V$, $T_a=-20$ to $85^{\circ}C$

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
A/D conversion time	tADC	fAD=240kHz to 2.5MHz	20		21	clock	1
Sampling time	tsmp	fAD=240kHz to 2.5MHz		8		clock	1

Note) 1. fAD=fPRS=fOSC/2n or fAD=fOSC/2 (fAD: A/D conversion clock frequency, fOSC: oscillation clock frequency, n=1–16: PRSM setting value + 1)

7.7 Oscillation Characteristics

Oscillation characteristics change depending on conditions (board pattern, components used, etc.). Use the following characteristics as reference values. In particular, when a ceramic oscillator or crystal oscillator is used, use the oscillator manufacturer's recommended values for constants such as capacitance and resistance.

7.7.1 Crystal oscillation circuit

Unless otherwise specified: $V_{DD}=2.7$ to $5.5V$, $V_{SS}=0V$, $T_a=-20$ to $85^{\circ}C$, Crystal oscillator: CA301 4.194304MHz *, $R_f=1M\Omega$, $C_G=C_D=15pF$

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Oscillation start voltage	Vsta		2.7			V	
Oscillation start time	tsta				20	mS	1
Oscillation stop voltage	Vstp		2.7			V	
Built-in gate capacitance	C_G			16		pF	
Built-in drain capacitance	C_D			13		pF	
Frequency/IC deviation	$\partial f/\partial IC$		-10		10	ppm	
Frequency/supply voltage deviation	$\partial f/\partial V$				1	ppm /V	
Permitted leak resistance	R_{leak}	Between OSC1 and Vss	200			M Ω	

* CA301 4.194304MHz: made by Seiko Epson

Note) 1. The crystal oscillation start time varies according to the crystal oscillator, C_G and C_D to be used.

7.7.2 Ceramic oscillation circuit

Unless otherwise specified: $V_{DD}=2.7$ to $5.5V$, $V_{SS}=0V$, $T_a=-20$ to $85^{\circ}C$, Ceramic oscillator: CSA 4.00MG *, $R_f=1M\Omega$, $C_G=C_D=30pF$

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Oscillation start voltage	Vsta		2.7			V	
Oscillation start time	tsta				5	mS	
Oscillation stop voltage	Vstp		2.7			V	

* CSA 4.00MG: made by Murata Mfg. Co.

7.7.3 CR oscillation circuit

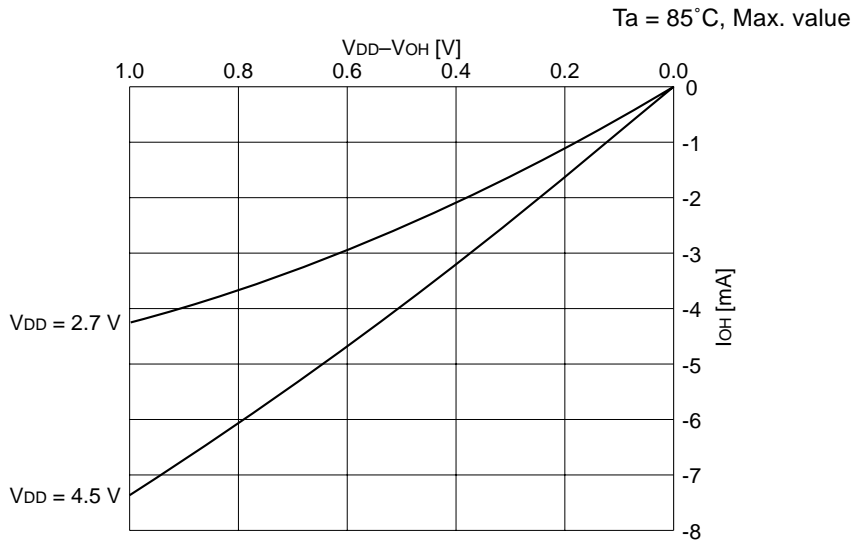
Unless otherwise specified: $V_{DD}=2.7$ to $5.5V$, $V_{SS}=0V$, $T_a=-20$ to $85^{\circ}C$

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Oscillation start voltage	Vsta		2.7			V	
Oscillation start time	tsta				1	mS	
Oscillation stop voltage	Vstp		2.7			V	
Frequency/IC deviation	$\partial f/\partial IC$	RCR = constant	-25		25	%	

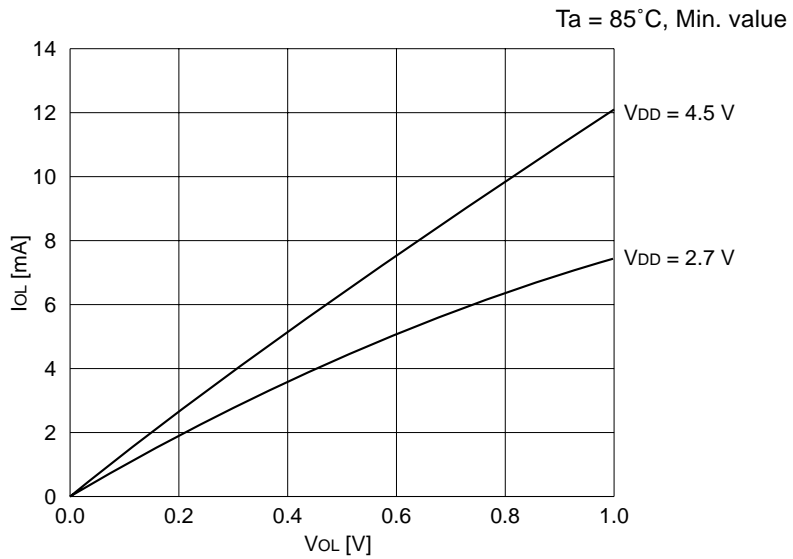
7.8 Characteristic Curves (reference value)

7.8.1 Output current characteristics

High level output current (Pxx, Rxx, BZ)

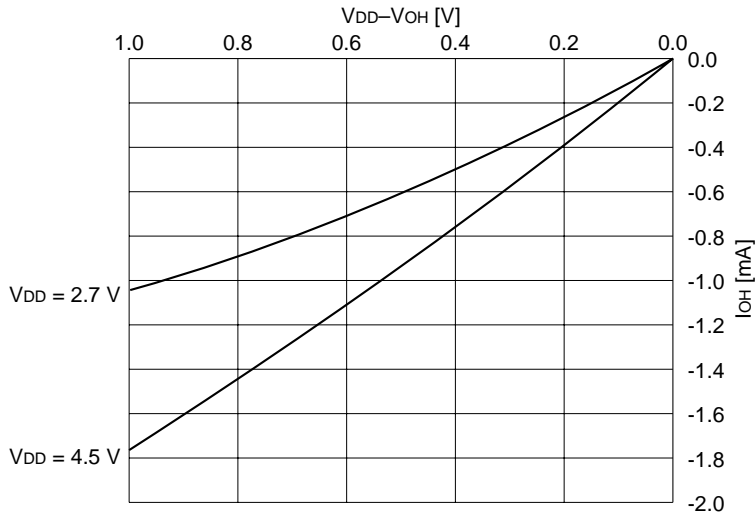


Low level output current (Pxx, Rxx, BZ)



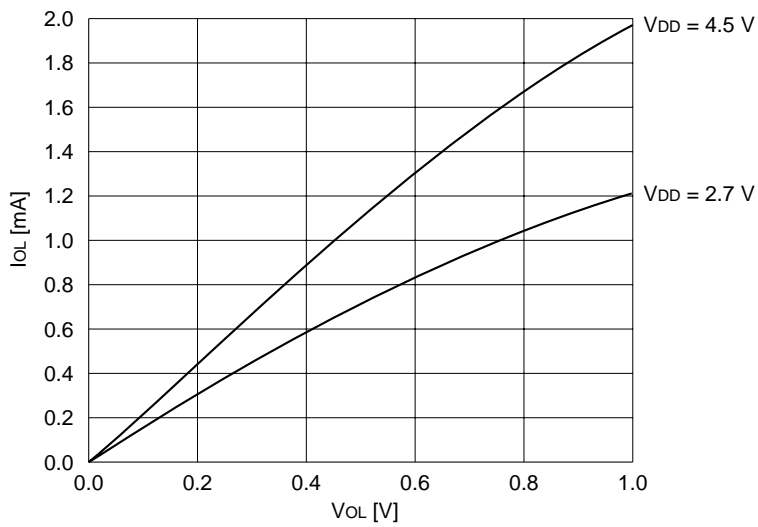
High level output current (SEGxx)

Ta = 85°C, Max. value



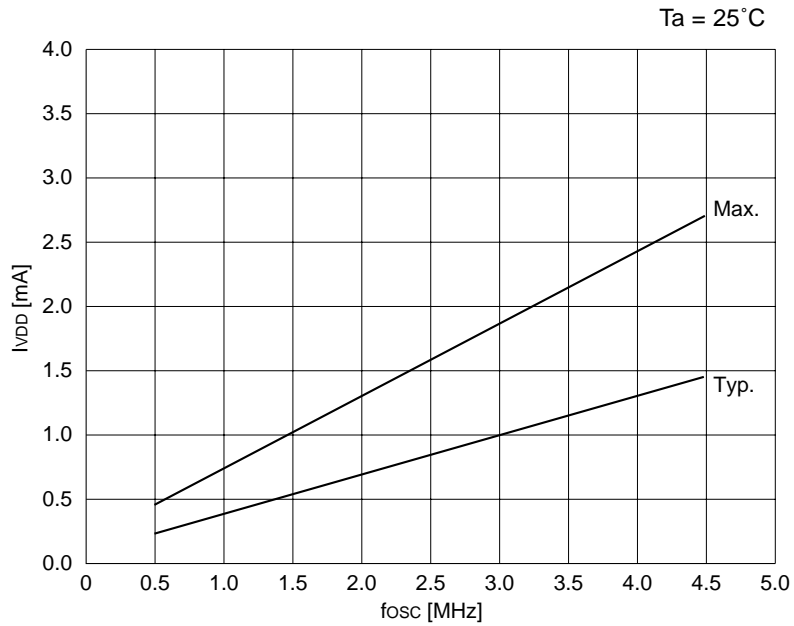
Low level output current (SEGxx)

Ta = 85°C, Min. value

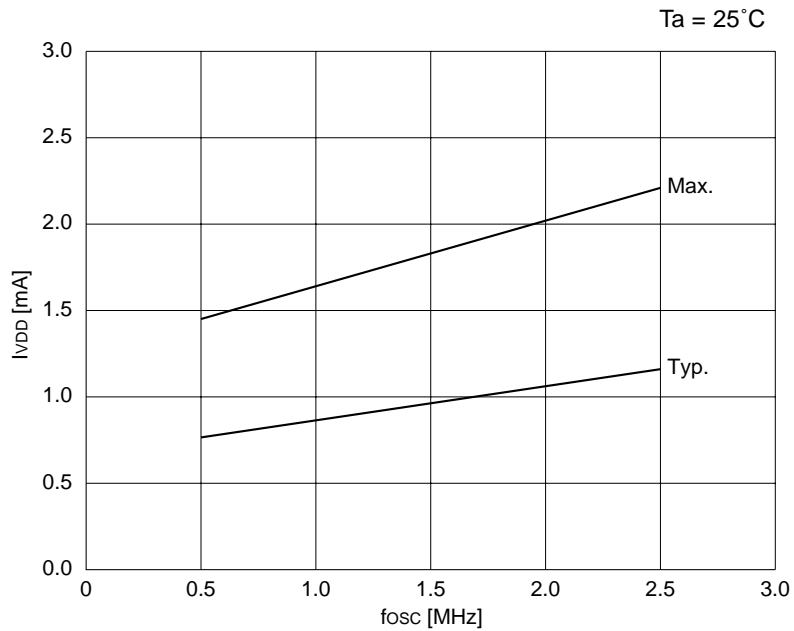


7.8.2 Power current - frequency characteristics

Crystal oscillation/ceramic oscillation (during operation)

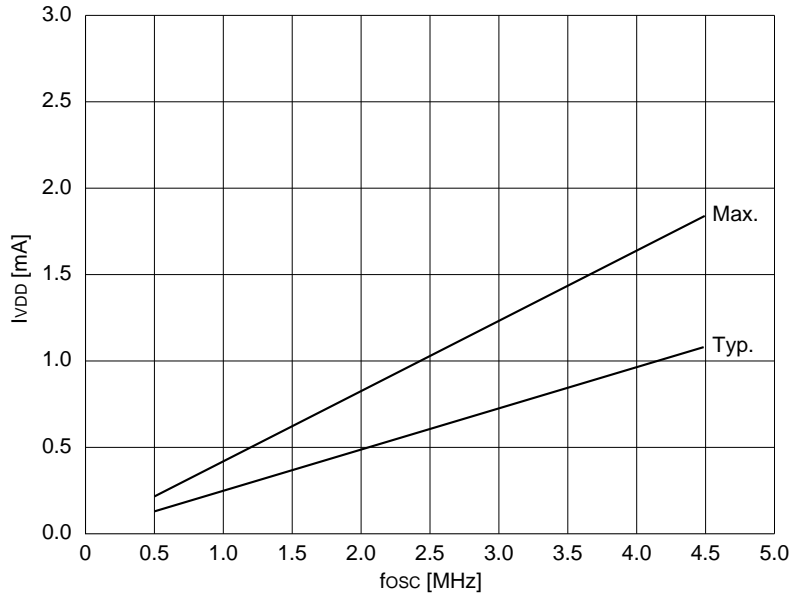


CR oscillation (during operation)



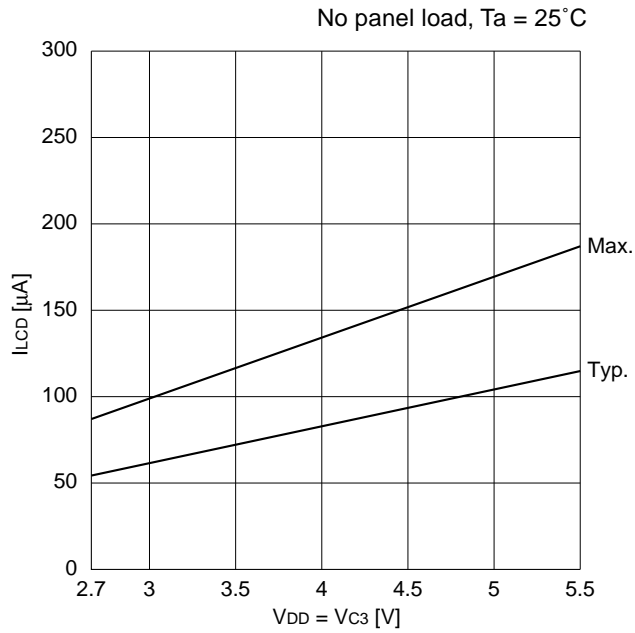
External clock (during operation)

Ta = 25°C



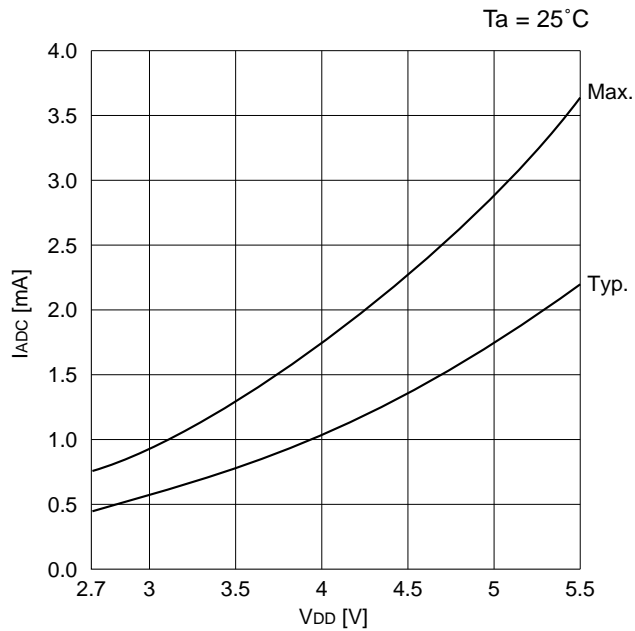
7.8.3 Analog system operating current - voltage characteristic

LCD system operating current



A/D converter operating current

Note: Since the A/D converter operating current varies according to the A/D conversion clock frequency (f_{AD}) and analog input voltage, use the following voltage characteristics only for reference.

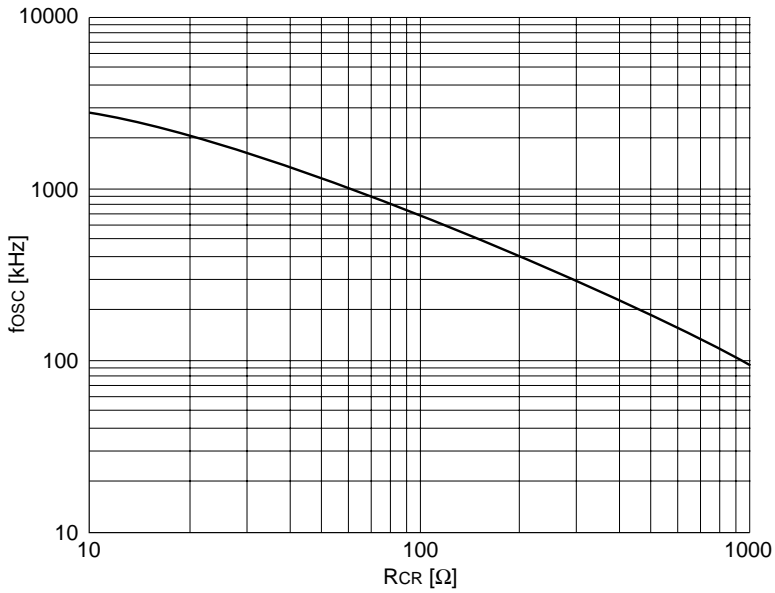


7.8.4 CR oscillation frequency characteristics

Note: Oscillation frequency changes depending on the conditions (components used, board pattern, etc.). In particular, extensively depending on the product form (chip, plastic package or ceramic package) and board capacitance. Therefore, use the following chart for reference only and select the resistance value after evaluating the actual product.

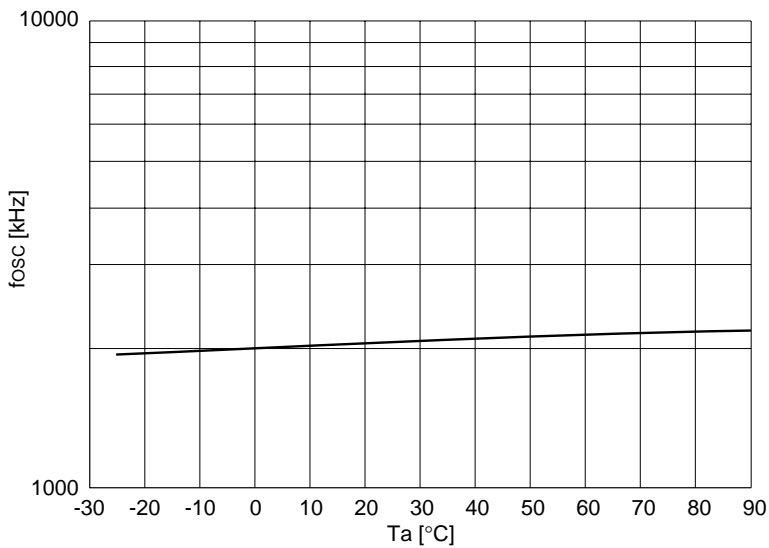
Oscillation frequency - resistance characteristic

Ta = 25°C, Typ. value



Oscillation frequency - temperature characteristic

RCR = 20 kΩ

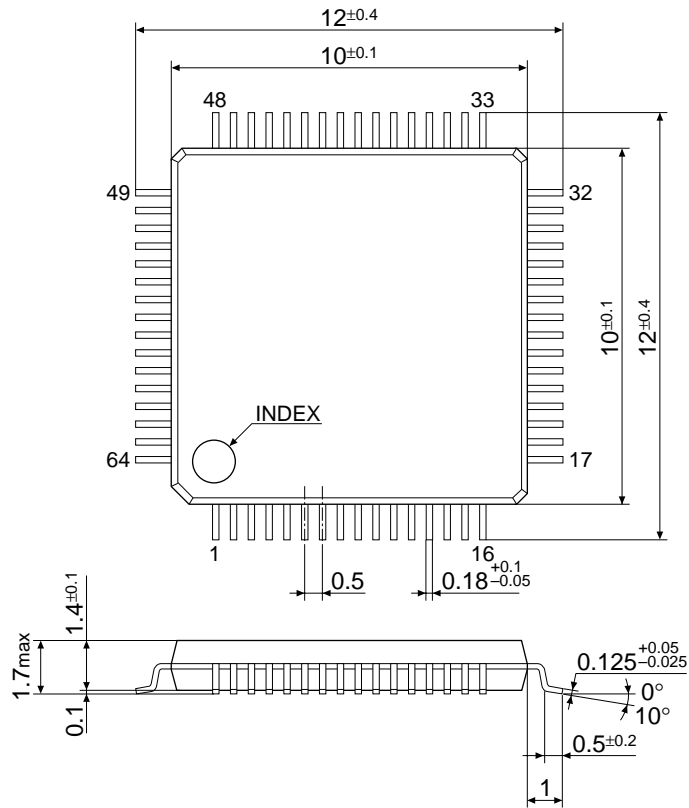


CHAPTER 8 PACKAGE

8.1 Plastic Package

QFP13-64pin

(Unit: mm)

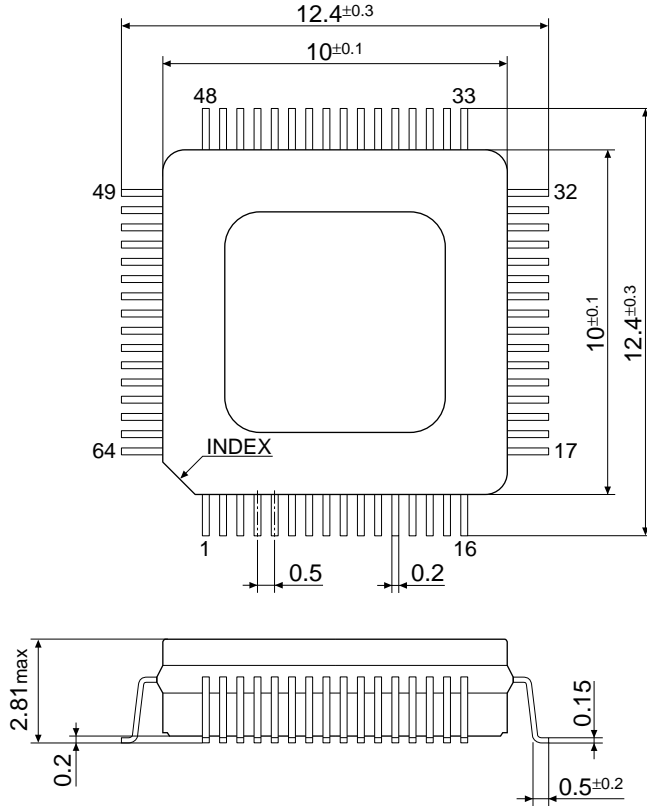


The dimensions are subject to change without notice.

8.2 Ceramic Package for Test Samples

QFP13-64pin

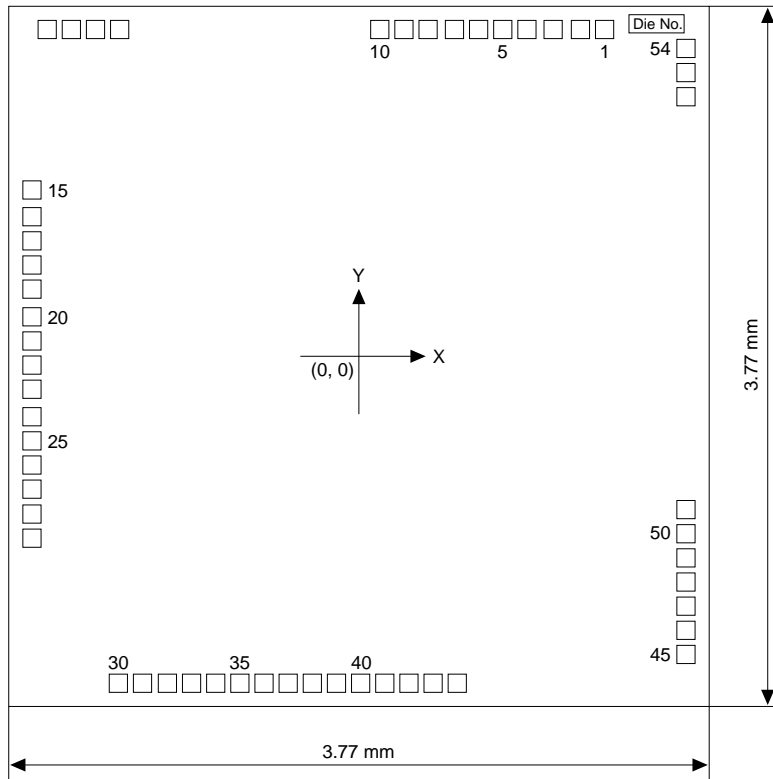
(Unit: mm)



The dimensions are subject to change without notice.

CHAPTER 9 PAD LAYOUT

9.1 Diagram of Pad Layout



Chip thickness: 400 μm
Pad opening: 100 μm

9.2 Pad Coordinates

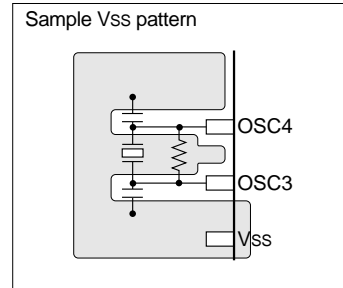
Unit: μm

No.	Pad name	X	Y	No.	Pad name	X	Y	No.	Pad name	X	Y
1	RESET	1322	1760	19	R03	-1760	362	37	SEG5	-381	-1760
2	TEST	1192	1760	20	P20	-1760	213	38	SEG6	-251	-1760
3	Vss	1045	1760	21	P21	-1760	83	39	SEG7	-121	-1760
4	OSC3	904	1760	22	P22	-1760	-47	40	SEG8	9	-1760
5	OSC4	774	1760	23	P23	-1760	-177	41	SEG9	139	-1760
6	Vd1	644	1760	24	K00	-1760	-325	42	SEG10	269	-1760
7	VDD	514	1760	25	K01	-1760	-455	43	SEG11	399	-1760
8	AVDD	372	1760	26	K02	-1760	-585	44	SEG12	529	-1760
9	AVREF	242	1760	27	K03	-1760	-715	45	SEG13	1760	-1605
10	AVSS	112	1760	28	COM0	-1760	-849	46	SEG14	1760	-1475
11	P40	-1288	1760	29	COM1	-1760	-979	47	SEG15	1760	-1345
12	P41	-1418	1760	30	COM2	-1295	-1760	48	SEG16	1760	-1215
13	P42	-1548	1760	31	COM3	-1165	-1760	49	SEG17	1760	-1085
14	P43	-1678	1760	32	SEG0	-1031	-1760	50	SEG18	1760	-955
15	BZ	-1760	896	33	SEG1	-901	-1760	51	SEG19	1760	-825
16	R00	-1760	752	34	SEG2	-771	-1760	52	Vc1	1760	1398
17	R01	-1760	622	35	SEG3	-641	-1760	53	Vc2	1760	1528
18	R02	-1760	492	36	SEG4	-511	-1760	54	Vc3	1760	1658

CHAPTER 10 PRECAUTIONS ON MOUNTING

<Oscillation Circuit>

- Oscillation characteristics change depending on conditions (board pattern, components used, etc.). In particular, when a ceramic oscillator or crystal oscillator is used, use the oscillator manufacturer's recommended values for constants such as capacitance and resistance.
- Disturbances of the oscillation clock due to noise may cause a malfunction. Consider the following points to prevent this:
 - (1) Components which are connected to the OSC3 and OSC4 terminals, such as oscillators, resistors and capacitors, should be connected in the shortest line.
 - (2) As shown in the right hand figure, make a Vss pattern as large as possible at circumscription of the OSC3 and OSC4 terminals and the components connected to these terminals. Furthermore, do not use this Vss pattern for any purpose other than the oscillation system.
 - (3) When supplying an external clock to the OSC3 terminal, the clock source should be connected to the OSC3 terminal in the shortest line. Furthermore, do not connect anything else to the OSC4 terminal.
- In order to prevent unstable operation of the oscillation circuit due to current leak between OSC3 and VDD, please keep enough distance between OSC3 and VDD or other signals on the board pattern.

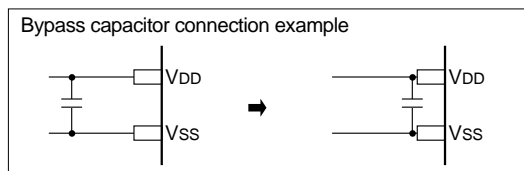


<Reset Circuit>

- The power-on reset signal which is input to the $\overline{\text{RESET}}$ terminal changes depending on conditions (power rise time, components used, board pattern, etc.). Decide the time constant of the capacitor and resistor after enough tests have been completed with the application product. When the built-in pull-up resistor is added to the $\overline{\text{RESET}}$ terminal by mask option, take into consideration dispersion of the resistance for setting the constant.
- In order to prevent any occurrences of unnecessary resetting caused by noise during operating, components such as capacitors and resistors should be connected to the $\overline{\text{RESET}}$ terminal in the shortest line.

<Power Supply Circuit>

- Sudden power supply variation due to noise may cause malfunction. Consider the following points to prevent this:
 - (1) The power supply should be connected to the VDD, Vss, AVDD, AVSS and AVREF terminal with patterns as short and large as possible. In particular, the power supply for AVDD, AVSS and AVREF affects A/D conversion precision. Furthermore, similar consideration is necessary when VC3 is supplied from outside the IC.
 - (2) When connecting between the VDD and Vss terminals with a bypass capacitor, the terminals should be connected as short as possible.



(3) Components which are connected to the VD1, VC1, VC2 and VC3 terminals, such as capacitors and resistors, should be connected in the shortest line.

In particular, the VC1, VC2 and VC3 voltages affect the display quality.

- Do not connect anything to the VC1, VC2 and VC3 terminals when the LCD driver is not used.

<A/D Converter>

- When the A/D converter is not used, the power supply terminals for the analog system should be connected as shown below.

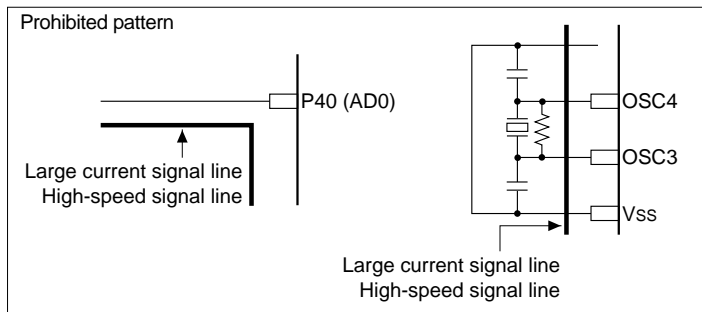
AVDD → VDD

AVSS → VSS

AVREF → VSS

<Arrangement of Signal Lines>

- In order to prevent generation of electromagnetic induction noise caused by mutual inductance, do not arrange a large current signal line near the circuits that are sensitive to noise such as the oscillation unit and analog input unit.
- When a signal line is parallel with a high-speed line in long distance or intersects a high-speed line, noise may be generated by mutual interference between the signals and it may cause a malfunction. Do not arrange a high-speed signal line especially near circuits that are sensitive to noise such as the oscillation unit and analog input unit.



<Precautions for Visible Radiation (when bare chip is mounted)>

- Visible radiation causes semiconductor devices to change the electrical characteristics. It may cause this IC to malfunction. When developing products which use this IC, consider the following precautions to prevent malfunctions caused by visible radiations.
 - (1) Design the product and implement the IC on the board so that it is shielded from visible radiation in actual use.
 - (2) The inspection process of the product needs an environment that shields the IC from visible radiation.
 - (3) As well as the face of the IC, shield the back and side too.

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