MF1208-02

EPSON

CMOS 32-BIT SINGLE CHIP MICROCOMPUTER **E0C33 Family**

DMT/EPOD/MEM BOARD MANUAL

- **DMT33004/DMT33004PD**
- **DMT33005/DMT33005PD**
- **DMT33MON/DMT33MONLV**
- **DMT33AMP**
- **DMT33AMP2**
- **EPOD33001/EPOD33001LV**
- **EPOD33208/EPOD33208LV**
- **EPOD332L01LV**
- **MEM33201/MEM33201LV**

ENERGY SAVING EPSON

SEIKO EPSON CORPORATION

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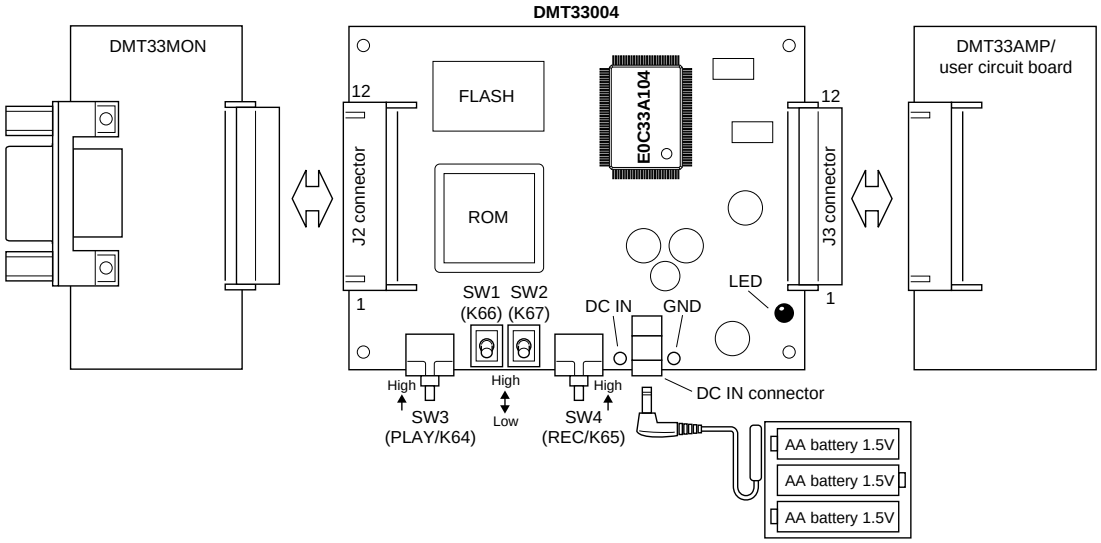
E0C33A104 Demonstration Board

DMT33004/DMT33004PD

Description

The DMT33004 is a demonstration tool of the E0C33A104 32-bit RISC type microcomputer. The DMT33004 board contains a 128KB ROM, a 1MB RAM, a 1MB Flash memory, and two connectors, one for interfacing with the DMT33MON board and the other for a voice I/O circuit board such as DMT33AMP. This board can be used as a development tool for the voice application as well as various applications that use the E0C33A104. The DMT33004PD contains the QFP type socket used to connect the POD33001 as a substitute for the E0C33A104 chip.



Package

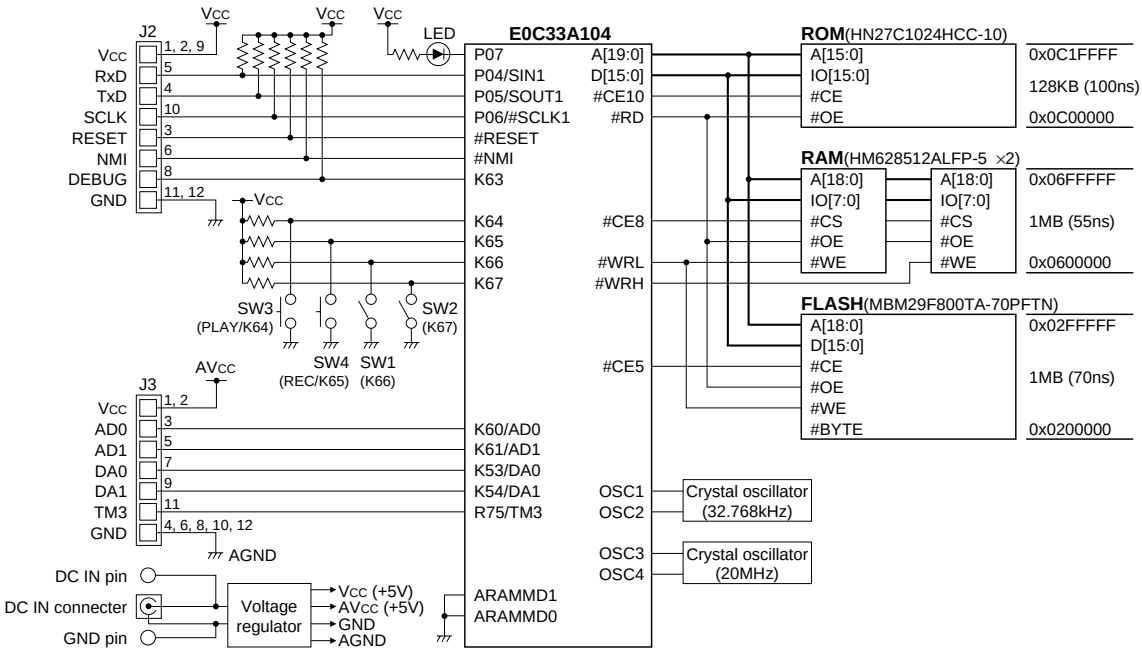
The DMT33004 package contains the following items:

(1) DMT33004 board 1
(2) Battery holder 1
(3) DC power cable 1
(4) I/F connectors for user board 2
(5) DMT33004/DMT33004PD Manual ..... 1 (E&J)
(6) User registration card ..... 1 (E&J)
(7) Warranty card ..... 1 (E&J)
(8) Usage precautions ..... 1 (E&J)

Specifications

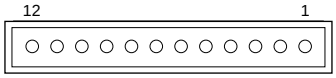
No.	Component	Item	Specifications	Remarks
1	DMT33004	Dimensions	80mm(L) × 60mm(W) × 25mm(H)	
		CPU	E0C33A104	
		ROM	128KB, 100ns, HN27C1024HCC-10(Hitachi, PLCC)	Area 10(0x0c00000–0x0c1ffff)
		RAM	1MB, 55ns, HM628512ALFP-5(Hitachi)	Area 8(0x0600000–0x06fffff)
		FLASH	1MB, 70ns, MBM29F800TA-70PFTN(Fujitsu)	Area 5(0x0200000–0x02fffff)
		Operating (input) voltage	5V(+3V to +5V)	
		Current consumption (typ.)	Approx. 75mA (varies according to the memory access condition)	
		J2 connector	S12B-XH-ST(Nichiatsu)	
		J3 connector	12JQ-ST(Nichiatsu)	
2	Supplied connector		S12B-XH-ST(Nichiatsu)	×2
3	Battery holder		AA battery × 3(ELPA)	
4	DC power cable	Length	Approx. 60cm	
		Plug	JXP4802(Hoshiden)	

Block Diagram



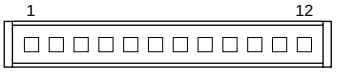
Connector Pin Assignment

J2 connector (for connecting DMT33MON)



No.	Pin name	No.	Pin name
1	VCC (5V)	7	NC
2	VCC (5V)	8	DEBUG(K63)
3	RESET	9	VCC (5V)
4	TxD(P05)	10	SCLK(P06)
5	RxD(P04)	11	GND
6	NMI	12	GND

J3 connector (for connecting DMT33AMP/user board)



No.	Pin name	No.	Pin name
1	VCC (5V)	7	DA0(K53)
2	VCC (5V)	8	GND
3	AD0(K60)	9	DA1(K54)
4	GND	10	GND
5	AD1(K61)	11	TM3(R75)
6	GND	12	GND

Precautions

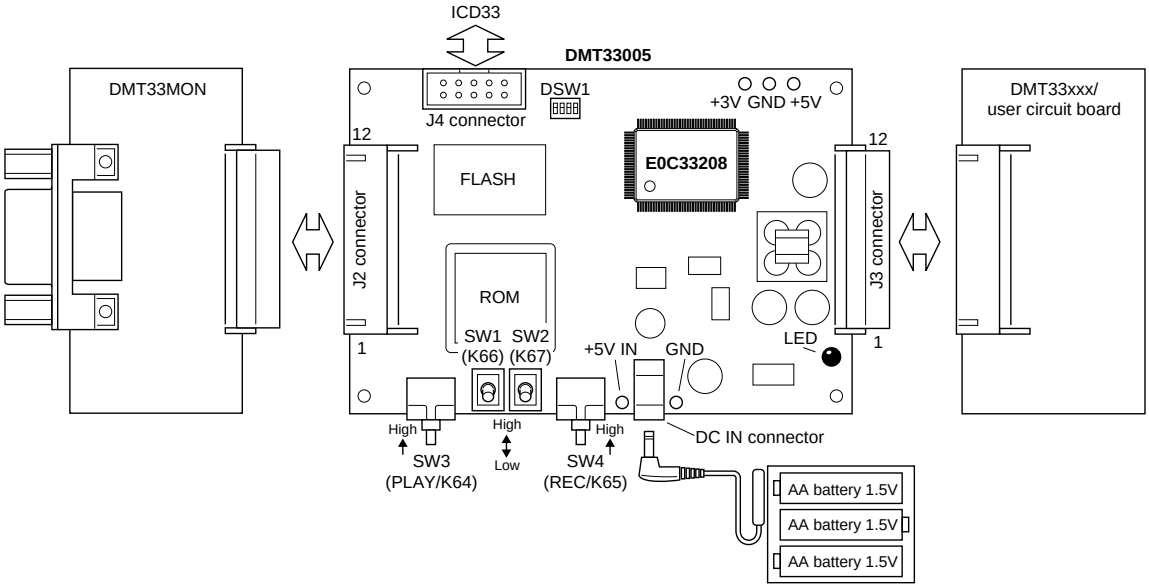
- Make sure that the power of all boards/equipment of the system are off before installing/removing boards to/from the DMT33004.
- The power for the DMT33004 can be supplied between the DC IN and GND pins instead of the DC IN connector. The supply voltage range must be within the range of 3V to 5V and do not confuse the polarity (+ and -) as it may cause a malfunction.
- If the DEBUG signal of the J2 connector is set to high or is left open (such as when the DMT33MON is not connected) when the DMT33004 is turned on, the DMT33004 loads the reset vector stored in the Flash memory to the Program Counter to execute the program from that address. (After shipping, the demonstration program that makes the LED blink is executed.) If the DEBUG signal is set to low (SW3 of the DMT33MON = ON), the debug monitor in the ROM will start up.
- When connecting the DMT33004PD to the POD33001, align the cutout of each socket.

E0C33208 Demonstration Board

DMT33005/DMT33005PD

Description

The DMT33005 is a demonstration tool of the E0C33208 32-bit RISC type microcomputer. The DMT33005 board contains a 128KB ROM, a 1MB RAM, a 1MB Flash memory, and three connectors for interfacing with the DMT33MON board, for an option board or user circuit board and for the ICD33 debug tool. This board can be used as a development tool for various applications that use the E0C33208. The DMT33005PD contains the QFP type socket used to connect the EPOD33001 as a substitute for the E0C33208 chip.



Package

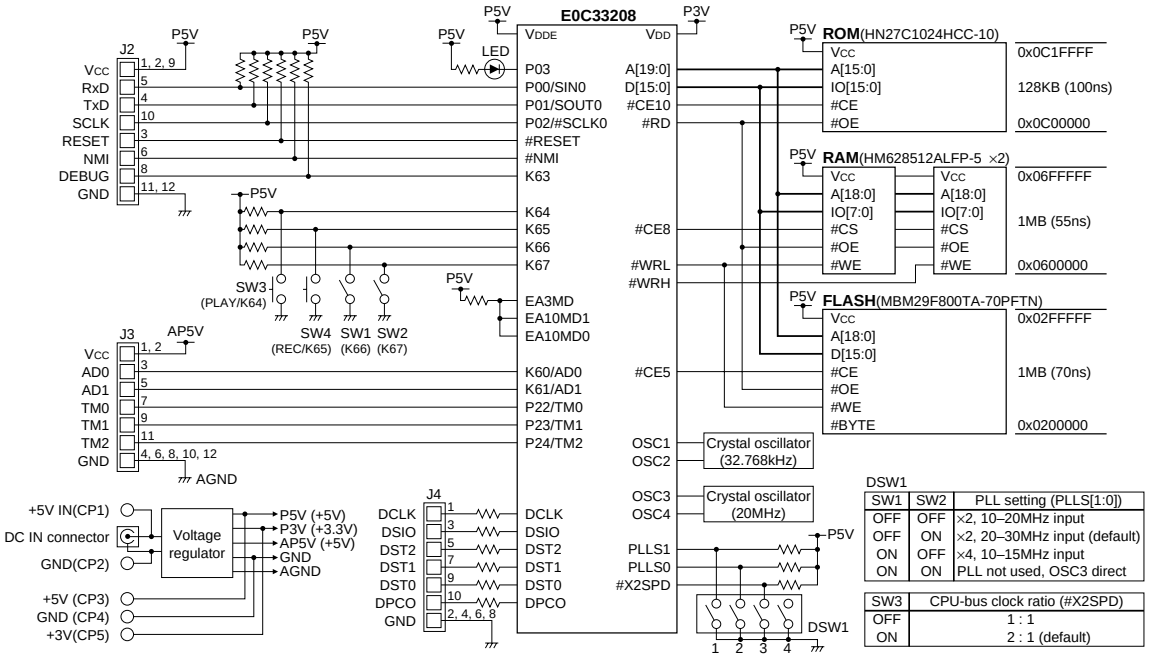
The DMT33005 package contains the following items:

(1) DMT33005 board 1
(2) Battery holder 1
(3) DC power cable 1
(4) I/F connectors for user board 2
(5) DMT33005/DMT33005PD Manual ..... 1 (E&J)
(6) User registration card ..... 1 (E&J)
(7) Warranty card ..... 1 (E&J)
(8) Usage precautions ..... 1 (E&J)

Specifications

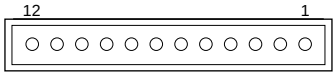
No.	Component	Item	Specifications	Remarks
1	DMT33005	Dimensions	80mm(L) × 60mm(W) × 25mm(H)	
		CPU	E0C33208	
		ROM	128KB, 100ns, HN27C1024HCC-10(Hitachi, PLCC)	Area 10(0x0c00000–0x0c1ffff)
		RAM	1MB, 55ns, HM628512ALFP-5(Hitachi)	Area 8(0x0600000–0x06fffff)
		FLASH	1MB, 70ns, MBM29F800TA-70PFTN(Fujitsu)	Area 5(0x0200000–0x02fffff)
		Operating (input) voltage	5V(+3V to +5V)	
		Current consumption (typ.)	Approx. 75mA (varies according to the memory access condition)	
		J2 connector	S12B-XH-ST(Nichiatsu)	
		J3 connector	12JQ-ST(Nichiatsu)	
2	Supplied connector		S12B-XH-ST(Nichiatsu)	× 2
3	Battery holder		AA battery × 3(ELPA)	
4	DC power cable	Length	Approx. 60cm	
		Plug	JXP4802(Hoshiden)	

Block Diagram



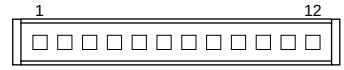
Connector Pin Assignment

J2 connector



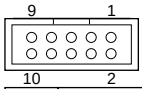
No.	Pin name	No.	Pin name
1	Vcc (5V)	7	NC
2	Vcc (5V)	8	DEBUG(K63)
3	RESET	9	Vcc (5V)
4	TxD(P01)	10	SCLK(P02)
5	RxD(P00)	11	GND
6	NMI	12	GND

J3 connector



No.	Pin name	No.	Pin name
1	Vcc (5V)	7	TM0(P22)
2	Vcc (5V)	8	GND
3	AD0(K60)	9	TM1(P23)
4	GND	10	GND
5	AD1(K61)	11	TM2(P24)
6	GND	12	GND

J4 connector



No.	Pin name	No.	Pin name
1	DCLK	6	GND
2	GND	7	DST1
3	DSIO	8	GND
4	GND	9	DST0
5	DST2	10	DPCO

Precautions

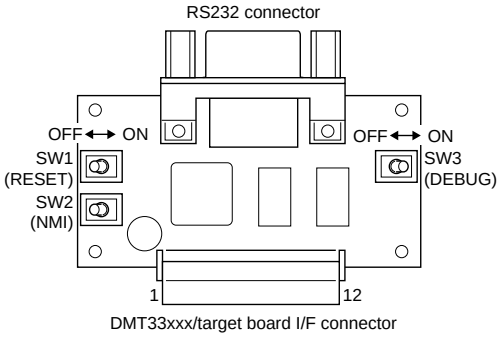
- Make sure that the power of all boards/equipment of the system are off before installing/removing boards to/from the DMT33005.
- The power for the DMT33005 can be supplied between the DC IN and GND pins instead of the DC IN connector. The supply voltage range must be within the range of 3V to 5V and do not confuse the polarity (+ and -) as it may cause a malfunction.
- If the DEBUG signal of the J2 connector is set to high or is left open (such as when the DMT33MON is not connected) when the DMT33005 is turned on, the DMT33005 loads the reset vector stored in the Flash memory to the Program Counter to execute the program from that address. (After shipping, the demonstration program that makes the LED blink is executed.) If the DEBUG signal is set to low (SW3 of the DMT33MON = ON), the debug monitor in the ROM will start up.
- When connecting the DMT33004PD to the EPOD33001, align the cutout of each socket.

E0C33 Family Debug Monitor Interface Board

DMT33MON/DMT33MONLV

Description

The DMT33MON board provides the interface for the debug monitor to the demonstration tools such as the DMT33004/33005 or the user target board. The DMT33MON allows on-board debugging using the debugger (db33.exe) on a personal computer by connecting it to the target board in which the E0C33 Family debug monitor (MON33) has been implemented.
The DMT33MON board is for 5V operation and the DMT33MONLV is for 3.3V operation.
For details on how to use the DMT33MON, refer to the "E0C33 Family MON33 Debug Monitor Manual".



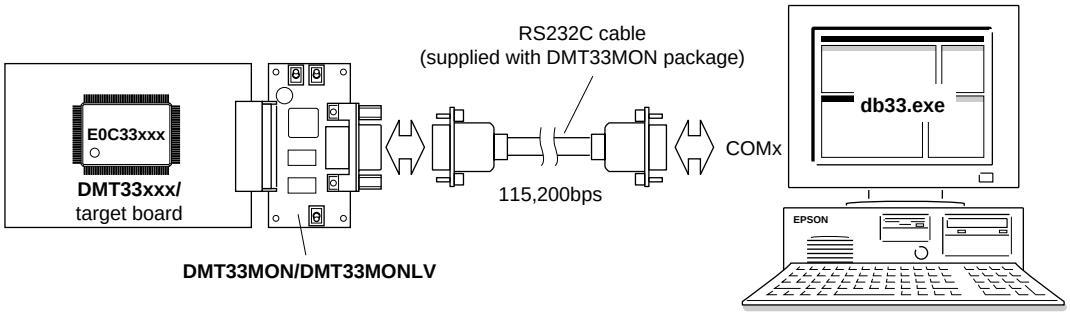
Package

The DMT33MON package contains the following items:

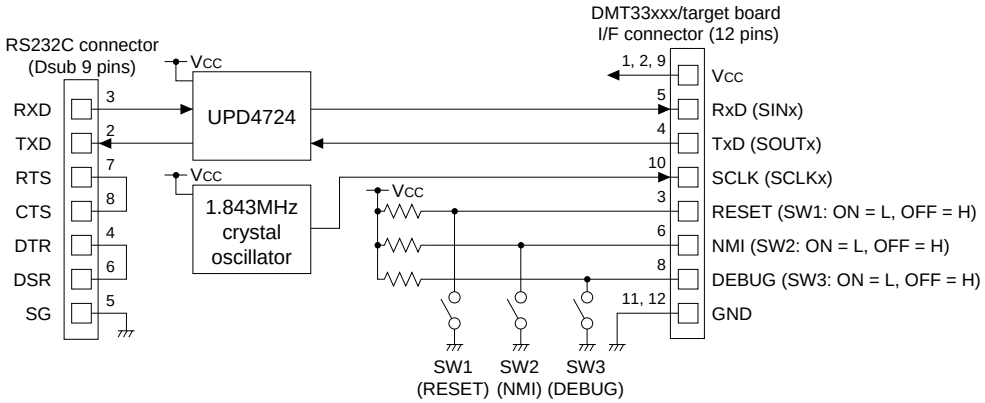
(1) DMT33MON board 1
(2) PC connection cable (RS232C) 1
(3) I/F connectors for connecting target board 2
(4) DMT33MON/DMT33MONLV Manual ..... 1 (E&J)
(5) User registration card ..... 1 (E&J)
(6) Warranty card ..... 1 (E&J)
(7) Usage precautions ..... 1 (E&J)

Please prepare the "E0C33 Family MON33 Debug Monitor" package and the "E0C33 Family C Compiler" package containing the debugger separately.

System Configuration

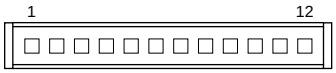


Block Diagram



Connector Pin Assignment

Target board I/F connector



No.	Pin name	No.	Pin name
1	Vcc	7	NC
2	Vcc	8	DEBUG(SW3)
3	RESET(SW1)	9	Vcc
4	TxD(SOUT)	10	SCLK
5	RxD(SIN)	11	GND
6	NMI(SW2)	12	GND

PC I/F (RS-232C) connector

No.	Pin name	No.	Pin name
1	–	6	DSR
2	TXD	7	RTS
3	RXD	8	CTS
4	DTR	9	–
5	SG		

Precautions

- Make sure that the power of the DMT33xxx/target board and the personal computer are off before connecting or disconnecting the system.
- Use a +5V±0.5V power supply for the DMT33MON and a +3.3V±0.3V for the DMT33MONLV. Supplying any other voltage may cause a malfunction. Also, do not confuse the polarity (+ and -).
- Do not connect the DMT33MONLV to a DMT33xxx board with 5V specification as it may cause a malfunction.

Specifications

No.	Component	Item	Specifications	Remarks
1	DMT33MON/ DMT33MONLV	Dimensions	30mm(L) × 60mm(W) × 20mm(H)	
		Operating (input) voltage	DMT33MON: +5V±0.5V	
			DMT33MONLV: +3.3V±0.3V	
		Current consumption (typ.)	Approx. 10mA	
2	RS-232C cable (for IBM-PC/AT)/ connector	Length	3m	
		Cable connector	DMT side: D-sub 9pins(female)	
			Host side: D-sub 9pins(male)	
		Connector on DMT	DELC-J9SAF-23L0(JAE)	
3	Target board I/F connector	Connector on DMT	12JQ-ST(Nichiatsu)	
		Connector for target board	S12B-XH-ST(Nichiatsu)	× 2

Voice Input/Output Board for DMT

DMT33AMP

Description

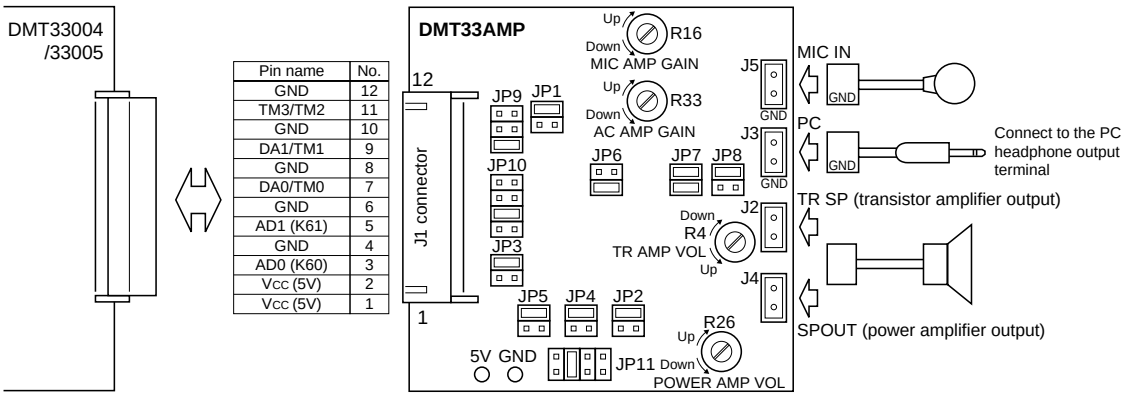
The DMT33AMP is an optional board that provides a voice I/O function for the DMT33004/33005 and the user target board. The DMT33AMP allows voice input or output with the microphone and on-board amplifier. It is suitable for developing voice applications. It also allows configuration of the on-board low-pass and high-pass filters for the microphone input and speaker output signals to test the effects.

Package

The DMT33AMP package contains the following items:

(1) DMT33AMP board 1
(2) Speaker 1
(3) Microphone 1
(4) I/F connector for user board 1
(5) PC headphone output connection cable 1
(6) DMT33AMP Manual ..... 1 (E&J)
(7) User registration card ..... 1 (E&J)
(8) Warranty card ..... 1 (E&J)
(9) Usage precautions ..... 1 (E&J)

Board Layout



Jumper switch

JP1 DMT / MIC — Selects the voice source to be output.
DMT: DMT33004/33005 output (default)
MIC: Microphone input of this board

JP2 DA / TM — Selects an input for the transistor amplifier circuit.
DA: DMT33004 D/A output (default)
TM: DMT33005 PWM output

JP3 DA / TM — Selects an input for the CR 2nd order filter circuit.
DA: DMT33004 D/A output (default)
TM: DMT33005 PWM output

JP4 SP / MIC — Selects a filter in the OP AMP 4th order filter circuit (for speaker and MIC).
SP: For speaker (default)
MIC: For microphone

JP5 SP / MIC — Selects an filter in the OP AMP 4th order filter circuit (for speaker and MIC).
SP: For speaker (default)
MIC: For microphone

JP6 AD1 / AD0 — Selects the A/D channel on the DMT33004/33005 used to convert the MIC input.
AD0: Channel 0 (default)
AD1: Channel 1

JP7 3300pF / 1500pF — Selects a cutoff frequency in the CR 1sr order high-pass filter circuit.
Short 3300pF only: 300 Hz
Short 1500pF only: 500 Hz
Short both: 250 Hz (default)

JP8 MIC / MLP — Selects whether the OP AMP 4th order filter circuit for the MIC circuit is used or not.
MIC: Not used (default)
MLP: Used

JP9 TM3/TM2 / DA1/TM1 / DA0/TM0 — Selects a DMT33004/33005 output signal.
TM3/TM2: DMT33004 TM3 or DMT33005 TM2
DA1/TM1: DMT33004 DA1 or DMT33005 TM1
DA1/TM1: DMT33004 DA0 or DMT33005 TM0 (default)

JP10 TR / 2LP / 4LP / MLP — Selects the circuit to be used for voice output.
TR: Transistor amplifier circuit
2LP: CR 2nd order filter circuit
4LP: OP AMP 4th order filter circuit (for speaker) (default)
MLP: OP AMP 4th order filter circuit (for speaker and MIC)

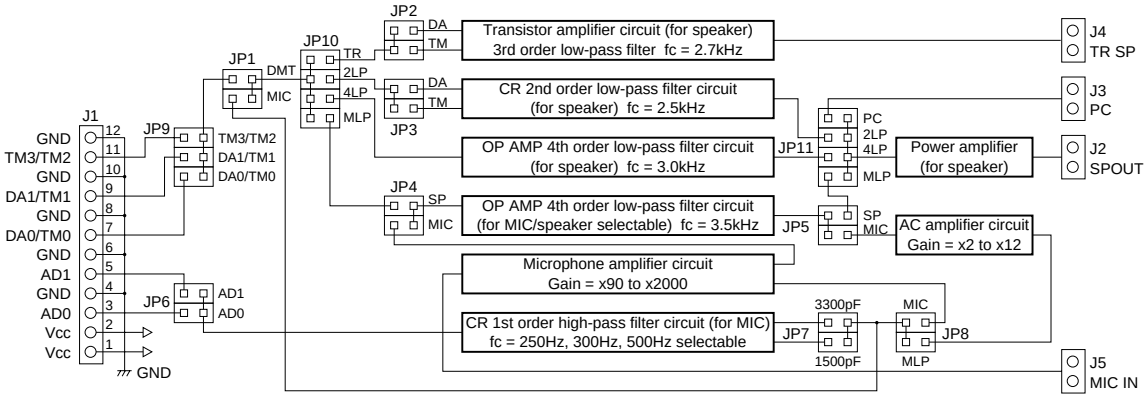
JP11 PC / 2LP / 4LP / MLP — Selects a power amplifier input.
PC: PC headphone output
2LP: CR 2nd order filter circuit
4LP: OP AMP 4th order filter circuit (for speaker) (default)
MLP: OP AMP 4th order filter circuit (for speaker and MIC)

Note: The DMT33AMP is set for connecting the DMT33004 by default. When using with the DMT33005, select TM using JP2 and JP3, and DA1/TM1 using JP9.

Control

R26 Volume adjustment for the power amplifier
R4 Volume adjustment for the transistor amplifier
R33 Gain adjustment for the AC amplifier (x2 to x12)
R16 Gain adjustment for the microphone input (microphone amplifier) (x90 to x2000)

Block Diagram



Precautions

- Make sure that the power of all boards/equipment of the system are off before installing/removing boards to/from the DMT33AMP.
- The +5V source voltage is supplied to the DMT33AMP through the 5V and GND pins or the J1 connector. Do not connect the power supply to the 5V and GND pins when supplying the source voltage through the J1 connector (such as when the DMT33004/33005 is connected).

Specifications

No.	Component	Item	Specifications	Remarks
1	DMT33AMP	Dimensions	60mm(L) × 60mm(W) × 20mm(H)	
		Operating (input) voltage	+5V±0.5V	
		Current consumption (typ.)	Approx. 10mA (idling), Approx. 100mA (speaker driven)	
		I/F connector (male)	S12B-XH-ST(Nichiatsu)	
2	Accessory	Condencer microphone	WM-034DM(Panasonic)	
		Speaker	8Ω, 0.25W, TO50S11A000(Foster)	
		PC connection cable	Length: approx. 50cm Connector: HKP02FS01(HONDA)	
		Connector for user board (female)	12JQ-ST(Nichiatsu)	

Voice Input/Output Board for DMT

DMT33AMP2

Description

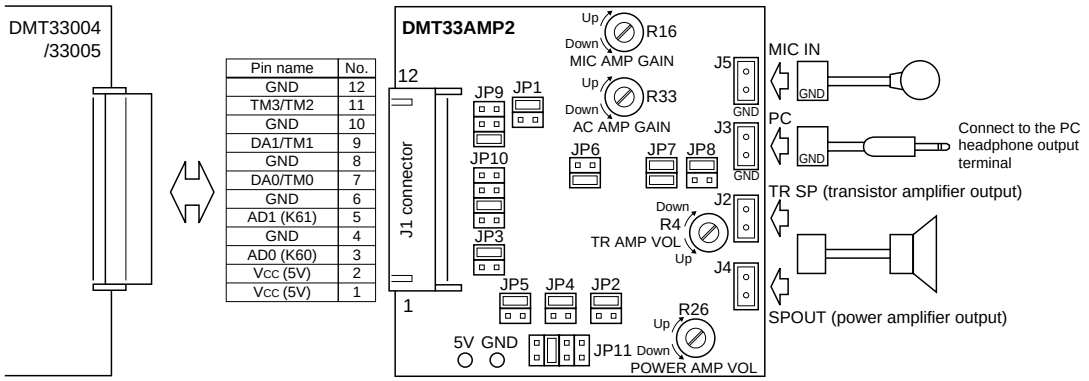
The DMT33AMP2 is an optional board that provides a voice I/O function for the DMT33004/33005 and the user target board. The DMT33AMP2 allows voice input or output with the microphone and on-board amplifier. It is suitable for developing voice applications. It also allows configuration of the on-board low-pass and high-pass filters for the microphone input and speaker output signals to test the effects. The DMT33AMP2 supports 16kHz and 22kHz sampling rate (8kHz is not available). For 8kHz sampling, DMT33AMP is available.

Package

The DMT33AMP2 package contains the following items:

(1) DMT33AMP2 board 1
(2) Speaker 1
(3) Microphone 1
(4) I/F connector for user board 1
(5) PC headphone output connection cable 1
(6) DMT33AMP2 Manual ..... 1 (E&J)
(7) User registration card ..... 1 (E&J)
(8) Warranty card ..... 1 (E&J)
(9) Usage precautions ..... 1 (E&J)

Board Layout



Jumper switch

JP1 DMT / MIC
Selects the voice source to be output.
DMT: DMT33004/33005 output (default)
MIC: Microphone input of this board

JP2 DA / TM
Selects an input for the transistor amplifier circuit.
DA: DMT33004 D/A output (default)
TM: DMT33005 PWM output

JP3 DA / TM
Selects an input for the CR 2nd order filter circuit.
DA: DMT33004 D/A output (default)
TM: DMT33005 PWM output

JP4 SP / MIC
Selects a filter in the OP AMP 4th order filter circuit (for speaker and MIC).
SP: For speaker (default)
MIC: For microphone

JP5 SP / MIC
Selects an filter in the OP AMP 4th order filter circuit (for speaker and MIC).
SP: For speaker (default)
MIC: For microphone

JP6 AD1 / AD0
Selects the A/D channel on the DMT33004/33005 used to convert the MIC input.
AD0: Channel 0 (default)
AD1: Channel 1

JP7 3300pF / 1500pF
Selects a cutoff frequency in the CR 1sr order high-pass filter circuit.
Short 3300pF only: 300 Hz
Short 1500pF only: 500 Hz
Short both: 250 Hz (default)

JP8 MIC / MLP
Selects whether the OP AMP 4th order filter circuit for the MIC circuit is used or not.
MIC: Not used (default)
MLP: Used

JP9 TM3/TM2 / DA1/TM1 / DA0/TM0
Selects a DMT33004/33005 output signal.
TM3/TM2: DMT33004 TM3 or DMT33005 TM2
DA1/TM1: DMT33004 DA1 or DMT33005 TM1
DA1/TM1: DMT33004 DA0 or DMT33005 TM0 (default)

JP10 TR / 2LP / 4LP / MLP
Selects the circuit to be used for voice output.
TR: Transistor amplifier circuit
2LP: CR 2nd order filter circuit
4LP: OP AMP 4th order filter circuit (for speaker) (default)
MLP: OP AMP 4th order filter circuit (for speaker and MIC)

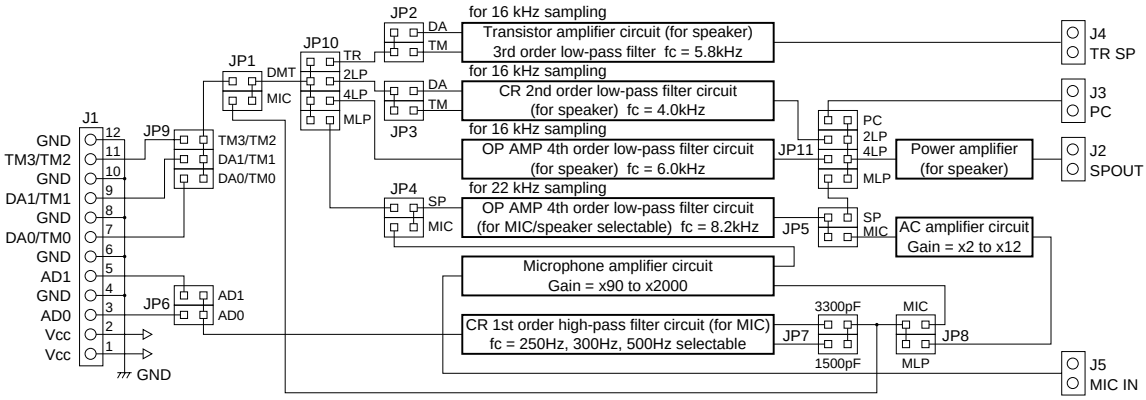
JP11 PC / 2LP / 4LP / MLP
Selects a power amplifier input.
PC: PC headphone output
2LP: CR 2nd order filter circuit
4LP: OP AMP 4th order filter circuit (for speaker) (default)
MLP: OP AMP 4th order filter circuit (for speaker and MIC)

Note: The DMT33AMP is set for connecting the DMT33004 by default. When using with the DMT33005, select TM using JP2 and JP3, and DA1/TM1 using JP9.

Control

R26 Volume adjustment for the power amplifier
R4 Volume adjustment for the transistor amplifier
R33 Gain adjustment for the AC amplifier (x2 to x12)
R16 Gain adjustment for the microphone input (microphone amplifier) (x90 to x2000)

Block Diagram



Precautions

- Make sure that the power of all boards/equipment of the system are off before installing/removing boards to/from the DMT33AMP2.
- The +5V source voltage is supplied to the DMT33AMP2 through the 5V and GND pins or the J1 connector. Do not connect the power supply to the 5V and GND pins when supplying the source voltage through the J1 connector (such as when the DMT33004/33005 is connected).

Specifications

No.	Component	Item	Specifications	Remarks
1	DMT33AMP2	Dimensions	60mm(L) × 60mm(W) × 20mm(H)	
		Operating (input) voltage	+5V±0.5V	
		Current consumption (typ.)	Approx. 10mA (idling), Approx. 100mA (speaker driven)	
		I/F connector (male)	S12B-XH-ST(Nichiatsu)	
2	Accessory	Condencer microphone	WM-034DM(Panasonic)	
		Speaker	8Ω, 0.25W, TO50S11A000(Foster)	
		PC connection cable	Length: approx. 50cm Connector: HKP02FS01(HONDA)	
		Connector for user board (female)	12JQ-ST(Nichiatsu)	

E0C33208 Emulation Probe Of Device

EPOD33001/EPOD33001LV

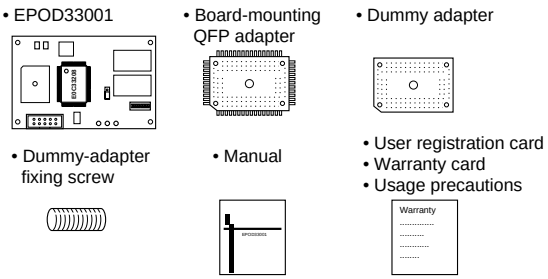
Description

The EPOD33001 (Pod for the E0C33208) is a tool for developing the programs to be written to the internal ROM of the E0C332xx Series microcomputers. By attaching a board-mounting QFP adapter to the E0C332xx mounting part of the user target system, the target system can be connected to the ICD33 via the EPOD33001. The EPOD33001 emulates the internal ROM of the E0C332xx chip using its RAM and the program can be debugged using the ICD33. The EPOD33001 comes with the E0C33208, crystal oscillators (OSC3 = 20MHz, OSC1 = 32.768kHz) and 256KB RAM (for Area 10 or 3 internal ROM emulation) making it possible to debug the program using the ICD33 or MON33 and to execute the program using the OTP mode. The EPOD33001 is for 5V operation and the EPOD33001LV is for 3.3V operation.

Package

The EPOD33001 package contains the following items:

(1) EPOD33001 board 1
(2) Board-mounting QFP adapter 1
(3) Dummy adapter 1
(4) Dummy-adapter fixing screw 1
(5) EPOD33001/EPOD33001LV Manual ..... 1 (E&J)
(6) User registration card ..... 1 (E&J)
(7) Warranty card ..... 1 (E&J)
(8) Usage precautions ..... 1 (E&J)

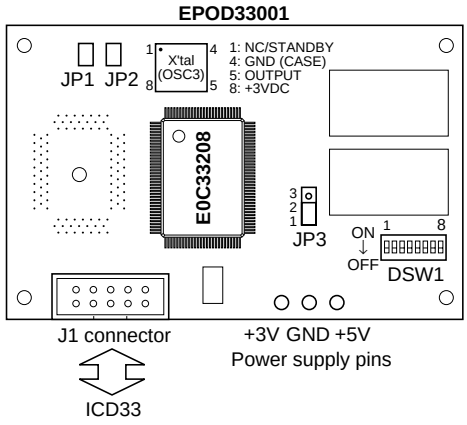


Board Layout

JP1 (3V power supply selection)
Open: Inputs 3V from the EPOD33001 power supply pins.
Short: Inputs 3V from the target system. (default)

JP2 (5V power supply selection, 3V for LV)
Open: Inputs 5V from the EPOD33001 power supply pins.
Short: Inputs 5V from the target system. (default)

JP3 (ROM emulation area selection)
Short 1-2: EPOD33001 RAM emulates the internal ROM in Area 10.
Short 3-2: EPOD33001 RAM emulates the internal ROM in Area 3. (default)



DSW1-2 (#X2SPD pin set-up)

SW1-2	CPU : bus clock
OFF	1 : 1
ON	2 : 1 (default)

DSW1-4, 1-3 (PLLS[1:0] pin set-up)

SW1-4	SW1-3	PLL setting
OFF	OFF	x2 10–20MHz input
OFF	ON	x2 20–25MHz input (default)
ON	OFF	x4 10–12.5MHz input
ON	ON	x1 OSC3 direct

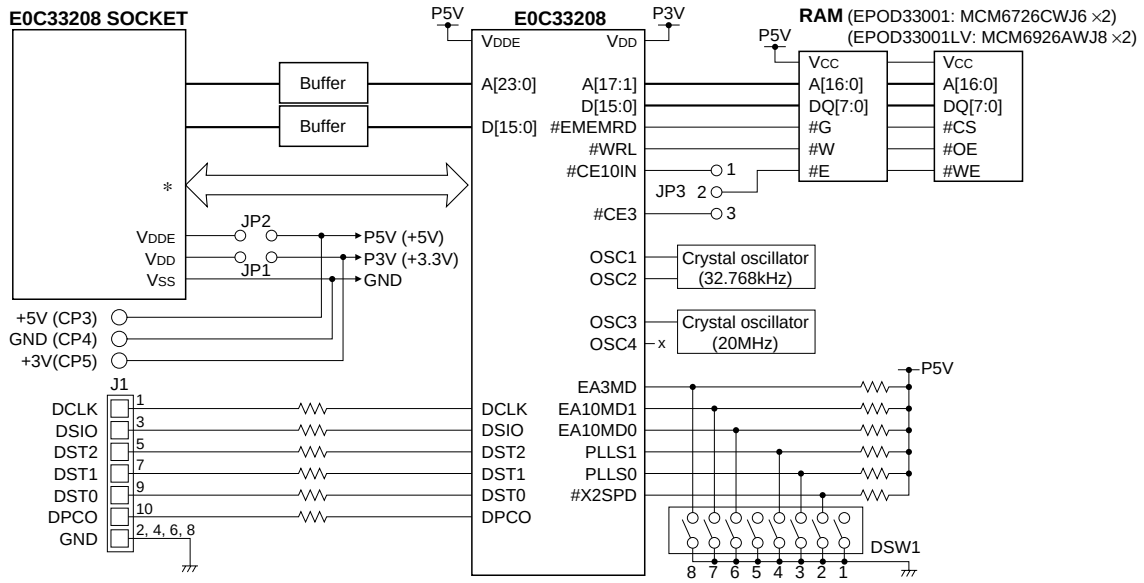
DSW1-7, 1-6 (EA10MD[1:0] pin set-up)

SW1-4	SW1-3	Area 10 mode
OFF	OFF	External ROM mode (default)
OFF	ON	Internal ROM mode
ON	OFF	OTP mode
ON	ON	ROM emulation mode

DSW1-8 (EA3MD pin set-up)

SW1-8	Area 3 mode
OFF	Internal ROM mode
ON	ROM emulation mode (default)

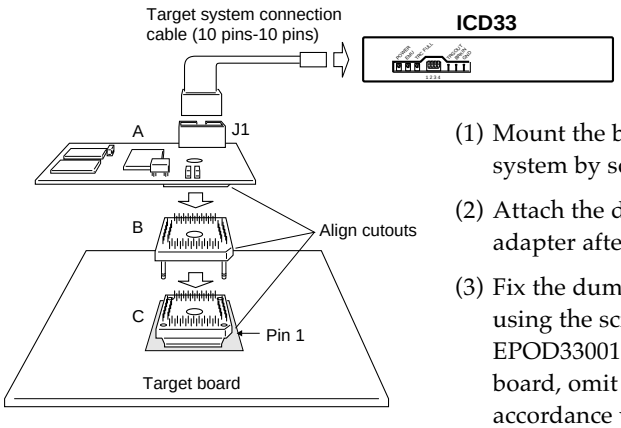
Block Diagram



∗ See "Board-Mounting QFP Adapter Pin Assignment" for the signals connected to the socket.

Connecting the EPOD33001

Fitting and connection procedures



(1) Mount the board-mounting QFP adapter (A) to the target system by soldering.

(2) Attach the dummy adapter (B) to the board-mounting QFP adapter after aligning its cutout with its counterpart.

(3) Fix the dummy adapter to the board-mounting QFP adapter using the screw included with the package. If the EPOD33001-fixing hole can be opened in the target system board, omit this procedure and fix the dummy adapter in accordance with step (5).

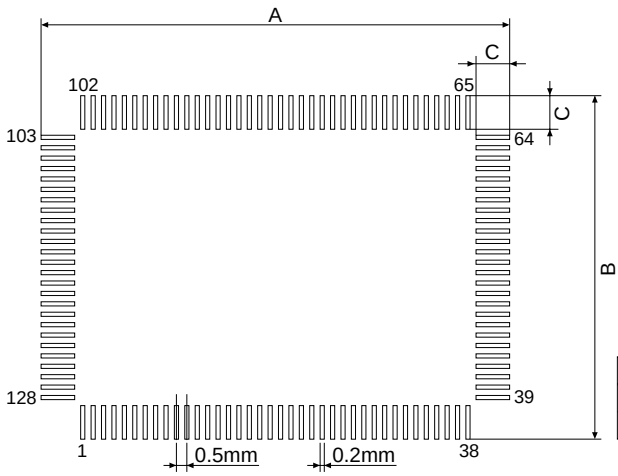
(4) Attach the EPOD33001 (C) to the dummy adapter after aligning its cutout with its counterpart. Normally, the EPOD33001 board should be only inserted or removed to connect or disconnect the dummy adapter.

(5) If the EPOD33001-fixing hole can be opened in the target system board, omit step (3) and fix the board-mounting QFP adapter, dummy adapter, and the EPOD33001 to the target system board here.

(6) Connect the EPOD33001 to the ICD33 using the 10-pin cable (supplied in the ICD33 package).

Note: When inserting or removing the dummy adapter and the EPOD33001, be sure to push or pull them vertically. If they are inserted or removed at an angle, the pins may be bent or a device malfunction may occur. In addition, inserting and removal can only be guaranteed up to 100 times.

Dimensions of the QFP adapter pins/foot pattern



Dimensions	A	B	C
TQPACK	22.0 mm	16.0 mm	1.005 mm
Foot pattern	23.0 mm	17.0 mm	1.8 mm

Note: Dimensions differ from those of the actual IC. To design mass-production boards for actual IC installation, see the "E0C33208/204/202 Technical Manual".

Mounting the board-mounting QFP adapter by soldering

Follow the procedure described below to solder the board-mounting QFP adapter to the target system.

(1) To ensure that the position of Pin 1 is not mistaken, check the direction of the board-mounting QFP adapter in which it is fitted to the target-system board. Pin 1 is at the cutout part of the board-mounting QFP adapter.

(2) Apply a coating of cream solder to the foot pattern on the target-system board. Process the pins on the board-mounting QFP adapter with flux in advance.

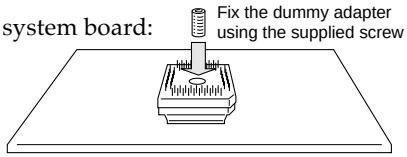
(3) Apply a coating of adhesive to the four protrusions located at the bottom of the board-mounting QFP adapter and temporarily fix the QFP adapter to the target system board. Use of an instant adhesive or epoxy-based adhesive is recommended.

(4) Solder the QFP adapter to the target system board using a reflow furnace or by manually soldering. The soldering temperature conditions should be as follows:
Reflow furnace: 240°C, within 20 sec.
Manual soldering: 240°C, within 10 sec. (per pin)

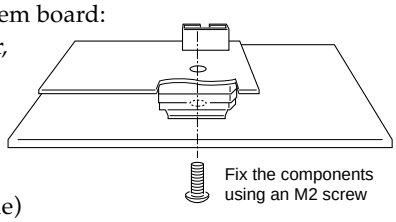
Method for fixing the EPOD33001

The following shows the method for fixing the EPOD33001 to the target system board:

(1) When the EPOD33001-fixing hole cannot be opened in the target system board:
After attaching the board-mounting QFP adapter and dummy adapter, fix the dummy adapter to the board-mounting QFP adapter using the screw included with the package.



(2) When the EPOD33001-fixing hole can be opened in the target system board:
After attaching the board-mounting QFP adapter, dummy adapter, and EPOD33001, fix these components using a screw from the reverse side of the target system board. The following conditions must be met when the EPOD33001-fixing hole is opened:
Size of the screw hole: ϕ2.4 mm
Wiring-prohibited area: ϕ3.6 mm (from the center of the screw hole)
Fixing screw: M2 (mm)



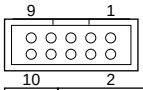
Note: Be careful not to tighten the screw excessively, as damage to the screw threads or a device malfunction may result.

Board-Mounting QFP Adapter Pin Assignment

No.	Pin name	No.	Pin name	No.	Pin name	No.	Pin name
1	P24/TM2	33	K65/AD5	65	#RESET	97	A16
2	VSS	34	K50/#DMAREQ0	66	#NMI	98	ICEMD
3	P25/TM3	35	K64/AD4	67	A0/#BSL	99	A17
4	P26/TM4	36	K63/AD3	68	A1	100	A18
5	P15/EXCL4/#DMAEND0	37	K62/AD2	69	P34/#BUSREQ/#CE6	101	A19
6	P27/TM5	38	AVDDE	70	VSS	102	P04/SIN1/#DMAACK2
7	BCLK	39	K61/AD1	71	A2	103	P05/SOUT1/#DMAEND2
8	P00/SIN0	40	K60/AD0	72	A3	104	P06/#SCLK1/DMAACK3
9	P01/SOUT0	41	D6	73	A4	105	VSS
10	D15	42	VSS	74	A5	106	**N.C.** (PLLC)
11	VDD	43	D5	75	A6	107	VSS
12	P03/#SRDY0	44	D4	76	**N.C.** (#CE10IN)	108	**N.C.** (PLLS1)
13	D14	45	D3	77	VDD	109	**N.C.** (PLLS0)
14	P31/#BUSGET/#GARD	46	D2	78	**N.C.** (#EMEMRD)	110	P07/#SRDY1/#DMAEND3
15	D13	47	D1	79	A7	111	**N.C.** (#X2SPD)
16	P32/#DMAACK0	48	D0	80	#HCAS/#UWE	112	**N.C.** (EA10MD0)
17	D12	49	P35/#BUSACK	81	A8	113	**N.C.** (EA10MD1)
18	P33/#DMAACK1	50	VDDE	82	#LCAS/#CAS	114	VDD
19	D11	51	#CE9/#CE17	83	A9	115	**N.C.** (EA3MD)
20	K54/#DMAREQ3	52	**N.C.** (OSC2)	84	P16/EXCL5/#DMAEND1	116	**N.C.** (OSC4)
21	D10	53	#CE7/#RAS0/#CE13/#RAS2	85	A10	117	P20/#DRD
22	K53/#DMAREQ2	54	**N.C.** (OSC1)	86	A20	118	**N.C.** (OSC3)
23	D9	55	#CE6	87	A11	119	P21/#DWE/#GAAS
24	K52/#ADTRG	56	#RD	88	A21	120	**N.C.** (#CE3)
25	VSS	57	VSS	89	A12	121	P22/TM0
26	K51/#DMAREQ1	58	#WRL/#WR/#WE/#LWE	90	A22	122	P23/TM1
27	P02/#SCLK0	59	#WRH/#BSH/#UWE	91	A13	123	**N.C.** (DSIO)
28	D8	60	#CE10EX	92	A23	124	**N.C.** (P10/EXCL0/T8UF0/DST0)
29	D7	61	#CE8/#RAS1/#CE14/#RAS3	93	VSS	125	**N.C.** (P11/EXCL1/T8UF1/DST1)
30	VDDE	62	#CE5/#CE15	94	A14	126	**N.C.** (P12/EXCL2/T8UF2/DST2)
31	K67/AD7	63	#CE4/#CE11	95	A15	127	**N.C.** (P13/EXCL3/T8UF3/DPCO)
32	K66/AD6	64	P30/#WAIT/#CE4&5	96	VDDE	128	**N.C.** (P14/FOSC1/DCLK)

N.C. : No Connection

J1 Connector Pin Assignment



No.	Pin name	No.	Pin name
1	DCLK	6	GND
2	GND	7	DST1
3	DSIO	8	GND
4	GND	9	DST0
5	DST2	10	DPCO

Power Supply

When supplying the power of the target system from the EPOD33001, connect the power to the 3V (3–3.6V), 5V (3–5.5V) and GND terminals of the EPOD33001 and open the jumpers JP1 (3V) and JP2 (5V). When supplying the power from the target system to the EPOD33001, short JP1 (3V) and JP2 (5V), and do not connect anything to the 3V, 5V and GND terminals of the EPOD33001.

Internal ROM Emulation

Select an area to be emulated from between Area 3 and Area 10 using JP3. Further more, select an emulation mode using DSW1-8 for Area 3 or DSW1-6 and 1-7 for Area 10. The EPOD33001 contains 256KB emulation RAM. Note that the program should be created within the actual RAM size when developing the program for the model with a RAM smaller than 256KB. The EPOD33001 emulation RAM allows the target program to write data in half word units (the actual ROM does not). When executing data fill, copy and enter commands to the emulation area from the debugger, use the commands for half word data.

High-Speed (OSC3) Oscillation Clock

The EPOD33001 comes with a 3.3V, 20MHz crystal oscillator (SEIKO EPSON SG8002DC) for generating the OSC3 clock. Please change it if another oscillator must be used.

Precautions

- Before connecting or disconnecting the EPOD33001 system, be sure to turn the host computer, ICD33, and target system off to prevent a malfunction.
- When inserting or removing the dummy adapter and the EPOD33001, be sure to push or pull them vertically. If they are inserted or removed at an angle, the pins may be bent or a device malfunction may occur. In addition, inserting and removal can only be guaranteed up to 100 times.
- Be careful not to tighten the screw excessively, as damage to the screw threads or a device malfunction may result.

Specifications

No.	Component	Item	Specifications	Remarks
1	EPOD33001	Dimensions	80mm(L) × 60mm(W) × 15mm(H)	
		CPU	E0C33208	
		RAM	256KB, EPOD33001: MCM6726CWJ6(Motorola) × 2 EPOD33001LV: MCM6926AWJ8(Motorola) × 2	
		Crystal oscillator (OSC3)	20MHz (+3.3V), SG8002DC(Seiko Epson)	Exchangeable
		Operating (input) voltage	+5V(5V±10%), +3V(3.3V±0.3V)	
		Current consumption (typ.)	+5V system: approx.125mA, +3V system: approx. 26mA (varies according to the memory access condition)	
2	Board-mounting QFP adapter	Dimensions	19mm(L) × 25mm(W) × 9.5mm(H)	Pin hight included
		Model	TQPACK128RD(Tokyo Eletech)	
3	Dummy adapter	Dimensions	21mm(L) × 27mm(W) × 15mm(H)	Pin hight included
		Model	TQSOCKET128RDP(Tokyo Eletech)	

E0C33208 Emulation Probe Of Device

EPOD33208/EPOD33208LV

Overview

The EPOD33208/EPOD33208LV board comes with an E0C33208 CPU, emulation memory for built-in ROM, oscillator, and probe for connecting to a target board. (* EPOD stands for Emulation Probe of Device.) You can connect the board to a target board that is equipped with minimum external peripheral circuits to easily create a system equivalent to the actual product. Connected to a separately sold emulation board (MEM33201/MEM33201LV, etc.), the board is capable of emulating external memory. The boards are also equipped with a connector for interfacing with the ICD33 (In-Circuit Debugger for the E0C33 Family). You may use the db33 to download programs to emulated memory for execution and debugging.
The boards have the following major features.

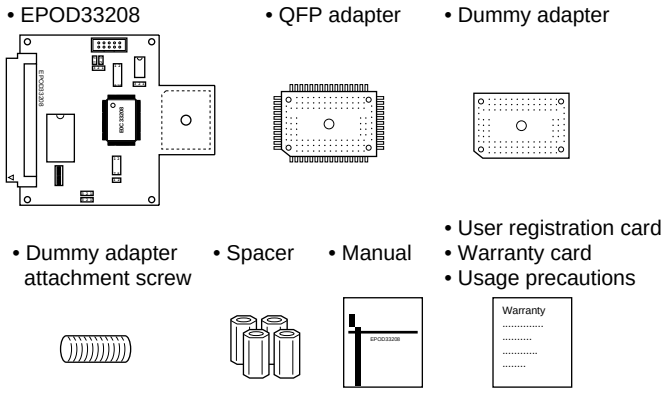
- May be used to develop products for the 32-bit RISC CPU E0C33208/204/202.
- CPU package probe for connecting to a user target board (QFP5-128 pins)
- Capable of emulating PLL multiplication (maximum 50 MHz) operations
- Emulation memory for built-in ROM (with a maximum capacity of 256KB) *optional*
  When a system consists only of the ROM built into the E0C33208/204/202, no emulation memory is required for external units.
- DIP switches for setting E0C33208/204/202 CPU operation modes
- ICD33 interface
- Standard interface for an external memory emulation board (MEM33201)
- Clock oscillators
  OSC1 (low-speed) 32 kHz
  OSC3 (high-speed) 25 MHz (standard specification)
  (equivalent to the EPSON SG8002DC; may be replaced by the user)

The EPOD33208 and EPOD33208LV run at 5 V and 3.3 V, respectively. In this document, the EPOD33208/EPOD33208LV will be referred to as the EPOD33208, the MEM33201/MEM33201LV as the MEM33201, and the QFP adapter for board installation as the QFP adapter.

Package Contents

The EPOD33208 package includes the following.

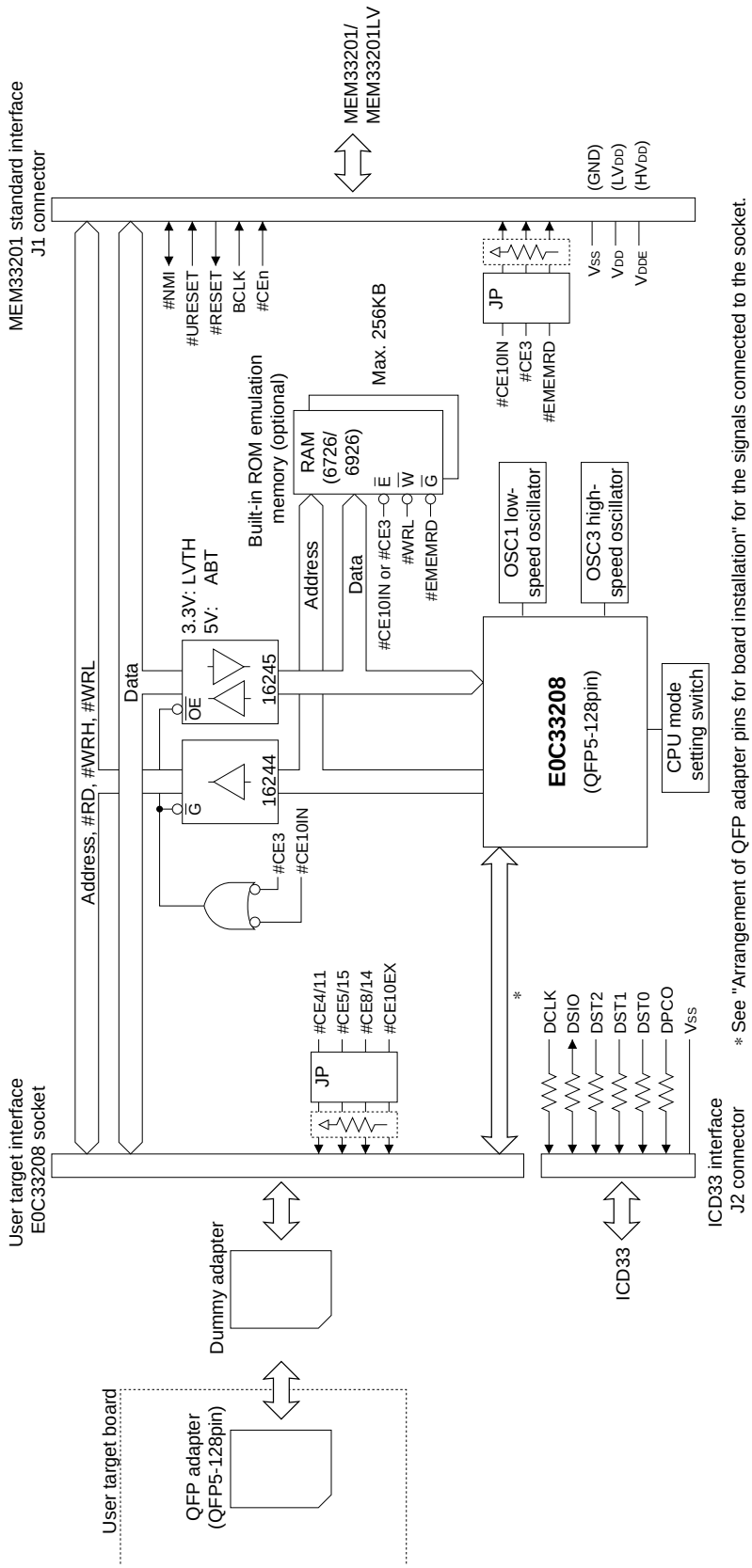
(1) EPOD33208 unit 1
(2) QFP adapter for installing the user target board (TQPACK128RD) 1
(3) Dummy adapter (TQSOKET128RDP) 1
(4) Dummy adapter attachment screw 1
(5) Spacer 4
(6) EPOD33208/EPOD33208LV Manual ..... 1 (E&J)
(7) User registration card ..... 1 (E&J)
(8) Warranty card ..... 1 (E&J)
(9) Usage precautions ..... 1 (E&J)



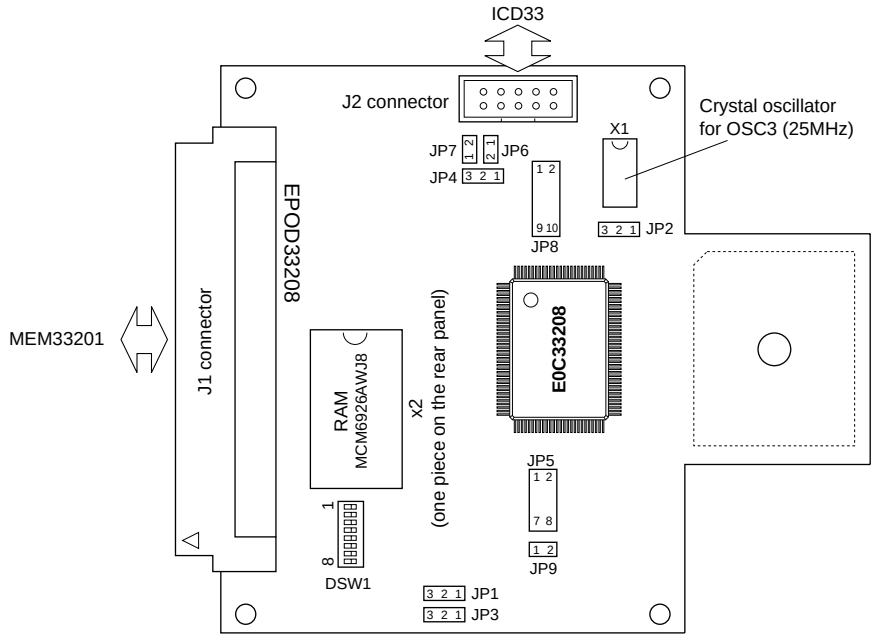
Specifications

Component	Item	Specifications	Remarks
EPOD33208 (EPOD33208LV)	Dimensions	90 mm (L) × 100 mm (W) × 25 mm (H)	Including the spacer and POD tip projection
	CPU	E0C33208	
	RAM	256KB, EPOD33208: MCM6726CWJ6 (Motorola) × 2 EPOD33208LV: MCM6926CWJ8 (Motorola) × 2	Option
	Crystal oscillator (OSC3)	25 MHz (+3.3 V), SG8002DC (with OE) (Seiko Epson)	Replaceable
	Operating (input) voltage	+5 V(5 V ± 10%), +3 V(3.3 V ± 0.3 V)	
	Current consumption	EPOD33208: approx.230 mA (Typ.) EPOD33208LV: approx.150 mA (Typ.) (depending on memory access conditions)	External memory In 25 MHz operation
QFP adapter	Dimensions	19 mm (L) × 25 mm (W) × 9.5 mm (H)	Including pin height
	Model	TQPACK128RD (Tokyo Eletech)	
Dummy adapter	Dimensions	21 mm (L) × 27 mm (W) × 15 mm (H)	Including pin height
	Model	TQSOCKET128RDP (Tokyo Eletech)	

Block Diagram



Unit Operations



Arrangement of the EPOD33208 board components

Setting the Jumper Pins

Note: Turn off the EPOD33208 before changing jumper pin settings.

JP1 Selection of the OSC1 (32 kHz) input clock

1-2 short: Inputs from the target.
2-3 short: **Uses the 32 kHz crystal oscillator on the EPOD33208** (default).

Note: You cannot use a crystal resonator on the target to operate the EPOD33208 CPU's on-chip oscillation circuit.
Set the OSC1 input clock voltage to V_{DD} (3.3V core voltage), regardless of the V_{DDE} value (I/O voltage).

JP2 Selection of the OSC3 (high-speed) input clock

1-2 short: Inputs from the target.
2-3 short: **Uses the crystal oscillator on the EPOD33208** (default).
The EPOD33208 has a 25-MHz crystal oscillator as part of standard specifications (replaceable).

Note: You cannot use a ceramic oscillator on the target to operate the EPOD33208 CPU's on-chip oscillation circuit.
Set the OSC3 input clock voltage to V_{DD} (3.3 V core voltage), regardless of the V_{DDE} value (I/O voltage).

JP3 #RESET signal input

1-2 short: Inputs the #RESET signal from the MEM33201.
2-3 short: **Inputs the #RESET signal from the target** (default).

JP4 Selection of the built-in ROM area

1-2 short: **Accesses Area 10 with #CE10IN** (default).
2-3 short: Accesses Area 3 with #CE3.

Note: The E0C33208/204/202 does not have built-in ROM.

JP5 Setting sending of #CE (area selection) signals to the target

1-2 open: **Does not send the #CE10EX signal to the target** (default).
1-2 short: Sends the #CE10EX signal to the target.

3-4 open: Does not send the #CE8/14 signal to the target.
3-4 short: **Sends the #CE8/14 signal to the target** (default).

5-6 open: Does not send the #CE5/15 signal to the target.
5-6 short: **Sends the #CE5/15 signal to the target** (default).

7-8 open: Does not send the #CE4/11 signal to the target.
7-8 short: **Sends the #CE4/11 signal to the target** (default).

Note: When using the external memory emulation board (MEM33201), do not feed the #CE signal of the area set as valid on the MEM33201 (used as emulation memory) to the target; this will result in MEM33201 and target bus collision and malfunction.
If you use #CE signals other than the above signals in the user circuit of the MEM33201 CPLD (Altera Flex10K100A), set them as invalid, or avoid using them on the target.
The MEM33201 is set to use #CE9/17 for CPLD and #CE10EX for emulation RAM in the default setting. When using these areas on the user target, change the MEM33201 setting.

JP6 Sending the #CE10IN signal to the MEM33201 (Use the default setting.)

1-2 open: **Does not send the #CE10IN signal to the MEM33201** (default).
1-2 short: Sends the #CE10IN signal to the MEM33201.

Note: When the signal is sent to the MEM33201, the #CE10IN pin is pulled through at 10kΩ.

JP7 Sending the #CE3 signal to the MEM33201 (Use the default setting.)

1-2 open: **Does not send the #CE3 signal to the MEM33201** (default).
1-2 short: Sends the #CE3 signal to the MEM33201.

Note: When the signal is sent to the MEM33201, the #CE3 pin is pulled up through 10kΩ.

JP8 Sending the ICD33 signals to the user target

1-2 open: **Does not send P14/DCLK* to the target** (default).
1-2 short: Sends P14/DCLK* to the target.

3-4 open: **Does not send P13/DPC0 to the target** (default).
3-4 short: Sends P13/DPC0 to the target.

5-6 open: **Does not send P12/DST2* to the target** (default).
5-6 short: Sends P12/DST2* to the target.

7-8 open: **Does not send P11/DST1 to the target** (default).
7-8 short: Sends P11/DST1 to the target.

9-10 open: **Does not send P10/DST0 to the target** (default).
9-10 short: Sends P10/DST0 to the target.

Note: When you use these signals for ICD33, open the jumper.

* If you use ICD33, do not use the pins P14/DCLK or P12/DST2 for user applications, since they are required for ICD33. If you do not use the ICD33 trace function, you may use P13/DPC0, P11/DST1 and P10/DST0 as the I/O ports for user applications. The I/O voltage of these ICD33 ports is the core voltage (3.3 V), not I/O voltage (V_{DDE}) of the E0C33208/204/202.

JP9 Sending the #EMEMRD signal to the MEM33201 (Use the default setting.)

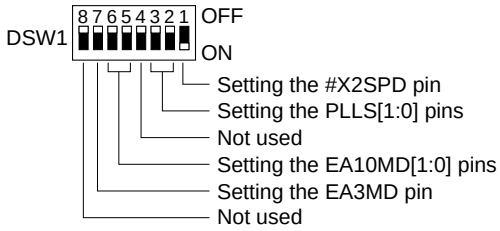
1-2 open: **Does not send the #EMEMRD signal to the MEM33201** (default).
1-2 short: Sends the #EMEMRD signal to the MEM33201.

Note: When the signal is sent to the MEM33201, the #EMEMRD pin is pulled up through 10kΩ.

Setting the DIP Switches

Note: Turn off the EPOD33208 before changing the DIP switch settings.

DSW1 Setting the operation mode of the E0C33208



DSW1-1 (Setting the #X2SPD pin)

ON: **CPU clock = Bus clock x 2** (default)

OFF: CPU clock = Bus clock x 1

DSW1-2, DSW1-3 (Setting the PLLS [1:0] pins)

Setting PLL mode

DSW1-3	DSW1-2	PLL mode
OFF	OFF	x2, OSC3 input frequency 10 to 20 MHz (default)
OFF	ON	x2, OSC3 input frequency 20 to 25 MHz
ON	OFF	x4, OSC3 input frequency 10 to 12.5 MHz
ON	ON	PLL not used

DSW1-4 (not used)

DSW1-5, DSW1-6 (Setting the EA10MD [1:0] pins)

Setting Area 10 mode

DSW1-6	DSW1-5	Area 10 mode
OFF	OFF	External ROM mode (default)
OFF	ON	Built-in ROM mode
ON	OFF	OTP mode
ON	ON	Built-in ROM emulation mode

DSW1-7 (Setting the EA3MD pin)

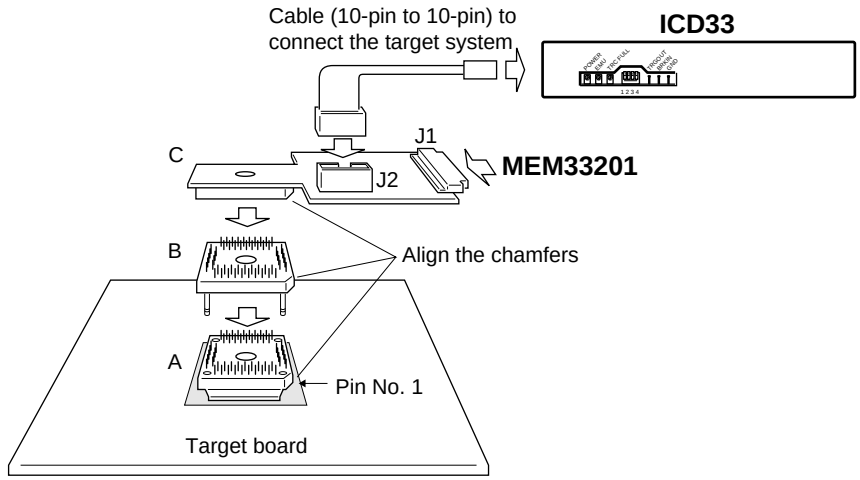
ON: Emulates Area 3 built-in ROM

OFF: **Does not emulate Area 3 built-in ROM** (default)

DSW1-8 (not used)

Note: The 256KB RAM on this board can be used for either Area 10 or Area 3 built-in ROM emulation. When DSW1-5 and 1-6 (EA10MD) are set to [ON, ON], it emulates a 256KB ROM (0xc00000 to 0xc3ffff) in Area 3, and when DSW1-7 (EA3MD) is set to ON, it emulates a 256KB ROM (0x80000 to 0xbffff) in Area 3.
Area 3 built-in ROM emulation mode can also be selected by setting the A3EEN bit (0x48130/DB) in the BCU to "0" (default) even if the DSW1-7 (EA3MD) is set to OFF.
In addition to these settings, either Area 10 (default) or Area 3 must be selected using JP4.

Installation to the User Target



Installing EPOD33208

(1) Solder the QFP adapter (A) for user target installation to the target system.

(2) Couple the dummy adapter (B) and QFP adapter with aligned chamfers.

(3) Attach the dummy adapter to the QFP adapter with the supplied attachment screw. If you can drill a hole on the target system board to attach the EPOD33208, skip this step and attach it in step (5).

(4) Couple EPOD33208 (C) and the dummy adapter with aligned chamfers. To disconnect the EPOD33208, pull it out while keeping the dummy board in place.

(5) If you can drill a hole on the target system board to attach the EPOD33208, skip step (3) and attach the QFP adapter, dummy adapter and EPOD33208 to the target system board in this step.

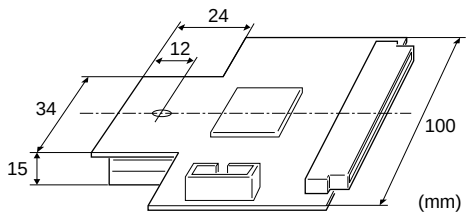
(6) Connect EPOD33208 and ICD33 with the 10-pin cable (enclosed in the ICD33 package).

Note: When you connect or disconnect the EPOD33208 or dummy adapter, push or pull it vertically. Pushing or pulling the pins at an angle will bend the pins and lead to system malfunctions. Avoid frequent removal of the EPOD33208 or dummy adapter; they are designed for no more than 100 connections/disconnections.

To connect EPOD33208 to the user target, always use the dummy adapter. If you directly insert the socket of the EPOD33208 into the QFP adapter, signals will short-circuit and cause the system to malfunction.

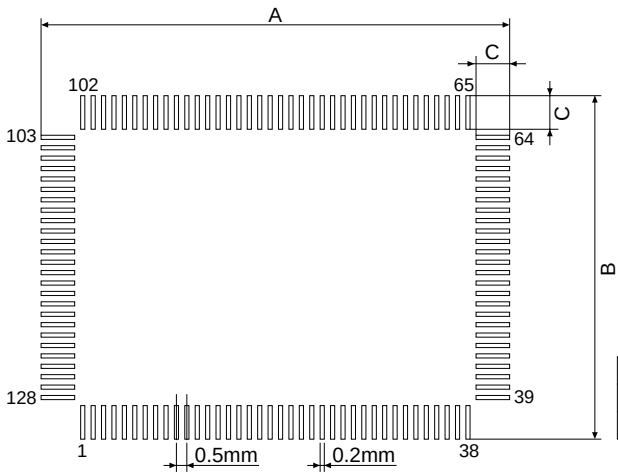
Area occupied by the EPOD33208

The EPOD33208 occupies the area shown in the illustration below. Design the target system to prevent interference with the EPOD33208.



Dimensions of the EPOD33208

Dimensions of the QFP adapter pins/foot pattern



Dimensions	A	B	C
TQPACK	22.0 mm	16.0 mm	1.005 mm
Foot pattern	23.0 mm	17.0 mm	1.8 mm

Dimensions of the QFP adapter

Note: Dimensions differ from those of the actual IC. To design mass-production boards for actual IC installation, see the "E0C33208/204/202 Technical Manual".

Soldering installing QFP adapter

Follow the steps given below to solder the QFP adapter to the target system board.

(1) The chamfered part of the QFP adapter is the position of pin No. 1. Set the QFP adapter on the target system board in the proper direction.

(2) Clean the QFP adapter pins for board installation with flux. Apply cream solder to the foot pattern of the target system board.

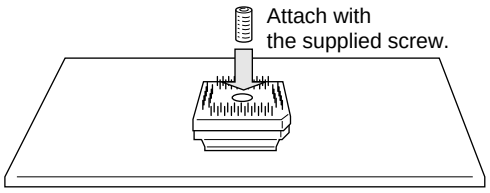
(3) Apply an instant-bond adhesive or epoxy-based adhesive to the four projections on the bottom of the QFP adapter. Temporarily attach the QFP adapter to the target system board.

(4) Solder the QFP adapter to the target system board by hand or in a reflow furnace at the following temperatures.
Reflow: 240°C for 20 seconds or less
Manual: 240°C for 10 seconds or less per pin

Attaching the EPOD33208

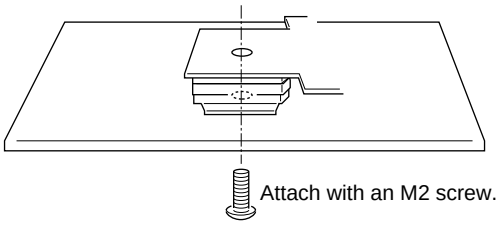
Attach the EPOD33208 to the target board by the following method.

(1) If you are unable to drill a hole on the target system board to attach the EPOD33208:
After coupling the QFP and dummy adapters, attach with the supplied screw.



Attaching the EPOD33208 (1)

(2) If you can drill a hole on the target system board to attach the EPOD33208:
After coupling the QFP adapter, dummy adapter and EPOD33208, attach with a screw from the rear panel of the target system board.
Drill the hole to the following specifications.
Size of the screw hole: ϕ2.4mm
Wiring prohibited area: ϕ3.6mm (from the screw hole center)
Attachment screw: M2 (mm)



Attaching the EPOD33208 (2)

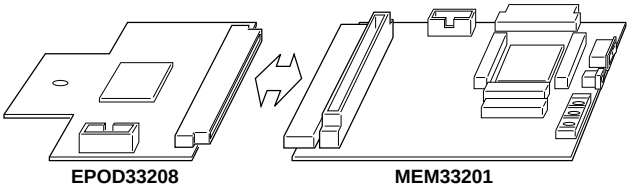
Note: To guard against thread-stripping and resulting system malfunctions, avoid overtightening the screw.

For detailed technical information on the QFP adapter, see the Tokyo Eletech Corporation home page.
http://www.tetc.co.jp/e_tet.htm

Connecting the MEM33201 Board

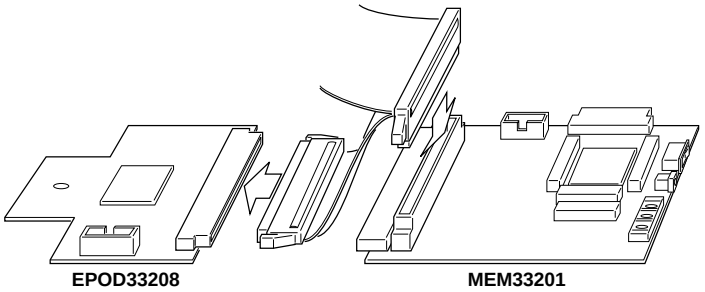
When using the external memory emulation board MEM33201, connect it to the user target board by one of the following methods that best suits the profile of the board.

(1) Direct connection of the EPOD33208 and MEM33201 connector
Direct-connect the J1 connector of the EPOD33208 and the J10 connector of the MEM33201 (angle connector).



Connecting the MEM33201 board (1)

(2) Connection with a flat cable
Connect the J1 connector of the EPOD33208 and the J11 connector of the MEM33201 (straight connector) with the supplied flat cable.



Connecting the MEM33201 board (2)

Supplying Power

Supply power to EPOD33208 by one of the following two methods.

(1) From the user target:
The power source of the EPOD33208 is connected to the power source of the user target through the QFP socket. When power is supplied to the user target, therefore, power is also supplied to EPOD33208. Use the system at the following voltages.
V_{DD} = 3.0 to 3.6 V, V_{DDE} = AV_{DDE} = 3.0 to 5.5 V, V_{SS} = AV_{SS} = 0 V

You can supply power to the external emulation board (MEM33201) connected to EPOD33208 from the power source unit of the user target. Since the MEM33201 draws a current of several hundred milliamperes, the power source unit of the user target must be able to supply this current. You can also supply power to the MEM33201 separately.

(2) From MEM33201:
If you set JP7 (for V_{DD}) and JP8 (for V_{DDE}) of the MEM33201 as "1-2 short", power is supplied to EPOD33208 from the MEM33201 and the user target.

Note: The voltage supplied from the MEM33201 are V_{DD} (3.3 V core voltage) and V_{DDE} (I/O voltage) only. Supply AV_{DDE} (voltage for analog signals) from the user target.
If you supply V_{DD} and V_{DDE} from the MEM33201, do not supply any additional voltage from the user target.

Built-in ROM Emulation

Installing emulation RAM

When using the following RAM, you can optionally emulate built-in ROM.
EPOD33208 (5 V): Motorola MCM6726CWJ6 2 pieces
EPOD33208LV (3.3 V): Motorola MCM6926AWJ8 2 pieces

Insert the RAM into the sockets on the front and back sides of the EPOD33208. Always use two RAM chips. If you use only one RAM, the system will not work.

Installing RAM

Set pin No. 1 to the correct position.
This emulation memory supports bus clocks of maximum 50 MHz.

Area 10 emulation

Set area to emulate at Area 10 with JP4 (default), and Area 10 mode with DSW 1-5 and 1-6. An emulation RAM of maximum 256KB may be installed on the EPOD33208.

Note: The RAM for built-in ROM emulation (equivalent to the Motorola MCM6726/6926) is optional.

You may use the target program to write data to emulation RAM in half-word size. You cannot write data to the actual ROM. To fill, copy, or input data to this area using a debugger, use the commands for half-words.

Setting the capacity of built-in ROM

The capacity of the ROM built into the E0C33208/204/202 is determined by A10R[2:0] (D[E:C]) of the Area 10–9 setup register (0x48126) in the BCU.

Built-in ROM capacity

A10R2(DE)	A10R2(DD)	A10R2(DC)	Built-in ROM capacity
1	1	1	2MB
1	1	0	1MB
1	0	1	512KB
1	0	0	256KB
0	1	1	128KB
0	1	0	64KB
0	0	1	32KB
0	0	0	16KB

To download a program to the built-in ROM area through ICD33, set its capacity as shown in the following example.
In E0C33208/204/202, data that exceeds the capacity of the built-in ROM is automatically changed to access external memory.
In the emulation RAM of the EPOD33208, the built-in ROM part and the external emulation memory are independent. To download a program, note that the built-in ROM area and external emulation memory area are used in the following manner, due to the limited capacity of the built-in ROM.

Example: Setting the capacity of the built-in ROM to 128KB

Write 0x3037 in the address 0x48126.

The capacity of the built-in ROM of the E0C33208/204/202 is set to 2MB (D[E:C] = 0x111) as the default setting. Change it to 128KB (D[E:C] = 0x011).
Keep the contents of other BCU registers unchanged at this stage.
With this setting, the data exceeding 128KB is automatically switched to access external memory.
If you do not set the capacity of the built-in ROM, you can access the ROM up to 256KB set to EPOD33208. Use care; data exceeding 256KB may be overwritten by the address mirror.

Area 3 emulation

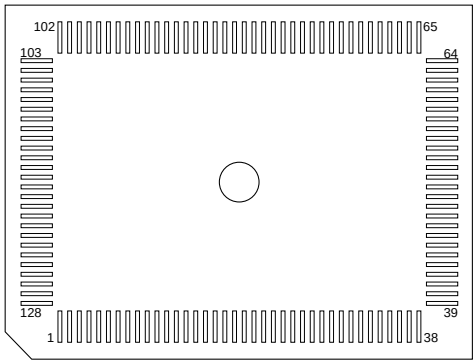
Set Area 3 with JP4. Furthermore, set DSW1-7 to ON or the Area 3 emulation bit (0x48130/DB) in a BCU register to "0".
With this setting, you may use 0x80000 to 0xbffff of the installed RAM for the emulation of built-in 256KB ROM.

OSC3 Crystal Oscillator

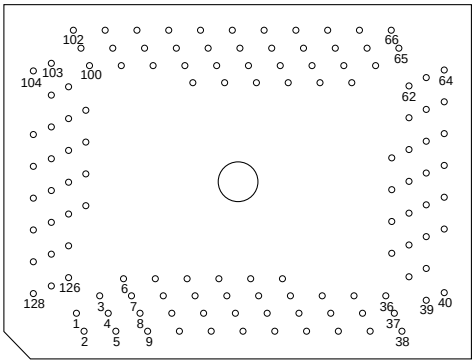
The EPOD33208 comes standard with a 25-MHz crystal oscillator, SG8002DC (with OE) for 3.3 V operations, manufactured by Seiko Epson, for OSC3 clock input. This oscillator may be replaced if necessary.

Pin Arrangement

QFP Adapter for Board Installation



QFP adapter pins

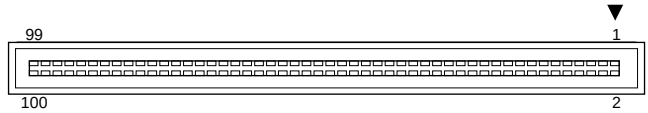


Dummy adapter pins

No.	Pin name	No.	Pin name	No.	Pin name	No.	Pin name
1	P24/TM2	33	K65/AD5	65	#RESET	97	A16
2	VSS	34	K50/#DMAREQ0	66	#NMI	98	ICEMD
3	P25/TM3	35	K64/AD4	67	A0/#BSL	99	A17
4	P26/TM4	36	K63/AD3	68	A1	100	A18
5	P15/EXCL4/#DMAEND0	37	K62/AD2	69	P34/#BUSREQ/#CE6	101	A19
6	P27/TM5	38	AVDDE	70	VSS	102	P04/SIN1/#DMAACK2
7	BCLK	39	K61/AD1	71	A2	103	P05/SOUT1/#DMAEND2
8	P00/SIN0	40	K60/AD0	72	A3	104	P06/#SCLK1/DMAACK3
9	P01/SOUT0	41	D6	73	A4	105	VSS
10	D15	42	VSS	74	A5	106	**N.C.** (PLLC)
11	VDD	43	D5	75	A6	107	VSS
12	P03/#SRDY0	44	D4	76	**N.C.** (#CE10IN)	108	**N.C.** (PLLS1)
13	D14	45	D3	77	VDD	109	**N.C.** (PLLS0)
14	P31/#BUSGET/#GARD	46	D2	78	**N.C.** (#EMEMRD)	110	P07/#SRDY1/#DMAEND3
15	D13	47	D1	79	A7	111	**N.C.** (#X2SPD)
16	P32/#DMAACK0	48	D0	80	#HCAS	112	**N.C.** (EA10MD0)
17	D12	49	P35/#BUSACK	81	A8	113	**N.C.** (EA10MD1)
18	P33/#DMAACK1	50	VDDE	82	#LCAS	114	VDD
19	D11	51	#CE9/#CE17/#CE17&18	83	A9	115	**N.C.** (EA3MD)
20	K54/#DMAREQ3	52	**N.C.** (OSC2)	84	P16/EXCL5/#DMAEND1	116	**N.C.** (OSC4)
21	D10	53	#CE7/#RAS0/#CE13/#RAS2	85	A10	117	P20/#DRD
22	K53/#DMAREQ2	54	**N.C.** (OSC1)	86	A20	118	**N.C.** (OSC3)
23	D9	55	#CE6/#CE7&8	87	A11	119	P21/#DWE/#GAAS
24	K52/#ADTRG	56	#RD	88	A21	120	**N.C.** (#CE3)
25	VSS	57	VSS	89	A12	121	P22/TM0
26	K51/#DMAREQ1	58	#WRL/#WR/#WE	90	A22	122	P23/TM1
27	P02/#SCLK0	59	#WRH/#BSH	91	A13	123	**N.C.** (DSIO)
28	D8	60	#CE10EX/#CE9&10EX	92	A23	124	P10/EXCL0/T8UF0/DST0
29	D7	61	#CE8/#RAS1/#CE14/#RAS3	93	VSS	125	P11/EXCL1/T8UF1/DST1
30	VDDE	62	#CE5/#CE15/#CE15&16	94	A14	126	P12/EXCL2/T8UF2/DST2
31	K67/AD7	63	#CE4/#CE11/#CE11&12	95	A15	127	P13/EXCL3/T8UF3/DPCO
32	K66/AD6	64	P30/#WAIT/#CE4&5	96	VDDE	128	P14/FOSC1/DCLK

Arrangement of the QFP adapter pins for board installation

Connector for MEM33201 Connection

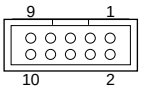


No.	Pin name	No.	Pin name	No.	Pin name	No.	Pin name
1	VDDE (HVDD)	26	A19	51	D9	76	#CE4/#CE11/#CE11&12
2	VDDE (HVDD)	27	GND	52	GND	77	#CE5/#CE15/#CE15&16
3	A0/#BSL	28	A20	53	D10	78	#CE6/#CE7&8
4	A1	29	A21	54	GND	79	#CE9/#CE17/#CE17&18
5	A2	30	A22	55	D11	80	#CE10EX/#CE9&10EX
6	A3	31	A23	56	GND	81	#CE10IN
7	GND	32	GND	57	D12	82	GND
8	A4	33	D0	58	GND	83	P30/#WAIT/#CE4&5
9	A5	34	GND	59	D13	84	GND
10	A6	35	D1	60	GND	85	P34/#BUSREQ/#CE6
11	A7	36	GND	61	D14	86	GND
12	GND	37	D2	62	GND	87	P21/#DWE/#GAAS
13	A8	38	GND	63	D15	88	P31/#BUSGET/#GARD
14	A9	39	D3	64	GND	89	GND
15	A10	40	GND	65	#RD	90	#CE3
16	A11	41	D4	66	GND	91	#EMEMRD
17	GND	42	GND	67	#WRL/#WR/#WE	92	#URESET *1
18	A12	43	D5	68	#WRH/#BSH	93	#RESET *2
19	A13	44	GND	69	GND	94	GND
20	A14	45	D6	70	#CE7/#RAS0/#CE13/#RAS2	95	#NMI *3
21	A15	46	GND	71	#CE8/#RAS1/#CE14/#RAS3	96	GND
22	GND	47	D7	72	GND	97	BCLK
23	A16	48	GND	73	#HCAS	98	GND
24	A17	49	D8	74	#LCAS	99	VDD (LVDD)
25	A18	50	GND	75	GND	100	VDD (LVDD)

*1: Outputs a reset signal from the user target to the MEM33201.
*2: Reset input signal from the MEM33201
*3: #NMI input signal from the MEM33201 (The MEM33201 side can also be set for input by the Flex10K100A terminal setting.)

Arrangement of connector pins for connecting MEM33201

Connector for ICD33 Connection



No.	Pin name	No.	Pin name
1	DCLK	6	GND
2	GND	7	DST1
3	DSIO	8	GND
4	GND	9	DST0
5	DST2	10	DPCO

Arrangement of connector pins for connecting ICD33

Precautions

Connecting, installing, and removing components

- Always turn off the system power before connecting or disconnecting the EPOD33208, ICD33, target system, and MEM33201, or setting jumpers or DIP switches. Connecting or disconnecting these components with the power on will damage the system.
- Use the dummy adapter to install the EPOD33208 to the user target. Inserting the EPOD33208 socket directly into the QFP adapter will short-circuit signal currents and cause the system to malfunction.
- When connecting or disconnecting the EPOD33208 or dummy adapter, be careful to push or pull straight in or out. Pushing or pulling the pins at an angle will bend or break the pins and lead to system malfunctions. Avoid connecting/disconnecting the EPOD33208 or dummy adapter more than 100 times.
- To prevent thread-stripping and system malfunctions, avoid overtightening the EPOD33208 attachment screw.

Power supply

The voltage supplied from the MEM33201 to the EPOD33208 are VDD (3.3 V core voltage) and VDDE (I/O voltage) only. Supply AVDDE (voltage for analog signals) from the user target.
If you supply VDD and VDDE from the MEM33201, do not supply any additional voltage from the user target.

Emulation of built-in ROM

The current version of the E0C33208/204/202 does not have built-in ROM.
To use Area 10 in built-in ROM emulation mode, set the capacity of the built-in ROM by A10R[2:0] (D[E:C]) of the Area 10-9 setup register (0x48126) of the E0C33208 BCU.
As an option, you can install built-in ROM emulation memory (maximum 256KB) on the EPOD33208. However, the above register is initially set to 2MB. Work cautiously, since data exceeding 256KB may be overwritten in the built-in ROM emulation memory rather than external memory.

Oscillation circuit and clock input

- You cannot use the crystal resonator or ceramic oscillator on the target to operate the oscillation circuits (OSC1 and OSC3) built into the EPOD33208 CPU.
- If you input OSC1 and OSC3 clock signals from the user target, set the input clock voltage to VDD (3.3 V core voltage), regardless of the VDDE value (I/O voltage).

Bus-release control by #BUSREQ

You cannot perform bus-release control of the EPOD33208 with the external #BUSREQ signal. When necessary, install a CPU on the user target to evaluate bus-release control.

Bus-release control during DMA cycle

You cannot perform bus-release control of the EPOD33208 during the DMA cycle. When necessary, install a CPU on the user target to evaluate bus-release control.

#CE (area selection) signal

When using the external memory emulation board (MEM33201), do not feed the #CE signal of the area set as valid on the MEM33201 (used as emulation memory) to the target. This will result in MEM33201 and target bus collision and system malfunction.
If you use #CE signals other than the above signals in the user circuit of the MEM33201 CPLD (Altera Flex10K100A), set them as invalid, or avoid using them on the target.
The MEM33201 is set to use #CE9/17 for CPLD and #CE10EX for emulation RAM in the default setting. When using these areas on the user target, change the MEM33201 setting.

Bus drive capacity

The following EPOD33208 signals are sent to the target through a buffer (equivalent to the 7416244/7416245, LVTH for 3.3 V and ABT for 5 V).
A[23:0], D[15:0], #RD, #WRH, #WRL

The capacity will thus be higher than that of the actual IC.
Other signal pins, including the E0C33208 CPU power supply pins, are connected to the target directly.

Pull-up and damper resistors

- Pull-up resistors are connected to the following signal lines.
  - The #CE10IN signal is pulled up through 10 kΩ when it is sent to the MEM33201.
  - The #CE3 signal is pulled up through 10 kΩ when it is sent to the MEM33201.
  - The #EMEMRD signal is pulled up through 10 kΩ when it is sent to the MEM33201.
  - In bus-release control (with #BUSREQ/#BUSACK in use), the #BUSACK (P35) signal is pulled up through 10 kΩ.
- A 33 Ω damper resistor is inserted into the lines for I/O, OSC1, and OSC3 signals received from the user target (except the K60 and K67 lines used for analog input).

MEM33201 standard interface

In the MEM33201 standard interface, the #RESET and #NMI I/O directions are as follows.

#RESET: Input from the MEM33201 to the EPOD33208

#NMI: Input from the MEM33201 to the EPOD33208 (Output is possible through the Flex10K100A terminal setting.)

E0C332L01 Emulation Probe Of Device

EPOD332L01LV

Overview

The EPOD332L01LV board comes with an E0C332L01 CPU, emulation memory for built-in ROM, oscillator, and probe for connecting to a target board. (∗ EPOD stands for Emulation Probe of Device.) You can connect the board to a target board that is equipped with only minimum external peripheral circuits to easily create a system equivalent to the actual product. Connected to a separately sold emulation board (MEM33201LV, etc.), it is capable of emulating external memory. The board is also equipped with a connector for interfacing with the ICD33 (In-Circuit Debugger for the E0C33 Family). You may use the db33 to download programs to emulated memory for execution and debugging.
It has the following major features.

- May be used to develop products for the E0C332L01.
  E0C332L01 is a 32-bit RISC type CPU, with built-in LCD controller equivalent to the SED1375.
- CPU package probe for connection to a user target board (QFP18-176 pins)
- Capable of emulating PLL multiplication (maximum 40 MHz) operations
- Emulation memory for built-in ROM (with a maximum capacity of 256KB) *optional*
  When a system consists only of the ROM built into the E0C332L01, no emulation memory is required for external units.
- DIP switches for setting E0C332L01 CPU operation modes
- DIP switches for setting operation modes for the LCD controller equivalent to the SED1375
- ICD33 interface
- Standard interface for an external memory emulation board (MEM33201LV)
- Clock oscillators

OSC1 (low-speed)	32 kHz
OSC3 (high-speed)	20 MHz (standard specification) (equivalent to the EPSON SG8002DC; may be replaced by the user)
CLKI (for SED1375)	25 MHz (standard specification) (equivalent to the EPSON SG8002DC; may be replaced by the user)

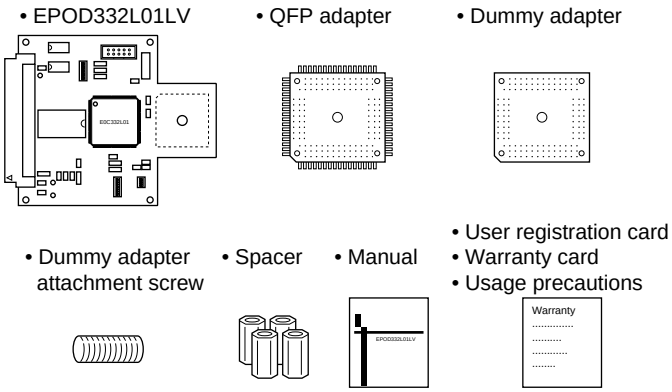
- Supports 3.3 V operating voltage

The QFP adapter for board installation will be referred to in this manual as the QFP adapter.

Package Contents

The EPOD332L01LV package includes the following.

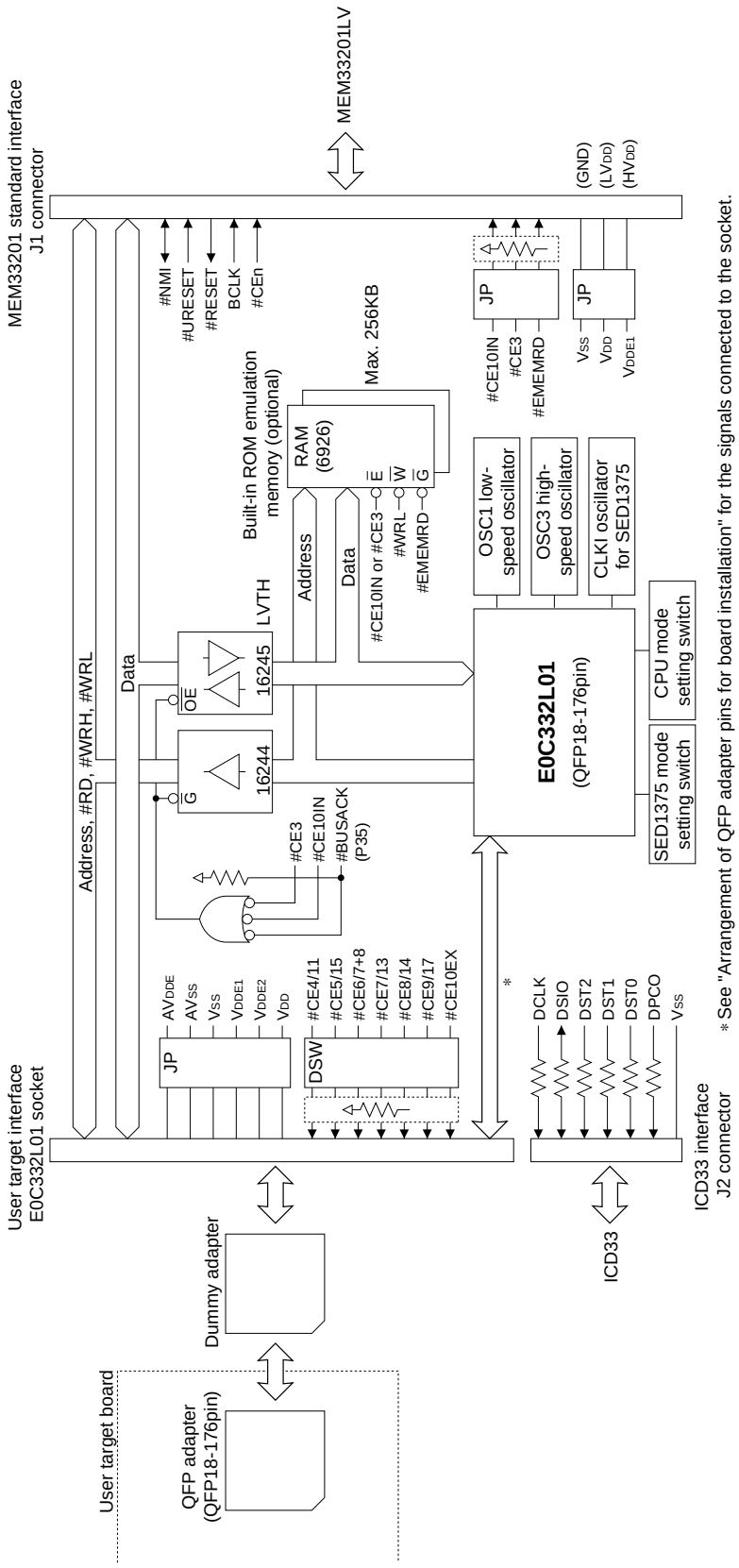
(1) EPOD332L01LV unit 1
(2) QFP adapter for installing the user target board (TQPACK176SD) 1
(3) Dummy adapter (TQSOKET176SDP) 1
(4) Dummy adapter attachment screw 1
(5) Spacer 4
(6) EPOD332L01LV Manual ..... 1 (E&J)
(7) User registration card ..... 1 (E&J)
(8) Warranty card ..... 1 (E&J)
(9) Usage precautions ..... 1 (E&J)



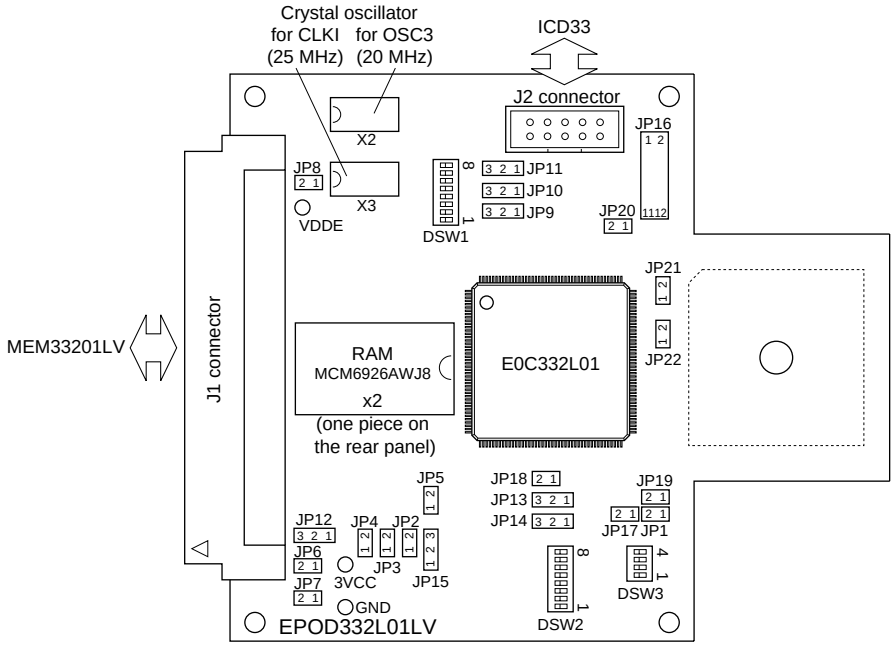
Specifications

Component	Item	Specifications	Remarks
EPOD332L01LV	Dimensions	117 mm (L) × 100 mm (W) × 30 mm (H)	Including the spacer and POD tip projection
	CPU	E0C332L01	
	RAM	256KB, MCM6926CWJ8 (Motorola) × 2	Option
	Crystal oscillator (OSC3)	20 MHz (+3.3 V), SG8002DC (with OE) (Seiko Epson)	Replaceable
	Crystal oscillator (CLKI)	25 MHz (+3.3 V), SG8002DC (with OE) (Seiko Epson)	Replaceable
	Operating (input) voltage	+5 V (5 V ± 10%), +3 V (3.3 V ± 0.3 V)	
	Current consumption	approx.280 mA (Typ.) (depending on memory access conditions)	During internal emulation at 20/40 MHz
QFP adapter	Dimensions	29 mm (L) × 29 mm (W) × 10 mm (H)	Including pin height
	Model	TQPACK176SD (Tokyo Eletech)	
Dummy adapter	Dimensions	31 mm (L) × 31 mm (W) × 15 mm (H)	Including pin height
	Model	TQSOCKET176SDP (Tokyo Eletech)	

Block Diagram



Unit Operations



Arrangement of the EPOD332L01LV board components

Setting the Jumper Pins

Note: Turn off the EPOD332L01LV power before changing jumper pin settings.

JP1 Jumper for GPIO4/INVERSE setting input

1-2 open: **Outputs FPDAT11** (default).
1-2 short: Inputs GPIO4/INVERSE setting.
The DSW3-3 setting may be input.

JP2 Sending the #CE10IN signal to the MEM33201LV (Use the default setting.)

1-2 open: **Does not send the #CE10IN signal to the MEM33201LV** (default).
1-2 short: Sends the #CE10IN signal to the MEM33201LV.

Note: When the signal is sent to the MEM33201LV, the #CE10IN pin is pulled up through 10kΩ.

JP3 Sending the #CE3 signal to the MEM33201LV (Use the default setting.)

1-2 open: **Does not send the #CE3 signal to the MEM33201LV** (default).
1-2 short: Sends the #CE3 signal to the MEM33201LV.

Note: When the signal is sent to the MEM33201LV, the #CE3 pin is pulled up through 10kΩ.

JP4 Sending the #EMEMRD signal to the MEM33201LV (Use the default setting.)

1-2 open: **Does not send the #EMEMRD signal to the MEM33201LV** (default).
1-2 short: Sends the #EMEMRD signal to the MEM33201LV.

Note: When the signal is sent to the MEM33201LV, the #EMEMRD pin is pulled through at 10kΩ.

JP5 Input of #NMI signal from the target

1-2 open: Does not connect the #NMI target signal to the E0C332L01.
1-2 short: **Connects the #NMI target signal to the E0C332L01** (default).

JP6 Connecting the MEM33201LV and the core power source (3.3V)

1-2 open: **Does not connect the LV$_{DD}$ of the MEM33201LV and the 3V$_{CC}$ (V$_{DD}$) of the EPOD332L01LV** (default).
1-2 short: Connects the LV$_{DD}$ of the MEM33201LV and the 3V$_{CC}$ (V$_{DD}$) of the EPOD332L01LV.

JP7 Connecting GND of the MEM33201LV

1-2 open: Does not connect the GND of the MEM33201LV and the AV$_{SS}$/GND of the EPOD332L01LV.
1-2 short: **Connects the GND of the MEM33201LV and the AV$_{SS}$/GND of the EPOD332L01LV** (default).

JP8 Connecting the MEM33201LV and V$_{DDE1}$

1-2 open: **Does not connect the HV$_{DD}$ of the MEM33201LV and the V$_{DDE1}$ of the EPOD332L01LV** (default).
1-2 short: Connects the HV$_{DD}$ of the MEM33201LV and the V$_{DDE1}$ of the EPOD332L01LV.

JP9 Selection of the OSC3 (high-speed) input clock

1-2 short: Inputs from the target.
2-3 short: **Uses the crystal oscillator on the EPOD332L01LV** (default).
The EPOD332L01LV has a 20-MHz crystal oscillator as part of standard specifications (replaceable).

Note: You cannot use the ceramic oscillator on the target to operate the EPOD332L01LV CPU's on-chip oscillation circuit. Set the OSC3 input clock voltage to the V$_{DD}$ voltage (3.3 V core voltage), regardless of the V$_{DDE}$ value (I/O voltage).

JP10 Selection of the SED1375 CLKI input clock

1-2 short: Inputs from the target.
2-3 short: **Uses the crystal oscillator on the EPOD332L01LV** (default).
The EPOD332L01LV has a 25-MHz crystal oscillator as part of standard specifications (replaceable).

Note: Set the CLKI input clock voltage to the V$_{DDE1}$ value (I/O voltage).

JP11 Selection of the OSC1 (32kHz) input clock

1-2 short: Inputs from the target.
2-3 short: **Uses the 32-kHz crystal oscillator on the EPOD332L01LV** (default).

Note: You cannot use the crystal resonator on the target to operate the EPOD332L01LV CPU's on-chip oscillation circuit. Set the OSC1 input clock voltage to V$_{DD}$ (3.3 V core voltage), regardless of the V$_{DDE1}$ value (I/O voltage).

JP12 #RESET signal input

1-2 short: Inputs the #RESET signal from the MEM33201LV.
2-3 short: **Inputs the #RESET signal from the target** (default).

JP13 Bus buffer (LVTH equivalent to the 16244/16245) control

1-2 short: **The buffer is active only when the external memory area is accessed** (default).
2-3 short: The buffer is always active.

JP14 D[15:0] data bus buffer (LVTH equivalent to the 16245) direction control

1-2 short: The buffer is in read direction only when reading external memory.
2-3 short: **Determined by the read/write signal for both internal and external memory** (default).

Note: Although you can set the buffer (16245 LVHT) active control using JP13, settings other than default combinations are prohibited.

(JP13)	(JP14)	
1-2 short	2-3 short	←Setting is possible.
2-3 short	1-2 short	←Setting is prohibited.

JP15 Selection of the built-in ROM area

1-2 short: **Accesses Area 10 with #CE10IN** (default).
2-3 short: Accesses Area 3 with #CE3.

JP16 Sending the ICD33 signals to the user target

1-2 open: **Does not send P14/DCLK* to the target** (default).
1-2 short: Sends P14/DCLK* to the target.

3-4 open: Does not send DSIO* to the target.
3-4 short: **Sends DSIO* to the target** (default).

5-6 open: **Does not send P12/DST2* to the target** (default).
5-6 short: Sends P12/DST2* to the target.

7-8 open: **Does not send P11/DST1 to the target** (default).
7-8 short: Sends P11/DST1 to the target.

9-10 open: **Does not send P10/DST0 to the target** (default).
9-10 short: Sends P10/DST0 to the target.

11-12 open: **Does not send P13/DPC0 to the target** (default).
11-12 short: Sends P13/DPC0 to the target.

* If you use ICD33, do not use pins DSIO, P14/DCLK, or P12/DST2 for user applications, since they are required for ICD33.
  If you do not use the ICD33 trace function, you may use P13/DPC0, P11/DST1 and P10/DST0 for user applications.
  The DSIO pin is dedicated to the ICD33.
  The I/O voltage of these ICD33 ports is the core voltage (3.3 V), not I/O voltage (V_{DDE1}) of the E0C332L01.

JP17 Connecting the target to the AV_{DDE}

1-2 open: Does not connect the target to the EPOD332L01LV AV_{DDE}.
1-2 short: **Connects the target to the EPOD332L01LV AV_{DDE}** (default).

JP18 Connecting the target to the AV_{SS}

1-2 open: Does not connect the target to the EPOD332L01LV AV_{SS}.
1-2 short: **Connects the target to the EPOD332L01LV AV_{SS}** (default).

JP19 Connecting the target to the V_{SS}

1-2 open: Does not connect the target to the EPOD332L01LV V_{SS}.
1-2 short: **Connects the target to the EPOD332L01LV V_{SS}** (default).

JP20 Connecting the target to the V_{DDE2}

1-2 open: Does not connect the target to the EPOD332L01LV V_{DDE2}.
1-2 short: **Connects the target to the EPOD332L01LV V_{DDE2}** (default).

JP21 Connecting the target to the V_{DDE1}

1-2 open: Does not connect the target to the EPOD332L01LV V_{DDE1}.
1-2 short: **Connects the target to the EPOD332L01LV V_{DDE1}** (default).

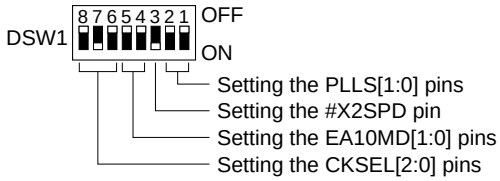
JP22 Connecting the target to the V_{DD} (3.3 V core voltage)

1-2 open: Does not connect the target to the EPOD332L01LV V_{DD}.
1-2 short: **Connects the target to the EPOD332L01LV V_{DD}** (default).

Setting the DIP Switches

Note: Turn off the EPOD332L01LV power before changing the DIP switch settings.

DSW1 Setting the E0C332L01 operation mode and the SED1375 clock



DSW1

DSW1-1, DSW1-2 (Setting the PLLS [1:0] pins)

Setting PLL mode

DSW1-2	DSW1-1	PLL mode
OFF	OFF	x2, OSC3 input frequency 10 to 20 MHz (default)
OFF	ON	x2, OSC3 input frequency 20 to 25 MHz
ON	OFF	x4, OSC3 input frequency 10 to 12.5 MHz
ON	ON	PLL not used

DSW1-3 (Setting the #X2SPD pin)

ON: **CPU clock = Bus clock x2** (default)
OFF: CPU clock = Bus clock x1

DSW1-4, DSW1-5 (Setting the EA10MD [1:0] pins)

Setting Area 10 mode

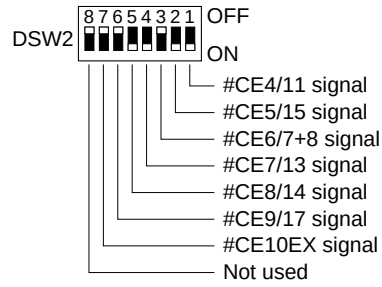
DSW1-5	DSW1-4	Area 10 mode
OFF	OFF	External ROM mode (default)
OFF	ON	Built-in ROM mode
ON	OFF	OTP mode
ON	ON	Built-in ROM emulation mode

DSW1-6, DSW1-7, DSW1-8 (Setting the CKSEL [2:0] pins)

Setting the SED1375 source clock

DSW1-8	DSW1-7	DSW1-6	SED1375 source clock
OFF	OFF	OFF	Reserved (setting disabled)
OFF	OFF	ON	1375 disable
OFF	ON	OFF	External clock input from CLKI (default)
OFF	ON	ON	OSC3 oscillation clock × 1/4
ON	OFF	OFF	OSC3 oscillation clock × 1/3
ON	OFF	ON	OSC3 oscillation clock × 1/2
ON	ON	OFF	OSC3 oscillation clock
ON	ON	ON	PLL output clock

DSW2 Setting sending of #CE (area selection) signal to the target



DSW2

DSW2-1 (#CE4/11)

OFF: Does not send the #CE4/11 signal to the target.
ON: **Sends the #CE4/11 signal to the target** (default).

DSW2-2 (#CE5/15)

OFF: Does not send the #CE5/15 signal to the target.
ON: S**ends the #CE5/15 signal to the target** (default).

DSW2-3 (#CE6/7+8)

OFF: **Does not send the #CE6/7+8 signal to the target** (default).
ON: Sends the #CE6/7+8 signal to the target.

DSW2-4 (#CE7/13)

OFF: Does not send the #CE7/13 signal to the target.
ON: **Sends the #CE7/13 signal to the target** (default).

DSW2-5 (#CE8/14)

OFF: Does not send the #CE8/14 signal to the target.
ON: **Sends the #CE8/14 signal to the target** (default).

DSW2-6 (#CE9/17)

OFF: **Does not send the #CE9/17 signal to the target** (default).
ON: Sends the #CE9/17 signal to the target.

DSW2-7 (#CE10EX)

OFF: **Does not send the #CE10EX signal to the target** (default).
ON: Sends the #CE10EX signal to the target.

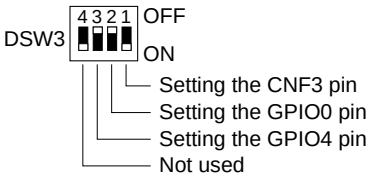
DSW2-8 (Bus release control)

OFF: **Does not use #BUSACK/P35 for bus-release control of the EPOD332L01LV** (default), but as a normal port.
ON: Uses #BUSACK/P35 for bus-release control of the EPOD332L01LV.

The address bus, data bus, #WRH/#WRL, and #RD signals of the E0C332L01 are supplied from EPOD332L01LV to the target through a buffer (equivalent to the 16244/16245). The #BUSACK signal also raises the resistance of the buffer output. To input a bus-release request (#BUSREQ signal) from the target, set DSW2-8 to ON.

Note: When using the external memory emulation board (MEM33201LV), do not feed the #CE signal of the area set as valid on the MEM33201LV (used as emulation memory) to the target; this will result in MEM33201LV and target bus collision and malfunction.
If you use #CE signals other than the above signals in the user circuit of the MEM33201LV CPLD (Altera Flex10K100A), set them as invalid, or avoid using them on the target.
The MEM33201LV is set to use #CE9/17 for CPLD and #CE10EX for emulation RAM in the default setting. When using these areas on the user target, change the MEM33201LV setting.
Do not use #CE6/7+8, as this area is used by E0C332L01 for the SED1375 block.

DSW3 Setting the SED1375 mode



DSW3

DSW3-1 (Setting the CNF3 pin)

OFF: CNF3 pin = High, big endian
ON: **CNF3 pin = Low, little endian** (default)

DSW3-2 (Setting the GPIO0 pin)

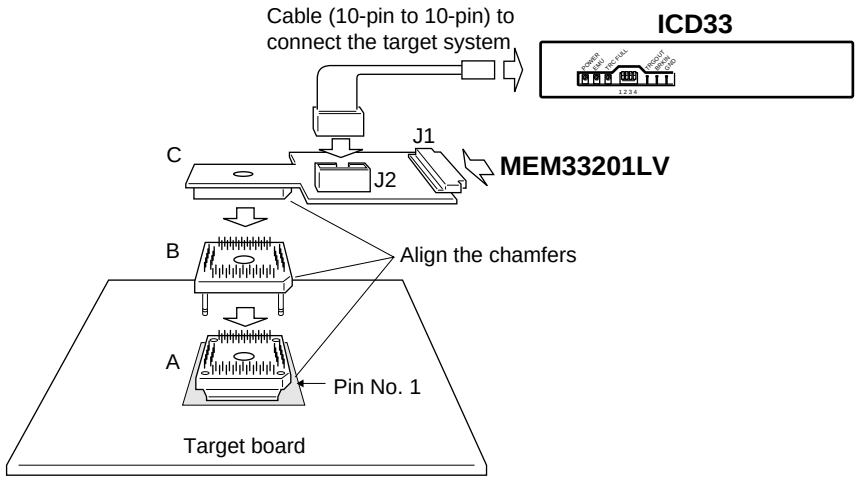
OFF: **GPIO0 pin = High** (default)
ON: GPIO0 pin = Low

DSW3-3 (Setting the GPIO4 pin)

OFF: **GPIO4 pin = High** (default)
ON: GPIO4 pin = Low

DSW3-4 (not used)

Installation to the User Target



Installing EPOD332L01LV

(1) Solder the QFP adapter (A) for user target installation to the target system.

(2) Couple the dummy adapter (B) and QFP adapter with aligned chamfers.

(3) Attach the dummy adapter to the QFP adapter with the supplied attachment screw. If you can drill a hole on the target system board to attach the EPOD332L01LV, skip this step and attach it in step (5).

(4) Couple EPOD332L01LV (C) and the dummy adapter with aligned chamfers. To disconnect the EPOD332L01LV, pull it out while keeping the dummy board in place.

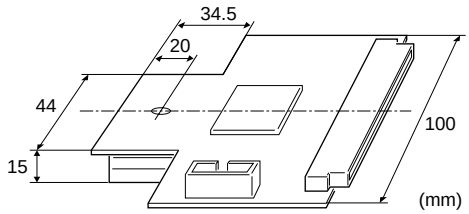
(5) If you can drill a hole on the target system board to attach the EPOD332L01LV, skip step (3) and attach the QFP adapter, dummy adapter, and EPOD332L01LV on the target system board in this step.

(6) Connect EPOD332L01LV and ICD33 with the 10-pin cable (enclosed in the ICD33 package).

Note: When you connect or disconnect the EPOD332L01LV or the dummy adapter, push or pull in vertically. Pushing or pulling the pins at an angle will bend the pins and lead to system malfunctions. Avoid connecting/disconnecting the EPOD332L01LV or dummy adapter more than 100 times.
To connect EPOD332L01LV to the user target, always use the dummy adapter. If you directly insert the socket of the EPOD332L01LV into the QFP adapter, signals will short-circuit and cause the system to malfunction.

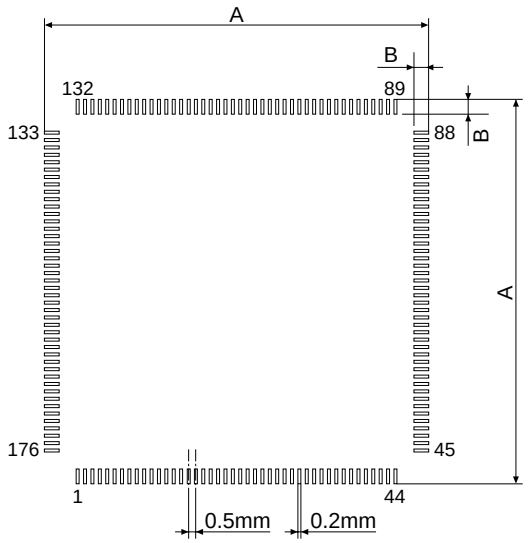
Area occupied by the EPOD332L01LV

The EPOD332L01LV occupies the area shown in the illustration below. Design the target system to prevent interference with the EPOD332L01LV.



Dimensions of the EPOD332L01LV

Dimensions of the QFP adapter pins/foot pattern



Dimensions	A	B
TQPACK	26.0 mm	1.125 mm
Foot pattern	27.0 mm	1.9 mm

Dimensions of the QFP adapter

Note: Dimensions differ from those of the actual IC. To design mass-production boards for actual IC installation, see the "E0C332L01 Technical Manual".

Soldering installing QFP adapter

Follow the steps given below to solder the QFP adapter to the target system board.

(1) The chamfered part of the QFP adapter is the position of pin No. 1. Set the QFP adapter on the target system board in the proper direction.

(2) Clean the QFP adapter pins for board installation with flux. Apply cream solder to the foot pattern of the target system board.

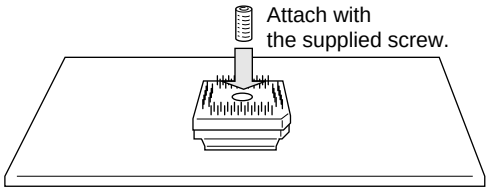
(3) Apply an instant-bond adhesive or epoxy-base adhesive to the four projections on the bottom of the QFP adapter. Temporarily attach the QFP adapter to the target system board.

(4) Solder the QFP adapter to the target system board by hand or in a reflow furnace at the following temperatures.
Reflow furnace: 240°C for 20 seconds or less
Manual: 240°C for 10 seconds or less per pin

Attaching the EPOD332L01LV

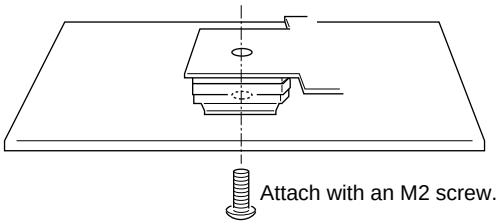
Attach the EPOD332L01LV to the target board by the following method.

(1) If you are unable to drill a hole on the system board to attach the EPOD332L01LV:
After coupling the QFP and dummy adapters, attach with the supplied screw.



Attaching the EPOD332L01LV (1)

(2) If you can drill a hole on the target system board to attach the EPOD332L01LV:
After coupling the QFP adapter, dummy adapter and EPOD332L01LV, attach with a screw from the rear panel of the target system board.
Drill the hole to the following specifications.
Size of the screw hole ϕ2.4mm
Wiring prohibited area: ϕ3.6mm (from the screw hole center)
Attachment screw: M2 (mm)



Attaching the EPOD332L01LV (2)

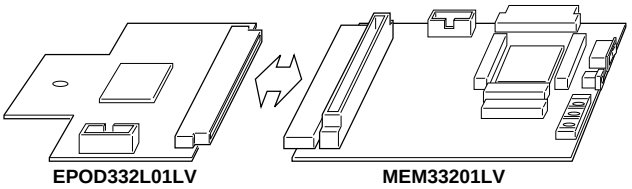
Note: To guard against thread-stripping and resulting system malfunctions, avoid overtightening the screw.

For detailed technical information on the QFP adapter, see the Tokyo Eletech Corporation home page.
http://www.tetc.co.jp/e_tet.htm

Connecting the MEM33201LV Board

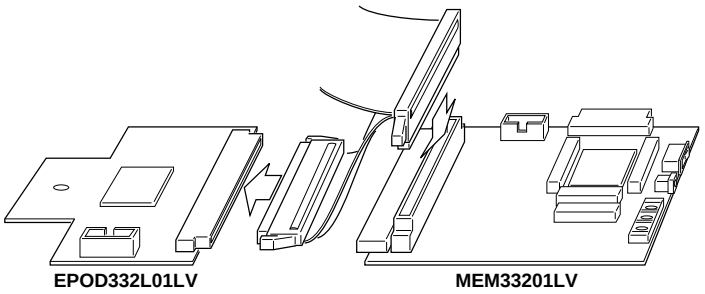
When using the external memory emulation board MEM33201LV, connect it to the user target board by one of the following methods that best suits the profile of the board.

(1) Direct connection of the EPOD332L01LV and MEM33201LV connector
Direct-connect the J1 connector of the EPOD332L01LV and the J10 connector of the MEM33201LV (angle connector).



Connecting the MEM33201LV board (1)

(2) Connection with a flat cable
Connect the J1 connector of the EPOD332L01LV and the J11 connector of the MEM33201LV (straight connector) with the supplied flat cable.



Connecting the MEM33201LV board (2)

Supplying Power

Supply power to EPOD332L01LV by one of the following three methods.

(1) From the user target:
The power source of the EPOD332L01LV is connected to the power source of the user target through the QFP socket at the jumper (JP17 to JP22) default setting.
JP17 1-2 short: Connects the target to the EPOD332L01LV AVDDE.
JP18 1-2 short: Connects the target to the EPOD332L01LV AVSS.
JP19 1-2 short: Connects the target to the EPOD332L01LV VSS.
JP20 1-2 short: Connects the target to the EPOD332L01LV VDDE2.
JP21 1-2 short: Connects the target to the EPOD332L01LV VDDE1.
JP22 1-2 short: Connects the target to the EPOD332L01LV VDD.

The power supplied to the user target is also supplied to EPOD332L01LV at this setting. Use the system at the following voltages.
VDD = 3.0 to 3.6V, VDDE1 = VDDE2 = AVDDE = 3.0 to 5.5V, VSS = AVSS = 0V

To supply power to the external memory emulation board (MEM33201LV) connected to EPOD332L01LV from the user target, set JP6, JP7, and JP8 as follows to connect the power lines between the MEM33201LV and EPOD332L01LV.
JP6 1-2 short: Connects the LVDD of the MEM33201LV and the 3VCC (VDD) of the EPOD332L01LV.
JP7 1-2 short: Connects the GND of the MEM33201LV and the AVSS/GND of the EPOD332L01LV.
JP8 1-2 short: Connects the HVDD of the MEM33201LV and the VDDE1 of the EPOD332L01LV.

Since the MEM33201 consumes a current of several hundred milliamperes, the power source unit of the user target must be able to supply this current. If the target power source is inadequate, supply power separately to the MEM33201LV with the supplied AC adapter. In this case, do not connect the power sources for the MEM33201LV and EPOD332L01LV.

(2) Form the EPOD332L01LV test pins:
You can supply power from the following EPOD332L01LV test pins.
TP1 (3VCC): VDD (3.0 to 3.3V)
TP2 (VDDE): VDDE1 (3.0 to 5.5V)
TP3 (GND): VSS (0V)

To do this, set JP6, JP7, and JP8 as follows.
JP6 1-2 short: Connects the LVDD of the MEM33201LV and the 3VCC (VDD) of the EPOD332L01LV.
JP7 1-2 short: Connects the GND of the MEM33201LV and the AVSS/GND of the EPOD332L01LV.
JP8 1-2 short: Connects the HVDD of the MEM33201LV and the VDDE1 of the EPOD332L01LV.

The power supplied from the test pins is also supplied to the user target according to the default settings for JP17 to JP22, shown in (1). If you connect MEM33201LV at the above jumper setting, supply power from the MEM33201LV side, since the power supply line connection to the test pins is unreliable.

(3) From MEM33201LV:
Set JP6, JP7, and JP8 as follows, and supply power to the MEM33201LV.
JP6 1-2 short: Connects the LVDD of the MEM33201LV and the 3VCC (VDD) of the EPOD332L01LV.
JP7 1-2 short: Connects the GND of the MEM33201LV and the AVSS/GND of the EPOD332L01LV.
JP8 1-2 short: Connects the HVDD of the MEM33201LV and the VDDE1 of the EPOD332L01LV.

The power supplied from the MEM33201LV is also supplied to the user target according to the default settings for JP17 to JP22, shown in (1).

Note: The voltage supplied by the methods (2) and (3) are VDD (3.3V core voltage) and VDDE1 (I/O voltage) only. Supply AVDDE (voltage for analog signals) and VDDE2 (voltage for SED1375) from the user target. If you supply power (VDD/VDDE1) from the MEM33201LV, set the jumpers to separate it from the user target power source.

Built-in ROM Emulation

Installing emulation RAM

When using the following RAM, you can optionally emulate built-in ROM.
Motorola MCM6926AWJ8 2 pieces

Insert the RAM into the sockets on the front and back sides of the EPOD332L01LV. Always use two RAM chips. If you use only one RAM, the system will not work.

Align the chamfered part of the socket at pin No. 1 (○) on the IC.

Installing RAM

Set pin No. 1 to the correct position.
This emulation memory supports bus clocks of maximum 40MHz.

Area 10 emulation

Set area to emulate at Area 10 (default) with JP15, and Area 10 mode with DSW 1-4 and 1-5. An emulation RAM of 256KB may be installed on the EPOD332L01LV.

Note: The RAM for built-in ROM emulation (equivalent to the Motorola MCM6926) is optional.

You may use the target program to write data to emulation RAM in half-word size. You cannot write data to actual ROMs. To fill, copy, or input data to this area using a debugger, use the commands for half-words.

Setting the capacity of the built-in ROM

The capacity of the ROM built into the E0C332L01 is determined by A10R[2:0] (D[E:C]) of the Area 10-9 setup register (0x48126) in the BCU.

Built-in ROM capacity

A10R2(DE)	A10R2(DD)	A10R2(DC)	Built-in ROM capacity
1	1	1	2MB
1	1	0	1MB
1	0	1	512KB
1	0	0	256KB
0	1	1	128KB
0	1	0	64KB
0	0	1	32KB
0	0	0	16KB

To download a program to the built-in ROM area through ICD33, set its capacity as shown in the following example.
In E0C332L01, data that exceeds the capacity of the built-in ROM is automatically changed to access external memory.
In the emulation RAM of the EPOD332L01LV, the built-in ROM part and the external emulation memory are independent. To download a program, note that the built-in ROM area and external emulation memory area are used in the following manner, due to the limited capacity of the built-in ROM.

Example: Setting the capacity of the built-in ROM to 128KB

Write 0x3037 in the address 0x48126.

The capacity of the built-in ROM of the E0C332L01 is set to 2MB (D[E:C] = 0x111) as the default setting. Change it to 128KB (D[E:C] = 0x011).
Keep the contents of other BCU registers unchanged at this stage.
With this setting, the data exceeding 128KB is automatically switched to access external memory.
If you do not set the capacity of the built-in ROM, you can access the ROM up to 256KB set to EPOD332L01LV. Use care; data exceeding 256KB may be overwritten by the address mirror.

Area 3 emulation

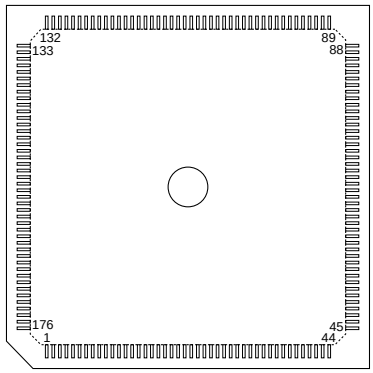
Set Area 3 with JP4 and the Area 3 emulation bit (0x48130/DB) in a BCU register to "0".
With this setting, you may use 0x80000 to 0xbffff of the installed RAM for the emulation of built-in 256KB ROM.

Crystal Oscillator

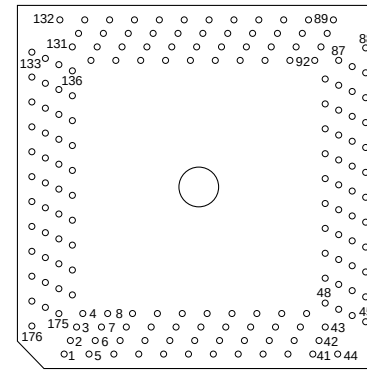
The EPOD332L01LV has a 20-MHz crystal oscillator for the OSC3 clock and a 25-MHz crystal oscillator for CLKI (clock for SED1375) input as the standard specification. These oscillators are the SG8002DC (with OE) for 3.3 V operations manufactured by Seiko Epson. These oscillators may be replaced if necessary.

Pin Arrangement

QFP Adapter for Board Installation



QFP adapter pins

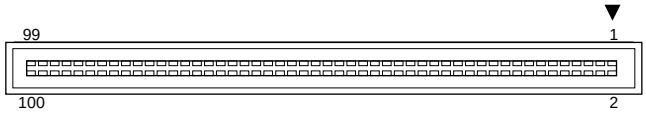


Dummy adapter pins

No.	Pin name	No.	Pin name	No.	Pin name	No.	Pin name
1	A23	45	D2	89	N.C.	133	P21/#DWE/#GAAS
2	A22	46	D1	90	VSS	134	P20/#DRD
3	A21	47	D0	91	**N.C.** (GPIO0)	135	P16/EXCL5/#DMAEND1
4	A20	48	VSS	92	FPDAT11/GPIO4/INVERSE	136	P15/EXCL4/#DMAEND0
5	VDDE1	49	BCLK	93	FPDAT10/GPIO3	137	VDDE1
6	A19	50	**N.C.** (#EMEMRD)	94	FPDAT9/GPIO2	138	P14/FOSC1/DCLK
7	A18	51	#RD	95	VDDE2	139	P13/EXCL3/T8UF3/DPCO
8	A17	52	#WRL/#WR/#WE	96	FPDAT8/GPIO1	140	P12/EXCL2/T8UF2/DST2
9	A16	53	#WRH/#BSH	97	FPSHIFT	141	P11/EXCL1/T8UF1/DST1
10	A15	54	VDDE1	98	FPDAT7	142	P10/EXCL0/T8UF0/DST0
11	VSS	55	#CE10EX/#CE9&10EX	99	FPDAT6	143	VSS
12	A14	56	**N.C.** (#CE10IN)	100	FPDAT5	144	P07/#SRDY1/#DMAEND3
13	A13	57	**N.C.** (#CE3)	101	VDD	145	P06/#SCLK1/DMAACK3
14	A12	58	VSS	102	FPDAT4	146	P05/SOUT1/#DMAEND2
15	A11	59	K67/AD7	103	FPDAT3	147	P04/SIN1/#DMAACK2
16	A10	60	K66/AD6	104	FPDAT2	148	VDD
17	VDD	61	K65/AD5	105	FPDAT1	149	**N.C.** (OSC2)
18	A9	62	AVDDE	106	VSS	150	OSC1
19	A8	63	K64/AD4	107	FPDAT0	151	VSS
20	A7	64	K63/AD3	108	FPLINE	152	P03/#SRDY0
21	A6	65	K62/AD2	109	FPFRAME	153	P02/#SCLK0
22	A5	66	AVSS	110	DRDY/MOD/FPSHIFT2	154	P01/SOUT0
23	VSS	67	K61/AD1	111	VDDE2	155	P00/SIN0
24	A4	68	K60/AD0	112	LCDPWR	156	**N.C.** (CNF3)
25	A3	69	K54/#DMAREQ3	113	N.C.	157	**N.C.** (CKSEL2)
26	A2	70	K53/#DMAREQ2	114	N.C.	158	**N.C.** (CKSEL1)
27	A1	71	K52/#ADTRG	115	N.C.	159	**N.C.** (CKSEL0)
28	A0/#BSL	72	VDD	116	N.C.	160	VDDE1
29	VDDE1	73	K51/#DMAREQ1	117	N.C.	161	CLKI
30	D15	74	K50/#DMAREQ0	118	VSS	162	ICEMD
31	D14	75	#LCAS	119	P35/#BUSACK	163	VSS
32	D13	76	#HCAS	120	P34/#BUSREQ/#CE6	164	**N.C.** (OSC4)
33	D12	77	#CE9/#CE17/#CE17&18	121	P33/#DMAACK1	165	OSC3
34	D11	78	VSS	122	P32/#DMAACK0	166	**N.C.** (EA10MD1)
35	VSS	79	#CE8/#RAS1/#CE14/#RAS3	123	P31/#BUSGET/#GARD	167	**N.C.** (EA10MD0)
36	D10	80	#CE7/#RAS0/#CE13/#RAS2	124	P30/#WAIT/#CE4&5	168	**N.C.** (#X2SPD)
37	D9	81	#CE5/#CE15/#CE15&16	125	VDD	169	VDD
38	D8	82	#CE4/#CE11/#CE11&12	126	P27/TM5	170	**N.C.** (PLLS1)
39	D7	83	#CE6/#CE7&8	127	P26/TM4	171	**N.C.** (PLLS0)
40	D6	84	VDDE1	128	P25/TM3	172	#NMI
41	VDD	85	N.C.	129	P24/TM2	173	VSS
42	D5	86	N.C.	130	P23/TM1	174	**N.C.** (PLLC)
43	D4	87	N.C.	131	VSS	175	#RESET
44	D3	88	N.C.	132	P22/TM0	176	DSIO

Arrangement of the QFP adapter pins for board installation

Connector for MEM33201LV Connection

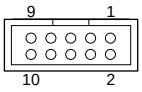


No.	Pin name	No.	Pin name	No.	Pin name	No.	Pin name
1	VDDE (HVDD)	26	A19	51	D9	76	#CE4/#CE11/#CE11&12
2	VDDE (HVDD)	27	GND	52	GND	77	#CE5/#CE15/#CE15&16
3	A0/#BSL	28	A20	53	D10	78	#CE6/#CE7&8
4	A1	29	A21	54	GND	79	#CE9/#CE17/#CE17&18
5	A2	30	A22	55	D11	80	#CE10EX/#CE9&10EX
6	A3	31	A23	56	GND	81	#CE10IN
7	GND	32	GND	57	D12	82	GND
8	A4	33	D0	58	GND	83	P30/#WAIT/#CE4&5
9	A5	34	GND	59	D13	84	GND
10	A6	35	D1	60	GND	85	P34/#BUSREQ/#CE6
11	A7	36	GND	61	D14	86	GND
12	GND	37	D2	62	GND	87	P21/#DWE/#GAAS
13	A8	38	GND	63	D15	88	P31/#BUSGET/#GARD
14	A9	39	D3	64	GND	89	GND
15	A10	40	GND	65	#RD	90	#CE3
16	A11	41	D4	66	GND	91	#EMEMRD
17	GND	42	GND	67	#WRL/#WR/#WE	92	#URESET *1
18	A12	43	D5	68	#WRH/#BSH	93	#RESET *2
19	A13	44	GND	69	GND	94	GND
20	A14	45	D6	70	#CE7/#RAS0/#CE13/#RAS2	95	#NMI *3
21	A15	46	GND	71	#CE8/#RAS1/#CE14/#RAS3	96	GND
22	GND	47	D7	72	GND	97	BCLK
23	A16	48	GND	73	#HCAS	98	GND
24	A17	49	D8	74	#LCAS	99	VDD (LVDD)
25	A18	50	GND	75	GND	100	VDD (LVDD)

*1: Outputs a reset signal from the user target to the MEM33201LV.
*2: Reset input signal from the MEM33201LV
*3: #NMI input signal from the MEM33201LV (The MEM33201LV side can also be set for input by the Flex10K100A terminal setting.)

Arrangement of connector pins for connecting MEM33201LV

Connector for ICD33 Connection



No.	Pin name	No.	Pin name
1	DCLK	6	GND
2	GND	7	DST1
3	DSIO	8	GND
4	GND	9	DST0
5	DST2	10	DPCO

Arrangement of connector pins for connecting ICD33

Precautions

Connecting, installing, and removing components

- Always turn off the system power before connecting or disconnecting the EPOD332L01LV, ICD33, target system and MEM33201LV, or setting jumpers or DIP switches. Connecting or disconnecting these components with the power on will damage the system.
- Use the dummy adapter to install EPOD332L01LV to the user target. Inserting the EPOD332L01LV socket directly into the QFP adapter will short-circuit signal currents and cause the system to malfunction.
- When connecting or disconnecting the EPOD332L01LV or dummy adapter, be careful to push or pull straight in or out. Pushing or pulling the pins at an angle will bend or break the pins and lead to system malfunctions. Avoid connecting/disconnecting the EPOD332L01LV or dummy adapter more than 100 times.
- To prevent thread-stripping and system malfunctions, avoid overtightening the EPOD332L01LV attachment screw.

Power supply

The voltage supplied from the MEM33201LV or EPOD332L01LV test pins are V_{DD} (3.3 V core voltage) and V_{DDE1} (I/O voltage) only. Supply AV_{DDE} (voltage for analog signals) and V_{DDE2} (voltage for SED1375 block) from the user target.
If you supply power (V_{DD}/V_{DDE1}) from the MEM33201LV, set the jumpers to separate it from the user target power source.

Emulation of built-in ROM

To use Area 10 in built-in ROM emulation mode, set the capacity of the built-in ROM by A10R[2:0] (D[E:C]) of the Area 10-9 setup register (0x48126) of the E0C332L01 BCU.
As an option, you can install built-in ROM emulation memory (maximum 256KB) on the EPOD332L01LV. However, the above register is initially set to 2MB. Work cautiously, since data exceeding 256KB may be overwritten in the built-in ROM emulation memory rather than external memory.

Oscillating circuit and clock input

- You cannot use the crystal resonator or ceramic oscillator on the target to operate the oscillation circuits (OSC1 and OSC3) built into the EPOD332L01LV CPU.
- If you input OSC1 and OSC3 clock signals from the user target, set the input clock voltage to V_{DD} (3.3 V core voltage), regardless of the V_{DDE1} value (I/O voltage).
- If you input the CLKI clock from the user target, set the input clock voltage to V_{DDE1} (I/O voltage).

Bus-release control

- To input the #BUSREQ signal for bus-release control from the user target, set DSW2-8 to ON (to use #BUSACK/P35 for bus-release control of the EPOD332L01LV).
  The buffer output will not present a high impedance if the above setting is not performed, since the E0C332L01 address bus, data bus, #WRH/#WRL, and #RD signals are sent from EPOD332L01LV to the target through a buffer (equivalent to the 16244/16245).
- You cannot perform bus-release control of the EPOD332L01LV during the DMA cycle. When necessary, install a CPU on the user target to evaluate bus-release control.

#CE (area selection) signal

When using the external memory emulation board (MEM33201LV), do not feed the #CE signal of the area set as valid on the MEM33201LV (used as emulation memory) to the target; this will result in MEM33201LV and target bus collision and malfunction.
If you use #CE signals other than the above signals in the user circuit of the MEM33201LV CPLD (Altera Flex10K100A), set them as invalid, or avoid using them on the target.
The MEM33201LV is set to use #CE9/17 for CPLD and #CE10EX for emulation RAM in the default setting. When using these areas on the user target, change the MEM33201LV setting.
Do not use #CE6/7+8, as this area is used by E0C332L01 for the SED1375 block.

Bus drive capacity

The following EPOD332L01LV signals are sent to the target through a buffer (equivalent to the 7416244/7416245, LVTH).
A[23:0], D[15:0], #RD, #WRH, #WRL

The capacity will thus be higher than that of the actual IC.
Other signal pins, including the E0C332L01 CPU power supply pins, are connected to the target directly.

Pull-up and damper resistors

- Pull-up resistors are connected to the following signal lines.
  - The #CE10IN signal is pulled up through 10 kΩ when it is sent to the MEM33201LV.
  - The #CE3 signal is pulled up through 10 kΩ when it is sent to the MEM33201LV.
  - The #EMEMRD signal is pulled up through 10 kΩ when it is sent to the MEM33201LV.
  - In bus-release control (with #BUSREQ/#BUSACK in use), the #BUSACK (P35) signal is pulled up through 10 kΩ.
- A 33 Ω damper resistor is inserted into the lines for OSC1, OSC3 and CLKI signals received from the user target.

MEM33201 standard interface

In the MEM33201 standard interface, the #RESET and #NMI I/O directions are as follows.
#RESET: Input from the MEM33201LV to the EPOD332L01LV
#NMI: Input from the MEM33201LV to the EPOD332L01LV (Output is possible through the Flex10K100A terminal setting.)

Emulation Memory Board

MEM33201/MEM33201LV

Overview

The MEM33201/MEM33201LV (hereinafter referred to as MEM33201) is a memory board used to develop products that use the 32-bit E0C332XX RISC CPU series. This memory board can be connected to a EPOD332XX (Emulation Probe of Device) or user targets as external memory and comes with 4MB of high-speed SRAM (maximum 33 MHz one-wait operation possible) and 1MB of flash ROM to enable real-time emulation of product memory.
The MEM33201 comes with a large-capacity high-speed CPLD (Altera Corp. FLEX 10K100A-2: equivalent to 100,000 logic gates) for user logic implementation and offers break functions to strengthen ICD33 debugging capabilities. You may program CPLD user logic to use the MEM33201 as an external ASIC, or as a prototype of a 2-in-1 LSI system.

Features

- High-speed external emulation memory
  - High-speed asynchronous SRAM: 4MB (mapping possible within each 2MB block)
    Access time 15 ns, 33 MHz one-wait operation (no-wait operation is not possible)
  - Flash ROM: 1MB
    Access time 55 ns/MEM33201 (5 V), 70 ns/MEM33201LV (3.3 V), 25 MHz one-wait operation, AMD type.
  - May be used as general-purpose RAM or ROM (allowing program downloads).
- #CE (area selection signal) for MEM33201 access may be changed (selected from seven areas).
- Comes with a standard interface to connect to an EPOD332XX (direct or flat cable connection between boards).
- Cascade-connections are possible between MEM33201 boards.
- Comes with an AC adapter (5 V/2 A) (may be used for both 5 V and 3.3 V systems).
- Equipped with CPLD for user logic implementation (equivalent to 100,000 gates).
  - Altera Corp. FLEX10K100A (EPF10K100ARC240-2)
  - User logic configuration with JTAG
  - Comes with a configuration EEPROM (Altera Corp. EPC2) for FLEX10K100A.
  - Provided with user logic test pins and interface connector
- CPLD circuit to extend debug function (to connect to ICD33)
  - CE break function
  - Map break function
  - Bus break function
  - Area break function
- Equipped with test pins (60-pin) for the E0C332XX bus monitor
- Incorporates a dynamic write-protect function for external emulation RAM.
  May be used as external write-protected ROM during emulation.

Models

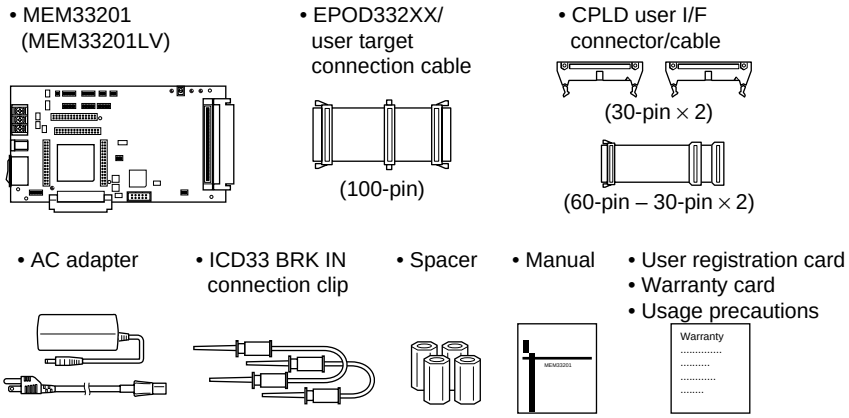
MEM33201: For 5 V operation at V_{DDE} (I/O voltage) = 5 V and V_{DD} (core voltage) = 3.3 V
MEM33201LV: For 3.3 V operation at V_{DDE} (I/O voltage) = 3.3 V and V_{DD} (core voltage) = 3.3 V

Use the same operating voltage for the connected EPOD332XX and the user target. Both the MEM33201/MEM33201LV and the EPOD332XX/EPOD332XXLV will be referred to as the MEM33201 and EPOD332XX, except in cases where a distinction needs to be made.

Package Contents

The MEM33201 package includes the following.

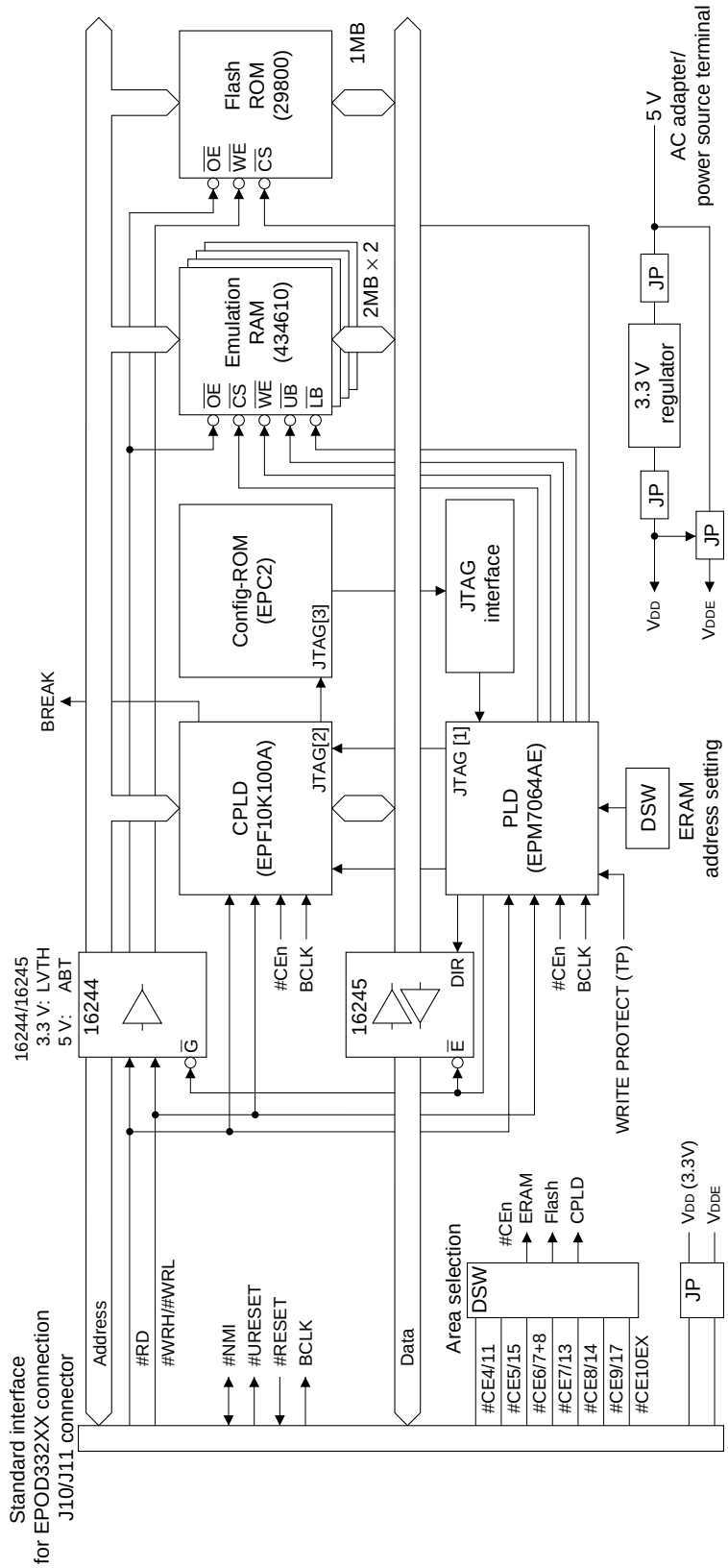
(1) MEM33201 unit 1
(2) Flat cable (100-pin) for connecting EPOD332XX and MEM33201 1
(3) CPLD user interface connector (30-pin) 2
(4) CPLD user interface cable (60-pin → 30-pin x2) 1
(5) Clip for ICD33 connection 2
(6) Spacer 4
(7) AC adapter (5V 2A) 1
(8) MEM33201 / MEM33201LV Manual ..... 1 (E&J)
(9) User registration card ..... 1 (E&J)
(10) Warranty card ..... 1 (E&J)
(11) Usage precautions ..... 1 (E&J)



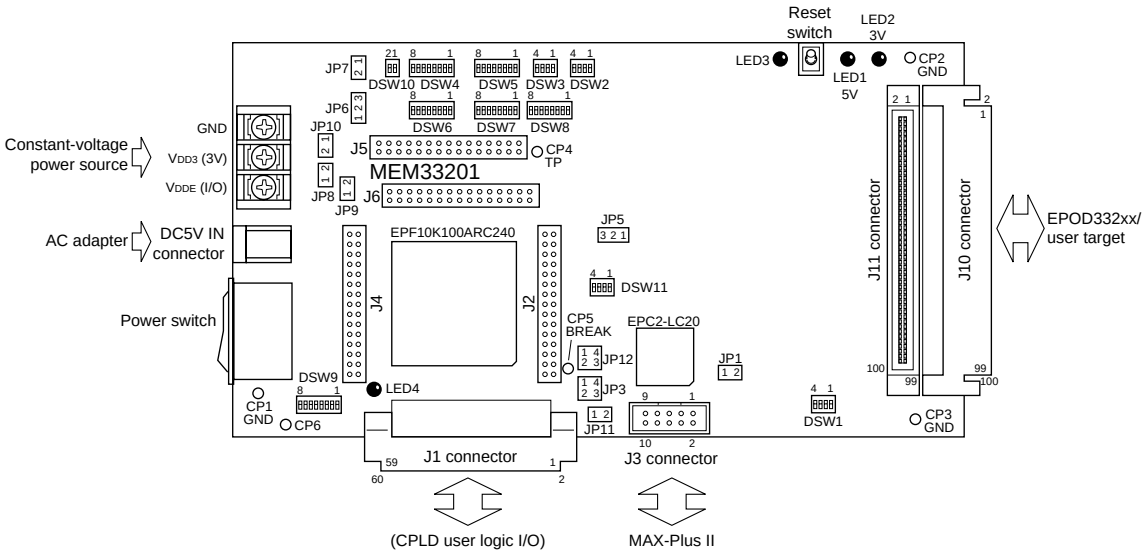
Specifications

Component	Item	Specifications	Remarks
MEM33201 (MEM33201LV)	Dimensions	175 mm (L) × 100 mm (W) × 30 mm (H)	Including the spacer and projections
	Operating voltage	DC 5 V ± 5%	
	Operating current	MEM33201: approx.100 mA (Typ.) MEM33201LV: approx.70 mA (Typ.)	MEM33201 (LV), Depending on the conditions for memory access and the CPLD circuit.
	EPOD332XX connector	KEL 8800-100-170L or 8801-100-170L right angle, 100-pin, half-pitch	For direct connection
		KEL 8830E-100-170S straight, 100-pin, half-pitch	For flat cable connection
	CPLD connector	KEL 8830E-60-170L right angle, 60-pin, half-pitch	
AC adapter	Dimensions	110 mm (L) × 57.5 mm (W) × 33.5 mm (H)	
	Input voltage	AC 100 to 240 V	
	Input frequency	47 to 440 Hz	
	Operating current	0.19 to 0.33 A	
	Output voltage/current	DC 5 V/2 A (Max.)	
EPOD332XX connection cable	Length	170 mm (100 mm + 70 mm)	
	Cable connector	KEL 8825E-100-175	x3
CPLD user interface connector/cable	Target connector	3M 3440-6002LC (30-pin, full-pitch)	x2
	Cable length	approx.200 mm	
	Cable connector	KEL 8822E-060-171 (60-pin, half-pitch)	x1, MEM33201 side
		3M 7930-6500SC (30-pin, full-pitch)	x2, user target side
ICD33 connection clip	Length	400 mm	x2

Block Diagram



Unit Operations



Arrangement of the MEM33201 board components

Switches

Power switch

This is the MEM33201 power switch.

Note: This switch controls power from the AC adapter or power supply terminals on the MEM33201, but is disabled if power is set to be supplied from the user target or the EPOD332XX by jumper setting (JP7, JP8).

Reset switch

This switch generates a #RESET signal that can be output to external units through the standard interface connector (J10, J11) by a jumper setting (JP1).

Setting the Jumper Pins

Note: Turn off the MEM33201 power before changing jumper pin settings.

JP1 #RESET signal output

1-2 open: **Does not output standard interface #RESET signal** (default).
1-2 short: Outputs the #RESET signal.

The setting "Outputs" connects the MEM33201 reset switch signal and the #URESET signal (reset signal from the user target) input from the standard interface connector (J10, J11) to the #RESET signal of the standard interface connector, producing two output signals.
The setting "Does not output" does not connect the above two signals to the #RESET signal. However, the #RESET signal input from external units through the standard interface connector is valid.

Note: If you output a #RESET signal, make sure the xRESET signal of the cascade-connected MEM33201 and EPOD332XX does not conflict with the #RESET signal.

JP3 Signal connection between Altera FLEX10K100A and configuration ROM (EPC2)

(Use the default setting.)

1-2 open: Does not connect nStatus (FLEX10K100A) and OE (EPC2).
1-2 short: **Connects nStatus (FLEX10K100A) and OE (EPC2)** (default).

3-4 open: Does not connect CONF_DONE (FLEX10K100A) and nCS (EPC2).
3-4 short: **Connects CONF_DONE (FLEX10K100A) and nCS (EPC2)** (default).

JP5 Setting the built-in ROM area (Use the default setting.)

1-2 short: **Area 10/#CE10IN** (default)
2-3 short: Area 3/#CE3IN

JP6 Setting the VDDE (I/O voltage)

(when 5 V is applied from the AC adapter or external constant-voltage power source.)

1-2 short: VDDE = 5 V (default of MEM33201)
2-3 short: VDDE = 3.3 V (default of MEM33201LV)

Note: When using 3.3 V, set JP9 for "1-2 short" to generate 3.3 V (by supplying 5 V to the 3.3 V regulator).

JP7 Connecting the VDDE (I/O voltage) power line to an EPOD332XX (or user target)

1-2 open: **Does not connect the VDDE of EPOD332XX** (default).
1-2 short: Connects the VDDE of EPOD332XX.

This setting connects or disconnects the VDDE pin of the standard interface connector (J10, J11) to or from the MEM33201 VDDE.

JP8 Connecting the VDD (3.3 V core voltage) power line to an EPOD332XX (or user target)

1-2 open: **Does not connect the VDD of EPOD332XX** (default).
1-2 short: Connects the VDD of EPOD332XX.

This setting connects or disconnects the VDD pin of the standard interface connector (J10, J11) to or from the MEM33201 VDD.

JP9 Supplying voltage to the 3.3 V regulator

1-2 open: Does not supply voltage to the 3.3 V regulator.
1-2 short: **Supplies voltage to the 3.3 V regulator** (default).

You may use the 3.3 V regulator if you supply 5 V from the AC adapter or an external constant-voltage power source.

JP10 Supplying the voltage output from the 3.3 V regulator

1-2 open: Does not connect the 3.3 V regulator output.
1-2 short: **Connects the 3.3 V regulator output** (default).

To control power supply involving JP8 to JP10, see "Supplying Power".

JP11 Connecting the FLEX10K100A pin No. 103 and the #NMI signal

(#NMI on the standard interface and the xNMI input/pin No. 87 of FLEX10K100A)
1-2 open: **Does not connect pin Nos. 87 and 103 for the FLEX10K100A** (default).
1-2 short: Connects pin Nos. 87 and 103 of FLEX10K100A.

Note: If you set to output the #NMI of FLEX10K100A, note that it is output to an EPOD332XX (user target). If you connect the #NMI signal, set the I/O of the FLEX10K100A correctly (terminal).

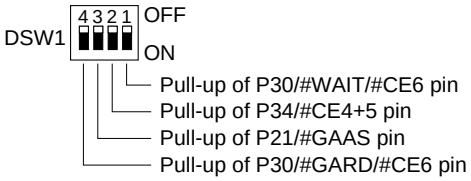
JP12 Setting the CPLD operating voltage (configuration EEPROM EPC2 for FLEX10K100A)

Do not change the following settings.
1-2 open
3-4 open

Setting the DIP Switches

Note: Turn off the MEM33201 power before changing the DIP switch settings.

DSW1 Setting the pull-up for the E0C332XX P port extended function pin



DSW1

DSW1-1 (Pull-up of P30/#WAIT/#CE6 pin)
OFF: **No pull-up resistor** (default)
ON: With pull-up resistor

DSW1-2 (Pull-up of P34/#CE4+5 pin)
OFF: **No pull-up resistor** (default)
ON: With pull-up resistor

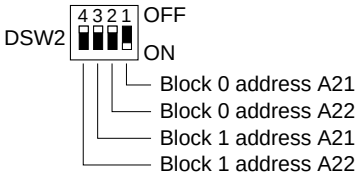
DSW1-3 (Pull-up of P21/#GAAS pin)
OFF: **No pull-up resistor** (default)
ON: With pull-up resistor

DSW1-4 (Pull-up of P30/#GARD/#CE6 pin)
OFF: **No pull-up resistor** (default)
ON: With pull-up resistor

Note: The pull-up resistance is 10 kΩ.

DSW2 Setting emulation RAM address blocks

Sets the addresses (decoder by the E0C332XX A22 and A21 signals) for emulation RAM (SRAM) allocation.
The 4MB of emulation RAM is divided into two 2MB blocks (blocks 0 and 1). You may set the starting address to either block.



DSW2

DSW2-1, DSW2-2 (block 0 starting address)
DSW2-3, DSW2-4 (block 1 starting address)

Setting the block 0 starting address

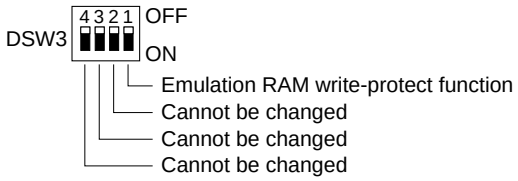
DSW2-2(4)	DSW2-1(3)	A[22:21]	Accessible address range
OFF	OFF	11	0x#E00000–0x#FFFFFF or 0x#600000–0x#7FFFFF
OFF	ON	10	0x#C00000–0x#DFFFFF or 0x#400000–0x#5FFFFF
ON	OFF	01	0x#A00000–0x#BFFFFF or 0x#200000–0x#3FFFFF
ON	ON	00	0x#800000–0x#9FFFFF or 0x#000000–0x#1FFFFF

(# = 0–F)

The default setting is given below.
Block 0: DSW2-2 = OFF, DSW2-1 = ON (0x#C00000 to 0x#DFFFFF or 0x#400000 to 0x#5FFFFF)
Block 1: DSW2-2 = OFF, DSW2-1 = OFF (0x#E00000 to 0x#FFFFFF or 0x#600000 to 0x#7FFFFF)

This setting decodes the address signal A[23:0] input from the standard interface connector to access to each of the two 2MB blocks.
Allocation of emulation RAM also requires the selection of area (#CEn) by DSW4 (for block 0) and DSW5 (for block 1). The range (ending address) of accessible addresses depends on the size of the selected #CE area.
To allocate addresses, see "MEM33201 Mapping".

DSW3 PLD mode SW



DSW3

DSW3-1 (Setting the emulation RAM write-protect function)

OFF: **Do not use the emulation RAM write-protect function** (default).
ON: Use the emulation RAM write-protect function.

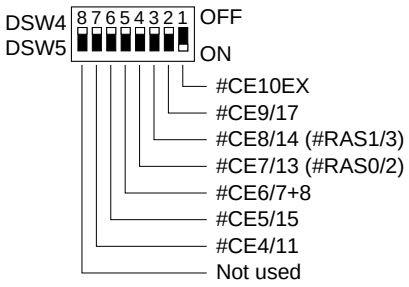
Set DSW3-1 to ON to use emulation RAM as an external ROM. This setting prevents writing by the target program during emulation.

Note: When using the emulation RAM write-protect function, connect the ICD33 EMU pin and the MEM33201 CP4 pin with the supplied clip.
Under these conditions, do not allow the CP4 pin to float. If the pin is floating when the emulation RAM write-protect function is set, write signals in emulation RAM become unstable, destroying RAM contents or preventing data downloads.
This write-protect function is valid for both blocks 0 and 1. It cannot be set for a single block.

DSW3-2, DSW3-3 and DSW3-4 (This setting cannot be changed.)

Be sure to use the default setting.

DSW4 Selection of the area (#CE signal) of emulation RAM block 0
DSW5 Selection of the area (#CE signal) of emulation RAM block 1



DSW4, DSW5

DSW4-1, DSW5-1 (#CE10EX)

OFF: Other than #CE10EX area
ON: **Selects the #CE10EX area** (default).

DSW4-2, DSW5-2 (#CE9/17)

OFF: **Other than #CE9/17 area** (default)
ON: Selects the #CE9/17 area.

DSW4-3, DSW5-3 (#CE8/14)

OFF: **Other than #CE8/14 (#RAS1/#RAS3) area** (default)
ON: Selects the #CE8/14 (#RAS1/#RAS3) area.

DSW4-4, DSW5-4 (#CE7/13)

OFF: **Other than #CE7/13 (#RAS0/#RAS2) area** (default)
ON: Selects the #CE7/13 (#RAS0/#RAS2) area.

DSW4-5, DSW5-5 (#CE6/7+8)

OFF: **Other than #CE6/7+8 area** (default)
ON: Selects the #CE6/7+8 area.

DSW4-6, DSW5-6 (#CE5/15)

OFF: **Other than #CE5/15 area** (default)
ON: Selects the #CE5/15 area.

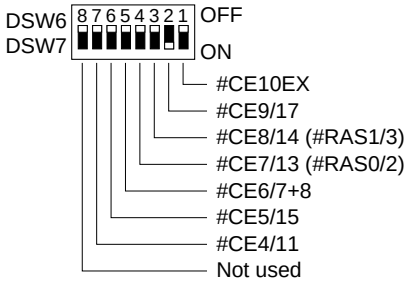
DSW4-7, DSW5-7 (#CE4/11)

OFF: **Other than #CE4/11 area** (default)
ON: Selects the #CE4/11 area.

DSW4-8, DSW5-8 (not used)

Select only a single area with the area selection DIP switches.
If you set all DSW4 switches to OFF, emulation RAM block 0 is set to "not used". If you set all DSW5 switches to OFF, emulation RAM block 1 is set to "not used".
For information on allocating memory, see "MEM33201 Mapping".

DSW6 Selection of the area (#CE signal) of emulation CPLD block 0
DSW7 Selection of the area (#CE signal) of emulation CPLD block 1



DSW6, DSW7

DSW6-1, DSW7-1 (#CE10EX)
OFF: **Other than #CE10EX area** (default)
ON: Selects the #CE10EX area.

DSW6-2, DSW7-2 (#CE9/17)
OFF: Other than #CE9/17 area
ON: **Selects the #CE9/17 area** (default).

DSW6-3, DSW7-3 (#CE8/14)
OFF: **Other than #CE8/14 (#RAS1/#RAS3) area** (default)
ON: Selects the #CE8/14 (#RAS1/#RAS3) area.

DSW6-4, DSW7-4 (#CE7/13)
OFF: **Other than #CE7/13 (#RAS0/#RAS2) area** (default)
ON: Selects the #CE7/13 (#RAS0/#RAS2) area.

DSW6-5, DSW7-5 (#CE6/7+8)
OFF: **Other than #CE6/7+8 area** (default)
ON: Selects the #CE6/7+8 area.

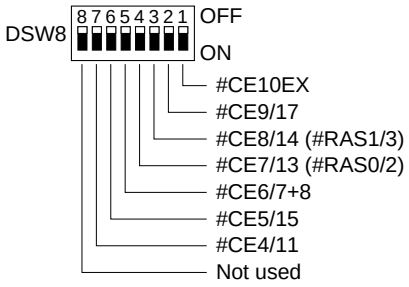
DSW6-6, DSW7-6 (#CE5/15)
OFF: **Other than #CE5/15 area** (default)
ON: Selects the #CE5/15 area.

DSW6-7, DSW7-7 (#CE4/11)
OFF: **Other than #CE4/11 area** (default)
ON: Selects the #CE4/11 area.

DSW6-8, DSW7-8 (not used)

Select only a single area with the area selection DIP switches.
If you set all DSW6 switches to OFF, CPLD block 0 is set to "not used". If you set all DSW7 switches to OFF, CPLD block 1 is set to "not used".
For information on allocating memory, see "MEM33201 Mapping".

DSW8 Selection of the area (#CE signal) of the flash ROM



DSW8

DSW8-1 (#CE10EX)
OFF: **Other than #CE10EX area** (default)
ON: Selects the #CE10EX area.

DSW8-2 (#CE9/17)
OFF: **Other than #CE9/17 area** (default)
ON: Selects the #CE9/17 area.

DSW8-3 (#CE8/14)
OFF: **Other than #CE8/14(#RAS1/#RAS3) area** (default)
ON: Selects the #CE8/14(#RAS1/#RAS3) area.

DSW8-4 (#CE7/13)
OFF: **Other than #CE7/13(#RAS0/#RAS2) area** (default)
ON: Selects the #CE7/13(#RAS0/#RAS2) area.

DSW8-5 (#CE6/7+8)
OFF: **Other than #CE6/7+8 area** (default)
ON: Selects the #CE6/7+8 area.

DSW8-6 (#CE5/15)
OFF: **Other than #CE5/15 area** (default)
ON: Selects the #CE5/15 area.

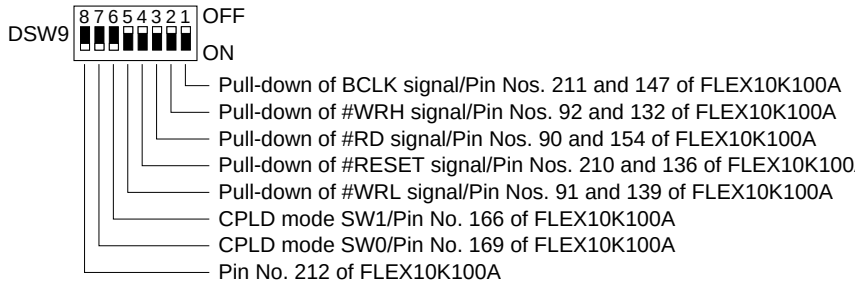
DSW8-7 (#CE4/11)
OFF: **Other than #CE4/11 area** (default)
ON: Selects the #CE4/11 area.

DSW8-8 (not used)

Select only a single area with the selection DIP switches.
If you set all DSW8 switches to OFF, the flash ROM is set to "not used".
For information on allocating memory, see "MEM33201 Mapping".

You may load the flash routine on the debugger (db33) with the "lf" command to delete or write the flash ROM installed in MEM33201. You can also fill, copy, and input data into flash ROM using a memory function for half words.

DSW9 Treatment of FLEX10K100A pin



DSW9

DSW9-1 (Pull-down of BCLK signal/Pin Nos. 211 and 147 of FLEX10K100A)
OFF: **No pull-down resistor** (default)
ON: With pull-down resistor

DSW9-2 (Pull-down of #WRH signal/Pin Nos. 92 and 132 of FLEX10K100A)
OFF: **No pull-down resistor** (default)
ON: With pull-down resistor

DSW9-3 (Pull-down of #RD signal/Pin Nos. 90 and 154 of FLEX10K100A)
OFF: **No pull-down resistor** (default)
ON: With pull-down resistor

DSW9-4 (Pull-down of #RESET signal/Pin Nos. 210 and 136 of FLEX10K100A)
OFF: **No pull-down resistor** (default)
ON: With pull-down resistor

DSW9-5 (Pull-down of #WRL signal/Pin Nos. 91 and 139 of FLEX10K100A)
OFF: **No pull-down resistor** (default)
ON: With pull-down resistor

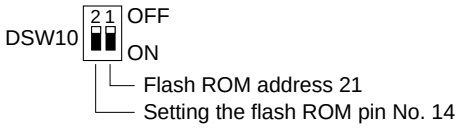
DSW9-6 (CPLD mode SW1/setting of the input level of the pin No. 166 of FLEX10K100A)
OFF: High level input
ON: **Low level input** (default)

DSW9-7 (CPLD mode SW0/setting of the input level of the pin No. 169 of FLEX10K100A)
OFF: High level input
ON: **Low level input** (default)

DSW9-8 (Treatment of the input terminal of FLEX10K100A, pin No. 212)
OFF: No pull-up resistor
ON: **With pull-up resistor** (default)

Note: The pull-down and pull-up resistor values are 10 kΩ.

DSW10 Setting the signal supply to the flash ROM (for supporting 32M bits)



DSW10

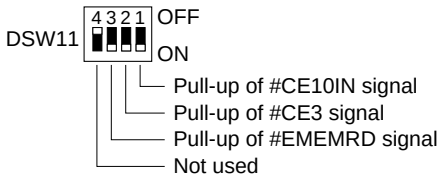
DSW10-1 (Connecting the address 21)

OFF: **Does not connect address 21 to the flash ROM** (default).
ON: Connects address 21 to the flash ROM (32M bits).

DSW10-2 (Setting flash ROM pin No. 14)

OFF: **Pin No. 14 is open** (default).
ON: Uses as XWP / ACC (32M bits).

DSW11 Pull-up of built-in ROM control signal



DSW11

DSW11-1 (Pull-up of #CE10IN signal)

OFF: No pull-up resistor
ON: **With pull-up resistor** (default)

DSW11-2 (Pull-up of #CE3 signal)

OFF: No pull-up resistor
ON: **With pull-up resistor** (default)

DSW11-3 (Pull-up of #EMEMRD signal)

OFF: No pull-up resistor
ON: **With pull-up resistor** (default)

DSW11-4 (Not used)

Note: The pull-up resistance is 10 kΩ.

LEDs

LED1 5V

LED1 lights up when V_{DDE} (I/O voltage: 5 V or 3.3 V) is supplied to the MEM33201.

LED2 3V

LED2 lights up when V_{DD} (core voltage: 3.3 V) is generated on the MEM33201 or supplied from an external power source.

LED3

LED3 lights up when the signal input into the CP4 (TP) pin is high, goes off when the signal is low, and is unstable when the CP4 (TP) pin is open. When you use the emulation ROM write-protect function, the ICE33 EMU signal is input into the CP4 (TP) pin to light the LED.
ON: When the target program is interrupted (reading and writing in emulation RAM possible).
OFF: When the target program is in operation (read-only possible for emulation RAM).

To use the write-protect function, set DSW3-1 to ON.

LED4

LED4 is connected to pin No. 173 of CPLD (FLEX10K100A) and remains on.

Note: If LED4 is not on, CPLD (FLEX10K100A) was set incorrectly by the ROM EPC2 configuration when the power was turned on. Turn the power on again.

If you have modified the CPLD logic, LED4 is on or off, according to the modified user logic.

Test Pins

The MEM33201 comes with the following test pins.

CP1, CP2, CP3 (GND)

These pins are located at the GND (V_{SS}) level of the board.

CP4 (TP)

When using the emulation RAM write-protect function (DSW3-1 on), connect the EMU signal from ICD33 to this pin.

Note: When using the emulation RAM write-protect function, avoid making the CP4 pin float.

CP5 (BREAK)

This pin outputs a forced-break signal to ICD33. When using ICD33 to perform debugging, connect this pin to the ICD33 BRK IN pin with the supplied clip.
This pin outputs a low pulse signal if a break results from a debugger setting from the debug function-extending circuit installed as standard configuration on the MEM33201 CPLD. It is normally in the high-impedance state.
This test pin is connected to pin No. 7 of CPLD (FLEX10K100A).

CP6 (Global input of CPLD)

CP6 is connected to global input pin No. 212 of CPLD (FLEX10K100A) (pulled up at 10 kΩ).

Monitor Pins

You may use the following monitor pins (2.54 mm pitch) to check the status of user-defined pins for the CPLD (FLEX10K100A) and the E0C332XX bus and control signals.
For information on pin arrangement, see "Pin Arrangement".

J2, J4 CPLD user-defined pins (FLEX10K100A)

J5, J6 E0C332XX bus and control signals

You may check the following signals.
Address bus [A23:0], data bus D[15:0]
#CE3, #CE4/11, #CE5/15, #CE6/7+8, #CE7/13(#RAS0/2), #CE8/14(#RAS1/3), #CE9/17, #CE10EX, #CE10IN, #RD, #WRL/#WR/#WE, #WRH/BSH, #HCAS, #LCAS, #EMEMRD, P30/#WAIT/#CE6, P34/#BUSREQ/#CE4+5, P21/#GAAS, P31/#GARD, BCLK

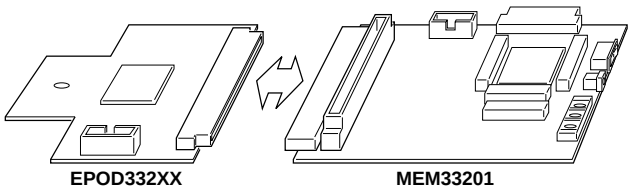
Note: Following input into MEM33201, the address bus [A23:0], data bus D[15:0], #RD, #WRL, and #WRH signals transmit the status after passing a buffer to the monitor pins. These signals delay the time required to pass the buffer (equivalent to 16244/16245, LVTH for 3.3 V and ABT for 5 V) from the E0C332XX output. The EPOD332XX also has signals to pass a buffer. For detailed information, see the EPOD332XX Manual.

Connecting the MEM33201 to an EPOD332XX/User Target Board

Connect the MEM33201 to an EPOD332XX, or directly to a DMT board or user target board by one of the following two methods. To connect a MEM33201 directly to the user target board, you must use the standard interface 100-pin connector and cable.

Direct connection of the EPOD332XX and MEM33201 connector

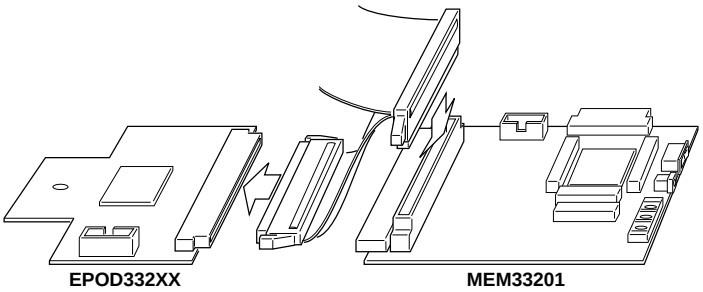
Connect the EPOD332XX J1 connector and the MEM33201 J10 connector (angle connector) directly.



Connecting the EPOD332XX (1)

Flat-cable connection

Connect the EPOD332XX J1 connector and the MEM33201 J11 connector (straight connector) with the supplied 100-pin flat cable.

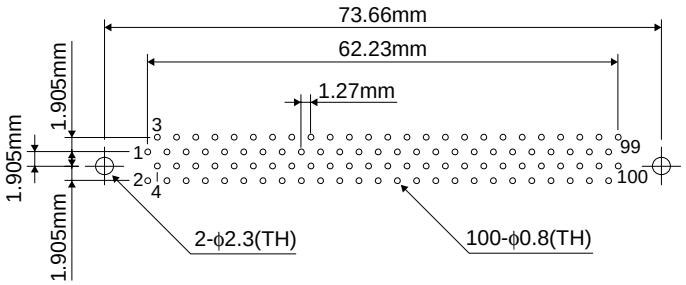


Connecting the EPOD332XX (2)

Direct connection to the user target

If you connect MEM33201 to a user target board that has a CPU without using EPOD332XX, follow one of the two methods given above. You must install a connector identical to that for the EPOD332XX. Use one of the following two connectors.
100-pin straight type: KEL 8830E-100-170S
100-pin right-angle type: KEL 8830E-100-170L

The connector used for the EPOD332XX is the right-angle type.
See the figure below for the on-board connector fixing pin arrangement. Connect the power lines and all signals to these pins. You do not need to connect the #CE10IN, #CE3, and #EMEMRD signals, since they can be pulled up on the MEM33201.

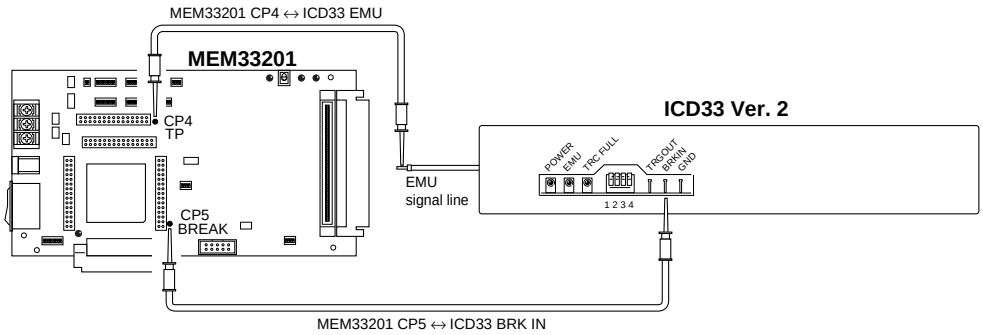


Connector fixing pin arrangement on the user target board

To connect the MEM33201 to the user target with a cable (method (2) given above), use the supplied 100-pin flat cable.

Connection to ICD33

When debugging with the ICD33 basic and trace functions, use the ICD33 connector on the EPOD332XX (or user target) and the cable in the ICD33 package to connect the ICD33.
If you also use the break function of the debug extending circuit installed on the MEM33201 CPLD, connect the MEM33201 CP5 (BREAK) pin and the ICD33 BRK IN pin with the supplied clip.
When using the emulation RAM write-protect function, connect the MEM33201 CP4 (TP) pin and the ICD33 EMU pin with the supplied clip. To use this function, set MEM33201 DSW3-1 to ON. If it is set to OFF (default), read and write functions are always enabled. When DSW3-1 is set to ON, be sure to provide a high or low signal to the CP4 pin to avoid high-impedance state.

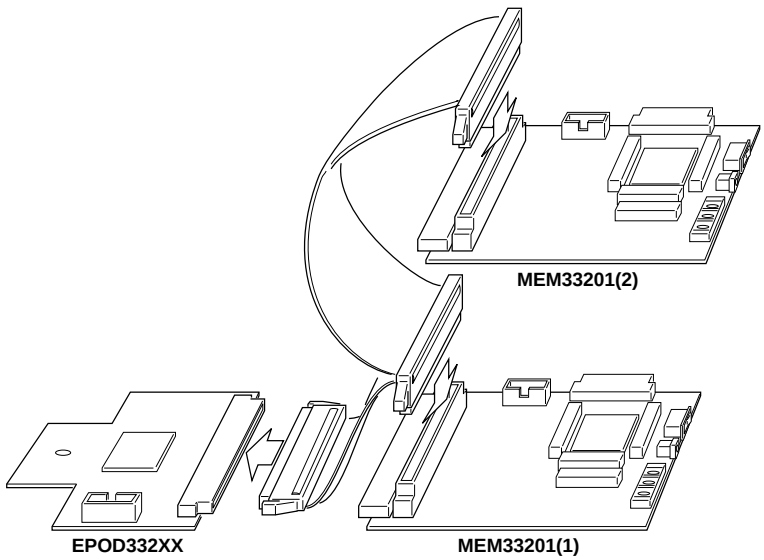


Connection to ICD33

Note: You may use the extended break and write-protect functions for MEM33201 emulation RAM with ICD33 ver. 2 or later, and a E0C33 Family C compiler package of ver. 3 or later.

Cascade-Connecting the MEM33201

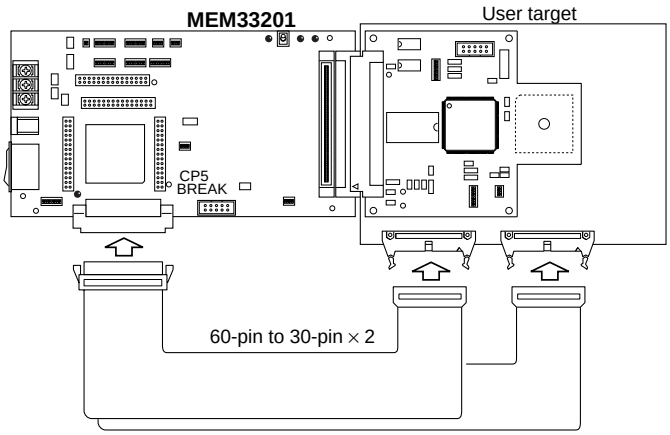
Use the supplied 100-pin flat cable to connect J11 connectors from two MEM33201 boards for a cascade-connection.



Cascade-connection for MEM33201

Connecting the CPLD User Logic Signal

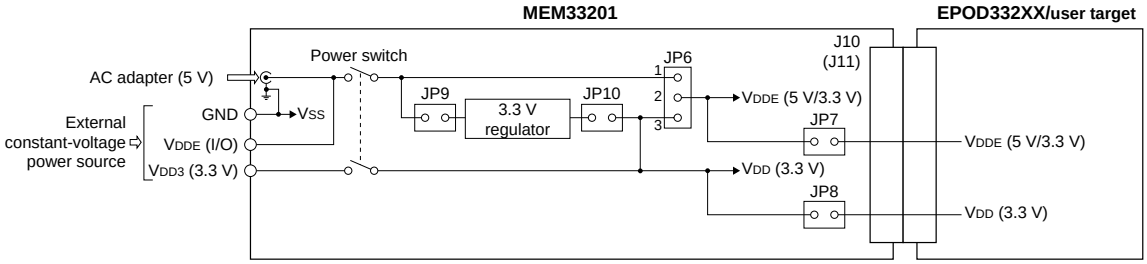
To connect the I/O signal of the user logic defined on CPLD, use the two supplied 30-pin connectors and the 60-pin to 30-pin × 2 flat cable.



Connecting the CPLD user logic signal

Supplying Power

You can supply power to the MEM33201 board directly, or from EPOD332XX/user target side.



Power supply system

Connecting the power source to the MEM33201

Use the supplied AC adapter or a general-purpose 5 V constant-voltage power source.

Supplying power from the AC adapter

Insert the DC plug of the AC adapter (5 V, 2 A) into the DC input jack on MEM33201, and turn on the power switch.
Use the default settings for jumpers J9 and J10 (both set to "1-2 short"). The MEM33201 regulator will generate VDD (with a core voltage of 3.3 V). To set VDDE to 3.3 V (for the MEM33201LV), connect (short-circuit) the pin Nos. 2 and 3 of JP6.

Supplying power from an external constant voltage power source

Connect the VDDE terminals of the power supply terminal (DC2) to a 5 V power source, and turn on the power source.
Use the default settings for jumpers J9 and J10 (both set to "1-2 short"). The MEM33201 regulator will generate VDD (core voltage 3.3 V).
If you set both J9 and J10 to "1-2 open", the voltage of 5 V is not supplied to the 3.3 V regulator, and its output is also cut from the VDD line. If you connect the 3.3 V power source to the VDDE and VDD3 of the power sypply terminal under these conditions, you may operate the MEM33201LV at 3.3 V.

Supplying power from the user target

Set JP7 and JP8 as follows. Power is supplied from the EPOD332XX/user target side through the VDDE and 3VDD pins of the standard interface connector (J10, J11).
JP7: 1-2 short (connection of VDDE)
JP8: 1-2 short (connection of VDD)

At this setting, the MEM33201 power switch is disabled. Turn the user target power source switch on or off to supply or cut power.

Notes:
- *The MEM33201 consumes a current of several hundred milliamperes. If the capacity of the target side power source is inadequate, supply power to MEM33201 directly by the method given above. To do this, set JP7 and JP8 open to release the MEM33201 from the EPOD332XX/user target power source.*
- *Some EPOD332XX products require a specific jumper setting to supply power to MEM33201 from the standard interface connector. For more information, see the EPOD332XX Manual.*

Supplying power from the MEM33201 to an EPOD332XX/user target

To supply power from the MEM33201 to an EPOD332XX/user target, connect the power source to the MEM33201 directly by the method given in "Connecting the power source to the MEM33201". Set JP7 and JP8 as follows.
JP7: 1-2 short (connection of VDDE)
JP8: 1-2 short (connection of VDD)

This method applies only when the capacity of the power source used is adequate and the VDD and VDDE lines of EPOD332XX/user target are not connected to a power source. The only voltages supplied are VDD and VDDE. Supply power separately to the user target for analog signals and other uses.

Power supply to cascade-connected MEM33201 boards

Use the method given in "Supplying power from the MEM33201 to an EPOD332XX/user target" to supply power to the main board of the cascade-connected MEM33201 boards if the VDD and VDDE lines are not connected to a power source, or if these lines can be opened from MEM33201 on EPOD332XX.
If the power sources for the EPOD332XX/user target and MEM33201 sides conflict, set JP7 and JP8 of the MEM33201 to separate the power sources and to supply power to each MEM33201 board independently.

MEM33201 Mapping

Selecting #CE signal

You can access each MEM33201 device block with the following #CE signal, allocated with DIP switches.

1. Emulation RAM block 0 (2MB): DSW4 (default: #CE10EX)
2. Emulation RAM block 1 (2MB): DSW5 (default: #CE10EX)
3. Flash ROM (1MB): DSW8 (default: not used)
4. CPLD block 0: DSW6 (default: #CE9/17)
5. CPLD block 1: DSW7 (default: #CE9/17)

Each switch corresponds to the following #CE signal. Set the switch to ON to select the #CE signal.
DSWx-1: #CE10EX
DSWx-2: #CE9/17
DSWx-3: #CE8/14
DSWx-4: #CE7/13
DSWx-5: #CE6/7+8
DSWx-6: #CE5/15
DSWx-7: #CE4/11
DSWx-8: Not used

Select only one #CE signal.
If you set all switches to OFF, the block will be set as "not used".

Setting emulation RAM addresses

Set the allocated address (address A22 or A21 of the E0C332XX) to each 2MB block of emulation RAM (SRAM) with DSW2.
DSW2-1, DSW2-2: Block 0 starting address
DSW2-3, DSW2-4: Block 1 starting address

Address map of emulation RAM blocks 0 and 1

DSW2-2(4)	DSW2-1(3)	A[22:21]	Accessible address range
OFF	OFF	11	0x#E00000–0x#FFFFFF or 0x#600000–0x#7FFFFF
OFF	ON	10	0x#C00000–0x#DFFFFF or 0x#400000–0x#5FFFFF
ON	OFF	01	0x#A00000–0x#BFFFFF or 0x#200000–0x#3FFFFF
ON	ON	00	0x#800000–0x#9FFFFF or 0x#000000–0x#1FFFFF

(# = 0–F)

Example (Default)

- DSW4-1 = ON (#CE10EX area)
- DSW2-2 = OFF, DSW2-1 = ON

This setting allocates emulation RAM block 0 to the range 0xC00000 to 0x0DFFFFF (2MB).

- DSW5-1 = ON (#CE10EX area)
- DSW2-4 = OFF, DSW2-3 = OFF

This setting allocates emulation RAM block 1 to the range 0x0E00000 to 0x0FFFFFF (2MB).

In this way, the default setting allocates emulation RAM to the E0C33's 4MB external memory boot area (Area 10).

With two MEM33201 boards cascade-connected to provide additional emulation RAM, bus collisions will occur if you set both MEM33201 boards to the same address block of a #CE area. You can circumvent this problem by setting address blocks to make the emulation RAMs continuous. You may create up to 8MB of emulation space.

Precautions

- When you allocate memory to emulation RAM blocks, CPLD blocks, and flash ROM with DIP switches, avoid overlapping areas to prevent bus collisions.
- Avoid overlapping addresses when setting the starting addresses of emulation RAM blocks with DIP switches.
- You can cascade-connect two MEM33201 boards. Set the areas and addresses of the MEM33201 boards to prevent bus collisions.
- The #CE signals and address bus are also connected to the user target side. Avoid any overlapping areas or addresses anywhere in the system.

CPLD (FLEX10K100A)

Note: Please consult the appropriate Altera Corp. manuals for detailed information on Altera Corp. devices and development tools and writing with JTAG.

Overview

The MEM33201 comes with a CPLD for installing user logic and the following related devices.

1) CPLD (EPF10K100ARC240-2) equivalent to 100,000 gates

- Enables downloading of user logic.

2) PLD (EPM7064AE-7)

- PLD for MEM33201 internal circuit control
- Rewriting by user is prohibited

3) Configuration ROM (EPC2LC20)

- Data ROM to set the circuit in the CPLD when the power source switch is turned on
- Rewriting by user is enabled

The configuration ROM comes with extended circuit data to augment the ICD33 debugging function, which performs CPLD configuration when the power is turned on. For information on the expanded debug function, see "Debug Function Extended Circuit".

If you do not use the augmented debug function, you can install a user logic.
CPLD comes with all standard interface signals for the EPOD332XX. You can use these signals to compose an E0C332XX and added gate array system. You can also input and output signals through the user CPLD interface connector, and use MEM33201 as the external ASIC or the prototype 2-in-1 system LSI.

Installing User Logic

Install user logic by one of the following two methods.

(1) Download user logic to the CPLD through JTAG

This method does not require rewriting the configuration ROM, allowing you to keep data for the debug function extended circuit intact. However, you must download user logic data to the CPLD every time you turn on the power.

(2) Write user logic to configuration ROM

If you write user logic to configuration ROM, you do not need to download the data when you turn on the power, since the data is automatically set in the CPLD.

Note: You cannot use configuration ROM as the debug function expanding circuit once you write user logic to it. Whenever possible, we recommend downloading user logic to the CPLD through the JTAG.

You can design user logic programs and create data in the integrated Alter Corp. CPLD development environment (Max-PlusII) as follows.

1. Start Altera Corp. Max-PlusII.
2. Create the user logic project.
3. Register the circuit (Circuit diagram: GDF, language: AHDL, VHDL or Verilog-HDL, entering Wave-Form).
4. Compile to Fitting
   The compiler offers several options, including Device-Option and Global-Logic Synthesis. Select the appropriate device (EPF10K100ARC240-2) and set other options according to the circuit size and operating speed.
   If an error prompt displays the message that arrangement and wiring cannot be performed in the CPLD, reset the Global-Logic Synthesis option. This may clear the error.
5. Floor Plan
   Use the Floor Plan Editor to define pin arrangements.
   Perform pin arrangement and net registration for the EPOD332XX standard interface signals.
6. Simulation/Programmer
   After Compile/Fitting is completed without a user logic data error, download the circuit to the CPLD through JTAG, or write to configuration ROM to check board function. Use the Max-PlusII Function/Timing Simulator to run simulations before actual system deployment.

Notes:
- *If you want to download user logic to the CPLD RAM, download it every time you turn on the power. Otherwise, circuit data written to configuration ROM will be set in the CPLD.*
- *To prevent floating, pins in Altera Corp. devices are set for output if they are undefined for input or output. If the output signal collides with the EPOD332XX standard interface signal, the EPOD332XX and MEM33201 control signals (#CEn, #RD, #WRH/#WRL and bus signals) will not function correctly.*
  For this reason, define the EPOD332XX standard interface signals, even for unused pins.

Given below are some examples of pin definition and user logic programs.

[Template for Verilog-HDL]

The following defines the EPOD332XX standard interface signals.

```
/*************************************************************************
      Standard Interface Signals of MEM33201(LV) (EPF10K100ARC240-2)
*************************************************************************/
//  Module Declaration
module test(
      ic33_bclk,        // c33 BCLK             (Global)    CLK=211
      f_ubclk,          // c33 BCLK
      ic33_xreset,      // c33 xRESET           (Global)    INPUT=210
      f_xreset,         // c33 xRESET
//    igl_in,           // EPF10K100A Input     (Global)    INPUT=212/Future Purpose
      ic33_xrd,         // c33 xRD              (Global)    INPUT=90
      f_xrd,            // c33 xRD
      ic33_xwrh,        // c33 xWRH             (Global)    INPUT=92
      f_xwrh,           // c33 xWRH
      ic33_xwrl,        // c33 xWRL             (Global)    CLK=91
      f_xwrl,           // c33 xWRL
      ic33_xnmi,        // c33 xNMI             (Input  Direction)
      oc33_xnmi,        // c33 xNMI             (Output Direction)
      ic33_xhcas,       // c33 xHCAS
      ic33_xlcas,       // c33 xLCAS
      ic33_addr,        // c33 Address Bus      [23:0]
      ic33_data,        // c33 Data Bus         [15:0]
      ic33_xce3,        // c33 xCE3IN           (for IROM Emulation)
      ic33_xce10in,     // c33 xCE10IN          (for IROM Emulation)
      ic33_xememrd,     // c33 xEMEMRD          (for IROM Emulation)
      ifpga_xce_pld,    // FPGA area select     [1:0] via PLD
      ifpga_xce,        // FPGA area select     [1:0] Direct
      ic33_xce4,        // c33 xCE4/11
      ic33_xce5,        // c33 xCE5/15
      ic33_xce6,        // c33 xCE6/78
      ic33_xras2,       // c33 xCE7/xRAS0/xCE13/xRAS2
      ic33_xras3,       // c33 xCE8/xRAS1/xCE14/xRAS3
      ic33_xce9,        // c33 xCE9/17
      ic33_xce10ex,     // c33 xCE10EX
      ic33_p21,         // c33 P21/xGAAS
      ic33_p31,         // c33 P31/xGARD
      ic33_p30,         // c33 P30/xWAIT
      ic33_p34,         // c33 P34/xCE45
      ifpgamd,          // FPGA Mode            [1:0]
      oled,             // LED Output
// Define additional user I/O.
      oc33_bclk         // c33 BCLK Output
      );
/*************************************************************************
      EPF10K100ARC240-2 Pin & I/O Direction Definitions
*************************************************************************/
// Control
input       ic33_bclk;        // c33 BCLK             (Global) CLK=211
input       f_ubclk;          // c33 BCLK
input       ic33_xreset;      // c33 xRESET           (Global) INPUT=210
input       f_xreset;         // c33 xRESET
// input    igl_in;           // EPF10K100A Input     (Global) INPUT=212/Future Purpose
// Read/Write
input       ic33_xrd;         // c33 xRD              (Global) INPUT=90
input       f_xrd;            // c33 xRD
input       ic33_xwrh;        // c33 xWRH             (Global) INPUT=92
input       f_xwrh;           // c33 xWRH
input       ic33_xwrl;        // c33 xWRL             (Global) CLK=91
input       f_xwrl;           // c33 xWRL
// xNMI Control
input       ic33_xnmi;        // c33 xNMI             (Input  Direction)
output      oc33_xnmi;        // c33 xNMI             (Output Direction)
// DRAM Interface Signals (2CAS)
input       ic33_xhcas;       // c33 xHCAS
input       ic33_xlcas;       // c33 xLCAS
```

```
// c33208 Address and Data Bus
input[23:0]       ic33_addr;        // c33 Address Bus [23:0]
input[15:0]       ic33_data;        // c33 Data Bus    [15:0] Input Setting
//inout[15:0]     ic33_data         // c33 Data Bus    [15:0] Bi-Directional Setting
// c33208 Emulation Memory Control Signals
input             ic33_xce3;        // c33 xCE3IN      (for IROM Emulation)
input             ic33_xce10in;     // c33 xCE10IN     (for IROM Emulation)
input             ic33_xememrd;     // c33 xEMEMRD     (for IROM Emulation)
// FPGA Area Select
input[1:0]        ifpga_xce_pld;    // CPLD area select via PLD
input[1:0]        ifpga_xce;        // CPLD area select Direct
// c33208 Chip Enable Signals
input             ic33_xce4;        // c33 xCE4/11
input             ic33_xce5;        // c33 xCE5/15
input             ic33_xce6;        // c33 xCE6/78
input             ic33_xras2;       // c33 xCE7/xRAS0/xCE13/xRAS2
input             ic33_xras3;       // c33 xCE8/xRAS1/xCE14/xRAS3
input             ic33_xce9;        // c33 xCE9/17
input             ic33_xce10ex;     // c33 xCE10EX
// c33208 Port Extended Functions
input             ic33_p21;         // c33 P21/xGAAS
input             ic33_p31;         // c33 P31/xGARD
input             ic33_p30;         // c33 P30/xWAIT
input             ic33_p34;         // c33 P34/xCE45
input[1:0]        ifpgamd;          // FPGA Mode
output            oled;             // LED Output

// Define additional user I/O.
// Control output
output            oc33_bclk;        // c33208 bclk out

// Reg Declaration
reg               n_div_bclk;
// Wire Declaration
// Port Declaration
// Parameter Declaration
/*****************************************************************************
      Logic Statement
*****************************************************************************/
// c33208 BCLK 1/2 Divider
// Describe user logic here.
// Example of description of the simplest BCLK 1/2 division circuit.
always  @(posedge ic33_bclk or negedge ic33_xreset) begin
        if (!ic33_xreset) begin
            n_div_bclk <= 0;
        end
        else begin
        n_div_bclk <= !n_div_bclk;
        end
end     //always
assign  oc33_bclk = n_div_bclk;

// LED connection port = 1 (always lit)
assign oled = 1;
// xNMI output of CPLD = 1 (inactive)
assign oc33_xnmi = 1;
endmodule
/*****************************************************************************/
```

The following pin arrangement assumes pin allocation on installation of the MEM33201 standard debug function.

```
CHIP "test" ASSIGNED TO AN EPF10K100ARC240-2
                              F10K100A    User I/F
TCK                           : 1
CONF_DONE                     : 2
nCEO                          : 3
TDO                           : 4
VCC                           : 5
oc33_bclk                     : 6      UP1(No. 3)
J2_UP4                        : 7      UP2(No. 4)  //BREAK signal (for ICD33)
```

```
RESERVED                        : 8
RESERVED                        : 9      UP3(No. 5)
GND                             : 10
RESERVED                        : 11
J2_UP4                          : 12     UP4(No. 6)
RESERVED                        : 13     UP5(No. 7)
RESERVED                        : 14
RESERVED                        : 15     UP6(No. 8)   // For internal debugging
VCC                             : 16
RESERVED                        : 17
RESERVED                        : 18     UP7(No. 9)
J2_UP10                         : 19     UP8(No. 10)
RESERVED                        : 20
RESERVED                        : 21     UP9(No. 11)
GND                             : 22
RESERVED                        : 23
RESERVED                        : 24     UP10(No. 12) // Agreement of CE break
RESERVED                        : 25
RESERVED                        : 26
VCC                             : 27
RESERVED                        : 28     UP11(No. 13)
J2_UP12                         : 29     UP12(No. 14)
RESERVED                        : 30
RESERVED                        : 31     UP13(No. 15)
GND                             : 32
RESERVED                        : 33     UP14(No. 16) // Agreement of map break
RESERVED                        : 34
RESERVED                        : 35     UP15(No. 17)
J2_UP16                         : 36     UP16(No. 18)
VCC                             : 37
RESERVED                        : 38
RESERVED                        : 39     UP17(No. 19)
RESERVED                        : 40     UP18(No. 20) // Agreement of bus break
RESERVED                        : 41
GND                             : 42
RESERVED                        : 43     UP19(No. 21)
J2_UP20                         : 44     UP20(No. 22)
RESERVED                        : 45
RESERVED                        : 46     UP21(No. 23)
VCC                             : 47
RESERVED                        : 48     UP22(No. 24) // Agreement of area breaks
RESERVED                        : 49
RESERVED                        : 50     UP23(No. 25)
RESERVED                        : 51     UP24(No. 26)
GND                             : 52
RESERVED                        : 53
RESERVED                        : 54     UP25(No. 27)
RESERVED                        : 55     UP26(No. 28)
RESERVED                        : 56
VCC                             : 57
TMS                             : 58
TRST                            : 59
nSTATUS                         : 60

ic33_data7                      : 61     *
RESERVED                        : 62
ic33_data6                      : 63     *
RESERVED                        : 64
ic33_data5                      : 65     *
RESERVED                        : 66
ic33_data4                      : 67     *
RESERVED                        : 68
GND                             : 69
ic33_data3                      : 70     *
RESERVED                        : 71
ic33_data2                      : 72     *
RESERVED                        : 73
ic33_data1                      : 74     *
RESERVED                        : 75
ic33_data0                      : 76     *
VCC                             : 77
```

```
ifpga_xce_pld0                  : 78     *     // CPLD area select signal(0) through PLD
ifpga_xce_pld1                  : 79     *     // CPLD area select signal(1) through PLD
ic33_xememrd                    : 80
ic33_p34                        : 81     *
ic33_p30                        : 82     *
RESERVED                        : 83
ic33_xhcas                      : 84     *
GND                             : 85
ic33_xlcas                      : 86     *
ic33_xnmi                       : 87     *
ic33_xce3                       : 88     *
VCC                             : 89     *
ic33_xrd                        : 90     *
ic33_xwrl                       : 91     *
ic33_xwrh                       : 92     *
GND                             : 93
ic33_xce10in                    : 94     *
ic33_xce10ex                    : 95     *
VCC                             : 96
ic33_xce9                       : 97     *
ic33_xras3                      : 98     *
ic33_xras2                      : 99     *
ic33_xce6                       : 100    *
ic33_xce5                       : 101    *
ic33_xce4                       : 102    *
oc33_xnmi                       : 103    *
GND                             : 104    *
ic33_addr7                      : 105    *
RESERVED                        : 106
ic33_addr6                      : 107    *
RESERVED                        : 108
ic33_addr5                      : 109    *
RESERVED                        : 110
ic33_addr4                      : 111    *
VCC                             : 112
RESERVED                        : 113
ic33_addr3                      : 114    *
RESERVED                        : 115
ic33_addr2                      : 116    *
RESERVED                        : 117
ic33_addr1                      : 118    *
RESERVED                        : 119
ic33_addr0                      : 120    *

nCONFIG                         : 121
VCC                             : 122
MSEL1                           : 123
MSEL0                           : 124
GND                             : 125
RESERVED                        : 126    UP27(No. 31)
RESERVED                        : 127    UP28(No. 32)
RESERVED                        : 128
RESERVED                        : 129    UP29(No. 33)
VCC                             : 130
RESERVED                        : 131    UP30(No. 34)
f_xwrh                          : 132    *           (xWRH for addition)
RESERVED                        : 133    UP31(No. 35)
RESERVED                        : 134    UP32(No. 36)
GND                             : 135
f_xreset                        : 136    *           (xRESET for addition)
RESERVED                        : 137    UP33(No. 37)
RESERVED                        : 138    UP34(No. 38)
f_xwrl                          : 139    *           (xWRL for addition)
VCC                             : 140
RESERVED                        : 141    UP35(No. 39)
RESERVED                        : 142    UP36(No. 40)
RESERVED                        : 143
RESERVED                        : 144    UP37(No. 41)
GND                             : 145
RESERVED                        : 146    UP38(No. 42)
f_ubclk                         : 147    *           (BCLK for addition)
```

```
RESERVED                        : 148    UP39(No. 43)
RESERVED                        : 149    UP40(No. 44)
VCC                             : 150
RESERVED                        : 151
RESERVED                        : 152    UP41(No. 45)
RESERVED                        : 153    UP42(No. 46)
f_xrd                           : 154    *           (xRD for addition)
GND                             : 155
RESERVED                        : 156    UP43(No. 47)
RESERVED                        : 157    UP44(No. 48)
RESERVED                        : 158
RESERVED                        : 159    UP45(No. 49)
VCC                             : 160
RESERVED                        : 161    UP46(No. 50)
RESERVED                        : 162
RESERVED                        : 163    UP47(No. 51)
ifpga_xce1                      : 164    UP48(No. 52) // CPLD area select signal (1)
                                                      // SW direct
GND                             : 165
ifpgamd1                        : 166    *            // CPLD moder SW1 (DSW9-3)
RESERVED                        : 167    UP49(No. 53)
RESERVED                        : 168    UP50(No. 54)
ifpgamd0                        : 169    *            //CPLD mode SW0 (DSW9-2)
VCC                             : 170
RESERVED                        : 171    UP51(No. 55)
RESERVED                        : 172    UP52(No. 56)
oled                            : 173
RESERVED                        : 174    UP53(No. 57)
ifpga_xce0                      : 175    UP54(No. 58) // CPLD area select signal (0)
                                                      // SW direct
GND                             : 176
TDI                             : 177
nCE                             : 178
DCLK                            : 179
DATA0                           : 180

RESERVED                        : 181
RESERVED                        : 182
RESERVED                        : 183
ic33_addr8                      : 184
RESERVED                        : 185
RESERVED                        : 186
ic33_addr9                      : 187
RESERVED                        : 188
VCC                             : 189
RESERVED                        : 190
ic33_addr10                     : 191
ic33_addr11                     : 192
ic33_addr12                     : 193
ic33_addr13                     : 194
ic33_addr14                     : 195
ic33_addr15                     : 196
GND                             : 197
ic33_addr16                     : 198
ic33_addr17                     : 199
ic33_addr18                     : 200
ic33_addr19                     : 201
RESERVED                        : 202
ic33_addr20                     : 203
RESERVED                        : 204
VCC                             : 205
ic33_addr21                     : 206
RESERVED                        : 207
ic33_addr22                     : 208
RESERVED                        : 209
ic33_xreset                     : 210
ic33_bclk                       : 211
GND                             : 212
RESERVED                        : 213
RESERVED                        : 214
ic33_addr23                     : 215
```

```
GND                             : 216
RESERVED                        : 217
ic33_p21                        : 218
ic33_p31                        : 219
RESERVED                        : 220
ic33_data8                      : 221
RESERVED                        : 222
ic33_data9                      : 223
VCC                             : 224
RESERVED                        : 225
ic33_data10                     : 226
RESERVED                        : 227
ic33_data11                     : 228
RESERVED                        : 229
ic33_data12                     : 230
RESERVED                        : 231
GND                             : 232
ic33_data13                     : 233
ic33_data14                     : 234
RESERVED                        : 235
RESERVED                        : 236
ic33_data15                     : 237
RESERVED                        : 238
RESERVED                        : 239
RESERVED                        : 240
```

Writing User Logic with the JTAG

The MEM33201 comes with Altera Corp. PLD, CPLD, and JTAG connector (J3) for rewriting configuration ROM.
Use the Altera Corp. PL-Byte Blaster MV (3.3 V/5 V) cable for connections and MAX-PlusII for writing.

Notes: • *Use one of the following two methods to configure the CPLD (FLEX10K100A).*
PS (Passive Serial)
JTAG
If you use PL-Byte Blaster MV to configure the MEM33201 CPLD (downloading the circuit to RAM), set and rewrite the circuit with the Multi-Device JTAG Chain.

• *MEM33201 does not support writes with Flex-Chain. Use JTAG to make settings.*

The JTAG chain is set in the Altera Corp. devices on the MEM33201 in the following order. Follow the steps given below to write user logic with MaxPlusII.

1. Select Programmer (writing) from the MaxPlusII menu.
2. JTAG/Multi-Device JTAG Chain Setup

Device Name:	Programming	File Name
1 EPM7064AE	<none>	
2 EPF10K100A	<user logic.sof>	
3 EPC2	<none> or <user logic.pof>	

   If you specify <none>, user logic will not be written to the device. Do not rewrite EPM7064AE data (specify <none>), or the MEM33201 will not function.
   .sof is data to download to the CPLD SRAM.
   .pof is data to write in EEPROM.
3. Main Screen
   • To download the circuit to CPLD RAM, click "Configure".
   • To write data to EPC2, click "Program".

Note: If a "verify error" occurs when writing data to the configuration ROM, try rewriting.
You can write data to configuration ROM up to 100 times. To enable additional writing, replace the configuration ROM (EPC2LC20) on the socket.

Debug Function Extended Circuit

The MEM33201 is shipped with debug function expanding circuit data for the ICD33 in configuration ROM for CPLD.
When you turn on the power, the data configures CPLD to allow execution of the following break functions by the debugger through the ICD33.

Note: Once user logic is written to configuration ROM, you cannot use it as a debug function expanding circuit.

Additional Break Functions

The debug function expanding circuit provides the ICD33 debugging system with the following break functions.

CE break

This function breaks program execution when the specified #CE area is accessed.
You can select two or more #CE areas for this purpose. You can also break program execution when an area where #CE signals are not output is accessed.
You can set read/write access condition for breaking program execution.

Map break

This function breaks program execution if the specified 32KB range in the specified #CE area is accessed (for reading/writing).
You can select two or more #CE and 32KB areas for this purpose. You can also break program execution when an area where #CE signals are not output is accessed.

Bus break

You can set combinations of up to six access conditions against which the execution cycle is compared. Program execution is broken when the conditions are satisfied.You can specify a mask for each comparative condition.
A combination of bus break conditions is given below.

1. #CE signal (you can specify no-#CE access.)
2. Address (24-bit)
3. Data (16-bit or 32-bit*)
4. Read and/or write

* In 16-bit access, you can set up to six combinations of the above conditions. In 32-bit access, you can set up to three combinations of conditions.

For a bus break, you can also specify a sequential break to break program execution only when six (or fewer) specified combinations are satisfied in succession.
A 16-bit counter breaks program execution when break conditions are met for the specified number of times. This counter is common to the six condition combinations. In the sequential break, only the number of hits for the last bus break condition is counted.

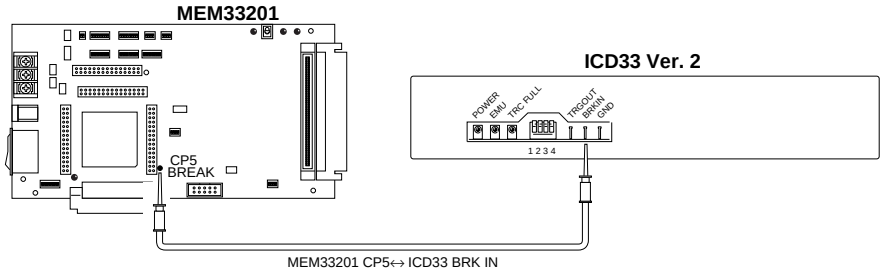
Area break

You can specify a #CE signal and a range of addresses so that program execution is broken when the addresses within or outside the range are accessed.
You can select two or more #CE areas for this purpose. You can also break program execution when an area where #CE signals are not output is accessed.
You can set read/write access condition for breaking program execution.
You can set the area break at two places.

How to Use the Break Function

Connection

When debugging with the ICD33 basic and trace functions, connect the EPOD332XX (or user target) ICD33 connector and the ICD33 using the cable supplied with the ICD33.
If you also use the preceding break functions, connect the MEM33201 CP5 (BREAK) pin and the ICD33 BRK IN pin with the supplied clip.



Connection to ICD33

Note: You can use the MEM33201 expanded break function with ICD33 ver. 2 or later.

Debugging

Use the E0C33 Family debugger db33 to debug programs including break condition settings. For detailed information on db33 usage, see the "E0C33 Family C Compiler Package Manual".

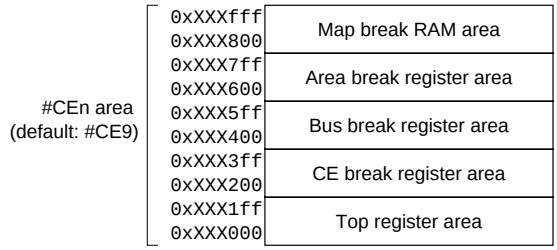
Note: To use the MEM33201 expanded break function, use the db33 included in the E0C33 Family C Compiler Package ver. 3 or later.

Output pins

The CP5 (BREAK) pin connected to the ICD33 BRK IN pin is normally at high impedance, and outputs a low pulse signal when a break occurs. Other J2 monitor pins output the following signals.
Pin No. 4: BREAK signal (same as CP5)
Pin No. 8: Bus cycle signal for internal debugging
Pin No. 12: Agreement of CE breaks (Agreement: H, non-agreement: L)
Pin No. 16: Agreement of map break (Agreement: H, non-agreement: L)
Pin No. 20: Agreement of bus break (Agreement: H, non-agreement: L)
Pin No. 24: Agreement of area break (Agreement: H, non-agreement: L)

Address map

The debug function extended circuit (CPLD) is mapped to the #CE9 area at the default setting. To use #CE9 on the user target, switch CPLD to a different area with DSW6.
Also describe this setting in the debugger parameter file. (Example: ;!MEM33_CE4)
A register dedicated to break setting is allocated at the starting 4KB (at the mirror after the starting 4KB) of each area shown below.



Address map

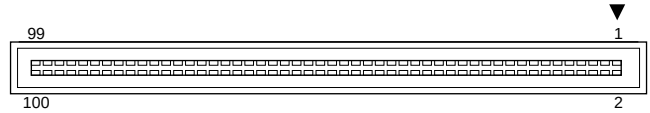
Note: The addresses 0xX00fff and higher are also the mirror of the register area. Do not use the same #CE signal on the user target.

Precautions

- You can use the MEM33201 extended break function only with the db33 included with ICD33 ver. 2 or later and the E0C33 Family C compiler package ver. 3 or later.
- Executing programs actually break at least two or three cycles after the bus cycle that meets the break condition.
- The upper limit of the bus clock frequency for stabilizing the break function is one wait or over, or approximately 33 MHz, depending on the bus load.
  Under the no-wait (read) condition, the decisiveness of a break depends on load conditions. As much as possible, avoid using the no-wait condition.
  Set the number of DRAM CAS cycles at 2CAS or higher. At 1CAS, operations are unstable, just as with no-wait (read) conditions. As much as possible, avoid using 1CAS.
- A break in which #CE is not output tends to start malfunctioning (wrong break occurs) at a bus clock of approximately 30 MHz.
  Under these circumstances, avoid using NO CE break insofar as possible for CE or map breaks. (Specify ;!MEM33_NOCE_DISABLE in the parameter file. The default setting is DISABLE.)
- A state in which #CE is not output indicates that reading or writing is executed when any #CE signal of #CE4 to 9, #CE10EX, #CE10IN, #CE3, P30, or P34 signal is not at low level. P30 and P34 are included in the judgement condition even when they are not set for #CE output. Therefore, NO CE breaks do not occur when they are outputting a low signal as a general-purpose port.
- The bus break data comparison may become comparatively unstable. Mask data comparison to stabilize it.
- Access to map RAM requires an access cycle at the level of 120 ns. Access the map RAM at two waits or over at the bus clock frequency of 25 MHz or less, or at three waits or over at the bus clock frequency of 33 MHz or less.
  Access registers at one wait or over at frequencies of 30 MHz or less, or at two waits at frequencies of 30 MHz or higher. In the debugger, registers are accessed at seven waits.
- If you use the BSL/BSH system (x16 SRAM), mask #WRH (specify ;!MEM33_WRH_MASK in the parameter file).
- If you use DRAM in the #CE7 and 8 areas, be sure to set DRAM (specify ;!MEM33_CE7_DRAM or ;!MEM33_CE8_DRAM in the parameter file). If you do not set DRAM, wrong breaks may occur, even if you do not break in these areas.
- Set the internal delay at "2" (default, 8 ns) (specify ;!MEM33_DELAY 2 in the parameter file).
  If you use DRAM, do not set "0" or "1". With SRAM, performance may improve slightly if you set "0" or "1".
- The comparison of data conditions at DRAM reading supports read timing in high-speed page mode, but not to that in EDO page mode.
- If you use the 32-bit sequential bus break, the next break point will not be recognized unless at least one bus cycle for accessing points other than the break point intervenes between break point accesses.

Pin Arrangement

Standard Interface Connectors (J10, J11)

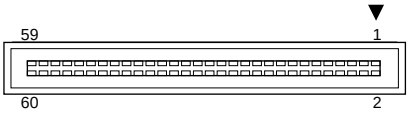


No.	Pin name	No.	Pin name	No.	Pin name	No.	Pin name
1	V_{DDE} (HV_{DD})	26	A19	51	D9	76	#CE4/#CE11/#CE11&12
2	V_{DDE} (HV_{DD})	27	GND	52	GND	77	#CE5/#CE15/#CE15&16
3	A0/#BSL	28	A20	53	D10	78	#CE6/#CE7&8
4	A1	29	A21	54	GND	79	#CE9/#CE17/#CE17&18
5	A2	30	A22	55	D11	80	#CE10EX/#CE9&10EX
6	A3	31	A23	56	GND	81	#CE10IN
7	GND	32	GND	57	D12	82	GND
8	A4	33	D0	58	GND	83	P30/#WAIT/#CE4&5
9	A5	34	GND	59	D13	84	GND
10	A6	35	D1	60	GND	85	P34/#BUSREQ/#CE6
11	A7	36	GND	61	D14	86	GND
12	GND	37	D2	62	GND	87	P21/#DWE/#GAAS
13	A8	38	GND	63	D15	88	P31/#BUSGET/#GARD
14	A9	39	D3	64	GND	89	GND
15	A10	40	GND	65	#RD	90	#CE3
16	A11	41	D4	66	GND	91	#EMEMRD
17	GND	42	GND	67	#WRL/#WR/#WE	92	#URESET ∗1
18	A12	43	D5	68	#WRH/#BSH	93	#RESET ∗2
19	A13	44	GND	69	GND	94	GND
20	A14	45	D6	70	#CE7/#RAS0/#CE13/#RAS2	95	#NMI ∗3
21	A15	46	GND	71	#CE8/#RAS1/#CE14/#RAS3	96	GND
22	GND	47	D7	72	GND	97	BCLK
23	A16	48	GND	73	#HCAS	98	GND
24	A17	49	D8	74	#LCAS	99	V_{DD} (LV_{DD})
25	A18	50	GND	75	GND	100	V_{DD} (LV_{DD})

∗1: Reset signal input from the user target.
∗2: The JP1 setting determines the I/O direction (the default is input).
∗3: #NMI output signal from MEM33201 (may be set for input by the FLEX10K100A terminal setting).

Standard interface connector (J10, J11)

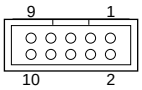
CPLD User Logic I/O Connector (J1)



No.	Pin name	When debug circuit is installed:	No.	Pin name	When debug circuit is installed:
1	VDDE (HVDD)		31	UN2 (N.C.)	
2	VDDE (HVDD)		32	UP28 (10K100A pin 127)	
3	UP1 (10K100A pin 6)		33	UP29 (10K100A pin 129)	
4	UP2 (10K100A pin 7)	BREAK signal (for ICD33)	34	UP30 (10K100A pin 131)	
5	UP3 (10K100A pin 9)		35	UP31 (10K100A pin 133)	
6	UP4 (10K100A pin 12)	(For internal debugging)	36	UP32 (10K100A pin 134)	
7	UP5 (10K100A pin 13)		37	UP33 (10K100A pin 137)	
8	UP6 (10K100A pin 15)	Agreement of CE break	38	UP34 (10K100A pin 138)	
9	UP7 (10K100A pin 18)		39	UP35 (10K100A pin 141)	
10	UP8 (10K100A pin 19)		40	UP36 (10K100A pin 142)	
11	UP9 (10K100A pin 21)		41	UP37 (10K100A pin 144)	
12	UP10 (10K100A pin 24)	Agreement of map break	42	UP38 (10K100A pin 146)	
13	UP11 (10K100A pin 28)		43	UP39 (10K100A pin 148)	
14	UP12 (10K100A pin 29)		44	UP40 (10K100A pin 149)	
15	UP13 (10K100A pin 31)		45	UP41 (10K100A pin 152)	
16	UP14 (10K100A pin 33)	Agreement of bus break	46	UP42 (10K100A pin 153)	
17	UP15 (10K100A pin 35)		47	UP43 (10K100A pin 156)	
18	UP16 (10K100A pin 36)		48	UP44 (10K100A pin 157)	
19	UP17 (10K100A pin 39)		49	UP45 (10K100A pin 159)	
20	UP18 (10K100A pin 40)	Agreement of area break	50	UP46 (10K100A pin 161)	
21	UP19 (10K100A pin 43)		51	UP47 (10K100A pin 163)	
22	UP20 (10K100A pin 44)		52	UP48 (10K100A pin 164)	CPLD block 1 selection signal
23	UP21 (10K100A pin 46)		53	UP49 (10K100A pin 167)	
24	UP22 (10K100A pin 48)		54	UP50 (10K100A pin 168)	
25	UP23 (10K100A pin 50)		55	UP51 (10K100A pin 171)	
26	UP24 (10K100A pin 51)		56	UP52 (10K100A pin 172)	
27	UP25 (10K100A pin 54)		57	UP53 (10K100A pin 174)	
28	UP26 (10K100A pin 55)		58	UP54 (10K100A pin 175)	CPLD block 0 selection signal
29	UP27 (10K100A pin 126)		59	GND (VSS)	
30	UN1 (N.C.)		60	GND (VSS)	

CPLD user logic I/O connector (J1)

JTAG Connector (J3)

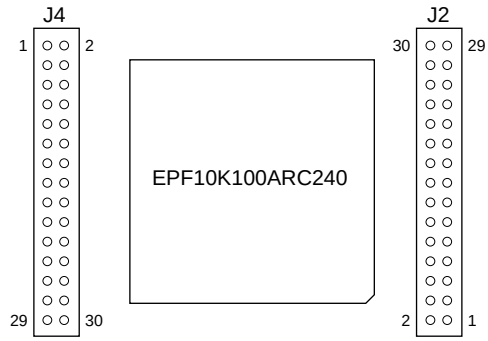


No.	Pin name	No.	Pin name
1	TCK *	6	N.C.
2	GND	7	N.C.
3	TDO	8	N.C.
4	VCC(VDDE)	9	TDI *
5	TMS *	10	GND

* pulled up with 10kΩ

JTAG connector (J3)

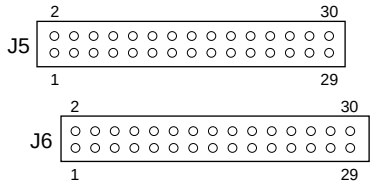
CPLD Monitor Pins (J2, J4)

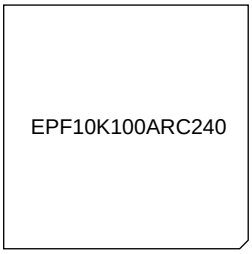


J2			J4		
No.	Pin name	When debug circuit is installed:	No.	Pin name	When debug circuit is installed:
1	VDDE (HVDD)		1	UN2 (N.C.)	
2	VDDE (HVDD)		2	UP28 (10K100A pin 127)	
3	UP1 (10K100A pin 6)		3	UP29 (10K100A pin 129)	
4	UP2 (10K100A pin 7)	BREAK signal (for ICD33)	4	UP30 (10K100A pin 131)	
5	UP3 (10K100A pin 9)		5	UP31 (10K100A pin 133)	
6	UP4 (10K100A pin 12)		6	UP32 (10K100A pin 134)	
7	UP5 (10K100A pin 13)		7	UP33 (10K100A pin 137)	
8	UP6 (10K100A pin 15)	(For internal debugging)	8	UP34 (10K100A pin 138)	
9	UP7 (10K100A pin 18)		9	UP35 (10K100A pin 141)	
10	UP8 (10K100A pin 19)		10	UP36 (10K100A pin 142)	
11	UP9 (10K100A pin 21)		11	UP37 (10K100A pin 144)	
12	UP10 (10K100A pin 24)	Agreement of CE break	12	UP38 (10K100A pin 146)	
13	UP11 (10K100A pin 28)		13	UP39 (10K100A pin 148)	
14	UP12 (10K100A pin 29)		14	UP40 (10K100A pin 149)	
15	UP13 (10K100A pin 31)		15	UP41 (10K100A pin 152)	
16	UP14 (10K100A pin 33)	Agreement of map break	16	UP42 (10K100A pin 153)	
17	UP15 (10K100A pin 35)		17	UP43 (10K100A pin 156)	
18	UP16 (10K100A pin 36)		18	UP44 (10K100A pin 157)	
19	UP17 (10K100A pin 39)		19	UP45 (10K100A pin 159)	
20	UP18 (10K100A pin 40)	Agreement of bus break	20	UP46 (10K100A pin 161)	
21	UP19 (10K100A pin 43)		21	UP47 (10K100A pin 163)	
22	UP20 (10K100A pin 44)		22	UP48 (10K100A pin 164)	CPLD block 1 selection signal
23	UP21 (10K100A pin 46)		23	UP49 (10K100A pin 167)	
24	UP22 (10K100A pin 48)	Agreement of area break	24	UP50 (10K100A pin 168)	
25	UP23 (10K100A pin 50)		25	UP51 (10K100A pin 171)	
26	UP24 (10K100A pin 51)		26	UP52 (10K100A pin 172)	
27	UP25 (10K100A pin 54)		27	UP53 (10K100A pin 174)	
28	UP26 (10K100A pin 55)		28	UP54 (10K100A pin 175)	CPLD block 0 selection signal
29	UP27 (10K100A pin 126)		29	GND (VSS)	
30	UN1 (N.C.)		30	GND (VSS)	

CPLD monitor pins (J2, J4)

E0C33 Bus Monitor Pins (J5, J6)





J5				J6			
No.	Pin name	No.	Pin name	No.	Pin name	No.	Pin name
1	A0/#BSL	16	A15	1	D6	16	#CE10EX/#CE9&10EX
2	A1	17	A16	2	D7	17	#CE10IN
3	A2	18	A17	3	D8	18	#CE3
4	A3	19	A18	4	D9	19	P34/#BUSREQ/#CE6
5	A4	20	A19	5	D10	20	#RD
6	A5	21	A20	6	D11	21	#WRL/#WR/#WE
7	A6	22	A21	7	D12	22	#WRH/#BSH
8	A7	23	A22	8	D13	23	#CE7/#RAS0/#CE13/#RAS2
9	A8	24	A23	9	D14	24	#CE8/#RAS1/#CE14/#RAS3
10	A9	25	D0	10	D15	25	#HCAS
11	A10	26	D1	11	#CE4/#CE11/#CE11&12	26	#LCAS
12	A11	27	D2	12	#CE5/#CE15/#CE15&16	27	#EMEMRD
13	A12	28	D3	13	P30/#WAIT/#CE4&5	28	P21/#DWE/#GAAS
14	A13	29	D4	14	#CE6/#CE7&8	29	P31/#BUSGET/#GARD
15	A14	30	D5	15	#CE9/#CE17/#CE17&18	30	BCLK

Note: Because the address bus [A23:0], data bus D[15:0], #RD, #WRL and #WRH on J5 and J6 are signals that have passed the MEM33201 buffer, they delay the amount of time required to pass the buffer (equivalent to 16244/16245, LVTH for 3.3 V and ABT for 5 V) from actual E0C332XX output.

E0C33 bus monitor pins (J5, J6)

Precautions

Power source

Power switch

The MEM33201 power switch supplies or cuts power from the AC adapter or power supply terminal on the board. If power is supplied from an EPOD332XX or user target, this switch is disabled. When power is supplied to MEM33201, the power LED remains lit.

Power supply to cascade-connected MEM33201 boards

You can supply power from a MEM33201 board to another through the standard interface connector (J10, J11) with J7 and J8 settings. However, this setting also supplies power to the EPOD332XX/user target side. To supply power (V_{DD}, V_{DDE}) to the user target side separately, disconnect the EPOD332XX power line from the MEM33201 boards. Some EPOD332XX products will not permit you to disconnect power lines. For these products, disconnect the power line of the standard interface connector on the MEM33201 and supply power to the MEM33201 boards separately.

Power source capacity

The MEM33201 consumes a current of several hundred milliamperes.
The power source must have a sufficiently large capacity to supply power to the MEM33201 from the target side, or from the MEM33201 to the EPOD332XX/user target side. If the power source capacity is inadequate, supply power separately to the MEM33201 and EPOD332XX/user target.

Separation of power source for the user target side

To supply power separately to the MEM33201 and EPOD332XX/user target, set JP7 (V_{DDE})/JP8 (V_{DD}) open to separate the MEM33201 and EPOD332XX/user target power sources.

3.3 V regulator

To generate the voltage of 3.3 V with the MEM33201 regulator, connect the regulator to the power line using J9 and J10, and supply 5 V from the AC adapter or the V_{DDE} power supply terminal. You cannot generate 3.3 V with the V_{DDE} supplied from the EPOD332XX/user target side.

MEM33201 mapping

Selecting the #CE area

- When you allocate #CE signals to the emulation RAM blocks, CPLD blocks, and flash ROM blocks with DIP switches, do not allocate two or more #CE signals to a single block or different blocks to an area, or a bus collision will occur.
- The #CE signals and address bus are also connected to the user target side. Avoid overlapping areas or addresses anywhere in the system.

Emulation RAM address

- A starting address is set with DIP switches for each of the two emulation RAM blocks. Avoid overlapping addresses.
- For MEM33201 cascade-connections, set areas and addresses to avoid bus collisions. Set address blocks to make emulation RAM continuous. You can allocate two MEM33201 boards to an area to create a maximum emulation space of 8MB.

Standard interface signals to EPOD332XX/user target

#RESET signal

If you set JP1 open, the reset switch on MEM33201 is connected to the #RESET pin of the standard interface connector to make an output signal. Avoid having the xRESET signals on the cascade-connected MEM33201 and EPOD332XX collide with the output #RESET signal.
With the JP1 default setting, the above reset switch is separated and disabled. The MEM33201 also has a simple power-on reset circuit with a CR constant. However, to ensure a reliable reset, input the #RESET signal from the EPOD332XX/user target.

#NMI signal

- If you set the FLEX10K100A #NMI circuit for output, note that it outputs the #NMI signal to the EPOD332XX (user target).
- If you connect the #NMI signal, set the FLEX10K100A terminal correctly for input or output.

Pull-up resistor, pull-down resistor, damper resistor

- A 10 kΩ pull-up/pull-down resistor is connected with the DIP switch setting. Process signals correctly on the user target.

Signal	DIP switch	Default
- P30/#WAIT/#CE6	DSW1-1	No pull-up
- P34/#CE4+5	DSW1-2	No pull-up
- P21/#GAAS	DSW1-3	No pull-up
- P30/#GARD	DSW1-4	No pull-up
- #CE10IN	DSW11-1	With pull-up
- #CE3	DSW11-2	With pull-up
- #EMEMRD	DSW11-3	With pull-up
- BCLK	DSW9-1	No pull-down
- #WRH	DSW9-2	No pull-down
- #RD	DSW9-3	No pull-down
- #WRL	DSW9-5	No pull-down

- A damper resistor (33 Ω) is inserted in series into the standard interface for all signals.

Signal through a buffer

The following signals are supplied to the devices on the MEM33201 through a buffer (equivalent to 7416244/7416245, LVTH for 3.3 V or ABT for 5 V).
A[23:0], D[15.0], #RD, #WRH, #WRL

LEDs

When the MEM33201 is supplied with power and functions normally, LEDs 1 to 4 are lit. If a LED or LEDs fail to light, check the following.

LED1: Is V_{DDE} (I/O voltage, 5 V or 3.3 V) supplied to the MEM33201?

LED2: Is V_{DD} (core voltage 3.3 V) supplied or generated on the MEM33201?

LED3: Does the LED light when the power source switch is turned on again? If not, the MEM33201 may be defective.

LED4: Does the LED light when the power source switch is turned on again? If not, the MEM33201 may be defective.
If you have rewritten the CPLD logic, this LEDs represent the conditions set by the logic.

Dynamic write protection for the emulation RAM

- When using the emulation RAM write-protect function, connect the ICD33 EMU pin and the MEM33201 CP4 pin with the supplied clip.
  Under these conditions, avoid making the CP4 pin float. If the pin floats when the emulation RAM write-protect function is set, write signals for emulation RAM become unstable, destroying the RAM contents or preventing data downloads.
- This write-protection function is valid for both blocks 0 and 1. It cannot be set for a single block.
- You can use this write-protection function with ICD33 ver. 2 or later.

Extended break function (standard specification of CPLD)

- To use the break function (standard specification of CPLD), connect the ICD33 BRK IN pin and the MEM33201 CP5 pin using the supplied clip.
- You can use the MEM33201 extended break function with ICD33 ver. 2 or later.
- You cannot use this break function once you have rewritten CPLD user logic.

CPLD (FLEX10K100A)

Pin definitions

To prevent floating, pins in Altera Corp. devices are set for output if they are undefined either for input or output. If the output signal collides with the EPOD332XX standard interface signal, the EPOD332XX and MEM33201 control signals (#CEn #RD, #WRH/#WRL and bus signals) will not function correctly. For this reason, when user logic is installed, set the EPOD332XX standard interface signal, even for unused pins.

CPLD configuration

- If you want to download user logic to the CPLD RAM, download it every time you turn on the power. Otherwise, circuit data written to configuration ROM will be set in the CPLD.
- Use one of the following two methods to configure the CPLD (FLEX10K100A).
  PS (Passive Serial)
  JTAG
  If you use PL-Byte Blaster MV to configure the MEM33201 CPLD (downloading the circuit to RAM), set and rewrite the circuit with the Multi-Device JTAG Chain.
- MEM33201 does not support writes with Flex-Chain. Use JTAG to make settings.

Configuration ROM (EPC2)

- You cannot use configuration ROM as a debug function expanding circuit once you write user logic to it. Whenever possible, we recommend downloading user logic to the CPLD through the JTAG.
- If a "verify error" occurs when writing data to configuration ROM, try rewriting.
  You can write data to configuration ROM up to 100 times. To enable additional writing, replace the configuration ROM (EPC2LC20) on the socket.

PLD (EPM7064AE)

The JTAG chain is also set in PLD (EPM7064AE). Avoid rewriting data, or MEM33201 will not function. Specify <none>.

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