

SLA35000 Series

High Density Gate Array

- Super-high-density gate array
- Operates on 3.0/3.3/5.0V power sources
- Number of gates: 41 to 162k gates (sea of gates)

DESCRIPTION

The SLA 35000 series are Sea-of-gate type CMOS gate arrays adopting a super-high-density architecture and having a significantly increased number of gates per chip than their equivalent processing equipment. This series are ideal for midsize systems having a relatively small number of I/Os and provide high cost performance.

There are four models ranging from 41,417 to 161,841 gates which can be operated on any power source of 3.0, 3.3 or 5.0V, enabling them to be used in a variety of low-voltage applied fields.

Their demands are approximately 30% smaller ($0.77\mu\text{W/MHz/BC}$ when the internal cell is 3.0V) than those of their equivalent SLA 30000 series. This allows them to be used more easily in high density circuits to be mounted on small packages and employed for various applications such as for image processing and in communication equipment.

To develop high-speed/high-density circuits in a shorter period of time, the series enable diverse design techniques to be employed during development such as high accuracy simulation of wiring resistance and blunted waveform in addition to the conventional wiring capacity components, and provide a new layout tool for reducing clock skew.

FEATURES

- Super-high density (adopting $0.6\mu\text{m}$ silicon gate CMOS with 3-metal layer)
- High-speed operation (operation delay of internal gate = 0.4ns at 3.3V, 2-input power NAND standard)
- Selectable supply voltage: 5.0V, 3.3V, and 3.0V
- Low power consumption ($0.77\mu\text{W/MHz/BC}$ when internal cell = 3.0V)
- Output drivability ($I_{OL} = 1, 4, 8, 12\text{ mA}$ when 5.0V, $I_{OL} = 500\mu, 2, 4, 6\text{ mA}$ when 3.3V)
- On-chip RAM available

PRODUCT LINEUP

Master		SLA3504	SLA3506	SLA3509	SLA3516
Total BCs (Raw Gates)		41,417	64,320	95,760	161,841
Usable Bcs		26,921	38,592	52,668	80,920
Number of PADS		110	130	162	210
Propagation Delay	Internal Gates	tpd = 0.30ns (standard at 5.0V), tpd = 0.40ns (standard at 3.3V)			
	Input Buffers	tpd = 0.48ns (standard at 5.0V), tpd = 0.63ns (standard at 3.3V)			
	Output Buffers	tpd = 2.08ns (standard at 5.0V), tpd = 2.86ns (standard at 3.3V) CL = 50pF			
I/O Level		CMOS, TTL			
Input Mode		TTL, CMOS, Pull-up/Pull-down			
Output Mode		Normal, 3-state, Bi-directional			

ABSOLUTE MAXIMUM RATINGS

 (V_{SS} = 0V)

Item	Symbol	Rating	Unit
Power voltage	V _{DD}	-0.3 to 6.0	V
Input voltage	V _I	-0.3 to V _{DD} +0.5	V
Output voltage	V _O	-0.3 to V _{DD} +0.5	V
Output current/pin	I _{OUT}	±25 (±50*)	mA
Storage temperature	T _{stg}	-65 to 150	°C

*1: For cell of 24mA output current

■ RECOMMENDED OPERATING CONDITION

● Single power supply

Item	Symbol	Min.	Typ.	Max.	Unit
Power voltage	V _{DD}	2.70	3.00	3.30	V
		3.00	3.30	3.60	
		4.75	5.00	5.25	
		4.50	5.00	5.50	
Input voltage	V _I	V _{SS}	–	V _{DD}	V
Operating temperature	T _{opr}	0	25	70	°C
		–40	25	85	°C
Normal input during input rise time	t _{ri}	–	–	50	ns
Normal input during input fall time	t _{fi}	–	–	50	ns
Schmitt input during input rise time	t _{ri}	–	–	5	ms
Schmitt input during input fall time	t _{fi}	–	–	5	ms

■ ELECTRICAL CHARACTERISTICS (V_{DD}=5V)

(V_{DD} = 5V, V_{SS} = 0V, T_a = –40 to 85°C)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit	
Stand-by current *	I _{DDs}	Stop position	–	–	400	μA	
Input leakage current	I _{LI}	–	–1	–	1	μA	
Off-state leakage current	I _{oz}	–	–1	–	1	μA	
High level output voltage	V _{OH}	I _{OH} = –1mA (Type M), –4mA (Type 1), –8mA (Type 2), –12mA (Type 3) V _{DD} = Min.	V _{DD} –4	–	–	V	
Low level output voltage	V _{OL}	I _{OL} = 1mA (Type M), 4mA (Type 1), 8mA (Type 2), 12mA (Type 3) V _{DD} = Min.	–	–	0.4	V	
High level input voltage	V _{IH1}	CMOS level, V _{DD} = Max.	3.5	–	–	V	
Low level input voltage	V _{IL1}	CMOS level, V _{DD} = Min.	–	–	1.0	V	
High level input voltage	V _{T1+}	CMOS Schmitt, V _{DD} = 5.0V	–	–	4.0	V	
Low level input voltage	V _{T1-}	CMOS Schmitt, V _{DD} = 5.0V	0.8	–	–	V	
Hysteresis voltage	V _{H1}	CMOS Schmitt, V _{DD} = 5.0V	0.3	–	–	V	
High level input voltage	V _{IH2}	TTL level, V _{DD} = Max.	2.0	–	–	V	
Low level input voltage	V _{IL2}	TTL level, V _{DD} = Min.	–	–	0.8	V	
High level input voltage	V _{T2+}	TTL Schmitt, V _{DD} = 5.0V	–	–	2.4	V	
Low level input voltage	V _{T2-}	TTL Schmitt, V _{DD} = 5.0V	0.6	–	–	V	
Hysteresis voltage	V _{H2}	TTL Schmitt, V _{DD} = 5.0V	0.1	–	–	V	
Pull-up resistor	R _{PU}	V _I = 0V	Type 1	25	50	100	KΩ
			Type 2	50	100	200	
Pull-down resistor	R _{PD}	V _I = V _{DD}	Type 1	25	50	100	KΩ
			Type 2	50	100	200	
Input pin capacitance	C _I	f = 1MHz, V _{DD} = 0V	–	–	12	pF	
Output pin capacitance	C _O	f = 1MHz, V _{DD} = 0V	–	–	12	pF	
I/O pin capacitance	C _{IO}	f = 1MHz, V _{DD} = 0V	–	–	12	pF	

* Stand by current is a representative value of eresy series

■ ELECTRICAL CHARACTERISTICS (VDD=3V)

(VDD = 3V±0.3V, VSS = 0V, Ta = -40 to 85°C)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit	
Stand-by current*	IDDS	Stop position	–	–	500	µA	
Input leakage current	ILI	–	–1	–	1	µA	
Off-state leakage current	Ioz	–	–1	–	1	µA	
High level output voltage	VOH	IOH = –0.5mA (Type M), –1.8mA (Type 1), –3.5mA (Type 2), –5mA (Type 3) VDD = Min.	VDD –0.3	–	–	V	
Low level output voltage	VOL	IOL = 0.5mA (Type M), 1.8mA (Type 1), 3.5mA (Type 2), 5mA (Type 3) VDD = Min.	–	–	0.3	V	
High level input voltage	VIH1	CMOS level, VDD = Max.	2.0	–	–	V	
Low level input voltage	VIL1	CMOS level, VDD = Min.	–	–	0.8	V	
High level input voltage	VT1+	CMOS Schmitt, VDD = 3.0V	–	–	2.3	V	
Low level input voltage	VT1-	CMOS Schmitt, VDD = 3.0V	0.5	–	–	V	
Hysteresis voltage	VH1	CMOS Schmitt, VDD = 3.0V	0.1	–	–	V	
Pull-up resistor	RPU	Vi = 0V	Type 1	50	100	200	KΩ
			Type 2	100	200	400	
Pull-down resistor	RPD	Vo = VDD	Type 1	50	100	200	KΩ
			Type 2	100	200	400	
Input pin capacitance	CI	f = 1MHz, VDD = 0V	–	–	12	pF	
Output pin capacitance	CO	f = 1MHz, VDD = 0V	–	–	12	pF	
I/O pin capacitance	CIO	f = 1MHz, VDD = 0V	–	–	12	pF	

* Stand by current is a representative value of eryl series

■ ELECTRICAL CHARACTERISTICS (VDD=3.3V)

(VDD = 3.3V±0.3V, VSS = 0V, Ta = -40 to 85°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	
Stand-by current*	IDDS	Stop position	–	–	500	µA	
Input leakage current	ILI	–	–1	–	1	µA	
Off-state leakage current	Ioz	–	–1	–	1	µA	
High level output voltage	VOH	IOH = –0.5mA (Type M), –2mA (Type 1), –4mA (Type 2), –6mA (Type 3) VDD = Min.	VDD –0.3	–	–	V	
Low level output voltage	VOL	IOL = 0.5mA (Type M), 2mA (Type 1), 4mA (Type 2), 6mA (Type 3) VDD = Min.	–	–	0.3	V	
High level input voltage	VIH1	CMOS level, VDD = Max.	2.2	–	–	V	
Low level input voltage	VIL1	CMOS level, VDD = Min.	–	–	0.8	V	
High level input voltage	VT1+	CMOS Schmitt, VDD = 3.3V	–	–	2.4	V	
Low level input voltage	VT1-	CMOS Schmitt, VDD = 3.3V	0.6	–	–	V	
Hysteresis voltage	VH1	CMOS Schmitt, VDD = 3.3V	0.1	–	–	V	
Pull-up resistor	RPU	Vi = 0V	Type 1	45	90	180	KΩ
			Type 2	90	180	360	
Pull-down resistor	RPD	Vi = VDD	Type 1	45	90	180	KΩ
			Type 2	90	180	360	
Input pin capacitance	CI	f = 1MHz, VDD = 0V	–	–	12	pF	
Output pin capacitance	CO	f = 1MHz, VDD = 0V	–	–	12	pF	
I/O pin capacitance	CIO	f = 1MHz, VDD = 0V	–	–	12	pF	

* Stand by current is a representative value of eryl series

■ PERFORMANCE CURVES (VDD=5V)

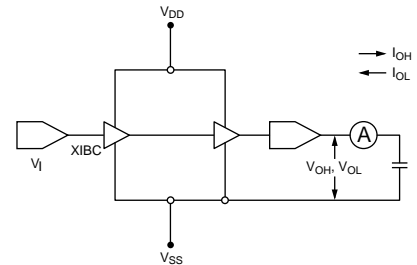
● Output Current Characteristics (5.0V±10%)

TYPE number	Output current	
	I _{OH} (mA)	I _{OL} (mA)
TYPE M	-1	1
TYPE 1	-4	4
TYPE 2	-8	8
TYPE 3	-12	12

The alphanumeric of the **TYPE*** (M, 1-3) indicate the output cell names (xx * x).

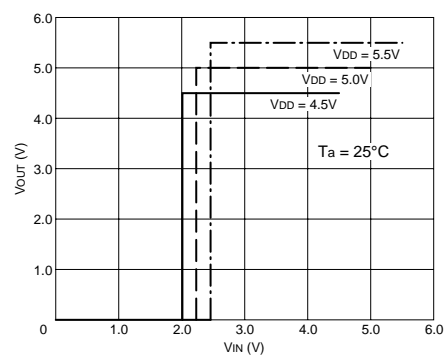
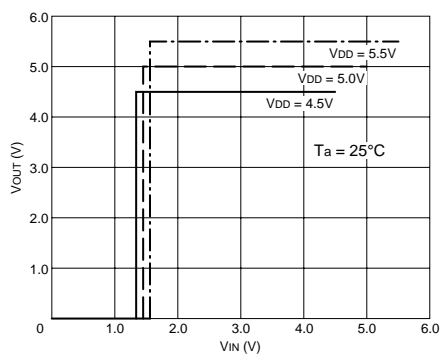
Example: XUO3 Å® Indicates TYPE3

● Measurement Circuit

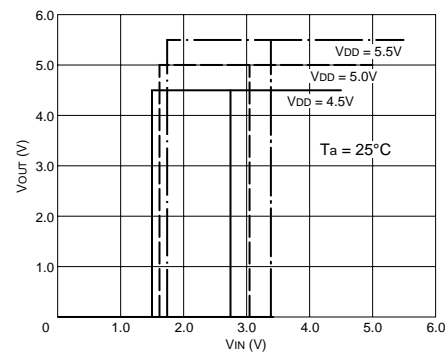
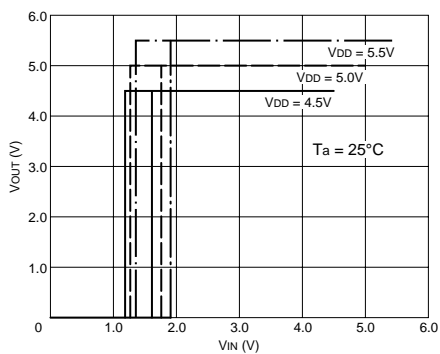


● Output Buffer Characteristics (5V±10%)

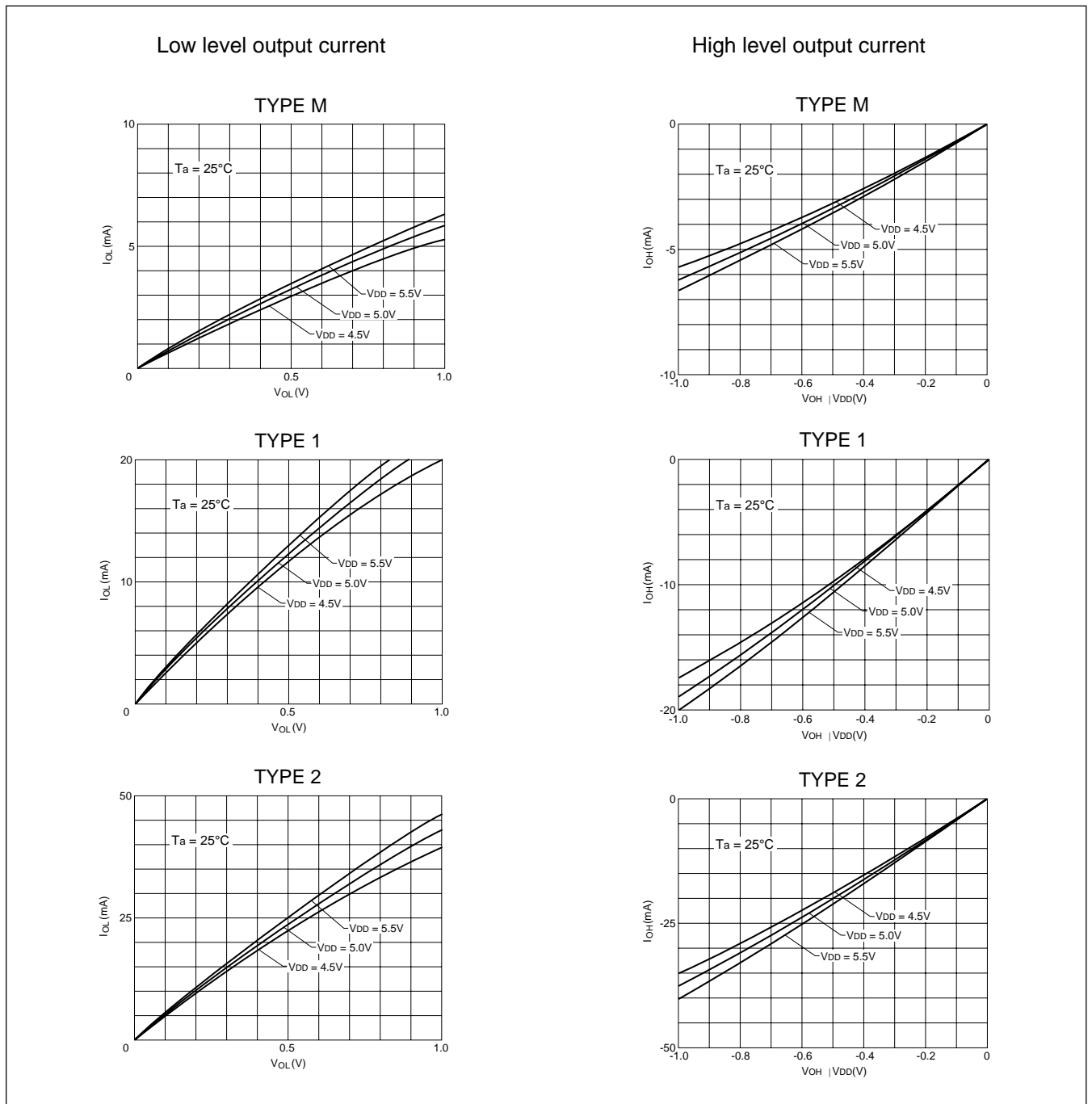
Standard Type



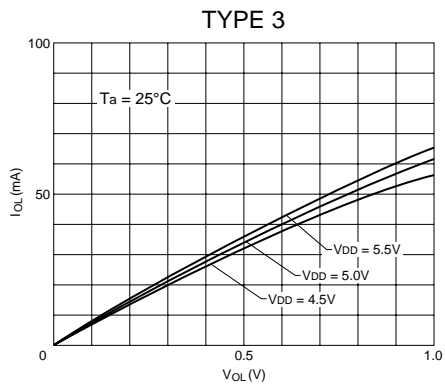
Schmitt – Trigger cell



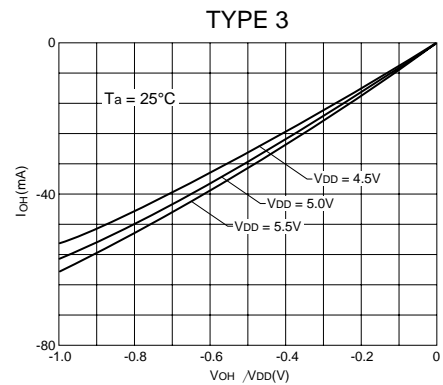
● Output Driver Characteristics



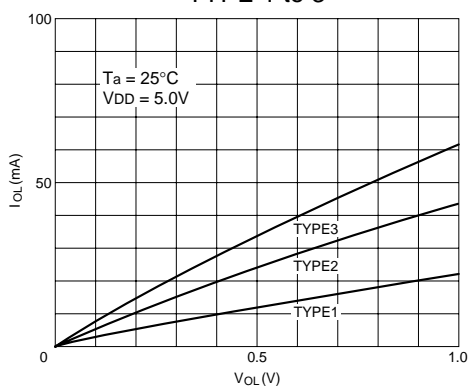
Low level output current



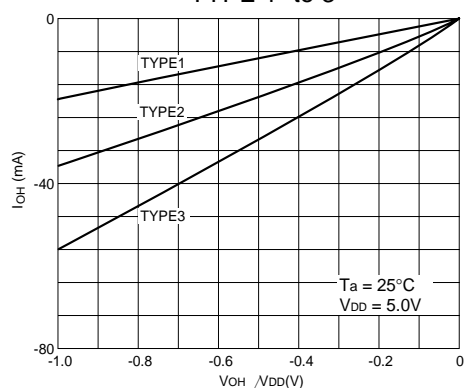
High level output current



TYPE 1 to 3

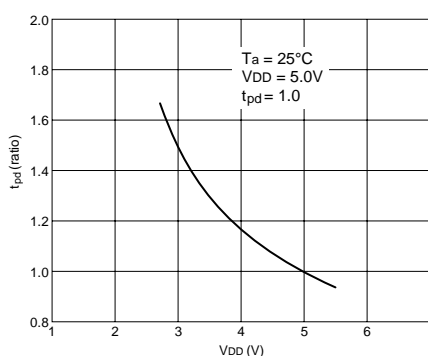


TYPE 1 to 3

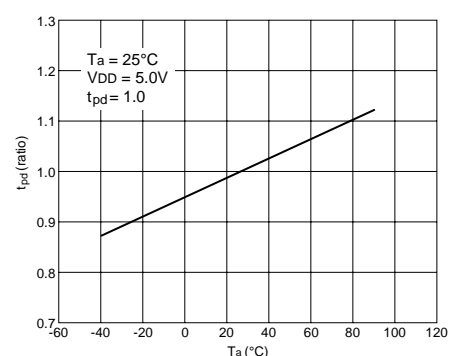


● Delay Characteristics

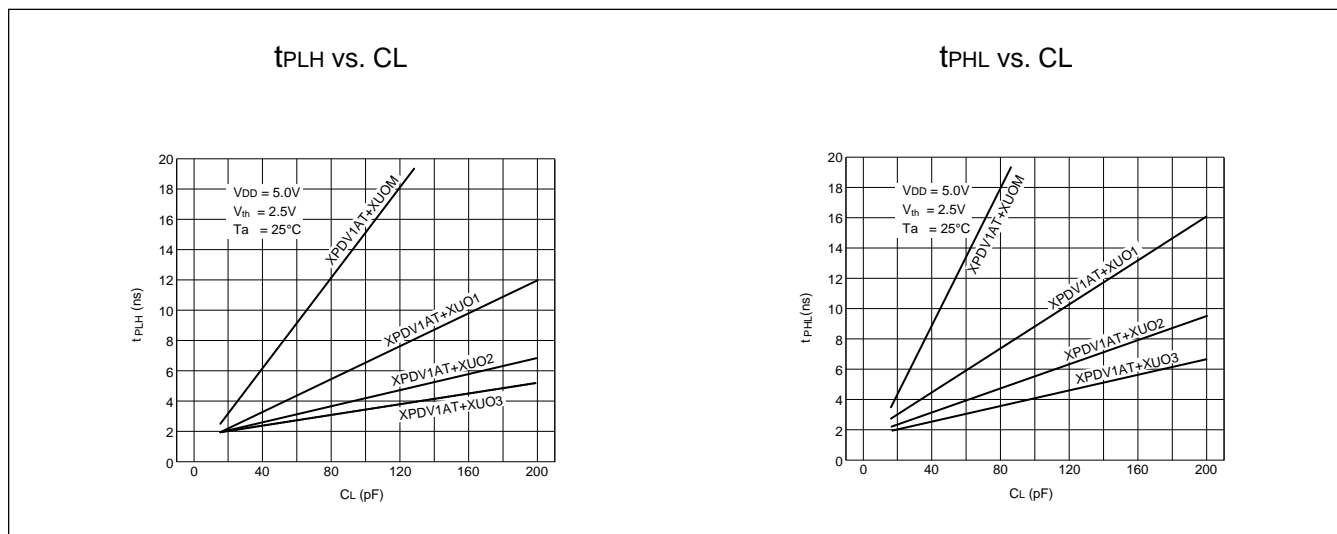
t_{pd} vs. V_{DD}



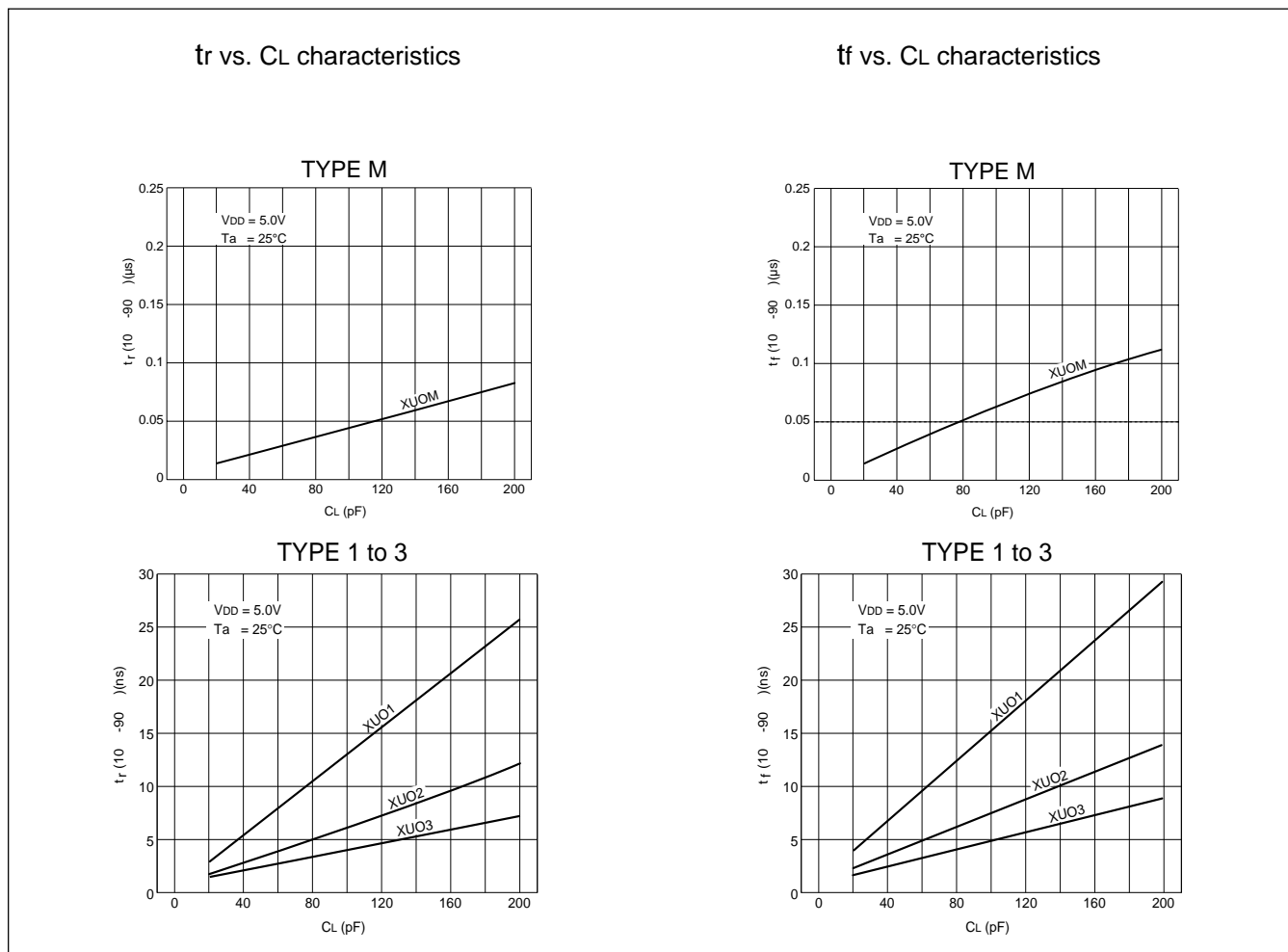
t_{pd} vs. T_a



● Output delay time vs. CL



● Output Buffer tr, tf vs. CL



■ PERFORMANCE CURVES (VDD=3.3V)

● Output Current Characteristics (3.3V±0.3V)

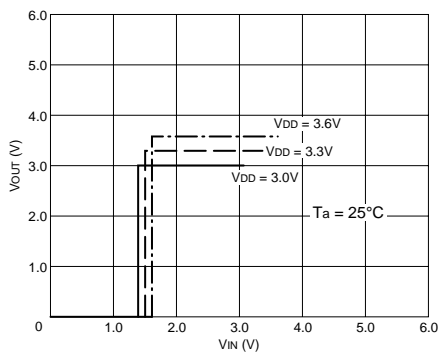
TYPE number	Output current	
	I _{OH} (mA)	I _{OL} (mA)
TYPE M	-0.5	0.5
TYPE 1	-2	2
TYPE 2	-4	4
TYPE 3	-6	6

The alphanumeric of the *TYPE** (M, 1-3) indicate the output cell names (xx * x).

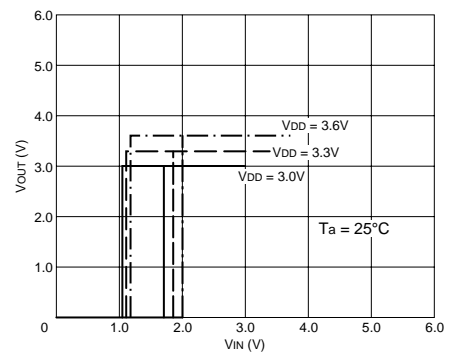
Example: XUO3 Å® Indicates TYPE3

● Output Buffer Characteristics (3.3V±0.3V)

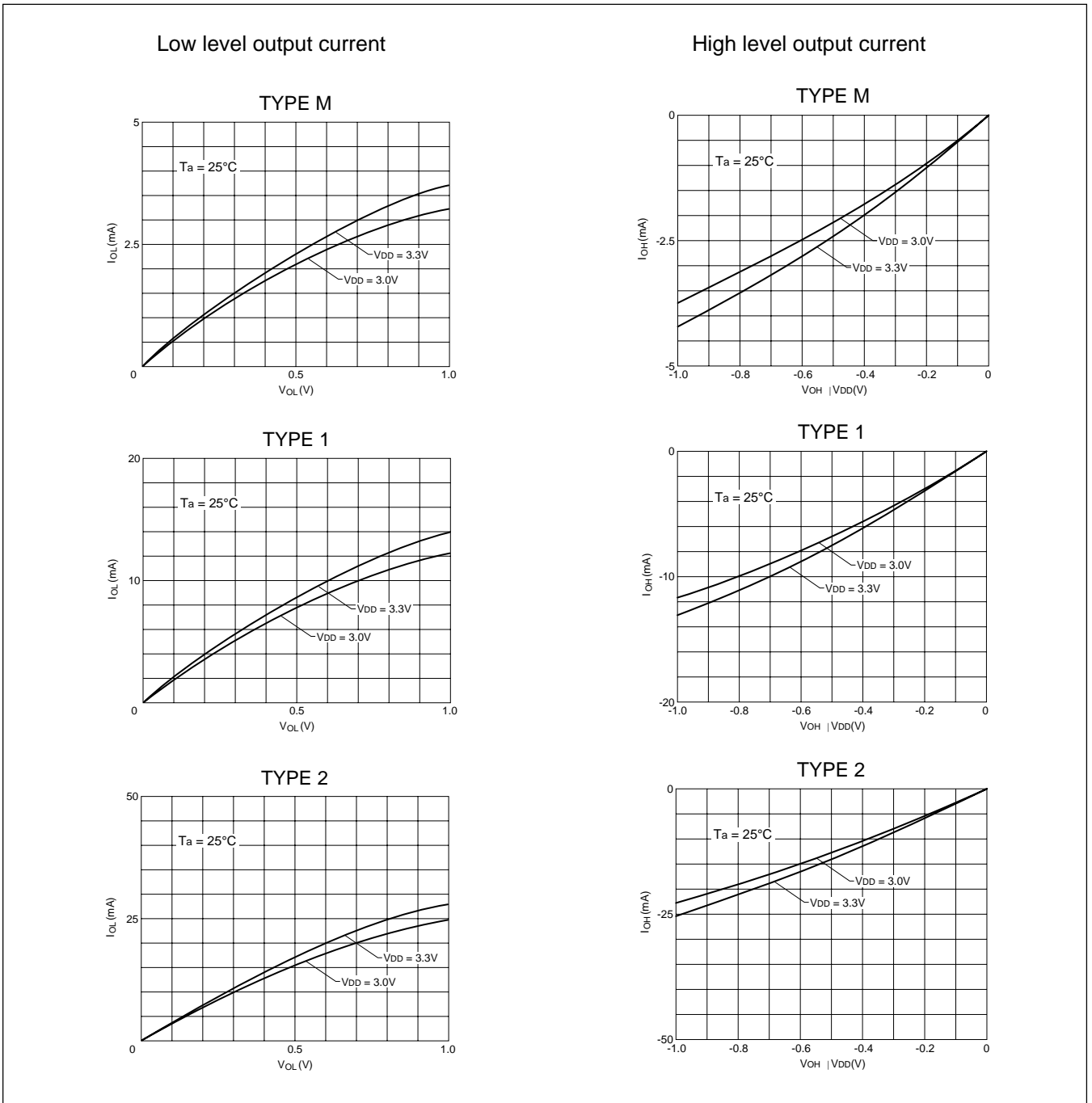
Standard Type



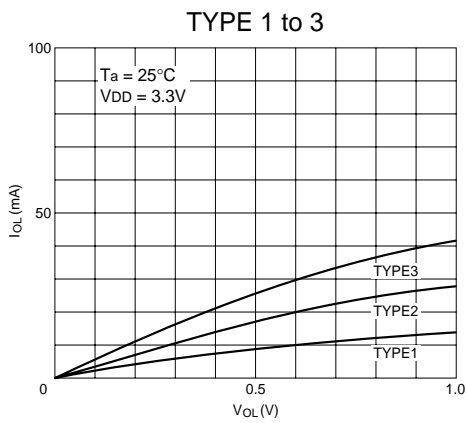
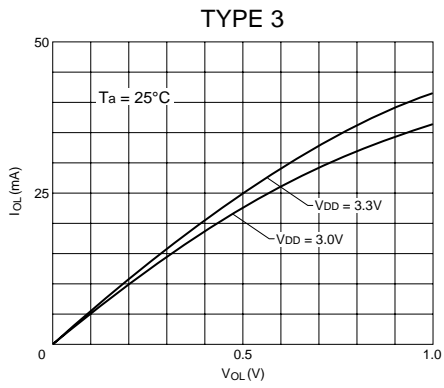
Schmitt-Trigger cell



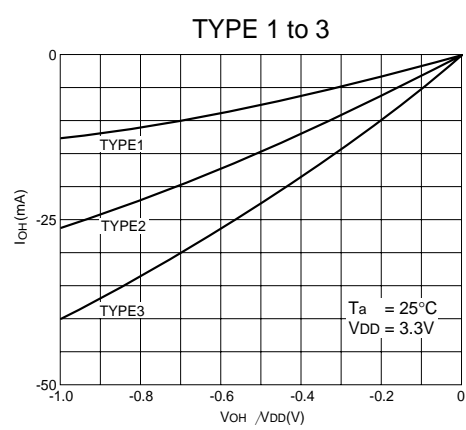
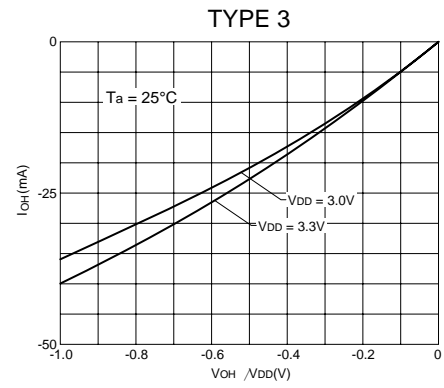
● Output Driver Characteristics



Low level output current

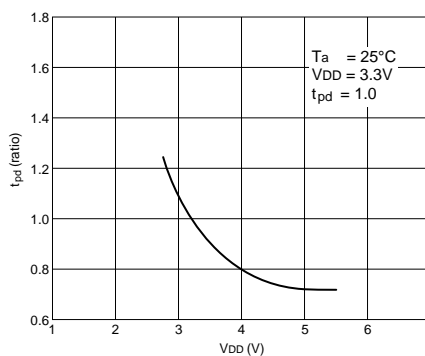


High level output current

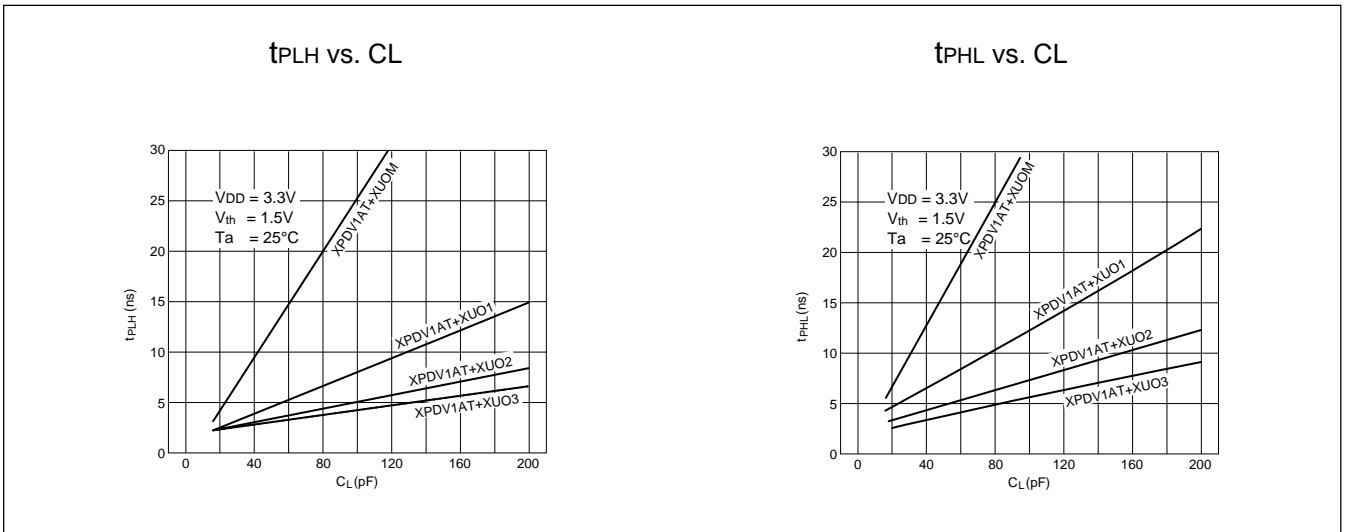


● Delay Characteristics

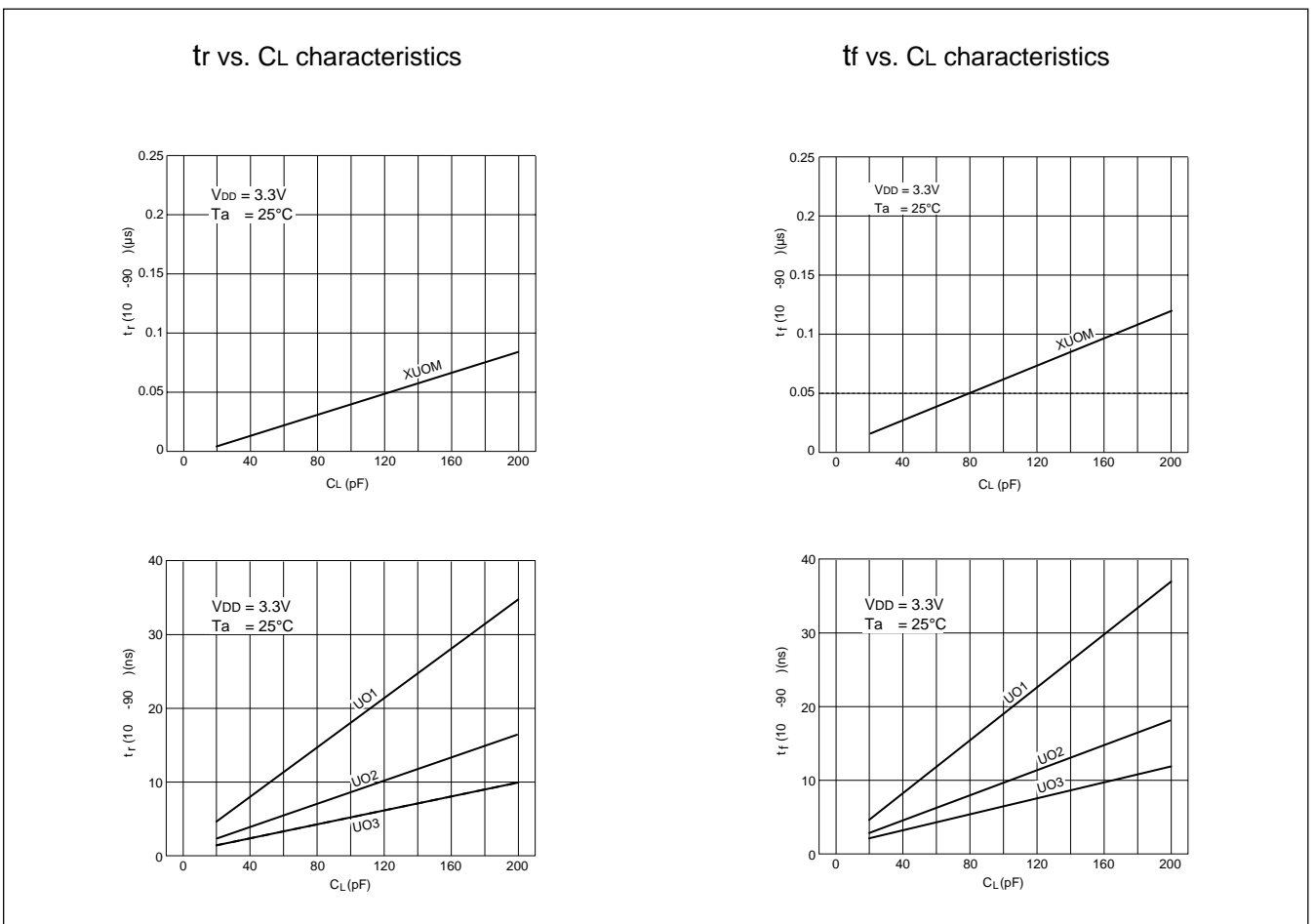
t_{pd} vs. V_{DD}



● Output delay time vs. CL



● Output Buffer tr, tf vs. CL



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