Preliminary

EPSON

SLA60000 Series

High Speed Gate Array

0.25um CMOS Gate Array
Low power consumption
Covered from 99k to 2,519k raw gates

DESCRIPTION

The SLA60000 Series are CMOS Gate Arrays which are adopting on 0.25um silicon gate process with 3 and 4-metal layers. There are 10 arrays which are covering from 98,892 to 2,588,040 raw gate for immediate applications to large scale and high speed systems.

FEATURES

- Adopting on 0.25um CMOS silicon gate with 3 and 4 metal layers
- 10 arrays covered with 98,892 to 2,588,040 gates
- 2.5V single power supply or 2.5/3.3V dual power supply operation
- 56ps propagation delay at 2.5V - 2 input NAND gate, F/O=1, Typical
- Low power consumption - 0.17uW/BC/MHz at 2.5V, F/O=1
- Input / Output Level - CMOS, LVTTL, Schmitt, PCI, LVDS*
- ? Output drive ability - I_{OL}=0.1 / 1 / 3 / 8 / 12 / 24mA at HV_{DD}=3.3V, LV_{DD}=2.5V
- ? SRAM, ROM, Flash and various function cells are available

*Planning

PRODUCT LINEUP - Planning

Master		SLA6009	SLA6017	SLA6028	SLA6040	SLA6059	SLA6083	SLA6123*	SLA6158*	SLA6190*	SLA6251*
Total BC (Raw gates)		99,200	171,720	284,394	400,290	595,362	831,572	1,234,820	1,587,754	1,902,960	2,519,604
Usable BC	3LM	79,376	137,376	199,076	280,203	416,753	540,522	802,633	1,032,040	1,141,776	1,511,762
	4LM	89,298	154,548	241,735	340,247	506,058	665,258	987,856	1,270,203	1,427,220	1,889,703
number of PAD	80um	(104)	(132)	(168)	(200)	(240)	284	344	388	424	488
	70um	112	148	188	224	272	(320)	(388)	(440)	(480)	(552)
Delay	Internal	tpd = 56ps (2 input NAND gate, 2.5V, Typical)									
	Input	tpd = 270ps (2.5V, F/O=2, Typical)									
	Output	tpd = 1600ps (2.5V, CL = 15pF, Typical)									
I/O Level		CMOS, LVTTL, PCI3.3V, LVDS*									
Input Mode		Normal, Pull-up/Pull down, Schmitt, level shifter, Fail-safe*, Gated*									
Output Mode		Normal, Open drain, 3-state, Bi-directional, Level shifter, Fail-safe*, Gated*									

*Planning