EPSON

E0C332128/264

32-bit Single Chip Microcomputer

Preliminary

- High-speed 32-bit RISC Core
- Multiply Accumulation
- 10-bit ADC
- Built-in RAM
- High-speed DMA, Intelligent DMA
- Twin-clock Oscillator

■ DESCRIPTION

The E0C332128/264 is a CMOS 32-bit microcomputer composed of a CMOS 32-bit RISC core, ROM, RAM, DMA, timers, SIO, PLL and other circuits. The E0C332128/264 can be operated with high speed and spend little current. With the ADC, PWM and the MAC function, the E0C332128/264 is suitable for voice applications, PDAs and OA products such as printers.

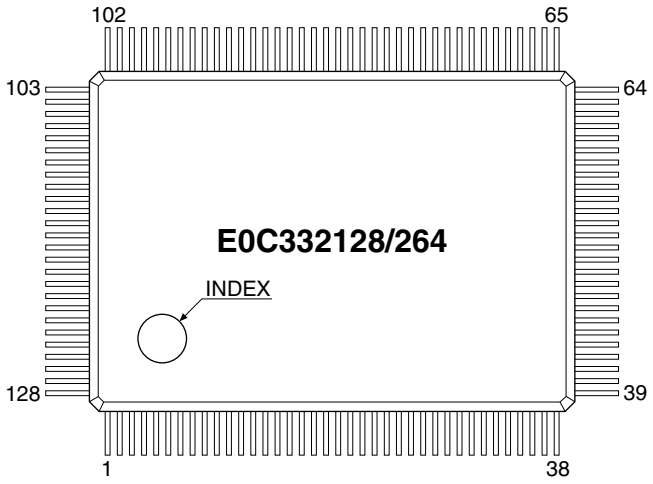
■ FEATURES

- CMOS LSI 32-bit parallel processing ..... E0C33000 RISC core
- Main clock ..... 50MHz (Max., up to 12.5MHz external clock input)
- Sub clock ..... 32.768kHz (Typ., crystal)
- Instruction set ..... 16-bit fixed length, 105 instructions
  (MAC instruction is included, 2 cycles)
- Internal RAM size ..... 8,192 bytes
- Internal ROM size ..... 131,072 bytes (E0C332128), 65,536 bytes (E0C33264)
- Clock timer ..... 1 channel
- Programmable timer ..... 8 bits × 4 channels and 16 bits × 6 channels
- PWM timer ..... Realized with a 16-bit programmable timer
- Watchdog timer ..... Realized with a 16-bit programmable timer
- Serial interface ..... 2 channels
  Clock synchronization type and asynchronization type are selectable. Usable as an infrared ray (IrDA) interface.
- 10-bit A/D converter ..... Successive approximation type, 8 input channels
- High-speed DMA ..... 4 channels
- Intelligent DMA ..... 128 channels
- I/O port ..... Input port : 13 bits
  I/O port : 29 bits
  Pins are shared with the inputs and outputs of built-in peripheral circuits.
- Interrupt controller ..... External interrupts : 10 types
  Internal interrupts : 29 types
- External bus interface ..... 24-bit address bus, 16-bit data bus, 7 chip enable pins
  DRAM and burst ROM may be connected directly.
- Shipping form QFP5-128pin
- Supply voltage ..... Core voltage : 1.8 to 3.6V
  I/O voltage : 1.8 to 5.5V
- Power consumption ..... HALT state : TBD (3.3V, 32.768kHz)
  RUN state : TBD (3.3V, 50MHz)

∗ This model is under development, therefore the contents of the above specifications may be revised at final.

■ PIN LAYOUT

QFP5-128pin



No.	Pin name	No.	Pin name	No.	Pin name	No.	Pin name
1	P24/TM2	33	K65/AD5	65	#RESET	97	A16
2	VSS	34	K50/#DMAREQ0	66	#NMI	98	ICEMD
3	P25/TM3	35	K64/AD4	67	A0/#BSL	99	A17
4	P26/TM4	36	K63/AD3	68	A1	100	A18
5	P15/EXCL4/#DMAEND0	37	K62/AD2	69	P34/#BUSREQ/#CE6	101	A19
6	P27/TM5	38	AVDDE	70	VSS	102	P04/SIN1/#DMAACK2
7	BCLK	39	K61/AD1	71	A2	103	P05/SOUT1/#DMAEND2
8	P00/SIN0	40	K60/AD0	72	A3	104	P06/#SCLK1/DMAACK3
9	P01/SOUT0	41	D6	73	A4	105	VSS
10	D15	42	VSS	74	A5	106	PLLC
11	VDD	43	D5	75	A6	107	VSS
12	P03/#SRDY0	44	D4	76	#CE10IN	108	PLLS1
13	D14	45	D3	77	VDD	109	PLLS0
14	P31/#BUSGET/#GARD	46	D2	78	#EMEMRD	110	P07/#SRDY1/#DMAEND3
15	D13	47	D1	79	A7	111	#X2SPD
16	P32/#DMAACK0	48	D0	80	#HCAS	112	EA10MD0
17	D12	49	P35/#BUSACK	81	A8	113	EA10MD1
18	P33/#DMAACK1	50	VDDE	82	#LCAS	114	VDD
19	D11	51	#CE9/#CE17	83	A9	115	N.C.
20	K54/#DMAREQ3	52	OSC2	84	P16/EXCL5/#DMAEND1	116	OSC4
21	D10	53	#CE7/#RAS0/#CE13/#RAS2	85	A10	117	P20/#DRD
22	K53/#DMAREQ2	54	OSC1	86	A20	118	OSC3
23	D9	55	#CE6	87	A11	119	P21/#DWE/#GAAS
24	K52/#ADTRG	56	#RD	88	A21	120	#CE3
25	VSS	57	VSS	89	A12	121	P22/TM0
26	K51/#DMAREQ1	58	#WRL/#WR/#WE	90	A22	122	P23/TM1
27	P02/#SCLK0	59	#WRH/#BSH	91	A13	123	DSIO
28	D8	60	#CE10EX	92	A23	124	P10/EXCL0/T8UF0/DST0
29	D7	61	#CE8/#RAS1/#CE14/#RAS3	93	VSS	125	P11/EXCL1/T8UF1/DST1
30	VDDE	62	#CE5/#CE15	94	A14	126	P12/EXCL2/T8UF2/DST2
31	K67/AD7	63	#CE4/#CE11	95	A15	127	P13/EXCL3/T8UF3/DPCO
32	K66/AD6	64	P30/#WAIT/#CE4&5	96	VDDE	128	P14/FOSC1/DCLK