EPSON

Micro MINI E0C6008

4-bit Single Chip Microcomputer

Low Voltage Operation Products

- E0C6200C Core CPU
- Built-in LCD Driver
- Serial Interface

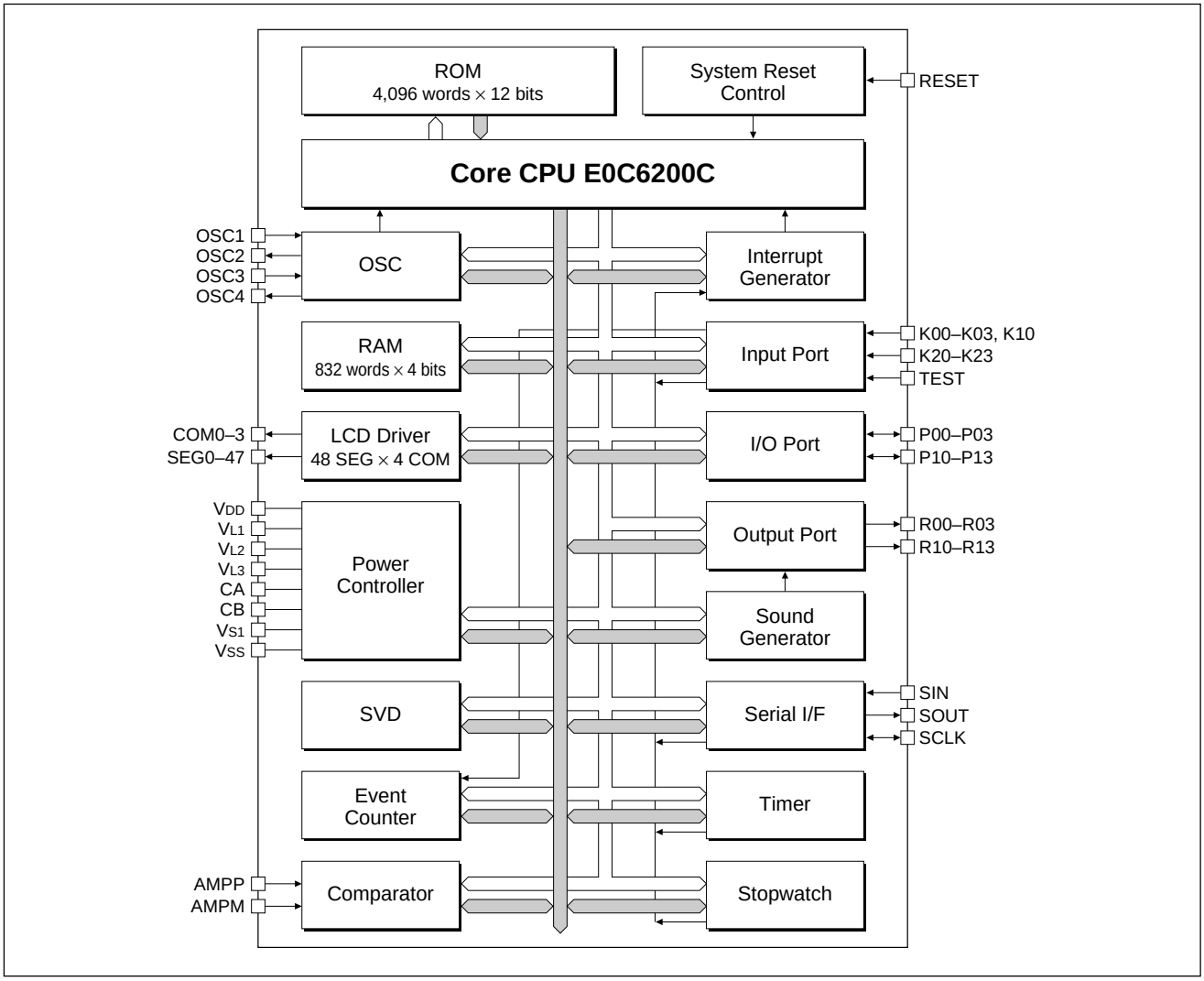
■ DESCRIPTION

Micro MINI "E0C6008" is a single chip microcomputer for battery-driven products with 7-segment LCD display. It achieves low cost performance, and is suitable for a product added some feature instead of standard IC. It consists that Seiko Epson's original core CPU E0C6200C, LCD driver (48 segments × 4 commons), 832 words RAM, 4K words ROM, serial interface, clock timer and so on.

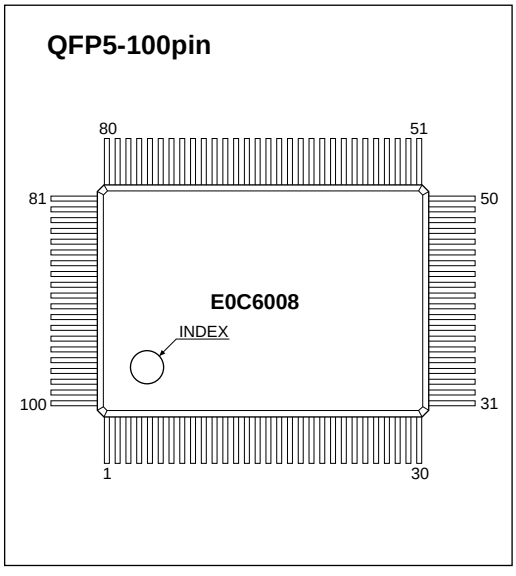
■ FEATURES

- CMOS LSI 4-bit parallel processing
- Main clock 32.768kHz
- Sub clock ..... 500kHz (Typ. CR/Ceramic)
- Instruction set ..... 108 instructions
- ROM capacity ..... 4,096 × 12 bits
- RAM capacity ..... 832 × 4 bits
- I/O port ..... I: 9 bits
O: 8 bits
I/O: 8 bits
- Battery low detection circuit (BLD) 1.2V (E0C60L08)
2.4V (E0C6008)
2.4V (E0C60A08)
- Clock timer ..... 1ch.
- Stopwatch timer ..... 1ch.
- Watchdog timer ..... Built-in
- Serial interface ..... Synchronous 8 bits
- LCD driver ..... 48 segments × 4/3/2 commons
- Operation voltage ..... 0.9 to 1.7V (E0C60L08)
1.8 to 3.5V (E0C6008)
2.2 to 3.5V (E0C60A08)
- Power consumption ..... 1.0µA (32.768kHz X'tal, 3.0V, HALT)
2.2µA (32.768kHz X'tal, 3.0V, RUN)
50µA (500kHz Ceramic, 3.0V, RUN)
- Package ..... Die form, QFP15-100pin or QFP5-100pin

■ BLOCK DIAGRAM



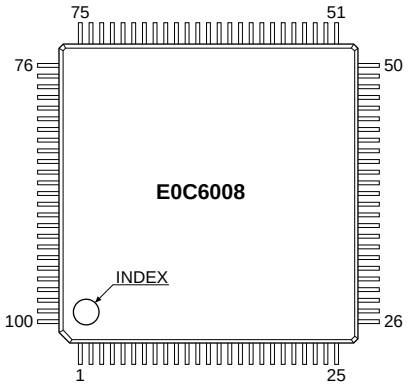
■ PIN CONFIGURATION



No.	Pin name	No.	Pin name	No.	Pin name	No.	Pin name	No.	Pin name
1	COM1	21	SEG29	41	SEG10	61	K01	81	R12
2	COM0	22	SEG28	42	SEG9	62	K00	82	R11
3	SEG47	23	SEG27	43	SEG8	63	SIN	83	R10
4	SEG46	24	SEG26	44	SEG7	64	SOUT	84	R13
5	SEG45	25	SEG25	45	SEG6	65	N.C.	85	V_{SS}
6	SEG44	26	SEG24	46	SEG5	66	SCLK	86	RESET
7	SEG43	27	TEST	47	SEG4	67	P03	87	OSC4
8	SEG42	28	SEG23	48	SEG3	68	P02	88	OSC3
9	SEG41	29	SEG22	49	SEG2	69	P01	89	V_{S1}
10	SEG40	30	SEG21	50	SEG1	70	P00	90	OSC2
11	SEG39	31	SEG20	51	SEG0	71	N.C.	91	OSC1
12	SEG38	32	SEG19	52	AMPP	72	N.C.	92	V_{DD}
13	SEG37	33	SEG18	53	AMPM	73	P13	93	V_{L3}
14	SEG36	34	SEG17	54	K23	74	P12	94	V_{L2}
15	SEG35	35	SEG16	55	K22	75	P11	95	V_{L1}
16	SEG34	36	SEG15	56	K21	76	P10	96	CA
17	SEG33	37	SEG14	57	K20	77	R03	97	CB
18	SEG32	38	SEG13	58	K10	78	R02	98	N.C.
19	SEG31	39	SEG12	59	K03	79	R01	99	COM3
20	SEG30	40	SEG11	60	K02	80	R00	100	COM2

N.C. = No Connection

QFP15-100pin



No.	Pin name	No.	Pin name	No.	Pin name	No.	Pin name	No.	Pin name
1	SEG47	21	SEG27	41	SEG9	61	K00	81	R10
2	SEG46	22	SEG26	42	SEG8	62	SIN	82	R13
3	SEG45	23	SEG25	43	SEG7	63	SOUT	83	V_{SS}
4	SEG44	24	SEG24	44	SEG6	64	N.C.	84	RESET
5	SEG43	25	TEST	45	SEG5	65	SCLK	85	OSC4
6	SEG42	26	SEG23	46	SEG4	66	N.C.	86	OSC3
7	SEG41	27	SEG22	47	SEG3	67	P03	87	V_{S1}
8	SEG40	28	SEG21	48	SEG2	68	P02	88	OSC2
9	SEG39	29	SEG20	49	SEG1	69	P01	89	OSC1
10	SEG38	30	SEG19	50	SEG0	70	P00	90	V_{DD}
11	SEG37	31	SEG18	51	AMPP	71	P13	91	V_{L3}
12	SEG36	32	SEG17	52	AMPM	72	P12	92	V_{L2}
13	SEG35	33	SEG16	53	K23	73	P11	93	V_{L1}
14	SEG34	34	SEG15	54	K22	74	P10	94	CA
15	SEG33	35	SEG14	55	K21	75	R03	95	CB
16	SEG32	36	SEG13	56	K20	76	R02	96	N.C.
17	SEG31	37	SEG12	57	K10	77	R01	97	COM3
18	SEG30	38	N.C.	58	K03	78	R00	98	COM2
19	SEG29	39	SEG11	59	K02	79	R12	99	COM1
20	SEG28	40	SEG10	60	K01	80	R11	100	COM0

N.C. = No Connection

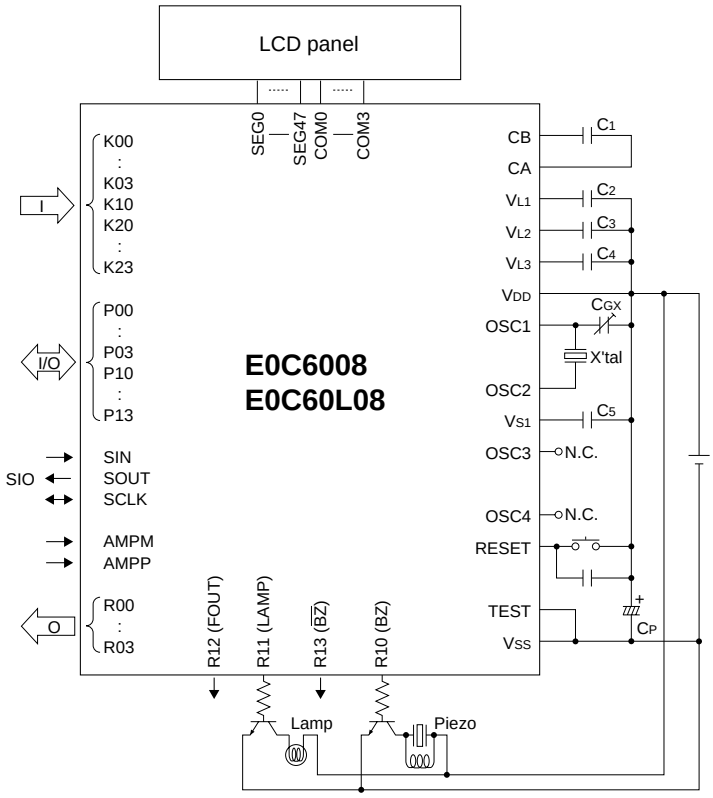
■ PIN DESCRIPTION

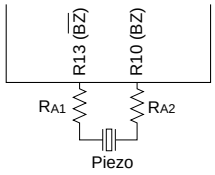
Pin name	Pin No.		I/O	Function
	QFP5-100	QFP15-100		
V_{DD}	92	90	(I)	Power supply pin (+)
V_{SS}	85	83	(I)	Power supply pin (-)
V_{S1}	89	87	–	Oscillation and internal logic system voltage output pin
V_{L1}	95	93	–	LCD drive voltage output pin (approx. -1.05 V or 1/2·V_{L2})
V_{L2}	94	92	–	LCD drive voltage output pin (2·V_{L1} or approx. -2.10 V)
V_{L3}	93	91	–	LCD drive voltage output pin (3·V_{L1} or 3/2·V_{L2})
CA, CB	96, 97	94, 95	–	Boost capacitor connecting pin
OSC1	91	89	I	Cryctal oscillation input pin
OSC2	90	88	O	Crystal oscillation output pin
OSC3	88	86	I	CR or ceramic oscillation input pin * (N.C. for E0C6008 and E0C60L08)
OSC4	87	85	O	CR or ceramic oscillation output pin * (N.C. for E0C6008 and E0C60L08)
K00–K03	62–59	61–58	I	Input port pin
K10	58	57	I	Input port pin
K20–K23	57–54	56–53	I	Input port pin
P00–P03	70–67	70–67	I/O	I/O port pin
P10–P13	76–73	74–71	I/O	I/O port pin
R00–R03	80–77	78–75	O	Output port pin
R10	83	81	O	Output port pin or BZ output pin *
R13	84	82	O	Output port pin or $\overline{BZ}$ output pin *
R11	82	80	O	Output port pin or SIOF output pin *
R12	81	79	O	Output port pin or FOUT output pin *
SIN	63	62	I	Serial interface data input pin
SOUT	64	63	O	Serial interface data output pin
SCLK	66	65	I/O	Serial interface clock input/output pin
AMPP	52	51	I	Analog comparator non-inverted input pin
AMPM	53	52	I	Analog comparator inverted input pin
SEG0–47	51–28, 26–3	50–39, 37–26, 24–1	O	LCD segment output pin or DC output pin *
COM0–3	2, 1, 100, 99	100–97	O	LCD common output pin (1/2, 1/3 or 1/4 duty are selectable *)
RESET	86	84	I	Initial reset input pin
TEST	27	25	I	Input pin for test

* Can be selected by mask option

■ BASIC EXTERNAL CONNECTION DIAGRAM

E0C6008 and E0C60L08

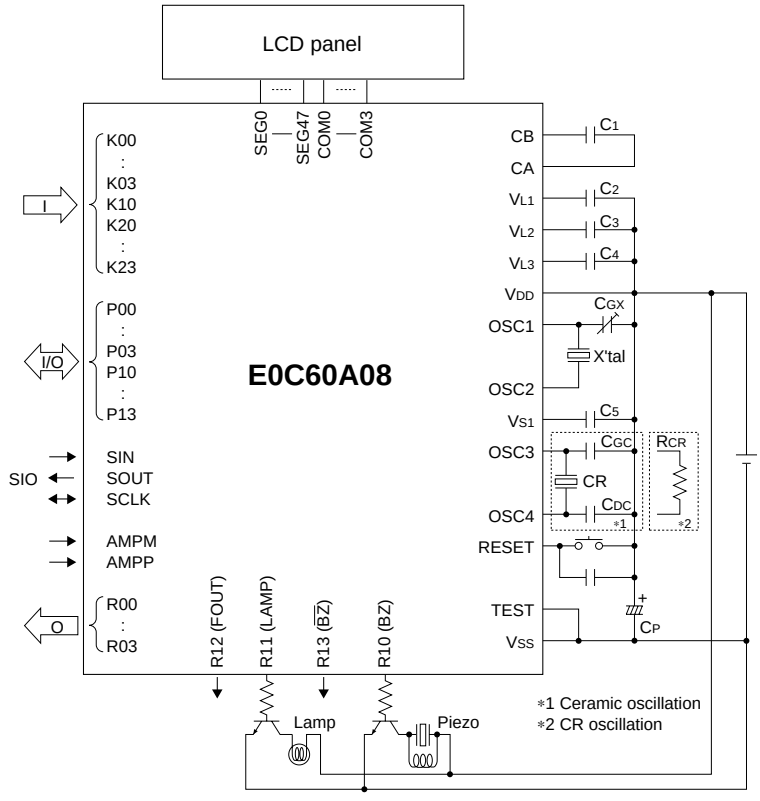


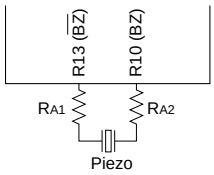


When the piezoelectric buzzer is driven directly

X'tal	Crystal oscillator	32.768 kHz or 38.400 kHz, C_I = 35 kΩ
C_{GX}	Trimmer capacitor	5–25 pF
C_1	Capacitor	0.1 µF
C_2	Capacitor	0.1 µF
C_3	Capacitor	0.1 µF
C_4	Capacitor	0.1 µF
C_5	Capacitor	0.1 µF
C_P	Capacitor	3.3 µF
R_{A1}	Protection resistor	100 Ω
R_{A2}	Protection resistor	100 Ω

E0C60A08





When the piezoelectric buzzer is driven directly

X'tal	Crystal oscillator	32.768 kHz or 38.400 kHz, C_I = 35 kΩ
C_{GX}	Trimmer capacitor	5–25 pF
CR	Ceramic oscillator	500 kHz
C_{GC}	Gate capacitor	100 pF
C_{DC}	Drain capacitor	100 pF
R_{CR}	Resistor for CR oscillation	82 kΩ
C_1	Capacitor	0.1 µF
C_2	Capacitor	0.1 µF
C_3	Capacitor	0.1 µF
C_4	Capacitor	0.1 µF
C_5	Capacitor	0.1 µF
C_P	Capacitor	3.3 µF
R_{A1}	Protection resistor	100 Ω
R_{A2}	Protection resistor	100 Ω

Note: The above tables are simply an example, and are not guaranteed to work.

■ ELECTRICAL CHARACTERISTICS

● Absolute Maximum Ratings

E0C6008 and E0C60A08

(V_{DD}=0V)

Rating	Symbol	Value	Unit
Supply voltage	V_{SS}	-5.0 to 0.5	V
Input voltage (1)	V_I	V_{SS}-0.3 to 0.5	V
Input voltage (2)	V_{IOSC}	V_{S1}-0.3 to 0.5	V
Permissible total output current *1	ΣI_{VSS}	10	mA
Operating temperature	Topr	-20 to 70	°C
Storage temperature	Tstg	-65 to 150	°C
Soldering temperature / time	Tsol	260°C, 10sec (lead section)	–
Permissible dissipation *2	P_D	250	mW

*1: The permissible total output current is the sum total of the current (average current) that simultaneously flows from the output pins (or is draw in).
*2: In case of plastic package.

E0C60L08

(V_{DD}=0V)

Rating	Symbol	Value	Unit
Supply voltage	V_{SS}	-2.0 to 0.5	V
Input voltage (1)	V_I	V_{SS}-0.3 to 0.5	V
Input voltage (2)	V_{IOSC}	V_{S1}-0.3 to 0.5	V
Permissible total output current *1	ΣI_{VSS}	10	mA
Operating temperature	Topr	-20 to 70	°C
Storage temperature	Tstg	-65 to 150	°C
Soldering temperature / time	Tsol	260°C, 10sec (lead section)	–
Permissible dissipation *2	P_D	250	mW

*1: The permissible total output current is the sum total of the current (average current) that simultaneously flows from the output pins (or is draw in).
*2: In case of plastic package.

● Recommended Operating Conditions

E0C6008

(Ta=-20 to 70°C)

Condition	Symbol	Remark	Min.	Typ.	Max.	Unit
Supply voltage	V_{SS}	V_{DD}=0V	-3.5	-3.0	-1.8	V
Oscillation frequency	f_{OSC1}	Either one is selected	–	32.768	–	kHz
			–	38.400	–	kHz

E0C60L08

(Ta=-20 to 70°C)

Condition	Symbol	Remark	Min.	Typ.	Max.	Unit
Supply voltage	V_{SS}	V_{DD}=0V	-1.7	-1.5	-1.1	V
		V_{DD}=0V, with software control *1	-1.7	-1.5	-0.9 *2	V
		V_{DD}=0V, when analog comparator is used	-1.7	-1.5	-1.2	V
Oscillation frequency	f_{OSC1}	Either one is selected	–	32.768	–	kHz
			–	38.400	–	kHz

*1: When switching to heavy load protection mode.
*2: The possibility of LCD panel display differs depending on the characteristics of the LCD panel.

E0C60A08

(Ta=-20 to 70°C)

Condition	Symbol	Remark	Min.	Typ.	Max.	Unit
Supply voltage	V_{SS}	V_{DD}=0V	-3.5	-3.0	-2.2	V
Oscillation frequency (1)	f_{OSC1}	Either one is selected	–	32.768	–	kHz
			–	38.400	–	kHz
Oscillation frequency (2)	f_{OSC3}	duty 50±5%	50	500	600	kHz

● DC Characteristics

E0C6008 and E0C60A08

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-3.0V, f_{OSC1}=32.768kHz, Ta=25°C, V_{S1}/V_{L1}–V_{L3} are internal voltage, C_1–C_5=0.1µF)

Characteristic	Symbol	Condition		Min.	Typ.	Max.	Unit
High level input voltage (1)	V_{IH1}		K00–03, K10, K20–23, P00–03 P10–13, SIN	0.2·V_{SS}		0	V
High level input voltage (2)	V_{IH2}		SCLK, RESET, TEST	0.1·V_{SS}		0	V
Low level input voltage (1)	V_{IL1}		K00–03, K10, K20–23, P00–03 P10–13, SIN	V_{SS}		0.8·V_{SS}	V
Low level input voltage (2)	V_{IL2}		SCLK, RESET, TEST	V_{SS}		0.9·V_{SS}	V
High level input current (1)	I_{IH1}	V_{IH1}=0V No pull-down	K00–03, K10, K20–23, P00–03 P10–13, SIN, SCLK, AMPP AMPM, RESET	0		0.5	µA
High level input current (2)	I_{IH2}	V_{IH2}=0V With pull-down	K00–03, K10, K20–23, SIN SCLK	4		16	µA
High level input current (3)	I_{IH3}	V_{IH3}=0V With pull-down	P00–03, P10–13, RESET, TEST	25		100	µA
Low level input current	I_{IL}	V_{IL}=V_{SS}	K00–03, K10, K20–23, P00–03 P10–13, SIN, SCLK, AMPP AMPM, RESET, TEST	-0.5		0	µA
High level output current (1)	I_{OH1}	V_{OH1}=0.1·V_{SS}	R10, R11, R13			-1.8	mA
High level output current (2)	I_{OH2}	V_{OH2}=0.1·V_{SS}	R00–03, R12, P00–03, P10–13 SOUT, SCLK			-0.9	mA
Low level output current (1)	I_{OL1}	V_{OL1}=0.9·V_{SS}	R10, R11, R13	6.0			mA
Low level output current (2)	I_{OL2}	V_{OL2}=0.9·V_{SS}	R00–03, R12, P00–03, P10–13 SOUT, SCLK	3.0			mA
Common output current	I_{OH3}	V_{OH3}=-0.05V	COM0–3			-3	µA
	I_{OL3}	V_{OL3}=V_{L3}+0.05V		3			µA
Segment output current (during LCD output)	I_{OH4}	V_{OH4}=-0.05V	SEG0–47			-3	µA
	I_{OL4}	V_{OL4}=V_{L3}+0.05V		3			µA
Segment output current (during DC output)	I_{OH5}	V_{OH5}=0.1·V_{SS}	SEG0–47			-200	µA
	I_{OL5}	V_{OL5}=0.9·V_{SS}		200			µA

E0C60L08

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-1.5V, f_{OSC1}=32.768kHz, Ta=25°C, V_{S1}/V_{L1}–V_{L3} are internal voltage, C_1–C_5=0.1µF)

Characteristic	Symbol	Condition		Min.	Typ.	Max.	Unit
High level input voltage (1)	V_{IH1}		K00–03, K10, K20–23, P00–03 P10–13, SIN	0.2·V_{SS}		0	V
High level input voltage (2)	V_{IH2}		SCLK, RESET, TEST	0.1·V_{SS}		0	V
Low level input voltage (1)	V_{IL1}		K00–03, K10, K20–23, P00–03 P10–13, SIN	V_{SS}		0.8·V_{SS}	V
Low level input voltage (2)	V_{IL2}		SCLK, RESET, TEST	V_{SS}		0.9·V_{SS}	V
High level input current (1)	I_{IH1}	V_{IH1}=0V No pull-down	K00–03, K10, K20–23, P00–03 P10–13, SIN, SCLK, AMPP AMPM, RESET	0		0.5	µA
High level input current (2)	I_{IH2}	V_{IH2}=0V With pull-down	K00–03, K10, K20–23, SIN SCLK	2		10	µA
High level input current (3)	I_{IH3}	V_{IH3}=0V With pull-down	P00–03, P10–13, RESET, TEST	12		60	µA
Low level input current	I_{IL}	V_{IL}=V_{SS}	K00–03, K10, K20–23, P00–03 P10–13, SIN, SCLK, AMPP AMPM, RESET, TEST	-0.5		0	µA
High level output current (1)	I_{OH1}	V_{OH1}=0.1·V_{SS}	R10, R11, R13			-300	µA
High level output current (2)	I_{OH2}	V_{OH2}=0.1·V_{SS}	R00–03, R12, P00–03, P10–13 SOUT, SCLK			-150	µA
Low level output current (1)	I_{OL1}	V_{OL1}=0.9·V_{SS}	R10, R11, R13	1400			µA
Low level output current (2)	I_{OL2}	V_{OL2}=0.9·V_{SS}	R00–03, R12, P00–03, P10–13 SOUT, SCLK	700			µA
Common output current	I_{OH3}	V_{OH3}=-0.05V	COM0–3			-3	µA
	I_{OL3}	V_{OL3}=V_{L3}+0.05V		3			µA
Segment output current (during LCD output)	I_{OH4}	V_{OH4}=-0.05V	SEG0–47			-3	µA
	I_{OL4}	V_{OL4}=V_{L3}+0.05V		3			µA
Segment output current (during DC output)	I_{OH5}	V_{OH5}=0.1·V_{SS}	SEG0–47			-100	µA
	I_{OL5}	V_{OL5}=0.9·V_{SS}		100			µA

● Analog Circuit Characteristics and Current Consumption

E0C6008 (Normal Operating Mode)

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-3.0V, f_{OSC1}=32.768kHz, Ta=25°C, C_G=25pF, V_{S1}/V_{L1}–V_{L3} are internal voltage, C_1–C_5=0.1µF)

Characteristic	Symbol	Condition		Min.	Typ.	Max.	Unit
LCD drive voltage	V_{L1}	Connect 1 MΩ load resistor between V_{DD} and V_{L1} (without panel load)		1/2·V_{L2} - 0.1		1/2·V_{L2} ×0.9	V
	V_{L2}	Connect 1 MΩ load resistor between V_{DD} and V_{L2} (without panel load)		-2.30	-2.10	-1.90	V
	V_{L3}	Connect 1 MΩ load resistor between V_{DD} and V_{L3} (without panel load)		3/2·V_{L2} - 0.1		3/2·V_{L2} ×0.9	V
BLD voltage *1	V_{B0}	BLC="0"		-2.35	-2.20	-2.05	V
	V_{B1}	BLC="1"		-2.40	-2.25	-2.10	V
	V_{B2}	BLC="2"		-2.45	-2.30	-2.15	V
	V_{B3}	BLC="3"		-2.50	-2.35	-2.20	V
	V_{B4}	BLC="4"		-2.55	-2.40	-2.25	V
	V_{B5}	BLC="5"		-2.60	-2.45	-2.30	V
	V_{B6}	BLC="6"		-2.65	-2.50	-2.35	V
	V_{B7}	BLC="7"		-2.70	-2.55	-2.40	V
BLD circuit response time	t_B					100	µsec
Sub-BLD voltage	V_{BS}			-2.55	-2.40	-2.25	V
Sub-BLD circuit response time	t_{BS}					100	µsec
Analog comparator input voltage	V_{IP}	Non-inverted input (AMPP)		V_{SS}+0.3		V_{DD}-0.9	V
	V_{IM}	Inverted input (AMPM)					
Analog comparator offset voltage	V_{OF}					10	mV
Analog comparator response time	t_{AMP}	V_{IP}=-1.5V V_{IM}=V_{IP}±15mV				3	msec
Current consumption	I_{OP}	During HALT	Without panel load		1.0	2.0	µA
		During operation *2			2.2	4.0	µA

*1: The relationships among V_{B0}–V_{B7} are V_{B0}>V_{B1}>V_{B2}>...V_{B5}>V_{B6}>V_{B7}.
*2: The BLD circuit, sub-BLD circuit and analog comparator are in the OFF status.

E0C6008 (Heavy Load Protection Mode)

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-3.0V, f_{OSC1}=32.768kHz, Ta=25°C, C_G=25pF, V_{S1}/V_{L1}–V_{L3} are internal voltage, C_1–C_5=0.1µF)

Characteristic	Symbol	Condition		Min.	Typ.	Max.	Unit
LCD drive voltage	V_{L1}	Connect 1 MΩ load resistor between V_{DD} and V_{L1} (without panel load)		1/2·V_{L2} - 0.1		1/2·V_{L2} ×0.9	V
	V_{L2}	Connect 1 MΩ load resistor between V_{DD} and V_{L2} (without panel load)		-2.30	-2.10	-1.90	V
	V_{L3}	Connect 1 MΩ load resistor between V_{DD} and V_{L3} (without panel load)		3/2·V_{L2} - 0.1		3/2·V_{L2} ×0.9	V
BLD voltage *1	V_{B0}	BLC="0"		-2.35	-2.20	-2.05	V
	V_{B1}	BLC="1"		-2.40	-2.25	-2.10	V
	V_{B2}	BLC="2"		-2.45	-2.30	-2.15	V
	V_{B3}	BLC="3"		-2.50	-2.35	-2.20	V
	V_{B4}	BLC="4"		-2.55	-2.40	-2.25	V
	V_{B5}	BLC="5"		-2.60	-2.45	-2.30	V
	V_{B6}	BLC="6"		-2.65	-2.50	-2.35	V
	V_{B7}	BLC="7"		-2.70	-2.55	-2.40	V
BLD circuit response time	t_B					100	µsec
Sub-BLD voltage	V_{BS}			-2.55	-2.40	-2.25	V
Sub-BLD circuit response time	t_{BS}					100	µsec
Analog comparator input voltage	V_{IP}	Non-inverted input (AMPP)		V_{SS}+0.3		V_{DD}-0.9	V
	V_{IM}	Inverted input (AMPM)					
Analog comparator offset voltage	V_{OF}					10	mV
Analog comparator response time	t_{AMP}	V_{IP}=-1.5V V_{IM}=V_{IP}±15mV				3	msec
Current consumption	I_{OP}	During HALT	Without panel load		10	20	µA
		During operation *2			12	25	µA

*1: The relationships among V_{B0}–V_{B7} are V_{B0}>V_{B1}>V_{B2}>...V_{B5}>V_{B6}>V_{B7}.
*2: The BLD circuit and sub-BLD circuit are in the ON status (HLMOD="1", BLS="0").
The analog comparator is in the OFF status.

E0C60L08 (Normal Operating Mode)

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-1.5V, f_{OSC1}=32.768kHz, Ta=25°C, C_G=25pF, V_{S1}/V_{L1}–V_{L3} are internal voltage, C_1–C_5=0.1µF)

Characteristic	Symbol	Condition		Min.	Typ.	Max.	Unit
LCD drive voltage	V_{L1}	Connect 1 MΩ load resistor between V_{DD} and V_{L1} (without panel load)		-1.15	-1.05	-0.95	V
	V_{L2}	Connect 1 MΩ load resistor between V_{DD} and V_{L2} (without panel load)		$2 \cdot V_{L1}$ - 0.1		$2 \cdot V_{L1}$ ×0.9	V
	V_{L3}	Connect 1 MΩ load resistor between V_{DD} and V_{L3} (without panel load)		$3 \cdot V_{L1}$ - 0.1		$3 \cdot V_{L1}$ ×0.9	V
BLD voltage *1	V_{B0}	BLC="0"		-1.15	-1.05	-0.95	V
	V_{B1}	BLC="1"		-1.20	-1.10	-1.00	V
	V_{B2}	BLC="2"		-1.25	-1.15	-1.05	V
	V_{B3}	BLC="3"		-1.30	-1.20	-1.10	V
	V_{B4}	BLC="4"		-1.35	-1.25	-1.15	V
	V_{B5}	BLC="5"		-1.40	-1.30	-1.20	V
	V_{B6}	BLC="6"		-1.45	-1.35	-1.25	V
	V_{B7}	BLC="7"		-1.50	-1.40	-1.30	V
BLD circuit response time	t_B					100	µsec
Sub-BLD voltage	V_{BS}			-1.30	-1.20	-1.10	V
Sub-BLD circuit response time	t_{BS}					100	µsec
Analog comparator input voltage	V_{IP}	Non-inverted input (AMPP)		V_{SS}+0.3		V_{DD}-0.9	V
	V_{IM}	Inverted input (AMPM)					
Analog comparator offset voltage	V_{OF}					20	mV
Analog comparator response time	t_{AMP}	V_{IP}=-1.1V V_{IM}=V_{IP}±30mV				3	msec
Current consumption	I_{OP}	During HALT	Without panel load		1.0	2.0	µA
		During operation *2			2.2	4.0	µA

*1: The relationships among V_{B0}–V_{B7} are V_{B0}>V_{B1}>V_{B2}>...V_{B5}>V_{B6}>V_{B7}.
*2: The BLD circuit, sub-BLD circuit and analog comparator are in the OFF status.

E0C60L08 (Heavy Load Protection Mode)

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-1.5V, f_{OSC1}=32.768kHz, Ta=25°C, C_G=25pF, V_{S1}/V_{L1}–V_{L3} are internal voltage, C_1–C_5=0.1µF)

Characteristic	Symbol	Condition		Min.	Typ.	Max.	Unit
LCD drive voltage	V_{L1}	Connect 1 MΩ load resistor between V_{DD} and V_{L1} (without panel load)		-1.15	-1.05	-0.95	V
	V_{L2}	Connect 1 MΩ load resistor between V_{DD} and V_{L2} (without panel load)		$2 \cdot V_{L1}$ - 0.1		$2 \cdot V_{L1}$ ×0.85	V
	V_{L3}	Connect 1 MΩ load resistor between V_{DD} and V_{L3} (without panel load)		$3 \cdot V_{L1}$ - 0.1		$3 \cdot V_{L1}$ ×0.85	V
BLD voltage *1	V_{B0}	BLC="0"		-1.15	-1.05	-0.95	V
	V_{B1}	BLC="1"		-1.20	-1.10	-1.00	V
	V_{B2}	BLC="2"		-1.25	-1.15	-1.05	V
	V_{B3}	BLC="3"		-1.30	-1.20	-1.10	V
	V_{B4}	BLC="4"		-1.35	-1.25	-1.15	V
	V_{B5}	BLC="5"		-1.40	-1.30	-1.20	V
	V_{B6}	BLC="6"		-1.45	-1.35	-1.25	V
	V_{B7}	BLC="7"		-1.50	-1.40	-1.30	V
BLD circuit response time	t_B					100	µsec
Sub-BLD voltage	V_{BS}			-1.30	-1.20	-1.10	V
Sub-BLD circuit response time	t_{BS}					100	µsec
Analog comparator input voltage	V_{IP}	Non-inverted input (AMPP)		V_{SS}+0.3		V_{DD}-0.9	V
	V_{IM}	Inverted input (AMPM)					
Analog comparator offset voltage	V_{OF}					20	mV
Analog comparator response time	t_{AMP}	V_{IP}=-1.1V V_{IM}=V_{IP}±30mV				3	msec
Current consumption	I_{OP}	During HALT	Without panel load		6.5	10	µA
		During operation *2			8.5	15	µA

*1: The relationships among V_{B0}–V_{B7} are V_{B0}>V_{B1}>V_{B2}>...V_{B5}>V_{B6}>V_{B7}.
*2: The BLD circuit and sub-BLD circuit are in the ON status (HLMOD="1", BLS="0").
The analog comparator is in the OFF status.

E0C60A08 (Normal Operating Mode)

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-3.0V, f_{OSC1}=32.768kHz, Ta=25°C, C_G=25pF, V_{S1}/V_{L1}–V_{L3} are internal voltage, C_1–C_5=0.1µF)

Characteristic	Symbol	Condition		Min.	Typ.	Max.	Unit
LCD drive voltage	V_{L1}	Connect 1 MΩ load resistor between V_{DD} and V_{L1} (without panel load)		-1.15	-1.05	-0.95	V
	V_{L2}	Connect 1 MΩ load resistor between V_{DD} and V_{L2} (without panel load)		$2 \cdot V_{L1}$ - 0.1		$2 \cdot V_{L1}$ ×0.9	V
	V_{L3}	Connect 1 MΩ load resistor between V_{DD} and V_{L3} (without panel load)		$3 \cdot V_{L1}$ - 0.1		$3 \cdot V_{L1}$ ×0.9	V
BLD voltage *1	V_{B0}	BLC="0"		-2.35	-2.20	-2.05	V
	V_{B1}	BLC="1"		-2.40	-2.25	-2.10	V
	V_{B2}	BLC="2"		-2.45	-2.30	-2.15	V
	V_{B3}	BLC="3"		-2.50	-2.35	-2.20	V
	V_{B4}	BLC="4"		-2.55	-2.40	-2.25	V
	V_{B5}	BLC="5"		-2.60	-2.45	-2.30	V
	V_{B6}	BLC="6"		-2.65	-2.50	-2.35	V
	V_{B7}	BLC="7"		-2.70	-2.55	-2.40	V
BLD circuit response time	t_B					100	µsec
Sub-BLD voltage	V_{BS}			-2.55	-2.40	-2.25	V
Sub-BLD circuit response time	t_{BS}					100	µsec
Analog comparator input voltage	V_{IP}	Non-inverted input (AMPP)		V_{SS}+0.3		V_{DD}-0.9	V
	V_{IM}	Inverted input (AMPM)					
Analog comparator offset voltage	V_{OF}					10	mV
Analog comparator response time	t_{AMP}	V_{IP}=-1.5V V_{IM}=V_{IP}±15mV				3	msec
Current consumption	I_{OP}	During HALT	Without panel load		1.1	2.0	µA
		During operation *2			3.0	5.0	µA
		During operation at 500kHz *2			50	70	µA

*1: The relationships among V_{B0}–V_{B7} are V_{B0}>V_{B1}>V_{B2}>...V_{B5}>V_{B6}>V_{B7}.

*2: The BLD circuit, sub-BLD circuit and analog comparator are in the OFF status.

E0C60A08 (Heavy Load Protection Mode)

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-3.0V, f_{OSC1}=32.768kHz, Ta=25°C, C_G=25pF, V_{S1}/V_{L1}–V_{L3} are internal voltage, C_1–C_5=0.1µF)

Characteristic	Symbol	Condition		Min.	Typ.	Max.	Unit
LCD drive voltage	V_{L1}	Connect 1 MΩ load resistor between V_{DD} and V_{L1} (without panel load)		-1.15	-1.05	-0.95	V
	V_{L2}	Connect 1 MΩ load resistor between V_{DD} and V_{L2} (without panel load)		$2 \cdot V_{L1}$ - 0.1		$2 \cdot V_{L1}$ ×0.9	V
	V_{L3}	Connect 1 MΩ load resistor between V_{DD} and V_{L3} (without panel load)		$3 \cdot V_{L1}$ - 0.1		$3 \cdot V_{L1}$ ×0.9	V
BLD voltage *1	V_{B0}	BLC="0"		-2.35	-2.20	-2.05	V
	V_{B1}	BLC="1"		-2.40	-2.25	-2.10	V
	V_{B2}	BLC="2"		-2.45	-2.30	-2.15	V
	V_{B3}	BLC="3"		-2.50	-2.35	-2.20	V
	V_{B4}	BLC="4"		-2.55	-2.40	-2.25	V
	V_{B5}	BLC="5"		-2.60	-2.45	-2.30	V
	V_{B6}	BLC="6"		-2.65	-2.50	-2.35	V
	V_{B7}	BLC="7"		-2.70	-2.55	-2.40	V
BLD circuit response time	t_B					100	µsec
Sub-BLD voltage	V_{BS}			-2.55	-2.40	-2.25	V
Sub-BLD circuit response time	t_{BS}					100	µsec
Analog comparator input voltage	V_{IP}	Non-inverted input (AMPP)		V_{SS}+0.3		V_{DD}-0.9	V
	V_{IM}	Inverted input (AMPM)					
Analog comparator offset voltage	V_{OF}					10	mV
Analog comparator response time	t_{AMP}	V_{IP}=-1.5V V_{IM}=V_{IP}±15mV				3	msec
Current consumption	I_{OP}	During HALT	Without panel load		6.5	10	µA
		During operation *2			8.5	15	µA
		During operation at 500kHz *2			55	75	µA

*1: The relationships among V_{B0}–V_{B7} are V_{B0}>V_{B1}>V_{B2}>...V_{B5}>V_{B6}>V_{B7}.

*2: The BLD circuit and sub-BLD circuit are in the ON status (HLMOD="1", BLS="0").
The analog comparator is in the OFF status.

● Oscillation Characteristics

Oscillation characteristics will vary according to different conditions (elements used, boad pattern). Use the following characteristics are as reference values.

E0C6008 (OSC1 Crystal Oscillation)

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-3.0V, Crystal: C-002R (C_I=35kΩ), C_G=25pF, C_D=built-in, Ta=25°C)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start voltage	Vsta	tsta≤5sec (V_{SS})	-1.8			V
Oscillation stop voltage	Vstp	tstp≤10sec (V_{SS})	-1.8			V
Built-in capacitance (drain)	C_D	Including the parasitic capacitance inside the chip		20		pF
Frequency/voltage deviation	Δf/ΔV	V_{SS}=-1.8 to -3.5V			5	ppm
Frequency/IC deviation	Δf/ΔIC		-10		10	ppm
Frequency adjustment range	Δf/ΔC_G	C_G=5 to 25pF	35	45		ppm
Harmonic oscillation start voltage	V_{hho}	(V_{SS})			-3.5	V
Permitted leak resistance	R_{leak}	Between OSC1 and V_{DD}	200			MΩ

E0C60L08 (OSC1 Crystal Oscillation)

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-1.5V, Crystal: C-002R (C_I=35kΩ), C_G=25pF, C_D=built-in, Ta=25°C)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start voltage	Vsta	tsta≤5sec (V_{SS})	-1.1			V
Oscillation stop voltage	Vstp	tstp≤10sec (V_{SS})	-1.1 (-0.9)*1			V
Built-in capacitance (drain)	C_D	Including the parasitic capacitance inside the chip		20		pF
Frequency/voltage deviation	Δf/ΔV	V_{SS}=-1.1 (-0.9)*1 to -1.7V			5	ppm
Frequency/IC deviation	Δf/ΔIC		-10		10	ppm
Frequency adjustment range	Δf/ΔC_G	C_G=5 to 25pF	35	45		ppm
Harmonic oscillation start voltage	V_{hho}	(V_{SS})			-1.7	V
Permitted leak resistance	R_{leak}	Between OSC1 and V_{DD}	200			MΩ

*1: Parentheses indicate value for operation in heavy load protection mode.

E0C60A08 (OSC1 Crystal Oscillation)

Unless otherwise specified: V_{DD}=0V, V_{SS}=-3.0V, Crystal: C-002R (C_I=35kΩ), C_G=25pF, C_D=built-in, Ta=25°C

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start voltage	Vsta	tsta≤5sec (V_{SS})	-2.2			V
Oscillation stop voltage	Vstp	tstp≤10sec (V_{SS})	-2.2			V
Built-in capacitance (drain)	C_D	Including the parasitic capacitance inside the chip		20		pF
Frequency/voltage deviation	Δf/ΔV	V_{SS}=-2.2 to -3.5V			5	ppm
Frequency/IC deviation	Δf/ΔIC		-10		10	ppm
Frequency adjustment range	Δf/ΔC_G	C_G=5 to 25pF	35	45		ppm
Harmonic oscillation start voltage	V_{hho}	(V_{SS})			-3.5	V
Permitted leak resistance	R_{leak}	Between OSC1 and V_{DD}	200			MΩ

E0C60A08 (OSC3 CR Oscillation)

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-3.0V, R_{CR}=82kΩ, Ta=25°C)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation frequency dispersion	f_{OSC3}		-30	480kHz	30	%
Oscillation start voltage	Vsta	(V_{SS})	-2.2			V
Oscillation start time	tsta	V_{SS}=-2.2 to -3.5V			3	msec
Oscillation stop voltage	Vstp	(V_{SS})	-2.2			V

E0C60A08 (OSC3 Ceramic Oscillation)

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-3.0V, Ceramic oscillator: 500kHz, C_{GC}=C_{DC}=100pF, Ta=25°C)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start voltage	Vsta	(V_{SS})	-2.2			V
Oscillation start time	tsta	V_{SS}=-2.2 to -3.5V			5	msec
Oscillation stop voltage	Vstp	(V_{SS})	-2.2			V

SEIKO EPSON CORPORATION
ELECTRONIC DEVICES MARKETING DIVISION
IC Marketing & Engineering Group

ED International Marketing Department I (Europe & U.S.A.)
421-8, Hino, Hino-shi, Tokyo 191-8501, JAPAN
Phone : 042-587-5812 FAX : 042-587-5564

ED International Marketing Department II (Asia)
421-8, Hino, Hino-shi, Tokyo 191-8501, JAPAN
Phone : 042-587-5814 FAX : 042-587-5110