EPSON

CMOS 4-BIT SINGLE CHIP MICROCOMPUTER

E0C6007 *TECHNICAL MANUAL*

E0C6007 Technical Hardware

ENERGY
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CONTENTS

CHAPTER 1 OUTLINE

The E0C6007 is a microcomputer with a C-MOS 4-bit core CPU E0C6200C as main component, and ROM, RAM, dot matrix LCD driver, time base counter and other circuits built-in.

1.1 Features

Oscillation circuit........................OSC1: 32.768 kHz (Typ.) Crystal or CR oscillation circuit (∗1)
OSC3: 2 MHz (Max.)   CR or ceramic oscillation circuit (∗1)

Instruction set...............................108 types

Instruction execution time......32.768 kHz: 152.6 μsec   213.6 μsec   366.2 μsec
1 MHz: 5.0 μsec   7.0 μsec   12.0 μsec
2 MHz: 2.5 μsec   3.5 μsec   6.0 μsec

ROM capacity..............................4,096 words × 12 bits

RAM capacity..............................Data memory: 512 words × 4 bits
Display memory: 160 words × 4 bits

Input port......................................4 bits   (Pull-up resistors may be supplemented ∗1)

Output port...................................6 bits   (Buzzer and clock outputs are possible ∗1)

I/O port...4 bits

Dot matrix type LCD driver..40 segments × 16 or 8 commons (∗2)

Time base counter.......................Clock timer, stopwatch timer

Programmable timer.................8-bit timer × 1 ch., with event counter and clock output functions

Watchdog timer...........................Built-in

Sound generator..........................8 programmable sounds (8 types of frequency)
with envelope and 1-shot output functions

External interrupt......................Input port interrupt: 1 system

Internal interrupt.......................Clock timer interrupt: 1 system
Stopwatch timer interrupt: 1 system
Programmable timer interrupt: 1 system

Power supply voltage................2.2 V to 5.5 V (Min. 1.8 V when the OSC3 oscillation circuit is not used)

Current consumption (Typ.)..During HALT: 32.768 kHz (crystal oscillation), 3.0 V   2.5 μA
During operation: 32.768 kHz (crystal oscillation), 3.0 V   6.5 μA
2 MHz (CR oscillation), 3.0 V   1 mA

Package...QFP15-100pin (plastic) or chip

∗1: Can be selected with mask option   ∗2: Can be selected with software

1.2 Block Diagram
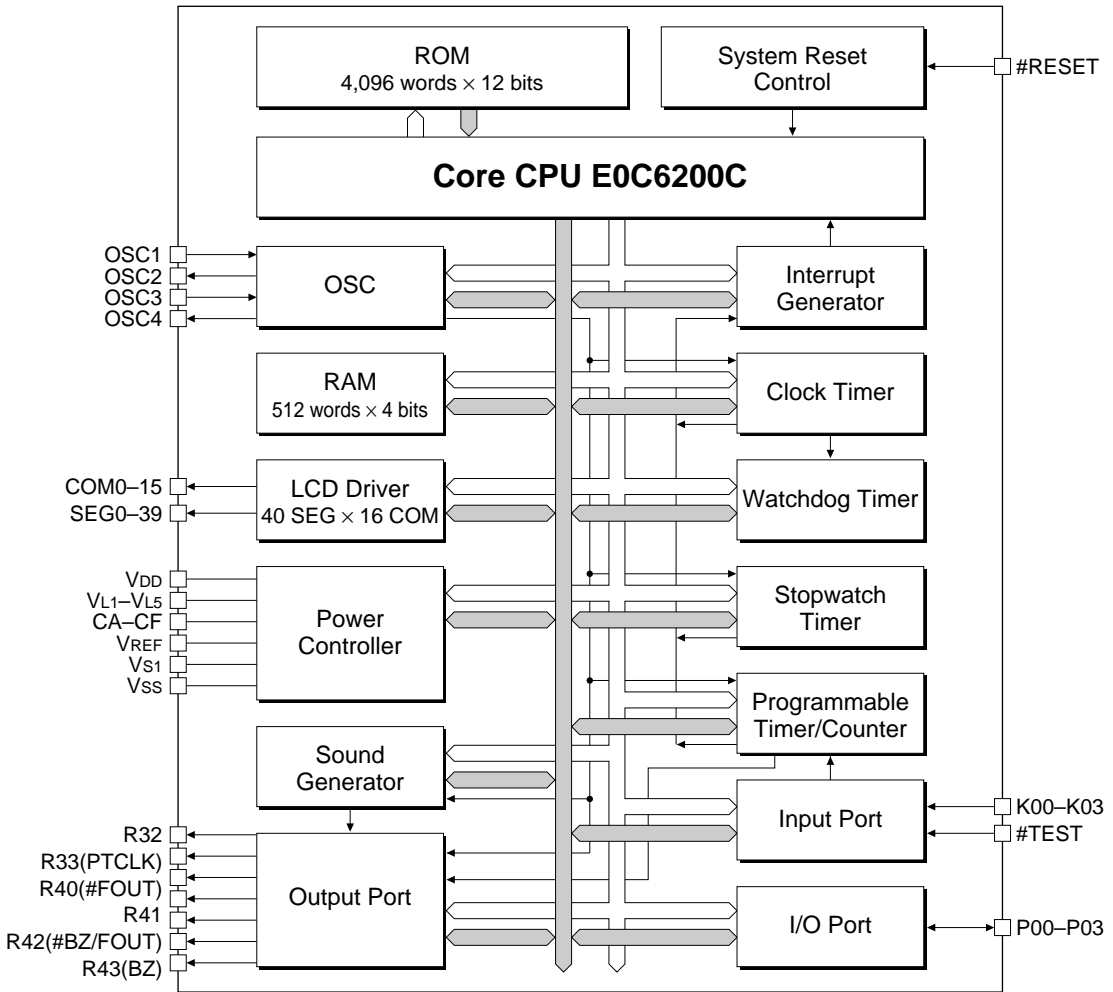
Fig. 1.2.1 Block diagram

1.3 Pin Layout Diagram

QFP15-100pin

No.	Pin name	No.	Pin name	No.	Pin name	No.	Pin name
1	V_{L4}	26	N.C.	51	N.C.	76	N.C.
2	V_{L5}	27	SEG39	52	SEG15	77	N.C.
3	CF	28	SEG38	53	SEG14	78	N.C.
4	CE	29	SEG37	54	SEG13	79	R43
5	CD	30	SEG36	55	SEG12	80	R42
6	CC	31	SEG35	56	SEG11	81	R41
7	CB	32	SEG34	57	SEG10	82	R40
8	CA	33	SEG33	58	SEG9	83	R33
9	COM0	34	SEG32	59	SEG8	84	R32
10	COM1	35	SEG31	60	SEG7	85	#RESET
11	COM2	36	SEG30	61	SEG6	86	#TEST
12	COM3	37	SEG29	62	SEG5	87	V_{SS}
13	COM4	38	SEG28	63	SEG4	88	OSC4
14	COM5	39	SEG27	64	SEG3	89	OSC3
15	COM6	40	SEG26	65	SEG2	90	V_{S1}
16	COM7	41	SEG25	66	SEG1	91	OSC2
17	COM8	42	SEG24	67	SEG0	92	OSC1
18	COM9	43	SEG23	68	K03	93	V_{DD}
19	COM10	44	SEG22	69	K02	94	V_{REF}
20	COM11	45	SEG21	70	K01	95	V_{L1}
21	COM12	46	SEG20	71	K00	96	V_{L2}
22	COM13	47	SEG19	72	P03	97	V_{L3}
23	COM14	48	SEG18	73	P02	98	N.C.
24	COM15	49	SEG17	74	P01	99	N.C.
25	N.C.	50	SEG16	75	P00	100	N.C.

N.C.: No Connection

Fig. 1.3.1 Pin layout diagram

1.4 Pin Description

Table 1.4.1 Pin description

Pin name	Pin No.	I/O	Function	
V_{DD}	93	–	Power supply (+)	
V_{SS}	87	–	Power supply (-)	
V_{S1}	90	–	Internal logic system/oscillation system regulated voltage output	
V_{L1}–V_{L5}	95–97, 1, 2	–	LCD system power supply 1/4 bias generated internally, 1/5 bias generated externally *1	
V_{REF}	94	O	LCD system power test pin *2	
CA–CF	8–3	–	LCD system voltage booster condenser connecting pin	
OSC1	92	I	Crystal or CR oscillator input *1	
OSC2	91	O	Crystal or CR oscillator output *1, C_D buiil-in	
OSC3	89	I	CR or ceramic oscillator input *1	
OSC4	88	O	CR or ceramic oscillator output *1	
COM0–COM15	9–24	O	LCD common output (1/8 duty or 1/16 duty is selected on software)	
SEG0–SEG39	67–52, 50–27	O	LCD segment output	
K00–K03	71–68	I	Input port (pull up resistor is available by mask option) *1	
P00–P03	75–72	I/O	I/O port	Complementary output or Nch open drain output *1
R32	84	O	Output port	
R33	83	O	Output port or PTCLK output	
R40	82	O	Output port or #FOUT output *1	
R41	81	O	Output port	
R42	80	O	Output port, #BZ output or FOUT output *1	
R43	79	O	Output port or BZ output *1	
#RESET	85	I	Initial reset input terminal	
#TEST	86	I	Testing input terminal *3	

*1 Selected by mask option

*2 Leave the V_{REF} pin unconnected (N.C.).

*3 The #TEST pin is used when the IC load is being detected.
During ordinary operation be certain to connect this pin to V_{DD}.

CHAPTER 2 CPU AND BUILT-IN MEMORY

2.1 CPU and Instruction Set

The E0C6007 uses the 4-bit core CPU E0C6200C for its CPU. It has almost the same register configurations, instructions, and other features as the other family devices which use the E0C6200/6200A/6200B, allowing full use of software assets. The instruction set of the E0C6007 has 108 types of instructions, all consisting of one word (12 bits).

For detailed information on the CPU and the instruction set, refer to the "E0C6200/6200A Core CPU Manual".

Note, however, that because E0C6007 does not assume SLEEP operation, the SLP instruction is not available in the E0C6200 instruction set.

The instruction list is shown in Tables 2.1.1(a)–(c).
The following lists the symbols used in the instruction list:

Symbols associated with registers and memory

A	A register
B	B register
X	XHL register (low order eight bits of index register IX)
Y	YHL register (low order eight bits of index register IY)
XH	XH register (high order four bits of XHL register)
XL	XL register (low order four bits of XHL register)
YH	YH register (high order four bits of YHL register)
YL	YL register (low order four bits of YHL register)
XP	XP register (high order four bits of index register IX)
YP	YP register (high order four bits of index register IY)
SP	Stack pointer SP
SPH	High-order four bits of stack pointer SP
SPL	Low-order four bits of stack pointer SP
MX, M(X)	Data memory whose address is specified with index register IX
MY, M(Y)	Data memory whose address is specified with index register IY
Mn, M(n)	Data memory address 000H–0FFH (address specified with immediate data n of 00H–0FH)
M(SP)	Data memory whose address is specified with stack pointer SP
r, q	Two-bit register code
	r, q is two-bit immediate data; according to the contents of these bits, they indicate registers A, B, and MX and MY (data memory whose addresses are specified with index registers IX and IY)

r		q		Register
r1	r0	q1	q0	specified
0	0	0	0	A
0	1	0	1	B
1	0	1	0	MX
1	1	1	1	MY

Symbols associated with program counter

NBP	New bank pointer
NPP	New page pointer
PCB	Program counter bank
PCP	Program counter page
PCS	Program counter step
PCSH	Four high order bits of PCS
PCSL	Four low order bits of PCS

Symbols associated with flags

F	Flag register (I, D, Z, C)
C	Carry flag
Z	Zero flag
D	Decimal flag
I	Interrupt flag
↓	Flag reset
↑	Flag set
↕	Flag set or reset

Associated with immediate data

p	Five-bit immediate data or label 00H–1FH
s	Eight-bit immediate data or label 00H–0FFH
l	Eight-bit immediate data 00H–0FFH
i	Four-bit immediate data 00H–0FH

Associated with arithmetic and other operations

+	Add
-	Subtract
∧	Logical AND
∨	Logical OR
∀	Exclusive-OR
★	Add-subtract instruction for decimal operation when the D flag is set

Table 2.1.1(a) Instruction sets (1)

Classification	Mne-monic	Operand	B	A	9	8	7	6	5	4	3	2	1	0	I	D	Z	C	Clock	Operation
Branch instructions	PSET	p	1	1	1	0	0	1	0	p4	p3	p2	p1	p0					5	NBP←p4, NPP←p3~p0
	JP	s	0	0	0	0	s7	s6	s5	s4	s3	s2	s1	s0					5	PCB←NBP, PCP←NPP, PCS←s7~s0
		C, s	0	0	1	0	s7	s6	s5	s4	s3	s2	s1	s0					5	PCB←NBP, PCP←NPP, PCS←s7~s0 if C=1
		NC, s	0	0	1	1	s7	s6	s5	s4	s3	s2	s1	s0					5	PCB←NBP, PCP←NPP, PCS←s7~s0 if C=0
		Z, s	0	1	1	0	s7	s6	s5	s4	s3	s2	s1	s0					5	PCB←NBP, PCP←NPP, PCS←s7~s0 if Z=1
		NZ, s	0	1	1	1	s7	s6	s5	s4	s3	s2	s1	s0					5	PCB←NBP, PCP←NPP, PCS←s7~s0 if Z=0
	JPBA		1	1	1	1	1	1	1	0	1	0	0	0					5	PCB←NBP, PCP←NPP, PCSH←B, PCSL←A
	CALL	s	0	1	0	0	s7	s6	s5	s4	s3	s2	s1	s0					7	M(SP-1)←PCP, M(SP-2)←PCSH, M(SP-3)←PCSL+1 SP←SP-3, PCP←NPP, PCS←s7~s0
	CALZ	s	0	1	0	1	s7	s6	s5	s4	s3	s2	s1	s0					7	M(SP-1)←PCP, M(SP-2)←PCSH, M(SP-3)←PCSL+1 SP←SP-3, PCP←0, PCS←s7~s0
	RET		1	1	1	1	1	1	0	1	1	1	1	1					7	PCSL←M(SP), PCSH←M(SP+1), PCP←M(SP+2) SP←SP+3
	RETS		1	1	1	1	1	1	0	1	1	1	1	0					12	PCSL←M(SP), PCSH←M(SP+1), PCP←M(SP+2) SP←SP+3, PC←PC+1
	RETD	l	0	0	0	1	l7	l6	l5	l4	l3	l2	l1	l0					12	PCSL←M(SP), PCSH←M(SP+1), PCP←M(SP+2) SP←SP+3, M(X)←l3~l0, M(X+1)←l7~l4, X←X+2
System control instructions	NOP5		1	1	1	1	1	1	1	1	1	0	1	1					5	No operation (5 clock cycles)
	NOP7		1	1	1	1	1	1	1	1	1	1	1	1					7	No operation (7 clock cycles)
	HALT		1	1	1	1	1	1	1	1	1	0	0	0					5	Halt (stop clock)
Index operation instructions	INC	X	1	1	1	0	1	1	1	0	0	0	0	0					5	X←X+1
		Y	1	1	1	0	1	1	1	1	0	0	0	0					5	Y←Y+1
	LD	X, x	1	0	1	1	x7	x6	x5	x4	x3	x2	x1	x0					5	XH←x7~x4, XL←x3~x0
		Y, y	1	0	0	0	y7	y6	y5	y4	y3	y2	y1	y0					5	YH←y7~y4, YL←y3~y0
		XP, r	1	1	1	0	1	0	0	0	0	0	r1	r0					5	XP←r
		XH, r	1	1	1	0	1	0	0	0	0	1	r1	r0					5	XH←r
		XL, r	1	1	1	0	1	0	0	0	1	0	r1	r0					5	XL←r
		YP, r	1	1	1	0	1	0	0	1	0	0	r1	r0					5	YP←r
		YH, r	1	1	1	0	1	0	0	1	0	1	r1	r0					5	YH←r
		YL, r	1	1	1	0	1	0	0	1	1	0	r1	r0					5	YL←r
		r, XP	1	1	1	0	1	0	1	0	0	0	r1	r0					5	r←XP
		r, XH	1	1	1	0	1	0	1	0	0	1	r1	r0					5	r←XH
		r, XL	1	1	1	0	1	0	1	0	1	0	r1	r0					5	r←XL
		r, YP	1	1	1	0	1	0	1	1	0	0	r1	r0					5	r←YP
		r, YH	1	1	1	0	1	0	1	1	0	1	r1	r0					5	r←YH
		r, YL	1	1	1	0	1	0	1	1	1	0	r1	r0					5	r←YL
	ADC	XH, i	1	0	1	0	0	0	0	0	i3	i2	i1	i0			↕	↕	7	XH←XH+i3~i0+C
		XL, i	1	0	1	0	0	0	0	1	i3	i2	i1	i0			↕	↕	7	XL←XL+i3~i0+C
		YH, i	1	0	1	0	0	0	1	0	i3	i2	i1	i0			↕	↕	7	YH←YH+i3~i0+C
		YL, i	1	0	1	0	0	0	1	1	i3	i2	i1	i0			↕	↕	7	YL←YL+i3~i0+C

Table 2.1.1(b) Instruction sets (2)

Classification	Mne-monic	Operand	B	A	9	8	7	6	5	4	3	2	1	0	I	D	Z	C	Clock	Operation
Index operation instructions	CP	XH, i	1	0	1	0	0	1	0	0	i3	i2	i1	i0			↕	↕	7	XH-i3~i0
		XL, i	1	0	1	0	0	1	0	1	i3	i2	i1	i0			↕	↕	7	XL-i3~i0
		YH, i	1	0	1	0	0	1	1	0	i3	i2	i1	i0			↕	↕	7	YH-i3~i0
		YL, i	1	0	1	0	0	1	1	1	i3	i2	i1	i0			↕	↕	7	YL-i3~i0
Data transfer instructions	LD	r, i	1	1	1	0	0	0	r1	r0	i3	i2	i1	i0					5	r←i3~i0
		r, q	1	1	1	0	1	1	0	0	r1	r0	q1	q0					5	r←q
		A, Mn	1	1	1	1	1	0	1	0	n3	n2	n1	n0					5	A←M(n3~n0)
		B, Mn	1	1	1	1	1	0	1	1	n3	n2	n1	n0					5	B←M(n3~n0)
		Mn, A	1	1	1	1	1	0	0	0	n3	n2	n1	n0					5	M(n3~n0)←A
		Mn, B	1	1	1	1	1	0	0	1	n3	n2	n1	n0					5	M(n3~n0)←B
	LDPX	MX, i	1	1	1	0	0	1	1	0	i3	i2	i1	i0					5	M(X)←i3~i0, X←X+1
		r, q	1	1	1	0	1	1	1	0	r1	r0	q1	q0					5	r←q, X←X+1
	LDPY	MY, i	1	1	1	0	0	1	1	1	i3	i2	i1	i0					5	M(Y)←i3~i0, Y←Y+1
		r, q	1	1	1	0	1	1	1	1	r1	r0	q1	q0					5	r←q, Y←Y+1
	LBPX	MX, l	1	0	0	1	l7	l6	l5	l4	l3	l2	l1	l0					5	M(X)←l3~l0, M(X+1)←l7~l4, X←X+2
Flag operation instructions	SET	F, i	1	1	1	1	0	1	0	0	i3	i2	i1	i0	↑	↑	↑	↑	7	F←F∨i3~i0
	RST	F, i	1	1	1	1	0	1	0	1	i3	i2	i1	i0	↓	↓	↓	↓	7	F←F∧i3~i0
	SCF		1	1	1	1	0	1	0	0	0	0	0	1				↑	7	C←1
	RCF		1	1	1	1	0	1	0	1	1	1	1	0				↓	7	C←0
	SZF		1	1	1	1	0	1	0	0	0	0	1	0			↑		7	Z←1
	RZF		1	1	1	1	0	1	0	1	1	1	0	1			↓		7	Z←0
	SDF		1	1	1	1	0	1	0	0	0	1	0	0		↑			7	D←1 (Decimal Adjuster ON)
	RDF		1	1	1	1	0	1	0	1	1	0	1	1		↓			7	D←0 (Decimal Adjuster OFF)
	EI		1	1	1	1	0	1	0	0	1	0	0	0	↑				7	I←1 (Enables Interrupt)
	DI		1	1	1	1	0	1	0	1	0	1	1	1	↓				7	I←0 (Disables Interrupt)
Stack operation instructions	INC	SP	1	1	1	1	1	1	0	1	1	0	1	1					5	SP←SP+1
	DEC	SP	1	1	1	1	1	1	0	0	1	0	1	1					5	SP←SP-1
	PUSH	r	1	1	1	1	1	1	0	0	0	0	r1	r0					5	SP←SP-1, M(SP)←r
		XP	1	1	1	1	1	1	0	0	0	1	0	0					5	SP←SP-1, M(SP)←XP
		XH	1	1	1	1	1	1	0	0	0	1	0	1					5	SP←SP-1, M(SP)←XH
		XL	1	1	1	1	1	1	0	0	0	1	1	0					5	SP←SP-1, M(SP)←XL
		YP	1	1	1	1	1	1	0	0	0	1	1	1					5	SP←SP-1, M(SP)←YP
		YH	1	1	1	1	1	1	0	0	1	0	0	0					5	SP←SP-1, M(SP)←YH
		YL	1	1	1	1	1	1	0	0	1	0	0	1					5	SP←SP-1, M(SP)←YL
		F	1	1	1	1	1	1	0	0	1	0	1	0					5	SP←SP-1, M(SP)←F
	POP	r	1	1	1	1	1	1	0	1	0	0	r1	r0					5	r←M(SP), SP←SP+1
		XP	1	1	1	1	1	1	0	1	0	1	0	0					5	XP←M(SP), SP←SP+1
		XH	1	1	1	1	1	1	0	1	0	1	0	1					5	XH←M(SP), SP←SP+1
		XL	1	1	1	1	1	1	0	1	0	1	1	0					5	XL←M(SP), SP←SP+1
		YP	1	1	1	1	1	1	0	1	0	1	1	1					5	YP←M(SP), SP←SP+1

Table 2.1.1(c) Instruction sets (3)

Classification	Mne-monic	Operand	Operation Code B A 9 8	7 6 5 4	3 2 1 0	Flag I D Z C	Clock	Operation
Stack operation instructions	POP	YH	1 1 1 1	1 1 0 1	1 0 0 0		5	YH← M(SP), SP← SP+1
		YL	1 1 1 1	1 1 0 1	1 0 0 1		5	YL← M(SP), SP← SP+1
		F	1 1 1 1	1 1 0 1	1 0 1 0	↕ ↕ ↕ ↕	5	F← M(SP), SP← SP+1
	LD	SPH, r	1 1 1 1	1 1 1 0	0 0 r1 r0		5	SPH← r
		SPL, r	1 1 1 1	1 1 1 1	0 0 r1 r0		5	SPL ← r
		r, SPH	1 1 1 1	1 1 1 0	0 1 r1 r0		5	r← SPH
		r, SPL	1 1 1 1	1 1 1 1	0 1 r1 r0		5	r← SPL
Arithmetic instructions	ADD	r, i	1 1 0 0	0 0 r1 r0	i3 i2 i1 i0	★ ↕ ↕	7	r← r+i3~i0
		r, q	1 0 1 0	1 0 0 0	r1 r0 q1 q0	★ ↕ ↕	7	r← r+q
	ADC	r, i	1 1 0 0	0 1 r1 r0	i3 i2 i1 i0	★ ↕ ↕	7	r← r+i3~i0+C
		r, q	1 0 1 0	1 0 0 1	r1 r0 q1 q0	★ ↕ ↕	7	r← r+q+C
	SUB	r, q	1 0 1 0	1 0 1 0	r1 r0 q1 q0	★ ↕ ↕	7	r← r-q
	SBC	r, i	1 1 0 1	0 1 r1 r0	i3 i2 i1 i0	★ ↕ ↕	7	r← r-i3~i0-C
		r, q	1 0 1 0	1 0 1 1	r1 r0 q1 q0	★ ↕ ↕	7	r← r-q-C
	AND	r, i	1 1 0 0	1 0 r1 r0	i3 i2 i1 i0	↕	7	r← r∧i3~i0
		r, q	1 0 1 0	1 1 0 0	r1 r0 q1 q0	↕	7	r← r∧q
	OR	r, i	1 1 0 0	1 1 r1 r0	i3 i2 i1 i0	↕	7	r← r∨i3~i0
		r, q	1 0 1 0	1 1 0 1	r1 r0 q1 q0	↕	7	r← r∨q
	XOR	r, i	1 1 0 1	0 0 r1 r0	i3 i2 i1 i0	↕	7	r← r∀i3~i0
		r, q	1 0 1 0	1 1 1 0	r1 r0 q1 q0	↕	7	r← r∀q
	CP	r, i	1 1 0 1	1 1 r1 r0	i3 i2 i1 i0	↕ ↕	7	r-i3~i0
		r, q	1 1 1 1	0 0 0 0	r1 r0 q1 q0	↕ ↕	7	r-q
	FAN	r, i	1 1 0 1	1 0 r1 r0	i3 i2 i1 i0	↕	7	r∧i3~i0
		r, q	1 1 1 1	0 0 0 1	r1 r0 q1 q0	↕	7	r∧q
	RLC	r	1 0 1 0	1 1 1 1	r1 r0 r1 r0	↕ ↕	7	d3← d2, d2← d1, d1← d0, d0← C, C← d3
	RRC	r	1 1 1 0	1 0 0 0	1 1 r1 r0	↕ ↕	5	d3← C, d2← d3, d1← d2, d0← d1, C← d0
	INC	Mn	1 1 1 1	0 1 1 0	n3 n2 n1 n0	↕ ↕	7	M(n3~n0)← M(n3~n0)+1
	DEC	Mn	1 1 1 1	0 1 1 1	n3 n2 n1 n0	↕ ↕	7	M(n3~n0)← M(n3~n0)-1
	ACPX	MX, r	1 1 1 1	0 0 1 0	1 0 r1 r0	★ ↕ ↕	7	M(X)← M(X)+r+C, X← X+1
	ACPY	MY, r	1 1 1 1	0 0 1 0	1 1 r1 r0	★ ↕ ↕	7	M(Y)← M(Y)+r+C, Y← Y+1
	SCPX	MX, r	1 1 1 1	0 0 1 1	1 0 r1 r0	★ ↕ ↕	7	M(X)← M(X)-r-C, X← X+1
	SCPY	MY, r	1 1 1 1	0 0 1 1	1 1 r1 r0	★ ↕ ↕	7	M(Y)← M(Y)-r-C, Y← Y+1
	NOT	r	1 1 0 1	0 0 r1 r0	1 1 1 1	↕	7	r← r̄

2.2 Program Memory (ROM)

The built-in ROM, a mask ROM for loading the program, has a capacity of 4,096 steps × 12 bits. The program area consists of 16 (0–15) pages × 256 (00H–FFH) steps. After initial reset, the program beginning address is set to bank 0, page 1, step 00H. The interrupt vector is allocated to page 1, steps 02H–0CH.
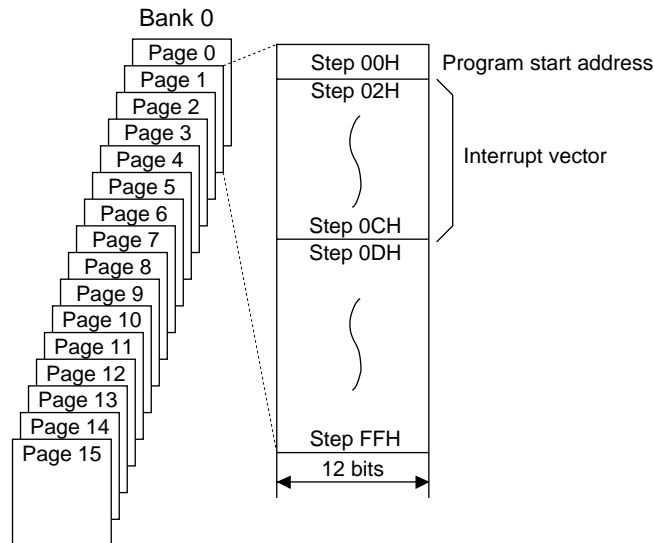

Fig. 2.2.1 Configuration of the built-in ROM

2.3 Data Memory (RAM)

The E0C6007 built-in data memories are configured a general-purpose RAM, display data memory of the LCD, and I/O data memory which controls the peripheral circuit.

General-purpose RAM: 512 words × 4 bits (000H–1FFH)
Display data memory: 160 words × 4 bits (E00H–E4FH, E80H–ECFH)
I/O memory: 33 words × 4 bits (F00H–F7FH)

During programming, take note of the following:

(1) Since the stack area is taken from the RAM area, take care that destruction of stack data due to data writing does not occur. Sub-routine calls or interrupts consume 3 words of the stack area.

(2) RAM address 000H–00FH are memory register areas that are addressed with register pointer RP.

The memory map of the built-in data memory (RAM) and details of the I/O data memory map are shown in Figure 2.3.1 and Tables 2.3.1(a)–(c), respectively.

Note: Memory is not mounted in unused area within the memory map and in memory area not indicated in this chapter. For this reason, normal operation cannot be assured for programs that have been prepared with access to these areas.
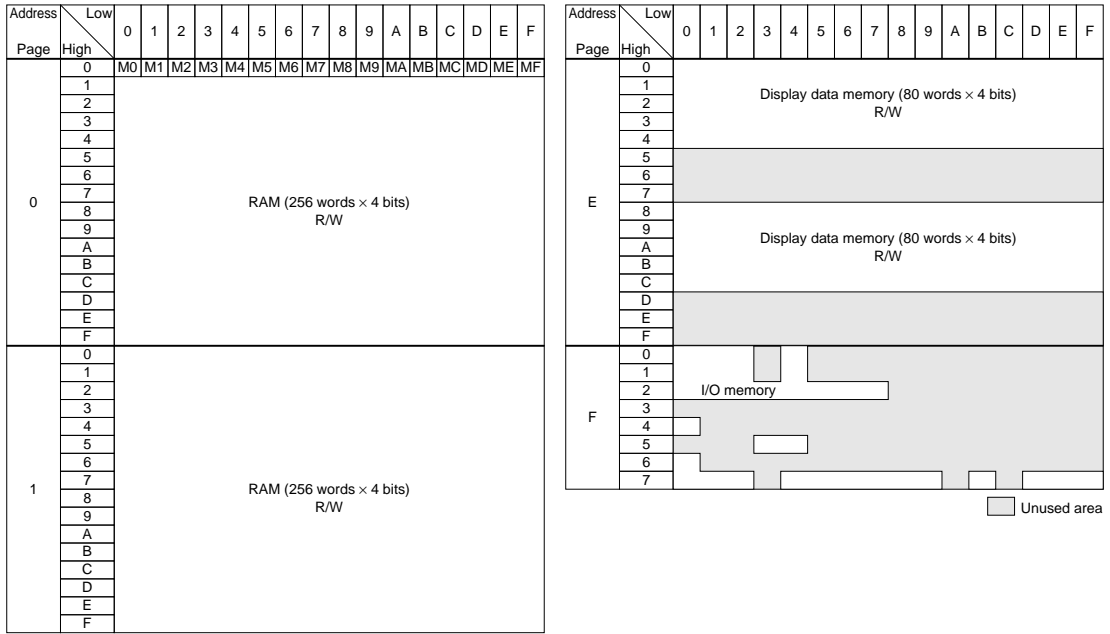
Address Page	Low High	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	0	M0	M1	M2	M3	M4	M5	M6	M7	M8	M9	MA	MB	MC	MD	ME	MF
	1																
	2																
	3																
	4																
	5																
	6																
	7					RAM (256 words × 4 bits)											
	8					R/W											
	9																
	A																
	B																
	C																
	D																
	E																
	F																
1	0																
	1																
	2																
	3																
	4																
	5																
	6																
	7					RAM (256 words × 4 bits)											
	8					R/W											
	9																
	A																
	B																
	C																
	D																
	E																
	F																

Address Page	Low High	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
E	0																
	1					Display data memory (80 words × 4 bits)											
	2					R/W											
	3																
	4																
	5																
	6																
	7																
	8																
	9					Display data memory (80 words × 4 bits)											
	A					R/W											
	B																
	C																
	D																
	E																
	F																
F	0																
	1																
	2	I/O memory															
	3																
	4																
	5																
	6																
	7																

□ Unused area

Fig. 2.3.1 Memory map

Table 2.3.1(a) I/O data memory map (1)

Address	Register D3	Register D2	Register D1	Register D0	Name	Init *1	1	0	Comment
F00H	IT1	IT2	IT8	IT32	IT1 *3	0	Yes	No	Interrupt factor flag (clock timer 1 Hz)
					IT2 *3	0	Yes	No	Interrupt factor flag (clock timer 2 Hz)
	R				IT8 *3	0	Yes	No	Interrupt factor flag (clock timer 8 Hz)
					IT32 *3	0	Yes	No	Interrupt factor flag (clock timer 32 Hz)
F01H	0	0	ISW1	ISW0	0 *4	– *2			
					0 *4	– *2			
	R				ISW1 *3	0	Yes	No	Interrupt factor flag (stopwatch 1 Hz)
					ISW0 *3	0	Yes	No	Interrupt factor flag (stopwatch 10 Hz)
F02H	0	0	0	IPT	0 *4	– *2			
					0 *4	– *2			
	R				0 *4	– *2			
					IPT *3	0	Yes	No	Interrupt factor flag (programmable timer)
F04H	0	0	0	IK0	0 *4	– *2			
					0 *4	– *2			
	R				0 *4	– *2			
					IK0 *3	0	Yes	No	Interrupt factor flag (K00–K03)
F10H	EIT1	EIT2	EIT8	EIT32	EIT1	0	Enable	Mask	Interrupt mask register (clock timer 1 Hz)
					EIT2	0	Enable	Mask	Interrupt mask register (clock timer 2 Hz)
	R/W				EIT8	0	Enable	Mask	Interrupt mask register (clock timer 8 Hz)
					EIT32	0	Enable	Mask	Interrupt mask register (clock timer 32 Hz)
F11H	0	0	EISW1	EISW0	0 *4	– *2			
					0 *4	– *2			
	R	R	R/W	R/W	EISW1	0	Enable	Mask	Interrupt mask register (stopwatch 1 Hz)
					EISW0	0	Enable	Mask	Interrupt mask register (stopwatch 10 Hz)
F12H	0	0	0	EIPT	0 *4	– *2			
					0 *4	– *2			
	R	R	R	R/W	0 *4	– *2			
					EIPT	0	Enable	Mask	Interrupt mask register (programmble timer)
F14H	EIK03	EIK02	EIK01	EIK00	EIK03	0	Enable	Mask	Interrupt mask register (K03)
					EIK02	0	Enable	Mask	Interrupt mask register (K02)
	R/W				EIK01	0	Enable	Mask	Interrupt mask register (K01)
					EIK00	0	Enable	Mask	Interrupt mask register (K00)
F20H	TM3	TM2	TM1	TM0	TM3	0			Clock timer data (16 Hz)
					TM2	0			Clock timer data (32 Hz)
	R				TM1	0			Clock timer data (64 Hz)
					TM0	0			Clock timer data (128 Hz)
F21H	TM7	TM6	TM5	TM4	TM7	0			Clock timer data (1 Hz)
					TM6	0			Clock timer data (2 Hz)
	R				TM5	0			Clock timer data (4 Hz)
					TM4	0			Clock timer data (8 Hz)
F22H	SWL3	SWL2	SWL1	SWL0	SWL3	0			⌐ MSB
					SWL2	0			Stopwatch timer
	R				SWL1	0			1/100 sec data (BCD)
					SWL0	0			⌐ LSB
F23H	SWH3	SWH2	SWH1	SWH0	SWH3	0			⌐ MSB
					SWH2	0			Stopwatch timer
	R				SWH1	0			1/10 sec data (BCD)
					SWH0	0			⌐ LSB
F24H	PT3	PT2	PT1	PT0	PT3	X *5			⌐ MSB
					PT2	X *5			
	R				PT1	X *5			Programmable timer data (low-order)
					PT0	X *5			⌐ LSB
F25H	PT7	PT6	PT5	PT4	PT7	X *5			⌐ MSB
					PT6	X *5			
	R				PT5	X *5			Programmable timer data (high-order)
					PT4	X *5			⌐ LSB

*1   Initial value following initial reset   *2   Not set in the circuit
*3   Reset (0) immediately after being read   *4   Always "0" when being read
*5   Undefined

Table 2.3.1(b) I/O data memory map (2)

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
F26H	RD3	RD2	RD1	RD0	RD3	X *5			MSB
					RD2	X *5			Programmable timer
	R/W				RD1	X *5			reload data (low-order)
					RD0	X *5			LSB
F27H	RD7	RD6	RD5	RD4	RD7	X *5			MSB
					RD6	X *5			Programmable timer
	R/W				RD5	X *5			reload data (high-order)
					RD4	X *5			LSB
F40H	K03	K02	K01	K00	K03	– *2	High	Low	
					K02	– *2	High	Low	
	R				K01	– *2	High	Low	Input port (K00–K03)
					K00	– *2	High	Low	
F53H	R33	R32	0	0	R33	X *5	High	Low	Output port (R33)
							Off	On	PTCLK output
	R/W		R		R32	X *5	High	Low	Output port (R32)
					0 *4	– *2			
					0 *4	– *2			
F54H	R43	R42	R41	R40	R43	1	High	Low	Output port (R43)
							Off	On	Buzzer output (BZ)
	R/W				R42	1	High	Low	Output port (R42)
							Off	On	Clock output (FOUT)
							*6	*6	[Buzzer inverted output (#BZ)]
					R41	1	High	Low	Output port (R41)
					R40	1	High	Low	Output port (R40)
							Off	On	Clock inverted output (#FOUT)
F60H	P03	P02	P01	P00	P03	X *5	High	Low	
					P02	X *5	High	Low	
	R/W				P01	X *5	High	Low	I/O port (P00–P03)
					P00	X *5	High	Low	
F70H	CLKCHG	OSCC	VSC1	VSC0	CLKCHG	0	OSC3	OSC1	CPU system clock switch
					OSCC	0	On	Off	OSC3 oscillation On/Off
	R/W				VSC1	0			
					VSC0	0			CPU operating voltage switch
F71H	ALOFF	ALON	LDUTY	HLMOD	ALOFF	1	All off	Normal	All LCD dots fade out control
					ALON	0	All on	Normal	All LCD dots displayed control
	R/W				LDUTY	0	1/8	1/16	LCD drive duty switch
					HLMOD	0	HLMOD	Normal	Heavy load protection mode
F72H	LC3	LC2	LC1	LC0	LC3	X *5			LCD contrast adjustment
					LC2	X *5			LC3–LC0 = 0 light
	R/W				LC1	X *5			:
					LC0	X *5			LC3–LC0 = 15 dark
F74H	SHOTPW	BZFQ2	BZFQ1	BZFQ0	SHOTPW	0	62.5 ms	31.25 ms	1-shot buzzer pulse width
					BZFQ2	0			
	R/W				BZFQ1	0			Buzzer frequency selection
					BZFQ0	0			
F75H	BZSHOT	ENVRST	ENVRT	ENVON	BZSHOT	0	Trigger	–	1-shot buzzer trigger (W)
							BUSY	READY	Status (R)
	W / R	W	R/W		ENVRST	RESET	Reset	–	Envelope reset
					ENVRT	0	1.0 sec	0.5 sec	Envelope cycle selection
					ENVON	0	On	Off	Envelope On/Off
F76H	0	0	TMRST	WDRST	0 *4	– *2			
					0 *4	– *2			
	R		W		TMRST *4	Reset	Reset	–	Clock timer reset
					WDRST	Reset	Reset	–	Watchdog timer reset
F77H	0	0	SWRST	SWRUN	0 *4	– *2			
					0 *4	– *2			
	R	W	R/W		SWRST *4	Reset	Reset	–	Stopwatch timer reset
					SWRUN	0	Run	Stop	Stopwatch timer Run/Stop

*1 Initial value following initial reset   *2 Not set in the circuit
*3 Reset (0) immediately after being read   *4 Always "0" when being read   *5 Undefined
*6 When selecting options enclosed in brackets [ ] as output option, the output register will function as register only and will not affect the individual outputs.

Table 2.3.1(c) I/O data memory map (3)

Address	Register D3	Register D2	Register D1	Register D0	Name	Init *1	1	0	Comment
F78H	0	0	PTRST	PTRUN	0 *4	– *2			
					0 *4	– *2			
	R	R	W	R/W	PTRST *4	Reset	Reset	–	Programmable timer reset
					PTRUN	0	Run	Stop	Programmable timer Run/Stop
F79H	PTCOUT	PTC2	PTC1	PTC0	PTCOUT	0	On	Off	Programmable timer clock output
					PTC2	0			
	R/W	R/W	R/W	R/W	PTC1	0			Programmable timer input clock selection
					PTC0	0			
F7BH	HZR3	0	0	0	HZR3	0	Output	High-Z	R32–R33 output high-impedance control
					0 *4	– *2			
	R/W	R	R	R	0 *4	– *2			
					0 *4	– *2			
F7DH	0	0	0	IOC0	0 *4	– *2			
					0 *4	– *2			
	R	R	R	R/W	0 *4	– *2			
					IOC0	0	Output	Input	I/O control (P00–P03)
F7EH	0	0	0	PUP0	0 *4	– *2			
					0 *4	– *2			
	R	R	R	R/W	0 *4	– *2			
					PUP0	0	Off	On	I/O pull up resistor On/Off (P00–P03)
F7FH	0	0	0	LCDOFF	0 *4	– *2			
					0 *4	– *2			
	R	R	R	R/W	0 *4	– *2			
					LCDOFF	1	Normal	Off	LCD display control

*1 Initial value following initial reset
*2 Not set in the circuit
*3 Reset (0) immediately after being read
*4 Always "0" when being read
*5 Undefined

CHAPTER 3 POWER SOURCE

3.1 Power Supply System

The E0C6007 operating power voltage is as follows:

2.2–5.5 V (Min. 1.8 V, when OSC3 oscillation circuit is not used)

The E0C6007 operates when a single power supply within the above range is applied between V_{DD} and V_{SS}. Even if the voltage is not within the above range necessary for the internal circuits, the IC itself can generate the following built-in power circuits.

Table 3.1.1 Power supply circuits

Circuit	Power supply circuit	Output voltage
Oscillation circuit and internal circuits	Regulated voltage circuit	V_{S1}
LCD driver	LCD system voltage circuit	V_{L1}–V_{L5}

Notes: • V_{L3} is used only when the driving voltage of the LCD system will be supplied externally (1/5 bias); when using the internal LCD system voltage circuit (1/4 bias), it should be shorted with V_{L2}.

  • See "13 Electrical Characteristics" for voltage values.
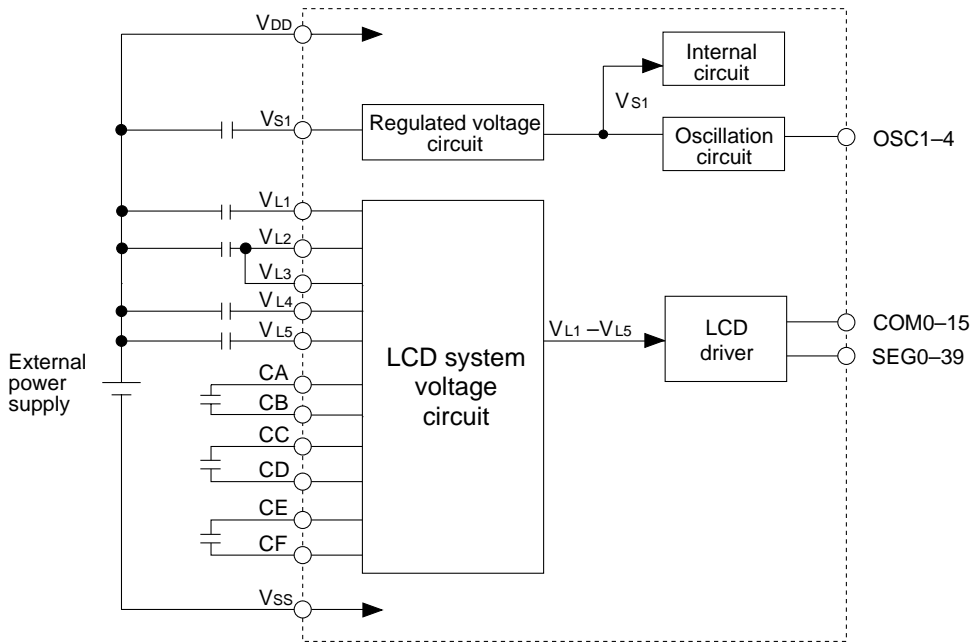
Fig. 3.1.1 Configuration of power supply

3.2 Heavy Load Protection Mode

Because the load of the battery in the E0C6007 becomes heavy due to the buzzer, lamp, and other features, it has been equipped with heavy load protection function in case of power voltage drop. This functions works in the heavy load protection mode.

Based on the workings of the heavy load protection function, the E0C6007 realizes operation at 2.2 V (Min. 1.8 V, when OSC3 oscillation circuit is not used) source voltage.

When driving heavy loads, set the IC to heavy load protection mode.

At the normal mode, the LCD system regulated voltage is created with V_{L2}; V_{L1} is 1/2 reduced V_{L2} voltage while V_{L4} and V_{L5} are created by boosting to 1.5 and 2 times voltages, respectively. On the other hand, at the heavy load protection mode, the regulated voltage is V_{L1}; V_{L2}, V_{L4}, and V_{L5} are created by boosting to 2, 3 and 4 times voltages. Because of this, the consumed current becomes greater than that in the normal mode, be careful not to set the heavy load protection unless necessary.

The LCD system voltage modes are shown in Table 3.2.1.

Table 3.2.1 LCD system voltage mode

Terminal	Normal mode	Heavy load protection mode
V_{L1}	1/2 V_{L2}	V_{L1} regulated voltage
V_{L2}	V_{L2} regulated voltage	2 V_{L1}
V_{L4}	3/2 V_{L2}	3 V_{L1}
V_{L5}	4/2 V_{L2}	4 V_{L1}

3.2.1 Control of heavy load protection mode

The control register for the heavy load protection mode are explained below.

Table 3.2.1.1 Control register for heavy load protection mode

Address	Register				Name	Init	1	0	Comment
	D3	D2	D1	D0					
F71H	ALOFF	ALON	LDUTY	HLMOD	ALOFF	1	All off	Normal	All LCD dots fade out control
					ALON	0	All on	Normal	All LCD dots displayed control
	R/W				LDUTY	0	1/8	1/16	LCD drive duty switch
					HLMOD	0	HLMOD	Normal	Heavy load protection mode

HLMOD (F71H [D0], R/W)

Controls the heavy load protection mode.

When "1" is written: Heavy load protection mode is set
When "0" is written: Heavy load protection mode is released
           Reading: Valid

Conversion to heavy load protection mode is done by writing "1" to HLMOD while cancellation of this mode is done by writing "0".

At initial reset, the mode is set to "0" (heavy load protection mode cancellation).

3.2.2 Programming notes

(1) When driving heavy loads, set it to heavy load protection mode. Unless it is necessary, be careful not to set the heavy load protection mode with the software.

(2) Perform heavy load driving only after setting up at least 1 ms wait time through the software, after switching to the heavy load protection mode. (See Figure 3.2.2.1.)

(3) When the heavy load protection mode is to canceled after completion of heavy load driving, set up at least 2 seconds wait time through the software. (See Figure 3.2.2.1.)
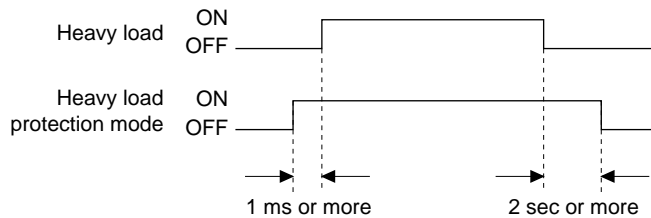
Fig. 3.2.2.1 Control timing for heavy load protection mode

3.3 CPU Operating Voltage Change

During operation, E0C6007 can change OSC1 and OSC3 system clocks through the software, and operation at clock mode or high-speed mode is then possible. In this case, to obtain stable operating, operating voltage V_{S1} of the internal circuit is changed through the software. For details, see Chapter 5, "Oscillation Circuit".

CHAPTER 4 INITIAL RESET

4.1 Initial Reset Factors

The E0C6007 requires initial reset function to initialize the circuits.

There are three types of initial reset factors:

(1) Initial reset by power-on reset

(2) External reset through low level input to the #RESET terminal

(3) External initial reset by simultaneous low level input of K00–K03 terminals (mask option)

(4) Initial reset by watchdog timer

Note: The E0C6007 must be reset after turning power on using the initial reset factor (1) or (2).

Figure 4.1.1 shows the configuration of the initial reset circuit.
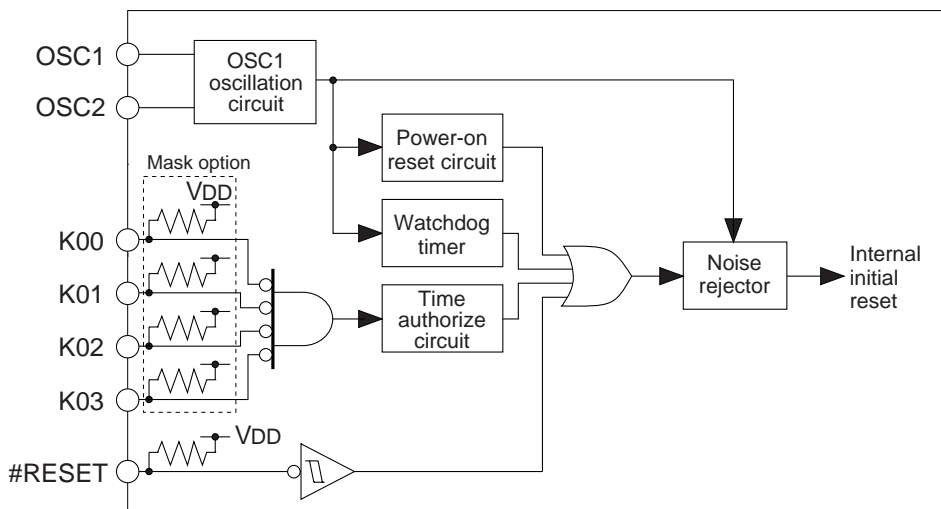
Fig. 4.1.1 Configuration of initial reset circuit

4.1.1 Power-on reset circuit

The power-on reset circuit outputs the initial reset signal at power-on until the oscillation circuit starts oscillating.

Note: The power-on reset circuit may not work properly due to unstable or lower voltage input.
       The following two initial reset method are recommended to generate the initial reset signal.

4.1.2 External initial reset by the #RESET terminal

An initial reset can be executed externally by setting the reset terminal to high level. This high level must be maintained for at least 2 ms (in case oscillation frequency f_{OSC1} = 32.768 kHz), because the initial reset circuit contains a noise rejector. When the reset terminal goes low, the CPU will start operating.

4.1.3 External initial reset by simultaneous low level input of K00–K03 terminals

Initial reset may be done by simultaneously providing low level input externally to the input port (K00–K03) selected by mask option. Because the initial reset circuit has time authorize circuit built-in, keep the specified input port terminal at Low level for at least 2 seconds (in case oscillation frequency $fosc_1 = 32.768$ kHz). The input port combination which can be selected from the mask option are as follows:

- Not use
- K00∗K01
- K00∗K01∗K02
- K00∗K01∗K02∗K03

4.1.4 Initial reset by watchdog timer

If the CPU runs away for some reason, the watchdog timer will detect this situation and output an initial reset signal. See "4.2 Watchdog Timer" for details.

4.1.5 Internal register at initial resetting

The CPU is initialized by initial resetting as follows:

Table 4.1.5.1 Initial values

CPU Core			
Name	Symbol	Bit size	Initial value
Program counter step	PCS	8	00H
Program counter page	PCP	4	1H
Program counter bank	PCB	1	0
New page pointer	NPP	4	1H
New bank pointer	NBP	1	0
Stack pointer	SP	8	Undefined
Index register X	X	12	Undefined
Index register Y	Y	12	Undefined
Register pointer	RP	4	Undefined
General-purpose register A	A	4	Undefined
General-purpose register B	B	4	Undefined
Interrupt flag	I	1	0
Decimal flag	D	1	0
Zero flag	Z	1	Undefined
Carry flag	C	1	Undefined

Peripheral Circuits		
Name	Bit size	Initial value
RAM	512×4	Undefined
Display memory	160×4	Undefined
Other peripheral circuits	–	∗

∗ See Tables 2.3.1(a)–(c).

4.2 Watchdog Timer

4.2.1 Configuration of watchdog timer

E0C6007 has a built-in watchdog timer with OSC1 (clock timer 1 Hz signal) basic oscillation. The watchdog timer needs to be reset periodically through the software, and if not reset within 3–4 seconds, it automatically generates an initial reset signal to the CPU.

Figure 4.2.1.1 shows the configuration of the watchdog timer.
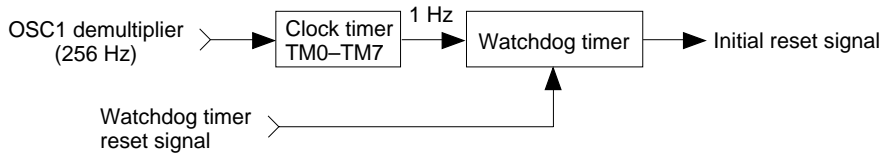
Fig. 4.2.1.1 Configuration of watchdog timer

By resetting the watchdog timer during the program's main routine, program runaways which do not pass the watchdog timer processing during main routine can be detected.

Note, however, that the watchdog timer operates even during HALT such that if the HALT condition continues for 3–4 seconds, it is re-initiated through initial resetting.

4.2.2 Control of watchdog timer

The control register of the watchdog timer is explained below.

Table 4.2.2.1 Control register of watchdog timer

Address	Register				Name	Init	1	0	Comment
	D3	D2	D1	D0					
F76H	0	0	TMRST	WDRST	0	–			
					0	–			
	R		W		TMRST	Reset	Reset	–	Clock timer reset
					WDRST	Reset	Reset	–	Watchdog timer reset

WDRST (F76H [D0], W)

This bit resets the watchdog timer.

   When "1" is written: Watchdog timer reset
   When "0" is written: No operation
           Reading: Always "0"

By writing "1" on WDRST, the watchdog timer is reset, after which it is immediately restarted. Writing "0" will mean no operation.

Because this bit is only for writing, it is always set to "0" during reading.

4.2.3 Programming notes

(1) The watchdog timer must reset within 3-second cycles by the software.

(2) When the clock timer is reset (TMRST ← "1"), the watchdog timer is counted up; reset the watchdog immediately after if necessary.

CHAPTER 5 OSCILLATION CIRCUIT

5.1 Configuration of Oscillation Circuit

The E0C6007 has two oscillation circuits (OSC1 and OSC3). OSC1 is either a crystal or a CR oscillation circuit that supplies the operating clock to the CPU and peripheral circuits. OSC3 is either a CR or a ceramic oscillation circuit. When processing with the E0C6007 requires high-speed operation, the CPU operating clock can be switched from OSC1 to OSC3 by the software. To stabilize operation of the internal circuits, the operating voltage V_{S1} must be switched according to the oscillation circuit to be used. Figure 5.1.1 is the block diagram of this oscillation system.
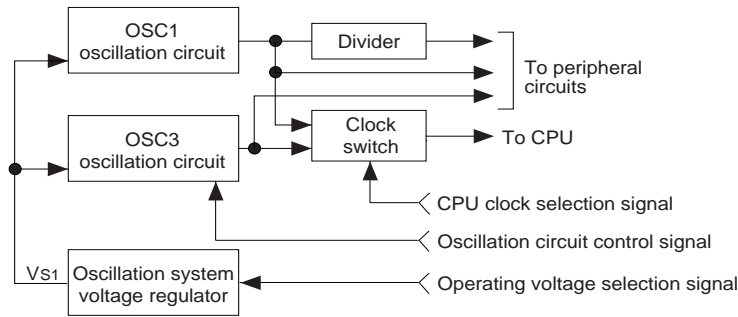
Fig. 5.1.1 Oscillation system block diagram

5.2 OSC1 Oscillation Circuit

The OSC1 oscillation circuit generates the main clock for the CPU and the peripheral circuits. Either the crystal oscillation circuit or the CR oscillation circuit can be selected as the circuit type by mask option. Figure 5.2.1 shows the configuration of the OSC1 oscillation circuit.

(1) Crystal oscillation circuit

(2) CR oscillation circuit
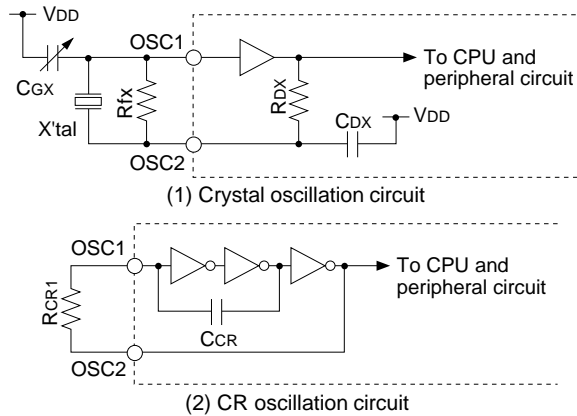
Fig. 5.2.1 OSC1 oscillation circuit

As shown in Figure 5.2.1, the crystal oscillation circuit can be configured simply by connecting the crystal oscillator (X'tal) of 32.768 kHz (Typ.) and the feedback resistor Rfx (10 MΩ) between the OSC1 and OSC2 terminals and the trimmer capacitor (C_{GX}) between the OSC1 and V_{DD} terminals when crystal oscillation is selected.

When CR oscillation is selected by mask option, connect the resistor R_{CR1} between the OSC1 and OSC2 terminals. See "13 Electrical Characteristics" for resistance value of R_{CR1}.

Notes: • The current consumption of CR oscillation is larger than crystal oscillation.

• Be aware that the CR oscillation frequency changes slightly.
Pay special attention to the circuits that use f_{OSC1} as the source clock, such as the timer (time lag), the LCD frame frequency (display quality, flicker in low frequency) and the sound generator (sound quality).

5.3 OSC3 Oscillation Circuit

The E0C6007 has built-in the OSC3 oscillation circuit that generates the CPU's sub-clock (Max. 2 MHz) for high speed operation. The mask option enables selection of either the CR or ceramic oscillation circuit. When CR oscillation is selected, only a resistance is required as an external element. When ceramic oscillation is selected, a ceramic oscillator and two capacitors (gate and drain capacitance) are required.

Figure 5.3.1 shows the configuration of the OSC3 oscillation circuit.

(1) CR oscillation circuit

(2) Ceramic oscillation circuit
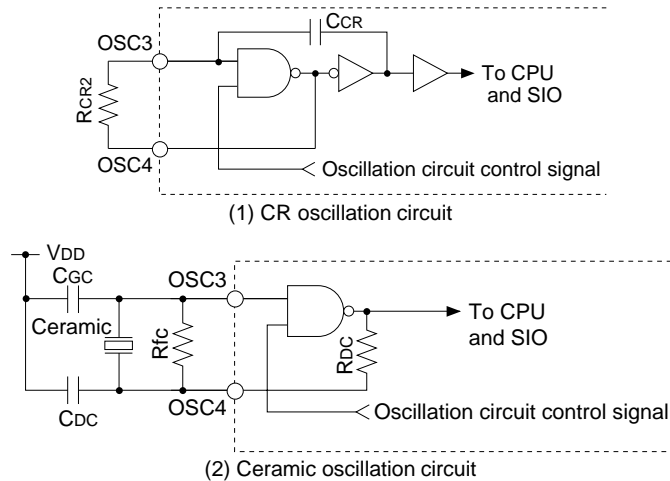
Fig. 5.3.1 OSC3 oscillation circuit

As shown in Figure 5.3.1, the CR oscillation circuit can be configured simply by connecting the resistor R_{CR2} between the OSC3 and OSC4 terminals when CR oscillation is selected. See "13 Electrical Characteristics" for resistance value of R_{CR2}.

When ceramic oscillation is selected, the ceramic oscillation circuit can be configured by connecting the ceramic oscillator (Max. 2 MHz) and feedback resistor Rfc (about 1 MΩ) between the OSC3 and OSC4 terminals, capacitor C_{GC} between the OSC3 and OSC4 terminals, and capacitor C_{DC} between the OSC4 and V_{DD} terminals. For both C_{GC} and C_{DC}, connect capacitors that are about 100 pF. To reduce current consumption of the OSC3 oscillation circuit, oscillation can be stopped by the software (OSCC register).

When the OSC3 oscillation circuit is not used, connect the OSC3 terminal to V_{S1}.
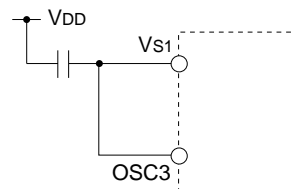
Fig. 5.3.2 Connection diagram when the OSC3 oscillation circuit is unused

5.4 Operating Voltage Change

E0C6007 can change OSC1 and OSC3 system clocks through the software. In this case, to obtain stable operation, operating voltage V_{S1} of the internal circuit is changed through the software.
Likewise, when selecting OSC1 as the system clock, there is need to change operating voltage V_{S1} according to the value of the power voltage (V_{DD}–V_{SS}).
Oscillation frequency and the corresponding operating voltage V_{S1} are shown in Table 5.4.1.

Table 5.4.1 Oscillation frequency and operating voltage

Oscillation frequency	Oscillation circuit	Operating voltage V_{S1}
32.768 kHz	OSC1	-1.2 V or -2.1 V
1 MHz	OSC3	-2.1 V
2 MHz	OSC3	-3.0 V

The V_{DD} reference voltage is used as the operating voltage V_{S1}.
When OSC3 is to be used as the CPU system clock, change the operating voltage V_{S1} accordingly through the software and then turn the OSC3 oscillation ON and switch the clock frequency.
If the OSC3 oscillation frequency is to be fixed around 1 MHz, set the operating voltage to -2.1 V; at 2 MHz, set the operating voltage to -3.0 V.
Moreover, when the CPU is to be operated with OSC1, set the operating voltage to -1.2 V if the power voltage is less than 3.1 V (V_{DD}–V_{SS} < 3.1 V); set the operating voltage to -2.1 V if the voltage is 3.1 V or more (V_{DD}–V_{SS} ≥ 3.1 V). However, it can be used fixed at -1.2 V (at OSC1 operation) for power whose initial value is 3.6 V or less as in lithium batteries.

Note: Switching V_{S1} when the power source voltage is lower than the set voltage may cause misoperation.

5.5 Clock Frequency and Instruction Execution Time

Table 5.5.1 shows the instruction execution time according to each frequency of the system clock.

Table 5.5.1 Clock frequency and instruction execution time

Clock frequency	Instruction execution time (μs)		
	5-clock instruction	7-clock instruction	12-clock instruction
32.768 kHz	152.6	213.6	366.2
1 MHz	5.0	7.0	12.0
2 MHz	2.5	3.5	6.0

5.6 Control of Oscillation Circuit

The control registers for the oscillation circuit are explained below.

Table 5.6.1 Control registers of oscillation circuit

Address	Register								Comment
	D3	D2	D1	D0	Name	Init	1	0	
F70H	CLKCHG	OSCC	VSC1	VSC0	CLKCHG	0	OSC3	OSC1	CPU system clock switch
					OSCC	0	On	Off	OSC3 oscillation On/Off
	R/W				VSC1	0			CPU operating voltage switch
					VSC0	0			

VSC0 and VSC1 (F70H [D0 and D1], R/W)

Switches the operating voltage of the internal circuit in accordance to the oscillation frequency and power source voltage.

The corresponding setting description is shown in Table 5.6.2.

Table 5.6.2 Corresponding between oscillation frequency, power source voltage, and operating voltage (V_{S1})

VSC1	VSC0	V_{S1}	Oscillation circuit	Oscillation frequency	Power source voltage (V_{DD}–V_{SS})
0	0	-1.2 V	OSC1	32.768 kHz	Under 3.1 V
0	1	-2.1 V	OSC1	32.768 kHz	3.1 V or more (∗)
0	1	-2.1 V	OSC3	1 MHz	2.2 V or more
1	×	-3.0 V	OSC3	2 MHz	3.1 V or more

The V_{DD} reference voltage is used as the operating voltage V_{S1}.

There is no need to set the (∗) state with regards to power whose initial value is 3.6 V or less as in lithium batteries.

VSC1 and VSC0 are set to "0" at initial reset.

Notes: • When switching V_{S1} from -1.2 V (for OSC1 crystal oscillation circuit) to -3.0 V (for OSC3 oscillation circuit), or vice versa, be sure to hold the -2.1 V setting for more than 5 ms first for power voltage stabilization.

$$(\text{VSC1, VSC0}) = (0, 0) \rightarrow (0, 1) \rightarrow 5 \text{ ms WAIT} \rightarrow (1, \times)$$
$$= (1, \times) \rightarrow (0, 1) \rightarrow 5 \text{ ms WAIT} \rightarrow (0, 0)$$

$$= (0, 0) \rightarrow (1, \times) \text{ is prohibited}$$
$$= (1, \times) \rightarrow (0, 0) \text{ is prohibited}$$

• When CR oscillation has been selected by the mask option as OSC1, V_{S1} becomes -2.1 V even when VSC1 = VSC0 = 0 and will never become -1.2 V. In addition, since the current consumption is great for CR oscillation compared with the quartz crystal oscillation, when low power consumption is required, you should select quartz crystal oscillation as OSC1.

OSCC (F70H [D2], R/W)

Controls the oscillation of the OSC3 oscillation circuit.

When "1" is written: OSC3 oscillation ON
When "0" is written: OSC3 oscillation OFF
          Reading: Valid

When high-speed operation of the CPU is required, OSCC is set to "1"; otherwise, set it to "0" to minimize power current consumption.

At initial reset, OSCC is set to "0".

Note: It takes 5 ms for the OSC3 oscillation circuit to stabilize after oscillation turns ON. Since oscillation stabilization time differs according to external oscillation terminal and usage conditions, set the stand-by time with enough allowance when switching the clock frequency.

CLKCHG (F70H [D3], R/W)
Selects the CPU operating clock.

  When "1" is written: OSC3 clock is selected
  When "0" is written: OSC1 clock is selected
            Reading: Valid

When assigning OSC3 as the CPU operating clock, set CLKCHG to "1"; when assigning OSC1, set it to "0".
At initial reset, CLKCHG is set to "0".

Note: When switching the CPU operating clock from OSC1 to OSC3, follow the flow chart shown in Figure 5.6.1 and then proceed with software processing.
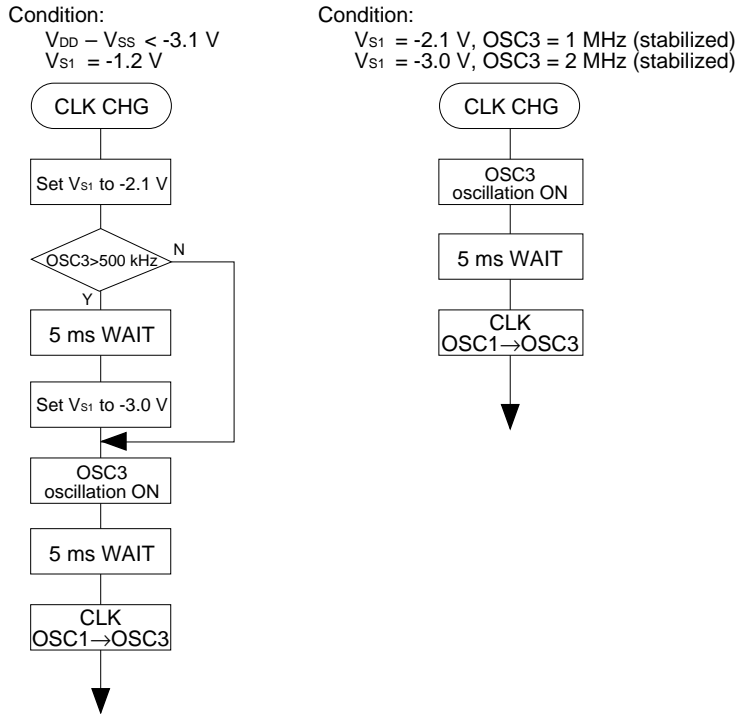
Condition:
  $V_{DD} - V_{SS} < -3.1$ V
  $V_{S1} = -1.2$ V

Condition:
  $V_{S1} = -2.1$ V, OSC3 = 1 MHz (stabilized)
  $V_{S1} = -3.0$ V, OSC3 = 2 MHz (stabilized)

(CLK CHG)

Set V_{S1} to -2.1 V

< OSC3>500 kHz > N

Y

5 ms WAIT

Set V_{S1} to -3.0 V

OSC3 oscillation ON

5 ms WAIT

CLK OSC1→OSC3

(CLK CHG)

OSC3 oscillation ON

5 ms WAIT

CLK OSC1→OSC3

Fig. 5.6.1 CPU operating clock control flow

5.7 Programming Notes

(1) When high-speed operation of the CPU is not required, observe the following reminders to minimize power current consumption.

Set the CPU operating clock to OSC1.
Turn the OSC3 oscillation OFF.
Set the internal operating voltage (V_{S1}) to -1.2 V or -2.1 V.

(2) When the CPU is to be operated with OSC1, set the operating voltage to -1.2 V if the power voltage is less than 3.1 V (V_{DD}–V_{SS} < 3.1 V); set the operating voltage to -2.1 V if the voltage is 3.1 V or more (V_{DD}–V_{SS} ≥ 3.1 V). Moreover, because -1.2 V will be set during initial reset, be sure to execute the previous process at the beginning of the initial routine. Note, however, that it can be used fixed at 1.2 V (at OSC1 operation) for power whose initial value is 3.6 V or less as in lithium batteries.

(3) When switching V_{S1} from -1.2 V (for OSC1 crystal oscillation circuit) to -3.0 V (for OSC3 oscillation circuit), or vice versa, be sure to hold the -2.1 V setting for more than 5 ms first for power voltage stabilization.

$$(VSC1, VSC0) = (0, 0) \rightarrow (0, 1) \rightarrow 5 \text{ ms WAIT} \rightarrow (1, \times)$$
$$= (1, \times) \rightarrow (0, 1) \rightarrow 5 \text{ ms WAIT} \rightarrow (0, 0)$$

$$= (0, 0) \rightarrow (1, \times) \text{ is prohibited}$$
$$= (1, \times) \rightarrow (0, 0) \text{ is prohibited}$$

(4) When switching the CPU operating clock from OSC1 to OSC3, follow the flow chart shown in Figure 5.6.1 and then proceed with software processing.

(5) Use separate instructions to switch the clock from OSC3 to OSC1 and turn the OSC3 oscillation OFF. Simultaneous processing with a single instruction may cause malfunction of the CPU.

CHAPTER 6 INPUT/OUTPUT PORTS

6.1 Input Port (Kxx)

6.1.1 Configuration of input ports

The E0C6007 has 4 bits of general input ports (K00–K03) built-in.
Figure 6.1.1.1 shows the configuration of the input port.
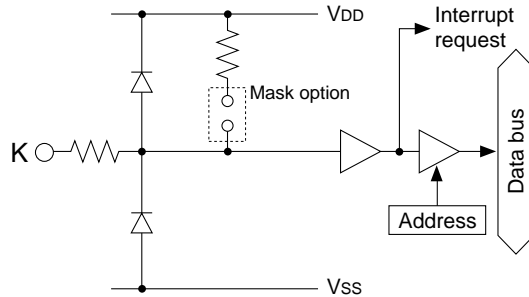
Fig. 6.1.1.1 Configuration of input port

The input port pin K03 is used as the clock input pins for the programmable timer. See "8.3 Programmable Timer" for details.

6.1.2 Mask option

The input ports (K00–K03) are provided with built-in pull up resistor the use of which may be selected for every bit with the mask option.
Selection of "Pull up resistor enable" with the mask option suits input from the push switch, key matrix, and so forth. When changing the input port from low level to high level with a pull up resistor, a delay in the waveform rise time will occur depending on the time constant of the pull up resistor and input gate capacity. Hence, when reading data from the input port, set an appropriate waiting time. Care is particularly required for key matrix configuration scanning. For reference, approximately 500 μs waiting time is required.
When "Pull up resistor disabled" is selected, the port can be used for slide switch input and interfacing with other LSIs. In this case, take care that floating state does not occur.

6.1.3 Interrupt function

All four bits of the input ports K00–K03 provide the interrupt function.
Whether to mask the interrupt function can be selected individually for all four bits by the software.
Figure 6.1.3.1 shows the configuration of the input (K00–K03) interrupt circuit.
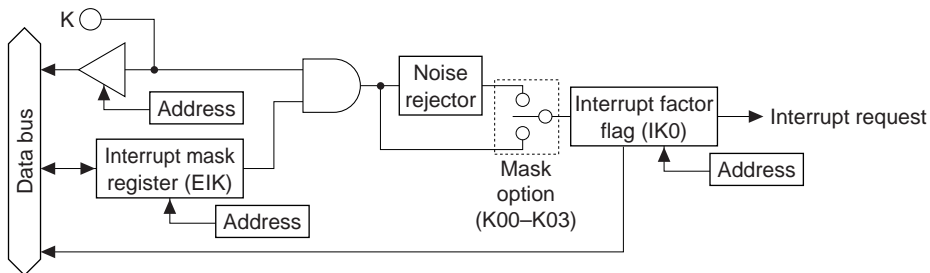
Fig. 6.1.3.1 Configuration of input (K00–K03) interrupt circuit

The interrupt mask registers (EIK00–EIK03) enable or mask the interrupt generation of the corresponding input port K00–K03. When an input signal which is not masked goes low, the interrupt factor flag (IK0) is set to "1" and an interrupt occurs at the falling edge of the input signal.

6.1.4 Control of input ports

The control registers for the input ports are explained below.

Table 6.1.4.1 Control registers of input ports

Address	Register				Name	Init	1	0	Comment
	D3	D2	D1	D0					
F04H	0	0	0	IK0	0	–			
					0	–			
	R				0	–			
					IK0	0	Yes	No	Interrupt factor flag (K00–K03)
F14H	EIK03	EIK02	EIK01	EIK00	EIK03	0	Enable	Mask	Interrupt mask register (K03)
					EIK02	0	Enable	Mask	Interrupt mask register (K02)
	R/W				EIK01	0	Enable	Mask	Interrupt mask register (K01)
					EIK00	0	Enable	Mask	Interrupt mask register (K00)
F40H	K03	K02	K01	K00	K03	–	High	Low	
					K02	–	High	Low	Input port (K00–K03)
	R				K01	–	High	Low	
					K00	–	High	Low	

K00–K03 (F40H, R)

Input data of the input port terminal may be read out with these registers.

> When "1" is read: High level
> When "0" is read: Low level
>   Writing: Invalid

The terminal voltage of 4 bits input ports (K00–K03) are each reading as "1" and "0" at high (V_{DD}) level and low (V_{SS}) level, respectively.

When these bits are used for reading only, writing operation becomes invalid.

EIK00–EIK03 (F14H, R/W)

This is the interrupt mask register of the input ports.

> When "1" is written: Enable
> When "0" is written: Mask
>   Reading: Valid

EIK0x corresponds to input port K0x. Whether to mask the interrupt function can be set in units of 1 bit.
Be sure that writing to the interrupt mask register is done with the interrupt in the DISABLE state (DI).
Writing to the interrupt mask register while in the ENABLE state (EI) may cause malfunction.
At initial reset, this register is set to "0" (mask).

IK0 (F04H [D0], R)

This is the interrupt factor flag of the input ports.

> When "1" is read: Interrupt has occurred
> When "0" is read: Interrupt has not occurred
>   Writing: Invalid

The interrupt factor flags IK0 is associated with K00–K03. From the status of this flag, the software can decide whether an input interrupt has occurred.
The flag will not be set even if an input port status changes when the interrupt mask register (EIK0x) is set to "0".
Be sure that the interrupt factor flag reading is done with the interrupt in the DISABLE state (DI).
Reading the interrupt factor flag while in the ENABLE state (EI) may cause malfunction.
At initial reset, this flag is set to "0".

6.1.5 Programming notes

(1) When changing the input port from low level to high level with a pull up resistor, a delay in the waveform rise time will occur depending on the time constant of the pull up resistor and input gate capacity. Hence, when reading data from the input port, set an appropriate waiting time. Care is particularly required for key matrix configuration scanning. For reference, approximately 500 μs waiting time is required.
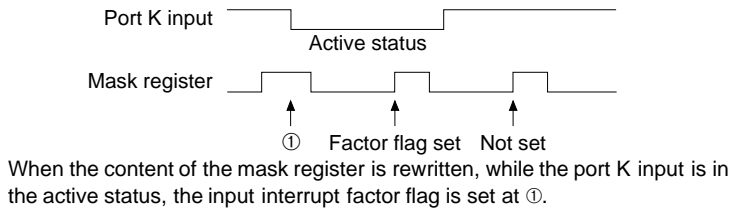
(2) Input interrupt programming related precautions

When the content of the mask register is rewritten, while the port K input is in the active status, the input interrupt factor flag is set at ①.

Fig. 6.1.5.1 Input interrupt timing

When using an input interrupt, if you rewrite the content of the mask register, when the value of the input terminal which becomes the interrupt input is in the active status (input terminal = low status), the factor flag for input interrupt may be set.

For example, a factor flag is set with the timing of ① shown in Figure 6.1.5.1. However, when clearing the content of the mask register with the input terminal kept in the low status and then setting it, the factor flag of the input interrupt is again set at the timing that has been set.

Consequently, when the input terminal is in the active status (low status), do not rewrite the mask register (clearing, then setting the mask register), so that a factor flag will only set at the rising edge in this case. When clearing, then setting the mask register, set the mask register, when the input terminal is not in the active status (high status).

(3) Be sure that writing to the interrupt mask register is done with the interrupt in the DISABLE state (DI). Writing to the interrupt mask register while in the ENABLE state (EI) may cause malfunction.

(4) Be sure that the interrupt factor flag reading is done with the interrupt in the DISABLE state (DI). Reading the interrupt factor flag while in the ENABLE state (EI) may cause malfunction.

6.2 Output Port (Rxx)

6.2.1 Configuration of output ports
The E0C6007 has 6 bits (R32, R33, and R40–R43) of general output ports built-in.
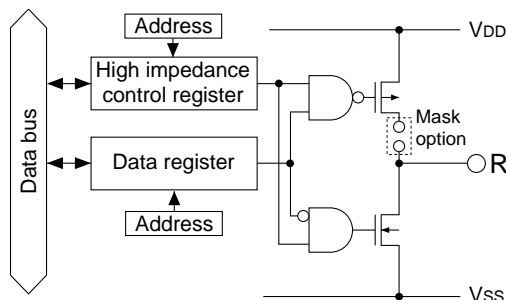Figure 6.2.1.1 shows the configuration of the output port.

Fig. 6.2.1.1 Configuration of output port

6.2.2 Mask option
The output ports may be selected for the following by mask option.

(1) Output specification of output ports
The output specification of each output port may be selected (in 1-bit units). Two types of output specification may be selected: complementary output and N channel (Nch) open drain output. However, even if Nch open drain is selected, application on the terminal of voltage exceeding the power current voltage is not permitted.

(2) Special output
Output ports R33, R40, R42 and R43 may be selected, in addition to DC output, as special output port as follows:

R33:   Programmable timer operating clock output (PTCLK)
R40:   Clock inverted output (#FOUT)
R42:   Buzzer inverted output (#BZ) or clock output (FOUT)
R43:   Buzzer output (BZ)

Buzzer outputs BZ (R43) and #BZ (R42)

Through mask option selection, R43 and R42 may be assigned as buzzer outputs. BZ and #BZ are buzzer signal outputs for driving piezo-electric buzzers, the buzzer signal being created by the division of fosc1. Moreover, digital envelope may be added to the buzzer signal.
See Chapter 9, "Sound Generator" for details.

Buzzer output BZ and #BZ can be controlled simultaneously by register R43. Note, however, that register R42 at #BZ output selection may be used as a 1-bit general register in which Read/Write operation is possible, and the data of said register will not affect #BZ (output from the R42 terminal).

Notes: • The BZ and #BZ output signals could generate hazards during ON/OFF switching.
       • When output port R43 is set to DC output, output port R42 may not be set to #BZ output.

Figure 6.2.2.1 shows the output waveform of BZ and #BZ.
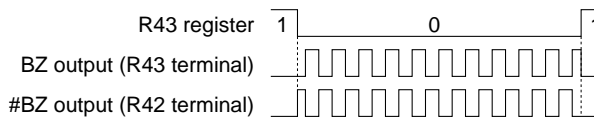
Fig. 6.2.2.1 Output waveform of BZ and #BZ

PTCLK (R33)

The operating clock for the programmable timer is output externally from this port. In this case, the clock output ON or OFF may be controlled from the R33 register by setting PTCOUT (F79H [D3]) to "1". The clock frequency is selected by the 3-bit register PTC0–PTC2.
Moreover, when PTCOUT is set to "0", output port R33 becomes DC output.
Because of the above functions, PTCLK output and DC output belong to a common option selection item. Refer to "8.3 Programmable Timer" regarding selection of clock frequency.

Clock outputs FOUT (R42), #FOUT (R40)

When R40 and R42 are selected to clock output, it outputs the clock of fosc3, fosc1 or the demultiplied fosc1. R40 (#FOUT) output generates an antiphase clock in relation to R42 (FOUT). Figure 6.2.2.2 shows the output waveform of FOUT and #FOUT. The clock frequency is selectable with the mask options, from the frequencies listed in Table 6.2.2.1.
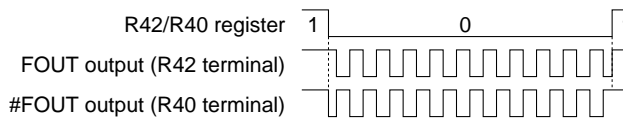

Fig. 6.2.2.2 Output waveform of FOUT and #FOUT

Note: Clock output signal could generate hazards during ON/OFF switching.

Table 6.2.2.1 FOUT clock frequency

Setting	Clock frequency (Hz)
fosc3	OSC3 oscillation frequency
fosc1/1	32,768
fosc1/2	16,384
fosc1/4	8,192
fosc1/8	4,096
fosc1/16	2,048
fosc1/32	1,024
fosc1/64	512
fosc1/128	256

6.2.3 High impedance control

The terminal output state of output ports R32 and R33 may be selected for high impedance state using the high impedance control register HZR3.

6.2.4 Control of output ports

The control registers for the output ports are explained below.

Table 6.2.4.1 Control registers of output ports

Address	Register				Name	Init	1	0	Comment
	D3	D2	D1	D0					
F53H	R33	R32	0	0	R33	X	High Off	Low On	Output port (R33) PTCLK output
	R/W		R		R32	X	High	Low	Output port (R32)
					0	–			
					0	–			
F54H	R43	R42	R41	R40	R43	1	High Off	Low On	Output port (R43) Buzzer output (BZ)
	R/W				R42	1	High Off	Low On	Output port (R42) Clock output (FOUT) [Buzzer inverted output (#BZ)]
					R41	1	High	Low	Output port (R41)
					R40	1	High Off	Low On	Output port (R40) Clock inverted output (#FOUT)
F7BH	HZR3	0	0	0	HZR3	0	Output	High-Z	R32–R33 output high-impedance control
	R/W		R		0	–			
					0	–			
					0	–			

HZR3 (F7BH [D3], R/W)

Controls high impedance loading to output ports R32 and R33.

When "1" is written: Data output
When "0" is written: High impedance
Reading: Valid

By writing "1" in the control register HZR3, the output register data (R32 and R33) is generated in the terminal; writing "0" will generate high impedance state.
During initial reset, this register is set to "0" and the ports acquire high impedance state.

When DC output is selected

R32, R33, R40–R43 (F53H [D2] and [D3], F54H, R/W)

Sets the output data for the output ports.

When "1" is written: High level
When "0" is written: Low level
Reading: Valid

Output port terminals will generate the data written into the corresponding registers (R32, R33, R40–R43) as it is. The output port terminal goes high (V$_{DD}$) when "1" is written to the register, and goes low (V$_{SS}$) when "0" is written.
At initial reset, only R40–R43 are set to "1" and the other output registers become undefined.

When special output is selected

R43 (F54H [D3], R/W) when BZ and #BZ output is selected

Performs the output control of buzzer signal (BZ, #BZ).

When "0" is written: Buzzer signal output
When "1" is written: Low level (DC)
              Reading: Valid

When "0" is set on R43, BZ signal is generated from R43 terminal; at the same time, #BZ signal (BZ inverted signal) is generated from R42 terminal if R42 is set to #BZ output.
When "1" is set on R43, R43 terminal (and R42 terminal too, when #BZ output is selected) output goes low (Vss).
Note, however, that R42 at #BZ output selection may be used as a 1-bit general register in which Read/Write operation is possible, and the data of said register will not affect #BZ (R42 terminal output).
At initial reset, R43 and R42 are set to "1".

R33 (F53H [D3], R/W) when PTCLK (DC) output is selected

Controls the output of the programmable timer operating clock (PTCLK).

When "0" is written: Clock output
When "1" is written: High level (DC)
              Reading: Valid

With "1" written on PTCOUT (F79H [D3]), the operating clock of the programmable timer may be generated externally by writing "0" on R33 register. Moreover, the output will go high (VDD) by writing "1".
However, when PTCOUT is "0", the output becomes regular DC output.

R40, R42 (F54H [D0, D2], R/W) when FOUT and #FOUT output is selected

Controls the #FOUT and FOUT (clock) output.

When "0" is written: Clock output
When "1" is written: High level (DC)
              Reading: Valid

When R42 is set to FOUT output, clock with the specified frequency is generated from R42 terminal by writing "0" on R42 register.
By writing "1", the R42 terminal will go high (VDD).
The same applies to R40. The clock phase when #FOUT signal is output from R40 is antiphase to that of R42.
At initial reset, R40 and R42 are set to "1".

6.2.5 Programming notes

(1) When BZ, #BZ, FOUT, #FOUT, and PTCLK (DC) are selected by mask option, a hazard may be observed in the output waveform when the data of the output register changes.

(2) Because the R32 and R33 ports gain high impedance during initial reset, be careful when using them as interface with external devices and the like.

6.3 I/O Port (Pxx)

6.3.1 Configuration of I/O ports

The E0C6007 has 4 bits of general I/O ports (P00–P03) built-in.
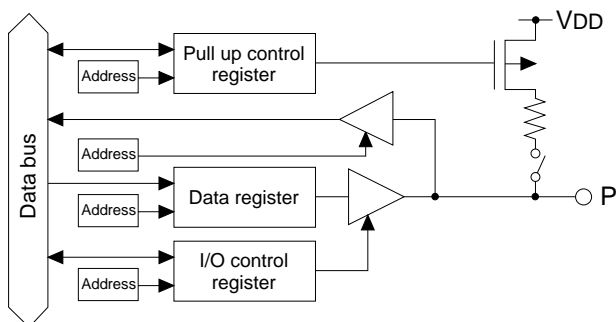Figure 6.3.1.1 shows the configuration of the I/O port.

Fig. 6.3.1.1 Configuration of I/O port

6.3.2 Mask option

Output specification (during output) for the I/O port may be selected by mask option (selected with the 4 bits group). Two types of output specification may be selected: complementary output and N channel (Nch) open drain output. However, even if Nch open drain is selected, application on the terminal of voltage exceeding the power current voltage is not permitted.

6.3.3 I/O control register and input/output mode

Input or output mode can be set for the four bits of I/O port P00–P03 by writing data to the I/O control register IOC0.

To set the input mode, "0" is written to the I/O control register. When an I/O port is set to input mode, it becomes high impedance state and works as an input port.

The output mode is set when "1" is written to the I/O control register. When an I/O port set to output mode works as an output port, it outputs a high level (V_{DD}) when the data of output register is "1", and a low level (V_{SS}) when the data of output register is "0".

6.3.4 Pull up resistor

Pull up resistors can be added to four bits of I/O ports by writing data to the pull up control register PUP0. When "0" is written to the pull up control register, the I/O port terminals are pulled up. When "1" is written, the pull up resistors are disconnected.

6.3.5 Control of I/O ports

The control registers for the I/O ports are explained below.

Table 6.3.5.1 Control register of I/O ports

Address	Register								Comment
	D3	D2	D1	D0	Name	Init	1	0	
F60H	P03	P02	P01	P00	P03	X	High	Low	
					P02	X	High	Low	I/O port (P00–P03)
	R/W				P01	X	High	Low	
					P00	X	High	Low	
F7DH	0	0	0	IOC0	0	–			
					0	–			
	R			R/W	0	–			I/O control (P00–P03)
					IOC0	0	Output	Input	
F7EH	0	0	0	PUP0	0	–			
					0	–			
	R			R/W	0	–			
					PUP0	0	Off	On	I/O pull up resistor On/Off (P00–P03)

IOC0 (F7DH [D0], R/W)

Input/output direction of I/O ports are set in units of 4 bits.

When "1" is written: Output mode
When "0" is written: Input mode
        Reading: Valid

By writing "1" to IOC0, the I/O ports enter the output mode, while writing "0" they enter the input mode. At initial reset, IOC0 is set to "0" and the I/O ports are all in the input mode.

PUP0 (F7EH [D0], R/W)

Whether the I/O ports will be pulled up or not is set in units of 4 bits.

When "0" is written: Pull up ON
When "1" is written: Pull up OFF
        Reading: Valid

By writing "0" to PUP0, the I/O ports are pulled up, while writing "1" turns the pull up function OFF. At initial reset, PUP0 is set at "0", and all I/O ports are pulled up.

P00–P03 (F60H, R/W)

• During writing operation
When "1" is written: High level
When "0" is written: Low level

When the I/O port is set at output port, the data written is generated on the I/O port terminal as it is. When "1" is written as port data, the port terminal goes high (VDD) and goes low (Vss) when "0" is written.
Note, however, that even at input mode, port data writing is also possible.

• During reading operation

When "1" is read: High level
When "0" is read: Low level

Reading the I/O port terminal voltage level. When the I/O port is at input mode, voltage level input of the port terminal is read; when set at output mode, output voltage level is read. When the terminal voltage is at high (VDD) level, port data reading is "1"; at low (Vss) level, it is "0".

6.3.6 Programming notes

(1) When the I/O port is set at output mode, and low impedance load is connected to the port terminal, the data written and read may differ.

(2) If the state of the I/O port meets all of the following 4 conditions, the reading data will be undefined:
- The input/output mode is set at output mode
- Output specification is set at Nch open drain
- The content of the data register is "1"
- The pull up resistor turned is OFF

CHAPTER 7 LCD DRIVER

The E0C6007 has 16 common terminals and 40 segment terminals and can drive a maximum of 640 (40 × 16) dots (8 characters × 2 lines) LCD.

This LCD driver performs the following control through the software.

• Drive duty can be set to 1/16 or 1/8 duty.

• LCD contrast can be adjusted through a 16 steps range.

• All dots of the LCD panel can be switched ON and OFF.

7.1 Drive Duty

Because the power for LCD driving is generated by the internal circuit of the CPU, there is no need to provide for it externally. Driving is done by 1/16 duty or 1/8 duty dynamic drive through 4 electric potentials (1/4 bias) : V_{L1}, V_{L2}, V_{L4}, and V_{L5}. The 5 electric potentials are entered in V_{L1}, V_{L2}, V_{L3}, V_{L4} and V_{L5} terminals and 1/5 bias driving may then be set.

Drive duty may be selected from the software. Dot number differences due to the selected duty are shown in Table 7.1.1.

Table 7.1.1 Differences due to selected duty

Duty	Common terminal in use	Maximum dot number	Frame frequency ∗
1/16	COM0–15	640 dots	32 Hz
1/8	COM0–7	320 dots	32 Hz

∗ Frame frequency = $f_{OSC1}/1,024$

Figure 7.1.1 shows the drive waveform for 1/16 duty (1/5 bias), and Figure 7.1.2 shows the drive waveform for 1/8 duty (1/4 bias).
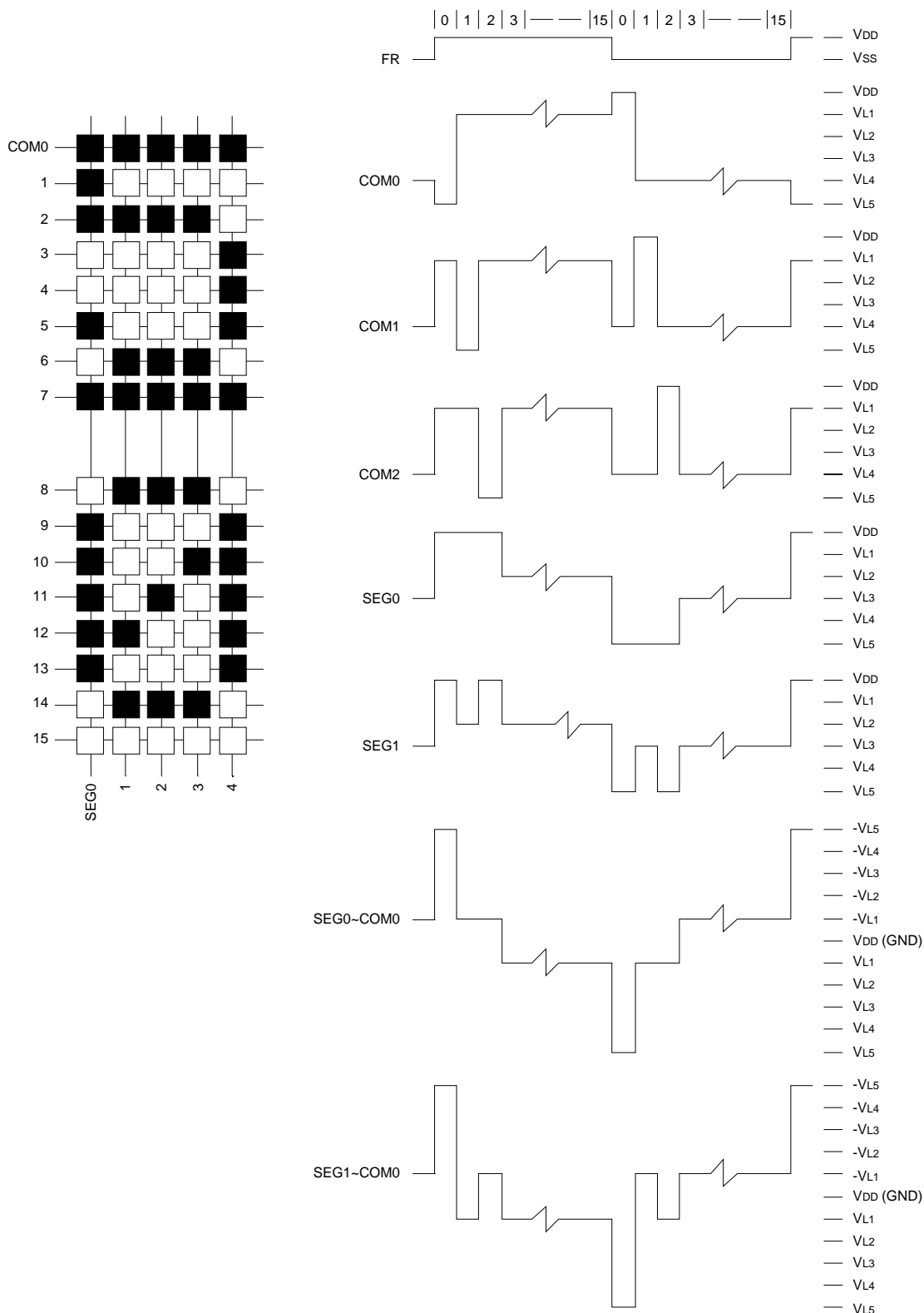
Fig. 7.1.1 Drive waveform for 1/16 duty (1/5 bias)

Note: 1/5 bias may only be utilized when power for LCD driving is supplied externally; when internal power circuit is used, 1/4 bias is utilized.
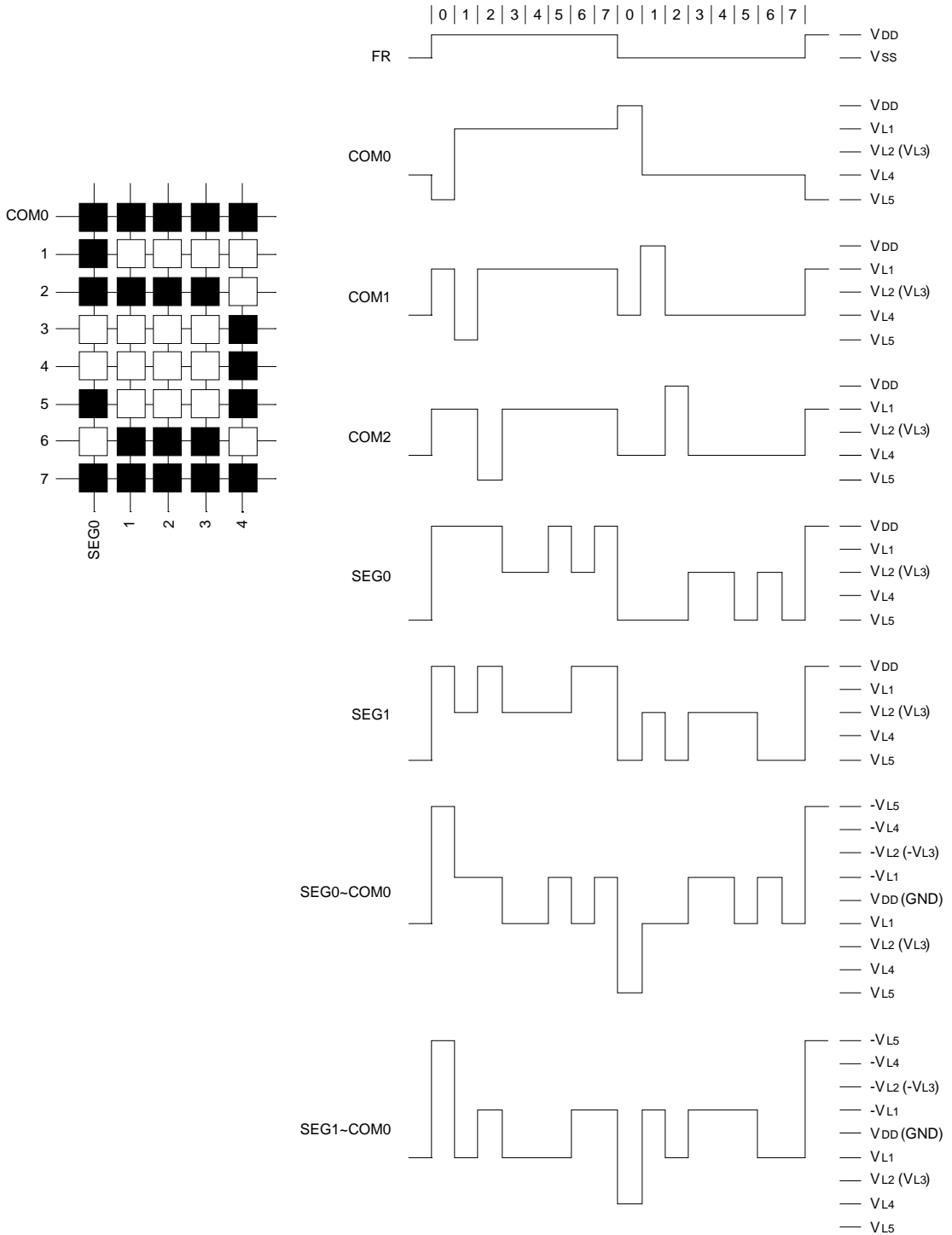
Fig. 7.1.2 Drive waveform for 1/8 duty (1/4 bias)

7.2 Mask Option

Disconnecting the internal power for LCD driving will enable electric potentials to be supplied externally. In such case, the 5 electric potentials are entered in V_{L1}, V_{L2}, V_{L3}, V_{L4} and V_{L5} terminals and 1/5 bias driving may then be set. Since 1/5 bias driving provides better display quality, when low power current consumption is not required (i.e., when power is supplied from AC outlet), select external power mode. However, note that in order to maintain a stable display, power source must be one which will remain stable even when heavy load such as buzzer, etc. is driven.

Moreover, in the external power mode, the contrast adjustment function cannot be used. Accommodate this limitation by utilizing the external circuit as necessary.

A sample circuit of external power for LCD driving when power is supplied externally is shown in Figure 7.2.1.
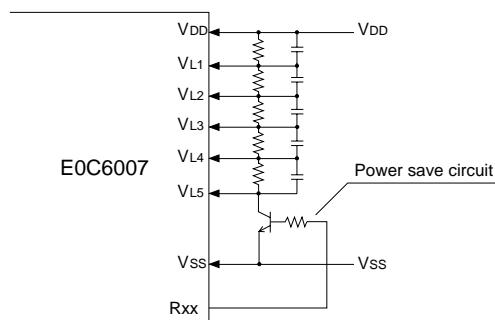
Fig. 7.2.1 Sample circuit of external power for LCD driving when power is supplied externally

7.3 Display Data Memory

The display data memory of the E0C6007 is allocated to the built-in RAM addresses E00H–E4FH and E80H–ECFH.

Figure 7.3.1 shows the correspondence between the display data memory and the LCD dot matrix.
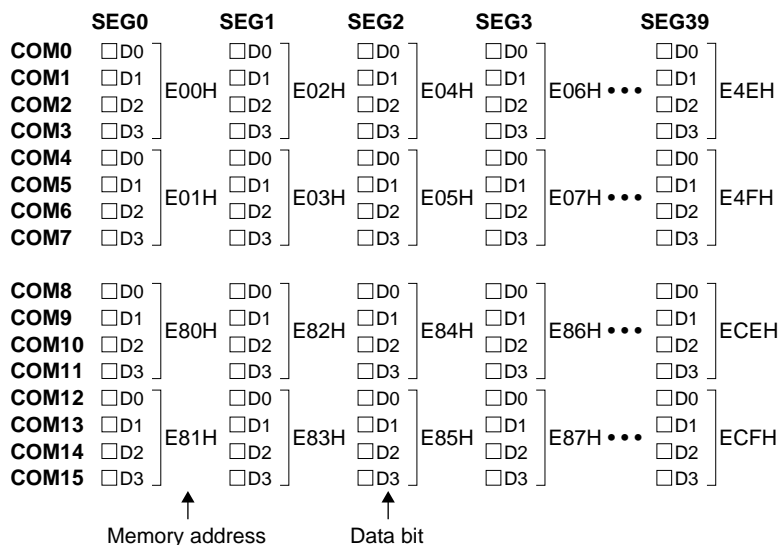
Fig. 7.3.1 LCD dot matrix and segment memory correspondence

When the segment memory bit is assigned as "1", the corresponding LCD dot lights up, and when assigned as "0", the dot dies out.

At 1/16 duty drive and 1/8 duty drive, COM0 to COM15 lines and COM0 to COM7 lines light up, respectively.

At initial reset, the display data memory content becomes undefined and hence, there is need to initialize by software.

7.4 Control of LCD Driver

The control registers for the LCD driver are explained below.

Table 7.4.1 Control registers of LCD driver

Address	Register				Name	Init	1	0	Comment
	D3	D2	D1	D0					
F71H	ALOFF	ALON	LDUTY	HLMOD	ALOFF	1	All off	Normal	All LCD dots fade out control
					ALON	0	All on	Normal	All LCD dots displayed control
					LDUTY	0	1/8	1/16	LCD drive duty switch
	R/W				HLMOD	0	HLMOD	Normal	Heavy load protection mode
F72H	LC3	LC2	LC1	LC0	LC3	X			LCD contrast adjustment
					LC2	X			⎤ LC3–LC0 = 0 light
					LC1	X			⋮
	R/W				LC0	X			⎦ LC3–LC0 = 15 dark
F7FH	0	0	0	LCDOFF	0 *4	– *2			
					0 *4	– *2			
	R			R/W	0 *4	– *2			
					LCDOFF	1	Normal	Off	LCD display control

LDUTY (F71H [D1], R/W)
Sets the LCD drive duty.

When "1" is written: 1/8 duty
When "0" is written: 1/16 duty
Reading: Valid

Writing "1" or "0" on LDUTY will set is to 1/8 duty or 1/16 duty, respectively.
At initial reset, LDUTY is set at "0".

ALON (F71H [D2], R/W)
Displays the all LCD dots on.

When "1" is written: All LCD dots displayed
When "0" is written: Normal operation
Reading: Valid

Writing "1" to ALON will display all the LCD dots on; writing "0" will set the LCD display back to normal. LCD panel testing may be conducted with this function.
Total LCD displaying at ALON = "1" is a static operation and does not affect the content of the display data memory.
ALON precedes ALOFF.
At initial reset, ALON is set at "0".

ALOFF (F71H [D3], R/W)
Fade outs the all LCD dots.

When "1" is written: All LCD dots fade out
When "0" is written: Normal operation
Reading: Valid

When "1" is written on ALOFF, all LCD dots will fade out; writing "0" will set it back to normal.
All fading out of LCD at ALOFF = "1" is due to light out signals and does not affect the content of the display data memory.
Flashing of the entire LCD panel is performed by this function.
At initial reset, ALOFF is set to "1".

LC0, LC1, LC2, LC3 (F72H, R/W)

Will adjust the LCD contrast.

Contrast may be adjusted to 16 levels as shown in Table 7.4.2.

Table 7.4.2 LCD contrast

	LC3	LC2	LC1	LC0	Contrast
0	0	0	0	0	light
1	0	0	0	1	↑
2	0	0	1	0	
3	0	0	1	1	
4	0	1	0	0	
5	0	1	0	1	
6	0	1	1	0	
7	0	1	1	1	
8	1	0	0	0	
9	1	0	0	1	
A	1	0	1	0	
B	1	0	1	1	
C	1	1	0	0	
D	1	1	0	1	
E	1	1	1	0	↓
F	1	1	1	1	dark

At room temperature, use setting number 7 or 8 as standard.

The voltage of the LCD system power terminals V_{L1}, V_{L2}, V_{L4} and V_{L5} changes through this function.

Because at initial reset, the contents of LC0–LC3 are undefined, initialize it by the software.

LCDOFF (F7FH [D0], R/W)

Control the LCD system voltage circuit ON and OFF.

   When "1" is written: Normal operation
   When "0" is written: Display OFF
             Reading: Valid

When "1" is written to LCDOFF, the LCD system voltage circuit turns ON and generate the LCD drive volatges. When "0" is written, all the drive voltages go to Vss level and the display turns OFF.

At initial reset, this register is set to "1".

7.5 Programming Note

Because at initial reset, the contents of display data memory and LC0–LC3 are undefined, there is need to initialize by software.

CHAPTER 8 TIMERS

8.1 Clock Timer

8.1.1 Configuration of clock timer

The E0C6007 has a clock timer with OSC1 (crystal oscillation) as basic oscillation built-in. The clock timer is configured with an 8 bits binary counter with 256 Hz signal divided from OSC1 as input clock, allowing 128 Hz–1 Hz of data to be read by the software.
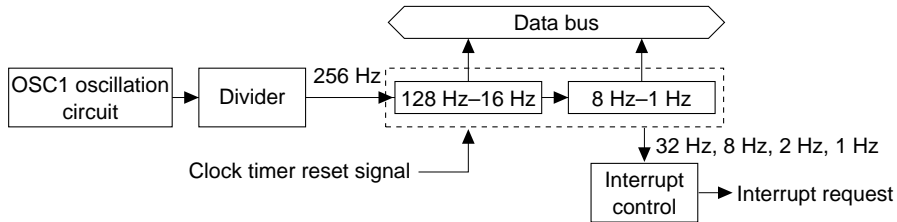Figure 8.1.1.1 shows the configuration of the clock timer.

Fig. 8.1.1.1 Configuration of clock timer

8.1.2 Interrupt function

The clock timer has interrupt capability, and interrupt is generated by the falling edge of 32 Hz, 8 Hz, 2 Hz, and 1 Hz signals. Figure 8.1.2.1 shows the timing chart of the clock timer.

Address	Register	Frequency	Clock timer timing chart
F20H	D0	128 Hz	
	D1	64 Hz	
	D2	32 Hz	
	D3	16 Hz	
F21H	D0	8 Hz	
	D1	4 Hz	
	D2	2 Hz	
	D3	1 Hz	
32 Hz interrupt request			
8 Hz interrupt request			
2 Hz interrupt request			
1 Hz interrupt request			

Fig. 8.1.2.1 Timing chart of clock timer

The clock timer interrupt is generated at the falling edge of the frequencies (32 Hz, 8 Hz, 2 Hz, and 1 Hz). At this time, the corresponding interrupt factor flag (IT32, IT8, IT2, and IT1) is set to "1".
Selection of whether to mask the separate interrupts can be made with the interrupt mask registers (EIT32, EIT8, EIT2, and EIT1). However, regardless of the interrupt mask register setting, the interrupt factor flag is set to "1" at the falling edge of the corresponding signal.

8.1.3 Control of clock timer

The control registers for the clock timer are explained below.

Table 8.1.3.1 Control registers of clock timer

Address	Register				Comment				
	D3	D2	D1	D0	Name	Init	1	0	Comment
F00H	IT1	IT2	IT8	IT32	IT1	0	Yes	No	Interrupt factor flag (clock timer 1 Hz)
					IT2	0	Yes	No	Interrupt factor flag (clock timer 2 Hz)
	R				IT8	0	Yes	No	Interrupt factor flag (clock timer 8 Hz)
					IT32	0	Yes	No	Interrupt factor flag (clock timer 32 Hz)
F10H	EIT1	EIT2	EIT8	EIT32	EIT1	0	Enable	Mask	Interrupt mask register (clock timer 1 Hz)
					EIT2	0	Enable	Mask	Interrupt mask register (clock timer 2 Hz)
	R/W				EIT8	0	Enable	Mask	Interrupt mask register (clock timer 8 Hz)
					EIT32	0	Enable	Mask	Interrupt mask register (clock timer 32 Hz)
F20H	TM3	TM2	TM1	TM0	TM3	0			Clock timer data (16 Hz)
					TM2	0			Clock timer data (32 Hz)
	R				TM1	0			Clock timer data (64 Hz)
					TM0	0			Clock timer data (128 Hz)
F21H	TM7	TM6	TM5	TM4	TM7	0			Clock timer data (1 Hz)
					TM6	0			Clock timer data (2 Hz)
	R				TM5	0			Clock timer data (4 Hz)
					TM4	0			Clock timer data (8 Hz)
F76H	0	0	TMRST	WDRST	0	–			
					0	–			
	R		W		TMRST	Reset	Reset	–	Clock timer reset
					WDRST	Reset	Reset	–	Watchdog timer reset

TMRST (F76H [D1], W)

This bit resets the clock timer.

> When "1" is written: Clock timer reset
> When "0" is written: No operation
> Reading: Always "0"

By writing "1" on TMRST, the clock timer is reset and all timer data are set to "0".
Because this bit is only for writing, it is always "0" during reading.

TM0–TM7 (F20H, F21H, R)

Will read the data of the clock timer.
TMx (x = 0–7) and frequency correspondence are as follows:

F20H	F21H
TM0: 128 Hz	TM4: 8 Hz
TM1: 64 Hz	TM5: 4 Hz
TM2: 32 Hz	TM6: 2 Hz
TM3: 16 Hz	TM7: 1 Hz

The above 8 bits are only for reading and render writing operation invalid.
At initial reset, timer data is initialized to "0".

EIT32, EIT8, EIT2, EIT1 (F10H, R/W)

These are the interrupt mask registers of the clock timer.

> When "1" is written: Enabled
> When "0" is written: Masked
> Reading: Valid

EIT32, EIT8, EIT2, and EIT1 correspond to 32 Hz, 8 Hz, 2 Hz, and 1 Hz timer interrupts, respectively.
Be sure that writing to the interrupt mask register is done with the interrupt in the DISABLE state (DI).
Writing to the interrupt mask register while in the ENABLE state (EI) may cause malfunction.
At initial reset, these registers are all set to "0" (mask).

IT32, IT8, IT2, IT1 (F00H, R)
These are the interrupt factor flags of the clock timer.

When "1" is read: Interrupt has occurred
When "0" is read: Interrupt has not occurred
Writing: Invalid

IT32, IT8, IT2, and IT1 correspond to 32 Hz, 8 Hz, 2 Hz, and 1 Hz timer interrupts, respectively.
The occurrence of clock timer interrupt can be determined by the software through these flags. However, regardless of interrupt masking, these flags are set to "1" due to the falling edge of the corresponding signal.
Be sure that the interrupt factor flag reading is done with the interrupt in the DISABLE state (DI).
Reading the interrupt factor flag while in the ENABLE state (EI) may cause malfunction.
At initial reset, these flags are set to "0".

8.1.4 Programming notes

(1) When the clock timer has been reset, the interrupt factor flag (IT) may sometimes be set to "1". Consequently, perform flag read (reset the flag) as necessary at reset.

(2) Because the watchdog timer counts up during reset as in the above (1), reset the watchdog timer as necessary.

(3) When the low-order digits (TM0–TM3) and high-order digits (TM4–TM7) are consecutively read, proper reading may not be obtained due to the carry from the low-order digits into the high-order digits (when the reading of the low-order digits and high-order digits span the timing of the carry). For this reason, perform multiple reading of timer data, make comparisons and use matching data as result.

(4) Be sure that writing to the interrupt mask register is done with the interrupt in the DISABLE state (DI). Writing to the interrupt mask register while in the ENABLE state (EI) may cause malfunction.

(5) Be sure that the interrupt factor flag reading is done with the interrupt in the DISABLE state (DI). Reading the interrupt factor flag while in the ENABLE state (EI) may cause malfunction.

8.2 Stopwatch Timer

8.2.1 Configuration of stopwatch timer

The E0C6007 has 1/100 sec unit (SWL) and 1/10 sec unit (SWH) stopwatch timer built-in. The stopwatch timer is configured with a 2 levels 4 bits BCD counter which has an input clock approximating 100 Hz signal (signal divided from OSC1 to the closest 100 Hz) and data can be read in units of 4 bits by software.

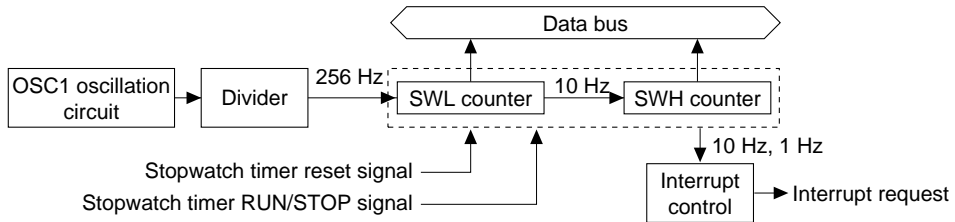Figure 8.2.1.1 shows the configuration of the stopwatch timer.

Fig. 8.2.1.1 Configuration of stopwatch timer

The stopwatch timer can be used as a separate timer from the clock timer. In particular, digital watch stopwatch functions can be realized easily with software.

8.2.2 Count-up pattern

The stopwatch timer is configured of 4 bits BCD counters SWL and SWH.

The counter SWL, at the stage preceding the stopwatch timer, has an approximated 100 Hz signal for the input clock. It counts up every 1/100 sec, and generates an approximated 10 Hz signal. The counter SWH has an approximated 10 Hz signal generated by the counter SWL for the input clock. In count-up every 1/10 sec, and generated 1 Hz signal.

Figure 8.2.2.1 shows the count-up pattern of the stopwatch timer.
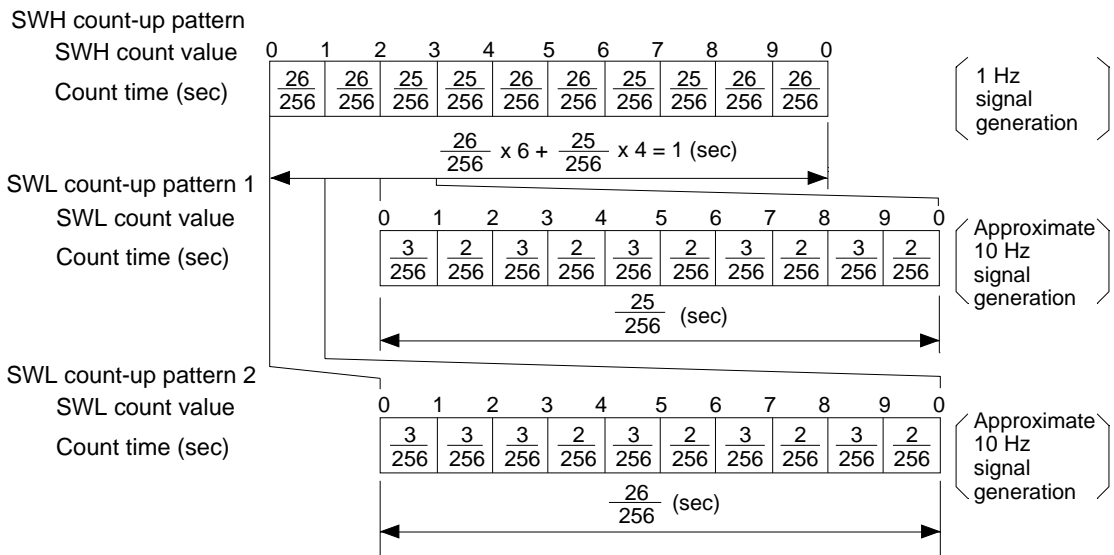
Fig. 8.2.2.1 Count-up pattern of stopwatch timer

SWL generates an approximated 10 Hz signal from the basic 256 Hz signal. The count-up intervals are 2/256 sec and 3/256 sec, so that finally two patterns are generated: 25/256 sec and 26/256 sec intervals. Consequently, these patterns do not amount to an accurate 1/100 sec.

SWH counts the approximated 10 Hz signals generated by the 25/256 sec and 26/256 sec intervals in the ratio of 4 : 6, to generate a 1 Hz signal. The count-up intervals are 25/256 sec and 26/256 sec, which do not amount to an accurate 1/10 sec.

8.2.3 Interrupt function

Stopwatch timers SWL and SWH, through their respective overflows, can generate 10 Hz (approximate 10 Hz) and 1 Hz interrupts.

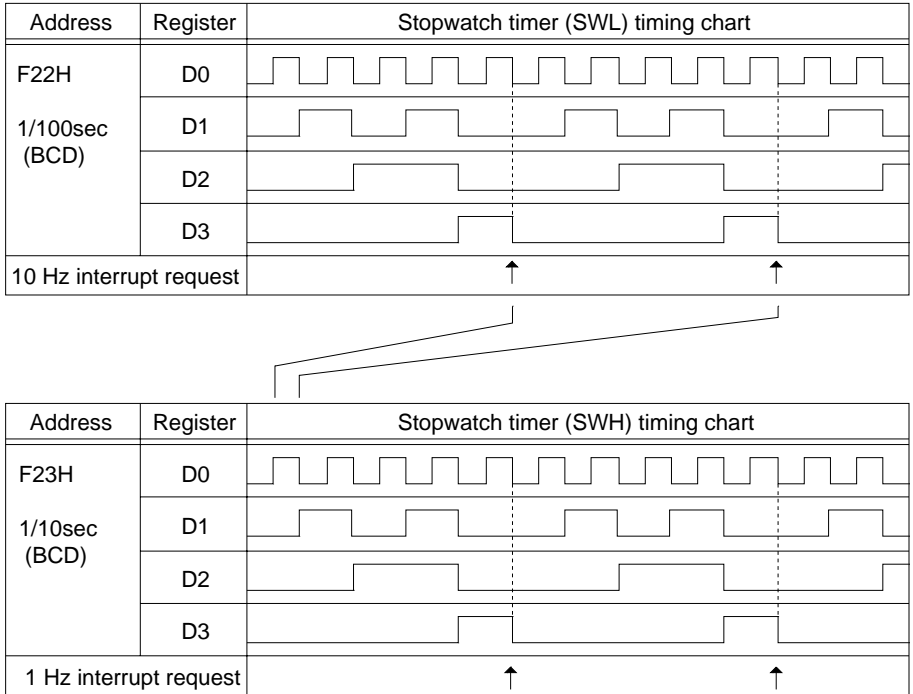Figure 8.2.3.1 shows the timing chart for the stopwatch timer.

Address	Register	Stopwatch timer (SWL) timing chart
F22H	D0	
1/100sec (BCD)	D1	
	D2	
	D3	
10 Hz interrupt request		

Address	Register	Stopwatch timer (SWH) timing chart
F23H	D0	
1/10sec (BCD)	D1	
	D2	
	D3	
1 Hz interrupt request		

Fig. 8.2.3.1 Timing chart for stopwatch timer

The stopwatch interrupts are generated by the overflow of their respective counters SWL and SWH (changing "9" to "0"). At this time, the corresponding interrupt factor flags (ISW0 and ISW1) are set to "1".

The respective interrupts can be masked separately through the interrupt mask registers (EISW0 and EISW1). However, regardless of the setting of the interrupt mask registers, the interrupt factor flags are set to "1" by the overflow of their corresponding counters.

8.2.4 Control of stopwatch timer

The control registers for the stopwatch timer are explained below.

Table 8.2.4.1 Control registers of stopwatch timer

Address	Register				Name	Init	1	0	Comment
	D3	D2	D1	D0					
F01H	0	0	ISW1	ISW0	0	–			
					0	–			
	R				ISW1	0		No	Interrupt factor flag (stopwatch 1 Hz)
					ISW0	0		No	Interrupt factor flag (stopwatch 10 Hz)
F11H	0	0	EISW1	EISW0	0	–			
					0	–			
	R		R/W		EISW1	0	Enable	Mask	Interrupt mask register (stopwatch 1 Hz)
					EISW0	0	Enable	Mask	Interrupt mask register (stopwatch 10 Hz)
F22H	SWL3	SWL2	SWL1	SWL0	SWL3	0			⌐ MSB
					SWL2	0			Stopwatch timer
	R				SWL1	0			1/100 sec data (BCD)
					SWL0	0			⌐ LSB
F23H	SWH3	SWH2	SWH1	SWH0	SWH3	0			⌐ MSB
					SWH2	0			Stopwatch timer
	R				SWH1	0			1/10 sec data (BCD)
					SWH0	0			⌐ LSB
F77H	0	0	SWRST	SWRUN	0	–			
					0	–			
	R		W	R/W	SWRST	Reset	Reset	–	Stopwatch timer reset
					SWRUN	0	Run	Stop	Stopwatch timer Run/Stop

SWRST (F77H [D1], W)

This bit resets the stopwatch timer.

When "1" is written: Stopwatch timer reset
When "0" is written: No operation
Reading: Always "0"

By writing "1" on SWRST, the stopwatch timer is reset. All timer data is set to "0".
When the stopwatch timer is reset in the RUN mode, it will re-start counting immediately after the reset and at STOP mode, the reset data is maintained.
Because this bit is for writing only, it is always "0" during reading.

SWRUN (F77H [D0], R/W)

This register controls RUN/STOP of the stopwatch timer.

When "1" is written: RUN
When "0" is written: STOP
Reading: Valid

By writing "1" on SWRUN, the stopwatch timer performs counting operation. Writing "0" will make the stopwatch stop counting.
Even if the stopwatch is stopped, the timer data at that point is kept.
When data of the counter is read at run mode, proper reading may not be obtained due to the carry from low-order digits (SWL) into high-order digits (SWH) (i.e., in case SWL and SWH reading span the timing of the carry). To avoid this occurrence, perform the reading after suspending the counter once and then set the SWRUN to "1" again.
Moreover, it is required that the suspension period not exceed 976 μs (1/4 cycle of 256 Hz).
At initial reset, SWRUN is set to "0".

SWL0–SWL3 (F22H, R)

Will read the stopwatch timer data to the 1/100 sec digits (BCD).
Since these bits are for reading only, writing operation is invalidated.
At initial reset, timer data is set to "0".

SWH0–SWH3 (F23H, R)

Will read the stopwatch timer data to the 1/10 sec digits (BCD).

Since these bits are for reading only, writing operation is invalidated.

At initial reset, timer data is set to "0".

EISW0, EISW1 (F11H [D0, D1], R/W)

These are the interrupt mask registers of the stopwatch timer.

When "1" is written: Enabled
When "0" is written: Masked
          Reading: Valid

EISW0 and EISW1 correspond to 10 Hz and 1 Hz stopwatch timer interrupts, respectively.

Be sure that writing to the interrupt mask register is done with the interrupt in the DISABLE state (DI).

Writing to the interrupt mask register while in the ENABLE state (EI) may cause malfunction.

At initial reset, these registers are all set to "0" (mask).

ISW0, ISW1 (F01H [D0, D1], R)

These are the interrupt factor flags of the stopwatch timer.

When "1" is read: Interrupt has occurred
When "0" is read: Interrupt has not occurred
         Writing: Invalid

ISW0 and ISW1 correspond to 10 Hz and 1 Hz stopwatch timer interrupts, respectively.

The occurrence of stopwatch timer interrupt can be determined by the software through these flags.

However, regardless of interrupt masking, these flags are set to "1" by the overflow of the corresponding counters.

Be sure that the interrupt factor flag reading is done with the interrupt in the DISABLE state (DI).

Reading the interrupt factor flag while in the ENABLE state (EI) may cause malfunction.

At initial reset, these flags are set to "0".

8.2.5 Programming notes

(1) When data of the counter is read at run mode, perform the reading after suspending the counter once and then set SWRUN to "1" again. Moreover, it is required that the suspension period not exceed 976 µs (1/4 cycle of 256 Hz).

(2) Be sure that writing to the interrupt mask register is done with the interrupt in the DISABLE state (DI). Writing to the interrupt mask register while in the ENABLE state (EI) may cause malfunction.

(3) Be sure that the interrupt factor flag reading is done with the interrupt in the DISABLE state (DI). Reading the interrupt factor flag while in the ENABLE state (EI) may cause malfunction.

8.3 Programmable Timer

8.3.1 Configuration of programmable timer

The E0C6007 has a programmable timer with OSC1 (crystal oscillation) as basic oscillation built-in. The programmable timer is configured with an 8 bits pre-settable down counter and it has been down-count at initial value by 256 Hz–8,192 Hz signal or by the input signal of input port K03.

The initial value of count data can be set by software to the reload register; at the point where the down-counter value is "0", the programmable timer reloads the initial value and continues to down-count.

The down-counter data may be read through the software. Moreover, the input clock being selected may be generated to output port R33.

Figure 8.3.1.1 shows the configuration of the programmable timer.
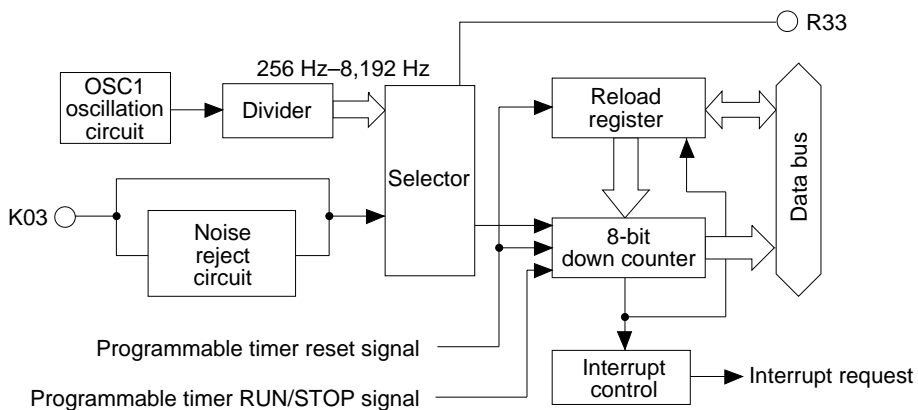
Fig. 8.3.1.1 Configuration of programmable timer

One input clock may be selected by software from any of the following 8 types:

(1) K03 input (with noise rejector)
(2) K03 input (direct)
(3) 256 Hz
(4) 512 Hz
(5) 1,024 Hz
(6) 2,048 Hz
(7) 4,096 Hz
(8) 8,192 Hz

Note, however, that down-count is done at falling edges of the input signal as shown in Figure 8.3.1.2.
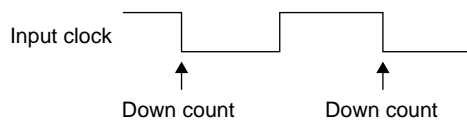
Fig. 8.3.1.2 Timing of down-counts

Type (1) K03 input (with noise rejector) is for counting by key entry, the input signal from which passes the 256 Hz sampling noise reject circuit. With this, no more than 2 ms of chattering is purged, and at least 4 ms signal is received.

8.3.2 Interrupt function

The programmable timer generates interrupt after the down-count from the initial setting is completed and the content of the down-counter indicates 00H.

After interrupt generation, the programmable timer reloads the initial count value into the down-counter and resumes counting.

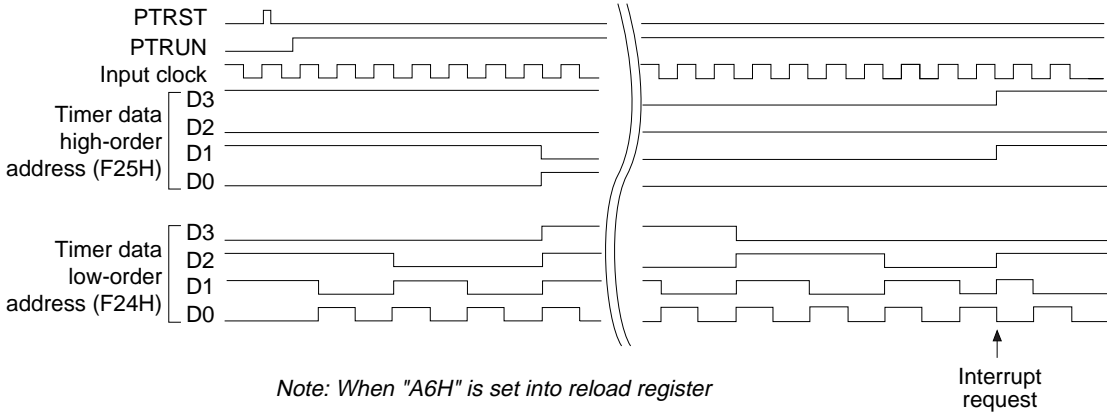Figure 8.3.2.1 shows the timing chart of the programmable timer.

Note: When "A6H" is set into reload register

Fig. 8.3.2.1 Timing chart of programmable timer

When the down-counter values PT0–PT7 have become 00H the interrupt factor flag IPT is set to "1" and an interrupt is generated. The interrupt can be masked through the interrupt mask register EIPT. However, regardless of the setting of the interrupt mask register, the interrupt factor flag is set to "1" when the down-counter equals 00H.

8.3.3 Control of programmable timer

The control registers for the programmable timer are explained below.

Table 8.3.3.1 Control registers of programmable timer

Address	Register				Name	Init	1	0	Comment
	D3	D2	D1	D0					
F02H	0	0	0	IPT	0	–			
					0	–			
	R				0	–			
					IPT	0	Yes	No	Interrupt factor flag (programmable timer)
F12H	0	0	0	EIPT	0	–			
					0	–			
	R			R/W	0	–			
					EIPT	0	Enable	Mask	Interrupt mask register (programmble timer)
F24H	PT3	PT2	PT1	PT0	PT3	X			⌐ MSB
					PT2	X			Programmable timer data (low-order)
	R				PT1	X			
					PT0	X			⌐ LSB
F25H	PT7	PT6	PT5	PT4	PT7	X			⌐ MSB
					PT6	X			Programmable timer data (high-order)
	R				PT5	X			
					PT4	X			⌐ LSB
F26H	RD3	RD2	RD1	RD0	RD3	X			⌐ MSB
					RD2	X			Programmable timer
	R/W				RD1	X			reload data (low-order)
					RD0	X			⌐ LSB
F27H	RD7	RD6	RD5	RD4	RD7	X			⌐ MSB
					RD6	X			Programmable timer
	R/W				RD5	X			reload data (high-order)
					RD4	X			⌐ LSB
F78H	0	0	PTRST	PTRUN	0	–			
					0	–			
	R		W	R/W	PTRST	Reset	Reset	–	Programmable timer reset
					PTRUN	0	Run	Stop	Programmable timer Run/Stop
F79H	PTCOUT	PTC2	PTC1	PTC0	PTCOUT	0	On	Off	Programmable timer clock output
					PTC2	0			
	R/W				PTC1	0			Programmable timer input clock selection
					PTC0	0			

PTC0, PTC1, PTC2 (F79H [D0–D2], R/W)
Selects the input clock.
The PTC0–PTC2 setting and input clock correspondence is shown in Table 8.3.3.2.

Table 8.3.3.2 Input clock setting

PTC2	PTC1	PTC0	Input clock
0	0	0	K03 input (with noise rejector)
0	0	1	K03 input (direct)
0	1	0	256 Hz
0	1	1	512 Hz
1	0	0	1,024 Hz
1	0	1	2,048 Hz
1	1	0	4,096 Hz
1	1	1	8,192 Hz

PTCOUT (F79H [D3], R/W)
Generates the input clock being selected to output port R33.
Refer to Section 6.2, "Output Port" regarding control methods.

RD0–RD3, RD4–RD7 (F26H, F27H, R/W)
These are reload registers for setting the initial value of the timer.
Sets the low-order 4 bits of the 8 bits timer data to RD0–RD3, and the high-order 4 bits to RD4–RD7.
The set timer data is loaded to the down-counter when the programmable timer is reset or when the content of the down-counter is 00H.
When data of reload registers is set at "00H", the down-counter becomes a 256-value counter.
At initial reset, this register will be undefined.

PTRST (F78H [D1], W)
This bit resets the programmable timer.

When "1" is written: Programmable timer reset
When "0" is written: No operation
    Reading: Always "0"

By writing "1" on PTRST, the programmable timer is reset.
The contents set in RD0–RD7 are loaded into the down-counter.
When the programmable timer is reset in the RUN mode, it will re-start counting immediately after loading and at STOP mode, the load data is maintained.
Because this bit is only for writing, it is always "0" during reading.

PTRUN (F78H [D0], R/W)
This register controls RUN/STOP of the programmable timer.

When "1" is written: RUN
When "0" is written: STOP
    Reading: Valid

By writing "1" on PTRUN, the programmable timer performs counting operation. Writing "0" will make the programmable timer stop counting.
Even if the programmable timer is stopped, the timer data at that point is kept.
When data of the counter is read at the RUN mode, proper reading may not be obtained due to the carry from the low-order digits (PT0–PT3) into the high-order digits (PT4–PT7) (when the reading of the low-order digits and high-order digits span the timing of the carry). To avoid this occurrence, perform the reading after suspending the programmable timer once, and set the PTRUN to "1" again. Moreover, it is required that the suspension period be within 1/4 cycle of the input clock (in case of 1/2 duty).
At initial reset, PTRUN is set to "0".

PT0–PT3, PT4–PT7 (F24H, F25H, R)
Will read the data from the down-counter of the programmable timer.
Will read the low-order 4 bits of the 8 bits counter data PT0–PT3, and the high-order 4 bits PT4–PT7.
Because these 8 bits are only for reading, writing operation is rendered invalid.
At initial reset, timer data will be undefined.

EIPT (F12H [D0], R/W)
This is the interrupt mask register of the programmable timer.

When "1" is written: Enabled
When "0" is written: Masked
    Reading: Valid

Be sure that writing to the interrupt mask register is done with the interrupt in the DISABLE state (DI).
Writing to the interrupt mask register while in the ENABLE state (EI) may cause malfunction.
At initial reset, this register is set to "0" (mask).

IPT (F02H [D0], R)

This is the interrupt factor flag of the programmable timer.

When "1" is read: Interrupt has occurred
When "0" is read: Interrupt has not occurred
Writing: Invalid

From the status of this flag, the software can decide whether the programmable timer interrupt. Note, however, that even if the interrupt is masked, this flag will be set to "1" by the counter value will become "00H".

Be sure that the interrupt factor flag reading is done with the interrupt in the DISABLE state (DI).
Reading the interrupt factor flag while in the ENABLE state (EI) may cause malfunction.
At initial reset, this flag is set to "0".

8.3.4 Programming notes

(1) When initiating programmable timer count, perform programming by the following steps:

   1. Set the initial data to RD0–RD7.
   2. Reset the programmable timer by writing "1" to PTRST.
   3. Start the down-count by writing "1" to PTRUN.

(2) When the reload register (RD0–RD7) value is set at "00H", the down-counter becomes a 256-value counter.

(3) When data of the timer is read consecutively in 8 bits in the RUN mode, perform the reading after suspending the timer once and then set the PTRUN to "1" again. Moreover, it is required that the suspension period be within 1/4 cycle of the input clock (in case of 1/2 duty). Accordingly, when the input clock is a fast clock faster than a 256 Hz, high speed processing by OSC3 is required.

(4) Be sure that writing to the interrupt mask register is done with the interrupt in the DISABLE state (DI). Writing to the interrupt mask register while in the ENABLE state (EI) may cause malfunction.

(5) Be sure that the interrupt factor flag reading is done with the interrupt in the DISABLE state (DI). Reading the interrupt factor flag while in the ENABLE state (EI) may cause malfunction.

CHAPTER 9 SOUND GENERATOR

9.1 Configuration of Sound Generator

The E0C6007 is capable of generating buzzer signals (BZ and #BZ) to drive a piezo-electric buzzer. The buzzer signal frequency may be selected by software from 8 types of signal divided from f_{OSC1} (32.768 kHz). Also, digital envelope which is duty ratio controlled may be added to the buzzer signal. In addition, 1-shot output circuit is built-in to output key operation check sound, and the like. Figure 9.1.1 shows the sound generator configuration. Figure 9.1.2 shows the sound generator timing chart.
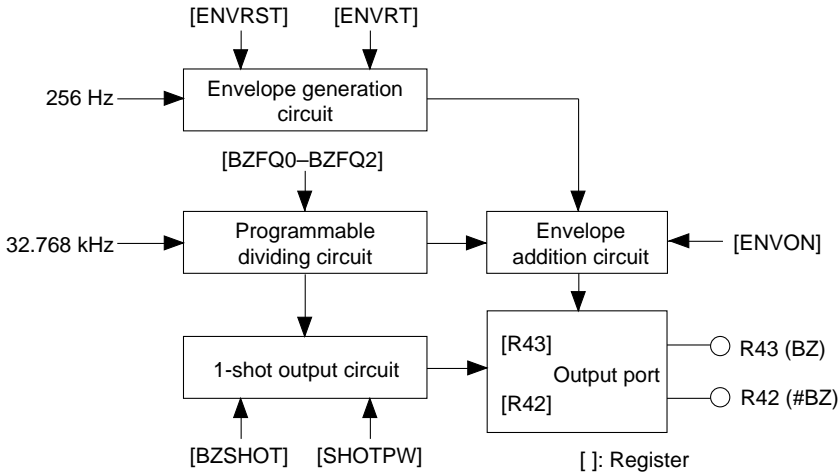
Fig. 9.1.1 Configuration of sound generator
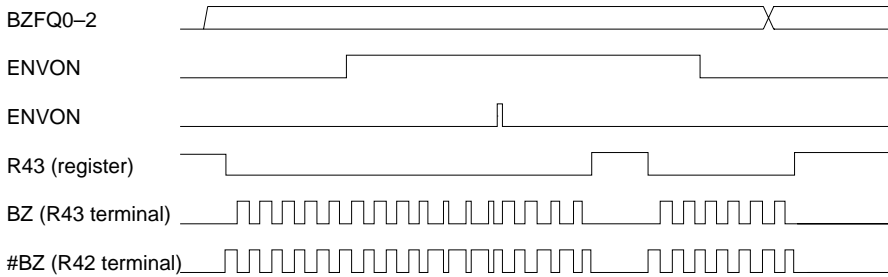
Fig. 9.1.2 Timing chart of sound generator

9.2 Mask Option

(1) Selection can be made whether to output the BZ signal from the R43 terminal.

(2) Selection can be made whether to output the #BZ signal from the R42 terminal.
   However, if the BZ signal is not output the #BZ signal cannot be output.

See Section 6.2, "Output Port" for details of the above mask option.

9.3 Frequency Setting

The frequencies of the buzzer signals (BZ, #BZ) are set by writing data to registers BZFQ0–BZFQ2.
Table 9.3.1 lists the register setting values and the frequencies that can be set.

Table 9.3.1 Setting of frequencies of buzzer signals

BZFQ2	BZFQ1	BZFQ0	Buzzer frequency (Hz)
0	0	0	4,096.0
0	0	1	3,276.8
0	1	0	2,730.7
0	1	1	2,340.6
1	0	0	2,048.0
1	0	1	1,638.4
1	1	0	1,365.3
1	1	1	1,170.3

Note: A hazard may be observed in the output waveform of the BZ and #BZ signals when switches the
buzzer frequency while the BZ and #BZ signals being output.

9.4 Digital Envelope

A duty ratio control data envelope (with duty ratio change in 8 steps) can be added to the buzzer signal
(BZ, #BZ).
Duty ratio refers to the ratio of pulse width to the pulse cycle; given that high level output time is TH,
and low level output time is TL, BZ output becomes TH/(TH+TL).
#BZ output becomes TL/(TH+TL) owing to the inverted output of the BZ output. Moreover, care is
necessary as the duty ratio differs according to the buzzer frequency.
Envelope addition is performed by writing "1" to ENVON; when "0" is written, the duty ratio is fixed at
the maximum (1/2 duty). Moreover, when envelope is added, writing "1" to ENVRST will cause the BZ
signal duty ratio to be returned to maximum.
The decay time of the envelope (time for the duty ratio to change) can be selected with the register
ENVRT. This time is 62.5 ms (16 Hz) when "0" is written, and 125 ms (8 Hz) when "1" is written.
However, a maximum difference of 4 ms is taken from envelope-ON until the first change.
Table 9.4.1 lists the duty ratio and buzzer frequencies.
Figure 9.4.1 shows the digital envelope timing chart.

Table 9.4.1 Duty ratio and buzzer frequencies

Duty ratio	Buzzer frequencies			
	4,096.6	3,276.8	2,730.7	2,340.6
	2,048.0	1,638.4	1,365.3	1,170.3
Level 1 (max.)	8/16	8/20	12/24	12/28
Level 2	7/16	7/20	11/24	11/28
Level 3	6/16	6/20	10/24	10/28
Level 4	5/16	5/20	9/24	9/28
Level 5	4/16	4/20	8/24	8/28
Level 6	3/16	3/20	7/24	7/28
Level 7	2/16	2/20	6/24	6/28
Level 8 (min.)	1/16	1/20	5/24	5/28

No change of duty level

t_{01}
t_{02-07}

$$t_{01} = 62.5 \,^{+0}_{-4} \text{ msec}$$
$$t_{02-07} = 62.5 \text{ msec}$$

$$t_{11} = 125 \,^{+0}_{-4} \text{ msec}$$
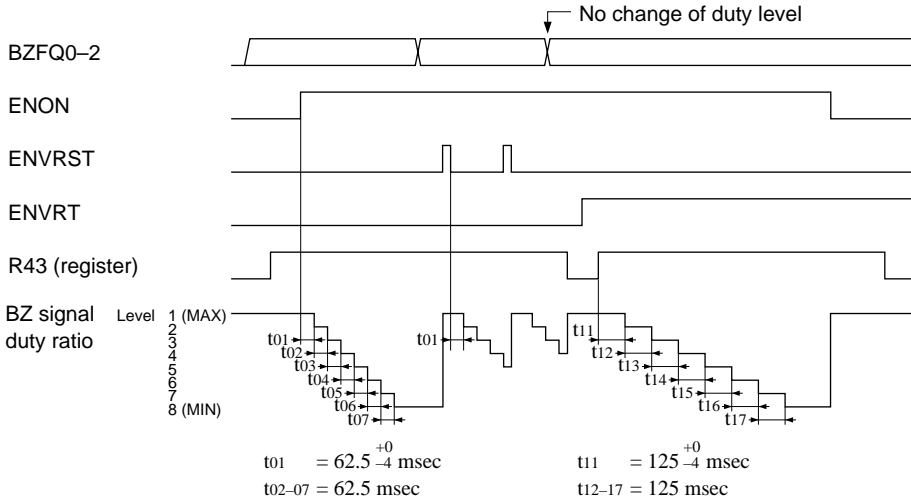$$t_{12-17} = 125 \text{ msec}$$

Fig. 9.4.1 Digital envelope timing chart

9.5 1-shot Output

In order to cause the buzzer to ring in a short period of time as in the case of key operation check sound, 1-shot output function is built-in. The time duration for buzzer signal to be output (BZ and #BZ) may be selected by SHOTPW; when "0" is written on SHOTPW, it is set to 31.25 ms and to 62.5 ms when "1" written.

Actual output operation is performed by writing "1" on BZSHOT; after performing the previously described writing operation, it synchronizes with the internal 256 Hz signal and buzzer signal is output in output port R43 (R42).

Moreover, after the set time has lapsed, it synchronizes with the same 256 Hz previously described and the buzzer signal is automatically turned off. Also, by reading BZSHOT, whether the 1-shot circuit is in operation or not may be determined with the software.

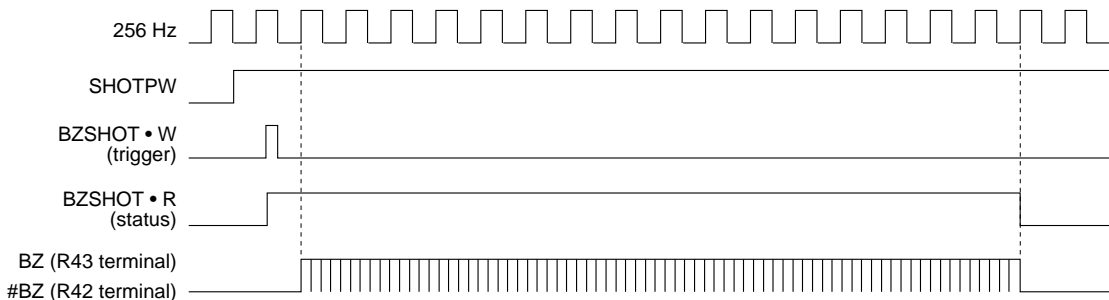Figure 9.5.1 shows the timing chart of the 1-shot output.

Fig. 9.5.1 Timing chart of 1-shot output

9.6 Control of Sound Generator

The control registers for the sound generator are explained below.

Table 9.6.1 Control registers of sound generator

Address	Register				Name	Init	1	0	Comment
	D3	D2	D1	D0					
F54H	R43	R42	R41	R40	R43	1	High Off	Low On	Output port (R43) Buzzer output (BZ)
		R/W			R42	1	High Off	Low On	Output port (R42) Clock output (FOUT) [Buzzer inverted output (#BZ)]
					R41	1	High	Low	Output port (R41)
					R40	1	High Off	Low On	Output port (R40) Clock inverted output (#FOUT)
F74H	SHOTPW	BZFQ2	BZFQ1	BZFQ0	SHOTPW	0	62.5 ms	31.25 ms	1-shot buzzer pulse width
		R/W			BZFQ2	0			Buzzer frequency selection
					BZFQ1	0			
					BZFQ0	0			
F75H	BZSHOT	ENVRST	ENVRT	ENVON	BZSHOT	0	Trigger BUSY	– READY	1-shot buzzer trigger (W) Status (R)
	W / R	W	R/W		ENVRST	RESET	Reset	–	Envelope reset
					ENVRT	0	1.0 sec	0.5 sec	Envelope cycle selection
					ENVON	0	On	Off	Envelope On/Off

BZFQ0–BZFQ2 (F74H [D0–D2], R/W)
Will select the buzzer signal frequency.

Table 9.6.2 Setting of frequencies of buzzer signals

BZFQ2	BZFQ1	BZFQ0	Buzzer frequency (Hz)
0	0	0	4,096.0
0	0	1	3,276.8
0	1	0	2,730.7
0	1	1	2,340.6
1	0	0	2,048.0
1	0	1	1,638.4
1	1	0	1,365.3
1	1	1	1,170.3

At initial reset, 4,096 Hz is selected.

ENVRST (F75H [D2], W)
This is the reset input to make the duty ratio of the buzzer signal the maximum.

When "1" is written: Reset input
When "0" is written: No operation
Reading: Always "0"

When envelope is added to the buzzer signal, by writing "1" on ENVRST, the envelope is reset and duty ratio becomes maximum. When envelope is not added, or when buzzer signal is not being output, reset operation is ineffective.

ENVON (F75H [D0], R/W)
This controls adding the envelope to the buzzer signal.

When "1" is written: Envelope added (ON)
When "0" is written: No envelope (OFF)
Reading: Valid

By writing "1" on ENVON, envelope is added to the buzzer signal. Writing "0" means envelope will not be added.
At initial reset, ENVON is set to "0" and envelope OFF will be selected.

ENVRT (F75H [D1], R/W)
Selects the attenuation time of the envelope added to the buzzer signal.

When "1" is written: 1.0 sec (125 ms $\times$ 7 = 875 ms)
When "0" is written: 0.5 sec (62.5 ms $\times$ 7 = 437.5 ms)
          Reading: Valid

The attenuation time of digital envelopes is determined by the time change for duty ratio. When "1" is written on ENVRT, attenuation time is set in 125 ms (8 Hz) units (125 ms $\times$ 7 = 875 ms), and in 62.5 ms (16 Hz) unit (62.5 ms $\times$ 7 = 437.5 ms) when "0" is written.
However, there is a maximum error of 4 ms from envelope ON to the first change in both cases.
At initial reset, ENVRT is set to "0".

R43, R42 (F54H [D3, D2], R/W)
Controls the output of the buzzer signals (BZ, #BZ).

When "0" is written: Buzzer signal output
When "1" is written: Low level (DC)
          Reading: Valid

When "0" is set on R43, BZ signal is generated from R43 terminal, and if R42 is set to #BZ output, #BZ signal (inverted signal of BZ) is generated at the same time.
When "1" is set on R43, R43 terminal (R42 too, if #BZ output is selected) becomes of low (Vss) level output.
However, R42 with #BZ output selected, may be used as a 1-bit general register capable of read/write function, the data of which register does not affect #BZ (R42 terminal output).
At initial reset, both R43 and R42 are set to "1".

Note: BZ and #BZ output signals may produce hazards during ON/OFF switching.

SHOTPW (F74H [D3], R/W)
Sets the output time duration of the 1-shot buzzer.

When "1" is written: 62.5 ms
When "0" is written: 31.25 ms
          Reading: Valid

Output time duration is set to 62.5 ms or 31.25 ms by writing "1" or "0", respectively, on SHOTPW.
At initial reset, SHOTPW is set to "0".

BZSHOT (F75H [D3], W, R)
Controls the output of the 1-shot buzzer.

• **During writing operation**
When "1" is written: Trigger
When "0" is written: No operation

When "1" is written on BZSHOT, the 1-shot circuit operates and the buzzer signal (BZ and #BZ) is output.
The 1-shot buzzer operates only when the regular buzzer output is in the OFF (R43 = "0") state and writing to BZSHOT becomes invalid in the ON (R43 = "1") state.

• **During reading operation**
When "1" is read: Busy
When "0" is read: Ready

The BZSHOT reads "1" when the 1-shot buzzer is ringing and "0" when it is not ringing. The period of "1" is from the time of the trigger until the buzzer output is turned OFF.
At initial reset, "0" is read.

9.7 Programming Notes

(1) The BZ and #BZ signals may generate hazards in the following cases:

- When the content of R43 register is changed, BZ and #BZ signals are switched ON or OFF.

- When the contents of buzzer frequency selection registers (BZFQ0–BZFQ2) while the buzzer signal (BZ and #BZ) is being output.

(2) The 1-shot buzzer operates only when the regular buzzer output is in the OFF (R43 = "0") state and writing to BZSHOT becomes invalid in the ON (R43 = "1") state.

CHAPTER *10* INTERRUPT AND HALT

The E0C6007 has the following interrupt functions built-in, and masking is possible for each one.

External interrupt	• Input interrupt (1 system)
Internal interrupt	• Clock timer interrupt (3 systems)
	• Stopwatch timer interrupt (2 systems)
	• Programmable timer interrupt (1 system)

To allow the interrupt to function, it is necessary that the interrupt mask register of the required system be set to "1" (enable) and, at the same time, the interrupt flag be set to "1" (EI).
When interrupt occurs, the interrupt flag is automatically reset to "0" (DI), prohibiting the any consequent interrupts.

The CPU stops the operating clock when a HALT instruction is executed and then enters the HALT state.
Re-running the CPU from the HALT state requires issuance of interrupt request.
If return through interrupt request is not effective, return is effected from initial reset by the watchdog timer.

Figure 10.1 shows the configuration of the interrupt circuit.
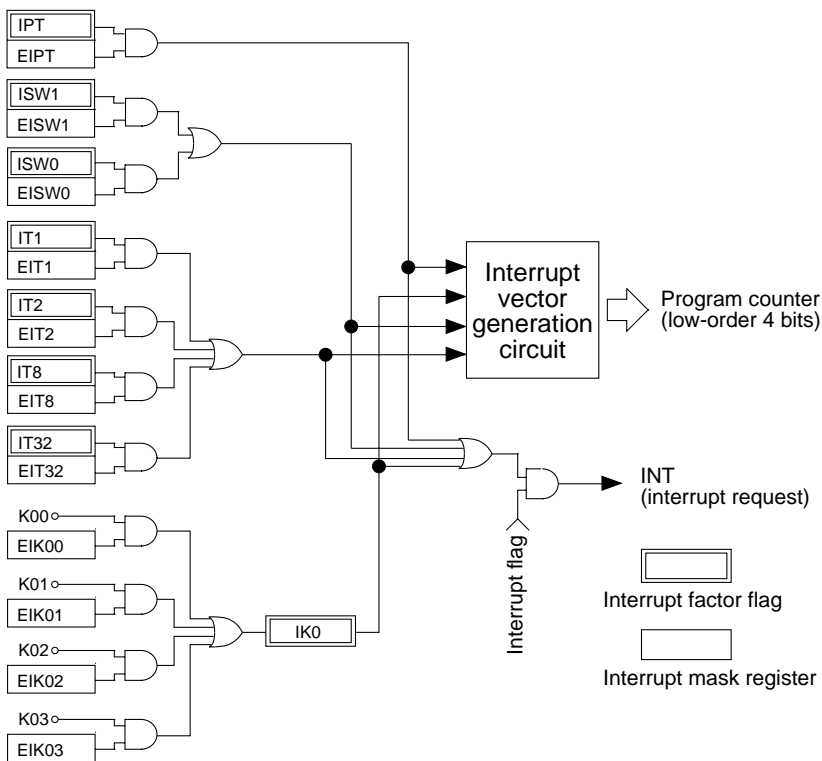See the explanations of the relevant circuits for interrupt details.

Fig. 10.1 Configuration of interrupt circuit

10.1 Interrupt Factor Flag and Interrupt Mask

The corresponding interrupt factor flag is set to "1" with the individual interrupt element.
If the following conditions exist, interrupt for the CPU occurs when the interrupt factor flag is set to "1".

• The corresponding interrupt mask register is set at "1" (enable).
• The interrupt flag is set at "1" (EI).

The interrupt factor flag is reset to "0" at the read-only register by reading the data.
Be sure that the interrupt factor flag reading is done with the interrupt in the DISABLE state (DI).
Reading the interrupt factor flag while in the ENABLE state (EI) may cause malfunction.
At initial reset, the interrupt factor flag is reset to "0".

The interrupt can be masked by the corresponding interrupt mask register.
The interrupt mask register is a register capable of read/write operation; by writing "1", it is enabled
(interrupt is allowed) and by writing "0", it is masked (interrupt is prohibited).
Be sure that writing to the interrupt mask register is done with the interrupt in the DISABLE state (DI).
Writing to the interrupt mask register while in the ENABLE state (EI) may cause malfunction.
At initial reset, the interrupt mask register is set to "0".

The interrupt factor flag is set to "1" by interrupt factor even if the interrupt is masked. (The input
interrupt factor flag IK0 will be eliminated.)

Table 10.1.1 shows the correspondence between interrupt factor flags and interrupt mask registers.

Table 10.1.1 Interrupt factor flags and interrupt mask registers

Interrupt factor	Interrupt factor flag	Interrupt mask register
Falling edge of clock timer (1 Hz)	IT1 (F00H [D3])	EIT1 (F10H [D3])
Falling edge of clock timer (2 Hz)	IT2 (F00H [D2])	EIT2 (F10H [D2])
Falling edge of clock timer (8 Hz)	IT8 (F00H [D1])	EIT8 (F10H [D1])
Falling edge of clock timer (32 Hz)	IT32 (F00H [D0])	EIT32 (F10H [D0])
Overflow of stopwatch timer (SWH) (1 Hz)	ISW1 (F01H [D1])	EISW1 (F11H [D1])
Overflow of stopwatch timer (SWL) (10 Hz)	ISW0 (F01H [D0])	EISW0 (F11H [D0])
Changing of input (K00–K03) status	IK0 (F04H [D0])	EIK03 (F14H [D3])
		EIK02 (F14H [D2])
		EIK01 (F14H [D1])
		EIK00 (F14H [D0])
Counter value of programmable timer = 00H	IPT (F02H [D0])	EIPT (F12H [D0])

10.2 Interrupt Vector

When an interrupt request is issued to the CPU, the CPU starts interrupt processing.
Interrupt processing is accomplished by the following steps after the instruction being executed is completed.

1. The address (value of the program counter) of the program which should be run next is saved in the stack area (RAM).

2. The vector address (1 page 02H–0CH) for each interrupt request is set to the program counter.

3. Branch instruction written to the vector is effected (branch to software interrupt processing routine).

Note: Time equivalent to 12 cycles of CPU system clock is required for steps 1 and 2.

The interrupt request and interrupt vector correspondence is shown in Table 10.2.1.

Table 10.2.1 Interrupt request and interrupt vectors

Interrupt vector (PCP and PCS)	Interrupt request	Priority
102H	Clock timer interrupt	Low
104H	Stopwatch timer interrupt	↑
106H	Input (K00–K03) interrupt	↓
10CH	Programmable timer interrupt	High

When multiple interrupts simultaneously occur, the high priority vector address is set to the program counter.

10.3 Programming Notes

(1) The interrupt factor flag is set when the interrupt conditions are established, regardless of the setting of the interrupt mask register. Note, however, that the input interrupt factor flag (IK0) will be eliminated.

(2) When an interrupt occurs, the interrupt flag will be reset by the hardware and it will become DI status. After completion of the interrupt processing, set to the EI status through the software as needed. Moreover, the nesting level may be set to be programmable by setting to the EI state at the beginning of the interrupt processing routine.

(3) The interrupt factor flags must always be reset before setting the EI status. When the interrupt mask register has been set to "1", the same interrupt will occur again if the EI status is set unless of resetting the interrupt factor flag.

(4) The interrupt factor flag will be reset by reading through the software. Because of this, when multiple interrupt factor flags are to be assigned to the same address, perform the flag check after the contents of the address has been stored in the RAM. Direct checking with the FAN instruction will cause all the interrupt factor flag to be reset.

(5) Be sure that the interrupt factor flag reading is done with the interrupt in the DISABLE state (DI). Reading the interrupt factor flag while in the ENABLE state (EI) may cause malfunction.

(6) Be sure that writing to the interrupt mask register is done with the interrupt in the DISABLE state (DI). Writing to the interrupt mask register while in the ENABLE state (EI) may cause malfunction.

(7) When multiple interrupts simultaneously occur, the high priority vector address is set to the program counter.

(8) If an interrupt occurs while the CPU is processing some other interrupt request of which the priority is lower than the new one but the CPU has not fetched the interrupt vector, the CPU may shift to a vector address (one of among 102H, 104H, 106H and 10CH) that is different from the new interrupt. Therefore, make sure the interrupt factor flag has been set immediately after the branch instruction stored in the vector address is executed and quit the interrupt processing if it has not been set. Furthermore, place a branch instruction for executing the interrupt processing routine in the vector address 10CH because the CPU may shift to that address. By setting the start address of the programmable timer interrupt processing routine as the branch destination, the priority level by hardware can be maintained.

If the program does not have the individual processing routine for each interrupt (for example, in the case of all interrupts using the same processing routine in which the type of interrupt is judged by reading the interrupt flags, or in the case of the main routine checking all the interrupt flags by branching the flow the RET instruction stored in all the vector address), place the instruction the same as the other interrupt vectors in address 10CH.

When the interrupt function is not used, it is not necessary to pay attention to the above mentioned precautions.

CHAPTER 11 SUMMARY OF NOTES

11.1 Notes for Low Current Consumption

The E0C6007 contains control registers for each of the circuits so that current consumption can be lowered. These control registers lower the current consumption through programs that operate the circuits at the minimum levels.

The following text explains the circuits that can control operation and their control registers. Refer to these when putting programs together.

Table 11.1.1 Circuits and control registers

Circuits (and Items)	Control registers	Order of consumed current
CPU	HALT instruction	See electrical characteristics (Chapter 13)
CPU operation frequency	CLKCHG, OSCC	See electrical characteristics (Chapter 13)
Internal regulated voltage	VSC0, VSC1	See electrical characteristics (Chapter 13)
Heavy load protection mode	HLMOD	See electrical characteristics (Chapter 13)

Below are the circuit status at initial reset.

CPU: Operating
CPU operating frequency: OSC1 side (CLKCHG = "0"),
                              OSC3 oscillation circuit is stopped (OSCC = "0")
Internal regulated voltage: -1.2 V (VSC0, VSC1 = "0")
                              When CR oscillation is selected by mask option, the internal regulated
                              voltage becomes -2.1 V.
Heavy load protection mode: Normal operating mode (HLMOD = "0")

Also, be careful about panel selection because the current consumption can differ by the order of several µA on account of the LCD panel characteristics.

11.2 Summary of Notes by Function

Here, the cautionary notes are summed up by function category. Keep these notes well in mined when programming.

Memory

Memory is not mounted in unused area within the memory map and in memory area not indicated in this manual. For this reason, normal operation cannot be assured for programs that have been prepared with access to these areas.

Heavy load protection mode

(1) When driving heavy loads, set it to heavy load protection mode. Unless it is necessary, be careful not to set the heavy load protection mode with the software.

(2) Perform heavy load driving only after setting up at least 1 ms wait time through the software, after switching to the heavy load protection mode. (See Figure 3.2.2.1.)

(3) When the heavy load protection mode is to canceled after completion of heavy load driving, set up at least 2 seconds wait time through the software. (See Figure 3.2.2.1.)

Watchdog timer

(1) The watchdog timer must reset within 3-second cycles by the software.

(2) When the clock timer is reset (TMRST ← "1"), the watchdog timer is counted up; reset the watchdog immediately after if necessary.

Oscillation circuit

(1) When high-speed operation of the CPU is not required, observe the following reminders to minimize power current consumption.

Set the CPU operating clock to OSC1.
Turn the OSC3 oscillation OFF.
Set the internal operating voltage (V_{S1}) to -1.2 V or -2.1 V.

(2) When the CPU is to be operated with OSC1, set the operating voltage to -1.2 V if the power voltage is less than 3.1 V (V_{DD}–V_{SS} < 3.1 V); set the operating voltage to -2.1 V if the voltage is 3.1 V or more (V_{DD}–V_{SS} ≥ 3.1 V). Moreover, because -1.2 V will be set during initial reset, be sure to execute the previous process at the beginning of the initial routine. Note, however, that it can be used fixed at 1.2 V (at OSC1 operation) for power whose initial value is 3.6 V or less as in lithium batteries.

(3) When switching V_{S1} from -1.2 V (for OSC1 crystal oscillation circuit) to -3.0 V (for OSC3 oscillation circuit), or vice versa, be sure to hold the -2.1 V setting for more than 5 ms first for power voltage stabilization.

$(VSC1, VSC0) = (0, 0) \rightarrow (0, 1) \rightarrow 5$ ms WAIT $\rightarrow (1, \times)$
$= (1, \times) \rightarrow (0, 1) \rightarrow 5$ ms WAIT $\rightarrow (0, 0)$

$= (0, 0) \rightarrow (1, \times)$ is prohibited
$= (1, \times) \rightarrow (0, 0)$ is prohibited

(4) When switching the CPU operating clock from OSC1 to OSC3, follow the flow chart shown in Figure 5.6.1 and then proceed with software processing.

(5) Use separate instructions to switch the clock from OSC3 to OSC1 and turn the OSC3 oscillation OFF. Simultaneous processing with a single instruction may cause malfunction of the CPU.

(6) When CR oscillation has been selected by the mask option, internal regulated voltage becomes -2.1 V and will never become -1.2 V.

Input port (Kxx)

(1) When changing the input port from low level to high level with a pull up resistor, a delay in the waveform rise time will occur depending on the time constant of the pull up resistor and input gate capacity. Hence, when reading data from the input port, set an appropriate waiting time. Care is particularly required for key matrix configuration scanning. For reference, approximately 500 μs waiting time is required.

(2) Input interrupt programming related precautions

When the content of the mask register is rewritten, while the port K input is in
the active status, the input interrupt factor flag is set at ①.

Fig. 11.2.1 Input interrupt timing

When using an input interrupt, if you rewrite the content of the mask register, when the value of the input terminal which becomes the interrupt input is in the active status (input terminal = low status), the factor flag for input interrupt may be set.

For example, a factor flag is set with the timing of ① shown in Figure 11.2.1. However, when clearing the content of the mask register with the input terminal kept in the low status and then setting it, the factor flag of the input interrupt is again set at the timing that has been set.

Consequently, when the input terminal is in the active status (low status), do not rewrite the mask register (clearing, then setting the mask register), so that a factor flag will only set at the rising edge in this case. When clearing, then setting the mask register, set the mask register, when the input terminal is not in the active status (high status).

Output port (Rxx)

(1) When BZ, #BZ, FOUT, #FOUT, and PTCLK (DC) are selected by mask option, a hazard may be observed in the output waveform when the data of the output register changes.

(2) Because the R32 and R33 ports gain high impedance during initial reset, be careful when using them as interface with external devices and the like.

I/O port (Pxx)

(1) When the I/O port is set at output mode, and low impedance load is connected to the port terminal, the data written and read may differ.

(2) If the state of the I/O port meets all of the following 4 conditions, the reading data will be undefined:
 • The input/output mode is set at output mode
 • Output specification is set at Nch open drain
 • The content of the data register is "1"
 • The pull up resistor turned is OFF

LCD driver

Because at initial reset, the contents of segment data memory and LC0–LC3 are undefined, there is need to initialize by software.

Clock timer

(1) When the clock timer has been reset, the interrupt factor flag (IT) may sometimes be set to "1". Consequently, perform flag read (reset the flag) as necessary at reset.

(2) Because the watchdog timer counts up during reset as in the above (1), reset the watchdog timer as necessary.

(3) When the low-order digits (TM0–TM3) and high-order digits (TM4–TM7) are consecutively read, proper reading may not be obtained due to the carry from the low-order digits into the high-order digits (when the reading of the low-order digits and high-order digits span the timing of the carry). For this reason, perform multiple reading of timer data, make comparisons and use matching data as result.

Stopwatch timer

When data of the counter is read at run mode, perform the reading after suspending the counter once and then set SWRUN to "1" again. Moreover, it is required that the suspension period not exceed 976 μs (1/4 cycle of 256 Hz).

Programmable timer

(1) When initiating programmable timer count, perform programming by the following steps:
   1. Set the initial data to RD0–RD7.
   2. Reset the programmable timer by writing "1" to PTRST.
   3. Start the down-count by writing "1" to PTRUN.

(2) When the reload register (RD0–RD7) value is set at "00H", the down-counter becomes a 256-value counter.

(3) When data of the timer is read consecutively in 8 bits in the RUN mode, perform the reading after suspending the timer once and then set the PTRUN to "1" again. Moreover, it is required that the suspension period be within 1/4 cycle of the input clock (in case of 1/2 duty). Accordingly, when the input clock is a fast clock faster than 256 Hz, high speed processing by OSC3 is required.

Sound generator

(1) The BZ and #BZ signals may generate hazards in the following cases:

   • When the content of R43 register is changed, BZ and #BZ signals are switched ON or OFF.

   • When the contents of buzzer frequency selection registers (BZFQ0–BZFQ2) while the buzzer signal (BZ and #BZ) is being output.

(2) The 1-shot buzzer operates only when the regular buzzer output is in the OFF (R43 = "0") state and writing to BZSHOT becomes invalid in the ON (R43 = "1") state.

Interrupt

(1) The interrupt factor flag is set when the interrupt conditions are established, regardless of the setting of the interrupt mask register. Note, however, that the input interrupt factor flag (IK0) will be eliminated.

(2) When an interrupt occurs, the interrupt flag will be reset by the hardware and it will become DI status. After completion of the interrupt processing, set to the EI status through the software as needed. Moreover, the nesting level may be set to be programmable by setting to the EI state at the beginning of the interrupt processing routine.

(3) The interrupt factor flags must always be reset before setting the EI status. When the interrupt mask register has been set to "1", the same interrupt will occur again if the EI status is set unless of resetting the interrupt factor flag.

(4) The interrupt factor flag will be reset by reading through the software. Because of this, when multiple interrupt factor flags are to be assigned to the same address, perform the flag check after the contents of the address has been stored in the RAM. Direct checking with the FAN instruction will cause all the interrupt factor flag to be reset.

(5) Be sure that the interrupt factor flag reading is done with the interrupt in the DISABLE state (DI). Reading the interrupt factor flag while in the ENABLE state (EI) may cause malfunction.

(6) Be sure that writing to the interrupt mask register is done with the interrupt in the DISABLE state (DI). Writing to the interrupt mask register while in the ENABLE state (EI) may cause malfunction.

(7) When multiple interrupts simultaneously occur, the high priority vector address is set to the program counter.

(8) If an interrupt occurs while the CPU is processing some other interrupt request of which the priority is lower than the new one but the CPU has not fetched the interrupt vector, the CPU may shift to a vector address (one of among 102H, 104H, 106H and 10CH) that is different from the new interrupt. Therefore, make sure the interrupt factor flag has been set immediately after the branch instruction stored in the vector address is executed and quit the interrupt processing if it has not been set. Furthermore, place a branch instruction for executing the interrupt processing routine in the vector address 10CH because the CPU may shift to that address. By setting the start address of the programmable timer interrupt processing routine as the branch destination, the priority level by hardware can be maintained.

If the program does not have the individual processing routine for each interrupt (for example, in the case of all interrupts using the same processing routine in which the type of interrupt is judged by reading the interrupt flags, or in the case of the main routine checking all the interrupt flags by branching the flow the RET instruction stored in all the vector address), place the instruction the same as the other interrupt vectors in address 10CH.

When the interrupt function is not used, it is not necessary to pay attention to the above mentioned precautions.

11.3 Precautions on Mounting

Oscillation Circuit

- Oscillation characteristics change depending on conditions (board pattern, components used, etc.). In particular, when a ceramic oscillator or crystal oscillator is used, use the oscillator manufacturer's recommended values for constants such as capacitance and resistance.

- Disturbances of the oscillation clock due to noise may cause a malfunction. Consider the following points to prevent this:

  (1) Components which are connected to the OSC1 (OSC3) and OSC2 (OSC4) terminals, such as oscillators, resistors and capacitors, should be connected in the shortest line.

  (2) As shown in the figure, make a V_{DD} pattern as large as possible at circumscription of the OSC1 (OSC3) and OSC2 (OSC4) terminals and the components connected to these terminals.
  Furthermore, do not use this V_{DD} pattern for any purpose other than the oscillation system.

Sample V_{DD} pattern (OSC3)
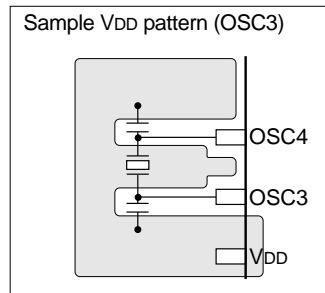
- In order to prevent unstable operation of the oscillation circuit due to current leak between OSC1 (OSC3) and V_{SS}, please keep enough distance between OSC3 and V_{SS} or other signals on the board pattern.

Reset Circuit

- The power-on reset signal which is input to the #RESET terminal changes depending on conditions (power rise time, components used, board pattern, etc.).
  Decide the time constant of the capacitor and resistor after enough tests have been completed with the application product.
  When using the built-in pull-up resistor of the #RESET terminal, take into consideration dispersion of the resistance for setting the constant.

- In order to prevent any occurrences of unnecessary resetting caused by noise during operating, components such as capacitors and resistors should be connected to the #RESET terminal in the shortest line.

Power Supply Circuit

- Sudden power supply variation due to noise may cause malfunction. Consider the following points to prevent this:

  (1) The power supply should be connected to the V_{DD} and V_{SS} terminal with patterns as short and large as possible.
  Furthermore, similar consideration is necessary when V_{L1}–V_{L5} are supplied from outside the IC.

(2) When connecting between the V_{DD} and V_{SS} terminals with a bypass capacitor, the terminals should be connected as short as possible.

```
┌─────────────────────────────────────────────────────┐
│ Bypass capacitor connection example                  │
│                                                       │
│      ┌───┐                      ┌───┐                 │
│   ┌──┤   │VDD               ┌───┤   │VDD              │
│   │  └───┘          ➡        │   └───┘                │
│  ═╪═ ┌───┐               ═╪═ └───┐                    │
│   └──┤   │VSS                └───┤   │VSS              │
│      └───┘                       └───┘                │
└─────────────────────────────────────────────────────┘
```
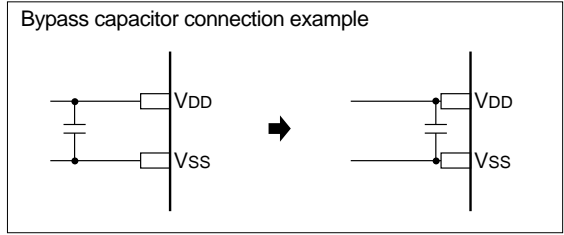
(3) Components which are connected to the V_{S1}, V_{L1}–V_{L5} terminals, such as capacitors and resistors, should be connected in the shortest line.
In particular, the V_{L1}–V_{L5} voltages affect the display quality.

• Do not connect anything to the V_{L1}–V_{L5} terminals when the LCD driver is not used.
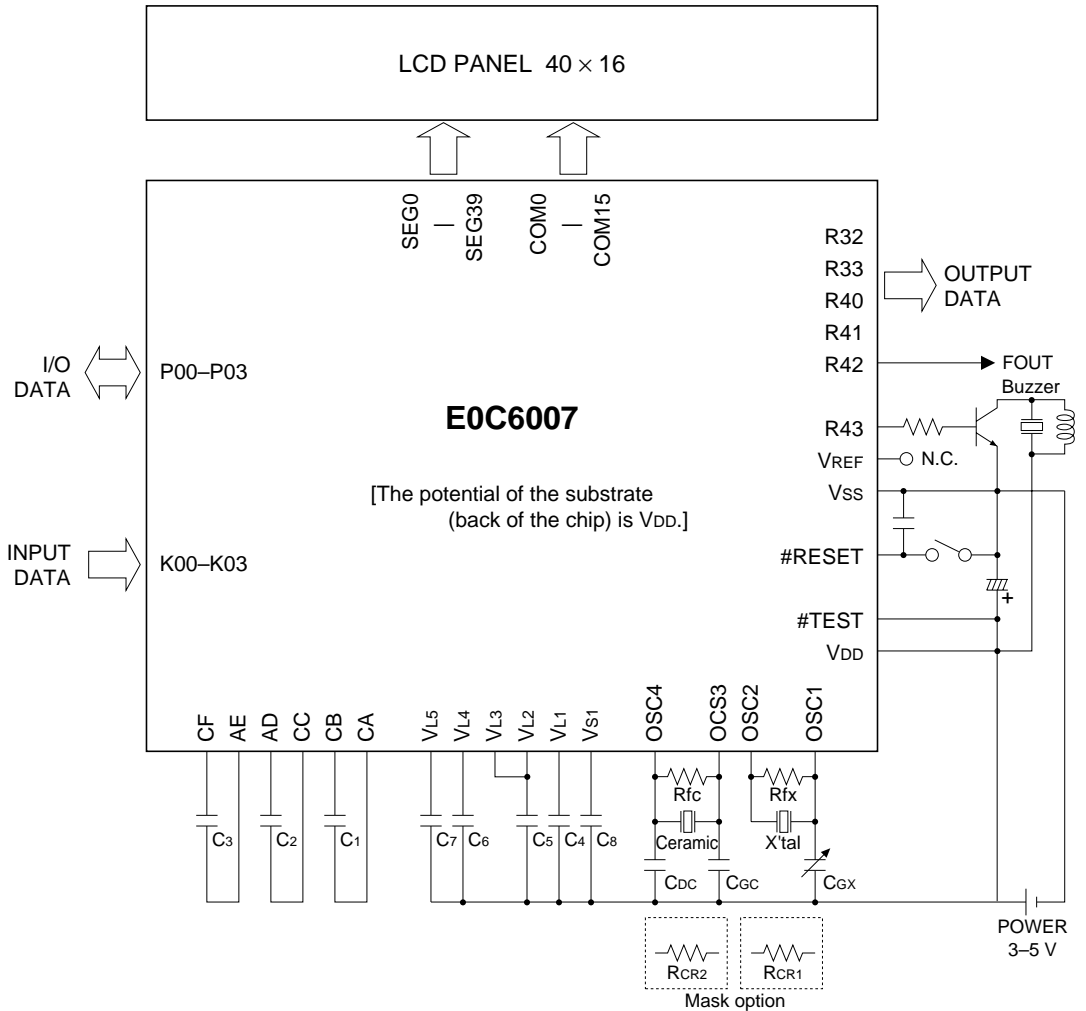
Arrangement of Signal Lines

• In order to prevent generation of electromagnetic induction noise caused by mutual inductance, do not arrange a large current signal line near the circuits that are sensitive to noise such as the oscillation unit.

• When a signal line is parallel with a high-speed line in long distance or intersects a high-speed line, noise may generated by mutual interference between the signals and it may cause a malfunction. Do not arrange a high-speed signal line especially near circuits that are sensitive to noise such as the oscillation unit.

```
┌───────────────────────────────────────────┐
│ Prohibited pattern                          │
│                                             │
│         ┌───┐                               │
│      ═╪═ │   ┌───┐                          │
│         │   ┤   │OSC4                        │
│       ▭ │≶  └───┘                           │
│         │   ┌───┐                           │
│      ═╪═ │   ┤   │OSC3                        │
│         │   └───┘                           │
│         │   ┌───┐                           │
│      ──►─┘   ┤   │VDD                        │
│             └───┘                           │
│  Large current signal line                  │
│  High-speed signal line                     │
└───────────────────────────────────────────┘
```
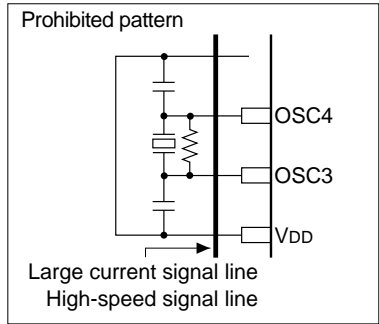
Precautions for Visible Radiation (when bare chip is mounted)

• Visible radiation causes semiconductor devices to change the electrical characteristics. It may cause this IC to malfunction. When developing products which use this IC, consider the following precautions to prevent malfunctions caused by visible radiation.

(1) Design the product and implement the IC on the board so that it is shielded from visible radiation in actual use.

(2) The inspection process of the product needs an environment that shields the IC from visible radiation.

(3) As well as the face of the IC, shield the back and side too.

CHAPTER 12 BASIC EXTERNAL CONNECTION DIAGRAM

LCD PANEL 40×16

SEG0 — SEG39 COM0 — COM15

R32
R33
R40
R41
R42

OUTPUT DATA

FOUT
Buzzer

I/O DATA P00–P03

R43
V_{REF} N.C.
V_{SS}

E0C6007

[The potential of the substrate (back of the chip) is V_{DD}.]

#RESET

INPUT DATA K00–K03

#TEST
V_{DD}

POWER 3–5 V

CF AE AD CC CB CA V_{L5} V_{L4} V_{L3} V_{L2} V_{L1} V_{S1} OSC4 OCS3 OSC2 OSC1

C_3 C_2 C_1 C_7 C_6 C_5 C_4 C_8

Rfc Rfx
Ceramic X'tal
C_{DC} C_{GC} C_{GX}

R_{CR2} R_{CR1}
Mask option

X'tal	Crystal oscillator	32.768 kHz, C_I(Max)=35 kΩ
Rfx	Feedback resistor	10 MΩ
C_{GX}	Trimmer capacitor	5–25 pF
(R_{CR1})	Resistor for OSC1 CR oscillation	1.6 MΩ (32 kHz Typ.)
Ceramic	Ceramic oscillator	500 kHz–2 MHz
Rfc	Feedback resistor	1 MΩ
C_{GC}	Gate capacitor	100 pF
C_{DC}	Drain capacitor	100 pF
(R_{CR2})	Resistor for OSC3 CR oscillation	20 kΩ–100 kΩ (VSC=2) 40 kΩ–100 kΩ (VSC=1)

C_1	Booster capacitor (1)	0.1μF ∗1
C_2	Booster capacitor (2)	0.1μF ∗1
C_3	Booster capacitor (3)	0.1μF ∗1
C_4	Capacitor between V_{DD} and V_{L1}	0.1μF ∗1
C_5	Capacitor between V_{DD} and V_{L2}	0.1μF ∗1
C_6	Capacitor between V_{DD} and V_{L4}	0.1μF ∗1
C_7	Capacitor between V_{DD} and V_{L5}	0.1μF ∗1
C_8	Capacitor between V_{DD} and V_{S1}	0.1μF

∗1 When the load on the liquid crystal system is large, increase the capacitance of the voltage booster capacitors (C_1–C_3) and the capacitors between V_{DD} and liquid crystal system power (C_4–C_7).

Note: The above table is simply an example. Refer to Chapter 13, "Electrical Characteristics", for detailed characteristics.

CHAPTER 13 ELECTRICAL CHARACTERISTICS

13.1 Absolute Maximum Rating

(V_{DD}=0V)

Item	Symbol	Rated value	Unit
Supply voltage	V_{SS}	-7.0 to 0.5	V
Input voltage (1)	V_I	V_{SS} - 0.3 to 0.5	V
Input voltage (2)	V_{IOSC}	V_{S1} - 0.3 to 0.5	V
Permissible total output current ∗1	ΣI_{VSS}	10	mA
Operating temperature	Topr	-20 to 70	°C
Storage temperature	Tstg	-65 to 150	°C
Soldering temperature / time	Tsol	260°C, 10sec (lead section)	–
Permissible dissipation ∗2	P_D	250	mW

∗1 The permissible total output current is the sum total of the current (average current) that simultaneously flows from the output pin (or is drawn in).

∗2 In case of plastic package.

13.2 Recommended Operating Conditions

(Ta=-20 to 70°C)

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Supply voltage	V_{SS}	V_{DD}=0V	VSC="0"	-3.8	-3.0	-1.8	V
			VSC="1"	-5.5	-3.0	-2.2	V
			VSC="2"	-5.5	-5.0	-3.5	V
Oscillation frequency (1)	f_{OSC1}			20	32.768	50	kHz
Oscillation frequency (2)	f_{OSC3}	VSC="1"		50	1,000	1,200	kHz
Oscillation frequency (3)	f_{OSC3}	VSC="2"		50	2,000	2,300	kHz
Voltage booster capacitor (1)	C_1				0.1		μF
Voltage booster capacitor (2)	C_2				0.1		μF
Voltage booster capacitor (3)	C_3				0.1		μF
Capacitor between V_{DD} and V_{L1}	C_4				0.1		μF
Capacitor between V_{DD} and V_{L2}	C_5				0.1		μF
Capacitor between V_{DD} and V_{L4}	C_6				0.1		μF
Capacitor between V_{DD} and V_{L5}	C_7				0.1		μF
Capacitor between V_{DD} and V_{S1}	C_8				0.1		μF

13.3 DC Characteristics

Conditions unless otherwise specified:

V_{DD}=0V, V_{SS}=-3.0V, V_{L1}=-1.0V, V_{L2}=-2.0V, V_{L4}=-3.0V, V_{L5}=-4.0V, f_{OSC1}=32.768kHz, f_{OSC3}=1MHz, Ta=25°C, C_1–C_8=0.047μF

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
High-level input voltage (1)	V_{IH1}	V_{SS}=-2.2 to -5.5V	K00–03, P00–03	0.2·V_{SS}		0	V
Low-level input voltage (1)	V_{IL1}	Ta=25°C		V_{SS}		0.8·V_{SS}	V
High-level input voltage (2)	V_{IH2}	V_{SS}=-2.2 to -5.5V	#RESET	-0.2		0	V
Low-level input voltage (2)	V_{IL2}	Ta=25°C		V_{SS}		V_{SS}+0.2	V
High-level input current	I_{IH}	V_{SS}=-3.0V, V_{IH}=0V	K00–03, P00–03, #RESET	0		0.5	μA
Low-level input current (1)	I_{IL1}	V_{SS}=-3.0V, V_{IL1}=V_{SS} With Pull-up resistor		-45		-15	μA
Low-level input current (2)	I_{IL2}	V_{SS}=-3.0V, V_{IL2}=V_{SS} No Pull-up resistor		-0.5		0	μA
High-level output current (1)	I_{OH1}	V_{SS}=-2.2V V_{OH1}=-0.5V	P00–03, R32, R33, R40, R41			-1.0	mA
Low-level output current (1)	I_{OL1}	V_{SS}=-2.2V, V_{OL1}=V_{SS}+0.5V		4.0			mA
High-level output current (2)	I_{OH2}	V_{SS}=-2.2V V_{OH2}=-0.5V	R42, R43			-2.0	mA
Low-level output current (2)	I_{OL2}	V_{SS}=-2.2V, V_{OL2}=V_{SS}+0.5V		8.0			mA
Common output current	I_{OH3}	V_{OH3}=-0.05V	COM0–15			-30	μA
	I_{OL3}	V_{OL3}=V_{L5}+0.05V		30			μA
Segment output current	I_{OH4}	V_{OH4}=-0.05V	SEG0–39			-10	μA
	I_{OL4}	V_{OL4}=V_{L5}+0.05V		10			μA

13.4 Analog Circuit Characteristics and Consumed Current

Conditions unless otherwise specified:

V_{DD}=0V, V_{SS}=-3.0V, V_{L1}=-1.0V, V_{L2}=-2.0V, V_{L4}=-3.0V, V_{L5}=-4.0V, f_{OSC1}=32.768kHz, f_{OSC3}=1MHz, Ta=25°C, C_1~C_8=0.047μF

| Item	Symbol	Condition		Min.	Typ.	Max.	Unit
LCD drive voltage (Normal mode)	V_{L1}	Connects a 1MΩ load resistance between V_{DD} and V_{L1} (No panel load)		$1/2 \cdot V_{L2}$ -0.1		$1/2 \cdot V_{L2}$ ×0.95	V
	V_{L2}	Connects a 1MΩ load resistance between V_{DD} and V_{L2} (No panel load)	LC="0"		-2.06		V
			LC="1"		-2.11		
			LC="2"		-2.17		
			LC="3"		-2.22		
			LC="4"		-2.27		
			LC="5"		-2.32		
			LC="6"		-2.38		
			LC="7"	Typ. ×1.12	-2.43	Typ. ×0.88	
			LC="8"		-2.48		
			LC="9"		-2.53		
			LC="10"		-2.59		
			LC="11"		-2.64		
			LC="12"		-2.69		
			LC="13"		-2.74		
			LC="14"		-2.80		
			LC="15"		-2.85		
	V_{L4}	Connects a 1MΩ load resistance between V_{DD} and V_{L4} (No panel load)		$3/2 \cdot V_{L2}$		$3/2 \cdot V_{L2}$ ×0.95	V
	V_{L5}	Connects a 1MΩ load resistance between V_{DD} and V_{L5} (No panel load)		$2 \cdot V_{L2}$		$2 \cdot V_{L2}$ ×0.95	V
LCD drive voltage (Heavy load protection mode)	V_{L1}	Connects a 1MΩ load resistance between V_{DD} and V_{L1} (No panel load)	LC="0"		-1.05		V
			LC="1"		-1.08		
			LC="2"		-1.11		
			LC="3"		-1.13		
			LC="4"		-1.16		
			LC="5"		-1.19		
			LC="6"		-1.21		
			LC="7"	Typ. ×1.12	-1.24	Typ. ×0.88	
			LC="8"		-1.26		
			LC="9"		-1.29		
			LC="10"		-1.32		
			LC="11"		-1.34		
			LC="12"		-1.37		
			LC="13"		-1.40		
			LC="14"		-1.42		
			LC="15"		-1.45		
	V_{L2}	Connects a 1MΩ load resistance between V_{DD} and V_{L2} (No panel load)		$2 \cdot V_{L1}$		$2 \cdot V_{L1}$ ×0.90	V
	V_{L4}	Connects a 1MΩ load resistance between V_{DD} and V_{L4} (No panel load)		$3 \cdot V_{L1}$		$3 \cdot V_{L1}$ ×0.90	V
	V_{L5}	Connects a 1MΩ load resistance between V_{DD} and V_{L5} (No panel load)		$4 \cdot V_{L1}$		$4 \cdot V_{L1}$ ×0.90	V
Current consumption [1] (OSC1/crystal oscillation)	I_{hlt}	During HALT (VSC="0", OSCC="0")			2.5	5.0	μA
	I_{EX1}	During operation at 32kHz (VSC="0", OSCC="0")			6.5	9.0	μA
	I_{EX2}	During operation at 1MHz (VSC="1")			400	600	μA
	I_{EX3}	During operation at 2MHz (VSC="2", V_{SS}=-5.0V)			1,000	1,500	μA
Current consumption [1] (OSC1/CR oscillation)	I_{hlt}	During HALT (VSC="0"or"1", OSCC="0")			20	70	μA
	I_{EX1}	During operation at f_{OSC1} (VSC="0"or"1", OSCC="0")			25	80	μA
	I_{EX2}	During operation at 1MHz (VSC="1")			420	600	μA
	I_{EX3}	During operation at 2MHz (VSC="2", V_{SS}=-5.0V)			1,000	1,500	μA

[1] No panel load.

13.5 AC Characteristics

#RESET input

Condition: V_{DD}=0V, V_{SS}=-3.0V, f_{OSC1}=32.768kHz, Ta=25°C, V_{IH}=0.5V_{SS}, V_{IL}=0.9V_{SS}

Item	Symbol	Min.	Typ.	Max.	Unit
#RESET input time	tsr	2.0			ms
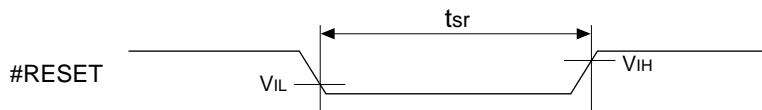
13.6 Oscillation Characteristics

The oscillation characteristics change depending on the conditions (components used, board pattern, etc.). Use the following characteristics as reference values.

OSC1 crystal oscillation characteristics
Conditions unless otherwise specified:

V_{DD}=0V, V_{SS}=-3.0V, Crystal: C-002R(C_I=35kΩ), C_{GX}=25pF, C_{DX}=built-in, Rfx=10MΩ, Ta=25°C, VSC="0"

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start time	tsta	V_{SS}=-2.2 to -5.5V			5	s
Built-in drain capacitance	C_D	Package as assembled		22		pF
		Bare chip		21		pF
Frequency/voltage deviation	$\partial f/\partial V$	V_{SS}=-2.2 to -5.5V			5	ppm
Frequency/IC deviation	$\partial f/\partial IC$		-10		+10	ppm
Frequency adjustable range	$\partial f/\partial C_G$	C_G=5 to 25pF	35	45		ppm
Harmonic oscillation start voltage	V_{hho}	C_G=5pF (V_{SS})			-5.5	V
Permitted leak resistance	R_{leak}	Between OSC1 and V_{DD}, V_{S1}	200			MΩ

OSC1 CR oscillation characteristics
Conditions unless otherwise specified:

V_{DD}=0V, V_{SS}=-3.0V, Ta=25°C, VSC="0" or "1"

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation frequency	f_{OSC1}	R_{CR1}=1.6MΩ	Typ. ×70%	32	Typ. ×130%	kHz
Oscillation start time	tsta	V_{SS}=-2.2 to -5.5V			3	ms
Frequency/voltage deviation	$\partial f/\partial V$	V_{SS}=-2.2 to -5.5V	-5		+5	%

OSC3 CR oscillation characteristics 1
Conditions unless otherwise specified:

V_{DD}=0V, V_{SS}=-3.0V, Ta=25°C, VSC="1"

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation frequency	f_{OSC3}	R_{CR2}=40kΩ	Typ. ×70%	860	Typ. ×130%	kHz
Oscillation start time	tsta	V_{SS}=-2.2 to -5.5V			3	ms
Frequency/voltage deviation	$\partial f/\partial V$	V_{SS}=-2.2 to -5.5V	-5		+5	%

OSC3 CR oscillation characteristics 2
Conditions unless otherwise specified:

V_{DD}=0V, V_{SS}=-5.0V, Ta=25°C, VSC="2"

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation frequency	f_{OSC3}	R_{CR2}=20kΩ	Typ. ×70%	1.7	Typ. ×130%	MHz
Oscillation start time	tsta	V_{SS}=-3.5 to -5.5V			3	ms
Frequency/voltage deviation	$\partial f/\partial V$	V_{SS}=-3.5 to -5.5V	-5		+5	%

OSC3 ceramic oscillation characteristics 1
Conditions unless otherwise specified:

V_{DD}=0V, V_{SS}=-3.0V, Ta=25°C, VSC="1", Ceramic oscillator: CSB 1000J [1] (1MHz), C_{GC}=C_{DC}=100pF, Rfc=1MΩ

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start time	tsta	V_{SS}=-2.2 to -5.5V			3	ms
Frequency/voltage deviation	$\partial f/\partial V$	V_{SS}=-2.2 to -5.5V	-3		+3	%

*1 Made by Murata Mfg. Co.

OSC3 ceramic oscillation characteristics 2
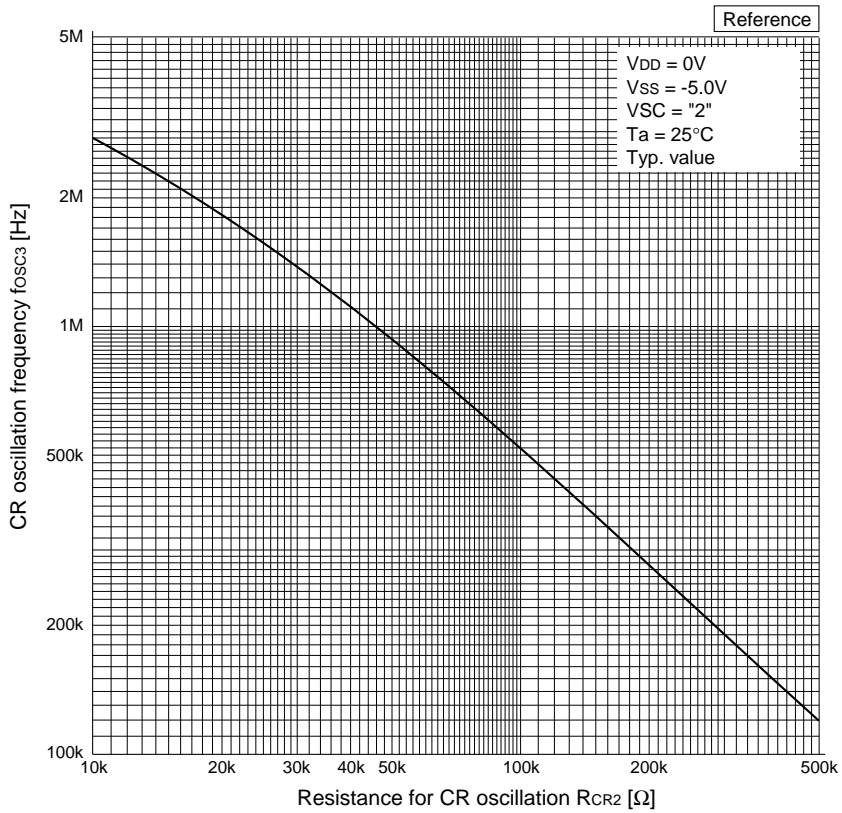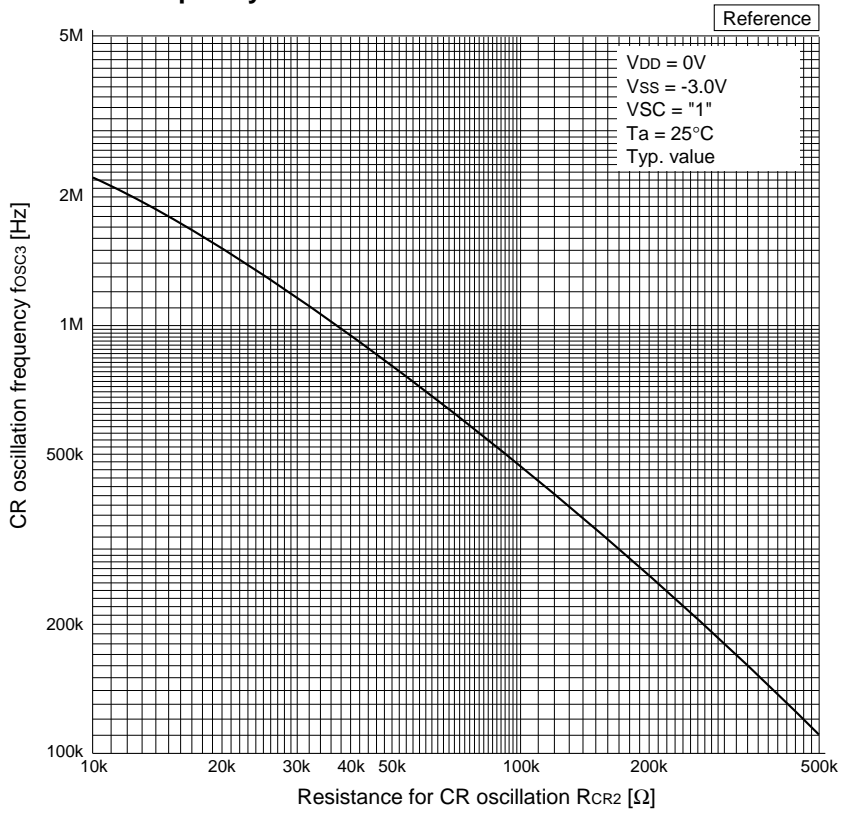Conditions unless otherwise specified:

V_{DD}=0V, V_{SS}=-5.0V, Ta=25°C, VSC="2", Ceramic oscillator: CSA 2.00MG [1] (2MHz), C_{GC}=C_{DC}=100pF, Rfc=1MΩ

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start time	tsta	V_{SS}=-3.5 to -5.5V			3	ms
Frequency/voltage deviation	$\partial f/\partial V$	V_{SS}=-3.5 to -5.5V	-3		+3	%

*1 Made by Murata Mfg. Co.

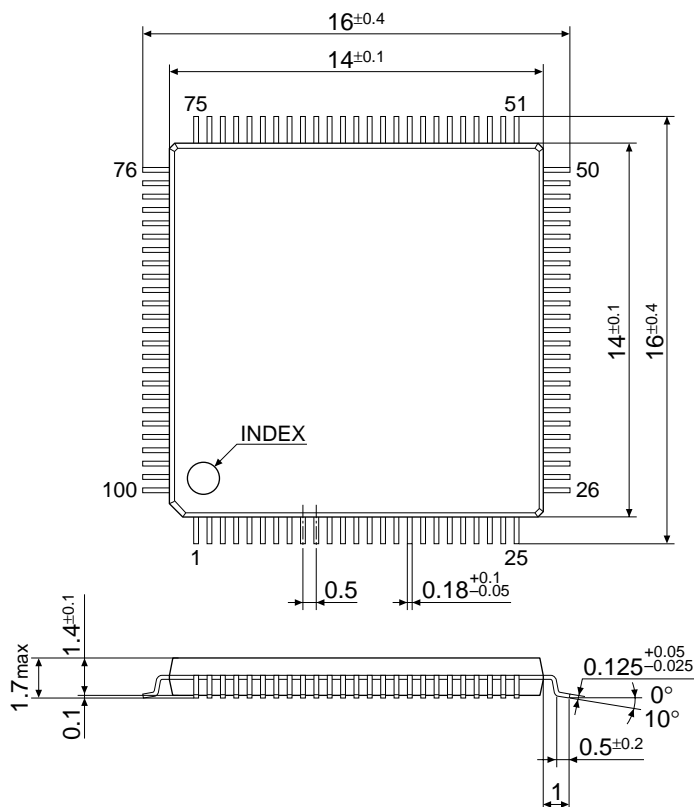## OSC3 CR oscillation frequency - resistance characteristic

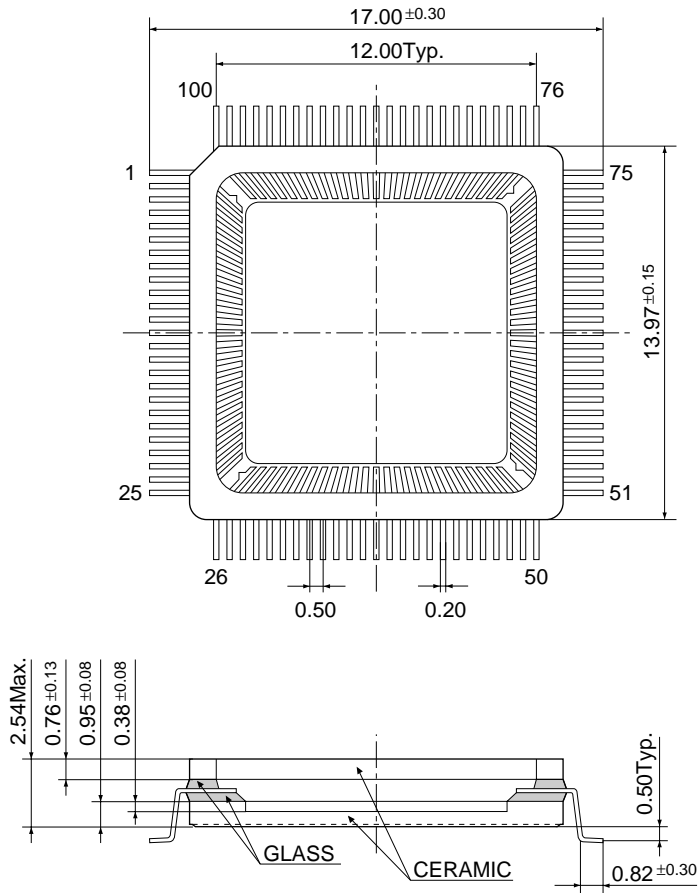# CHAPTER *14* PACKAGE

14.1 Plastic Package

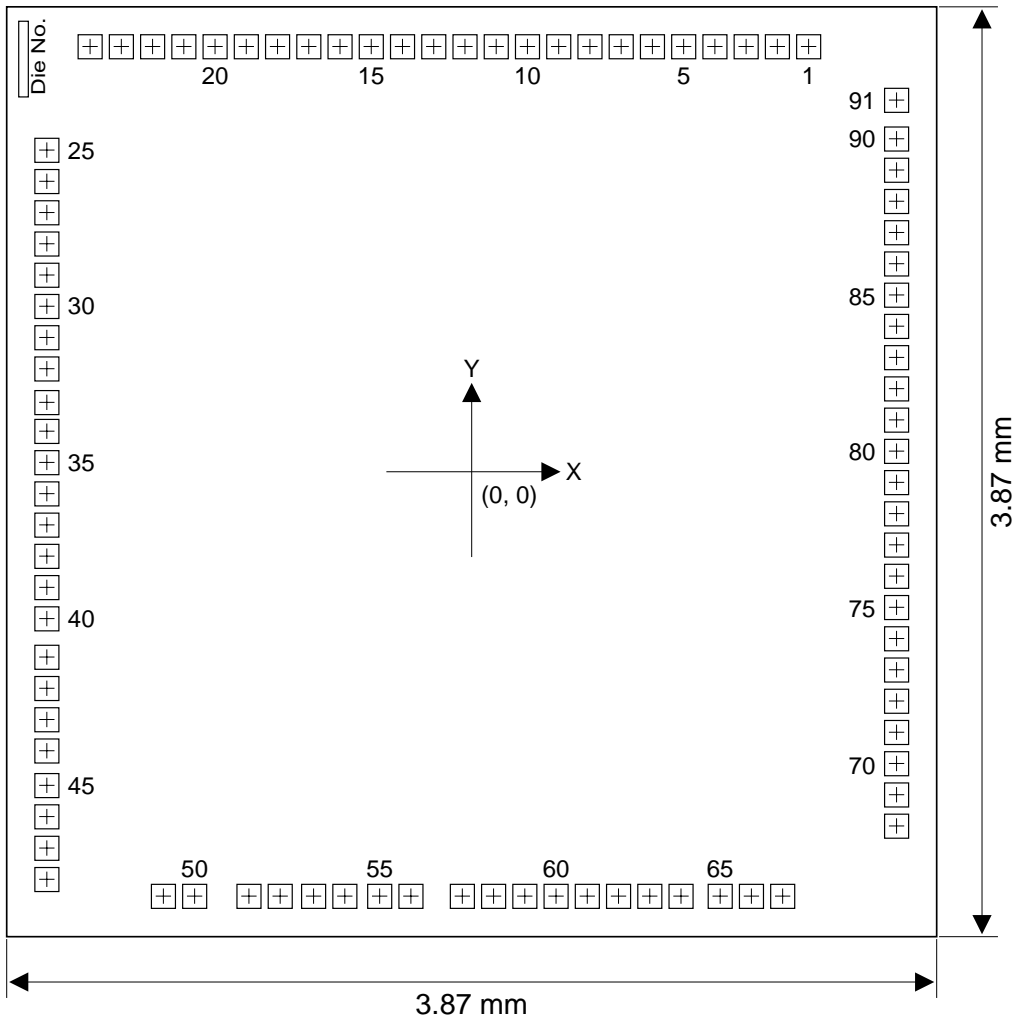**QFP15-100pin**

(Unit: mm)

14.2 Ceramic Package for Test Samples

QFP15-100pin

(Unit: mm)

CHAPTER 15 PAD LAYOUT

15.1 Diagram of Pad Layout

15.2 Pad Coordinates

(unit: µm)

No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y
	Pad	Coordinate			Pad	Coordinate			Pad	Coordinate	
1	SEG39	1,402	1,768	32	SEG8	-1,768	427	63	V$_{DD}$	741	-1,768
2	SEG38	1,272	1,768	33	SEG7	-1,768	297	64	V$_{REF}$	871	-1,768
3	SEG37	1,142	1,768	34	SEG6	-1,768	167	65	V$_{L1}$	1,034	-1,768
4	SEG36	1,012	1,768	35	SEG5	-1,768	37	66	V$_{L2}$	1,164	-1,768
5	SEG35	882	1,768	36	SEG4	-1,768	-93	67	V$_{L3}$	1,294	-1,768
6	SEG34	752	1,768	37	SEG3	-1,768	-223	68	V$_{L4}$	1,768	-1,476
7	SEG33	622	1,768	38	SEG2	-1,768	-353	69	V$_{L5}$	1,768	-1,346
8	SEG32	492	1,768	39	SEG1	-1,768	-483	70	CF	1,768	-1,216
9	SEG31	362	1,768	40	SEG0	-1,768	-613	71	CE	1,768	-1,086
10	SEG30	232	1,768	41	K03	-1,768	-773	72	CD	1,768	-956
11	SEG29	102	1,768	42	K02	-1,768	-903	73	CC	1,768	-826
12	SEG28	-28	1,768	43	K01	-1,768	-1,033	74	CB	1,768	-696
13	SEG27	-158	1,768	44	K00	-1,768	-1,163	75	CA	1,768	-566
14	SEG26	-288	1,768	45	P03	-1,768	-1,307	76	COM0	1,768	-436
15	SEG25	-418	1,768	46	P02	-1,768	-1,437	77	COM1	1,768	-306
16	SEG24	-548	1,768	47	P01	-1,768	-1,568	78	COM2	1,768	-176
17	SEG23	-678	1,768	48	P00	-1,768	-1,698	79	COM3	1,768	-46
18	SEG22	-808	1,768	49	R43	-1,283	-1,768	80	COM4	1,768	84
19	SEG21	-938	1,768	50	R42	-1,153	-1,768	81	COM5	1,768	214
20	SEG20	-1,068	1,768	51	R41	-927	-1,768	82	COM6	1,768	344
21	SEG19	-1,198	1,768	52	R40	-797	-1,768	83	COM7	1,768	474
22	SEG18	-1,328	1,768	53	R33	-658	-1,768	84	COM8	1,768	604
23	SEG17	-1,458	1,768	54	R32	-528	-1,768	85	COM9	1,768	734
24	SEG16	-1,588	1,768	55	#RESET	-383	-1,768	86	COM10	1,768	864
25	SEG15	-1,768	1,337	56	#TEST	-253	-1,768	87	COM11	1,768	994
26	SEG14	-1,768	1,207	57	V$_{SS}$	-39	-1,768	88	COM12	1,768	1,124
27	SEG13	-1,768	1,077	58	OSC4	91	-1,768	89	COM13	1,768	1,254
28	SEG12	-1,768	947	59	OSC3	221	-1,768	90	COM14	1,768	1,384
29	SEG11	-1,768	817	60	V$_{S1}$	351	-1,768	91	COM15	1,768	1,545
30	SEG10	-1,768	687	61	OSC2	481	-1,768	–	–	–	–
31	SEG9	-1,768	557	62	OSC1	611	-1,768	–	–	–	–

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