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CMOS 4-BIT SINGLE CHIP MICROCOMPUTER

E0C6008 TECHNICAL MANUAL

E0C6008 Technical Hardware

ENERGY SAVING EPSON

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CONTENTS

CHAPTER 1 OVERVIEW

The E0C6008 Series is a single-chip microcomputer made up of the 4-bit core CPU E0C6200C, ROM (4,096 words × 12 bits), RAM (832 words × 4 bits), LCD driver, serial interface, event counter with dial input function, watchdog timer, and two types of time base counter. Because of its low-voltage operation and low power consumption, this series is ideal for a wide range of applications, and is especially suitable for battery-driven systems.

1.1 Configuration

The E0C6008 Series is configured as follows, depending on supply voltage and oscillation circuits.

Table 1.1.1 Model configuration

Model	**E0C6008**	**E0C60L08**	**E0C60A08**
Supply voltage	3.0 V	1.5 V	3.0 V
Oscillation circuit	OSC1 only (Single clock)	OSC1 only (Single clock)	OSC1 and OSC3 (Twin clock)

1.2 Features

Table 1.2.1 Features

Model		**E0C6008**	**E0C60L08**	**E0C60A08**
OSC1 oscillation circuit		Crystal oscillation circuit 32.768 kHz (Typ.)/38.400 kHz (Typ.)		
OSC3 oscillation circuit		Unavailable		CR or ceramic oscillation circuit (selected by mask option) 500 kHz (Typ.)
Instruction set		108 types		
Instruction execution time (differs depending on instruction) (CLK: CPU operation frequency)		153 µsec, 214 µsec, 366 µsec (CLK = 32.768 kHz)		
		130 µsec, 182 µsec, 313 µsec (CLK = 38.400 kHz)		
		–		10 µsec, 14 µsec, 24 µsec (CLK = 500 kHz)
ROM capacity		4,096 words × 12 bits		
RAM capacity		832 words × 4 bits		
Input ports		9 bits (pull-down resistor can be added by mask option)		
Output ports		8 bits (BZ, $\overline{BZ}$, FOUT and SIOF outputs are available by mask option)		
I/O ports		8 bits (pull-down resistor is added during input data read-out)		
Serial interface		1 port (8-bit clock synchronous system)		
LCD driver		48 segments × 4, 3, or 2 commons (selected by mask option) V-3 V 1/4, 1/3 or 1/2 duty (voltage regulator and booster circuits built-in)		
Time base counter		Two types (timer and stopwatch)		
Watchdog timer		Built-in (can be disabled by mask option)		
Event counter		Two 8-bit inputs (dial input evaluation or independent)		
Sound generator		Programmable in 8 sounds (8 frequencies) Digital envelope built-in (can be disabled by mask option)		
Analog comparator		Inverted input × 1, non-inverted input × 1		
Battery low detection circuit (BLD)		Dual system (programmable in 8 values and a fixed value)		
		2.4 V, 2.2–2.55 V	1.2 V, 1.05–1.4 V	2.4 V, 2.2–2.55 V
External interrupt		Input interrupt: 3 systems		
Internal interrupt		Time base counter interrupt: 2 systems Serial interface interrupt: 1 system		
Supply voltage		3.0 V (1.8–3.5 V)	1.5 V (0.9–1.7 V)	3.0 V (2.2–3.5 V)
Current consumption (Typ. value)	CLK= 32.768 kHz (when halted)	1.0 µA	1.0 µA	1.1 µA
	CLK= 32.768 kHz (when executed)	2.2 µA	2.2 µA	3.0 µA
	CLK= 500 kHz (when executed)	–	–	50 µA
Form when shipped		QFP5-100pin, QFP15-100pin or chip		

1.3 Block Diagram

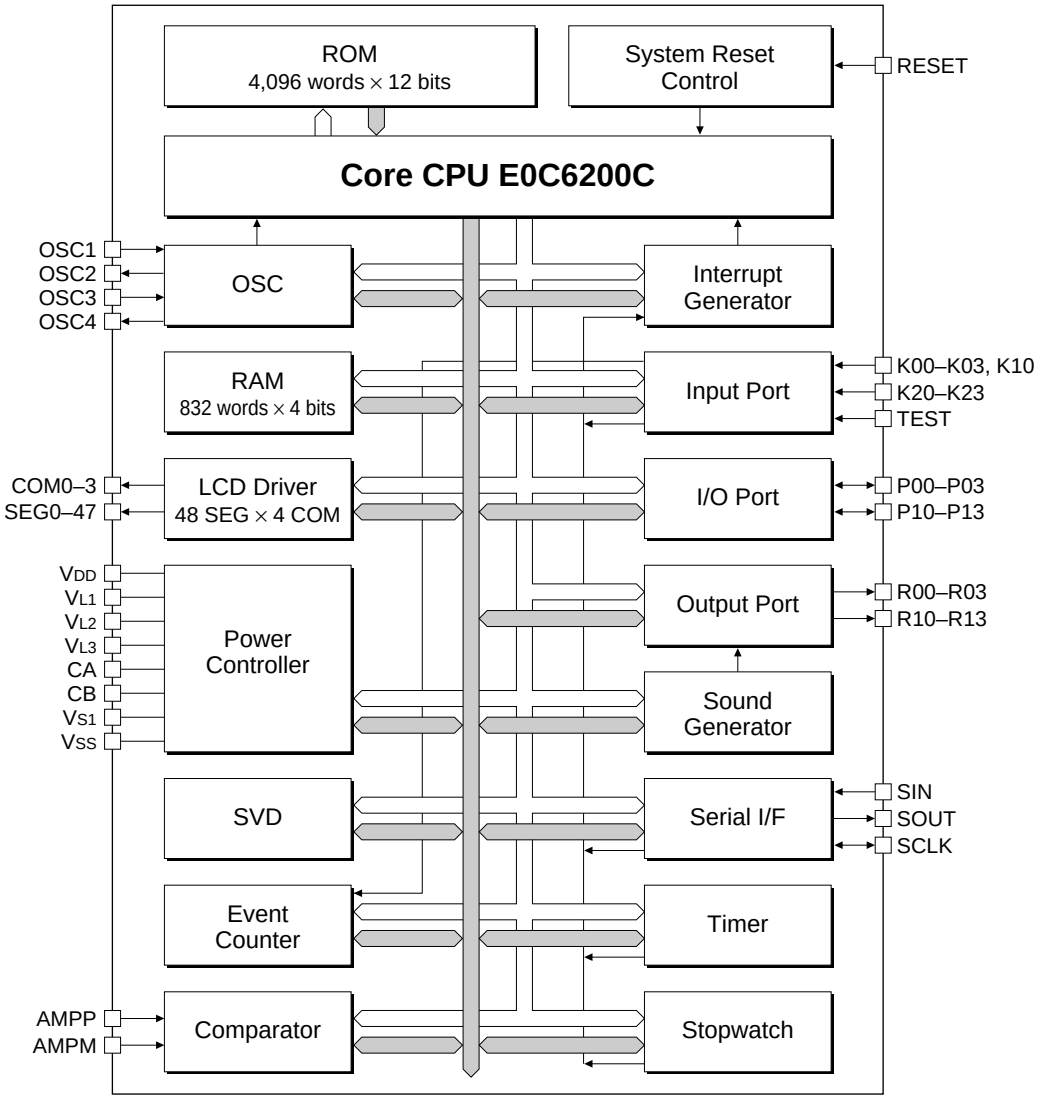
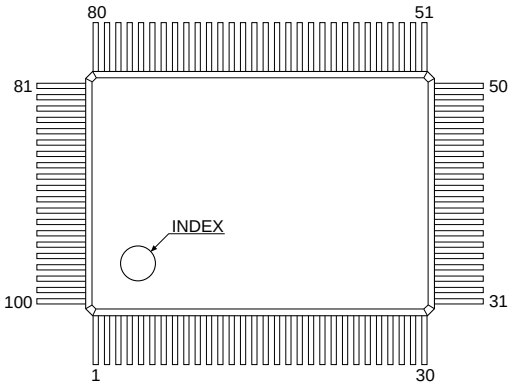


Fig. 1.3.1 Block diagram

1.4 Pin Layout Diagram

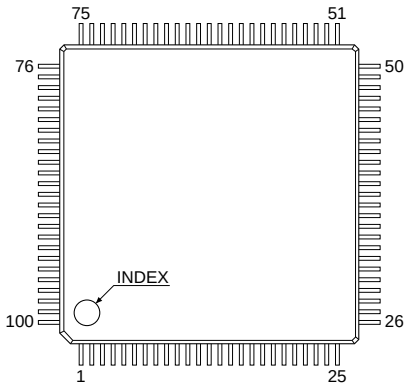
QFP5-100pin



No.	Pin name	No.	Pin name	No.	Pin name	No.	Pin name
1	COM1	26	SEG24	51	SEG0	76	P10
2	COM0	27	TEST	52	AMPP	77	R03
3	SEG47	28	SEG23	53	AMPM	78	R02
4	SEG46	29	SEG22	54	K23	79	R01
5	SEG45	30	SEG21	55	K22	80	R00
6	SEG44	31	SEG20	56	K21	81	R12
7	SEG43	32	SEG19	57	K20	82	R11
8	SEG42	33	SEG18	58	K10	83	R10
9	SEG41	34	SEG17	59	K03	84	R13
10	SEG40	35	SEG16	60	K02	85	V_{SS}
11	SEG39	36	SEG15	61	K01	86	RESET
12	SEG38	37	SEG14	62	K00	87	OSC4
13	SEG37	38	SEG13	63	SIN	88	OSC3
14	SEG36	39	SEG12	64	SOUT	89	V_{S1}
15	SEG35	40	SEG11	65	N.C.	90	OSC2
16	SEG34	41	SEG10	66	SCLK	91	OSC1
17	SEG33	42	SEG9	67	P03	92	V_{DD}
18	SEG32	43	SEG8	68	P02	93	V_{L3}
19	SEG31	44	SEG7	69	P01	94	V_{L2}
20	SEG30	45	SEG6	70	P00	95	V_{L1}
21	SEG29	46	SEG5	71	N.C.	96	CA
22	SEG28	47	SEG4	72	N.C.	97	CB
23	SEG27	48	SEG3	73	P13	98	N.C.
24	SEG26	49	SEG2	74	P12	99	COM3
25	SEG25	50	SEG1	75	P11	100	COM2

N.C. = No connection

QFP15-100pin



No.	Pin name	No.	Pin name	No.	Pin name	No.	Pin name
1	SEG47	26	SEG23	51	AMPP	76	R02
2	SEG46	27	SEG22	52	AMPM	77	R01
3	SEG45	28	SEG21	53	K23	78	R00
4	SEG44	29	SEG20	54	K22	79	R12
5	SEG43	30	SEG19	55	K21	80	R11
6	SEG42	31	SEG18	56	K20	81	R10
7	SEG41	32	SEG17	57	K10	82	R13
8	SEG40	33	SEG16	58	K03	83	V_{SS}
9	SEG39	34	SEG15	59	K02	84	RESET
10	SEG38	35	SEG14	60	K01	85	OSC4
11	SEG37	36	SEG13	61	K00	86	OSC3
12	SEG36	37	SEG12	62	SIN	87	V_{S1}
13	SEG35	38	N.C.	63	SOUT	88	OSC2
14	SEG34	39	SEG11	64	N.C.	89	OSC1
15	SEG33	40	SEG10	65	SCLK	90	V_{DD}
16	SEG32	41	SEG9	66	N.C.	91	V_{L3}
17	SEG31	42	SEG8	67	P03	92	V_{L2}
18	SEG30	43	SEG7	68	P02	93	V_{L1}
19	SEG29	44	SEG6	69	P01	94	CA
20	SEG28	45	SEG5	70	P00	95	CB
21	SEG27	46	SEG4	71	P13	96	N.C.
22	SEG26	47	SEG3	72	P12	97	COM3
23	SEG25	48	SEG2	73	P11	98	COM2
24	SEG24	49	SEG1	74	P10	99	COM1
25	TEST	50	SEG0	75	R03	100	COM0

N.C. = No connection

Fig. 1.4.1 Pin layout

1.5 Pin Description

Table 1.5.1 Pin description

Pin name	Pin No.		I/O	Function
	QFP5-100	QFP15-100		
V_{DD}	92	90	(I)	Power supply pin (+)
V_{SS}	85	83	(I)	Power supply pin (-)
V_{S1}	89	87	–	Oscillation and internal logic system voltage output pin
V_{L1}	95	93	–	LCD drive voltage output pin (approx. -1.05 V or $1/2 \cdot V_{L2}$)
V_{L2}	94	92	–	LCD drive voltage output pin ($2 \cdot V_{L1}$ or approx. -2.10 V)
V_{L3}	93	91	–	LCD drive voltage output pin ($3 \cdot V_{L1}$ or $3/2 \cdot V_{L2}$)
CA, CB	96, 97	94, 95	–	Boost capacitor connecting pin
OSC1	91	89	I	Cryctal oscillation input pin
OSC2	90	88	O	Crystal oscillation output pin
OSC3	88	86	I	CR or ceramic oscillation input pin * (N.C. for E0C6008 and E0C60L08)
OSC4	87	85	O	CR or ceramic oscillation output pin * (N.C. for E0C6008 and E0C60L08)
K00–K03	62–59	61–58	I	Input port pin
K10	58	57	I	Input port pin
K20–K23	57–54	56–53	I	Input port pin
P00–P03	70–67	70–67	I/O	I/O port pin
P10–P13	76–73	74–71	I/O	I/O port pin
R00–R03	80–77	78–75	O	Output port pin
R10	83	81	O	Output port pin or BZ output pin *
R13	84	82	O	Output port pin or $\overline{BZ}$ output pin *
R11	82	80	O	Output port pin or SIOF output pin *
R12	81	79	O	Output port pin or FOUT output pin *
SIN	63	62	I	Serial interface data input pin
SOUT	64	63	O	Serial interface data output pin
SCLK	66	65	I/O	Serial interface clock input/output pin
AMPP	52	51	I	Analog comparator non-inverted input pin
AMPM	53	52	I	Analog comparator inverted input pin
SEG0–47	51–28, 26–3	50–39, 37–26, 24–1	O	LCD segment output pin or DC output pin *
COM0–3	2, 1, 100, 99	100–97	O	LCD common output pin (1/2, 1/3 or 1/4 duty are selectable *)
RESET	86	84	I	Initial reset input pin
TEST	27	25	I	Input pin for test

* Can be selected by mask option

CHAPTER 2 POWER SUPPLY AND INITIAL RESET

2.1 Power Supply

With a single external power supply (∗1) supplied to VDD through VSS, the E0C6008 Series generates the necessary internal voltage with the regulated voltage circuit (<VS1> for oscillators, <VL1 or VL2> for LCD) and the voltage booster/reducer circuit (<VL2 and VL3, or VL1 and VL3> for LCD).

∗1 Supply voltage: E0C6008/60A08 .. 3 V, E0C60L08 .. 1.5 V

Figure 2.1.1 shows the power supply configuration of the E0C6008.
Figure 2.1.2 shows the power supply configuration of the E0C60A08 and E0C60L08.
The voltage <VS1> for the internal circuit that is generated by the internal system voltage regulator is -1.2 V (VDD ground).

The E0C6008 generates <VL2> with the LCD system voltage regulator and <VL1, VL3> with the voltage booster/reducer. The E0C60A08 and the E0C60L08 generate <VL1> with the voltage regulator and <VL2, VL3> with the voltage booster/reducer.

Notes: • *External loads cannot be driven by the output voltage of the voltage regulator and voltage booster/reducer.*
• *See Chapter 7, "Electrical Characteristics", for voltage values.*

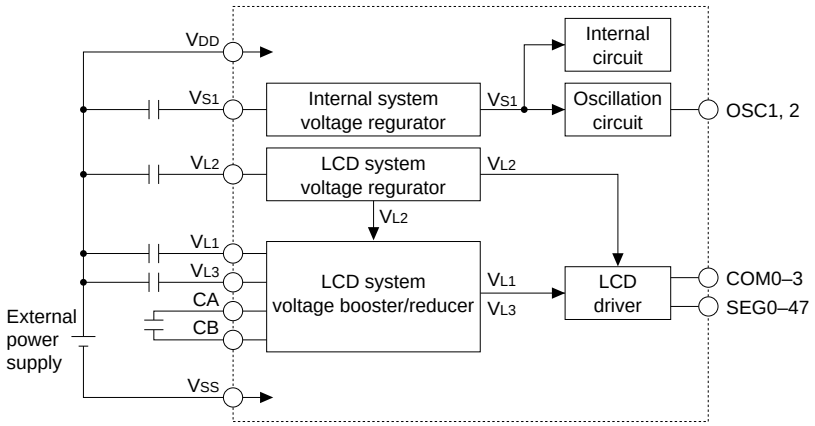


Fig. 2.1.1 Power supply configuration of E0C6008

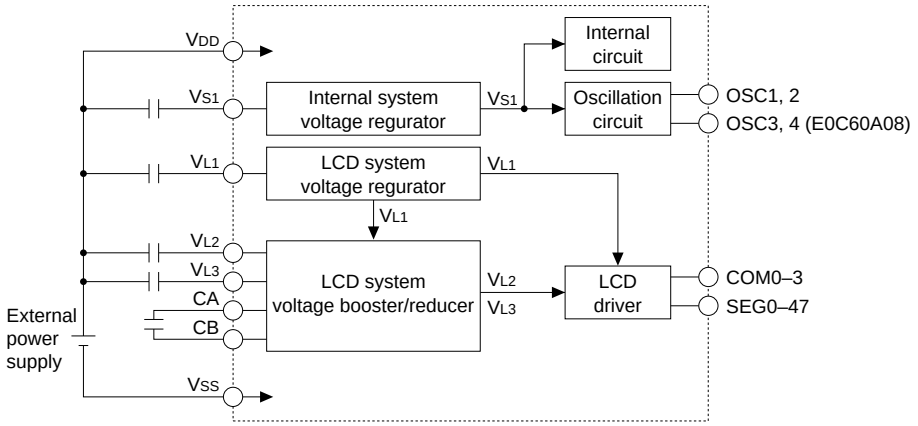


Fig. 2.1.2 Power supply configuration of E0C60A08 and E0C60L08

The LCD system voltage regulator can be disabled by mask option. In this case, external elements can be minimized because the external capacitors for the LCD system voltage regulator are not necessary. However when the LCD system voltage regulator is not used, the display quality of the LCD panel, when the supply voltage fluctuates (drops), is inferior to when the LCD system voltage regulator is used. Figure 2.1.3 shows the external element configuration when the LCD system voltage regulator is not used.

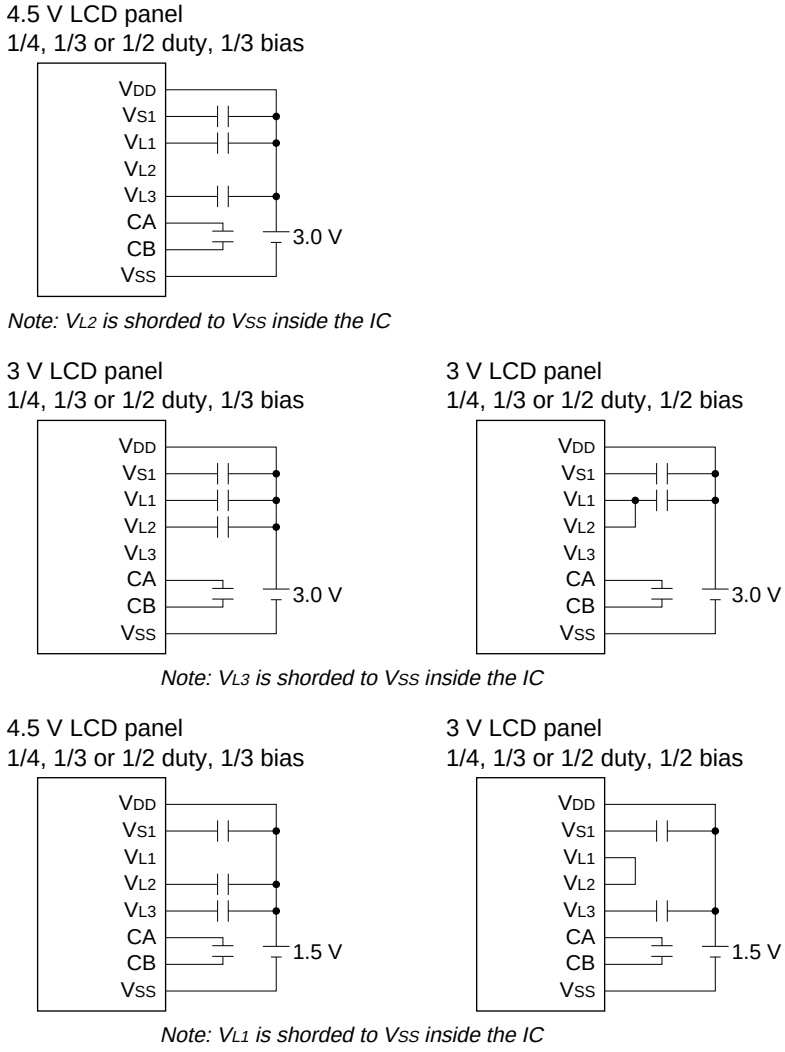


Fig. 2.1.3 External elements when LCD system voltage regulator is not used

Note: If there is any segment pad that is set to be DC type, the internal LCD voltage regulator cannot be chosen in all models. Or, if the internal LCD voltage regulator is chosen in any model, the segment pad cannot be set to be DC type.

Table 2.1.1 LCD voltage regulator and DC output from SEG terminals

LCD system voltage regulator	DC output from SEG terminals
Use	Not available
Not use	Available

2.2 Initial Reset

To initialize the E0C6008 Series circuits, initial reset must be executed. There are four ways of doing this.
(1) Initial reset by the power on reset circuit
(2) External initial reset by the RESET terminal
(3) External initial reset by simultaneous high input to terminals K00–K03
(4) Initial reset by the watchdog timer

Figure 2.2.1 shows the configuration of the initial reset circuit.

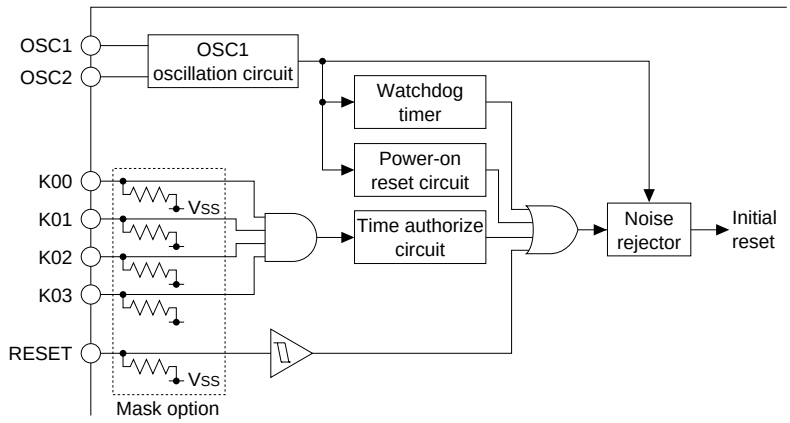


Fig. 2.2.1 Configuration of initial reset circuit

2.2.1 Power-on reset circuit

The power-on reset circuit outputs the initial reset signal at power-on until the oscillation circuit starts oscillating.

Note: The power-on reset circuit may not work properly due to unstable or lower voltage input. The following two initial reset method are recommended to generate the initial reset signal.

2.2.2 RESET terminal

Initial reset can be executed externally by setting the reset terminal to the high level. This high level must be maintained for at least 5 msec (when oscillating frequency is f_{OSC1} = 32 kHz), because the initial reset circuit contains a noise rejector. When the reset terminal goes low the CPU begins to operate.

2.2.3 Simultaneous high input to input ports (K00–K03)

Another way of executing initial reset externally is to input a high signal simultaneously to the input ports (K00–K03) selected with the mask option. The specified input port terminals must be kept high for at least 5 msec (when oscillating frequency is f_{OSC1} = 32 kHz), because the initial reset circuit contains a noise rejector. Table 2.2.3.1 shows the combinations of input ports (K00–K03) that can be selected with the mask option.

Table 2.2.3.1 Input port combination

Selection	Combination
A	Not used
B	K00∗K01
C	K00∗K01∗K02
D	K00∗K01∗K02∗K03

When, for instance, mask option D (K00*K01*K02*K03) is selected, initial reset is executed when the signals input to the four ports K00–K03 are all high at the same time.

Further, the time authorize circuit can be selected with the mask option. The time authorize circuit performs initial reset, when the input time of the simultaneous high input is authorized and found to be the same or more than the defined time (1 to 2 sec).

If you use this function, make sure that the specified ports do not go high at the same time during ordinary operation.

2.2.4 Watchdog timer

If the CPU runs away for some reason, the watchdog timer will detect this situation and output an initial reset signal. See Section 4.2, "Resetting Watchdog Timer", for details.

2.2.5 Internal register at initial reset

Initial reset initializes the CPU as shown in the table below.

Table 2.2.5.1 Initial values

CPU Core			
Name	Symbol	Bit size	Initial value
Program counter step	PCS	8	00H
Program counter page	PCP	4	1H
New page pointer	NPP	4	1H
Stack pointer	SP	8	Undefined
Index register X	X	10	Undefined
Index register Y	Y	10	Undefined
Register pointer	RP	4	Undefined
General-purpose register A	A	4	Undefined
General-purpose register B	B	4	Undefined
Interrupt flag	I	1	0
Decimal flag	D	1	0
Zero flag	Z	1	Undefined
Carry flag	C	1	Undefined

Peripheral Circuits		
Name	Bit size	Initial value
RAM	4	Undefined
Display memory	4	Undefined
Other peripheral circuits	4	*

* See Section 4.1, "Memory Map".

2.3 Test Terminal (TEST)

This terminal is used when the IC load is being detected. During ordinary operation be certain to connect this terminal to VSS.

CHAPTER 3 CPU, ROM, RAM

3.1 CPU

The E0C6008 Series employs the core CPU E0C6200C for the CPU, so that register configuration, instructions and so forth are virtually identical to those in other family processors using the E0C6200/6200A/6200B/6200C.
Refer to the "E0C6200/6200A Core CPU Manual" for details about the core CPU.
Note the following points with regard to the E0C6008 Series:

(1) The SLEEP operation is not assumed, so the SLP instruction cannot be used.

(2) Because the ROM capacity is 4,096 words, bank bits are unnecessary and PCB and NBP are not used.

(3) RAM is set up to four pages, so only the two low-order bits are valid for the page portion (XP, YP) of the index register that specifies addresses. (The two high-order bits are ignored.)

3.2 ROM

The built-in ROM, a mask ROM for loading the program, has a capacity of 4,096 steps, 12 bits each. The program area is 16 pages (0–15), each of 256 steps (00H–FFH). After initial reset, the program start address is page 1, step 00H. The interrupt vector is allocated to page 1, steps 01H–0FH.

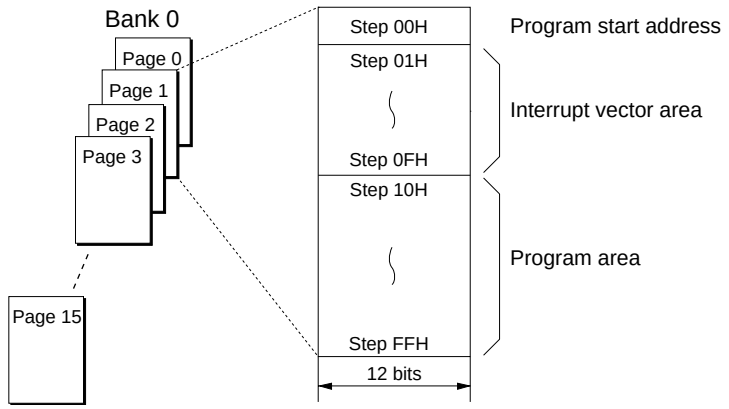


Fig. 3.2.1 ROM configuration

3.3 RAM

The RAM, a data memory for storing a variety of data, has a capacity of 832 words, 4-bit words. When programming, keep the following points in mind:

(1) Part of the data memory is used as stack area when saving subroutine return addresses and registers, so be careful not to overlap the data area and stack area.

(2) Subroutine calls and interrupts take up three words on the stack.

(3) Data memory 000H–00FH is the memory area pointed by the register pointer (RP).

CHAPTER 4 PERIPHERAL CIRCUITS AND OPERATION

Peripheral circuits (timer, I/O, and so on) of the E0C6008 Series are memory mapped. Thus, all the peripheral circuits can be controlled by using memory operations to access the I/O memory. The following sections describe how the peripheral circuits operate.

4.1 Memory Map

The data memory of the E0C6008 Series has an address space of 865 words (913 words when display memory is laid out in Page 2), of which 48 words are allocated to display memory and 33 words, to I/O memory. Figure 4.1.1 shows the overall memory map for the E0C6008 Series, and Tables 4.1.1(a)–(c), the memory maps for the peripheral circuits (I/O space).

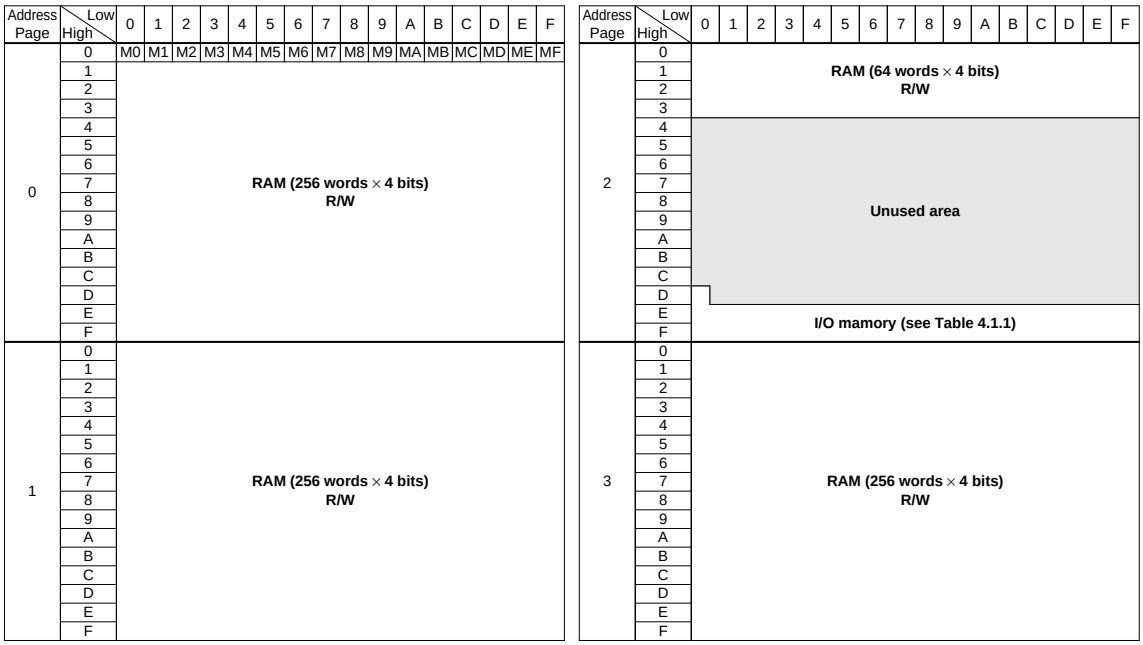


Fig. 4.1.1 Memory map

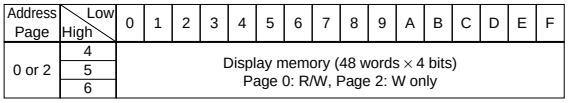


Fig. 4.1.2 Display memory map

Notes:
- *The display memory area can be selected from between Page 0 (040H–06FH) and Page 2 (240H–26FH) by mask option.*
  When Page 0 (040H–06FH) is selected, the display memory is assigned in the RAM area. So read/write operation is allowed.
  When Page 2 (240H–26FH) is selected, the display memory is assigned as a write-only memory.
- *Memory is not mounted in unused area within the memory map and in memory area not indicated in this manual. For this reason, normal operation cannot be assured for programs that have been prepared with access to these areas.*

Table 4.1.1(a) I/O memory map (2D0H, 2E0H–2ECH)

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
2D0H	0	0	0	LOF	0 *3	– *2	–	–	Unused
					0 *3	– *2	–	–	Unused
	R			R/W	0 *3	– *2	–	–	Unused
					LOF	1	Normal	All off	LCD all off control
2E0H	TM3	TM2	TM1	TM0	TM3	0			Clock timer data (2 Hz)
					TM2	0			Clock timer data (4 Hz)
	R				TM1	0			Clock timer data (8 Hz)
					TM0	0			Clock timer data (16 Hz)
2E1H	SWL3	SWL2	SWL1	SWL0	SWL3	0			MSB
					SWL2	0			Stopwatch timer 1/100 sec data (BCD)
	R				SWL1	0			Stopwatch timer 1/100 sec data (BCD)
					SWL0	0			LSB
2E2H	SWH3	SWH2	SWH1	SWH0	SWH3	0			MSB
					SWH2	0			Stopwatch timer 1/10 sec data (BCD)
	R				SWH1	0			Stopwatch timer 1/10 sec data (BCD)
					SWH0	0			LSB
2E3H	K03	K02	K01	K00	K03	– *2	High	Low	Input port data (K00–K03)
					K02	– *2	High	Low	Input port data (K00–K03)
	R				K01	– *2	High	Low	Input port data (K00–K03)
					K00	– *2	High	Low	Input port data (K00–K03)
2E4H	KCP03	KCP02	KCP01	KCP00	KCP03	0	↓	↑	Input comparison register (K00–K03)
					KCP02	0	↓	↑	Input comparison register (K00–K03)
	R/W				KCP01	0	↓	↑	Input comparison register (K00–K03)
					KCP00	0	↓	↑	Input comparison register (K00–K03)
2E5H	EIK03	EIK02	EIK01	EIK00	EIK03	0	Enable	Mask	Interrupt mask register (K00–K03)
					EIK02	0	Enable	Mask	Interrupt mask register (K00–K03)
	R/W				EIK01	0	Enable	Mask	Interrupt mask register (K00–K03)
					EIK00	0	Enable	Mask	Interrupt mask register (K00–K03)
2E6H	HLMOD	BLD0	EISWIT1	EISWIT0	HLMOD	0	Heavy load	Normal	Heavy load protection mode register
					BLD0	0	Low	Normal	Sub-BLD evaluation data
	R/W	R	R/W		EISWIT1	0	Enable	Mask	Interrupt mask register (stopwatch 1 Hz)
					EISWIT0	0	Enable	Mask	Interrupt mask register (stopwatch 10 Hz)
2E7H	SCTRG	EIK10	KCP10	K10	SCTRG*3	–	Trigger	–	Serial I/F clock trigger
					EIK10	0	Enable	Mask	Interrupt mask register (K10)
	W	R/W		R	KCP10	0	↓	↑	Input comparison register (K10)
					K10	– *2	High	Low	Input port data (K10)
2E8H	CSDC	ETI2	ETI8	ETI32	CSDC	0	Static	Dynamic	LCD drive switch
					ETI2	0	Enable	Mask	Interrupt mask register (clock timer 2 Hz)
	R/W				ETI8	0	Enable	Mask	Interrupt mask register (clock timer 8 Hz)
					ETI32	0	Enable	Mask	Interrupt mask register (clock timer 32 Hz)
2E9H	0	TI2	TI8	TI32	0 *3	– *2	–	–	Unused
					TI2 *4	0	Yes	No	Interrupt factor flag (clock timer 2 Hz)
	R				TI8 *4	0	Yes	No	Interrupt factor flag (clock timer 8 Hz)
					TI32 *4	0	Yes	No	Interrupt factor flag (clock timer 32 Hz)
2EAH	IK1	IK0	SWIT1	SWIT0	IK1 *4	0	Yes	No	Interrupt factor flag (K10)
					IK0 *4	0	Yes	No	Interrupt factor flag (K00–K03)
	R				SWIT1 *4	0	Yes	No	Interrupt factor flag (stopwatch 1 Hz)
					SWIT0 *4	0	Yes	No	Interrupt factor flag (stopwatch 10 Hz)
2EBH	R03	R02	R01	R00	R03	0	High	Low	Output port (R03)
					R02	0	High	Low	Output port (R02)
	R/W				R01	0	High	Low	Output port (R01)
					R00	0	High	Low	Output port (R00)
2ECH	R13	R12	R11 / SIOF	R10	R13	0	High/On	Low/Off	Output port (R13)/$\overline{BZ}$ output control
					R12	0	High/On	Low/Off	Output port (R12)/FOUT output control
					R11	0	High	Low	Output port (R11, LAMP)
	R/W		R/W / R	R/W	SIOF	0	Run	Stop	Output port (SIOF)
					R10	0	High/On	Low/Off	Output port (R10)/BZ output control

*1 Initial value at initial reset
*2 Not set in the circuit
*3 Always "0" being read
*4 Reset (0) immediately after being read
*5 Undefined

Table 4.1.1(b) I/O memory map (2EDH–2FAH)

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
2EDH	P03	P02	P01	P00	P03	– *2	High	Low	I/O port data (P00–P03)
					P02	– *2	High	Low	
					P01	– *2	High	Low	
	R/W				P00	– *2	High	Low	Output latch is reset at initial reset
2EEH	TMRST	SWRUN	SWRST	IOC0	TMRST*3	Reset	Reset	–	Clock timer reset
					SWRUN	0	Run	Stop	Stopwatch timer Run/Stop
	W	R/W	W	R/W	SWRST*3	Reset	Reset	–	Stopwatch timer reset
					IOC0	0	Output	Input	I/O control register 0 (P00–P03)
2EFH	WDRST	WD2	WD1	WD0	WDRST*3	Reset	Reset	–	Watchdog timer reset
					WD2	0			Timer data (watchdog timer) 1/4 Hz
	W	R			WD1	0			Timer data (watchdog timer) 1/2 Hz
					WD0	0			Timer data (watchdog timer) 1 Hz
2F0H	SD3	SD2	SD1	SD0	SD3	× *5			Serial I/F data register (low-order 4 bits)
					SD2	× *5			
	R/W				SD1	× *5			
					SD0	× *5			
2F1H	SD7	SD6	SD5	SD4	SD7	× *5			Serial I/F data register (high-order 4 bits)
					SD6	× *5			
	R/W				SD5	× *5			
					SD4	× *5			
2F2H	SCS1	SCS0	SE2	EISIO	SCS1	1			Serial I/F clock mode selection [SCS1, 0]: 0 Clock, 1 CLK, 2 CLK/2, 3 CLK/4, Slave
					SCS0	1			
	R/W				SE2	0	↑	↓	Serial I/F clock edge selection
					EISIO	0	Enable	Mask	Interrupt mask register (serial I/F)
2F3H	0	0	IK2	ISIO	0 *3	– *2	–	–	Unused
					0 *3	– *2	–	–	Unused
	R				IK2 *4	0	Yes	No	Interrupt factor flag (K20–K23)
					ISIO *4	0	Yes	No	Interrupt factor flag (serial I/F)
2F4H	K23	K22	K21	K20	K23	– *2	High	Low	Input port data (K20–K23)
					K22	– *2	High	Low	
	R				K21	– *2	High	Low	
					K20	– *2	High	Low	
2F5H	EIK23	EIK22	EIK21	EIK20	EIK23	0	Enable	Mask	Interrupt mask register (K20–K23)
					EIK22	0	Enable	Mask	
	R/W				EIK21	0	Enable	Mask	
					EIK20	0	Enable	Mask	
2F6H	BZFQ2	BZFQ1	BZFQ0	ENVRST	BZFQ2	0			Buzzer frequency selection [BZFQ2–0]: 0 fOSC1/8, 1 fOSC1/10, 2 fOSC1/12, 3 fOSC1/14, 4 fOSC1/16, 5 fOSC1/20, 6 fOSC1/24, 7 fOSC1/28
					BZFQ1	0			
	R/W			W	BZFQ0	0			
					ENVRST*3	Reset	Reset	–	Envelope reset
2F7H	ENVON	ENVRT	AMPDT	AMPON	ENVON	0	On	Off	Envelope On/Off
					ENVRT	0	1.0 sec	0.5 sec	Envelope cycle selection register
	R/W		R	R/W	AMPDT	1	+ > -	+ < -	Analog comparator data
					AMPON	0	On	Off	Analog comparator On/Off
2F8H	EV03	EV02	EV01	EV00	EV03	0			Event counter 0 (low-order 4 bits)
					EV02	0			
	R				EV01	0			
					EV00	0			
2F9H	EV07	EV06	EV05	EV04	EV07	0			Event counter 0 (high-order 4 bits)
					EV06	0			
	R				EV05	0			
					EV04	0			
2FAH	EV13	EV12	EV11	EV10	EV13	0			Event counter 1 (low-order 4 bits)
					EV12	0			
	R				EV11	0			
					EV10	0			

*1 Initial value at initial reset
*2 Not set in the circuit
*3 Always "0" being read
*4 Reset (0) immediately after being read
*5 Undefined

Table 4.1.1(c) I/O memory map (2FBH–2FFH)

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
2FBH	EV17	EV16	EV15	EV14	EV17	0			Event counter 1 (high-order 4 bits)
					EV16	0			
	R				EV15	0			
					EV14	0			
2FCH	EVSEL	ENRUN	EV1RST	EV0RST	EVSEL	0	Separate	Phase	Event counter mode selection
					EVRUN	0	Run	Stop	Event counter Run/Stop
	R/W		W		EV1RST*3	Reset	Reset	–	Event counter 1 reset
					EV0RST*3	Reset	Reset	–	Event counter 0 reset
2FDH	P13	P12	P11	P10	P13	– *2	High	Low	I/O port data (P10–P13)
					P12	– *2	High	Low	
	R/W				P11	– *2	High	Low	Output latch is reset at initial reset
					P10	– *2	High	Low	
2FEH	PRSM	CLKCHG	OSCC	IOC1	PRSM	0	38 kHz	32 kHz	OSC1 prescaler selection
					CLKCHG	0	OSC3	OSC1	CPU clock switch
	R/W				OSCC	0	On	Off	OSC3 oscillation On/Off
					IOC1	0	Output	Input	I/O control register (P10–P13)
2FFH	BLS	BLC2	BLC1	BLC0	BLS	0	On	Off	BLD On/Off
	BLD1				BLD1	0	Low	Normal	BLD evaluation data
	W	R/W			BLC2	× *5			Evaluation voltage setting register
	R				BLC1	× *5			
					BLC0	× *5			

Evaluation voltage setting register

[BLC2–0]	0	1	2	3	4	5	6	7	
E0C6008/A08	2.20	2.25	2.30	2.35	2.40	2.45	2.50	2.55	(V)
E0C60L08	1.05	1.10	1.15	1.20	1.25	1.30	1.35	1.40	(V)

*1 Initial value at initial reset
*2 Not set in the circuit
*3 Always "0" being read
*4 Reset (0) immediately after being read
*5 Undefined

4.2 Resetting Watchdog Timer

4.2.1 Configuration of watchdog timer

The E0C6008 Series incorporates a watchdog timer as the source oscillator for OSC1 (clock timer 2 Hz signal). The watchdog timer must be reset cyclically by the software. If reset is not executed in at least 3 or 4 seconds, the initial reset signal is output automatically for the CPU.
Figure 4.2.1.1 is the block diagram of the watchdog timer.

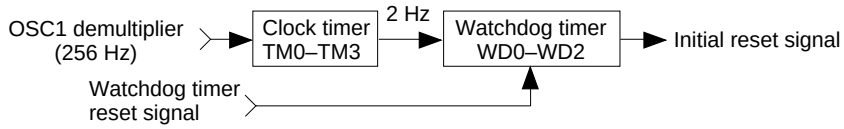


Fig. 4.2.1.1 Watchdog timer block diagram

The watchdog timer, configured of a three-bit binary counter (WD0–WD2), generates the initial reset signal internally by overflow of the MSB.
Watchdog timer reset processing in the program's main routine enables detection of program overrun, such as when the main routine's watchdog timer processing is bypassed. Ordinarily this routine is incorporated where periodic processing takes place, just as for the timer interrupt routine.
The watchdog timer operates in the halt mode. If the halt status continues for 3 or 4 seconds, the initial reset signal restarts operation.

4.2.2 Mask option

You can select whether or not to use the watchdog timer with the mask option. When "Not use" is chosen, there is no need to reset the watchdog timer.

4.2.3 Control of watchdog timer

Table 4.2.3.1 lists the watchdog timer's control bits and their addresses.

Table 4.2.3.1 Control bits of watchdog timer

Address	Register								Comment
	D3	D2	D1	D0	Name	Init *1	1	0	
2EFH	WDRST	WD2	WD1	WD0	WDRST*3	Reset	Reset	–	Watchdog timer reset
					WD2	0			Timer data (watchdog timer) 1/4 Hz
	W	R			WD1	0			Timer data (watchdog timer) 1/2 Hz
					WD0	0			Timer data (watchdog timer) 1 Hz

*1 Initial value at initial reset
*2 Not set in the circuit
*3 Always "0" being read
*4 Reset (0) immediately after being read
*5 Undefined

WDRST: Watchdog timer reset (2EFH•D3)
This is the bit for resetting the watchdog timer.

When "1" is written : Watchdog timer is reset
When "0" is written : No operation
Read-out : Always "0"

When "1" is written to WDRST, the watchdog timer is reset, and the operation restarts immediately after this. When "0" is written to WDRST, no operation results.
This bit is dedicated for writing, and is always "0" for read-out.

4.2.4 Programming note

When the watchdog timer is being used, the software must reset it within 3-second cycles, and timer data (WD0–WD2) cannot be used for timer applications.

4.3 Oscillation Circuit and Prescaler

4.3.1 Configuration of oscillation circuit and prescaler

The E0C6008 and E0C60L08 have one oscillation circuit (OSC1), and the E0C60A08 has two oscillation circuits (OSC1 and OSC3). OSC1 is a crystal oscillation circuit that supplies the operating clock the CPU and peripheral circuits. OSC3 is either a CR or ceramic oscillation circuit. When processing with the E0C60A08 requires high-speed operation, the CPU operating clock can be switched from OSC1 to OSC3. Figure 4.3.1.1 is the block diagram of this oscillation system.

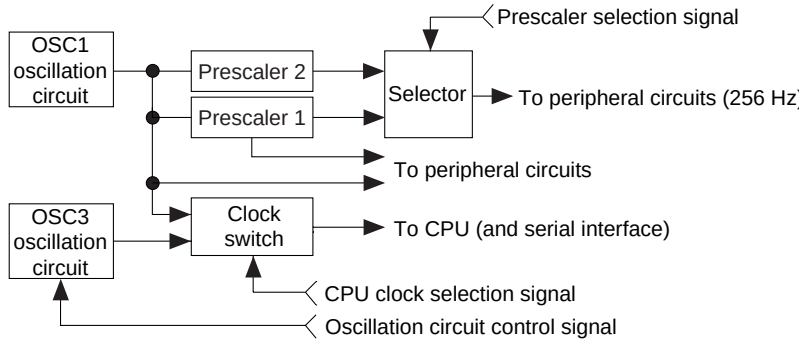


Fig. 4.3.1.1 Oscillation system

As Figure 4.3.1.1 indicates, two prescalers (demultiplier stage) are connected to the oscillation circuit. Prescaler 1 is for 32.768 kHz and prescaler 2 is for 38.4 kHz. These can be selected through the software to suit the crystal oscillator. This selection invokes the basic signal (256 Hz) for running the clock timer, stopwatch timer, and so forth.
Also for E0C60A08, selection of either OSC1 or OSC3 for the CPU's operating clock can be made through the software.

4.3.2 OSC1 oscillation circuit

The E0C6008 Series has a built-in crystal oscillation circuit (OSC1 oscillation circuit). As an external element, the OSC1 oscillation circuit generates the operating clock for the CPU and peripheral circuits by connecting the crystal oscillator (Typ. 32.768 kHz) and trimmer capacitor (5–25 pF).
Figure 4.3.2.1 is the block diagram of the OSC1 oscillation circuit.

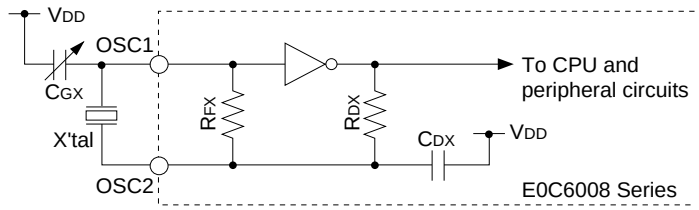


Fig. 4.3.2.1 OSC1 oscillation circuit

As Figure 4.3.2.1 indicates, the crystal oscillation circuit can be configured simply by connecting the crystal oscillator (X'tal) between terminals OSC1 and OSC2 to the trimmer capacitor (C_{GX}) between terminals OSC1 and V_{DD}.
Also, the crystal oscillator can be connected to the 38.4 kHz oscillator in addition to the 32.768 kHz oscillator.

4.3.3 OSC3 oscillation circuit

In the E0C6008 Series, the E0C60A08 has twin clock specification. The mask option enables selection of either the CR or ceramic oscillation circuit (OSC3 oscillation circuit) as the CPU's subclock source. Because the oscillation circuit itself is built-in, it provides the resistance as an external element when CR oscillation is selected, but when ceramic oscillation is selected both the ceramic oscillator and two capacitors (gate and drain capacitance) are required.
Figure 4.3.3.1 is the block diagram of the OSC3 oscillation circuit.

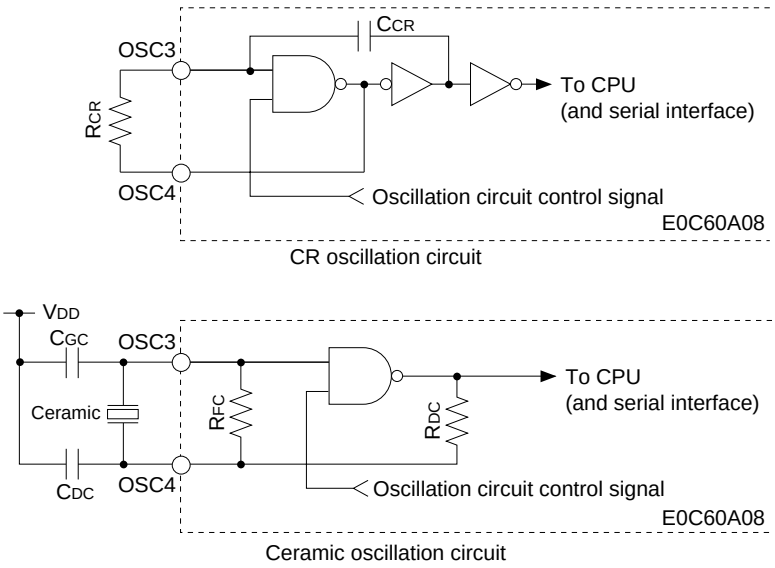


Fig. 4.3.3.1 OSC3 oscillation circuit

As indicated in Figure 4.3.3.1, the CR oscillation circuit can be configured simply by connecting the resistor (R_{CR}) between terminals OSC3 and OSC4 when CR oscillation is selected. When 82 kΩ is used for R_{CR}, the oscillation frequency is about 410 kHz. When ceramic oscillation is selected, the ceramic oscillation circuit can be configured by connecting the ceramic oscillator (Typ. 500 kHz) between terminals OSC3 and OSC4 to the two capacitors (C_{GC} and C_{DC}) located between terminals OSC3 and OSC4 and V_{DD}. For both C_{GC} and C_{DC}, connect capacitors that are about 100 pF. To lower current consumption of the OSC3 oscillation circuit, oscillation can be stopped through the software.

For the E0C6008 and E0C60L08 (single clock specification), do not connect anything to terminals OSC3 and OSC4.

4.3.4 Control of oscillation circuit and prescaler

Table 4.3.4.1 lists the control bits and their addresses for the oscillation circuit.

Table 4.3.4.1 Control bits of oscillation circuit and prescaler

Address	Register								Comment
	D3	D2	D1	D0	Name	Init *1	1	0	
2FEH	PRSM	CLKCHG	OSCC	IOC1	PRSM	0	38 kHz	32 kHz	OSC1 prescaler selection
					CLKCHG	0	OSC3	OSC1	CPU clock switch
	R/W				OSCC	0	On	Off	OSC3 oscillation On/Off
					IOC1	0	Output	Input	I/O control register (P10–P13)

*1 Initial value at initial reset
*2 Not set in the circuit
*3 Always "0" being read
*4 Reset (0) immediately after being read
*5 Undefined

OSCC: OSC3 oscillation control (2FEH•D1)

Controls oscillation ON/OFF for the OSC3 oscillation circuit. (E0C60A08 only.)

When "1" is written : The OSC3 oscillation ON
When "0" is written : The OSC3 oscillation OFF
Read-out : Valid

When it is necessary to operate the CPU of the E0C60A08 at high speed, set OSCC to "1". At other times, set it to "0" to reduce current consumption.
For E0C6008 and E0C60L08, keep OSCC set to "0".
At initial reset, OSCC is set to "0".

CLKCHG: CPU clock switch (2FEH•D2)

The CPU's operation clock is selected with this register. (E0C60A08 only.)

When "1" is written : OSC3 clock is selected
When "0" is written : OSC1 clock is selected
Read-out : Valid

When the E0C60A08's CPU clock is to be OSC3, set CLKCHG to "1"; for OSC1, set CLKCHG to "0". This register cannot be controlled for E0C6008 and E0C60L08, so that OSC1 is selected no matter what the set value.
At initial reset, CLKCHG is set to "0".

PRSM: OSC1 prescaler selection (2FEH•D3)

Selects the prescaler for the crystal oscillator of the OSC1 oscillation circuit.

When "1" is written : 38.4 kHz
When "0" is written : 32.768 kHz
Read-out : Valid

Operation of the clock timer and stopwatch timer can be mode accurate by selecting this register. When the set value for this register does not suit the crystal oscillator used, the operation cycles of the previously mentioned peripheral circuitry is multiplied as shown below.

f_{OSC1} = 32.768 kHz and PRSM = "1": $T' \cong 1.172T$
f_{OSC1} = 38.4 kHz and PRSM = "0": $T' \cong 0.853T$

At initial reset, PRSM is set to "0".

4.3.5 Programming notes

(1) It takes at least 5 msec from the time the OSC3 oscillation circuit goes ON until the oscillation stabilizes. Consequently, when switching the CPU operation clock from OSC1 to OSC3, do this after a minimum of 5 msec have elapsed since the OSC3 oscillation went ON.
Further, the oscillation stabilization time varies depending on the external oscillator characteristics and conditions of use, so allow ample margin when setting the wait time.

(2) When switching the clock form OSC3 to OSC1, use a separate instruction for switching the OSC3 oscillation OFF. An error in the CPU operation can result if this processing is performed at the same time by the one instruction.

(3) To operate the clock timer and stopwatch timer accurately, select the prescaler of the OSC1 to match the crystal oscillator used.

4.4 Input Ports (K00–K03, K10, K20–K23)

4.4.1 Configuration of input ports

The E0C6008 Series has nine bits (4 bits × 2 + 1 bit) of general-purpose input ports. Each of the input port terminals (K00–K03, K10, K20–K23) provides internal pull-down resistor. Pull-down resistor can be selected for each bit with the mask option.
Figure 4.4.1.1 shows the configuration of input port.

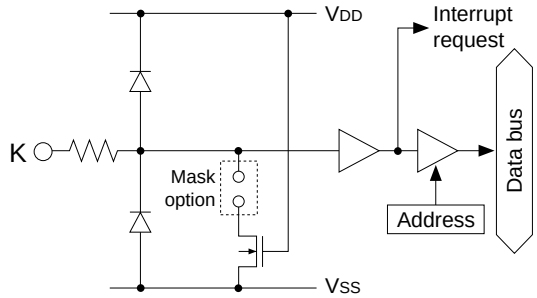


Fig. 4.4.1.1 Configuration of input port

Selection of "With pull-down resistor" with the mask option suits input from the push switch, key matrix, and so forth. When "Gate direct" is selected, the port can be used for slide switch input and interfacing with other LSIs.

Further, The input port terminal K02 and K03 are used as the input terminals for the event counter. (See Section 4.12, "Event Counter", for details.)

4.4.2 Input comparison registers and interrupt function

All nine bits of the input ports (K00–K03, K10, K20–K23) provide the interrupt function for the five bits, K00–K03 and K10. The conditions for issuing an interrupt can be set by the software for the five bits, K00–K03 and K10. Further, whether to mask the interrupt function can be selected individually for all nine bits by the software.
Figure 4.4.2.1 shows the configuration of K00–K03 and K10.
Figure 4.4.2.3 shows the configuration of K20–K23.

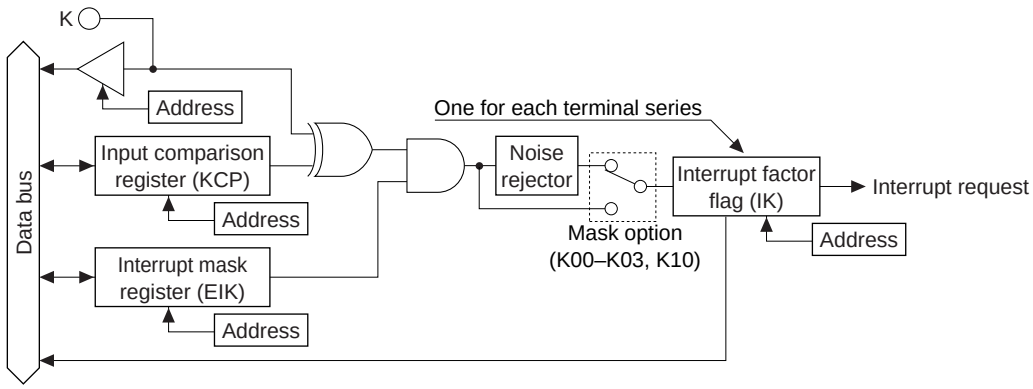


Fig. 4.4.2.1 Input interrupt circuit configuration (K00–K03, K10)

The input interrupt timing for K00–K03 and K10 depends on the value set for the input comparison registers (KCP00–KCP03 and KCP10). Interrupt can be selected to occur at the rising or falling edge of the input.
The interrupt mask registers (EIK00–EIK03, EIK10) enables the interrupt mask to be selected individually for K00–K03 and K10. However, whereas the interrupt function is enabled inside K00–K03, the interrupt occurs when the contents change from matching those of the input comparison register to non-matching contents. Interrupt for K10 can be generated by setting the same conditions individually.
When the interrupt is generated, the interrupt factor flag (IK0 and IK1) is set to "1".
Figure 4.4.2.2 shows an example of an interrupt for K00–K03.

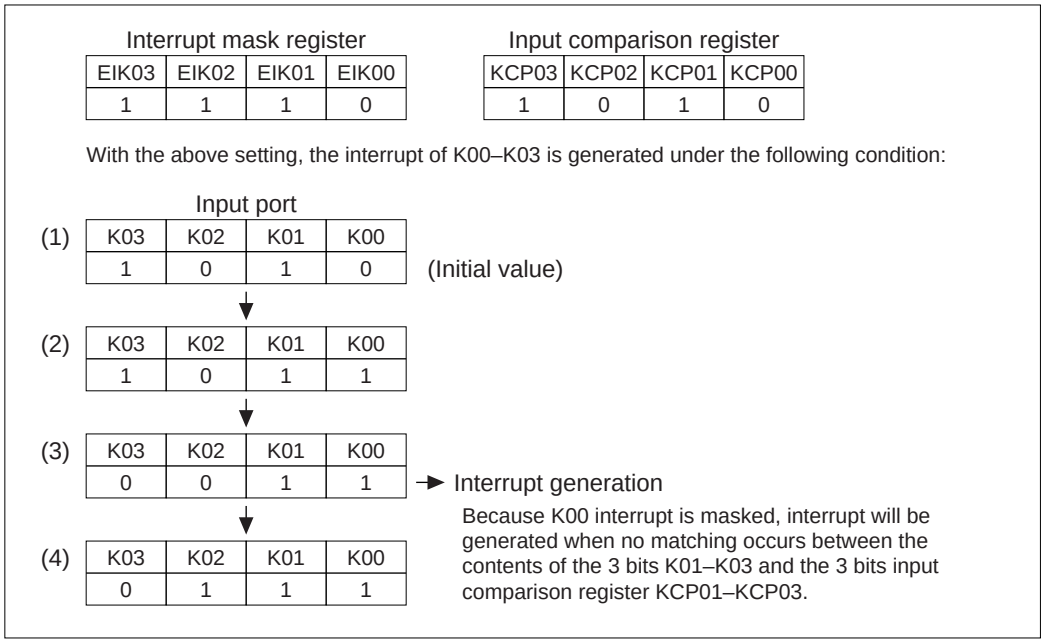


Fig. 4.4.2.2 Example of interrupt of K00–K03

K00 is masked by the interrupt mask register (EIK00), so that an interrupt does not occur at (2). At (3), K03 changes to "0"; the data of the terminal that is interrupt enabled no longer matches the data of the input comparison register, so that interrupt occurs. As already explained, the condition for the interrupt to occur is the change in the port data and contents of the input comparison register from matching to nonmatching. Hence, in (4), when the nonmatching status changes to another nonmatching status, an interrupt does not occur. Further, terminals that have been masked for interrupt do not affect the conditions for interrupt generation.

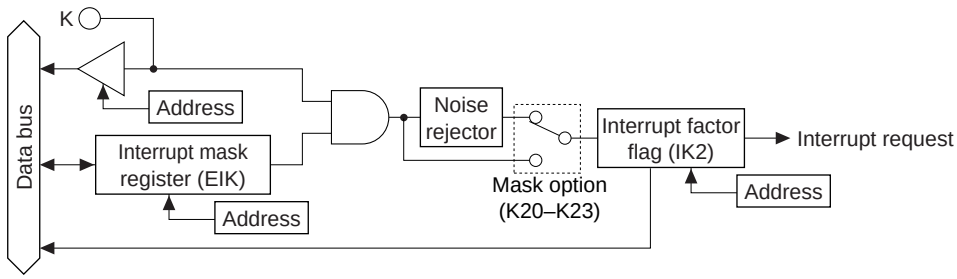


Fig. 4.4.2.3 Input interrupt circuit configuration (K20–K23)

There is no input comparison register for K20–K23, and interrupt is fixed to occur at th rising edge of input. The interrupt mask can be selected for each of the four terminals with the interrupt mask register (EIK20–EIK23). When all the enabled terminals are "0", interrupt occurs when one or more of the ports changed to "1".
When an interrupt occurs, the interrupt factor flag (IK2) is set to "1".
Figure 4.4.2.4 shows an example of an interrupt being generated for K20–K23.

Interrupt mask register

EIK23	EIK22	EIK21	EIK20
0	1	1	1

With the above setting, the interrupt of K20–K23 is generated under the following condition:

Input port

(1)

K23	K22	K21	K20
0	0	0	0

(Initial value)

(2)

K23	K22	K21	K20
1	0	0	0

(3)

K23	K22	K21	K20
1	0	1	0

→ Interrupt generation

Because K23 interrupt is masked, interrupt will be generated when one or more terminals among the 3 bits K20–K22 become "1" from a state where all terminals were "0".

(4)

K23	K22	K21	K20
1	0	1	1

Fig. 4.4.2.4 Example of interrupt of K20–K23

The mask register (EIK23) masks the interrupt of K23, so an interrupt does not occur at (2). At (3), K21 becomes "1", so that an interrupt occurs if the interrupt enabled terminals were all "0" and at least one terminal then changes to "1".
At (4), the conditions for interrupt are not established, so an interrupt does not occur.
Futher, terminals that have been masked for interrupt do not affect the conditions for interrupt generation.

4.4.3 Mask option

The contents that can be selected with the input port mask option are as follows:

(1) Internal pull-down resistor can be selected for each of the nine bits of the input ports (K00–K03, K10, K20–K23).
When you have selected "Gate direct", take care that the floating status does not occur for the input. Select "With pull-down resistor" for input ports that are not being used.

(2) The input interrupt circuit contains a noise rejector for preventing interrupt occurring through noise. The mask option enables selection of whether to use the noise rejector for each separate terminal series.
When "Use" is selected, a maximum delay of 1 msec occurs from the time interrupt condition is established until the interrupt factor flag (IK) is set to "1".

4.4.4 Control of input ports

Table 4.4.4.1 lists the input ports control bits and their addresses.

Table 4.4.4.1 Input port control bits

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
2E3H	K03	K02	K01	K00	K03	– *2	High	Low	Input port data (K00–K03)
					K02	– *2	High	Low	
					K01	– *2	High	Low	
	R				K00	– *2	High	Low	
2E4H	KCP03	KCP02	KCP01	KCP00	KCP03	0	↓	↑	Input comparison register (K00–K03)
					KCP02	0	↓	↑	
					KCP01	0	↓	↑	
	R/W				KCP00	0	↓	↑	
2E5H	EIK03	EIK02	EIK01	EIK00	EIK03	0	Enable	Mask	Interrupt mask register (K00–K03)
					EIK02	0	Enable	Mask	
					EIK01	0	Enable	Mask	
	R/W				EIK00	0	Enable	Mask	
2E7H	SCTRG	EIK10	KCP10	K10	SCTRG*3	–	Trigger	–	Serial I/F clock trigger
					EIK10	0	Enable	Mask	Interrupt mask register (K10)
					KCP10	0	↓	↑	Input comparison register (K10)
	W	R/W		R	K10	– *2	High	Low	Input port data (K10)
2EAH	IK1	IK0	SWIT1	SWIT0	IK1 *4	0	Yes	No	Interrupt factor flag (K10)
					IK0 *4	0	Yes	No	Interrupt factor flag (K00–K03)
					SWIT1 *4	0	Yes	No	Interrupt factor flag (stopwatch 1 Hz)
	R				SWIT0 *4	0	Yes	No	Interrupt factor flag (stopwatch 10 Hz)
2F3H	0	0	IK2	ISIO	0 *3	– *2	–	–	Unused
					0 *3	– *2	–	–	Unused
	R				IK2 *4	0	Yes	No	Interrupt factor flag (K20–K23)
					ISIO *4	0	Yes	No	Interrupt factor flag (serial I/F)
2F4H	K23	K22	K21	K20	K23	– *2	High	Low	Input port data (K20–K23)
					K22	– *2	High	Low	
					K21	– *2	High	Low	
	R				K20	– *2	High	Low	
2F5H	EIK23	EIK22	EIK21	EIK20	EIK23	0	Enable	Mask	Interrupt mask register (K20–K23)
					EIK22	0	Enable	Mask	
					EIK21	0	Enable	Mask	
	R/W				EIK20	0	Enable	Mask	

*1 Initial value at initial reset
*2 Not set in the circuit
*3 Always "0" being read
*4 Reset (0) immediately after being read
*5 Undefined

K00–K03, K10, K20–K23: Input port data (2E3H, 2E7H•D0, 2F4H)

Input data of the input port terminals can be read out with these registers.

When "1" is read out : High level
When "0" is read out : Low level
Writing : Invalid

The read-out is "1" when the terminal voltage of the nine bits of the input ports (K00–K03, K10, K20–K23) goes high (V_{DD}), and "0" when the voltage goes low (V_{SS}).
These bits are dedicated for read-out, so writing cannot be done.

KCP00–KCP03, KCP10: Input comparison registers (2E4H, 2E7H•D1)

Interrupt conditions for terminals K00–K03 and K10 can be set with these registers.

When "1" is written : Falling edge
When "0" is written : Rising edge
Read-out : Valid

Of the nine bits of the input ports, the interrupt conditions can be set for the rising or falling edge of input for each of the five bits (K00–K03 and K10), through the input comparison registers (KCP00–KCP03 and KCP10).
At initial reset, these registers are set to "0".

EIK00–EIK03, EIK10, EIK20–EIK23: Interrupt mask registers (2E5H, 2E7H•D2, 2F5H)

Masking the interrupt of the input port terminals can be selected with these registers.

When "1" is written : Enable
When "0" is written : Mask
Read-out : Valid

With these registers, masking of the input port bits can be selected for each of the nine bits.
Writing to the interrupt mask registers can be done only in the DI status (interrupt flag = "0").
At initial reset, these registers are all set to "0".

IK0, IK1, IK2: Interrupt factor flags (2EAH•D2 and D3, 2F3H•D1)

These flags indicate the occurrence of input interrupt.

When "1" is read out : Interrupt has occurred
When "0" is read out : Interrupt has not occurred
Writing : Invalid

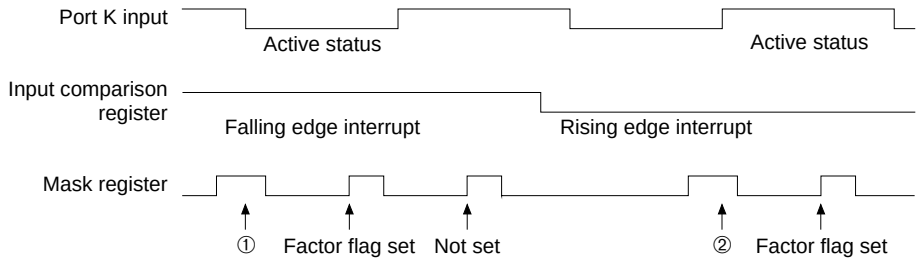
The interrupt factor flags IK0, IK1 and IK2 are associated with K00–K03, K10 and K20–K23, respectively. From the status of these flags, the software can decide whether an input interrupt has occurred.
These flags are reset when the software reads them. Read-out can be done only in the DI status (interrupt flag = "0").
At initial reset, these flags are set to "0".

4.4.5 Programming notes

(1) When input ports are changed from high to low by pull-down resistance, the fall of the waveform is delayed on account of the time constant of the pull-down resistance and input gate capacitance. Hence, when fetching input ports, set an appropriate wait time.
Particular care needs to be taken of the key scan during key matrix configuration. Aim for a wait time of about 1 msec.

(2) When "Use" is selected with the noise rejector mask option, a maximum delay of 1 msec occurs from time the interrupt conditions are established until the interrupt factor flag (IK) is set to "1" (until the interrupt is actually generated). Hence, pay attention to the timing when reading out (resetting) the interrupt factor flag. For example, when performing a key scan with the key matrix, the key scan changes the input status to set the interrupt factor flag, so it has to be read out to reset it. However, if the interrupt factor flag is read out immediately after key scanning, the delay will cause the flag to be set after read-out, so that it will not be reset.

(3) Input interrupt programing related precautions



When the content of the mask register is rewritten while the port K input is in the active status, the input interrupt factor flags are set at ① and ②, ① being the interrupt due to the falling edge and ② the interrupt due to the rising edge.

Fig. 4.4.5.1 Input interrupt timing

When using an input interrupt, if you rewrite the content of the mask register, when the value of the input terminal which becomes the interrupt input is in the active status, the factor flag for input interrupt may be set.
Therefore, when using the input interrupt, the active status of the input terminal implies
input terminal = low status, when the falling edge interrupt is effected and
input terminal = high status, when the rising edge interrupt is effected.
When an interrupt is triggered at the falling edge of an input terminal, a factor flag is set with the timing of ① shown in Figure 4.4.5.1. However, when clearing the content of the mask register with the input terminal kept in the low status and then setting it, the factor flag of the input interrupt is again set at the timing that has been set.
Consequently, when the input terminal is in the active status (low status), do not rewrite the mask register (clearing, then setting the mask register), so that a factor flag will only set at the falling edge in this case. When clearing, then setting the mask register, set the mask register, when the input terminal is not in the active status (high status).
When an interrupt is triggered at the rising edge of the input terminal, a factor flag will be set at the timing of ② shown in Figure 4.4.5.1. In this case, when the mask registers cleared, then set, you should set the mask register, when the input terminal is in the low status.
In addition, when the mask register = "1" and the content of the input comparison register is rewritten in the input terminal active status, an input interrupt factor flag may be set. Thus, you should rewrite the content of the input comparison register in the mask register = "0" status.

(4) Read out the interrupt factor flag (IK) only in the DI status (interrupt flag = "0"). Read-out during EI status (interrupt flag = "1") will cause malfunction.

(5) Write the interrupt mask register (EIK) only in the DI status (interrupt flag = "0"). Writing during EI status (interrupt flag = "1") will cause malfunction.

4.5 Output Ports (R00–R03, R10–R13)

4.5.1 Configuration of output ports

The E0C6008 Series has eight bits (4 bits × 2) of general output ports.
Output specifications of the output ports can be selected individually with the mask option. Two kinds of output specifications are available: complementary output and Pch open drain output.
Further, the mask option enables the output ports R10–R13 to be used as special output ports.
Figure 4.5.1.1 shows the configuration of the output ports.

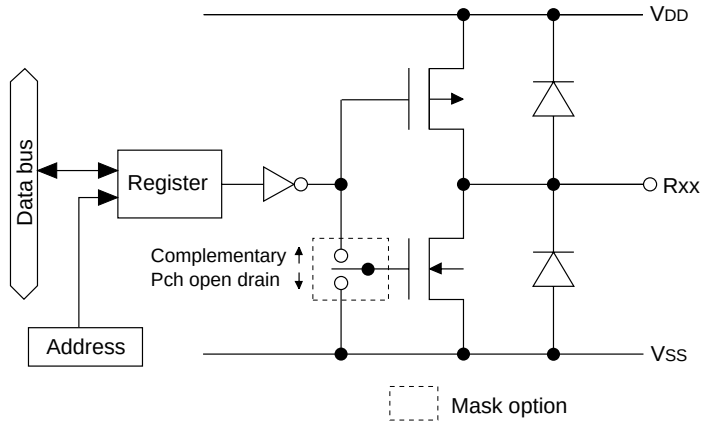


Fig. 4.5.1.1 Configuration of output ports

4.5.2 Mask option

The mask option enables the following output port selection.

(1) Output specifications of output ports

Output specifications for the output ports (R00–R03, R10–R13) enable selection of either complementary output or Pch open drain output for each of the eight bits.
However, even when Pch open drain output is selected, voltage exceeding source voltage must not be applied to the output port.

(2) Special output

In addition to the regular DC output, special output can be selected for the output ports R10–R13 as shown in Table 4.5.2.1. Figure 4.5.2.1 shows the structure of the output ports R10–R13.

Table 4.5.2.1 Special output

Output port	Special output
R10	BZ output
R13	$\overline{BZ}$ output (selectable only when R10 is used as BZ output)
R11	SIOF output
R12	FOUT output

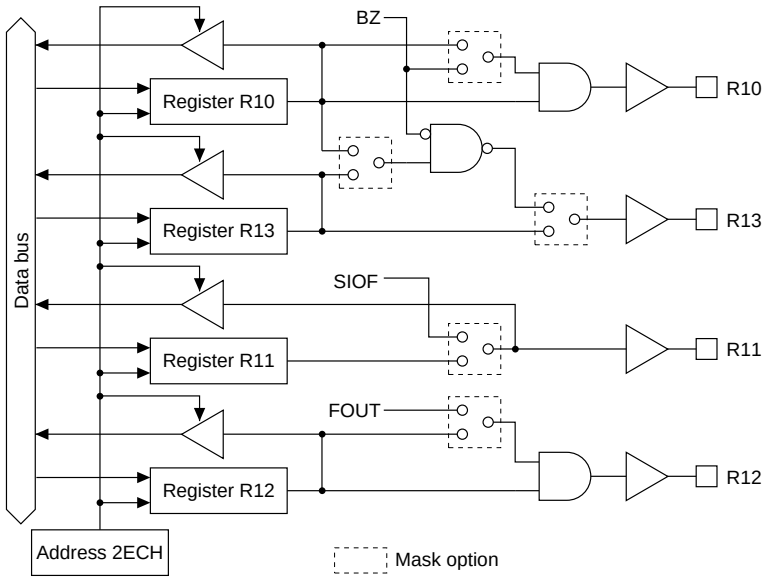


Fig. 4.5.2.1 Structure of output port R10–R13

BZ, $\overline{BZ}$ (R10, R13)

BZ and $\overline{BZ}$ are the buzzer signal output for driving the piezoelectric buzzer. The buzzer signal is generated by demultiplicaion of fOSC1. The buzzer signal frequency can be selected by software. Also, a digital envelope can be added to the buzzer signal. See Section 4.11, "Sound Generator", for details.

Notes: • When the BZ and $\overline{BZ}$ output signals are turned ON or OFF, a hazard can result.
• When DC output is set for the output port R10, the output port R13 cannot be set for $\overline{BZ}$ output.

Figure 4.5.2.2 shows the output waveform for BZ and $\overline{BZ}$.

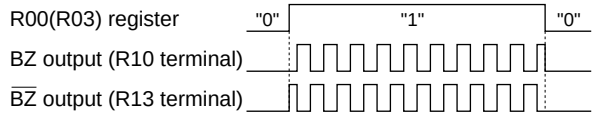


Fig. 4.5.2.2 Output waveform of BZ and $\overline{BZ}$

SIOF (R11)

When the output port R11 is set for SIOF output, it outputs the signal indicating the running status (RUN/STOP) of the serial interface. See Section 4.7, "Serial Interface", for details.

FOUT (R12)

When the output port R12 is set for FOUT output, it outputs the clock of fOSC1 or the demultiplied fOSC1. The clock frequency is selectable with the mask options, from the frequencies listed in Table 4.5.2.2.

Table 4.5.2.2 FOUT clock frequency

Setting value	Clock frequency (Hz)	
	fOSC1 = 32.768 kHz	fOSC1 = 38.400 kHz
fOSC1 / 1	32,768	38,400
fOSC1 / 2	16,384	19,200
fOSC1 / 4	8,192	9,600
fOSC1 / 8	4,096	4,800
fOSC1 / 16	2,048	2,400
fOSC1 / 32	1,024	1,200
fOSC1 / 64	512	600
fOSC1 / 128	256	300

Note: A hazard may occur when the FOUT signal is turned ON or OFF.

4.5.3 Control of output ports

Table 4.5.3.1 lists the output ports' control bits and their addresses.

Table 4.5.3.1 Control bits of output ports

Address	Register								Comment
	D3	D2	D1	D0	Name	Init *1	1	0	
2EBH	R03	R02	R01	R00	R03	0	High	Low	Output port (R03)
					R02	0	High	Low	Output port (R02)
	R/W				R01	0	High	Low	Output port (R01)
					R00	0	High	Low	Output port (R00)
2ECH	R13	R12	R11/SIOF	R10	R13	0	High/On	Low/Off	Output port (R13)/$\overline{BZ}$ output control
					R12	0	High/On	Low/Off	Output port (R12)/FOUT output control
	R/W		R/W	R/W	R11	0	High	Low	Output port (R11, LAMP)
			R		SIOF	0	Run	Stop	Output port (SIOF)
					R10	0	High/On	Low/Off	Output port (R10)/BZ output control

*1 Initial value at initial reset
*2 Not set in the circuit
*3 Always "0" being read
*4 Reset (0) immediately after being read
*5 Undefined

R00–R03, R10–R13 (when DC output): Output port data (2EBH, 2ECH)

Sets the output data for the output ports.

When "1" is written : High output
When "0" is written : Low output
Read-out : Valid

The output port terminals output the data written in the corresponding registers (R00–R03, R10–R13) without changing it. When "1" is written in the register, the output port terminal goes high (V_{DD}), and when "0" is written, the output port terminal goes low (V_{SS}).
At initial reset, all registers are set to "0".

R10, R13 (when BZ and $\overline{BZ}$ output is selected): Buzzer output control (2ECH•D0 and D3)

These bits control the output of the buzzer signals (BZ, $\overline{BZ}$).

When "1" is written : Buzzer signal is output
When "0" is written : Low level (DC) is output
Read-out : Valid

$\overline{BZ}$ is output from terminal R13. With the mask option, selection can be made perform this output control by R13, or to perform output control simultaneously with BZ by R10.

- ***When R13 controls $\overline{BZ}$ output***

  BZ output and $\overline{BZ}$ output can be controlled independently. BZ output is controlled by writing data to R10, and $\overline{BZ}$ output is controlled by writing data to R13.

- ***When R10 controls $\overline{BZ}$ output***

  BZ output and $\overline{BZ}$ output can be controlled simultaneously by writing data to R10 only. For this case, R13 can be used as a one-bit general register having both read and write functions, and data of this register exerts no affect on $\overline{BZ}$ output (output from the R13 pin).

At initial reset, registers R10 and R13 are set to "0".

R11 (when SIOF output is selected): Serial interface status (2ECH•D1)

Indicates the running status of the serial interface.

When "1" is read out : RUN
When "0" is read out : STOP
Writing : Valid

See Section 4.7, "Serial Interface", for details of SIOF.
This bit is exclusively for reading out, so data cannot be written to it.

R12 (when FOUT is selected): FOUT output control (2ECH•D2)

Controls the FOUT (clock) output.

When "1" is written : Clock output
When "0" is written : Low level (DC) output
Read-out : Valid

FOUT output can be controlled by writing data to R12.
At initial reset, this register is set to "0".

4.5.4 Programming note

When BZ, $\overline{BZ}$ and FOUT are selected with the mask option, a hazard may be observed in the output waveform when the data of the output register changes.

4.6 I/O Ports (P00–P03, P10–P13)

4.6.1 Configuration of I/O ports

The E0C6008 Series has eight bits (4 bits × 2) of general-purpose I/O ports. Figure 4.6.1.1 shows the configuration of the I/O ports.
The four bits of each of the I/O ports P00–P03 and P10–P13 can be set to either input mode or output mode. Modes can be set by writing data to the I/O control register.

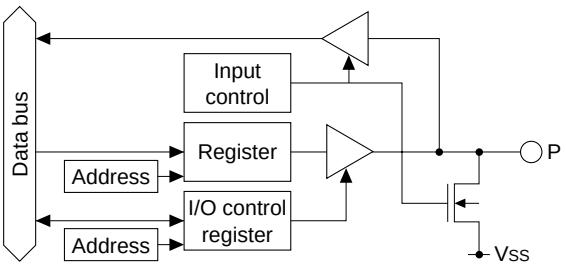


Fig. 4.6.1.1 Configuration of I/O port

4.6.2 I/O control register and I/O mode

Input or output mode can be set for the four bits of I/O port P00–P03 and I/O port P10–P13 by writing data into the corresponding I/O control register IOC0 and IOC1.

To set the input mode, "0" is written to the I/O control register. When an I/O port is set to input mode, it becomes high impedance status and works as an input port.
However, the input line is pulled down when input data is read.

The output mode is set when "1" is written to the I/O control register. When an I/O port set to output mode works as an output port, it outputs a high signal (V_{DD}) when the port output data is "1", and a low signal (V_{SS}) when the port output data is "0".

At initial reset, the I/O control registers are set to "0", and the I/O port enters the input mode.

4.6.3 Mask option

The output specification during output mode (IOC = "1") of these I/O ports can be set with the mask option for either complementary output or Pch open drain output. This setting can be performed for each bit of each port.
However, when Pch open drain output has been selected, voltage in excess of the power voltage must not be applied to the port.

4.6.4 Control of I/O ports

Table 4.6.4.1 lists the I/O ports' control bits and their addresses.

Table 4.6.4.1 I/O port control bits

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
2EDH	P03	P02	P01	P00	P03	– *2	High	Low	I/O port data (P00–P03)
					P02	– *2	High	Low	
	R/W				P01	– *2	High	Low	Output latch is reset at initial reset
					P00	– *2	High	Low	
2EEH	TMRST	SWRUN	SWRST	IOC0	TMRST*3	Reset	Reset	–	Clock timer reset
					SWRUN	0	Run	Stop	Stopwatch timer Run/Stop
	W	R/W	W	R/W	SWRST*3	Reset	Reset	–	Stopwatch timer reset
					IOC0	0	Output	Input	I/O control register 0 (P00–P03)
2FDH	P13	P12	P11	P10	P13	– *2	High	Low	I/O port data (P10–P13)
					P12	– *2	High	Low	
	R/W				P11	– *2	High	Low	Output latch is reset at initial reset
					P10	– *2	High	Low	
2FEH	PRSM	CLKCHG	OSCC	IOC1	PRSM	0	38 kHz	32 kHz	OSC1 prescaler selection
					CLKCHG	0	OSC3	OSC1	CPU clock switch
	R/W				OSCC	0	On	Off	OSC3 oscillation On/Off
					IOC1	0	Output	Input	I/O control register (P10–P13)

*1 Initial value at initial reset
*2 Not set in the circuit
*3 Always "0" being read
*4 Reset (0) immediately after being read
*5 Undefined

P00–P03, P10–P13: I/O port data (2EDH, 2FDH)

I/O port data can be read and output data can be set through these ports.

When writing data

When "1" is written : High level
When "0" is written : Low level

When an I/O port is set to the output mode, the written data is output unchanged from the I/O port terminal. When "1" is written as the port data, the port terminal goes high (V_{DD}), and when "0" is written, the level goes low (V_{SS}).
Port data can be written also in the input mode.

When reading data out

When "1" is read out : High level
When "0" is read out : Low level

The terminal voltage level of the I/O port is read out. When the I/O port is in the input mode the voltage level being input to the port terminal can be read out; in the output mode the output voltage level can be read. When the terminal voltage is high (V_{DD}) the port data that can be read is "1", and when the terminal voltage is low (V_{SS}) the data is "0".
Further, the built-in pull-down resistance goes ON during read-out, so that the I/O port terminal is pulled down.

Notes:
- *When the I/O port is set to the output mode and a low-impedance load is connected to the port terminal, the data written to the register may differ from the data read out.*
- *When the I/O port is set to the input mode and a low-level voltage (V_{SS}) is input, erroneous input results if the time constant of the capacitive load of the input line and the built-in pull-down resistance load is greater than the read-out time. When the input data is being read out, the time that the input line is pulled down is equivalent to 1.5 cycles of the CPU system clock. However, the electric potential of the terminals must be settled within 0.5 cycles. If this condition cannot be fulfilled, some measure must be devised such as arranging pull-down resistance externally, or performing multiple read-outs.*

IOC0, IOC1: I/O control registers (2EEH•D0, 2FEH•D0)

The input and output modes of the I/O ports can be set with these registers.

When "1" is written : Output mode
When "0" is written : Input mode
Read-out : Valid

The input and output modes of the I/O ports are set in units of four bits. IOC0 sets the mode for P00–P03, and IOC1 sets the mode for P10–P13.
Writing "1" to the I/O control register makes the corresponding I/O port enter the output mode, and writing "0" induces the input mode.
At initial reset, these two registers are set to "0", so the I/O ports are in the input mode.

4.6.5 Programming notes

(1) When input data are changed from high to low by built-in pull-down resistance, the fall of the waveform is delayed on account of the time constant of the pull-down resistance and input gate capacitance. Consequently, if data is read out while the CPU is running in the OSC3 oscillation circuit, data must be read out continuously for about 500 µsec.

(2) When the I/O port is set to the output mode and the data register has been read, the terminal data instead of the register data can be read out. Because of this, if a low-impedance load is connected and read-out performed, the value of the register and the read-out result may differ.

4.7 Serial Interface (SIN, SOUT, SCLK)

4.7.1 Configuration of serial interface

The E0C6008 Series has a synchronous clock type 8 bits serial interface built-in.
The configuration of the serial interface is shown in Figure 4.7.1.1.
The CPU, via the 8 bits shift register, can read the serial input data from the SIN terminal. Moreover, via the same 8 bits shift register, it can convert parallel data to serial data and output it to the SOUT terminal.
The synchronous clock for serial data input/output may be set by selecting by software any one of 3 types of master mode (internal clock mode: when the E0C6008 Series is to be the master for serial input/output) and a type of slave mode (external clock mode: when the E0C6008 Series is to be the slave for serial input/output).
Also, when the serial interface is used at slave mode, SIOF signal which indicates whether or not the serial interface is available to transmit or receive can be output to output port R11 by mask option.

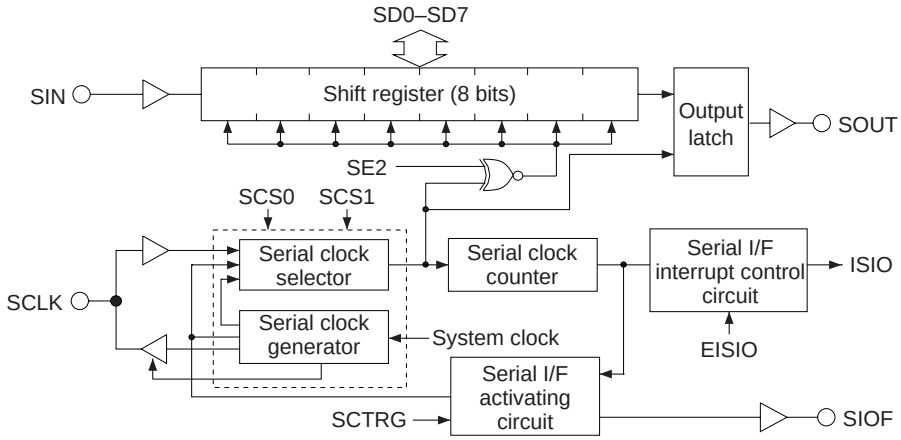


Fig. 4.7.1.1 Configuration of serial interface

4.7.2 Master mode and slave mode of serial interface

The serial interface of the E0C6008 Series has two types of operation mode: master mode and slave mode.
In the master mode, it uses an internal clock as synchronous clock of the built-in shift register, generates this internal clock at the SCLK terminal and controls the external (slave side) serial device.
In the slave mode, the synchronous clock output from the external (master side) serial device is input from the SCLK terminal and uses it as the synchronous clock to the built-in shift register.
The master mode and slave mode are selected by writing data to registers SCS1 and SCS0 (address 2F2H•D2, D3).
When the master mode is selected, a synchronous clock may be selected from among 3 types as shown in Table 4.7.2.1.

Table 4.7.2.1 Synchronous clock selection

SCS1	SCS0	Mode	Synchronous clock
0	0	Master mode	CLK
0	1		CLK/2
1	0		CLK/4
1	1	Slave mode	External clock

CLK: CPU system clock

At initial reset, the slave mode (external clock mode) is selected.
Moreover, the synchronous clock, along with the input/output of the 8 bits serial data, is controlled as follows:

- At master mode, after output of 8 clocks from the SCLK terminal, clock output is automatically suspended and SCLK terminal is fixed at low level.
- At slave mode, after input of 8 clocks to the SCLK terminal, subsequent clock inputs are masked.

Note: When using the serial interface in the master mode, CPU system clock is used as the synchronous clock. Accordingly, when the serial interface is operating, system clock switching ($f_{OSC1} \leftrightarrow f_{OSC3}$) should not be performed.

A sample basic serial input/output portion connection is shown in Figure 4.7.2.1.

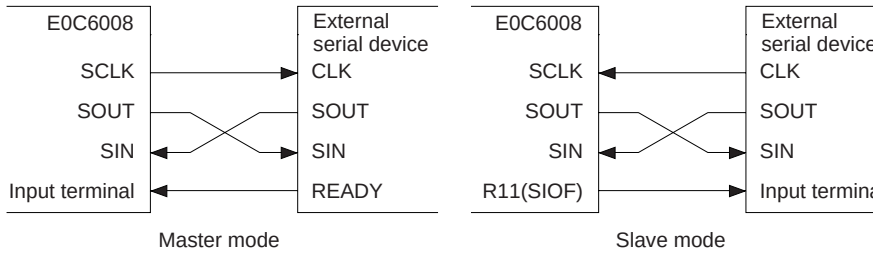


Fig. 4.7.2.1 Sample basic connection

4.7.3 Data input/output and interrupt function

The serial interface can input/output data via the internal 8 bits shift register. The shift register operates by synchronizing with either the synchronous clock output from SCLK terminal (master mode), or the synchronous clock input to SCLK (slave mode).
The serial interface generates interrupt on completion of the 8 bits serial data input/output. Detection of serial data input/output is done by the counting of the synchronous clock (SCLK); the clock completes input/output operation when 8 counts (equivalent to 8 cycles) have been made and then generates interrupt.
The serial data input/output procedure data is explained below:

(1) Serial data output procedure and interrupt

The serial interface is capable of outputting parallel data as serial data, in units of 8 bits.
By setting the parallel data to 4 bits registers SD0–SD3 (address 2F0H) and SD4–SD7 (address 2F1H) individually and writing "1" to SCTRG bit (address 2E7H·D3), it synchronizes with the synchronous clock and serial data is output at the SOUT terminal. The synchronous clock used here is as follows: in the master mode, internal clock which is output to the SCLK terminal while in the slave mode, external clock which is input from the SCLK terminal. The serial output of the SOUT termina changes with the rising edge of the clock that is input or output from the SCLK terminal.
The serial data to the built-in shift register is shifted with the rising edge of the SCLK signal when SE2 bit (address 2F2H•D1) is "1" and is shifted with the falling edge of the SCLK signal when SE2 bit (address 2F2H•D1) is "0".
When the output of the 8 bits data from SD0 to SD7 is completed, the interrupt factor flag ISIO (address 2F3H•D0) is set to "1" and interrupt is generated. Moreover, the interrupt can be masked by the interrupt mask register EISIO (address 2F2H•D0).

(2) Serial data input procedure and interrupt

The serial interface is capable of inputting serial data as parallel data, in units of 8 bits.
The serial data is input from the SIN terminal, synchronizes with the synchronous clock, and is sequentially read in the 8 bits shift register. As in the above item (1), the synchronous clock used here is as follows: in the master mode, internal clock which is output to the SCLK terminal while in the slave mode, external clock which is input from the SCLK terminal.
The serial data to the built-in shift register is read with the rising edge of the SCLK signal when SE2 bit is "1" and is read with the falling edge of the SCLK signal when SE2 bit is "0". Moreover, the shift register is sequentially shifted as the data is fetched.
When the input of the 8 bits data from SD0 to SD7 is completed, the interrupt factor flag ISIO is set to "1" and interrupt is generated. Moreover, the interrupt can be masked by the interrupt mask register EISIO. Note, however, that regardless of the setting of the interrupt mask register, the interrupt factor flag is set to "1" after input of the 8 bits data.
The data input in the shift register can be read from data registers SD0–SD7 by software.

(3) Serial data input/output permutation

The E0C6008 Series allows the input/output permutation of serial data to be selected by mask option as to either LSB first or MSB first. The block diagram showing input/output permutation in case of LSB first and MSB first is provided in Figure 4.7.3.1.

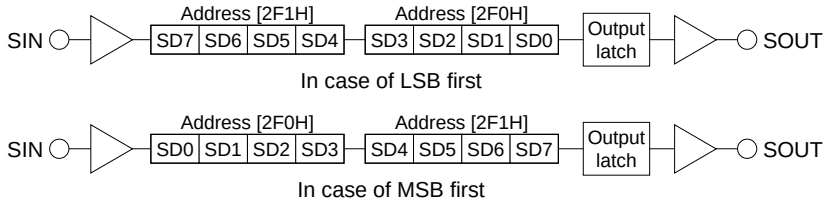


Fig. 4.7.3.1 Serial data input/output permutation

(4) SIOF signal

When the serial interface is used in the slave mode (external clock mode), SIOF is used to indicate whether the internal serial interface is available to transmit or receive data for the master side (external) serial device. SIOF signal is generated from output port R11 by mask option.
SIOF signal becomes "1" (high) when the E0C6008 serial interface becomes available to transmit or receive data; normally, it is at "0" (low).
SIOF signal changes from "0" to "1" immediately after "1" is written to SCTRG and returns from "1" to "0" when eight synchronous clock has been counted.

(5) Timing chart

The serial interface timing chart is shown in Figure 4.7.3.2.

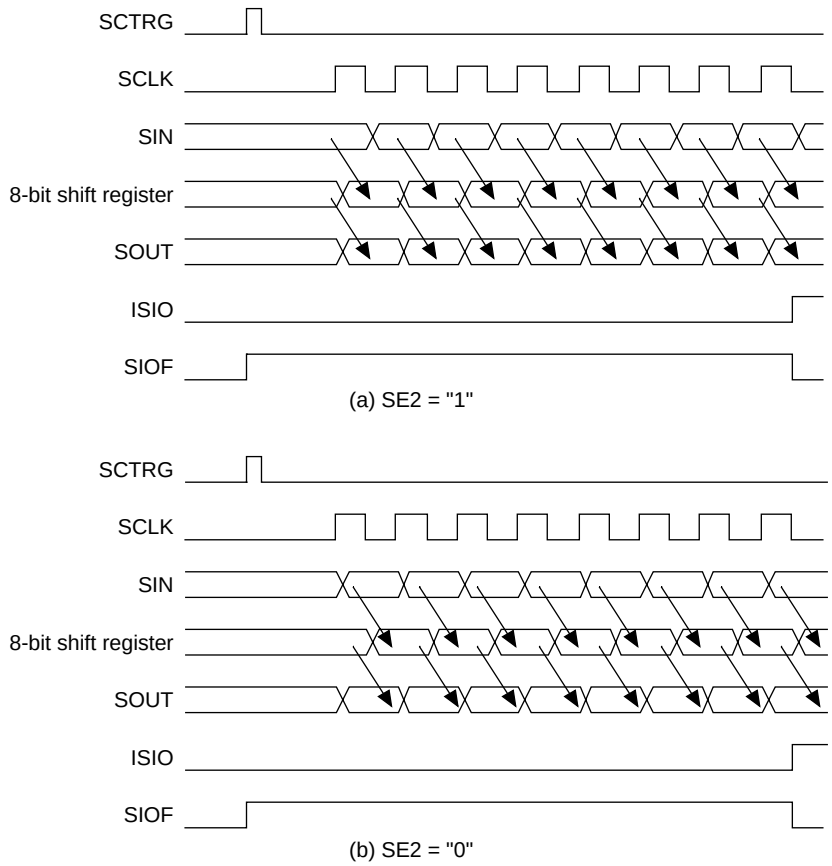


Fig. 4.7.3.2 Serial interface timing chart

4.7.4 Mask option

The serial interface may be selected for the following by mask option.

(1) Whether or not the SIN terminal will use built-in pull down resistor may be selected.
If the use of no pull down resistor is selected, take care that floating state does not occur at the SIN terminal. When the SIN terminal is not used, the use of pull down resistor should be selected.

(2) Either complementary output or P channel (Pch) open drain as output specification for the SOUT terminal may be selected.
However, even if Pch open drain has been selected, application of voltage exceeding power source voltage to the SOUT terminal will be prohibited.

(3) Whether or not the SCLK terminal will use pull down resistor which is turned ON during input mode (external clock) may be selected.
If the use of no pull down resistor is selected, take care that floating state does not occur at the SCLK terminal during input mode.
Normally, the use of pull down resistor should be selected.

(4) As output specification during output mode, either complementary output or P channel (Pch) open drain output may be selected for the SCLK terminal.

(5) Positive or negative logic can be selected for the signal logic of the SCLK pin (SCLK or $\overline{\text{SCLK}}$).
However, keep in mind that only pull-down resistance can be set for the input mode (pull-up resistance is not built-in).

(6) LSB first or MSB first as input/output permutation of serial data may be selected.

(7) Output port R11 may be assigned as SIOF output terminal which will indicate whether the serial interface is available to transmit or receive signals.

4.7.5 Control of serial interface

The control registers for the serial interface are explained below.

Table 4.7.5.1 Control bits of serial interface

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
2E7H	SCTRG	IK10	KCP10	K10	SCTRG*3	–	Trigger	–	Serial I/F clock trigger
					EIK0	0	Enable	Mask	Interrupt mask register (K10)
					KCP10	0	↓	↑	Input comparison register (K10)
	W	R/W		R	K10	– *2	High	Low	Input port data (K10)
2ECH	R13	R12	R11 / SIOF	R10	R13	0	High/On	Low/Off	Output port (R13)/$\overline{BZ}$ output control
					R12	0	High/On	Low/Off	Output port (R12)/FOUT output control
					R11	0	High	Low	Output port (R11, LAMP)
	R/W		R/W / R	R/W	SIOF		Run	Stop	Output port (SIOF)
					R10	0	High/On	Low/On	Output port (R10)/BZ output control
2F0H	SD3	SD2	SD1	SD0	SD3	× *5			Serial I/F data register (low-order 4 bits)
					SD2	× *5			
					SD1	× *5			
	R/W				SD0	× *5			
2F1H	SD7	SD6	SD5	SD4	SD7	× *5			Serial I/F data register (high-order 4 bits)
					SD6	× *5			
					SD5	× *5			
	R/W				SD4	× *5			
2F2H	SCS1	SCS0	SE2	EISIO	SCS1	1			Serial I/F clock mode selection [SCS1, 0]: 0 Clock, 1 CLK, 2 CLK/2, 3 CLK/4, Slave
					SCS0	1			
					SE2	0	↑	↓	Serial I/F clock edge selection
	R/W				EISIO	0	Enable	Mask	Interrupt mask register (serial I/F)
2F3H	0	0	IK2	ISIO	0 *3	– *2	–	–	Unused
					0 *3	– *2	–	–	Unused
	R				IK2 *4	0	Yes	No	Interrupt factor flag (K20–K23)
					ISIO *4	0	Yes	No	Interrupt factor flag (serial I/F)

*1 Initial value at initial reset
*2 Not set in the circuit
*3 Always "0" being read
*4 Reset (0) immediately after being read
*5 Undefined

SD0–SD3, SD4–SD7: Serial interface data registers (2F0H, 2F1H)

These registers are used for writing and reading serial data.

During writing operation

When "1" is written : High level
When "0" is written : Low level

Writes serial data will be output to SOUT terminal. From the SOUT terminal, the data converted to serial data as high (V_{DD}) level bit for bits set at "1" and as low (V_{SS}) level bit for bits set at "0".

During reading operation

When "1" is read out : High level
When "0" is read out : Low level

The serial data input from the SIN terminal can be read by this register.
The data converted to parallel data, as high (V_{DD}) level bit "1" and as low (V_{SS}) level bit "0" input from SIN terminal. Perform data reading only while the serial interface is halted (i.e., the synchronous clock is neither being input or output).

At initial reset, these registers will be undefined.

SCS1, SCS0: Clock mode selection register (2F2H•D3, D2)

Selects the synchronous clock for the serial interface (SCLK).

Table 4.7.5.2 Synchronous clock selection

SCS1	SCS0	Mode	Synchronous clock
0	0	Master mode	CLK
0	1		CLK/2
1	0		CLK/4
1	1	Slave mode	External clock

CLK: CPU system clock

Synchronous clock (SCLK) is selected from among the above 4 types: 3 types of internal clock and external clock.
At initial reset, external clock is selected.

SE2: Clock edge selection register (2F2H•D1)

Selects the timing for reading in the serial data input.

When "1" is written : Rising edge of SCLK
When "0" is written : Falling edge of SCLK
Read-out : Valid

Selects whether the fetching for the serial input data to registers (SD0–SD7) at the rising edge (at "1" writing) or falling edge (at "0" writing) of the SCLK signal.
Pay attention if the synchtonous clock goes into reverse phase (SCLK → $\overline{\text{SCLK}}$) through the mask option.

SCLK rising = $\overline{\text{SCLK}}$ falling, SCLK falling = $\overline{\text{SCLK}}$ rising

When the internal clock is selected as the synchronous clock (SCLK), a hazard occurs in the synchronous clock (SCLK) when data is written to register SE2.
The input data fetching timing may be selected but output timing for output data is fixed at SCLK rising edge.
At initial reset, falling edge of SCLK (SE2 = "0") is selected.

EISIO: Interrupt mask register (2F2H•D0)

This is the interrupt mask register of the serial interface.

When "1" is written : Enabled
When "0" is written : Masked
Read-out : Valid

At initial reset, this register is set to "0" (mask).

ISIO: Interrupt factor flag (2F3H•D0)

This is the interrupt factor flag of the serial interface.

When "1" is read out : Interrupt has occurred
When "0" is read out : Interrupt has not occurred
Writing : Invalid

From the status of this flag, the software can decide whether the serial interface interrupt.
The interrupt factor flag is reset when it has been read out.
Note, however, that even if the interrupt is masked, this flag will be set to "1" after the 8 bits data input/output.
Be sure that the interrupt factor flag reading is done with the interrupt in the DI status (interrupt flag = "0").
At initial reset, this flag is set to "0".

SCTRG: Clock trigger (2E7H•D3)

This is a trigger to start input/output of synchronous clock.

When "1" is written : Trigger
When "0" is written : No operation
Read-out : Always "0"

When this trigger is supplied to the serial interface activating circuit, the synchronous clock (SCLK) input/output is started.
As a trigger condition, it is required that data writing or reading on data registers SD0–SD7 be performed prior to writing "1" to SCTRG. (The internal circuit of the serial interface is initiated through data writing/reading on data registers SD0–SD7.)
Supply trigger only once every time the serial interface is placed in the RUN state. Refrain from perfoming trigger input multiple times, as leads to malfunctioning.
Moreover, when the synchronous clock SCLK is external clock, start to input the external clock after the trigger.

SIOF (R11): Serial interface status (2ECH•D1)

Indicates the running status of the serial interface.

When "1" is read out : RUN status
When "0" is read out : STOP status
Writing : Invalid

The RUN status is indicated from immediatery after "1" is written to SCTRG bit through to the end of serial data input/output.

4.7.6 Programming notes

(1) If the bit data of SE2 changes while SCLK is in the master mode, a hazard will be output to the SCLK pin. If this poses a problem for the system, be sure to set the SCLK to the external clock if the bit data of SE2 is to be changed.

(2) Be sure that read-out of the interrupt factor flag (ISIO) is done only when the serial port is in the STOP status (SIOF = "0") and the DI status (interrupt flag = "0"). If read-out is performed while the serial data is in the RUN status (during input or output), the data input or output will be suspended and the initial status resumed. Read-out during the EI status (interrupt flag = "1") causes malfunctioning.

(3) When using the serial interface in the master mode, the synchronous clock uses the CPU system clock. Accordingly, do not change the system clock ($f_{OSC1} \leftrightarrow f_{OSC3}$) while the serial interface is operating.

(4) Perform data writing/reading to data registers SD0–SD7 only while the serial interface is halted (i.e., the synchronous clock is neither being input or output).

(5) As a trigger condition, it is required that data writing or reading on data registers SD0–SD7 be performed prior to writing "1" to SCTRG. (The internal circuit of the serial interface is initiated through data writing/reading on data registers SD0–SD7.) Supply trigger only once every time the serial interface is placed in the RUN state. Moreover, when the synchronous clock SCLK is external clock, start to input the external clock after the trigger.

(6) Be sure that writing to the interrupt mask register is done only in the DI status (interrupt flag = "0"). Writing to the interrupt mask register while in the EI status (interrupt flag = "1") may cause malfunction.

4.8 LCD Driver (COM0–COM3, SEG0–SEG47)

4.8.1 Configuration of LCD driver

The E0C6008 Series has four common terminals and 48 (SEG0–SEG47) segment terminals, so that an LCD with a maximum of 192 (48 × 4) segments can be driven. The power for driving the LCD is generated by the internal circuit, so there is no need to supply power externally.
The driving method is 1/4 duty (or 1/3, 1/2 duty is selectable by mask option) dynamic drive, adopting the four types of potential (1/3 bias), V_{DD}, V_{L1}, V_{L2} and V_{L3}. Moreover, the 1/2 bias dynamic drive that uses three types of potential, V_{DD}, V_{L1} = V_{L2} and V_{L3}, can be selected by setting the mask option (drive duty can also be selected from 1/4, 1/3 or 1/2).
1/2 bias drive is effective when the LCD system voltage regulator is not used. The V_{L1} terminal and the V_{L2} terminal should be connected outside the IC.
The frame frequency is 32 Hz for 1/4 duty and 1/2 duty, and 42.7 Hz for 1/3 duty (in the case of f_{OSC1} = 32.768 kHz).
Figures 4.8.1.1 to 4.8.1.6 show the drive waveform for each duty and bias.

Notes: • *"f_{OSC1}" indicates the oscillation frequency of the oscillation circuit.*

- *If there is any segment pad that is set to be DC type, the internal LCD voltage regulator cannot be chosen in all models. Or, if the internal LCD voltage regulator is chosen in any model, the segment pad cannot be set to be DC type.*

Table 4.8.1.1 LCD voltage regulator and DC output from SEG terminals

LCD system voltage regulator	DC output from SEG terminals
Use	Not available
Not use	Available

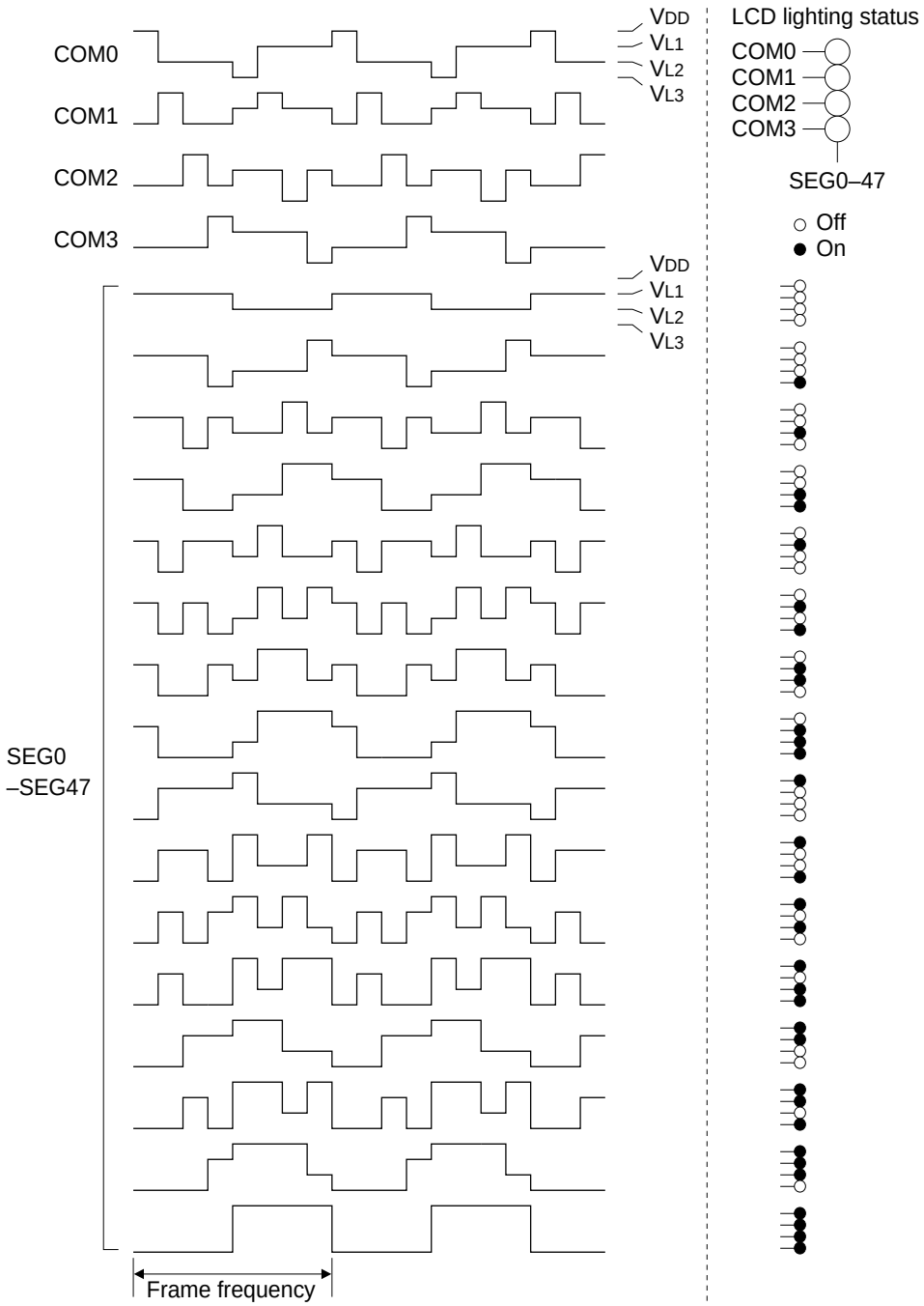


Fig. 4.8.1.1 Drive waveform for 1/4 duty (1/3 bias)

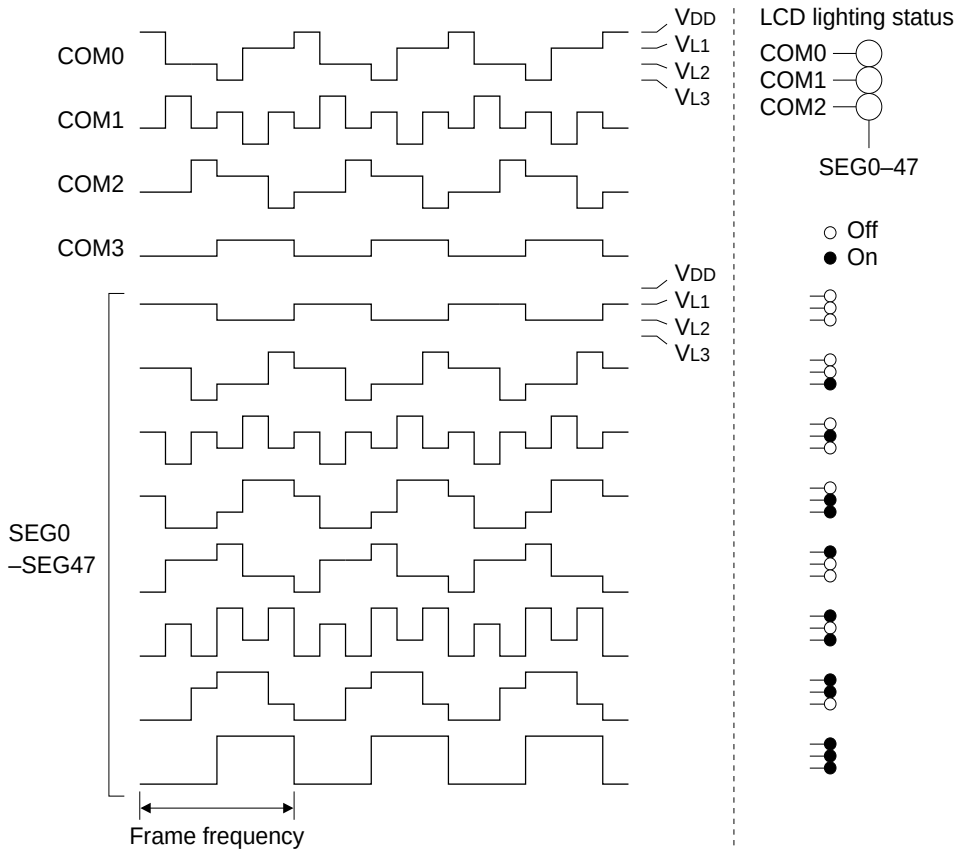


Fig. 4.8.1.2 Drive waveform for 1/3 duty (1/3 bias)

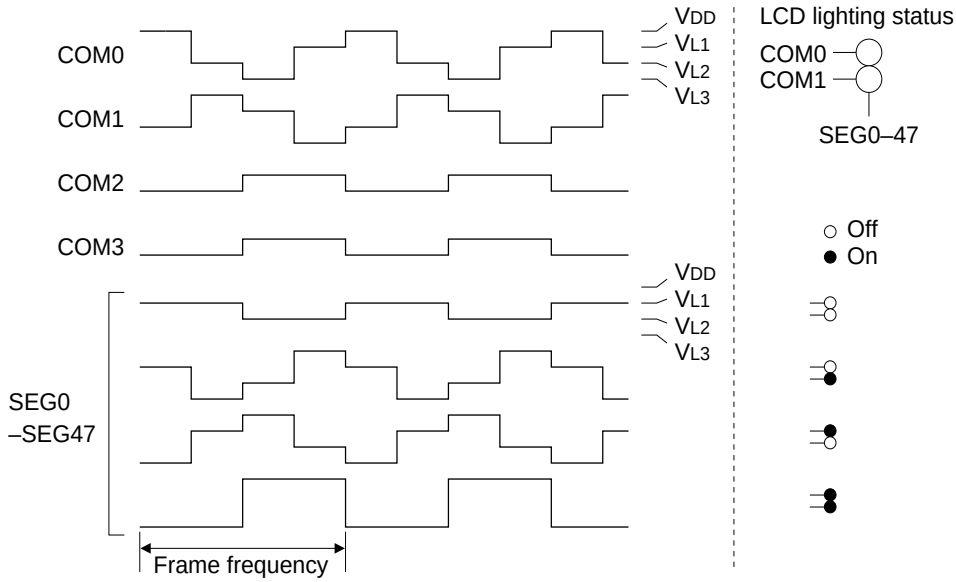


Fig. 4.8.1.3 Drive waveform for 1/2 duty (1/3 bias)

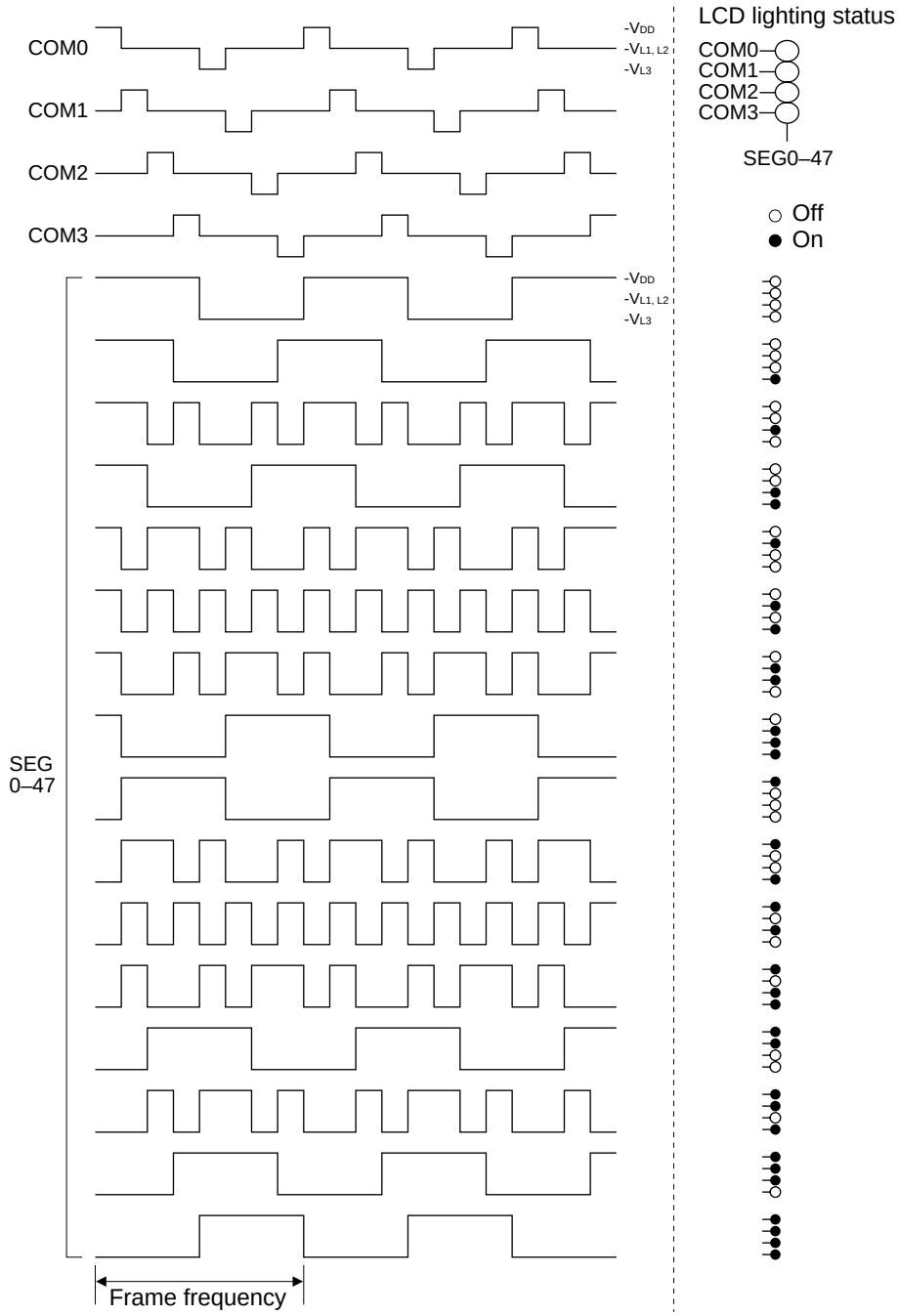


Fig. 4.8.1.4 Drive waveform for 1/4 duty (1/2 bias)

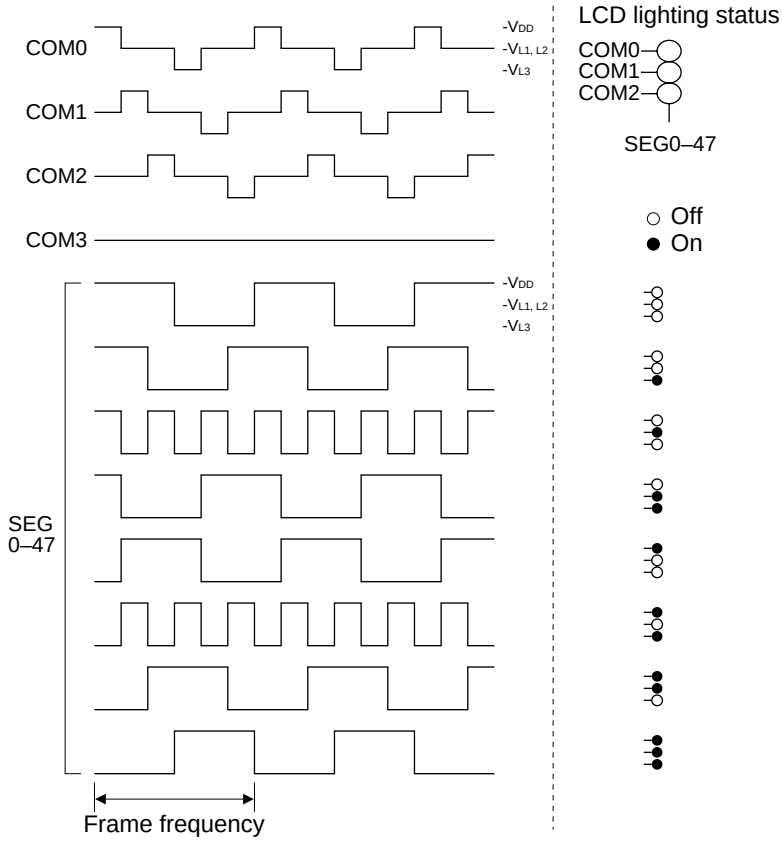


Fig. 4.8.1.5 Drive waveform for 1/3 duty (1/2 bias)

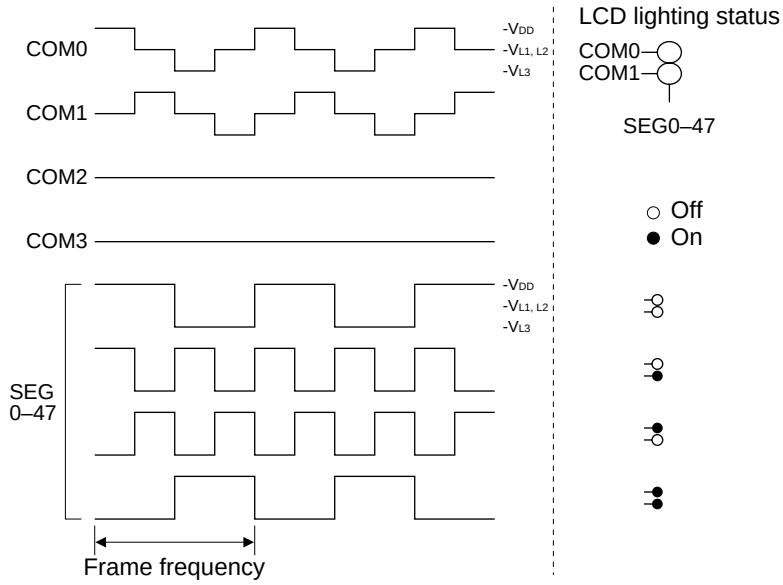


Fig. 4.8.1.6 Drive waveform for 1/2 duty (1/2 bias)

4.8.2 Cadence adjustment of oscillation frequency

In the E0C6008 Series, the LCD drive duty can be set to 1/1 duty by software. This function enables easy adjustment (cadence adjustment) of the oscillation frequency of the oscillation circuit.
The procedure to set to 1/1 duty drive is as follows:

① Write "1" to the CSDC register at address 2E8H•D3.

② Write the same value to all registers corresponding to COMs 0 through 3 of the display memory.

The frame frequency is 32 Hz (f_{OSC1}/1,024, when f_{OSC1} = 32.768 kHz).

Notes:
- *Even when l/3 or 1/2 duty is selected by the mask option, the display data corresponding to all COM are valid during 1/1 duty driving. Hence, for 1/1 duty drive, set the same value for all display memory corresponding to COMs 0 through 3.*
- *For cadence adjustment, set the display data corresponding to COMs 0 through 3, so that all the LCD segments go on.*

Figures 4.8.2.1 and 4.8.2.2 show the 1/1 duty drive waveform in 1/3 bias and 1/2 bias driving.

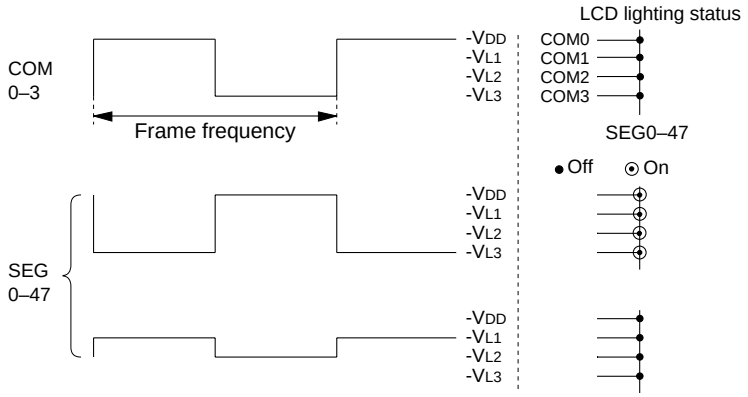


Fig. 4.8.2.1 Drive waveform for 1/1 duty (1/3 bias)

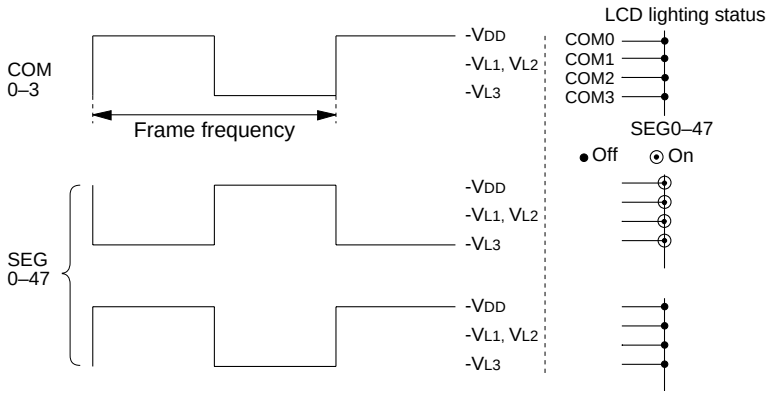


Fig. 4.8.2.2 Drive waveform for 1/1 duty (1/2 bias)

4.8.3 Mask option (segment allocation)

(1) Segment allocation

As shown in Figure 4.1.2, segment data of the E0C6008 Series is decided depending on display data written to the display memory at address 040H–06FH (Page 0) or 240H–26FH (Page 2).

- The mask option enables the display memory to be allocated entirely to either Page 0 or Page 2.
- The address and bits of the display memory can be made to correspond to the segment terminals (SEG0–SEG47) in any form through the mask option. This makes design easy by increasing the degree of freedom with which the liquid crystal panel can be designed.

Figure 4.8.3.1 shows an example of the relationship between the LCD segments (on the panel) and the display memory (when page 0 is selected) for the case of 1/3 duty.

Address	Data			
	D3	D2	D1	D0
09AH	d	c	b	a
09BH	p	g	f	e
09CH	d'	c'	b'	a'
09DH	p'	g'	f'	e'

Display data memory allocation

	Common 0	Common 1	Common 2
SEG10	9A, D0 (a)	9B, D1 (f)	9B, D0 (e)
SEG11	9A, D1 (b)	9B, D2 (g)	9A, D3 (d)
SEG12	9D, D1 (f')	9A, D2 (c)	9B, D3 (p)

Pin address allocation

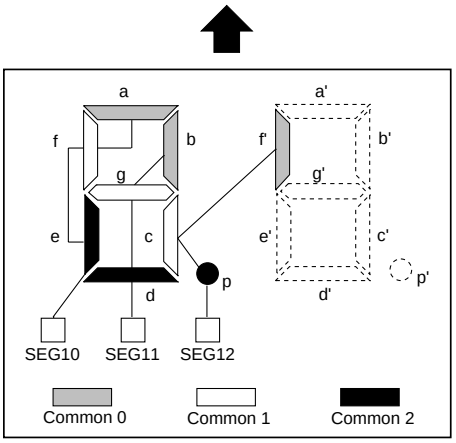


Fig. 4.8.3.1 Segment allocation

(2) Drive duty

According to the mask option, either 1/4, 1/3 or 1/2 duty can be selected as the LCD drive duty. Table 4.8.3.1 shows the differences in the number of segments according to the selected duty.

Table 4.8.3.1 Differences according to selected duty

Duty	COM used	Max. number of segments	Frame frequency *
1/4	COM0–COM3	192 (48 × 4)	fOSC1/1,024 (32 Hz)
1/3	COM0–COM2	144 (48 × 3)	fOSC1/768 (42.7 Hz)
1/2	COM0–COM1	96 (48 × 2)	fOSC1/1,024 (32 Hz)

* When fOSC1 = 32 kHz

(3) Output specification

- The segment terminals (SEG0–SEG47) are selected by mask option in pairs for either segment signal output or DC output (V_{DD} and V_{SS} binary output). When DC output is selected, the data corresponding to COM0 of each segment terminal is output.
- When DC output is selected, either complementary output or Pch open drain output can be selected for each terminal by mask option.

Note: The terminal pairs are the combination of SEG (2∗n) and SEG (2∗n + 1) (where n is an integer from 0 to 23).

(4) Drive bias

For the drive bias of the E0C6008 or the E0C60L08, either 1/3 bias or 1/2 bias can be selected by the mask option. When using the LCD system voltage regulator, it is fixed at 1/3 bias.

4.8.4 Control of LCD driver

Table 4.8.4.1 shows the LCD driver's control bits and their addresses. Figure 4.8.4.1 shows the display memory map.

Table 4.8.4.1 Control bits of LCD driver

Address	Register D3	D2	D1	D0	Name	Init ∗1	1	0	Comment
2D0H	0	0	0	LOF	0 ∗3	– ∗2	–	–	Unused
					0 ∗3	– ∗2	–	–	Unused
	R			R/W	0 ∗3	– ∗2	–	–	Unused
					LOF	1	Normal	All off	LCD all off control
2E8H	CSDC	ETI2	ETI8	ETI32	CSDC	0	Static	Dynamic	LCD drive switch
					ETI2	0	Enable	Mask	Interrupt mask register (clock timer 2 Hz)
	R/W				ETI8	0	Enable	Mask	Interrupt mask register (clock timer 8 Hz)
					ETI32	0	Enable	Mask	Interrupt mask register (clock timer 32 Hz)

∗1 Initial value at initial reset
∗2 Not set in the circuit
∗3 Always "0" being read
∗4 Reset (0) immediately after being read
∗5 Undefined

Address Page	Low / High	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0 or 2	4	Display memory (48 words × 4 bits) Page 0: R/W, Page 2: W only															
	5																
	6																

Fig. 4.8.4.1 Display memory map

LOF: LCD all Off control (2D0H•D0)

Controls the LCD display.

When "1" is written : LCD displayed
When "0" is written : LCD is all off
Read-out : Valid

By writing "0" to the LOF register, all the LCD dots goes off, and when "1" is written, it returns to normal display.
Writing "0" outputs an off waveform to the SEG terminals, and does not affect the content of the display memory.
After an initial reset, LOF is set to "1".

CSDC: LCD drive switch (2E8H•D3)

The LCD drive format can be selected with this switch.

When "1" is written : Static drive
When "0" is written : Dynamic drive
Read-out : Valid

At initial reset, dynamic drive (CSDC = "0") is selected.

Display memory (040H–06FH or 240H–26FH)

The LCD segments are lit or turned off depending on this data.

When "1" is written : Lit
When "0" is written : Not lit
Read-out : Valid for Page 0
Undefined Page 2

By writing data into the display memory allocated to the LCD segment (on the panel), the segment can be lit or put out.
At initial reset, the contents of the display memory are undefined.

4.8.5 Programming notes

(1) When Page 0 is selected for the display memory, the memory data and the display will not match until the area is initialized (through, for instance, memory clear processing by the CPU). Initialize the display memory by executing initial processing.

(2) When Page 2 is selected for the display memory, that area becomes write-only. Consequently, data cannot be rewritten by arithmetic operations (such as AND, OR, ADD, SUB).

4.9 Clock Timer

4.9.1 Configuration of clock timer

The E0C6008 Series has a built-in clock timer as the source oscillator for prescaler. The clock timer is configured of a seven-bit binary counter that serves as the input clock, a 256 Hz signal output by the prescaler. Data of the four high-order bits (16 Hz–2 Hz) can be read out by the software.
Figure 4.9.1.1 is the block diagram for the clock timer.

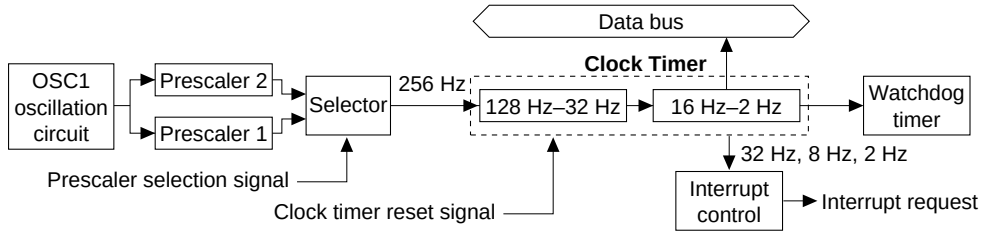


Fig. 4.9.1.1 Clock timer block diagram

Ordinarily, this clock timer is used for all types of timing functions such as clocks.
The input clock of the clock timer is output through the prescaler, so the prescaler mode must be set correctly to suit the crystal oscillator to be used (32.768 kHz or 38.4 kHz). For how to set the prescaler, see Section 4.3, "Oscillation Circuit and Prescaler".

4.9.2 Interrupt function

The clock timer can cause interrupts at the falling edge of 32 Hz, 8 Hz and 2 Hz signals. Software can set whether to mask any of these frequencies.
Figure 4.9.2.1 is the timing chart of the clock timer.

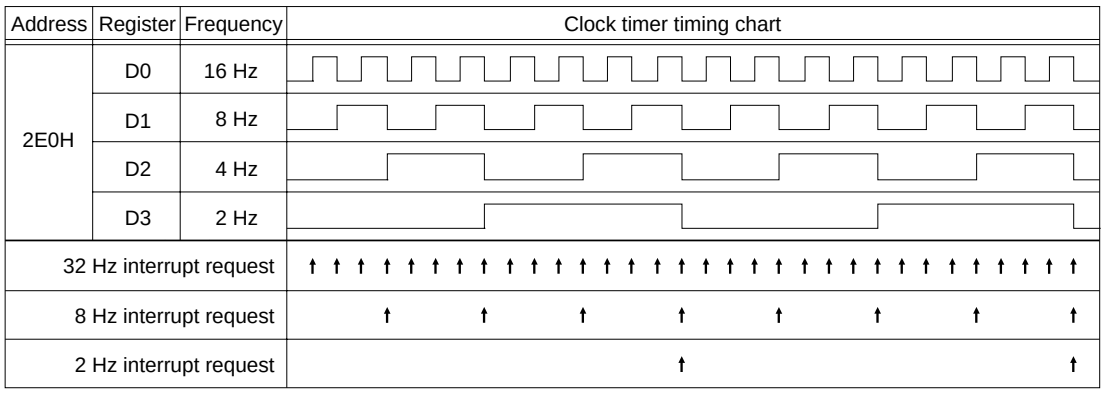


Fig. 4.9.2.1 Clock timer timing chart

As shown in Figure 4.9.2.1, interrupt is generated at the falling edge of the frequencies (32 Hz, 8 Hz , 2 Hz). At this time, the corresponding interrupt factor flag (TI32, TI8, TI2) is set to "1". Selection of whether to mask the separate interrupts can be made with the interrupt mask registers (ETI32, ETI8, ETI2). However, regardless of the interrupt mask register setting, the interrupt factor flag is set to "1" at the falling edge of the corresponding signal.

4.9.3 Control of clock timer

Table 4.9.3.1 shows the clock timer control bits and their addresses.

Table 4.9.3.1 Control bits of clock timer

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
2E0H	TM3	TM2	TM1	TM0	TM3	0			Clock timer data (2 Hz)
					TM2	0			Clock timer data (4 Hz)
	R				TM1	0			Clock timer data (8 Hz)
					TM0	0			Clock timer data (16 Hz)
2E8H	CSDC	ETI2	ETI8	ETI32	CSDC	0	Static	Dynamic	LCD drive switch
					ETI2	0	Enable	Mask	Interrupt mask register (clock timer 2 Hz)
	R/W				ETI8	0	Enable	Mask	Interrupt mask register (clock timer 8 Hz)
					ETI32	0	Enable	Mask	Interrupt mask register (clock timer 32 Hz)
2E9H	0	TI2	TI8	TI32	0 *3	– *2	–	–	Unused
					TI2 *4	0	Yes	No	Interrupt factor flag (clock timer 2 Hz)
	R				TI8 *4	0	Yes	No	Interrupt factor flag (clock timer 8 Hz)
					TI32 *4	0	Yes	No	Interrupt factor flag (clock timer 32 Hz)
2EEH	TMRST	SWRUN	SWRST	IOC0	TMRST*3	Reset	Reset	–	Clock timer reset
					SWRUN	0	Run	Stop	Stopwatch timer Run/Stop
	W	R/W	W	R/W	SWRST*3	Reset	Reset	–	Stopwatch timer reset
					IOC0	0	Output	Input	I/O control register 0 (P00–P03)

*1 Initial value at initial reset
*2 Not set in the circuit
*3 Always "0" being read
*4 Reset (0) immediately after being read
*5 Undefined

TM0–TM3: Timer data (2E0H)

The 16 Hz–2 Hz timer data of the clock timer can be read out with this register. These four bits are read-out only, and writing operations are invalid.
At initial reset, the timer data is initialized to "0H".

ETI32, ETI8, ETI2: Interrupt mask registers (2E8H•D0–D2)

These registers are used to select whether to mask the clock timer interrupt.

When "1" is written : Enabled
When "0" is written : Masked
Read-out : Valid

The interrupt mask registers (ETI32, ETI8, ETI2) are used to select whether to mask the interrupt to the separate frequencies (32 Hz, 8 Hz, 2 Hz).
Writing to the interrupt mask registers can be done only in the DI status (interrupt flag = "0").
At initial reset, these registers are all set to "0".

TI32, TI8, TI2: Interrupt factor flags (2E9H•D0–D2)

These flags indicate the status of the clock timer interrupt.

When "1" is read out : Interrupt has occurred
When "0" is read out : Interrupt has not occurred
Writing : Invalid

The interrupt factor flags (TI32, TI8, TI2) correspond to the clock timer interrupts of the respective frequencies (32 Hz, 8 Hz, 2 Hz). The software can judge from these flags whether there is a clock timer interrupt. However, even if the interrupt is masked, the flags are set to "1" at the falling edge of the signal.
These flags can be reset through being read out by the software. Also, the flags can be read out only in the DI status (interrupt flag = "0").
At initial reset, these flags are set to "0".

TMRST: Clock timer reset (2EEH•D3)

This bit resets the clock timer.

When "1" is written : Clock timer reset
When "0" is written : No operation
Read-out : Always "0"

The clock timer is reset by writing "1" to TMRST. The clock timer starts immediately after this. No operation results when "0" is written to TMRST.
This bit is write-only, and so is always "0" at read-out.

4.9.4 Programming notes

(1) The prescaler mode must be set correctly to suit the crystal oscillator to be used.

(2) When the clock timer has been reset, the interrupt factor flag (TI) may sometimes be set to "1". Consequently, perform flag read-out (reset the flag) as necessary at reset.

(3) The input clock of the watchdog timer is the 2 Hz signal of the clock timer, so that the watchdog timer may be counted up at timer reset.

(4) Read-out the interrupt factor flag (TI) only during the DI status (interrupt flag = "0"). Read-out during EI status (interrupt flag = "1") will cause malfunction.

4.10 Stopwatch Timer

4.10.1 Configuration of stopwatch timer

The E0C6008 Series incorporates a 1/100 sec and 1/10 sec stopwatch timer. The stopwatch timer is configured of a two-stage, four-bit BCD counter serving as the input clock of an approximately 100 Hz signal (signal obtained by approximately demultiplying the 256 Hz signal output by the prescaler). Data can be read out four bits at a time by the software.
Figure 4.10.1.1 is the block diagram of the stopwatch timer.

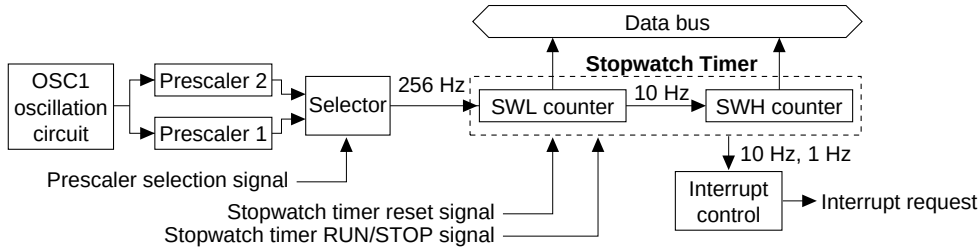


Fig. 4.10.1.1 Stopwatch timer block diagram

The stopwatch timer can be used as a separate timer from the clock timer. In particular, digital watch stopwatch functions can be realized easily with software.
The input clock of the stopwatch timer is output through the prescaler, so the prescaler mode must be set correctly to suit the crystal oscillator to be used (32.768 kHz or 38.4 kHz). For how to set the prescaler, see Section 4.3, "Oscillation Circuit and Prescaler".

4.10.2 Count-up pattern

The stopwatch timer is configured of four-bit BCD counters SWL and SWH.
The counter SWL, at the stage preceding the stopwatch timer, has an approximated 100 Hz signal for the input clock. It counts up every 1/100 sec, and generates an approximated 10 Hz signal. The counter SWH has an approximated 10 Hz signal generated by the counter SWL for the input clock. It count-up every 1/10 sec, and generated 1 Hz signal.
Figure 4.10.2.1 shows the count-up pattern of the stopwatch timer.

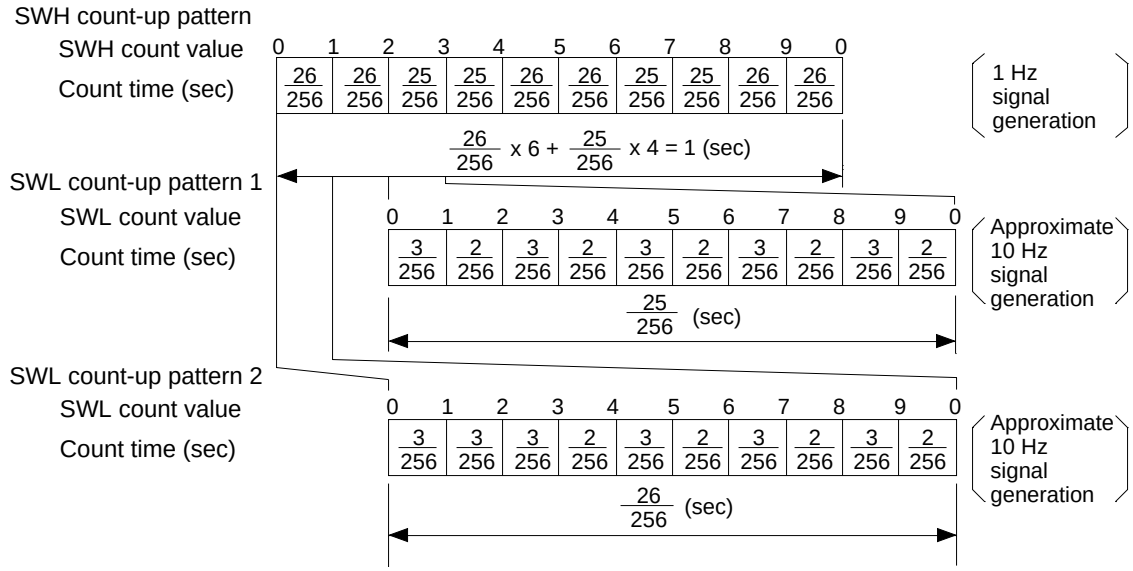


Fig. 4.10.2.1 Count-up pattern of stopwatch timer

SWL generates an approximated 10 Hz signal from the basic 256 Hz signal. The count-up intervals are 2/256 sec and 3/256 sec, so that finally two patterns are generated: 25/256 sec and 26/256 sec intervals. Consequently, these patterns do not amount to an accurate 1/100 sec.
SWH counts the approximated 10 Hz signals generated by the 25/256 sec and 26/256 sec intervals in the ratio of 4:6, to generate a 1 Hz signal. The count-up intervals are 25/256 sec and 26/256 sec, which do not amount to an accurate 1/10 sec.

4.10.3 Interrupt function

The 10 Hz (approximate 10 Hz) and 1 Hz interrupts can be generated through the overflow of stopwatch timers SWL and SWH respectively. Also, software can set whether to separately mask the frequencies described earlier.
Figure 4.10.3.1 is the timing chart for the stopwatch timer.

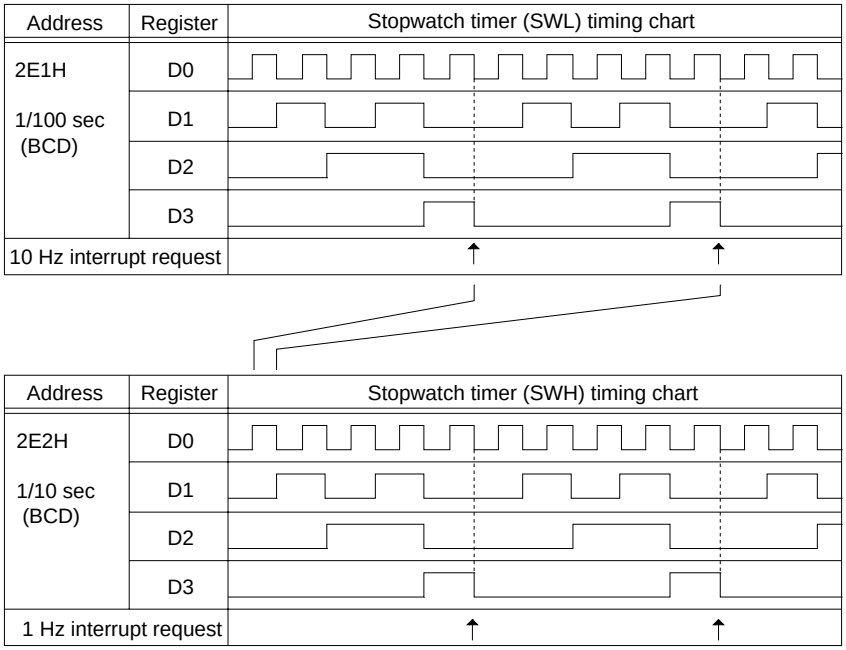


Fig. 4.10.3.1 Stopwatch timer timing chart

As shown in Figure 4.10.3.1, the interrupts are generated by the overflow of their respective counters ("9" changing to "0"). Also, at this time the corresponding interrupt factor flags (SWIT0, SWIT1) are set to "1". The respective interrupts can be masked separately through the interrupt mask registers (EISWIT0, EISWIT1). However, regardless of the setting of the interrupt mask registers, the interrupt factor flags are set to "1" by the overflow of their corresponding counters.

4.10.4 Control of stopwatch timer

Table 4.10.4.1 list the stopwatch timer control bits and their addresses.

Table 4.10.4.1 Control bits of stopwatch timer

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
2E1H	SWL3	SWL2	SWL1	SWL0	SWL3	0			MSB
					SWL2	0			
	R				SWL1	0			Stopwatch timer 1/100 sec data (BCD)
					SWL0	0			LSB
2E2H	SWH3	SWH2	SWH1	SWH0	SWH3	0			MSB
					SWH2	0			
	R				SWH1	0			Stopwatch timer 1/10 sec data (BCD)
					SWH0	0			LSB
2E6H	HLMOD	BLD0	EISWIT1	EISWIT0	HLMOD	0	Heavy load	Normal	Heavy load protection mode register
					BLD0	0	Low	Normal	Sub-BLD evaluation data
	R/W	R	R/W		EISWIT1	0	Enable	Mask	Interrupt mask register (stopwatch 1 Hz)
					EISWIT0	0	Enable	Mask	Interrupt mask register (stopwatch 10 Hz)
2EAH	IK1	IK0	SWIT1	SWIT0	IK1 *4	0	Yes	No	Interrupt factor flag (K10)
					IK0 *4	0	Yes	No	Interrupt factor flag (K00–K03)
	R				SWIT1 *4	0	Yes	No	Interrupt factor flag (stopwatch 1 Hz)
					SWIT0 *4	0	Yes	No	Interrupt factor flag (stopwatch 10 Hz)
2EEH	TMRST	SWRUN	SWRST	IOC0	TMRST*3	Reset	Reset	–	Clock timer reset
					SWRUN	0	Run	Stop	Stopwatch timer Run/Stop
	W	R/W	W	R/W	SWRST*3	Reset	Reset	–	Stopwatch timer reset
					IOC0	0	Output	Input	I/O control register 0 (P00–P03)

*1 Initial value at initial reset
*2 Not set in the circuit
*3 Always "0" being read
*4 Reset (0) immediately after being read
*5 Undefined

SWL0–SWL3: Stopwatch timer 1/100 sec (2E1H)

Data (BCD) of the 1/100 sec column of the stopwatch timer can be read out. These four bits are read-only, and cannot be used for writing operations.
At initial reset, the timer data is set to "0H".

SWH0–SWH3: Stopwatch timer 1/10 sec (2E2H)

Data (BCD) of the 1/10 sec column of the stopwatch timer can be read out. These four bits are read-only, and cannot be used for writing operations.
At initial reset, the timer data is set to "0H".

EISWIT0, EISWIT1: Interrupt mask registers (2E6H•D0 and D1)

These registers are used to select whether to mask the stopwatch timer interrupt.

When "1" is written : Enabled
When "0" is written : Masked
Read-out : Valid

The interrupt mask registers (EISWIT0, EISWIT1) are used to separately select whether to mask the 10 Hz and 1 Hz interrupts.
At initial reset, these registers are both set to "0".

SWIT0, SWIT1: Interrupt factor flags (2EAH•D0 and D1)

These flags indicate the status of the stopwatch timer interrupt.

When "1" is read out : Interrupt has occurred
When "0" is read out : Interrupt has not occurred
Writing : Invalid

The interrupt factor flags (SWIT0, SWIT1) correspond to the 10 Hz and 1 Hz interrupts respectively. With these flags, the software can judge whether a stopwatch timer interrupt has occurred. However, regardless of the interrupt mask register setting, these flags are set to "1" by the counter overflow.
These flags are reset when read out by the software. Also, read-out is only possible in the DI status (interrupt flag = "0").
At initial reset, these flags are set to "0".

SWRST: Stopwatch timer reset (2EEH•D1)

This bit resets the stopwatch timer.

When "1" is written : Stopwatch timer reset
When "0" is written : No operation
Read-out : Always "0"

The stopwatch timer is reset when "1" is written to SWRST. When the stopwatch timer is reset in the RUN status, operation restarts immediately. Also, in the STOP status the reset data is maintained.
This bit is write-only, and is always "0" at read-out.

SWRUN: Stopwatch timer RUN/STOP (2EEH•D2)

This bit controls RUN/STOP of the stopwatch timer.

When "1" is written : RUN
When "0" is written : STOP
Read-out : Valid

The stopwatch timer enters the RUN status when "1" is written to SWRUN, and the STOP status when "0" is written.
In the STOP status, the timer data is maintained until the next RUN status or resets timer. Also, when the STOP status changes to the RUN status, the data that was maintained can be used for resuming the count.
When the timer data is read out in the RUN status, correct read-out may be impossible because of the carry from the low-order bit (SWL) to the high-order bit (SWH). This occurs when read-out has extended over the SWL and SWH bits when the carry occurs. To prevent this, perform read out after entering the STOP status, and then return to the RUN status. Also, the duration of the STOP status must be within 976 µsec (256 Hz 1/4 cycle).
At initial reset, this register is set to "0".

4.10.5 Programming notes

(1) The prescaler mode must be set correctly so that the stopwatch timer suits the crystal oscillator to be used.

(2) If timer data is read out in the RUN status, the timer must be made into the STOP status, and after data is read out the RUN status can be restored. If data is read out when a carry occurs, the data cannot be read correctly.
Also, the processing above must be performed within the STOP interval of 976 µsec (256 Hz 1/4 cycle).

(3) Read-out of the interrupt factor flag (SWIT) must be done only in the DI status (interrupt flag = "0"). Read-out during EI status (interrupt flag = "1") will cause malfunction.

4.11 Sound Generator

4.11.1 Configuration of sound generator

The E0C6008 Series outputs buzzer signals (BZ, $\overline{BZ}$) to drive the piezoelectric buzzer.
The frequency of the buzzer signal is software-selectable from eight kinds of demultiplied fOSC1. Further, a digital envelope can be added to the buzzer signal through duty ratio control.
Figure 4.11.1.1 shows the sound generator configuration. Figure 4.11.1.2 shows the sound generator timing chart.

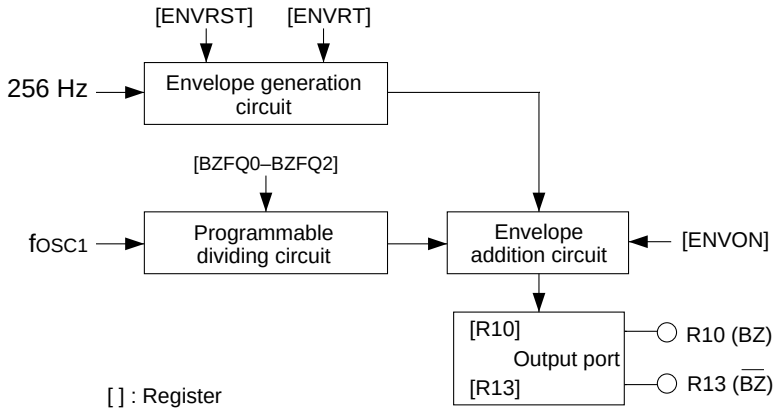


Fig. 4.11.1.1 Configuration of sound generator

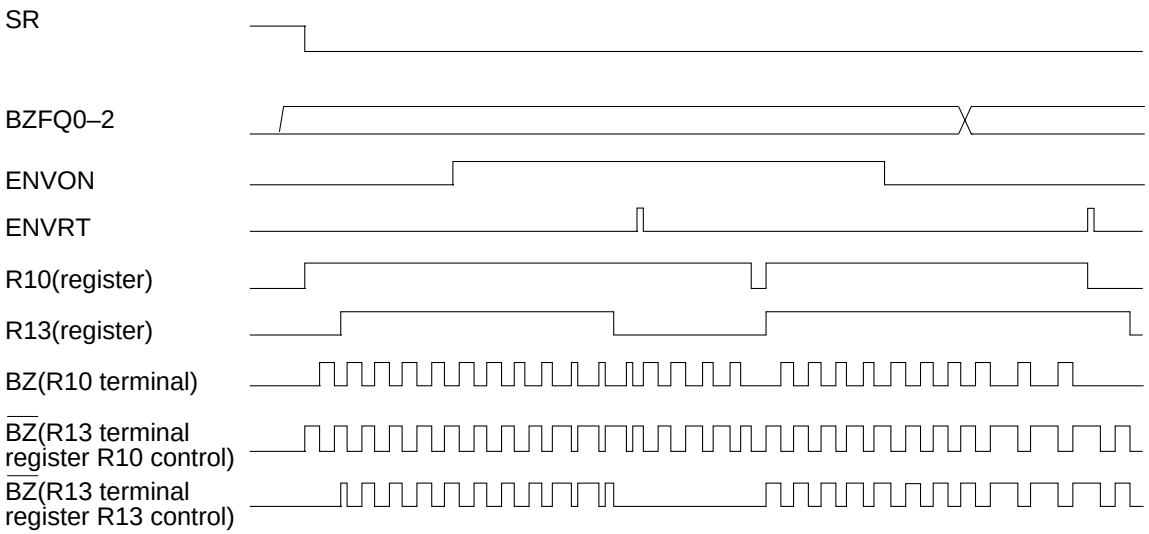


Fig. 4.11.1.2 Timing chart of sound generator

4.11.2 Frequency setting

The frequencies of the buzzer signals (BZ, $\overline{BZ}$) are set by writing data to registers BZFQ0–BZFQ2. Table 4.11.2.1 lists the register setting values and the frequencies that can be set.

Table 4.11.2.1 Setting of frequencies of buzzer signals

BZFQ			Buzzer frequency (Hz)		
2	1	0	Demultiplier ratio	When fosc1 = 32 kHz	When fosc1 = 38.4 kHz
0	0	0	fosc1/8	4,096.0	4,800.0
0	0	1	fosc1/10	3,276.8	3,840.0
0	1	0	fosc1/12	2,730.7	3,200.0
0	1	1	fosc1/14	2,340.6	2,742.9
1	0	0	fosc1/16	2,048.0	2,400.0
1	0	1	fosc1/20	1,638.4	1,920.0
1	1	0	fosc1/24	1,365.3	1,600.0
1	1	1	fosc1/28	1,170.3	1,371.4

Note: A hazard may be observed in the output waveform of the BZ and $\overline{BZ}$ signals when data of the buzzer frequency selection registers (BZFQ0–BZFQ2) changes.

4.11.3 Digital envelope

A duty ratio control data envelope (with duty ratio change in eight stages) can be added to the buzzer signal (BZ, $\overline{BZ}$).

The duty ratio is the ratio of the pulse width compared with the pulse cycle. The BZ output is TH/ (TH+TL) when the high level output is TH and the low level output is TL. The $\overline{BZ}$ output (BZ inverted output) is TL/ (TH+TL). Also, care must be taken because the duty ratio differs depending on the buzzer frequency.

The envelope is added by writing "1" to register ENVON. If "0" is written the duty ratio is fixed to the maximum. Also, if the envelope is added, the duty ratio is reverted to the maximum by writing "1" in register ENVRST, and the duty ratio also becomes the maximum at the start of the buzzer signal output.

The decay time of the envelope (time for the duty ratio to change) can be selected with the register ENVRT. This time is 62.5 msec (16 Hz) when "0" is written, and 125 msec (8 Hz) when "1" is written. However, a maximum difference of 4 msec is taken from envelope-ON until the first change.

Table 4.11.3.1 lists the duty rates and buzzer frequencies. Figure 4.11.3.1 shows the digital envelope timing chart.

Table 4.11.3.1 Duty rates and buzzer frequencies

BZFQ (register) / Duty rate	2	0	1	0	1	0	1	0	1
	1	0	0	0	0	1	1	1	1
	0	0	0	1	1	0	0	1	1
Level 1 (max.)		8/16		8/20		12/24		12/28	
Level 2		7/16		7/20		11/24		11/28	
Level 3		6/16		6/20		10/24		10/28	
Level 4		5/16		5/20		9/24		9/28	
Level 5		4/16		4/20		8/24		8/28	
Level 6		3/16		3/20		7/24		7/28	
Level 7		2/16		2/20		6/24		6/28	
Level 8 (min.)		1/16		1/20		5/24		5/28	

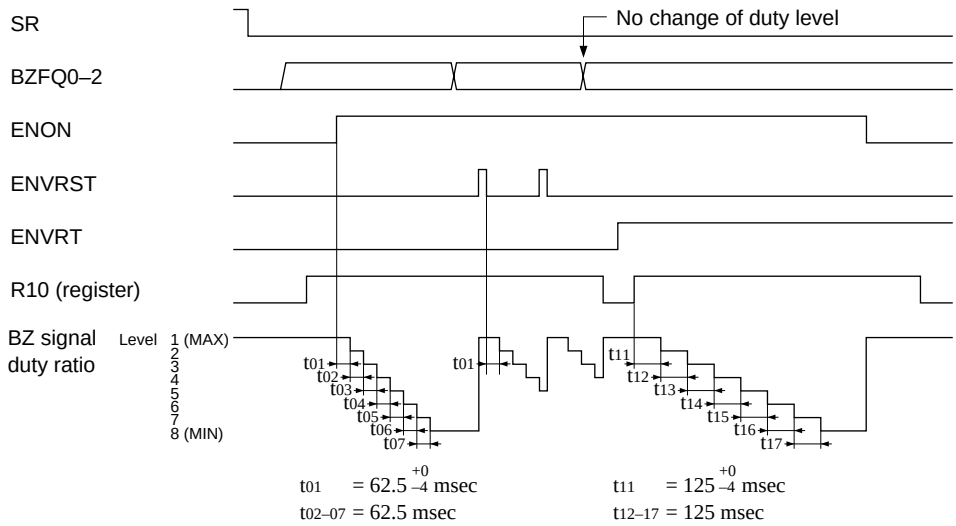


Fig. 4.11.3.1 Digital envelope timing chart

4.11.4 Mask option

(1) Selection can be made whether to output the BZ signal from the R10 terminal.

(2) Selection can be made whether to output the $\overline{BZ}$ signal from the R13 terminal. However, if the BZ signal is not output the $\overline{BZ}$ signal cannot be output.

(3) Selection can be made to perform the $\overline{BZ}$ signal output control through the R10 register or the R13 register.

See Section 4.5, "Output Ports" for details of the above mask option.

4.11.5 Control of sound generator

Table 4.11.5.1 lists the sound generator's control bits and their addresses.

Table 4.11.5.1 Control bits of sound generator

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
2ECH	R13	R12	R11 / SIOF	R10	R13	0	High/On	Low/Off	Output port (R13)/BZ output control
					R12	0	High/On	Low/Off	Output port (R12)/FOUT output control
	R/W		R/W / R	R/W	R11	0	High	Low	Output port (R11, LAMP)
					SIOF	0	Run	Stop	Output port (SIOF)
					R10	0	High/On	Low/On	Output port (R10)/BZ output control
2F6H	BZFQ2	BZFQ1	BZFQ0	ENVRST	BZFQ2	0			Buzzer frequency selection [BZFQ2–0] 0: fOSC1/8, 1: fOSC1/10, 2: fOSC1/12, 3: fOSC1/14, 4: fOSC1/16, 5: fOSC1/20, 6: fOSC1/24, 7: fOSC1/28
					BZFQ1	0			
	R/W			W	BZFQ0	0			
					ENVRST*3	Reset	Reset	–	Envelope reset
2F7H	ENVON	ENVRT	AMPDT	AMPON	ENVON	0	On	Off	Envelope On/Off
					ENVRT	0	1.0 sec	0.5 sec	Envelope cycle selection register
	R/W		R	R/W	AMPDT	1	+ > -	+ < -	Analog comparator data
					AMPON	0	On	Off	Analog comparator On/Off

*1 Initial value at initial reset
*2 Not set in the circuit
*3 Always "0" being read
*4 Reset (0) immediately after being read
*5 Undefined

BZFQ0–BZFQ2: Buzzer frequency selection register (2F6H•D1–D3)

This is used to select the frequency of the buzzer signal.

Table 4.11.5.2 Buzzer frequency

BZFQ2	BZFQ1	BZFQ0	Buzzer frequency (Hz)
0	0	0	fOSC1/8
0	0	1	fOSC1/10
0	1	0	fOSC1/12
0	1	1	fOSC1/14
1	0	0	fOSC1/16
1	0	1	fOSC1/20
1	1	0	fOSC1/24
1	1	1	fOSC1/28

Buzzer frequency is selected from the above eight types that have been divided by fOSC1 (oscillation frequency of the OSC1 oscillation circuit).
At initial reset, fOSC1/8 (Hz) is selected.

ENVRST: Envelope reset (2F6H•D0)

This is the reset input to make the duty ratio of the buzzer signal the maximum.

When "1" is written : Reset input
When "0" is written : No operation
Read-out : Always "0"

When the envelope is added to the buzzer signal, the duty ratio is made maximum through this reset input. When the envelope is not added or when the buzzer signal is not output, the reset input is invalid.

ENVON: Envelope ON/OFF (2F7H•D3)

This controls adding the envelope to the buzzer signal.

When "1" is written : Envelope added (ON)
When "0" is written : No envelope (OFF)
Read-out : Valid

The envelope is the digital envelope based on duty ratio control. When there is no envelope, the duty ratio is fixed to the maximum.
At initial reset, no envelope (OFF) is selected.

ENVRT: Envelope decay time (2F7H•D2)

This input selects the decay time of the envelope added to the buzzer signal.

When "1" is written : 1.0 sec (125 msec × 7 = 875 msec)
When "0" is written : 0.5 sec (62.5 msec × 7 = 437.5 msec)
Read-out : Valid

The decay time of the digital envelope is decided by the time taken for the duty ratio to change. When "1" is written to ENVRT the time is 125 msec (8 Hz) units, and when "0" is written it is 62.5 msec (16 Hz) units.
At initial reset, 0.5 sec (437.5 msec) is selected.

R10, R13 (at BZ, $\overline{BZ}$ output selection): Special output port data (2ECH•D0, D3)

These control output of the buzzer signals (BZ, $\overline{BZ}$).

When "1" is written : Buzzer signal output
When "0" is written : Low level (DC) output
Read-out : Valid

- ***BZ output under R13 control***

  BZ output and $\overline{BZ}$ output can be controlled independently. BZ output is controlled by writing data to register R10. $\overline{BZ}$ output is controlled by writing data to register R13.

- ***BZ output under R10 control***

  By writing data to register R10 only, BZ output and $\overline{BZ}$ output can be controlled simultaneously. In this case, register R13 can be used as a read/write one-bit general register. This register does not affect $\overline{BZ}$ output (output to pin R13).

At initial reset, R10 and R13 are set to "0".

4.11.6 Programming note

A hazard may be observed in the output waveform of the BZ and $\overline{BZ}$ signals when data of the output registers (R10, R13) and the buzzer frequency selection registers (BZFQ0–BZFQ2) changes.

4.12 Event Counter

4.12.1 Configuration of event counter

The E0C6008 Series has an event counter that counts the clock signals input from outside.
The event counter is configured of a pair of eight-bit binary counters (UP counters). The clock pulses are input through terminals K02 and K03 of the input port.
The clock signals input from the terminals are input to the event counter via the noise rejector.
The event counter detects the phases of the two clock signals. Software selection provides for two modes, the phase detection mode in which one of the counters can be chosen to input the clock signal, and the separate mode in which each clock signal is input to different counters.
Figure 4.12.1.1 shows the configuration of the event counter.

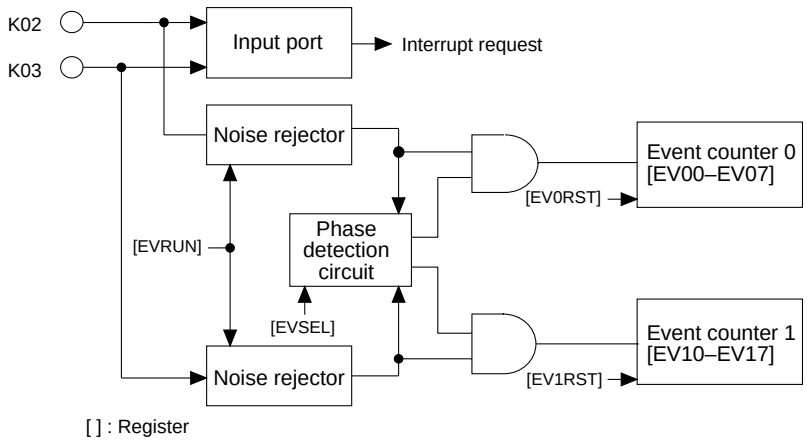
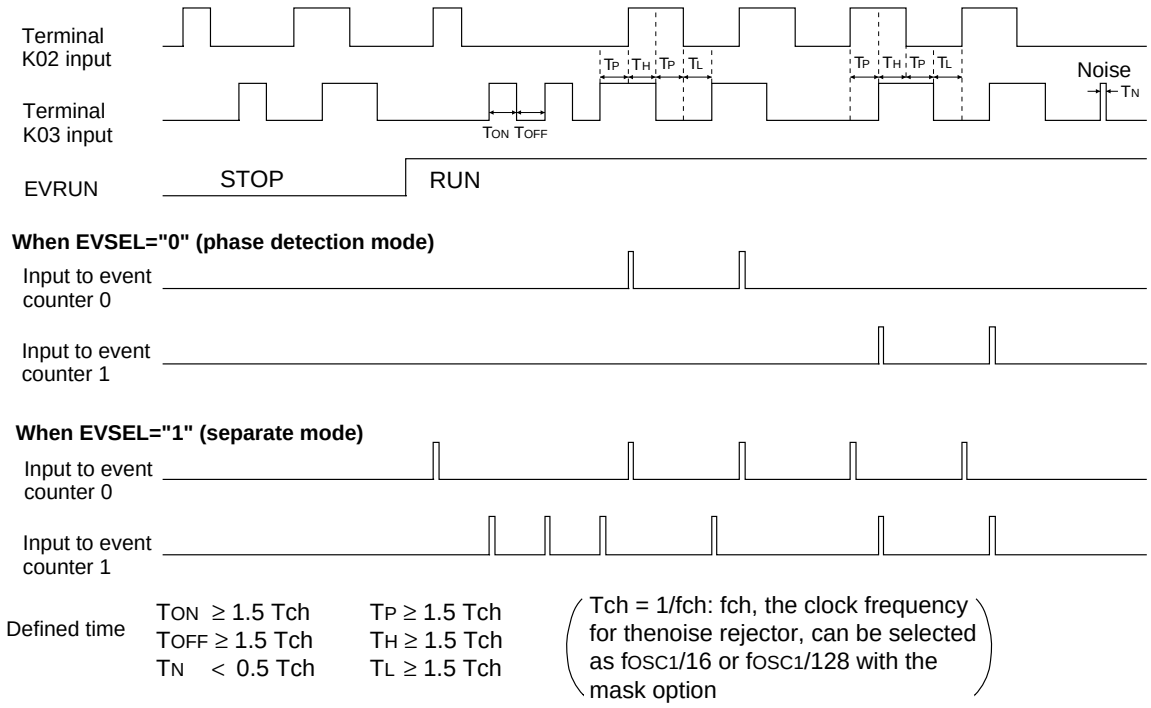


Fig. 4.12.1.1 Configuration of event counter

4.12.2 Switching count mode

The event counter detects the phases of the two clock signals. Software selection provides for two modes, the phase detection mode in which one of the counters can be chosen to input the clock signal, and the separate mode in which each clock signal is input to different counters.
Selection can be made by writing data to the EVSEL register. When "0" is written the phase detection mode is enabled, and when "1" is written the separate mode is enabled.
In the phase detection mode, the clock signals having different phases must be input simultaneously to terminals K02 and K03. When the input from terminal K02 is fast the clock signal is input to event counter 1, and when the input from terminal K03 is fast the clock signal is input to event counter 0.
In the separate mode, input from terminal K02 is made to event counter 0, and input from terminal K03 is made to event counter 1.
Figure 4.12.2.1 is the timing chart for the event counter.



Defined time

$T_{ON} \geq 1.5$ Tch	$T_P \geq 1.5$ Tch
$T_{OFF} \geq 1.5$ Tch	$T_H \geq 1.5$ Tch
$T_N < 0.5$ Tch	$T_L \geq 1.5$ Tch

(Tch = 1/fch: fch, the clock frequency for thenoise rejector, can be selected as $f_{OSC1}/16$ or $f_{OSC1}/128$ with the mask option)

Fig. 4.12.2.1 Event counter timing chart

4.12.3 Mask option

The clock frequency of the noise rejector can be selected as $f_{OSC1}/16$ or $f_{OSC1}/128$. Table 4.12.3.1 lists the defined time depending on the frequency selected.

Table 4.12.3.1 Defined time depending on frequency selected

Selection	f_{OSC1} = 32.768 kHz		f_{OSC1} = 38.400 kHz	
	$f_{OSC1}/16$	$f_{OSC1}/128$	$f_{OSC1}/16$	$f_{OSC1}/128$
T_N	0.24	1.95	0.20	1.66
T_{ON}	0.74	5.86	0.63	5.00
T_{OFF}	0.74	5.86	0.63	5.00
T_P	0.74	5.86	0.63	5.00
T_H	0.74	5.86	0.63	5.00
T_L	0.74	5.86	0.63	5.00

T_N : Max value (Unit: msec)
Others : Min value

4.12.4 Control of event counter

Table 4.12.4.1 shows the event counter control bits and their addresses.

Table 4.12.4.1 Control bits of event counter

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
2F8H	EV03	EV02	EV01	EV00	EV03	0			Event counter 0 (low-order 4 bits)
					EV02	0			
	R				EV01	0			
					EV00	0			
2F9H	EV07	EV06	EV05	EV04	EV07	0			Event counter 0 (high-order 4 bits)
					EV06	0			
	R				EV05	0			
					EV04	0			
2FAH	EV13	EV12	EV11	EV10	EV13	0			Event counter 1 (low-order 4 bits)
					EV12	0			
	R				EV11	0			
					EV10	0			
2FBH	EV17	EV16	EV15	EV14	EV17	0			Event counter 1 (high-order 4 bits)
					EV16	0			
	R				EV15	0			
					EV14	0			
2FCH	EVSEL	ENRUN	EV1RST	EV0RST	EVSEL	0	Separate	Phase	Event counter mode selection
					EVRUN	0	Run	Stop	Event counter Run/Stop
	R/W		W		EV1RST*3	Reset	Reset	–	Event counter 1 reset
					EV0RST*3	Reset	Reset	–	Event counter 0 reset

*1 Initial value at initial reset
*2 Not set in the circuit
*3 Always "0" being read
*4 Reset (0) immediately after being read
*5 Undefined

EV00–EV03: Event counter 0 low-order data (2F8H)

The four low-order data bits of event counter 0 are read out.
These four bits are read-only, and cannot be used for writing.
At initial reset, event counter 0 is set to "00H".

EV04–EV07: Event counter 0 high-order data (2F9H)

The four high-order data bits of event counter 0 are read out.
These four bits are read-only, and cannot be used for writing.
At initial reset, event counter 0 is set to "00H".

EV10–EV13: Event counter 1 low-order data (2FAH)

The four low-order data bits of event counter 1 are read out.
These four bits are read-only, and cannot be used for writing.
At initial reset, event counter 1 is set to "00H".

EV14–EV17: Event counter 1 high-order data (2FBH)

The four high-order data bits of event counter 1 are read out.
These four bits are read-only, and cannot be used for writing.
At initial reset, event counter 1 is set to "00H".

EV0RST: Event counter 0 reset (2FCH•D0)

This is the register for resetting event counter 0.

When "1" is written : Event counter 0 reset
When "0" is written : No operation
Read-out : Always "0"

When "1" is written, event counter 0 is reset and the data becomes "00H". When "0" is written, no operation is executed.
This is a write-only bit, and is always "0" at read-out.

EV1RST: Event counter 1 reset (2FCH•D1)

This is the register for resetting event counter 1.

When "1" is written : Event counter 1 reset
When "0" is written : No operation
Read-out : Always "0"

When "1" is written, event counter 1 is reset and the data becomes "00H". When "0" is written, no operation is executed.
This is a write-only bit, and is always "0" at read-out.

EVRUN: Event counter RUN/STOP (2FCH•D2)

This register controls the event counter RUN/STOP status.

When "1" is written : RUN
When "0" is written : STOP
Read-out : Valid

When "1" is written, the event counter enters the RUN status and starts receiving the clock signal input. When "0" is written, the event counter enters the STOP status and the clock signal input is ignored. (However, input to the input port is valid.)
At initial reset, this register is set to "0".

EVSEL: Event counter mode (2FCH•D3)

This register control the count mode of the event counter.

When "1" is written : Separate
When "0" is written : Phase detection
Read-out : Valid

When "0" is written, the phases of the two clock signals are detected, and the phase detection mode is selected, in which one of the counters is chosen to input the clock signal. When "1" is written, the separate mode is selected, in which each clock signal is input to different counters.
At initial reset, this register is set to "0".

4.12.5 Programming notes

(1) After the event counter has written data to the EVRUN register, it operates or stops in synchronization with the falling edge of the noise rejector clock or stops. Hence, attention must be paid to the above timing when input signals (input to K02 and K03) are being received.

(2) To prevent erroneous reading of the event counter data, read out the counter data several times, compare it, and use the matching data as the result.

4.13 Analog Comparator

4.13.1 Configuration of analog comparator

The E0C6008 Series incorporates an MOS input analog comparator. This analog comparator, which has two differential input terminals (inverted input terminal AMPM, non-inverted input terminal AMPP), can be used for general purposes.
Figure 4.13.1.1 shows the configuration of the analog comparator.

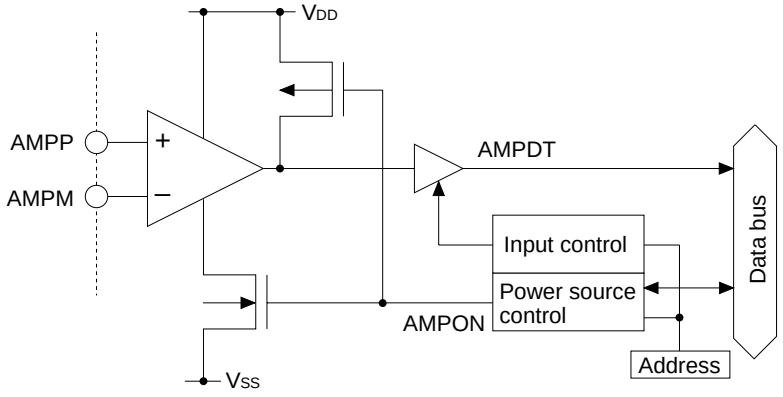


Fig. 4.13.1.1 Configuration of analog comparator

4.13.2 Operation of analog comparator

The analog comparator is ON when the AMPON register is "1", and compares the input levels of the AMPP and AMPM terminals. The result of the comparison is read from the AMPDT register. It is "1" when AMPP (+) > AMPM (-) and "0" when AMPP (+) < AMPM (-).

After the analog comparator goes ON it takes a maximum of 3 msec until the output stabilizes.

4.13.3 Control of analog comparator

Table 4.13.3.1 lists the analog comparator control bits and their addresses.

Table 4.13.3.1 Control bits of analog comparator

Address	Register								Comment
	D3	D2	D1	D0	Name	Init *1	1	0	
2F7H	ENVON	ENVRT	AMPDT	AMPON	ENVON	0	On	Off	Envelope On/Off
					ENVRT	0	1.0 sec	0.5 sec	Envelope cycle selection register
	R/W		R	R/W	AMPDT	1	+ > -	+ < -	Analog comparator data
					AMPON	0	On	Off	Analog comparator On/Off

*1 Initial value at initial reset
*2 Not set in the circuit
*3 Always "0" being read
*4 Reset (0) immediately after being read
*5 Undefined

AMPON: Analog comparator ON/OFF (2F7H•D0)

Switches the analog comparator ON and OFF.

When "1" is written : The analog comparator goes ON
When "0" is written : The analog comparator goes OFF
Read-out : Valid

The analog comparator goes ON when "1" is written to AMPON, and OFF when "0" is written.
At initial reset, AMPON is set to "0".

AMPDT: Analog comparator data (2F7H•D1)

Reads out the output from the analog comparator.

When "1" is read out : AMPP (+) > AMPM (-)
When "0" is read out : AMPP (+) < AMPM (-)
Writing : Invalid

AMPDT is "0" when the input level of the inverted input terminal (AMPM) is greater than the input level of the noninverted input terminal (AMPP); and "1" when smaller.
At initial reset, AMPDT is set to "1".

4.13.4 Programming notes

(1) To reduce current consumption, set the analog comparator to OFF when it is not necessary.

(2) After setting AMPON to "1", wait at least 3 msec for the operation of the analog comparator to stabilize before reading the output data of the analog comparator from AMPDT.

4.14 Battery Life Detection (BLD) Circuit

4.14.1 Configuration of BLD circuit

The E0C6008 Series has a built-in battery life detection (BLD) circuit, so that the software can find when the source voltage lowers. The configuration of the BLD circuit is shown in Figure 4.14.1.1.
Also provides a heavy load protection function and an associated sub-BLD circuit. See Section 4.15, "Heavy Load Protection Function and Sub-BLD Circuit".
Turning the BLD operation ON/OFF is controlled through the software (HLMOD, BLS). Moreover, when a drop in source voltage (BLD0 = "1") is detected by the sub-BLD circuit, BLD operation is periodically performed by the hardware until the source voltage is recovered (BLD0 = "0").
Because the power current consumption of the IC increases when the BLD operation is turned ON, set the BLD operation to OFF unless otherwise necessary.

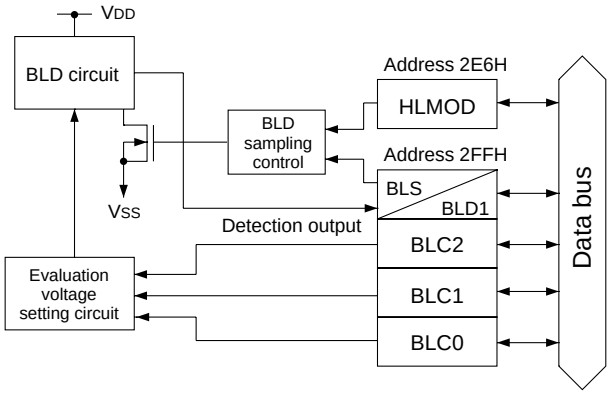


Fig. 4.14.1.1 Configuration of BLD circuit

4.14.2 Programmable selection of evaluation voltage

In the E0C6008 Series, the evaluation voltage for judging the battery life can be switched by programming. Consequently, the optimum evaluation voltage can be set for the battery used.
One of eight evaluation voltages can be selected with the software. Table 4.14.2.1 lists the evaluation voltages for the models in the E0C6008 Series.

Table 4.14.2.1 Evaluation voltages for BLD circuit

Register setting			Evaluation voltage (V)		
BLC2	BLC1	BLC0	E0C60L08	E0C6008	E0C60A08
0	0	0	1.05	2.20	2.20
0	0	1	1.10	2.25	2.25
0	1	0	1.15	2.30	2.30
0	1	1	1.20	2.35	2.35
1	0	0	1.25	2.40	2.40
1	0	1	1.30	2.45	2.45
1	1	0	1.35	2.50	2.50
1	1	1	1.40	2.55	2.55

See the electrical characteristics for the evaluation voltage accuracy.

4.14.3 Detection timing of BLD circuit

This section explains the timing for when the BLD circuit writes the result of the source voltage detection to the BLD latch.
Turning the BLD operation ON/OFF is controlled through the software (HLMOD, BLS). Moreover, when a drop in source voltage (BLD0 = "1") is detected by the sub-BLD circuit, BLD operation is periodically performed by the hardware until the source voltage is recovered (BLD0 = "0").
The result of the source voltage detection is written to the BLD latch by the BLD circuit, and this data can be read out by the software to find the status of the source voltage.
There are three status, explained below, for the detection timing of the BLD circuit.

(1) Sampling with HLMOD set to "1"

When HLMOD is set to "1" and BLD sampling executed, the detection results can be written to the BLD latch in the following two timings.

① Immediately after the time for one instruction cycle has ended immediately after HLMOD = "1"
② Immediately after sampling in the 2 Hz cycle output by the clock timer while HLMOD = "1"

Consequently, the BLD latch data is loaded immediately after HLMOD has been set to "1", and at the same time the new detection result is written in 2 Hz cycles.
To obtain a stable BLD detection result, the BLD circuit must be set to ON with at least 100 µsec.
When the CPU system clock is f_{OSC3} in the E0C60A08, the detection result at the timing in ① above may be invalid or incorrect. (When performing BLD detection using the timing in ①, be sure that the CPU system clock is f_{OSC1}.)

(2) Sampling with BLS set to "1"

When BLS is set to "1", BLD detection is executed. As soon as BLS is reset to "0" the detection result is loaded to the BLD latch. To obtain a stable BLD detection result, the BLD circuit must be set to ON with at least 100 µsec. Hence, to obtain the BLD detection result, follow the programming sequence below.

0. Set HLMOD to "1" (only when the CPU system clock is f_{OSC3} in the E0C60A08)
1. Set BLS to "1"
2. Maintain at 100 µsec minimum
3. Set BLS to "0"
4. Read out BLD
5. Set HLMOD to "0" (only when the CPU system clock is f_{OSC3} in the E0C60A08)

However, when a crystal oscillation clock (f_{OSC1}) is selected for the CPU system clock in the E0C6008, E0C60L08, and E0C60A08, the instruction cycles are long enough, so that there is no need for concern about maintaining 100 µsec for the BLS = "1" with the software.

(3) Sampling by hardware when sub-BLD latch is set to "1"

When BLD0 (sub-BLD latch) is set to "1", the detection results can be written to the BLD0 (sub-BLD latch) and BLD1 (BLD latch) in the following two timings (same as that sampling with HLMOD set to "1").

① Immediately after the time for one instruction cycle has ended immediately after BLD0 = "1"
② Immediately after sampling in the 2 Hz cycle output by the clock timer while BLD0 = "1"

Consequently, the BLD0 (sub-BLD latch) and BLD1 (BLD latch) data are loaded immediately after BLD0 (sub-BLD latch) has been set to "1", and at the same time the new detection result is written in 2 Hz cycles.
To obtain a stable BLD detection result, the BLD circuit must be set to ON with at least 100 µsec.
When the CPU system clock is f_{OSC3} in the E0C60A08, the detection result at the timing in ① above may be invalid or incorrect.

4.14.4 Control of BLD circuit

Table 4.14.4.1 shows the BLD circuit's control bits and their addresses.

Table 4.14.4.1 Control bits of BLD circuit

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
2E6H	HLMOD	BLD0	EISWIT1	EISWIT0	HLMOD	0	Heavy load	Normal	Heavy load protection mode register
					BLD0	0	Low	Normal	Sub-BLD evaluation data
	R/W	R	R/W		EISWIT1	0	Enable	Mask	Interrupt mask register (stopwatch 1 Hz)
					EISWIT0	0	Enable	Mask	Interrupt mask register (stopwatch 10 Hz)
2FFH	BLS / BLD1	BLC2	BLC1	BLC0	BLS	0	On	Off	BLD On/Off
					BLD1	0	Low	Normal	BLD evaluation data
					BLC2	× *5			Evaluation voltage setting register
	W / R	R/W			BLC1	× *5			[BLC2–0] 0 1 2 3 4 5 6 7
					BLC0	× *5			E0C6008/A08 2.20 2.25 2.30 2.35 2.40 2.45 2.50 2.55 (V)
									E0C60L08 1.05 1.10 1.15 1.20 1.25 1.30 1.35 1.40 (V)

*1 Initial value at initial reset
*2 Not set in the circuit
*3 Always "0" being read
*4 Reset (0) immediately after being read
*5 Undefined

HLMOD: Heavy load protection mode (2E6H•D3)

Sets the IC in heavy load protection mode.

When "1" is written : Heavy load protection mode is set
When "0" is written : Heavy load protection mode is released
Read-out : Valid

When HLMOD is set to "1", the IC operating status enters the heavy load protection mode and at the same time the battery life detection of the BLD circuit is controlled (ON/OFF).
For details about the heavy load protection mode, see Section 4.15, "Heavy Load Protection Function and Sub-BLD Circuit".
When HLMOD is set to "1", sampling control is executed for the BLD circuit ON time. There are two types of sampling time, as follows:

(1) The time of one instruction cycle immediately after HLMOD = "1"
(2) Sampling at cycles of 2 Hz output by the clock timer while HLMOD = "1"

The BLD circuit must be made ON with at least 100 µsec for the BLD circuit to respond. Hence, when the CPU system clock is f_{OSC3} in the E0C60A08, the detection result at the timing in (1) above may be invalid or incorrect. When performing BLD detection using the timing in (1), be sure that the CPU system clock is f_{OSC1}.
When BLD sampling is done with HLMOD set to "1", the results are written to the BLD latch in the timing as follows:

(1) As soon as the time has elapsed for one instruction cycle immediately following HLMOD = "1"
(2) Immediately on completion of sampling at cycles of 2 Hz output by the clock timer while HLMOD = "1"

Consequently, the BLD latch data is written immediately after HLMOD is set to "1", and at the same time the new detection result is written in 2 Hz cycles.

BLS/BLD1: BLD detection/BLD data (2FFH•D3)

Controls the BLD operation.

When "0" is written : BLD detection OFF
When "1" is written : BLD detection ON
When "0" is read out : Source voltage (V_{DD}–V_{SS}) is higher than BLD set value
When "1" is read out : Source voltage (V_{DD}–V_{SS}) is lower than BLD set value

Note that the function of this bit when written is different to when read out.
When this bit is written to, ON/OFF of the BLD detection operation is controlled; when this bit is read out, the result of the BLD detection (contents of BLD latch) is obtained. Appreciable current is consumed during operation of BLD detection, so keep BLD detection OFF except when necessary.

When BLS is set to "1", BLD detection is executed. As soon as BLS is reset to "0" the detection result is loaded to the BLD latch. To obtain a stable BLD detection result, the BLD circuit must be set to ON with at least 100 µsec. Hence, to obtain the BLD detection result, follow the programming sequence below.

0. Set HLMOD to "1" (only when the CPU system clock is f_{OSC3} in the E0C60A08)
1. Set BLS to "1"
2. Maintain at 100 µsec minimum
3. Set BLS to "0"
4. Read out BLD
5. Set HLMOD to "0" (only when the CPU system clock is f_{OSC3} in the E0C60A08)

However, when a crystal oscillation clock (f_{OSC1}) is selected for the CPU system clock in the E0C6008, E0C60L08, and E0C60A08, the instruction cycles are long enough, so that there is no need for concern about maintaining 100 µsec for the BLS = "1" with the software.

4.14.5 Programming notes

(1) It takes 100 µsec from the time the BLD circuit goes ON until a stable result is obtained. For this reason, keep the following software notes in mind:

When the CPU system clock is f_{OSC1}

1. When detection is done at HLMOD
   After writing "1" on HLMOD, read the BLD after 1 instruction has passed.
2. When detection is done at BLS
   After writing "1" on BLS, write "0" after at least 100 µsec has lapsed (possible with the next instruction) and then read the BLD.

When the CPU system clock is f_{OSC3} (in case of E0C60A08 only)

1. When detection is done at HLMOD
   After writing "1" on HLMOD, read the BLD after 0.6 second has passed. (HLMOD holds "1" for at least 0.6 second)
2. When detection is done at BLS
   Before writing "1" on BLS, write "1" on HLMOD first; after at least 100 µsec has lapsed after writing "1" on BLS, write "0" on BLS and then read the BLD.

(2) BLS resides in the same bit at the same address as BLD1, and one or the other is selected by write or read operation. This means that arithmetic operations (AND, OR, ADD, SUB and so forth) cannot be used for BLS control.

4.15 Heavy Load Protection Function and Sub-BLD Circuit

This section explains the heavy load protection and sub-BLD circuit.

4.15.1 Heavy load protection function

Note that the heavy load protection function on the E0C60L08 is different from the E0C6008/60A08.

(1) In case of E0C60L08

The E0C60L08 has the heavy load protection function for when the battery load becomes heavy and the source voltage drops, such as when an external buzzer sounds or an external lamp lights. The state where the heavy load protection function is in effect is called the heavy load protection mode. In this mode, operation with a lower voltage than normal is possible.
The normal mode changes to the heavy load protection mode in the following two cases:

① When the software changes the mode to the heavy load protection mode (HLMOD = "1")
② When source voltage drop (BLD0 = "1") in the sub-BLD circuit is detected, the mode will automatically shift to the heavy load protection mode until the source voltage is recovered (BLD0 = "0")

The sub-BLD circuit, a BLD circuit dedicated to 2.4 V/1.2 V detection, operates in synchronize with the BLD circuit. It is the E0C60L08's battery life detection circuit controlling the heavy load protection function so that operation is assured even when the source voltage drops.
Based on the workings of the sub-BLD circuit and the heavy load protection function, the E0C60L08 realizes operation at 0.9 V source voltage. See the electrical characteristics for the precisions of voltage detection by this sub-BLD circuit.
Figure 4.15.1.1 shows the configuration of the heavy load protection function and the sub-BLD circuit.

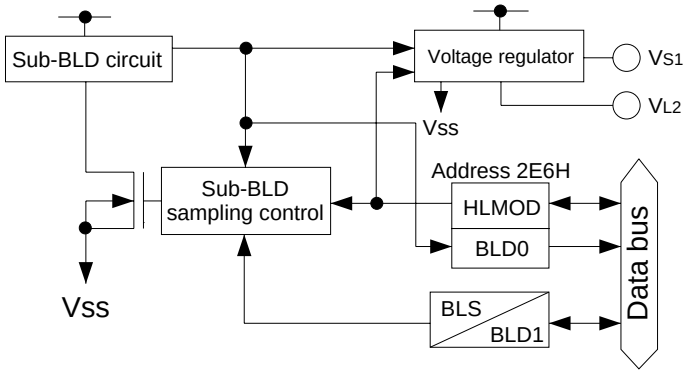


Fig. 4.15.1.1 Configuration of sub-BLD circuit

In the heavy load protection mode, the internally regulated voltage is generated by the liquid crystal driver source output V_{L2} so as to operate the internal circuit. Consequently, more current is consumed in the heavy load protection mode than in the normal mode. Unless it is necessary, be careful not to set the heavy load protection mode with the software.

(2) In case of E0C6008/60A08

The E0C6008/60A08 has the heavy load protection function for when the battery load becomes heavy and the source voltage changes, such as when an external buzzer sounds or an external lamp lights. The state where the heavy load protection function is in effect is called the heavy load protection mode. Compared with the normal operation mode, this mode can reduce the output voltage variation of the constant voltage/booster voltage circuit of the LCD system.
The normal mode changes to the heavy load protection mode in the following case:

- When the software changes the mode to the heavy load protection mode (HLMOD = "1")

The heavy load protection mode switches the constant voltage circuit of the LCD system to the high-stability mode from the low current consumption mode. Consequently, more current is consumed in the heavy load protection mode than in the normal mode. Unless it is necessary, be careful not to set the heavy load protection mode with the software.

4.15.2 Operation of sub-BLD circuit

Software control of the sub-BLD circuit is virtually the same as for the BLD circuit, except that the evaluation voltage cannot be set by programming.
Just as for the BLD circuit, HLMOD or BLS control the detection timing of the sub-BLD circuit and the timing for writing the detection data to the sub-BLD latch. However, for the E0C60L08, even if the sub-BLD circuit detects a drop in source voltage (1.2 V or below) and invokes the heavy load protection mode, this will be the same as when the software invokes the heavy load protection mode, in that the BLD circuit and sub-BLD circuit will be sampled in timing synchronized to the 2 Hz output from the prescaler. If the sub-BLD circuit detects a voltage drop and enters the heavy load protection mode, it will return to the normal mode once the source voltage recovers and the BLD circuit judges that the source voltage is 1.2 V or more.
For the E0C6008/60A08, when the sub-BLD circuit detects a drop in source voltage (2.4 V or below) and the detection data is written to the sub-BLD latch, the BLD circuit and sub-BLD circuit will be sampled in timing synchronized to the 2 Hz output from the prescaler. Once the source voltage recovers and the BLD circuit judges that the source voltage is 2.4 V or more, the BLD circuit and sub-BLD circuit won't be sampled in timing synchronized to the 2 Hz output from the prescaler.

4.15.3 Control of heavy load protection function and sub-BLD circuit

Table 4.15.3.1 shows the control bits and their addresses for the heavy load protection function and sub-BLD circuit.

Table 4.15.3.1 Control bits of heavy load protection function and sub-BLD circuit

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
2E6H	HLMOD	BLD0	EISWIT1	EISWIT0	HLMOD	0	Heavy load	Normal	Heavy load protection mode register
					BLD0	0	Low	Normal	Sub-BLD evaluation data
	R/W	R	R/W		EISWIT1	0	Enable	Mask	Interrupt mask register (stopwatch 1 Hz)
					EISWIT0	0	Enable	Mask	Interrupt mask register (stopwatch 10 Hz)
2FFH	BLS / BLD1	BLC2	BLC1	BLC0	BLS	0	On	Off	BLD On/Off
					BLD1	0	Low	Normal	BLD evaluation data
	W / R	R/W			BLC2	×*5			Evaluation voltage setting register
					BLC1	×*5			[BLC2–0] 0 1 2 3 4 5 6 7
					BLC0	×*5			E0C6008/A08 2.20 2.25 2.30 2.35 2.40 2.45 2.50 2.55 (V)
									E0C60L08 1.05 1.10 1.15 1.20 1.25 1.30 1.35 1.40 (V)

*1 Initial value at initial reset
*2 Not set in the circuit
*3 Always "0" being read
*4 Reset (0) immediately after being read
*5 Undefined

HLMOD: Heavy load protection mode (2E6H•D3)

Sets the IC in heavy load protection mode.

When "1" is written : Heavy load protection mode is set
When "0" is written : Heavy load protection mode is released
Read-out : Valid

When HLMOD is set to "1", the IC operating status enters the heavy load protection mode and at the same time the battery life detection of the BLD circuit is controlled (ON/OFF).
When HLMOD is set to "1", sampling control is executed for the BLD circuit ON time. There are two types of sampling time, as follows:

(1) The time of one instruction cycle immediately after HLMOD = "1"
(2) Sampling at cycles of 2 Hz output by the clock timer while HLMOD = "1"

The BLD circuit must be made ON with at least 100 µsec for the BLD circuit to respond. Hence, when the CPU system clock is f_{OSC3} in the E0C60A08, the detection result at the timing in (1) above may be invalid or incorrect. When performing BLD detection using the timing in (1), be sure that the CPU system clock is f_{OSC1}.
When BLD sampling is done with HLMOD set to "1", the results are written to the BLD latch in the timing as follows:

(1) As soon as the time has elapsed for one instruction cycle immediately following HLMOD = "1"
(2) Immediately on completion of sampling at cycles of 2 Hz output by the clock timer while HLMOD = "1"

Consequently, the BLD latch data is written immediately after HLMOD is set to "1", and at the same time the new detection result is written in 2 Hz cycles.

BLD0: Sub-BLD data (2E6H·D2)

The voltage detection data in the heavy load protection mode is read out.

When "0" is read out : High source voltage upward from about
2.4 V (E0C6008/60A08)/1.2 V (E0C60L08)
When "1" is read out : Low source voltage from about
2.4 V (E0C6008/60A08)/1.2 V (E0C60L08) or under
Writing : Invalid

When BLD0 is "1" the CPU enters the heavy load protection mode. In the heavy load protection mode, the detection operation of the BLD circuit and sub-BLD circuit is sampled in 2 Hz cycles, and the respective detection results are written to the BLD latch and sub-BLD latch.

BLS/BLD1: BLD detection/BLD data (2FFH•D3)

Controls the BLD operation.

When "0" is written : BLD detection OFF
When "1" is written : BLD detection ON
When "0" is read out : Source voltage (V_{DD}–V_{SS}) is higher than BLD set value
When "1" is read out : Source voltage (V_{DD}–V_{SS}) is lower than BLD set value

Note that the function of this bit when written is different to when read out.
When this bit is written to, ON/OFF of the BLD detection operation is controlled; when this bit is read out, the result of the BLD detection (contents of BLD latch) is obtained. Appreciable current is consumed during operation of BLD detection, so keep BLD detection OFF except when necessary.

When BLS is set to "1", BLD detection is executed. As soon as BLS is reset to "0" the detection result is loaded to the BLD latch. To obtain a stable BLD detection result, the BLD circuit must be set to ON with at least 100 µsec. Hence, to obtain the BLD detection result, follow the programming sequence below.

0. Set HLMOD to "1" (only when the CPU system clock is f_{OSC3} in the E0C60A08)
1. Set BLS to "1"
2. Maintain at 100 µsec minimum
3. Set BLS to "0"
4. Read out BLD
5. Set HLMOD to "0" (only when the CPU system clock is f_{OSC3} in the E0C60A08)

However, when a crystal oscillation clock (f_{OSC1}) is selected for the CPU system clock in the E0C6008, E0C60L08, and E0C60A08, the instruction cycles are long enough, so that there is no need for concern about maintaining 100 µsec for the BLS = "1" with the software.

4.15.4 Programming notes

(1) It takes 100 µsec from the time the BLD circuit goes ON until a stable result is obtained. For this reason, keep the following software notes in mind:

When the CPU system clock is f_{OSC1}

1. When detection is done at HLMOD
   After writing "1" on HLMOD, read the BLD after 1 instruction has passed.
2. When detection is done at BLS
   After writing "1" on BLS, write "0" after at least 100 µsec has lapsed (possible with the next instruction) and then read the BLD.

When the CPU system clock is f_{OSC3} (in case of E0C60A08 only)

1. When detection is done at HLMOD
   After writing "1" on HLMOD, read the BLD after 0.6 second has passed. (HLMOD holds "1" for at least 0.6 second)
2. When detection is done at BLS
   Before writing "1" on BLS, write "1" on HLMOD first; after at least 100 µsec has lapsed after writing "1" on BLS, write "0" on BLS and then read the BLD.

(2) BLS resides in the same bit at the same address as BLD1, and one or the other is selected by write or read operation. This means that arithmetic operations (AND, OR, ADD, SUB and so forth) cannot be used for BLS control.

(3) Select one of the following software processing to return to the normal mode after a heavy load has been driven in the heavy load protection mode in the E0C60L08.

① After heavy load drive is completed, return to the normal mode after at least one second has elapsed.

② After heavy load drive is completed, switch BLS ON and OFF (at least 100 µsec is necessary for the ON status) and then return to the normal mode.

The E0C6008/60A08 returns to the normal mode after driving a heavy load without special software processing.

(4) If the BLS is set to ON while the heavy load protection mode is in effect, keep the ON time within 10 msec.

4.16 Interrupt and HALT

The E0C6008 Series provides the following interrupt settings, each of which is maskable.

External interrupt: Input interrupt (three)
Internal interrupt: Timer interrupt (three)
Stopwatch interrupt (two)
Serial interface interrupt (one)

To authorize interrupt, the interrupt flag must be set to "1" (EI) and the necessary related interrupt mask registers must be set to "1" (enable).
When an interrupt occurs the interrupt flag is automatically reset to "0" (DI), and interrupts after that are inhibited.
When a HALT instruction is input the CPU operating clock stops, and the CPU enters the HALT status.
The CPU is reactivated from the HALT status when an interrupt request occurs.
If reactivation is not caused by an interrupt request, initial reset by the watchdog timer causes reactivates the CPU (when the watchdog timer is enabled).
Figure 4.16.1 shows the configuration of the interrupt circuit.

Interrupt vector map

Table 4.16.1 Interrupt vector map

Page	Step	Interrupt vector
1	00H	Initial reset
	01H	Serial interface interrupt
	02H	Input port interrupt
	03H	Serial interface + Input port interrupt
	04H	Clock timer interrupt
	05H	Serial interface + Clock timer interrupt
	06H	Input port + Clock timer interrupt
	07H	Serial interface + Input port + Clock timer interrupt
	08H	Stopwatch timer interrupt
	09H	Serial interface + Stopwatch timer interrupt
	0AH	Input port + Stopwatch timer interrupt
	0BH	Serial interface + Input port + Stopwatch timer interrupt
	0CH	Clock timer + Stopwatch timer interrupt
	0DH	Serial interface + Clock timer + Stopwatch timer interrupt
	0EH	Input port + Clock timer + Stopwatch timer interrupt
	0FH	All interrupts

The interrupt service routine start address should be written to each interrupt vector address.

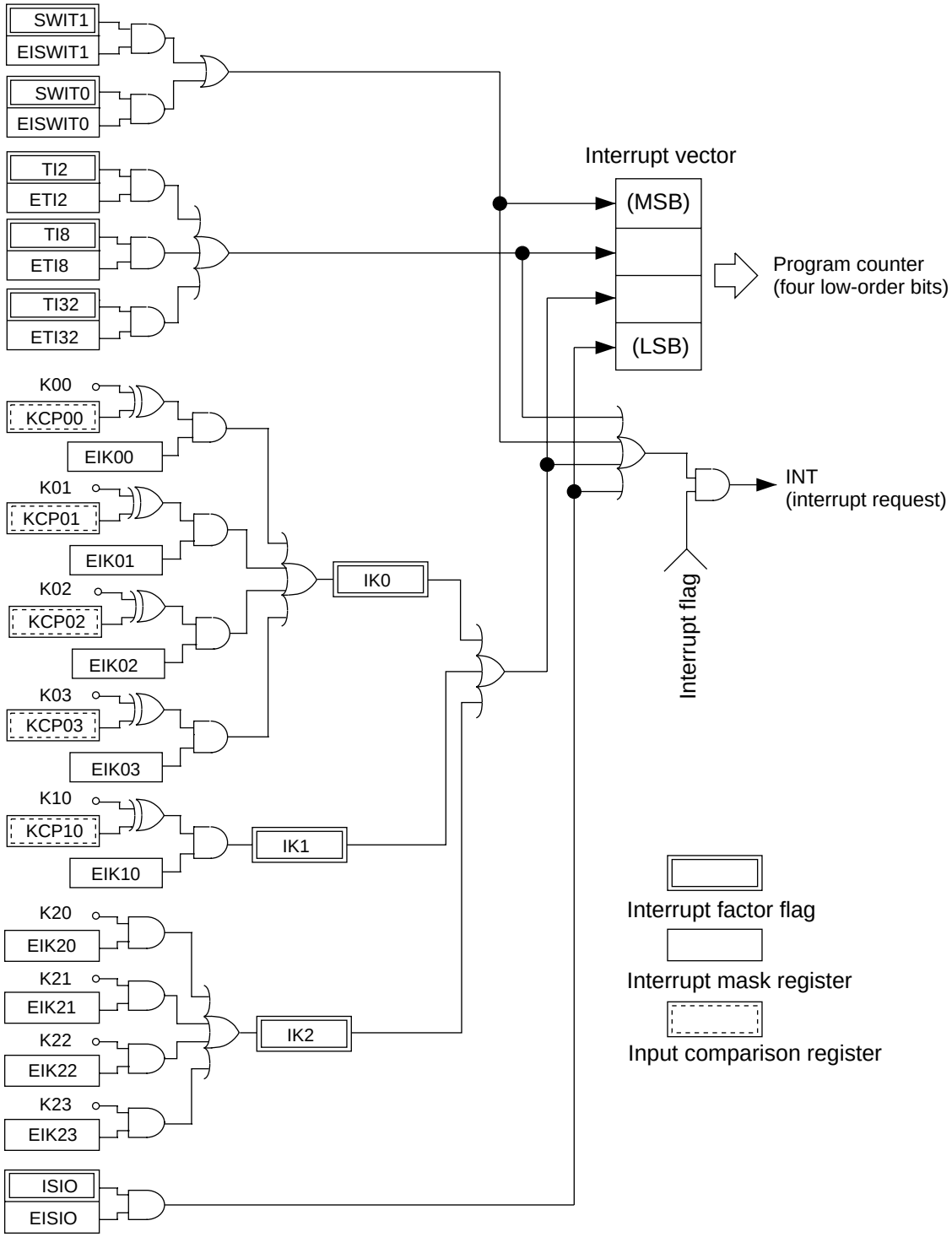


Fig. 4.16.1 Configuration of interrupt circuit

4.16.1 Interrupt factors

Table 4.16.1.1 shows the factors for generating interrupt requests.
The interrupt flags are set to "1" depending on the corresponding interrupt factors.
The CPU operation is interrupted when any of the conditions below set an interrupt factor flag to "1".

- The corresponding mask register is "1" (enabled)
- The interrupt flag is "1" (EI)

The interrupt factor flag is a read-only register, but can be reset to "0" when the register data is read out.
At initial reset, the interrupt factor flags are reset to "0".

Note: Read the interrupt factor flags only in the DI status (interrupt flag = "0"). A malfunction could result from read-out during the EI status (interrupt flag = "1").

Table 4.16.1.1 Interrupt factors

Interrupt factor	Interrupt factor flag
Clock timer 2 Hz falling edge	TI2 (2E9H•D2)
Clock timer 8 Hz falling edge	TI8 (2E9H•D1)
Clock timer 32 Hz falling edge	TI32 (2E9H•D0)
Stopwatch timer 1 Hz falling edge	SWIT1 (2EAH•D1)
Stopwatch timer 10 Hz falling edge	SWIT0 (2EAH•D0)
Serial interface When 8-bit data input/output has completed	ISIO (2F3H•D0)
Input (K00–K03) port rising/falling edge	IK0 (2EAH•D2)
Input (K10) port rising/falling edge	IK1 (2EAH•D3)
Input (K20–K23) port rising edge	IK2 (2F3H•D1)

4.16.2 Specific masks and factor flags for interrupt

The interrupt factor flags can be masked by the corresponding interrupt mask registers.
The interrupt mask registers are read/write registers. They are enabled (interrupt authorized) when "1" is written to them, and masked (interrupt inhibited) when "0" is written to them.
At initial reset, the interrupt mask register is set to "0".
Table 4.16.2.1 shows the correspondence between interrupt mask registers and interrupt factor flags.

Table 4.16.2.1 Interrupt mask registers and interrupt factor flags

Interrupt mask register		Interrupt factor flag	
ETI2	(2E8H•D2)	TI2	(2E9H•D2)
ETI8	(2E8H•D1)	TI8	(2E9H•D1)
ETI32	(2E8H•D0)	TI32	(2E9H•D0)
EISWIT1	(2E6H•D1)	SWIT1	(2EAH•D1)
EISWIT0	(2E6H•D0)	SWIT0	(2EAH•D0)
EISIO	(2F2H•D0)	ISIO	(2F3H•D0)
EIK03*	(2E5H•D3)	IK0	(2EAH•D2)
EIK02*	(2E5H•D2)		
EIK01*	(2E5H•D1)		
EIK00*	(2E5H•D0)		
EIK10*	(2E7H•D2)	IK1	(2EAH•D3)
EIK23*	(2F5H•D3)	IK2	(2F3H•D1)
EIK22*	(2F5H•D2)		
EIK21*	(2F5H•D1)		
EIK20*	(2F5H•D0)		

∗ There is an interrupt mask register for each pin of the input ports.

4.16.3 Interrupt vectors

When an interrupt request is input to the CPU, the CPU begins interrupt processing. After the program being executed is terminated, the interrupt processing is executed in the following order.

① The address data (value of program counter) of the program to be executed next is saved in the stack area (RAM).

② The interrupt request causes the value of the interrupt vector (page 1, 01H–0FH) to be set in the program counter.

③ The program at the specified address is executed (execution of interrupt processing routine by software).

Table 4.16.3.1 shows the correspondence of interrupt requests and interrupt vectors.

Note: The processing in ① and ② above take 12 cycles of the CPU system clock.

Table 4.16.3.1 Interrupt request and interrupt vectors

PC	Value	Interrupt request	
PCS3	1	Stopwatch timer interrupt	Enabled
	0		Masked
PCS2	1	Clock timer interrupt	Enabled
	0		Masked
PCS1	1	Input port interrupt	Enabled
	0		Masked
PCS0	1	Serial interface interrupt	Enabled
	0		Masked

The four low-order bits of the program counter are indirectly addressed through the interrupt request.

4.16.4 Control of interrupt and HALT

Table 4.16.4.1 shows the interrupt control bits and their addresses.

Table 4.16.4.1 Interrupt control bits

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
2E4H	KCP03	KCP02	KCP01	KCP00	KCP03	0	↓	↑	Input comparison register (K00–K03)
					KCP02	0	↓	↑	
					KCP01	0	↓	↑	
	R/W				KCP00	0	↓	↑	
2E5H	EIK03	EIK02	EIK01	EIK00	EIK03	0	Enable	Mask	Interrupt mask register (K00–K03)
					EIK02	0	Enable	Mask	
					EIK01	0	Enable	Mask	
	R/W				EIK00	0	Enable	Mask	
2E6H	HLMOD	BLD0	EISWIT1	EISWIT0	HLMOD	0	Heavy load	Normal	Heavy load protection mode register
					BLD0	0	Low	Normal	Sub-BLD evaluation data
	R/W	R	R/W		EISWIT1	0	Enable	Mask	Interrupt mask register (stopwatch 1 Hz)
					EISWIT0	0	Enable	Mask	Interrupt mask register (stopwatch 10 Hz)
2E7H	SCTRG	EIK10	KCP10	K10	SCTRG*3	–	Trigger	–	Serial I/F clock trigger
					EIK10	0	Enable	Mask	Interrupt mask register (K10)
	W	R/W		R	KCP10	0	↓	↑	Input comparison register (K10)
					K10	– *2	High	Low	Input port data (K10)
2E8H	CSDC	ETI2	ETI8	ETI32	CSDC	0	Static	Dynamic	LCD drive switch
					ETI2	0	Enable	Mask	Interrupt mask register (clock timer 2 Hz)
					ETI8	0	Enable	Mask	Interrupt mask register (clock timer 8 Hz)
	R/W				ETI32	0	Enable	Mask	Interrupt mask register (clock timer 32 Hz)
2E9H	0	TI2	TI8	TI32	0 *3	– *2	–	–	Unused
					TI2 *4	0	Yes	No	Interrupt factor flag (clock timer 2 Hz)
					TI8 *4	0	Yes	No	Interrupt factor flag (clock timer 8 Hz)
	R				TI32 *4	0	Yes	No	Interrupt factor flag (clock timer 32 Hz)
2EAH	IK1	IK0	SWIT1	SWIT0	IK1 *4	0	Yes	No	Interrupt factor flag (K10)
					IK0 *4	0	Yes	No	Interrupt factor flag (K00–K03)
					SWIT1 *4	0	Yes	No	Interrupt factor flag (stopwatch 1 Hz)
	R				SWIT0 *4	0	Yes	No	Interrupt factor flag (stopwatch 10 Hz)
2F2H	SCS1	SCS0	SE2	EISIO	SCS1	1			Serial I/F clock mode selection [SCS1, 0] 0 1 2 3 / Clock CLK CLK/2 CLK/4 Slave
					SCS0	1			
					SE2	0	↑	↓	Serial I/F clock edge selection
	R/W				EISIO	0	Enable	Mask	Interrupt mask register (serial I/F)
2F3H	0	0	IK2	ISIO	0 *3	– *2	–	–	Unused
					0 *3	– *2	–	–	Unused
	R				IK2 *4	0	Yes	No	Interrupt factor flag (K20–K23)
					ISIO *4	0	Yes	No	Interrupt factor flag (serial I/F)
2F5H	EIK23	EIK22	EIK21	EIK20	EIK23	0	Enable	Mask	Interrupt mask register (K20–K23)
					EIK22	0	Enable	Mask	
					EIK21	0	Enable	Mask	
	R/W				EIK20	0	Enable	Mask	

*1 Initial value at initial reset
*2 Not set in the circuit
*3 Always "0" being read
*4 Reset (0) immediately after being read
*5 Undefined

ETI32, ETI8, ETI2: Interrupt mask registers (2E8H•D0–D2)
TI32, TI8, TI2: Interrupt factor flags (2E9H•D0–D2)
See Section 4.9, "Clock Timer".

EISWIT0, EISWIT1: Interrupt mask registers (2E6H•D0–D1)
SWIT0, SWIT1: Interrupt factor flags (2EAH•D0–D1)
See Section 4.10, "Stopwatch Timer".

EISIO: Interrupt mask register (2F2H•D0)
ISIO: Interrupt factor flag (2F3H•D0)
See Section 4.7, "Serial Interface".

KCP00–KCP03: Input comparison registers (2E4H)
EIK00–EIK03: Interrupt mask registers (2E5H)
IK0: Interrupt factor flag (2EAH•D2)
See Section 4.4, "Input Ports".

KCP10: Input comparison register (2E7H•D1)
EIK10: Interrupt mask register (2E7H•D2)
IK1: Interrupt factor flag (2EAH•D3)
See Section 4.4, "Input Ports".

EIK20–EIK23: Interrupt mask register (2F5H)
IK2: Interrupt factor flag (2F3H•D1)
See Section 4.4, "Input Ports".

4.16.5 Programming notes

(1) When the interrupt mask register (EIK) is set to "0", the interrupt factor flag (IK) of the input port cannot be set even though the terminal status of the input port has changed.

(2) The interrupt factor flags of the clock timer, stopwatch timer and serial interface (TI, SWIT, ISIO) are set when the timing condition is established, even if the interrupt mask registers (ETI, EISWIT, EISIO) are set to "0".

(3) Read out the interrupt factor flags only in the DI status (interrupt flag = "0"). If read-out is performed in the EI status (interrupt flag = "1") a malfunction will result.

(4) Writing to the interrupt mask register only in the DI status (interrupt flag = "0"). Writing to the interrupt mask register while in the EI status (interrupt flag = "1") may cause mulfunction.

CHAPTER 5 SUMMARY OF NOTES

5.1 Notes for Low Current Consumption

The E0C6008 Series contains control registers for each of the circuits so that current consumption can be lowered. These control registers lower the current consumption through programs that operate the circuits at the minimum levels.
The following text explains the circuits that can control operation and their control registers. Refer to these when putting programs together.

Table 5.1.1 Circuits and control register

Circuit (and item)	Control register	Order of consumed current
CPU	HALT instruction	See Electrical Characteristics (Chapter 7)
CPU operating frequency (E0C60A08)	CLKCHG, OSCC	See Electrical Characteristics (Chapter 7)
Heavy load protection mode	HLMOD	See Electrical Characteristics (Chapter 7)
BLD circuit	HLMOD, BLS	Several tens µA
Analog comparator	AMPON	Several tens µA

Below are the circuit statuses at initial reset.

CPU: Operating status
CPU operating frequency: Low speed side (CLKCHG = "0"),
OSC3 oscillation circuit stop status (OSCC = "0")
Heavy load protection mode: Normal operating mode (HLMOD = "0")
BLD circuit: OFF status (HLMOD = "0", BLS = "0")
Analog comparator: OFF status (AMPON = "0")

Also, be careful about panel selection because the current consumption can differ by the order of several µA on account of the LCD panel characteristics.

5.2 Summary of Notes by Function

Here, the cautionary notes are summed up by function category. Keep these notes well in mind when programming.

Memory

Memory is not mounted in unused area within the memory map and in memory area not indicated in this manual. For this reason, normal operation cannot be assured for programs that have been prepared with access to these areas.

Watchdog timer

When the watchdog timer is being used, the software must reset it within 3-second cycles, and timer data (WD0–WD2) cannot be used for timer applications.

Oscillation circuit and prescaler

(1) It takes at least 5 msec from the time the OSC3 oscillation circuit goes ON until the oscillation stabilizes. Consequently, when switching the CPU operation clock from OSC1 to OSC3, do this after a minimum of 5 msec have elapsed since the OSC3 oscillation went ON.
Further, the oscillation stabilization time varies depending on the external oscillator characteristics and conditions of use, so allow ample margin when setting the wait time.

(2) When switching the clock form OSC3 to OSC1, use a separate instruction for switching the OSC3 oscillation OFF. An error in the CPU operation can result if this processing is performed at the same time by the one instruction.

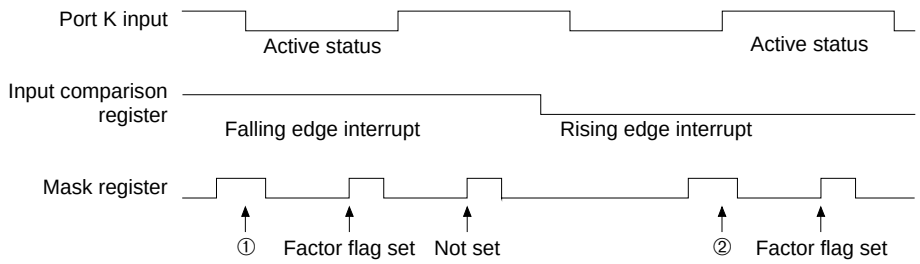
(3) To operate the clock timer and stopwatch timer accurately, select the prescaler of the OSC1 to match the crystal oscillator used.

Input port

(1) When input ports are changed from high to low by pull-down resistance, the fall of the waveform is delayed on account of the time constant of the pull-down resistance and input gate capacitance. Hence, when fetching input ports, set an appropriate wait time.
Particular care needs to be taken of the key scan during key matrix configuration. Aim for a wait time of about 1 msec.

(2) When "Use" is selected with the noise rejector mask option, a maximum delay of 1 msec occurs from time the interrupt conditions are established until the interrupt factor flag (IK) is set to "1" (until the interrupt is actually generated). Hence, pay attention to the timing when reading out (resetting) the interrupt factor flag. For example, when performing a key scan with the key matrix, the key scan changes the input status to set the interrupt factor flag, so it has to be read out to reset it. However, if the interrupt factor flag is read out immediately after key scanning, the delay will cause the flag to be set after read-out, so that it will not be reset.

(3) Input interrupt programing related precautions



When the content of the mask register is rewritten while the port K input is in the active status, the input interrupt factor flags are set at ① and ②, ① being the interrupt due to the falling edge and ② the interrupt due to the rising edge.

Fig. 5.2.1 Input interrupt timing

When using an input interrupt, if you rewrite the content of the mask register, when the value of the input terminal which becomes the interrupt input is in the active status, the factor flag for input interrupt may be set.
Therefore, when using the input interrupt, the active status of the input terminal implies
input terminal = low status, when the falling edge interrupt is effected and
input terminal = high status, when the rising edge interrupt is effected.
When an interrupt is triggered at the falling edge of an input terminal, a factor flag is set with the timing of ① shown in Figure 5.2.1. However, when clearing the content of the mask register with the input terminal kept in the low status and then setting it, the factor flag of the input interrupt is again set at the timing that has been set.
Consequently, when the input terminal is in the active status (low status), do not rewrite the mask register (clearing, then setting the mask register), so that a factor flag will only set at the falling edge in this case. When clearing, then setting the mask register, set the mask register, when the input terminal is not in the active status (high status).
When an interrupt is triggered at the rising edge of the input terminal, a factor flag will be set at the timing of ② shown in Figure 5.2.1. In this case, when the mask registers cleared, then set, you should set the mask register, when the input terminal is in the low status.
In addition, when the mask register = "1" and the content of the input comparison register is rewritten in the input terminal active status, an input interrupt factor flag may be set. Thus, you should rewrite the content of the input comparison register in the mask register = "0" status.

Output port

When BZ, $\overline{BZ}$ and FOUT are selected with the mask option, a hazard may be observed in the output waveform when the data of the output register changes.

I/O port

(1) When input data are changed from high to low by built-in pull-down resistance, the fall of the waveform is delayed on account of the time constant of the pull-down resistance and input gate capacitance. Consequently, if data is read out while the CPU is running in the OSC3 oscillation circuit, data must be read out continuously for about 500 μsec.

(2) When the I/O port is set to the output mode and the data register has been read, the terminal data instead of the register data can be read out. Because of this, if a low-impedance load is connected and read-out performed, the value of the register and the read-out result may differ.

Serial interface

(1) If the bit data of SE2 changes while SCLK is in the master mode, a hazard will be output to the SCLK pin. If this poses a problem for the system, be sure to set the SCLK to the external clock if the bit data of SE2 is to be changed.

(2) Be sure that read-out of the interrupt factor flag (ISIO) is done only when the serial port is in the STOP status (SIOF = "0") and the DI status (interrupt flag = "0"). If read-out is performed while the serial data is in the RUN status (during input or output), the data input or output will be suspended and the initial status resumed. Read-out during the EI status (interrupt flag = "1") causes malfunctioning.

(3) When using the serial interface in the master mode, the synchronous clock uses the CPU system clock. Accordingly, do not change the system clock ($f_{OSC1} \leftrightarrow f_{OSC3}$) while the serial interface is operating.

(4) Perform data writing/reading to data registers SD0–SD7 only while the serial interface is halted (i.e., the synchronous clock is neither being input or output).

(5) As a trigger condition, it is required that data writing or reading on data registers SD0–SD7 be performed prior to writing "1" to SCTRG. (The internal circuit of the serial interface is initiated through data writing/reading on data registers SD0–SD7.) Supply trigger only once every time the serial interface is placed in the RUN state. Moreover, when the synchronous clock SCLK is external clock, start to input the external clock after the trigger.

LCD driver

(1) When Page 0 is selected for the display memory, the memory data and the display will not match until the area is initialized (through, for instance, memory clear processing by the CPU). Initialize the display memory by executing initial processing.

(2) When Page 2 is selected for the display memory, that area becomes write-only. Consequently, data cannot be rewritten by arithmetic operations (such as AND, OR, ADD, SUB).

Clock timer

(1) The prescaler mode must be set correctly to suit the crystal oscillator to be used.

(2) When the clock timer has been reset, the interrupt factor flag (TI) may sometimes be set to "1". Consequently, perform flag read-out (reset the flag) as necessary at reset.

(3) The input clock of the watchdog timer is the 2 Hz signal of the clock timer, so that the watchdog timer may be counted up at timer reset.

Stopwatch timer

(1) The prescaler mode must be set correctly so that the stopwatch timer suits the crystal oscillator to be used.

(2) If timer data is read out in the RUN status, the timer must be made into the STOP status, and after data is read out the RUN status can be restored. If data is read out when a carry occurs, the data cannot be read correctly.
Also, the processing above must be performed within the STOP interval of 976 µsec (256 Hz 1/4 cycle).

Sound generator

A hazard may be observed in the output waveform of the BZ and $\overline{BZ}$ signals when data of the output registers (R10, R13) and the buzzer frequency selection registers (BZFQ0–BZFQ2) changes.

Event counter

(1) After the event counter has written data to the EVRUN register, it operates or stops in synchronization with the falling edge of the noise rejector clock or stops. Hence, attention must be paid to the above timing when input signals (input to K02 and K03) are being received.

(2) To prevent erroneous reading of the event counter data, read out the counter data several times, compare it, and use the matching data as the result.

Analog comparator

(1) To reduce current consumption, set the analog comparator to OFF when it is not necessary.

(2) After setting AMPON to "1", wait at least 3 msec for the operation of the analog comparator to stabilize before reading the output data of the analog comparator from AMPDT.

Battery life detection (BLD) circuit

(1) It takes 100 µsec from the time the BLD circuit goes ON until a stable result is obtained. For this reason, keep the following software notes in mind:

When the CPU system clock is f_{OSC1}

1. When detection is done at HLMOD
   After writing "1" on HLMOD, read the BLD after 1 instruction has passed.
2. When detection is done at BLS
   After writing "1" on BLS, write "0" after at least 100 µsec has lapsed (possible with the next instruction) and then read the BLD.

When the CPU system clock is fOSC3 (in case of E0C60A08 only)

1. When detection is done at HLMOD
   After writing "1" on HLMOD, read the BLD after 0.6 second has passed. (HLMOD holds "1" for at least 0.6 second)
2. When detection is done at BLS
   Before writing "1" on BLS, write "1" on HLMOD first; after at least 100 µsec has lapsed after writing "1" on BLS, write "0" on BLS and then read the BLD.

(2) BLS resides in the same bit at the same address as BLD1, and one or the other is selected by write or read operation. This means that arithmetic operations (AND, OR, ADD, SUB and so forth) cannot be used for BLS control.

Heavy load protection function and sub-BLD circuit

(1) It takes 100 µsec from the time the BLD circuit goes ON until a stable result is obtained. For this reason, keep the following software notes in mind:

When the CPU system clock is fOSC1

1. When detection is done at HLMOD
   After writing "1" on HLMOD, read the BLD after 1 instruction has passed.
2. When detection is done at BLS
   After writing "1" on BLS, write "0" after at least 100 µsec has lapsed (possible with the next instruction) and then read the BLD.

When the CPU system clock is fOSC3 (in case of E0C60A08 only)

1. When detection is done at HLMOD
   After writing "1" on HLMOD, read the BLD after 0.6 second has passed. (HLMOD holds "1" for at least 0.6 second)
2. When detection is done at BLS
   Before writing "1" on BLS, write "1" on HLMOD first; after at least 100 µsec has lapsed after writing "1" on BLS, write "0" on BLS and then read the BLD.

(2) BLS resides in the same bit at the same address as BLD1, and one or the other is selected by write or read operation. This means that arithmetic operations (AND, OR, ADD, SUB and so forth) cannot be used for BLS control.

(3) Select one of the following software processing to return to the normal mode after a heavy load has been driven in the heavy load protection mode in the E0C60L08.

① After heavy load drive is completed, return to the normal mode after at least one second has elapsed.

② After heavy load drive is completed, switch BLS ON and OFF (at least 100 µsec is necessary for the ON status) and then return to the normal mode.

The E0C6008/60A08 returns to the normal mode after driving a heavy load without special software processing.

(4) If the BLS is set to ON while the heavy load protection mode is in effect, keep the ON time within 10 msec.

Interrupt and HALT

(1) When the interrupt mask register (EIK) is set to "0", the interrupt factor flag (IK) of the input port cannot be set even though the terminal status of the input port has changed.

(2) The interrupt factor flags of the clock timer, stopwatch timer and serial interface (TI, SWIT, ISIO) are set when the timing condition is established, even if the interrupt mask registers (ETI, EISWIT, EISIO) are set to "0".

(3) Read out the interrupt factor flags only in the DI status (interrupt flag = "0"). If read-out is performed in the EI status (interrupt flag = "1") a malfunction will result.

(4) Writing to the interrupt mask register only in the DI status (interrupt flag = "0"). Writing to the interrupt mask register while in the EI status (interrupt flag = "1") may cause mulfunction.

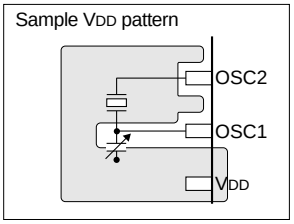
5.3 Precautions on Mounting

<Oscillation Circuit>

- Oscillation characteristics change depending on conditions (board pattern, components used, etc.). In particular, when using a crystal oscillator, use the oscillator manufacturer's recommended values for constants such as capacitance and resistance.
- Disturbances of the oscillation clock due to noise may cause a malfunction. Consider the following points to prevent this:

  (1) Components which are connected to the OSC1, OSC2, OSC3 and OSC4 terminals, such as oscillators, resistors and capacitors, should be connected in the shortest line.

  (2) As shown in the right hand figure, make a VDD pattern as large as possible at circumscription of the OSC1/OSC3 and OSC2/OSC4 terminals and the components connected to these terminals. Furthermore, do not use this VDD pattern for any purpose other than the oscillation system.



- In order to prevent unstable operation of the oscillation circuit due to current leak between OSC1/OSC3 and VSS, please keep enough distance between OSC1/OSC3 and VSS or other signals on the board pattern.

<Reset Circuit>

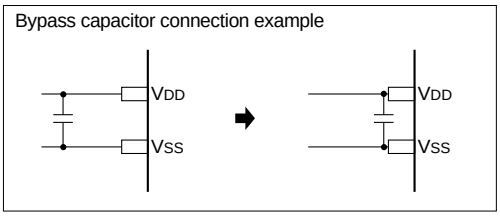
- The power-on reset signal which is input to the RESET terminal changes depending on conditions (power rise time, components used, board pattern, etc.).
  Decide the time constant of the capacitor and resistor after enough tests have been completed with the application product.
  When the built-in pull-down resistor is added to the RESET terminal by mask option, take into consideration dispersion of the resistance for setting the constant.
- In order to prevent any occurrences of unnecessary resetting caused by noise during operating, components such as capacitors and resistors should be connected to the RESET terminal in the shortest line.

<Power Supply Circuit>

- Sudden power supply variation due to noise may cause malfunction. Consider the following points to prevent this:

  (1) The power supply should be connected to the VDD and VSS terminal with patterns as short and large as possible.

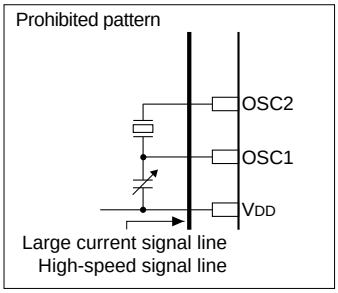
  (2) When connecting between the VDD and VSS terminals with a bypass capacitor, the terminals should be connected as short as possible.



  (3) Components which are connected to the VS1, VL1, VL2, VL3 terminals, such as a capacitor, should be connected in the shortest line.

<Arrangement of Signal Lines>

- In order to prevent generation of electromagnetic induction noise caused by mutual inductance, do not arrange a large current signal line near the circuits that are sensitive to noise such as the oscillation unit.
- When a signal line is parallel with a high-speed line in long distance or intersects a high-speed line, noise may generated by mutual interference between the signals and it may cause a malfunction. Do not arrange a high-speed signal line especially near circuits that are sensitive to noise such as the oscillation unit.



<Precautions for Visible Radiation (when bare chip is mounted)>

- Visible radiation causes semiconductor devices to change the electrical characteristics. It may cause this IC to malfunction. When developing products which use this IC, consider the following precautions to prevent malfunctions caused by visible radiations.

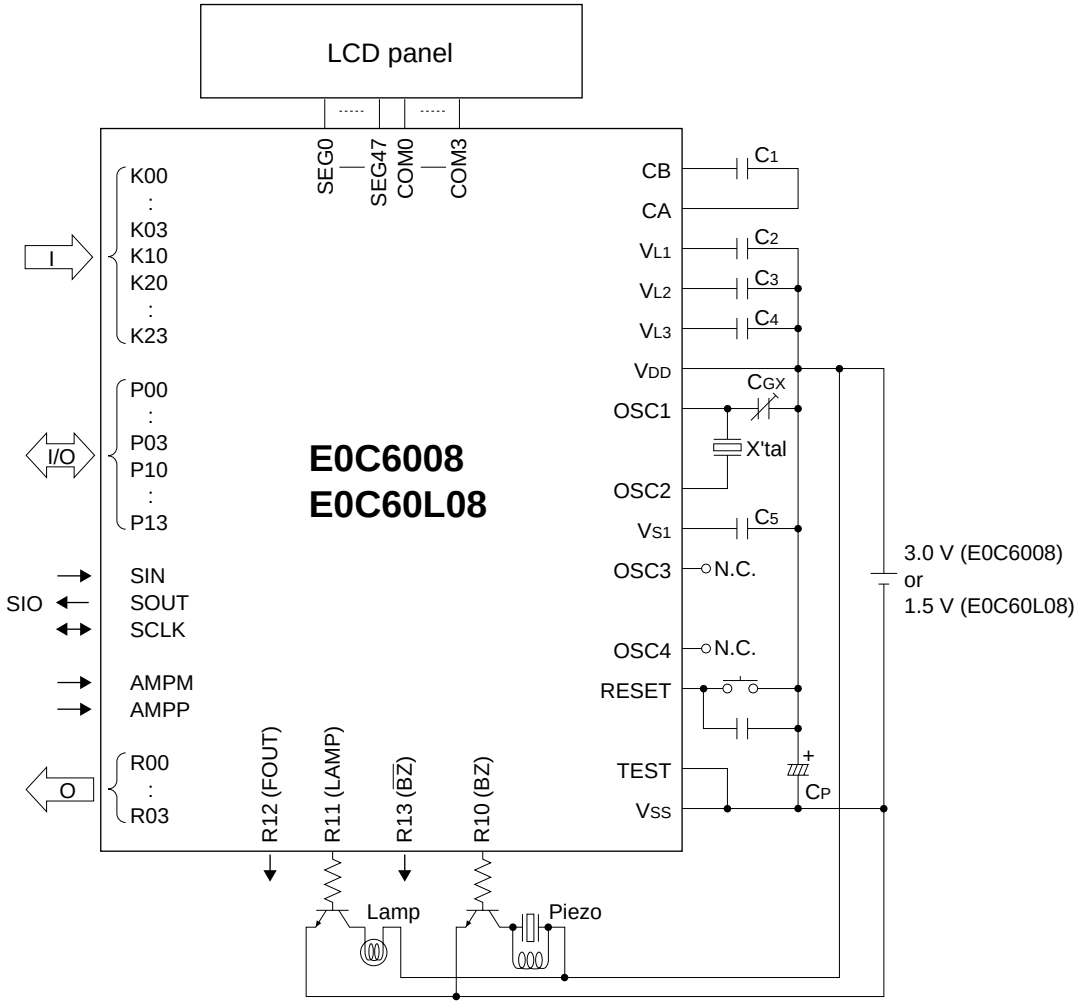
  (1) Design the product and implement the IC on the board so that it is shielded from visible radiation in actual use.

  (2) The inspection process of the product needs an environment that shields the IC from visible radiation.

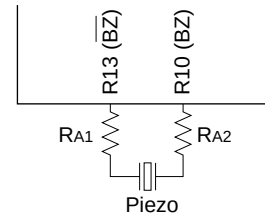
  (3) As well as the face of the IC, shield the back and side too.

CHAPTER 6 BASIC EXTERNAL WIRING DIAGRAM

E0C6008 and E0C60L08



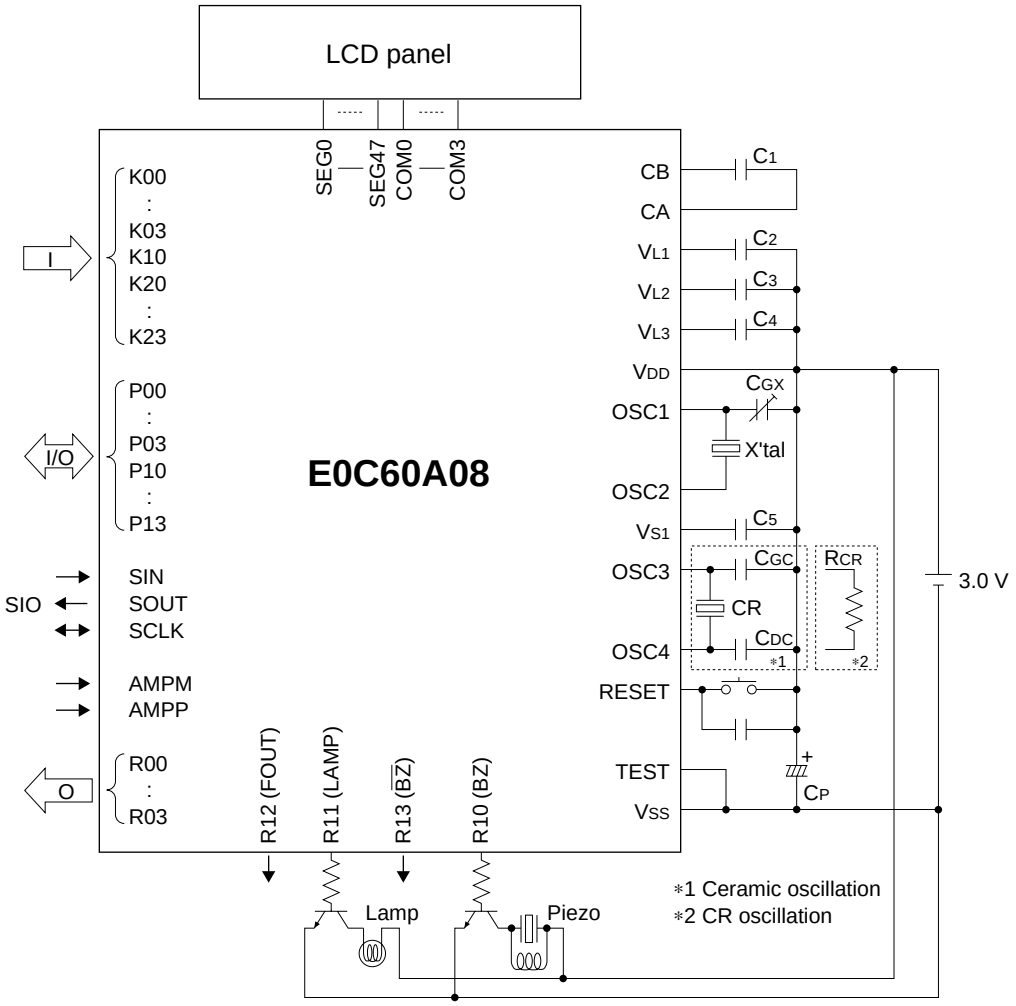
X'tal	Crystal oscillator	32.768 kHz or 38.400 kHz, C_I = 35 kΩ
C_{GX}	Trimmer capacitor	5–25 pF
C_1	Capacitor	0.1 µF
C_2	Capacitor	0.1 µF
C_3	Capacitor	0.1 µF
C_4	Capacitor	0.1 µF
C_5	Capacitor	0.1 µF
C_P	Capacitor	3.3 µF
R_{A1}	Protection resistor	100 Ω
R_{A2}	Protection resistor	100 Ω



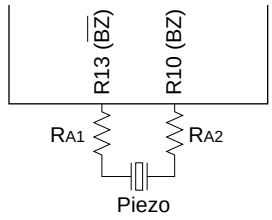
When the piezoelectric buzzer is driven directly

Note: The above table is simply an example, and is not guaranteed to work.

E0C60A08



X'tal	Crystal oscillator	32.768 kHz or 38.400 kHz, C_I = 35 kΩ
C_{GX}	Trimmer capacitor	5–25 pF
CR	Ceramic oscillator	500 kHz
C_{GC}	Gate capacitor	100 pF
C_{DC}	Drain capacitor	100 pF
R_{CR}	Resistor for CR oscillation	82 kΩ
C_1	Capacitor	0.1 µF
C_2	Capacitor	0.1 µF
C_3	Capacitor	0.1 µF
C_4	Capacitor	0.1 µF
C_5	Capacitor	0.1 µF
C_P	Capacitor	3.3 µF
R_{A1}	Protection resistor	100 Ω
R_{A2}	Protection resistor	100 Ω



When the piezoelectric buzzer is driven directly

Note: The above table is simply an example, and is not guaranteed to work.

CHAPTER 7 ELECTRICAL CHARACTERISTICS

7.1 Absolute Maximum Rating

E0C6008 and E0C60A08

(V_{DD}=0V)

Item	Symbol	Rated value	Unit
Supply voltage	V_{SS}	-5.0 to 0.5	V
Input voltage (1)	V_I	V_{SS}-0.3 to 0.5	V
Input voltage (2)	V_{IOSC}	V_{S1}-0.3 to 0.5	V
Permissible total output current *1	ΣI_{VSS}	10	mA
Operating temperature	Topr	-20 to 70	°C
Storage temperature	Tstg	-65 to 150	°C
Soldering temperature / time	Tsol	260°C, 10sec (lead section)	–
Permissible dissipation *2	P_D	250	mW

*1 The permissible total output current is the sum total of the current (average current) that simultaneously flows from the output pin (or is drawn in).

*2 In case of plastic package.

E0C60L08

(V_{DD}=0V)

Item	Symbol	Rated value	Unit
Supply voltage	V_{SS}	-2.0 to 0.5	V
Input voltage (1)	V_I	V_{SS}-0.3 to 0.5	V
Input voltage (2)	V_{IOSC}	V_{S1}-0.3 to 0.5	V
Permissible total output current *1	ΣI_{VSS}	10	mA
Operating temperature	Topr	-20 to 70	°C
Storage temperature	Tstg	-65 to 150	°C
Soldering temperature / time	Tsol	260°C, 10sec (lead section)	–
Permissible dissipation *2	P_D	250	mW

*1 The permissible total output current is the sum total of the current (average current) that simultaneously flows from the output pin (or is drawn in).

*2 In case of plastic package.

7.2 Recommended Operating Conditions

E0C6008

(Ta=-20 to 70°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply voltage	V_{SS}	V_{DD}=0V	-3.5	-3.0	-1.8	V
Oscillation frequency	f_{OSC1}	Either one is selected	–	32.768	–	kHz
			–	38.400	–	kHz

E0C60L08

(Ta=-20 to 70°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply voltage	V_{SS}	V_{DD}=0V	-1.7	-1.5	-1.1	V
		V_{DD}=0V, with software control *1	-1.7	-1.5	-0.9 *2	V
		V_{DD}=0V, when analog comparator is used	-1.7	-1.5	-1.2	V
Oscillation frequency	f_{OSC1}	Either one is selected	–	32.768	–	kHz
			–	38.400	–	kHz

*1 When switching to heavy load protection mode. (See Section 4.15 for details.)

*2 The possibility of LCD panel display differs depending on the characteristics of the LCD panel.

E0C60A08

(Ta=-20 to 70°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply voltage	V_{SS}	V_{DD}=0V	-3.5	-3.0	-2.2	V
Oscillation frequency (1)	f_{OSC1}	Either one is selected	–	32.768	–	kHz
			–	38.400	–	kHz
Oscillation frequency (2)	f_{OSC3}	duty 50±5%	50	500	600	kHz

7.3 DC Characteristics

E0C6008 and E0C60A08

Unless otherwise specified:
V_{DD}=0V, V_{SS}=-3.0V, f_{OSC1}=32.768kHz, Ta=25°C, V_{S1}/V_{L1}–V_{L3} are internal voltage, C_1–C_5=0.1µF

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
High level input voltage (1)	V_{IH1}		K00–03, K10, K20–23, P00–03 P10–13, SIN	0.2·Vss		0	V
High level input voltage (2)	V_{IH2}		SCLK, RESET, TEST	0.1·Vss		0	V
Low level input voltage (1)	V_{IL1}		K00–03, K10, K20–23, P00–03 P10–13, SIN	Vss		0.8·Vss	V
Low level input voltage (2)	V_{IL2}		SCLK, RESET, TEST	Vss		0.9·Vss	V
High level input current (1)	I_{IH1}	V_{IH1}=0V No pull-down	K00–03, K10, K20–23, P00–03 P10–13, SIN, SCLK, AMPP AMPM, RESET	0		0.5	µA
High level input current (2)	I_{IH2}	V_{IH2}=0V With pull-down	K00–03, K10, K20–23, SIN SCLK	4		16	µA
High level input current (3)	I_{IH3}	V_{IH3}=0V With pull-down	P00–03, P10–13, RESET, TEST	25		100	µA
Low level input current	I_{IL}	V_{IL}=Vss	K00–03, K10, K20–23, P00–03 P10–13, SIN, SCLK, AMPP AMPM, RESET, TEST	-0.5		0	µA
High level output current (1)	I_{OH1}	V_{OH1}=0.1·Vss	R10, R11, R13			-1.8	mA
High level output current (2)	I_{OH2}	V_{OH2}=0.1·Vss	R00–03, R12, P00–03, P10–13 SOUT, SCLK			-0.9	mA
Low level output current (1)	I_{OL1}	V_{OL1}=0.9·Vss	R10, R11, R13	6.0			mA
Low level output current (2)	I_{OL2}	V_{OL2}=0.9·Vss	R00–03, R12, P00–03, P10–13 SOUT, SCLK	3.0			mA
Common output current	I_{OH3}	V_{OH3}=-0.05V	COM0–3			-3	µA
	I_{OL3}	V_{OL3}=V_{L3}+0.05V		3			µA
Segment output current (during LCD output)	I_{OH4}	V_{OH4}=-0.05V	SEG0–47			-3	µA
	I_{OL4}	V_{OL4}=V_{L3}+0.05V		3			µA
Segment output current (during DC output)	I_{OH5}	V_{OH5}=0.1·Vss	SEG0–47			-200	µA
	I_{OL5}	V_{OL5}=0.9·Vss		200			µA

E0C60L08

Unless otherwise specified:
V_{DD}=0V, V_{SS}=-1.5V, f_{OSC1}=32.768kHz, Ta=25°C, V_{S1}/V_{L1}–V_{L3} are internal voltage, C_1–C_5=0.1µF

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
High level input voltage (1)	V_{IH1}		K00–03, K10, K20–23, P00–03 P10–13, SIN	0.2·Vss		0	V
High level input voltage (2)	V_{IH2}		SCLK, RESET, TEST	0.1·Vss		0	V
Low level input voltage (1)	V_{IL1}		K00–03, K10, K20–23, P00–03 P10–13, SIN	Vss		0.8·Vss	V
Low level input voltage (2)	V_{IL2}		SCLK, RESET, TEST	Vss		0.9·Vss	V
High level input current (1)	I_{IH1}	V_{IH1}=0V No pull-down	K00–03, K10, K20–23, P00–03 P10–13, SIN, SCLK, AMPP AMPM, RESET	0		0.5	µA
High level input current (2)	I_{IH2}	V_{IH2}=0V With pull-down	K00–03, K10, K20–23, SIN SCLK	2		10	µA
High level input current (3)	I_{IH3}	V_{IH3}=0V With pull-down	P00–03, P10–13, RESET, TEST	12		60	µA
Low level input current	I_{IL}	V_{IL}=Vss	K00–03, K10, K20–23, P00–03 P10–13, SIN, SCLK, AMPP AMPM, RESET, TEST	-0.5		0	µA
High level output current (1)	I_{OH1}	V_{OH1}=0.1·Vss	R10, R11, R13			-300	µA
High level output current (2)	I_{OH2}	V_{OH2}=0.1·Vss	R00–03, R12, P00–03, P10–13 SOUT, SCLK			-150	µA
Low level output current (1)	I_{OL1}	V_{OL1}=0.9·Vss	R10, R11, R13	1400			µA
Low level output current (2)	I_{OL2}	V_{OL2}=0.9·Vss	R00–03, R12, P00–03, P10–13 SOUT, SCLK	700			µA
Common output current	I_{OH3}	V_{OH3}=-0.05V	COM0–3			-3	µA
	I_{OL3}	V_{OL3}=V_{L3}+0.05V		3			µA
Segment output current (during LCD output)	I_{OH4}	V_{OH4}=-0.05V	SEG0–47			-3	µA
	I_{OL4}	V_{OL4}=V_{L3}+0.05V		3			µA
Segment output current (during DC output)	I_{OH5}	V_{OH5}=0.1·Vss	SEG0–47			-100	µA
	I_{OL5}	V_{OL5}=0.9·Vss		100			µA

7.4 Analog Circuit Characteristics and Current Cinsumption

E0C6008 (Normal operating mode)

Unless otherwise specified:
V_{DD}=0V, V_{SS}=-3.0V, f_{OSC1}=32.768kHz, Ta=25°C, C_G=25pF, V_{S1}/V_{L1}–V_{L3} are internal voltage, C_1–C_5=0.1µF

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
LCD drive voltage	V_{L1}	Connect 1 MΩ load resistor between V_{DD} and V_{L1} (without panel load)		1/2·V_{L2} - 0.1		1/2·V_{L2} ×0.9	V
	V_{L2}	Connect 1 MΩ load resistor between V_{DD} and V_{L2} (without panel load)		-2.30	-2.10	-1.90	V
	V_{L3}	Connect 1 MΩ load resistor between V_{DD} and V_{L3} (without panel load)		3/2·V_{L2} - 0.1		3/2·V_{L2} ×0.9	V
BLD voltage *1	V_{B0}	BLC="0"		-2.35	-2.20	-2.05	V
	V_{B1}	BLC="1"		-2.40	-2.25	-2.10	V
	V_{B2}	BLC="2"		-2.45	-2.30	-2.15	V
	V_{B3}	BLC="3"		-2.50	-2.35	-2.20	V
	V_{B4}	BLC="4"		-2.55	-2.40	-2.25	V
	V_{B5}	BLC="5"		-2.60	-2.45	-2.30	V
	V_{B6}	BLC="6"		-2.65	-2.50	-2.35	V
	V_{B7}	BLC="7"		-2.70	-2.55	-2.40	V
BLD circuit response time	t_B					100	µsec
Sub-BLD voltage	V_{BS}			-2.55	-2.40	-2.25	V
Sub-BLD circuit response time	t_{BS}					100	µsec
Analog comparator input voltage	V_{IP}	Non-inverted input (AMPP)		V_{SS}+0.3		V_{DD}-0.9	V
	V_{IM}	Inverted input (AMPM)					
Analog comparator offset voltage	V_{OF}					10	mV
Analog comparator response time	t_{AMP}	V_{IP}=-1.5V V_{IM}=V_{IP}±15mV				3	msec
Current consumption	I_{OP}	During HALT	Without panel load		1.0	2.0	µA
		During operation *2			2.2	4.0	µA

*1 The relationships among V_{B0}–V_{B7} are V_{B0}>V_{B1}>V_{B2}>...V_{B5}>V_{B6}>V_{B7}.
*2 The BLD circuit, sub-BLD circuit and analog comparator are in the OFF status.

E0C6008 (Heavy load protection mode)

Unless otherwise specified:
V_{DD}=0V, V_{SS}=-3.0V, f_{OSC1}=32.768kHz, Ta=25°C, C_G=25pF, V_{S1}/V_{L1}–V_{L3} are internal voltage, C_1–C_5=0.1µF

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
LCD drive voltage	V_{L1}	Connect 1 MΩ load resistor between V_{DD} and V_{L1} (without panel load)		1/2·V_{L2} - 0.1		1/2·V_{L2} ×0.9	V
	V_{L2}	Connect 1 MΩ load resistor between V_{DD} and V_{L2} (without panel load)		-2.30	-2.10	-1.90	V
	V_{L3}	Connect 1 MΩ load resistor between V_{DD} and V_{L3} (without panel load)		3/2·V_{L2} - 0.1		3/2·V_{L2} ×0.9	V
BLD voltage *1	V_{B0}	BLC="0"		-2.35	-2.20	-2.05	V
	V_{B1}	BLC="1"		-2.40	-2.25	-2.10	V
	V_{B2}	BLC="2"		-2.45	-2.30	-2.15	V
	V_{B3}	BLC="3"		-2.50	-2.35	-2.20	V
	V_{B4}	BLC="4"		-2.55	-2.40	-2.25	V
	V_{B5}	BLC="5"		-2.60	-2.45	-2.30	V
	V_{B6}	BLC="6"		-2.65	-2.50	-2.35	V
	V_{B7}	BLC="7"		-2.70	-2.55	-2.40	V
BLD circuit response time	t_B					100	µsec
Sub-BLD voltage	V_{BS}			-2.55	-2.40	-2.25	V
Sub-BLD circuit response time	t_{BS}					100	µsec
Analog comparator input voltage	V_{IP}	Non-inverted input (AMPP)		V_{SS}+0.3		V_{DD}-0.9	V
	V_{IM}	Inverted input (AMPM)					
Analog comparator offset voltage	V_{OF}					10	mV
Analog comparator response time	t_{AMP}	V_{IP}=-1.5V V_{IM}=V_{IP}±15mV				3	msec
Current consumption	I_{OP}	During HALT	Without panel load		10	20	µA
		During operation *2			12	25	µA

*1 The relationships among V_{B0}–V_{B7} are V_{B0}>V_{B1}>V_{B2}>...V_{B5}>V_{B6}>V_{B7}.
*2 The BLD circuit and sub-BLD circuit are in the ON status (HLMOD="1", BLS="0").
The analog comparator is in the OFF status.

E0C60L08 (Normal operating mode)

Unless otherwise specified:
V_{DD}=0V, V_{SS}=-1.5V, f_{OSC1}=32.768kHz, Ta=25°C, C_G=25pF, V_{S1}/V_{L1}–V_{L3} are internal voltage, C_1–C_5=0.1µF

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
LCD drive voltage	V_{L1}	Connect 1 MΩ load resistor between V_{DD} and V_{L1} (without panel load)		-1.15	-1.05	-0.95	V
	V_{L2}	Connect 1 MΩ load resistor between V_{DD} and V_{L2} (without panel load)		$2 \cdot V_{L1}$ - 0.1		$2 \cdot V_{L1}$ ×0.9	V
	V_{L3}	Connect 1 MΩ load resistor between V_{DD} and V_{L3} (without panel load)		$3 \cdot V_{L1}$ - 0.1		$3 \cdot V_{L1}$ ×0.9	V
BLD voltage *1	V_{B0}	BLC="0"		-1.15	-1.05	-0.95	V
	V_{B1}	BLC="1"		-1.20	-1.10	-1.00	V
	V_{B2}	BLC="2"		-1.25	-1.15	-1.05	V
	V_{B3}	BLC="3"		-1.30	-1.20	-1.10	V
	V_{B4}	BLC="4"		-1.35	-1.25	-1.15	V
	V_{B5}	BLC="5"		-1.40	-1.30	-1.20	V
	V_{B6}	BLC="6"		-1.45	-1.35	-1.25	V
	V_{B7}	BLC="7"		-1.50	-1.40	-1.30	V
BLD circuit response time	t_B					100	µsec
Sub-BLD voltage	V_{BS}			-1.30	-1.20	-1.10	V
Sub-BLD circuit response time	t_{BS}					100	µsec
Analog comparator input voltage	V_{IP}	Non-inverted input (AMPP)		V_{SS}+0.3		V_{DD}-0.9	V
	V_{IM}	Inverted input (AMPM)					
Analog comparator offset voltage	V_{OF}					20	mV
Analog comparator response time	t_{AMP}	V_{IP}=-1.1V V_{IM}=V_{IP}±30mV				3	msec
Current consumption	I_{OP}	During HALT	Without panel load		1.0	2.0	µA
		During operation *2			2.2	4.0	µA

*1 The relationships among V_{B0}–V_{B7} are V_{B0}>V_{B1}>V_{B2}>...V_{B5}>V_{B6}>V_{B7}.

*2 The BLD circuit, sub-BLD circuit and analog comparator are in the OFF status.

E0C60L08 (Heavy load protection mode)

Unless otherwise specified:
V_{DD}=0V, V_{SS}=-1.5V, f_{OSC1}=32.768kHz, Ta=25°C, C_G=25pF, V_{S1}/V_{L1}–V_{L3} are internal voltage, C_1–C_5=0.1µF

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
LCD drive voltage	V_{L1}	Connect 1 MΩ load resistor between V_{DD} and V_{L1} (without panel load)		-1.15	-1.05	-0.95	V
	V_{L2}	Connect 1 MΩ load resistor between V_{DD} and V_{L2} (without panel load)		$2 \cdot V_{L1}$ - 0.1		$2 \cdot V_{L1}$ ×0.85	V
	V_{L3}	Connect 1 MΩ load resistor between V_{DD} and V_{L3} (without panel load)		$3 \cdot V_{L1}$ - 0.1		$3 \cdot V_{L1}$ ×0.85	V
BLD voltage *1	V_{B0}	BLC="0"		-1.15	-1.05	-0.95	V
	V_{B1}	BLC="1"		-1.20	-1.10	-1.00	V
	V_{B2}	BLC="2"		-1.25	-1.15	-1.05	V
	V_{B3}	BLC="3"		-1.30	-1.20	-1.10	V
	V_{B4}	BLC="4"		-1.35	-1.25	-1.15	V
	V_{B5}	BLC="5"		-1.40	-1.30	-1.20	V
	V_{B6}	BLC="6"		-1.45	-1.35	-1.25	V
	V_{B7}	BLC="7"		-1.50	-1.40	-1.30	V
BLD circuit response time	t_B					100	µsec
Sub-BLD voltage	V_{BS}			-1.30	-1.20	-1.10	V
Sub-BLD circuit response time	t_{BS}					100	µsec
Analog comparator input voltage	V_{IP}	Non-inverted input (AMPP)		V_{SS}+0.3		V_{DD}-0.9	V
	V_{IM}	Inverted input (AMPM)					
Analog comparator offset voltage	V_{OF}					20	mV
Analog comparator response time	t_{AMP}	V_{IP}=-1.1V V_{IM}=V_{IP}±30mV				3	msec
Current consumption	I_{OP}	During HALT	Without panel load		6.5	10	µA
		During operation *2			8.5	15	µA

*1 The relationships among V_{B0}–V_{B7} are V_{B0}>V_{B1}>V_{B2}>...V_{B5}>V_{B6}>V_{B7}.

*2 The BLD circuit and sub-BLD circuit are in the ON status (HLMOD="1", BLS="0").
The analog comparator is in the OFF status.

E0C60A08 (Normal operating mode)

Unless otherwise specified:
V_{DD}=0V, V_{SS}=-3.0V, f_{OSC1}=32.768kHz, Ta=25°C, C_G=25pF, V_{S1}/V_{L1}–V_{L3} are internal voltage, C_1–C_5=0.1µF

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
LCD drive voltage	V_{L1}	Connect 1 MΩ load resistor between V_{DD} and V_{L1} (without panel load)		-1.15	-1.05	-0.95	V
	V_{L2}	Connect 1 MΩ load resistor between V_{DD} and V_{L2} (without panel load)		2·V_{L1} - 0.1		2·V_{L1} ×0.9	V
	V_{L3}	Connect 1 MΩ load resistor between V_{DD} and V_{L3} (without panel load)		3·V_{L1} - 0.1		3·V_{L1} ×0.9	V
BLD voltage *1	V_{B0}	BLC="0"		-2.35	-2.20	-2.05	V
	V_{B1}	BLC="1"		-2.40	-2.25	-2.10	V
	V_{B2}	BLC="2"		-2.45	-2.30	-2.15	V
	V_{B3}	BLC="3"		-2.50	-2.35	-2.20	V
	V_{B4}	BLC="4"		-2.55	-2.40	-2.25	V
	V_{B5}	BLC="5"		-2.60	-2.45	-2.30	V
	V_{B6}	BLC="6"		-2.65	-2.50	-2.35	V
	V_{B7}	BLC="7"		-2.70	-2.55	-2.40	V
BLD circuit response time	t_B					100	µsec
Sub-BLD voltage	V_{BS}			-2.55	-2.40	-2.25	V
Sub-BLD circuit response time	t_{BS}					100	µsec
Analog comparator input voltage	V_{IP}	Non-inverted input (AMPP)		V_{SS}+0.3		V_{DD}-0.9	V
	V_{IM}	Inverted input (AMPM)					
Analog comparator offset voltage	V_{OF}					10	mV
Analog comparator response time	t_{AMP}	V_{IP}=-1.5V V_{IM}=V_{IP}±15mV				3	msec
Current consumption	I_{OP}	During HALT	Without panel load		1.1	2.0	µA
		During operation *2			3.0	5.0	µA
		During operation at 500kHz *2			50	70	µA

*1 The relationships among V_{B0}–V_{B7} are V_{B0}>V_{B1}>V_{B2}>...V_{B5}>V_{B6}>V_{B7}.

*2 The BLD circuit, sub-BLD circuit and analog comparator are in the OFF status.

E0C60A08 (Heavy load protection mode)

Unless otherwise specified:
V_{DD}=0V, V_{SS}=-3.0V, f_{OSC1}=32.768kHz, Ta=25°C, C_G=25pF, V_{S1}/V_{L1}–V_{L3} are internal voltage, C_1–C_5=0.1µF

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
LCD drive voltage	V_{L1}	Connect 1 MΩ load resistor between V_{DD} and V_{L1} (without panel load)		-1.15	-1.05	-0.95	V
	V_{L2}	Connect 1 MΩ load resistor between V_{DD} and V_{L2} (without panel load)		2·V_{L1} - 0.1		2·V_{L1} ×0.9	V
	V_{L3}	Connect 1 MΩ load resistor between V_{DD} and V_{L3} (without panel load)		3·V_{L1} - 0.1		3·V_{L1} ×0.9	V
BLD voltage *1	V_{B0}	BLC="0"		-2.35	-2.20	-2.05	V
	V_{B1}	BLC="1"		-2.40	-2.25	-2.10	V
	V_{B2}	BLC="2"		-2.45	-2.30	-2.15	V
	V_{B3}	BLC="3"		-2.50	-2.35	-2.20	V
	V_{B4}	BLC="4"		-2.55	-2.40	-2.25	V
	V_{B5}	BLC="5"		-2.60	-2.45	-2.30	V
	V_{B6}	BLC="6"		-2.65	-2.50	-2.35	V
	V_{B7}	BLC="7"		-2.70	-2.55	-2.40	V
BLD circuit response time	t_B					100	µsec
Sub-BLD voltage	V_{BS}			-2.55	-2.40	-2.25	V
Sub-BLD circuit response time	t_{BS}					100	µsec
Analog comparator input voltage	V_{IP}	Non-inverted input (AMPP)		V_{SS}+0.3		V_{DD}-0.9	V
	V_{IM}	Inverted input (AMPM)					
Analog comparator offset voltage	V_{OF}					10	mV
Analog comparator response time	t_{AMP}	V_{IP}=-1.5V V_{IM}=V_{IP}±15mV				3	msec
Current consumption	I_{OP}	During HALT	Without panel load		6.5	10	µA
		During operation *2			8.5	15	µA
		During operation at 500kHz *2			55	75	µA

*1 The relationships among V_{B0}–V_{B7} are V_{B0}>V_{B1}>V_{B2}>...V_{B5}>V_{B6}>V_{B7}.

*2 The BLD circuit and sub-BLD circuit are in the ON status (HLMOD="1", BLS="0").
The analog comparator is in the OFF status.

7.5 Oscillation Characteristics

The oscillation characteristics change depending on the conditions (components used, board pattern, etc.). Use the following characteristics as reference values.

E0C6008 (OSC1 crystal oscillation circuit)

Unless otherwise specified:
V_{DD}=0V, V_{SS}=-3.0V, Crystal: C-002R (C_I=35kΩ), C_G=25pF, C_D=built-in, Ta=25°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start voltage	Vsta	tsta≤5sec (V_{SS})	-1.8			V
Oscillation stop voltage	Vstp	tstp≤10sec (V_{SS})	-1.8			V
Built-in capacitance (drain)	C_D	Including the parasitic capacitance inside the chip		20		pF
Frequency/voltage deviation	Δf/ΔV	V_{SS}=-1.8 to -3.5V			5	ppm
Frequency/IC deviation	Δf/ΔIC		-10		10	ppm
Frequency adjustment range	Δf/ΔC_G	C_G=5 to 25pF	35	45		ppm
Harmonic oscillation start voltage	V_{hho}	(V_{SS})			-3.5	V
Permitted leak resistance	R_{leak}	Between OSC1 and V_{DD}	200			MΩ

E0C60L08 (OSC1 crystal oscillation circuit)

Unless otherwise specified:
V_{DD}=0V, V_{SS}=-1.5V, Crystal: C-002R (C_I=35kΩ), C_G=25pF, C_D=built-in, Ta=25°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start voltage	Vsta	tsta≤5sec (V_{SS})	-1.1			V
Oscillation stop voltage	Vstp	tstp≤10sec (V_{SS})	-1.1 (-0.9)*1			V
Built-in capacitance (drain)	C_D	Including the parasitic capacitance inside the chip		20		pF
Frequency/voltage deviation	Δf/ΔV	V_{SS}=-1.1 (-0.9)*1 to -1.7V			5	ppm
Frequency/IC deviation	Δf/ΔIC		-10		10	ppm
Frequency adjustment range	Δf/ΔC_G	C_G=5 to 25pF	35	45		ppm
Harmonic oscillation start voltage	V_{hho}	(V_{SS})			-1.7	V
Permitted leak resistance	R_{leak}	Between OSC1 and V_{DD}	200			MΩ

*1 Parentheses indicate value for operation in heavy load protection mode.

E0C60A08 (OSC1 crystal oscillation circuit)

Unless otherwise specified:
V_{DD}=0V, V_{SS}=-3.0V, Crystal: C-002R (C_I=35kΩ), C_G=25pF, C_D=built-in, Ta=25°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start voltage	Vsta	tsta≤5sec (V_{SS})	-2.2			V
Oscillation stop voltage	Vstp	tstp≤10sec (V_{SS})	-2.2			V
Built-in capacitance (drain)	C_D	Including the parasitic capacitance inside the chip		20		pF
Frequency/voltage deviation	Δf/ΔV	V_{SS}=-2.2 to -3.5V			5	ppm
Frequency/IC deviation	Δf/ΔIC		-10		10	ppm
Frequency adjustment range	Δf/ΔC_G	C_G=5 to 25pF	35	45		ppm
Harmonic oscillation start voltage	V_{hho}	(V_{SS})			-3.5	V
Permitted leak resistance	R_{leak}	Between OSC1 and V_{DD}	200			MΩ

E0C60A08 (OSC3 CR oscillation circuit)

Unless otherwise specified:
V_{DD}=0V, V_{SS}=-3.0V, R_{CR}=82kΩ, Ta=25°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation frequency dispersion	f_{OSC3}		-30	480kHz	30	%
Oscillation start voltage	Vsta	(V_{SS})	-2.2			V
Oscillation start time	tsta	V_{SS}=-2.2 to -3.5V			3	msec
Oscillation stop voltage	Vstp	(V_{SS})	-2.2			V

E0C60A08 (OSC3 ceramic oscillation circuit)

Unless otherwise specified:
V_{DD}=0V, V_{SS}=-3.0V, Ceramic oscillator: 500kHz, C_{GC}=C_{DC}=100pF, Ta=25°C

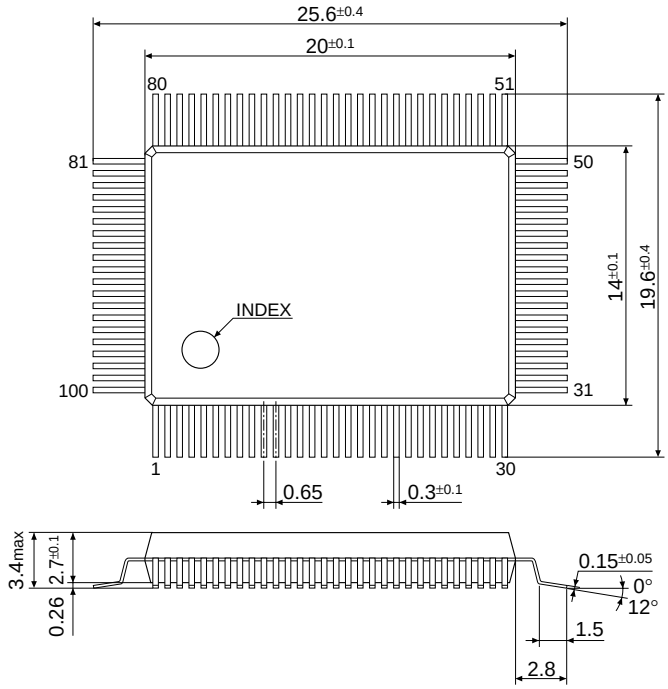
Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start voltage	Vsta	(V_{SS})	-2.2			V
Oscillation start time	tsta	V_{SS}=-2.2 to -3.5V			5	msec
Oscillation stop voltage	Vstp	(V_{SS})	-2.2			V

CHAPTER 8 PACKAGE

8.1 Plastic Package

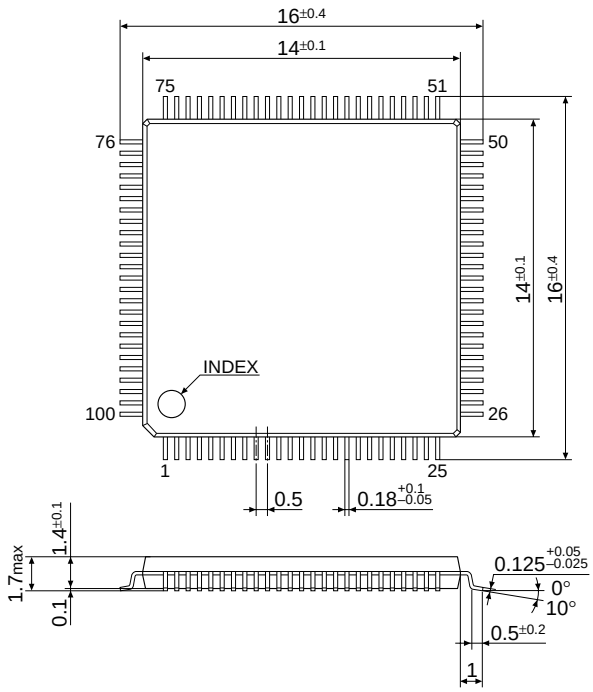
QFP5-100pin

(Unit: mm)



QFP15-100pin

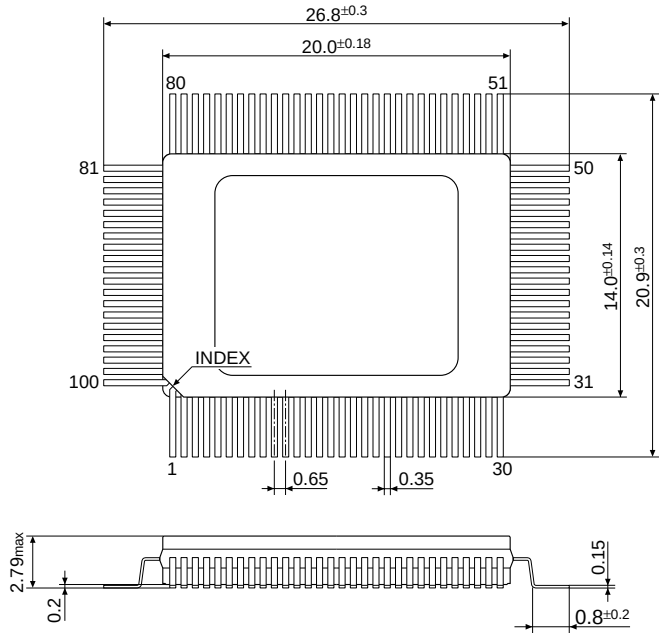
(Unit: mm)



8.2 Ceramic Package for Test Samples

QFP5-100pin

(Unit: mm)



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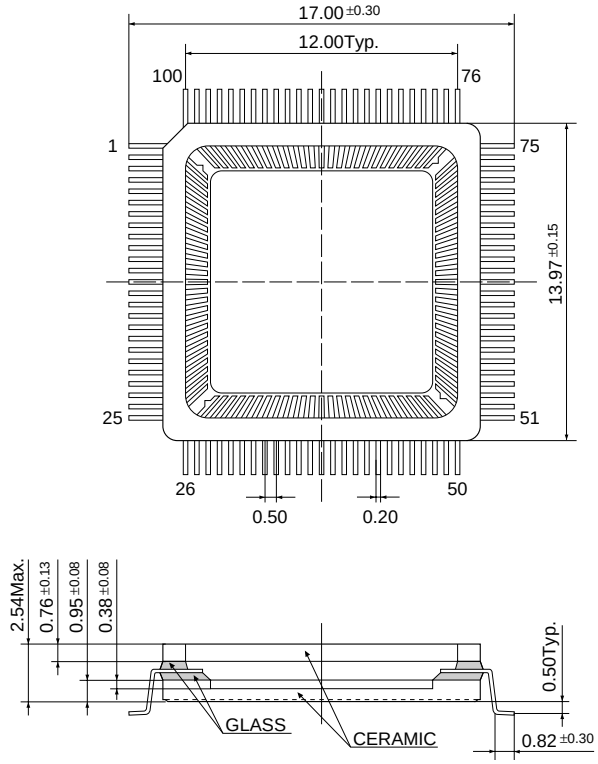
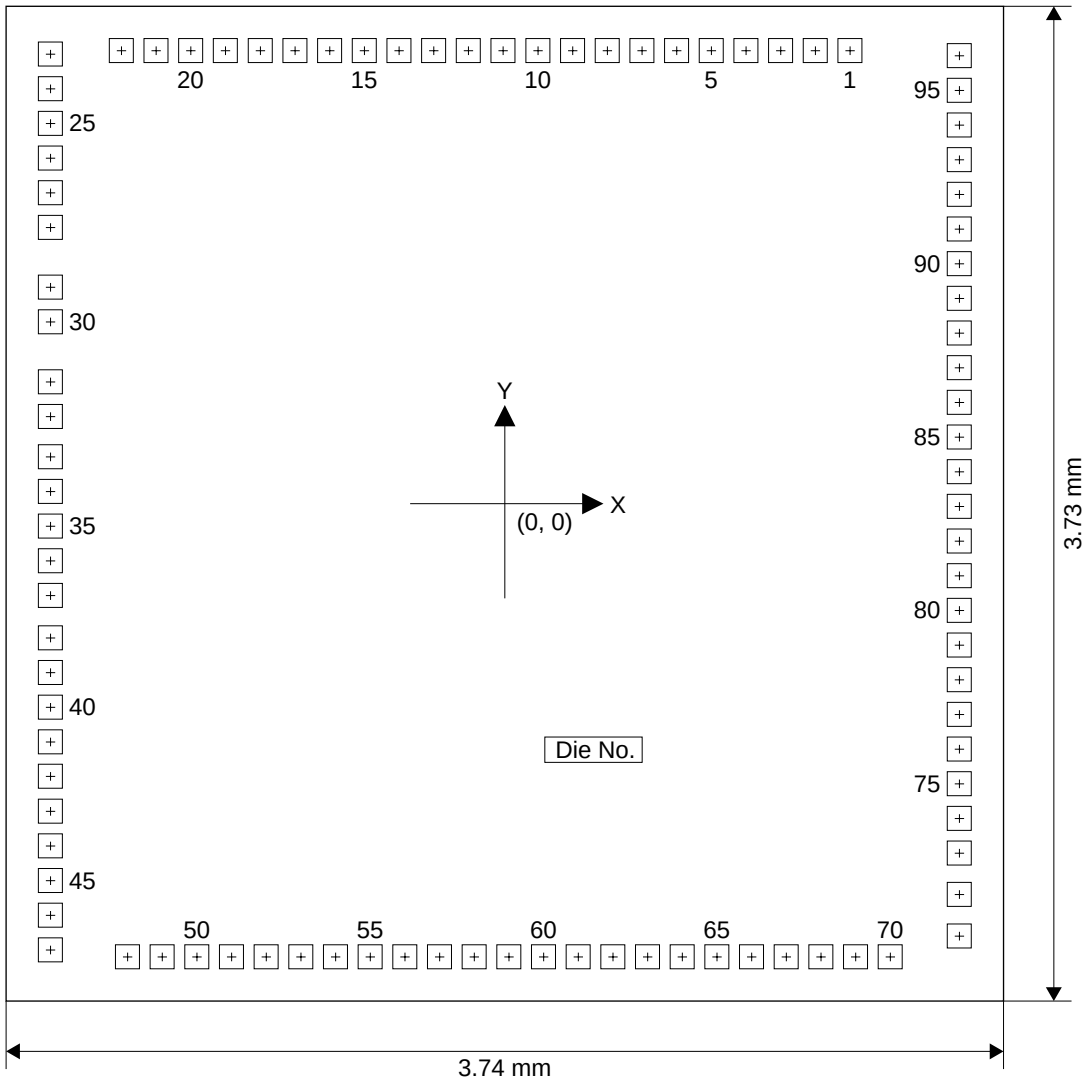
(Unit: mm)



CHAPTER 9 PAD LAYOUT

9.1 Diagram of Pad Layout



Chip thickness: 400µm
Pad opening: 95µm

9.2 Pad Coordinates

(Unit: µm)

No.	Pad name	X	Y	No.	Pad name	X	Y	No.	Pad name	X	Y
1	AMPP	1,294	1,699	33	OSC4	-1,704	176	65	SEG30	795	-1,699
2	AMPM	1,164	1,699	34	OSC3	-1,704	46	66	SEG29	925	-1,699
3	K23	1,034	1,699	35	V_{S1}	-1,704	-84	67	SEG28	1,055	-1,699
4	K22	904	1,699	36	OSC2	-1,704	-214	68	SEG27	1,185	-1,699
5	K21	774	1,699	37	OSC1	-1,704	-344	69	SEG26	1,315	-1,699
6	K20	644	1,699	38	V_{DD}	-1,704	-503	70	SEG25	1,445	-1,699
7	K10	514	1,699	39	V_{L3}	-1,704	-633	71	SEG24	1,704	-1,621
8	K03	384	1,699	40	V_{L2}	-1,704	-763	72	TEST	1,704	-1,465
9	K02	254	1,699	41	V_{L1}	-1,704	-893	73	SEG23	1,704	-1,310
10	K01	124	1,699	42	CA	-1,704	-1,022	74	SEG22	1,704	-1,180
11	K00	-7	1,699	43	CB	-1,704	-1,153	75	SEG21	1,704	-1,050
12	SIN	-137	1,699	44	COM3	-1,704	-1,283	76	SEG20	1,704	-920
13	SOUT	-267	1,699	45	COM2	-1,704	-1,413	77	SEG19	1,704	-790
14	SCLK	-397	1,699	46	COM1	-1,704	-1,543	78	SEG18	1,704	-660
15	P03	-527	1,699	47	COM0	-1,704	-1,673	79	SEG17	1,704	-530
16	P02	-657	1,699	48	SEG47	-1,415	-1,699	80	SEG16	1,704	-400
17	P01	-787	1,699	49	SEG46	-1,285	-1,699	81	SEG15	1,704	-270
18	P00	-917	1,699	50	SEG45	-1,155	-1,699	82	SEG14	1,704	-140
19	P13	-1,048	1,699	51	SEG44	-1,025	-1,699	83	SEG13	1,704	-10
20	P12	-1,178	1,699	52	SEG43	-895	-1,699	84	SEG12	1,704	120
21	P11	-1,308	1,699	53	SEG42	-765	-1,699	85	SEG11	1,704	250
22	P10	-1,438	1,699	54	SEG41	-635	-1,699	86	SEG10	1,704	380
23	R03	-1,704	1,686	55	SEG40	-505	-1,699	87	SEG9	1,704	510
24	R02	-1,704	1,556	56	SEG39	-375	-1,699	88	SEG8	1,704	640
25	R01	-1,704	1,426	57	SEG38	-245	-1,699	89	SEG7	1,704	770
26	R00	-1,704	1,296	58	SEG37	-115	-1,699	90	SEG6	1,704	900
27	R12	-1,704	1,166	59	SEG36	15	-1,699	91	SEG5	1,704	1,030
28	R11	-1,704	1,036	60	SEG35	145	-1,699	92	SEG4	1,704	1,160
29	R10	-1,704	812	61	SEG34	275	-1,699	93	SEG3	1,704	1,290
30	R13	-1,704	682	62	SEG33	405	-1,699	94	SEG2	1,704	1,420
31	V_{SS}	-1,704	457	63	SEG32	535	-1,699	95	SEG1	1,704	1,550
32	RESET	-1,704	327	64	SEG31	665	-1,699	96	SEG0	1,704	1,680

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