MF1190-01

EPSON

CMOS 4-BIT SINGLE CHIP MICROCOMPUTER

E0C6011 TECHNICAL MANUAL

E0C6011 Technical Hardware

ENERGY SAVING EPSON

SEIKO EPSON CORPORATION

CONTENTS

CHAPTER 1 INTRODUCTION

The E0C6011 single-chip microcomputer features an E0C6200B CMOS 4-bit CPU as the core. It contains a 1,536 (words) × 12 (bits) ROM, 144 (words) × 4 (bits) RAM, LCD driver, 4-bit input port (K00–K03), 4-bit output port (R00–R03), 8-bit I/O port (P00–P03, P10–P13) and a timer.

1.1 Features

Core CPU E0C6200B

Built-in oscillation circuit ..... CR oscillation circuit
Typ. 65 kHz, 130 kHz, 195 kHz or 260 kHz is selectable by mask option. (C, R built-in)

Instruction set ..... 101 instructions (supports SLEEP mode.)

ROM capacity ..... 1,536 words × 12 bits

RAM capacity ..... 144 words × 4 bits

Input port ..... 4 bits Pull-down resistors are available by mask option.

Output port ..... 4 bits Clock and buzzer outputs are selectable by mask option.

I/O port ..... 8 bits

LCD driver ..... 38 segments × 4, 3 or 2 commons
1/4, 1/3 or 1/2 duty and 1/3 bias for 4.5 V LCD panel or 1/2 bias for 3 V LCD panel are selectable by mask option.
LCD frame frequency (f_{OSC}/2,048 Hz, f_{OSC}/4,096 Hz, f_{OSC}/6,144 Hz or f_{OSC}/8,192 Hz) is selectable by software.

Time base counter ..... 1 system (clock timer) built-in

Interrupt ..... External: Input port interrupt 1 system
Internal: Timer interrupt 1 system

Reset input ..... Supports differential pulse reset.

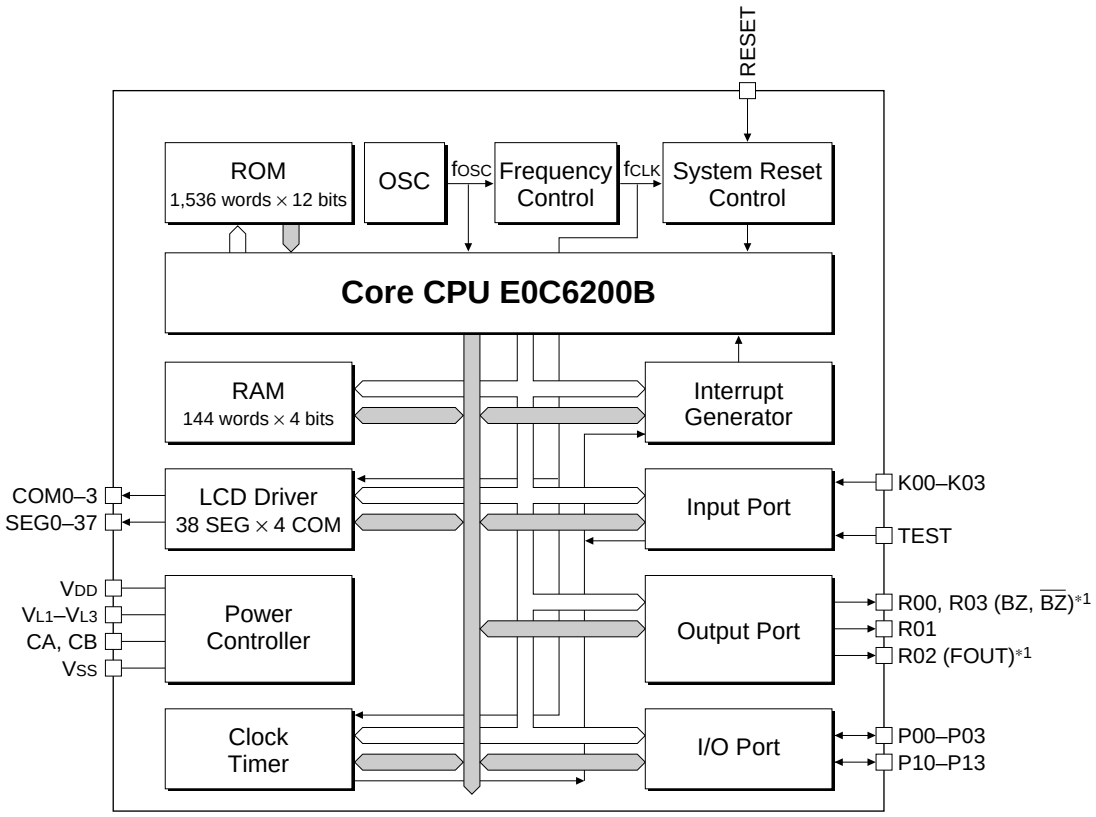
Supply voltage ..... 1.2 to 1.8 V

Current consumption .....

During SLEEP:	Max. 0.3 μA	
During HALT:	Typ. 4 μA	(65 kHz)
(without panel load)	Typ. 8 μA	(130 kHz)
	Typ. 11 μA	(195 kHz)
	Typ. 14 μA	(260 kHz)
During operation:	Typ. 8 μA	(65 kHz)
(without panel load)	Typ. 15 μA	(130 kHz)
	Typ. 20 μA	(195 kHz)
	Typ. 26 μA	(260 kHz)

Supply form ..... Die form, QFP5-80pin plastic package
or QFP14-80pin plastic package

1.2 Block Diagram

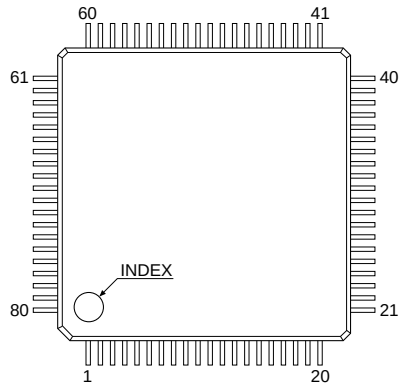


*1: Terminal specifications can be selected by mask option.

Fig. 1.2.1 E0C6011 block diagram

1.3 Pin Layout

QFP14-80pin

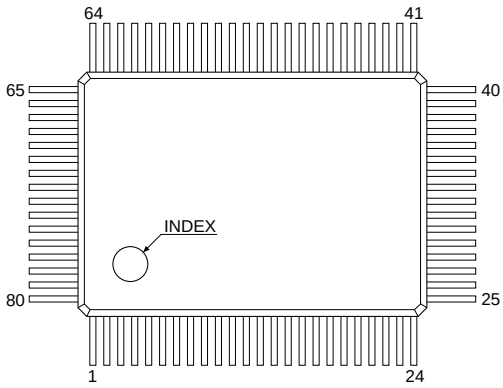


No.	Name	No.	Name	No.	Name	No.	Name
1	N.C.	21	SEG36	41	N.C.	61	N.C.
2	N.C.	22	N.C.	42	N.C.	62	SEG1
3	SEG19	23	N.C.	43	V_{SS}	63	SEG2
4	TEST	24	SEG37	44	RESET	64	SEG3
5	SEG20	25	K03	45	N.C.	65	SEG4
6	SEG21	26	K02	46	N.C.	66	SEG5
7	SEG22	27	K01	47	N.C.	67	SEG6
8	SEG23	28	K00	48	V_{DD}	68	SEG7
9	SEG24	29	P13	49	V_{L3}	69	SEG8
10	SEG25	30	P12	50	V_{L2}	70	SEG9
11	SEG26	31	P11	51	V_{L1}	71	SEG10
12	SEG27	32	P10	52	CB	72	SEG11
13	SEG28	33	P03	53	CA	73	SEG12
14	SEG29	34	P02	54	COM3	74	SEG13
15	SEG30	35	P01	55	COM2	75	SEG14
16	SEG31	36	P00	56	COM1	76	SEG15
17	SEG32	37	R02	57	COM0	77	SEG16
18	SEG33	38	R01	58	SEG0	78	SEG17
19	SEG34	39	R00	59	N.C.	79	SEG18
20	SEG35	40	R03	60	N.C.	80	N.C.

N.C. : No Connection

Fig. 1.3.1 Pin layout (QFP14-80pin)

QFP5-80pin



No.	Name	No.	Name	No.	Name	No.	Name
1	SEG35	21	R03	41	N.C.	61	N.C.
2	N.C.	22	N.C.	42	N.C.	62	N.C.
3	N.C.	23	N.C.	43	SEG1	63	N.C.
4	SEG36	24	N.C.	44	SEG2	64	SEG19
5	SEG37	25	V_{SS}	45	SEG3	65	TEST
6	K03	26	RESET	46	SEG4	66	SEG20
7	K02	27	N.C.	47	SEG5	67	SEG21
8	K01	28	N.C.	48	SEG6	68	SEG22
9	K00	29	N.C.	49	SEG7	69	SEG23
10	P13	30	V_{DD}	50	SEG8	70	SEG24
11	P12	31	V_{L3}	51	SEG9	71	SEG25
12	P11	32	V_{L2}	52	SEG10	72	SEG26
13	P10	33	V_{L1}	53	SEG11	73	SEG27
14	P03	34	CB	54	SEG12	74	SEG28
15	P02	35	CA	55	SEG13	75	SEG29
16	P01	36	COM3	56	SEG14	76	SEG30
17	P00	37	COM2	57	SEG15	77	SEG31
18	R02	38	COM1	58	SEG16	78	SEG32
19	R01	39	COM0	59	SEG17	79	SEG33
20	R00	40	SEG0	60	SEG18	80	SEG34

N.C. : No Connection

Fig. 1.3.2 Pin layout (QFP5-80pin)

1.4 Pin Description

Table 1.4.1 Pin description

Pin name	Pin No.		I/O	Function
	QFP14	QFP5		
V_{DD}	48	30	(I)	Power supply terminal (+)
V_{SS}	43	25	(I)	Power supply terminal (-)
$V_{L1–3}$	51–49	33–31	–	Power source for LCD
CA, CB	53, 52	35, 34	–	Booster capacitor connecting terminal
K00–03	28–25	9–6	I	Input port terminal
P00–03	36–33	17–14	I/O	I/O port terminal
P10–13	32–29	13–10	I/O	I/O port terminal
R00	39	20	O	Output port terminal (BZ output is selectable *)
R03	40	21	O	Output port terminal ($\overline{BZ}$ output is selectable *)
R01	38	19	O	Output port terminal
R02	37	18	O	Output port terminal (FOUT output is selectable *)
SEG0–37	58, 62–79, 3–21, 24	40, 43–60, 64, 66–80, 1, 4, 5	O	LCD segment output (DC output is selectable *)
COM0–3	57–54	39–36	O	LCD common output terminal (1/4, 1/3 or 1/2 duty are selectable *)
RESET	44	26	I	Initial reset input terminal
TEST	4	65	I	Test input terminal

∗ Can be selected by mask option

CHAPTER 2 POWER SUPPLY AND INITIAL RESET

2.1 Power Supply

With a single external power supply (∗) supplied to VDD through VSS, the E0C6011 generates the necessary internal voltages (<VL1–VL3> for driving LCD) with the internal power supply circuit.

∗ Supply voltage: 1.5 V (1.2 V to 1.8 V)

The internal power supply circuit is configured according to the LCD drive voltage specification selected by mask option. Figure 2.1.1 shows the configuration of the power supply circuit.

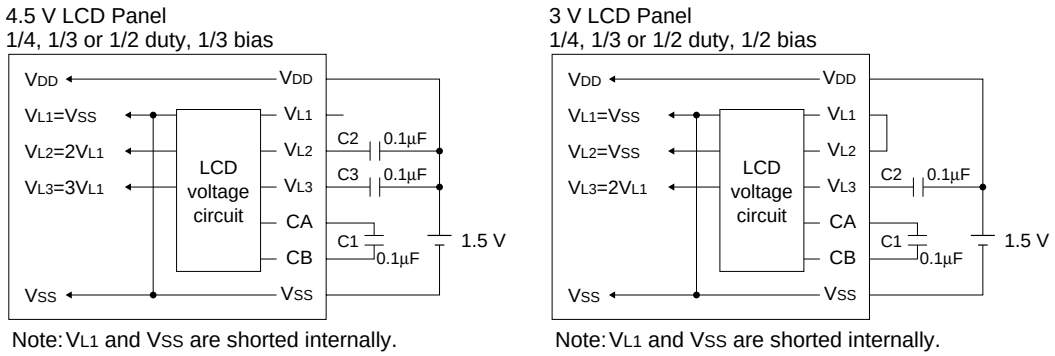


Fig. 2.1.1 Power supply configuration and external elements

Notes: • External loads cannot be driven by the output voltage of the internal power supply circuit.

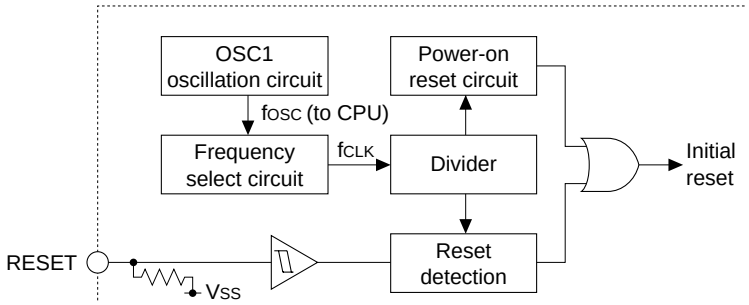
• See Chapter 6, "ELECTRICAL CHARACTERISTICS", for voltage values.

2.2 Initial Reset

To initialize the E0C6011 circuits, an initial reset must be executed. There are two ways of doing this.

(1) Initial reset by the power-on reset circuit
(2) External initial reset via the RESET terminal

Figure 2.2.1 shows the configuration of the initial reset circuit.



∗ fCLK is selectable from fosc Hz, fosc/2 Hz, fosc/3 Hz or fosc/4 Hz using the CLKFQ1–CLKFQ0 register.

Fig. 2.2.1 Configuration of initial reset circuit

2.2.1 Power-on reset circuit

The power-on reset circuit outputs the initial reset signal at power-on until the oscillation circuit starts oscillating.

Note: The power-on reset circuit may not work properly due to unstable or lower voltage input. The following initial reset method is recommended to generate the initial reset signal.

2.2.2 Reset terminal (RESET)

Initial reset can be executed externally by setting the reset terminal to a high level (VDD). There exists the external reset pulse detect circuit inside of the E0C6011. When this circuit detects the external reset signal, the internal reset signal turns high at the rising edge of the reset signal detect pulse. After about 10 msec (when fCLK = 65 kHz) has passed, the internal reset signal goes low to canceling the reset even if the external reset signal (RESET) keeps high level. An external reset must keep high level at least 1 msec (when fCLK = 65 kHz). Figure 2.2.2.1 shows the timing waveform of initial reset.

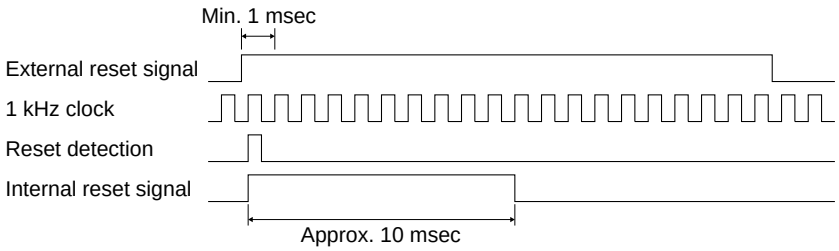


Fig. 2.2.2.1 Initial reset timing waveform

2.2.3 Internal register following initialization

An initial reset initializes the CPU as shown in the table below.

Table 2.2.3.1 Initial values

CPU Core			
Name	Symbol	Bit size	Initial value
Program counter step	PCS	8	00H
Program counter page	PCP	4	1H
New page pointer	NPP	4	1H
Stack pointer	SP	8	Undefined
Index register X	X	8	Undefined
Index register Y	Y	8	Undefined
Register pointer	RP	4	Undefined
General-purpose register A	A	4	Undefined
General-purpose register B	B	4	Undefined
Interrupt flag	I	1	0
Decimal flag	D	1	0
Zero flag	Z	1	Undefined
Carry flag	C	1	Undefined

Peripheral Circuits		
Name	Bit size	Initial value
RAM	4	Undefined
Display memory	4	Undefined
Other peripheral circuits	4	*

* See Section 4.1, "Memory Map".

2.3 Test Terminal (TEST)

This terminal is used when IC is inspected for shipment. During normal operation connect it to VSS or leave it open.

CHAPTER 3 CPU, ROM, RAM

3.1 CPU

The E0C6011 employs the E0C6200B core CPU, so that register configuration, instructions, and so forth are virtually identical to those in other processors in the family using the E0C6200/6200A/6200B. Refer to the "E0C6200/6200A Core CPU Manual" for details of the E0C6200B.

Note the following points with regard to the E0C6011:

(1) Since the E0C6011 provides the SLEEP function, the SLP instruction can be used.

(2) Because the ROM capacity is 1,536 words, 12 bits per word, bank bits are unnecessary, and PCB and NBP are not used.

(3) The RAM page is set to 0 only, so the page part (XP, YP) of the index register that specifies addresses is invalid.

```
PUSH XP    POP XP    LD XP,r    LD r,XP
PUSH YP    POP YP    LD YP,r    LD r,YP
```

3.2 ROM

The built-in ROM, a mask ROM for the program, has a capacity of 1,536 × 12-bit steps. The program area is 6 pages (0–5), each consisting of 256 steps (00H–FFH). After an initial reset, the program start address is set to page 1, step 00H. The interrupt vectors are allocated to page l, steps 01H–0FH.

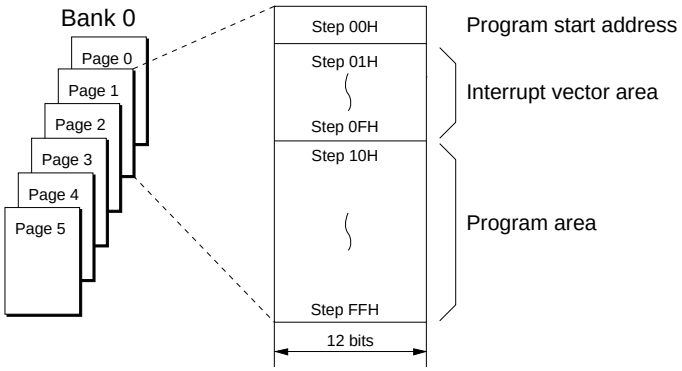


Fig. 3.2.1 ROM configuration

3.3 RAM

The RAM, a data memory for storing a variety of data, has a capacity of 144 words, 4-bit words. When programming, keep the following points in mind:

(1) Part of the data memory is used as stack area when saving subroutine return addresses and registers, so be careful not to overlap the data area and stack area.

(2) Subroutine calls and interrupts take up three words on the stack.

(3) Data memory 000H–00FH is the memory area pointed by the register pointer (RP).

CHAPTER 4 PERIPHERAL CIRCUITS AND OPERATION

Peripheral circuits (timer, I/O, and so on) of the E0C6011 are memory mapped. Thus, all the peripheral circuits can be controlled by using memory operations to access the I/O memory. The following sections describe how the peripheral circuits operate.

4.1 Memory Map

The data memory of the E0C6011 has an address space of 205 words, of which 48 words are allocated to display memory and 13 words, to I/O memory. Figure 4.1.1 show the overall memory map for the E0C6011, and Table 4.1.1, the memory maps for the peripheral circuits (I/O space).

Address Page	Low / High	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	0	M0	M1	M2	M3	M4	M5	M6	M7	M8	M9	MA	MB	MC	MD	ME	MF
	1	RAM area 112 words × 4 bits (R/W)															
	2																
	3																
	4																
	5																
	6																
	7	I/O memory See Table 4.1.1															
	8	RAM area 32 words × 4 bits (R/W)															
	9																
	A	Unused area															
	B																
	C																
	D																
	E																
	F	I/O memory See Table 4.1.1															

Fig. 4.1.1 Memory map

Address Page	Low / High	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	4 or C	Display memory 48 words × 4 bits 40H–6FH = R/W C0H–EFH = W only															
	5 or D																
	6 or E																

Fig. 4.1.2 Display memory map

Notes: • The display memory area can be selected from between 40H–6FH and C0H–EFH by mask option.
When 40H–6FH is selected, the display memory is assigned in the RAM area. So read/write operation is allowed.
When C0H–EFH is selected, the display memory is assigned as a write-only memory.

• Memory is not mounted in unused area within the memory map and in memory area not indicated in this chapter. For this reason, normal operation cannot be assured for programs that have been prepared with access to these areas.

Table 4.1.1 I/O memory map

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
070H	TM3	TM2	TM1	TM0	TM3	0			Clock timer data (2 Hz)
					TM2	0			Clock timer data (4 Hz)
					TM1	0			Clock timer data (8 Hz)
					TM0	0			Clock timer data (16 Hz)
	R								When f_{CLK} = 65,536 Hz
073H	K03	K02	K01	K00	K03	– *2	High	Low	Input port data (K00–K03)
					K02	– *2	High	Low	
					K01	– *2	High	Low	
	R				K00	– *2	High	Low	
075H	EIK03	EIK02	EIK01	EIK00	EIK03	0	Enable	Mask	Interrupt mask register (K00–K03)
					EIK02	0	Enable	Mask	
					EIK01	0	Enable	Mask	
	R/W				EIK00	0	Enable	Mask	
078H	CSDC	EIT2	EIT8	EIT32	CSDC	0	Static	Dynamic	LCD drive switch
					EIT2	0	Enable	Mask	Interrupt mask register (clock timer 2 Hz)
					EIT8	0	Enable	Mask	Interrupt mask register (clock timer 8 Hz)
	R/W				EIT32	0	Enable	Mask	Interrupt mask register (clock timer 32 Hz) — When f_{CLK} = 65,536 Hz
079H	0	IT2	IT8	IT32	0 *3	– *2	–	–	Unused
					IT2 *4	0	Yes	No	Interrupt factor flag (clock timer 2 Hz)
					IT8 *4	0	Yes	No	Interrupt factor flag (clock timer 8 Hz)
	R				IT32 *4	0	Yes	No	Interrupt factor flag (clock timer 32 Hz) — When f_{CLK} = 65,536 Hz
07AH	0	IK0	0	0	0 *3	– *2	–	–	Unused
					IK0 *4	0	Yes	No	Interrupt factor flag (K00–K03)
	R				0 *3	– *2	–	–	Unused
					0 *3	– *2	–	–	Unused
07CH	R03	R02	R01	R00	R03	0	High	Low	Output port (R03, $\overline{BZ}$)
					R02	0	High	Low	Output port (R02, FOUT)
					R01	0	High	Low	Output port (R01)
	R/W				R00	0	High	Low	Output port (R00, BZ)
07DH	P03	P02	P01	P00	P03	– *2	High	Low	I/O port data (P00–P03)
					P02	– *2	High	Low	
					P01	– *2	High	Low	Output latch is reset at initial reset
	R/W				P00	– *2	High	Low	
07EH	TMRST	0	0	IOC0	TMRST	Reset	Reset	–	Clock timer reset
					0 *3	– *2	–	–	Unused
	W	R		R/W	0 *3	– *2	–	–	Unused
					IOC0	0	Output	Input	I/O control register 0 (P00–P03)
0F6H	BZFQ	0	0	0	BZFQ	0	f_{CLK}/32	f_{CLK}/16	Buzzer frequency selection *5
					0 *3	– *2	–	–	Unused
	R/W	R			0 *3	– *2	–	–	Unused
					0 *3	– *2	–	–	Unused
0FDH	P13	P12	P11	P10	P13	– *2	High	Low	I/O port data (P10–P13)
					P12	– *2	High	Low	
					P11	– *2	High	Low	Output latch is reset at initial reset
	R/W				P10	– *2	High	Low	
0FEH	0	0	0	IOC1	0 *3	– *2	–	–	Unused
					0 *3	– *2	–	–	Unused
	R			R/W	0 *3	– *2	–	–	Unused
					IOC1	0	Output	Input	I/O control register 1 (P10–P13)
0FFH	CLKFQ1	CLKFQ0	0	LCDON	CLKFQ1	0			Peripheral system clock selection [CLKFQ1, 0]: 00 01 10 11 (f_{CLK}: fosc fosc/2 fosc/3 fosc/4)
					CLKFQ0	0			
	R/W		R	R/W	0 *3	– *2	–	–	Unused
					LCDON	1	On	Off	LCD display On/Off conrol

*1 Initial value at initial reset

*2 Not set in the circuit

*3 Always "0" being read

*4 Reset (0) immediately after being read

*5 f_{CLK} is selectable from fosc, fosc/2, fosc/3 and fosc/4 using the CLKFQ1–CLKFQ0 register.

4.2 Oscillation Circuit

The E0C6011 has a built-in CR oscillation circuit that generates the operating clock of the CPU and the peripheral circuit.

4.2.1 CR oscillation circuit

The CR oscillation circuit has a built-in capacitor and resistors, and an oscillation frequency can be selected by mask option.
The E0C6011 has a frequency divider circuit controlled by the CLKFQ1 and CLKFQ0 registers. These registers control the peripheral clock frequency fCLK. The CPU operate with the fOSC clock generated by the oscillation circuit.
Figure 4.2.1.1 shows the configuration of the CR oscillation circuit.

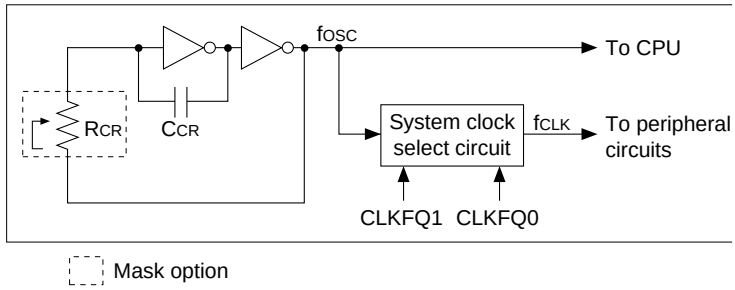


Fig. 4.2.1.1 Configuration of CR oscillation circuit

As Figure 4.2.1.1 indicates, the CR oscillation circuit can be configured using the built-in resistor RCR with different frequency selected by mask option.

4.2.2 Mask option

The mask option allows selection of an oscillation frequency using the built-in resistor. The following shows the alternatives of the mask option.

Table 4.2.2.1 Mask option for CR oscillation circuit

No.	Clock frequency
1	fOSC = 65 kHz
2	fOSC = 130 kHz
3	fOSC = 195 kHz
4	fOSC = 260 kHz

4.2.3 I/O memory for peripheral system clock

Table 4.2.3.1 lists the peripheral system clock control bits and their address.

Table 4.2.3.1 Peripheral system clock control bits

Address	Register								Comment
	D3	D2	D1	D0	Name	Init *1	1	0	
0FFH	CLKFQ1	CLKFQ0	0	LCDON	CLKFQ1	0			Peripheral system clock selection [CLKFQ1, 0]: 00 01 10 11 / fCLK: fOSC fOSC/2 fOSC/3 fOSC/4
					CLKFQ0	0			
	R/W		R	R/W	0 *3	– *2	–	–	Unused
					LCDON	1	On	Off	LCD display On/Off conrol

*1 Initial value at initial reset
*2 Not set in the circuit
*3 Always "0" being read
*4 Reset (0) immediately after being read

CLKFQ1, CLKFQ0: Peripheral system clock select registers (0FFH•D3, D2)

Select an operating clock frequency fCLK for the peripheral system. This selection affects the LCD frame frequency, timer data output, power-on reset time and differential pulse reset time.

Table 4.2.3.2 Selecting pheripheral system clock

CLKFQ1	CLKFQ0	fCLK	LCD frame frequency		
			1/4, 1/2 duty		1/3 duty
0	0	fOSC	fOSC/2048	32 Hz when fOSC = 65 kHz	42.7 Hz
0	1	fOSC/2	fOSC/(2×2048)	32 Hz when fOSC = 130 kHz	42.7 Hz
1	0	fOSC/3	fOSC/(3×2048)	32 Hz when fOSC = 195 kHz	42.7 Hz
1	1	fOSC/4	fOSC/(4×2048)	32 Hz when fOSC = 260 kHz	42.7 Hz

After an initial reset, these registers are set to "0".

4.3 Input Ports (K00–K03)

4.3.1 Configuration of input port

The E0C6011 has a 4-bit general-purpose input port. Each of the input port terminals (K00–K03) has an internal pull-down resistor. The pull-down resistor can be selected for each bit with the mask option. Figure 4.3.1.1 shows the configuration of input port.

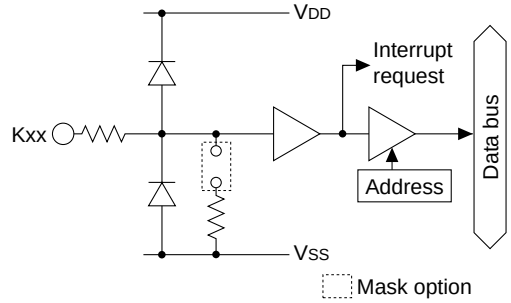


Fig. 4.3.1.1 Configuration of input port

Selecting "pull-down resistor enabled" with the mask option allows input from a push button, key matrix, and so forth. When "pull-down resistor disabled" is selected, the port can be used for slide switch input and interfacing with other LSIs.

4.3.2 Interrupt function

All four input port bits (K00–K03) provide the interrupt function. The conditions for issuing an interrupt can be set by the software for the four bits. Also, whether to mask the interrupt function can be selected individually for all four bits by the software. Figure 4.3.2.1 shows the configuration of K00–K03.

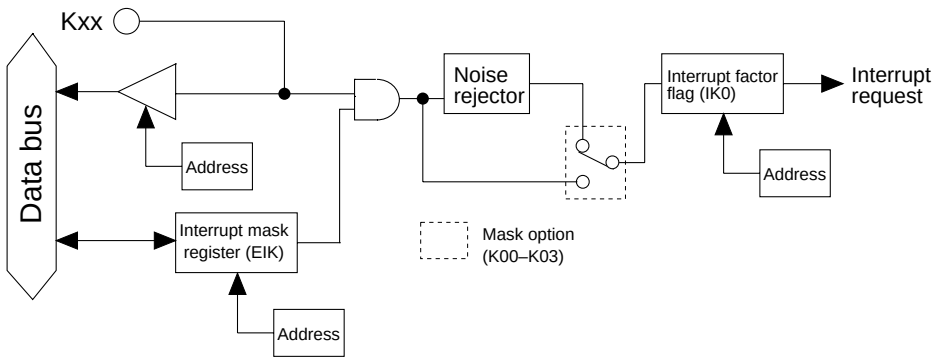
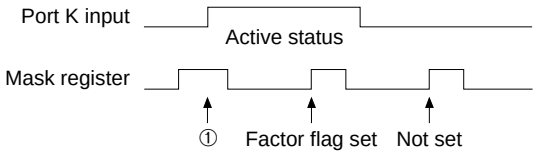


Fig. 4.3.2.1 Input interrupt circuit configuration (K00–K03)

The interrupt mask registers (EIK00–EIK03) enable the interrupt mask to be selected individually for K00–K03. An interrupt occurs when the input value which are not masked change and the interrupt factor flag (IK0) is set to "1".

Input interrupt programming related precautions



When the content of the mask register is rewritten, while the port K input is in the active status. The input interrupt factor flag is set at ①.

Fig. 4.3.2.2 Input interrupt timing

When using an input interrupt, if you rewrite the content of the mask register, when the value of the input terminal which becomes the interrupt input is in the active status (input terminal = high status), the factor flag for input interrupt may be set.
For example, a factor flag is set with the timing of ① shown in Figure 4.3.2.2. However, when clearing the content of the mask register with the input terminal kept in the high status and then setting it, the factor flag of the input interrupt is again set at the timing that has been set.
Consequently, when the input terminal is in the active status (high status), do not rewrite the mask register (clearing, then setting the mask register), so that a factor flag will only set at the rising edge in this case. When clearing, then setting the mask register, set the mask register, when the input terminal is not in the active status (low status).

4.3.3 Mask option

The contents that can be selected with the input port mask option are as follows:

(1) An internal pull-down resistor can be selected for each of the four bits of the input ports (K00–K03). Having selected "pull-down resistor disabled", take care that the input does not float. Select "pull-down resistor enabled" for input ports that are not being used.

(2) The input interrupt circuit contains a noise rejection circuit to prevent interrupts form occurring through noise. The mask option enables selection of the noise rejection circuit. When "use" is selected, a maximum delay of 0.5 msec (f_{CLK} = 65 kHz) occurs from the time an interrupt condition is established until the interrupt factor flag (IK0) is set to "1".

4.3.4 I/O memory of input port

Table 4.3.4.1 list the input port control bits and their addresses.

Table 4.3.4.1 Input port control bits

Address	Register								Comment
	D3	D2	D1	D0	Name	Init *1	1	0	
073H	K03	K02	K01	K00	K03	– *2	High	Low	Input port data (K00–K03)
					K02	– *2	High	Low	
	R				K01	– *2	High	Low	
					K00	– *2	High	Low	
075H	EIK03	EIK02	EIK01	EIK00	EIK03	0	Enable	Mask	Interrupt mask register (K00–K03)
					EIK02	0	Enable	Mask	
	R/W				EIK01	0	Enable	Mask	
					EIK00	0	Enable	Mask	
07AH	0	IK0	0	0	0 *3	– *2	–	–	Unused
					IK0 *4	0	Yes	No	Interrupt factor flag (K00–K03)
	R				0 *3	– *2	–	–	Unused
					0 *3	– *2	–	–	Unused

*1 Initial value at initial reset
*2 Not set in the circuit
*3 Always "0" being read
*4 Reset (0) immediately after being read

K00–K03: Input port data (073H)

The input data of the input port terminals can be read with these registers.

When "1" is read: High level
When "0" is read: Low level
Writing: Invalid

The value read is "1" when the terminal voltage of the input port (K00–K03) goes high (V_{DD}), and "0" when the voltage goes low (V_{SS}). These are read only bits, so writing cannot be done.

EIK00–EIK03: Interrupt mask registers (075H)

Masking the interrupt of the input port terminals can be done with these registers.

When "1" is written: Enable
When "0" is written: Mask
Reading: Valid

With these registers, masking of the input port bits can be done for each of the four bits.
After an initial reset, these registers are all set to "0".

IK0: Interrupt factor flag (07AH•D2)

This flag indicates the occurrence of an input interrupt.

When "1" is read: Interrupt has occurred
When "0" is read: Interrupt has not occurred
Writing: Invalid

The interrupt factor flag IK0 is associated with K00–K03. From the status of this flag, the software can decide whether an input interrupt has occurred.
This flag is reset when the software has read it.
Reading of interrupt factor flag is available at EI, but be careful in the following cases.
If the interrupt mask register value corresponding to the interrupt factor flag to be read is set to "1", an interrupt request will be generated by the interrupt factor flag set timing, or an interrupt request will not be generated.
After an initial reset, this flag is set to "0".

4.3.5 Programming note

When modifying the input port from high level to low level with pull-down resistor, a delay will occur at the fall of the waveform due to time constant of the pull-down resistor and input gate capacities. Provide appropriate waiting time in the program when performing input port reading.

4.4 Output Ports (R00–R03)

4.4.1 Configuration of output port

The E0C6011 has a 4-bit general output port (R00–R03).
Output specification of the output port can be selected in a bit units with the mask option. Two kinds of output specifications are available: complementary output and Pch open drain output. Also, the mask option enables the output ports R00, R02 and R03 to be used as special output ports. Figure 4.4.1.1 shows the configuration of the output port.

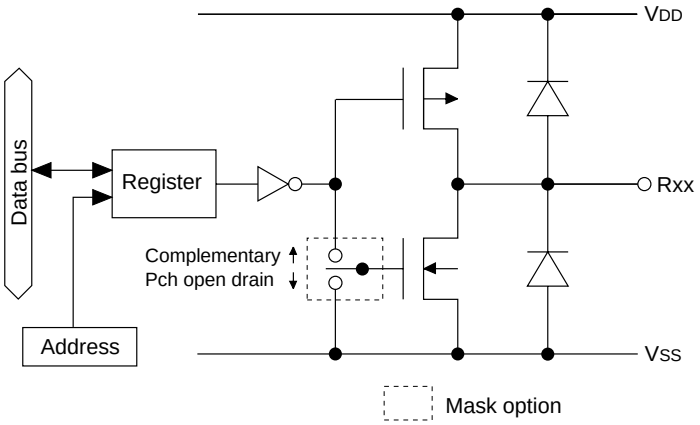


Fig. 4.4.1.1 Configuration of output port

4.4.2 Mask option

The mask option enables the following output port selection.

(1) Output specification of output port

The output specifications for the output port (R00–R03) may be set to either complementary output or Pch open drain output for each of the four bits. However, even when Pch open drain output is selected, a voltage exceeding the source voltage must not be applied to the output port.

(2) Special output

In addition to the regular DC output, special output can be selected for output ports R00, R02 and R03, as shown in Table 4.4.2.1. Figure 4.4.2.1 shows the structure of output ports R00–R03.

Table 4.4.2.1 Special output

Output port	Special output
R00	BZ output
R03	$\overline{BZ}$ output
R02	FOUT output

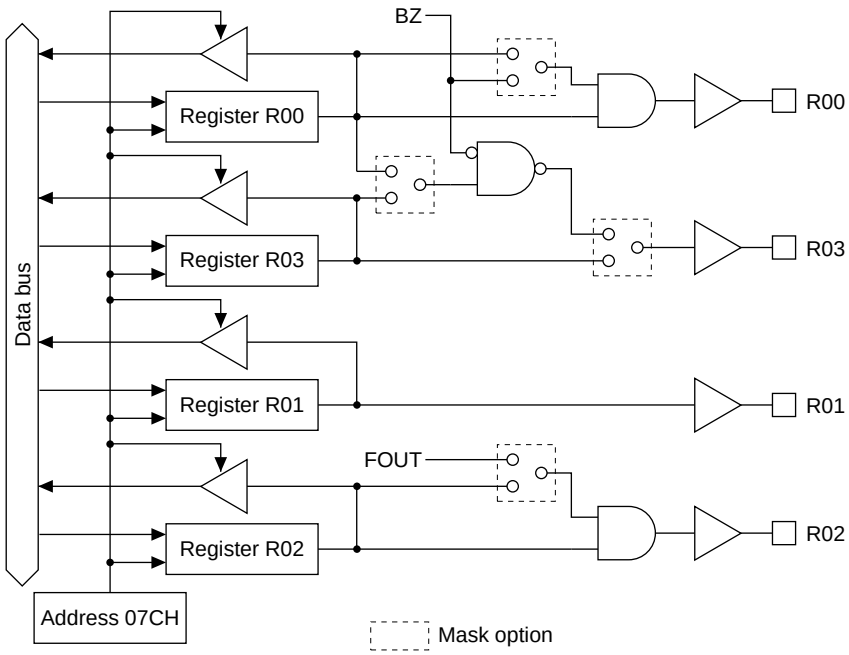


Fig. 4.4.2.1 Structure of output ports R00–R03

BZ, $\overline{BZ}$ (R00, R03)

The output ports R00 and R03 may be set to BZ output and $\overline{BZ}$ output (BZ reverse output), respectively, allowing for direct driving of the piezo-electric buzzer.
The BZ output is controlled by the R00 register. For the $\overline{BZ}$ output, the R00 register or the R03 register can be selected as the control register by mask option. When the R00 register is selected, the BZ and $\overline{BZ}$ outputs are controlled by the R00 register simultaneously.
The frequency of buzzer output may be selected by software to be either 2 kHz or 4 kHz (when f_{CLK} = 65 kHz). Figure 4.4.2.2 shows the output waveform.

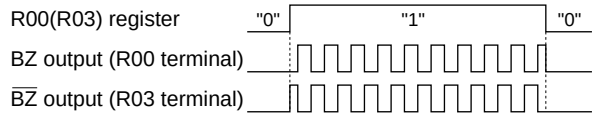


Fig. 4.4.2.2 Output waveform of BZ and $\overline{BZ}$

Notes: • A hazard may occur when the buzzer signal is turned on or off.

• When the R00 port is set for DC output, the R03 port cannot be set for the $\overline{BZ}$ output.

FOUT (R02)

When the output port R02 is set as the FOUT output port, the R02 will output the f_{CLK} (peripheral system clock frequency) clock or the clock that is generated by dividing the f_{CLK} clock. The clock frequency can be selected from among 8 types by mask option.
The types of frequency which can be selected are shown in Table 4.4.2.2.

Table 4.4.2.2 FOUT clock frequency

Setting value	Clock frequency (Hz)*
$f_{CLK}/2$	32,768
$f_{CLK}/4$	16,384
$f_{CLK}/8$	8,192
$f_{CLK}/16$	4,096
$f_{CLK}/32$	2,048
$f_{CLK}/64$	1,024
$f_{CLK}/128$	512
$f_{CLK}/256$	256

* When 65 kHz peripheral clock is selected

The FOUT output is controlled by the R02 register.
Figure 4.4.2.3 shows the output waveform.

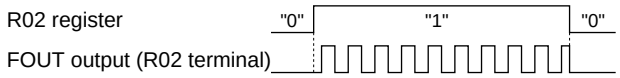


Fig. 4.4.2.3 Output waveform of FOUT

Note: A hazard may occur when the FOUT signal is turned on or off.

4.4.3 I/O memory of output port

Table 4.4.3.1 lists the output port control bits and their addresses.

Table 4.4.3.1 Control bits of output port

Address	Register								Comment
	D3	D2	D1	D0	Name	Init *1	1	0	
07CH	R03	R02	R01	R00	R03	0	High	Low	Output port (R03, $\overline{BZ}$)
					R02	0	High	Low	Output port (R02, FOUT)
	R/W				R01	0	High	Low	Output port (R01)
					R00	0	High	Low	Output port (R00, BZ)
0F6H	BZFQ	0	0	0	BZFQ	0	$f_{CLK}/32$	$f_{CLK}/16$	Buzzer frequency selection *5
					0 *3	– *2	–	–	Unused
	R/W	R			0 *3	– *2	–	–	Unused
					0 *3	– *2	–	–	Unused

*1 Initial value at initial reset
*2 Not set in the circuit
*3 Always "0" being read
*4 Reset (0) immediately after being read
*5 f_{CLK} is selectable from f_{OSC}, $f_{OSC}/2$, $f_{OSC}/3$ and $f_{OSC}/4$ using the CLKFQ1–CLKFQ0 register.

R00–R03 (when DC output is selected): Output port data (07CH)
Sets the output data for the output ports.

When "1" is written: High output
When "0" is written: Low output
Reading: Valid

The output port terminals output the data written to the corresponding registers (R00–R03) without changing it. When "1" is written to the register, the output port terminal goes high (V_{DD}), and when "0" is written, the output port terminal goes low (V_{SS}).
After an initial reset, all the registers are set to "0".

R00, R03 (when buzzer output is selected): Buzzer output control (07CH•D0, D3)
Controls the buzzer output.

When "1" is written: Buzzer output
When "0" is written: Low level (DC) output
Reading: Valid

The BZ signal is output from the R00 terminal by writing "1" to the R00 register. When "0" is written, the R00 terminal goes low.
For the $\overline{BZ}$ signal, either "R03 control" or "R00 control" can be selected by mask option.
When "R03 control" is selected, the $\overline{BZ}$ signal is output from the R03 terminal by writing "1" to the R03 register. When "0" is written to the R03 register, the R03 terminal goes low.
When "R00 control" is selected, the BZ and $\overline{BZ}$ signals are output simultaneously by writing "1" to the R00 register. When "0" is written to the R00 register, the R00 and R03 terminals go low.
After an initial reset, these registers are set to "0".

BZFQ: Buzzer frequency selection (0F6H•D3)

Selects the frequency of the buzzer signal.

When "1" is written: $f_{CLK}/32$ Hz
When "0" is written: $f_{CLK}/16$ Hz
Reading: Valid

When R00 and R03 ports are set to buzzer output, the frequency of the buzzer signal can be selected using this register.
When "1" is written to this register, the frequency is set to $f_{CLK}/32$ (2 kHz when f_{CLK} = 65 kHz) and when "0" is written, it is set to $f_{CLK}/16$ (4 kHz when f_{CLK} = 65 kHz). f_{CLK} is the peripheral system clock controlled by the CLKFQ1–CLKFQ0 register.
After an initial reset, this register is set to "0".

R02 (when FOUT is selected): FOUT output control (07CH•D2)

Controls the FOUT (fosc clock) output.

When "1" is written: Clock output
When "0" is written: Low level (DC) output
Reading: Valid

The FOUT signal is output from the R02 terminal by writing "1" to the R02 register. When "0" is written, the R02 terminal goes low.
After an initial reset, this register is set to "0".

4.4.4 Programming note

The buzzer (BZ, $\overline{BZ}$) or FOUT signal may produce hazards when it is turned on or off by the control register.

4.5 I/O Ports (P00–P03, P10–P13)

4.5.1 Configuration of I/O port

The E0C6011 has 8 bits of general-purpose I/O ports. Figure 4.5.1.1 shows the configuration of the I/O port. Each 4-bit I/O port (P00–P03 and P10–P13) can be set to either input mode or output mode by writing data to the I/O control register.

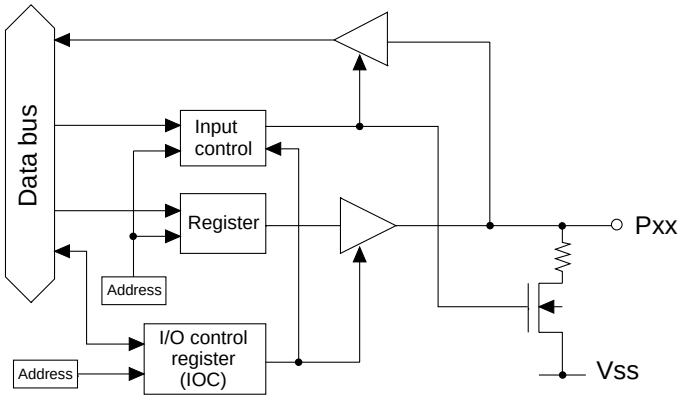


Fig. 4.5.1.1 Configuration of I/O port

4.5.2 I/O control register and I/O mode

Input or output mode can be set for each 4-bit I/O port (P00–P03, P10–P13) by writing data to the I/O control register (IOC0, IOC1).
To set the input mode, write "0" to the I/O control register. When an I/O port is set to input mode, it becomes high impedance status and works as an input port. However, the input line is pulled down when input data is read.

The output mode is set when "1" is written to the I/O control register. When an I/O port is set to output mode, it works as an output port. The port terminal goes high (V_{DD}) when the port output data is set to "1", and goes low (V_{SS}) when the port output data is set to "0".
After an initial reset, the I/O control registers are set to "0", and the I/O ports enter the input mode.

4.5.3 Mask option

The output specification during output mode (IOCx = "1") of the I/O port can be set with the mask option for either complementary output or Pch open drain output. This setting can be performed for each bit of the I/O port. However, when Pch open drain output has been selected, voltage in excess of the supply voltage must not be applied to the port.

4.5.4 I/O memory of I/O port

Table 4.5.4.1 lists the I/O port control bits and their addresses.

Table 4.5.4.1 I/O port control bits

Address	Register								Comment
	D3	D2	D1	D0	Name	Init *1	1	0	
07DH	P03	P02	P01	P00	P03	– *2	High	Low	I/O port data (P00–P03)
					P02	– *2	High	Low	
	R/W				P01	– *2	High	Low	Output latch is reset at initial reset
					P00	– *2	High	Low	
07EH	TMRST	0	0	IOC0	TMRST	Reset	Reset	–	Clock timer reset
					0 *3	– *2	–	–	Unused
	W	R		R/W	0 *3	– *2	–	–	Unused
					IOC0	0	Output	Input	I/O control register 0 (P00–P03)
0FDH	P13	P12	P11	P10	P13	– *2	High	Low	I/O port data (P10–P13)
					P12	– *2	High	Low	
	R/W				P11	– *2	High	Low	Output latch is reset at initial reset
					P10	– *2	High	Low	
0FEH	0	0	0	IOC1	0 *3	– *2	–	–	Unused
					0 *3	– *2	–	–	Unused
	R			R/W	0 *3	– *2	–	–	Unused
					IOC1	0	Output	Input	I/O control register 1 (P10–P13)

*1 Initial value at initial reset
*2 Not set in the circuit
*3 Always "0" being read
*4 Reset (0) immediately after being read

P00–P03, P10–P13: I/O port data registers (07DH, 0FDH)

I/O port data can be read and output data can be set through these registers.

Writing

When "1" is written: High level
When "0" is written: Low level

When an I/O port is set to the output mode, the written data is output from the I/O port terminal. When "1" is written as the port data, the port terminal goes high (V_{DD}), and when "0" is written, the terminal goes low (V_{SS}). Data can also be written in the input mode.

Reading

When "1" is read: High level
When "0" is read: Low level

The terminal voltage level of the I/O port is read out. When the I/O port is in the input mode the voltage level being input to the port can be read; in the output mode the output voltage level can be read. When the terminal voltage is high (V_{DD}), the port data read is "1", and when the terminal voltage is low (V_{SS}) the data read is "0". Also, the built-in pull-down resistor functions during reading, so the I/O port terminal is pulled down.

Note: When the I/O port is set to the input mode and a low-level voltage (Vss) is input, an erroneous input results if the time constant of the capacitive load of the input line and the built-in pull-down resistor load is greater than the read-out time. When the input data is being read, the time that the input line is pulled down is equivalent to 0.5 cycles of the CPU system clock. Hence, the electric potential of the terminals must settle within 0.5 cycles. If this condition cannot be met, some measure must be devised, such as arranging a pull-down resistor externally, or performing multiple read-outs.

IOC0, IOC1: I/O control registers (07EH•D0, 0FEH•D0)

The input or output mode of the I/O port can be set with these registers.

When "1" is written: Output mode
When "0" is written: Input mode
Reading: Valid

The input or output mode of the I/O port is set in units of four bits. For instance, IOC0 sets the mode for P00–P03 and IOC1 sets the mode for P10–P13.
Writing "1" to the I/O control register makes the corresponding I/O port enter the output mode, and writing "0" induces the input mode.
After an initial reset, these registers are set to "0", so the I/O ports are in the input mode.

4.5.5 Programming notes

(1) When the I/O port is set to the output mode and a low-impedance load is connected to the port terminal, the data written to the register may differ from the data read.

(2) When the I/O port is set to the input mode and a low-level voltage (Vss) is input, an erroneous input results if the time constant of the capacitive load of the input line and the built-in pull-down resistor load is greater than the read-out time. When the input data is being read, the time that the input line is pulled down is equivalent to 0.5 cycles of the CPU system clock. Hence, the electric potential of the terminals must settle within 0.5 cycles. If this condition cannot be met, some measure must be devised, such as arranging a pull-down resistor externally, or performing multiple read-outs.

4.6 LCD Driver (COM0–COM3, SEG0–SEG37)

4.6.1 Configuration of LCD driver

The E0C6011 has four common terminals and 38 (SEG0–SEG37) segment terminals, so that an LCD with a maximum of 152 (38 × 4) segments can be driven. The power for driving the LCD is generated by the internal circuit, so there is no need to supply power externally.
The driving method is 1/4 duty (or 1/3, 1/2 duty is selectable by mask option) dynamic drive, adopting the four types of potential (1/3 bias), V_{DD}, V_{L1}, V_{L2} and V_{L3}. Moreover, the 1/2 bias dynamic drive that uses three types of potential, V_{DD}, $V_{L1} = V_{L2}$ and V_{L3}, can be selected by setting the mask option (drive duty can also be selected from 1/4, 1/3 or 1/2).
The LCD drive voltages V_{L1} to V_{L3} are generated by the internal power supply circuit as shown in Table 4.6.1.1.

Table 4.6.1.1 LCD drive voltage

Mask option selection	Drive voltage		
	V_{L1}	V_{L2}	V_{L3}
4.5 V LCD, 1/3 bias	V_{SS}	2 V_{SS}	3 V_{SS}
3 V LCD, 1/2 bias	V_{SS}	V_{SS}	2 V_{SS}

When 1/2 bias drive option is selected, the V_{L1} terminal should be connected with the V_{L2} terminal outside the IC. Refer to Section 2.1, "Power Supply", for details of the power supply circuit.

The frame frequency is 32 Hz for 1/4 duty and 1/2 duty, and 42.7 Hz for 1/3 duty (in the case of f_{CLK} = 65 kHz).
Figures 4.6.1.1 to 4.6.1.6 show the drive waveform for each duty and bias.

Note: "f_{CLK}" indicates the peripheral system clock frequency selected by the CLKFQ1–CLKFQ0 register.

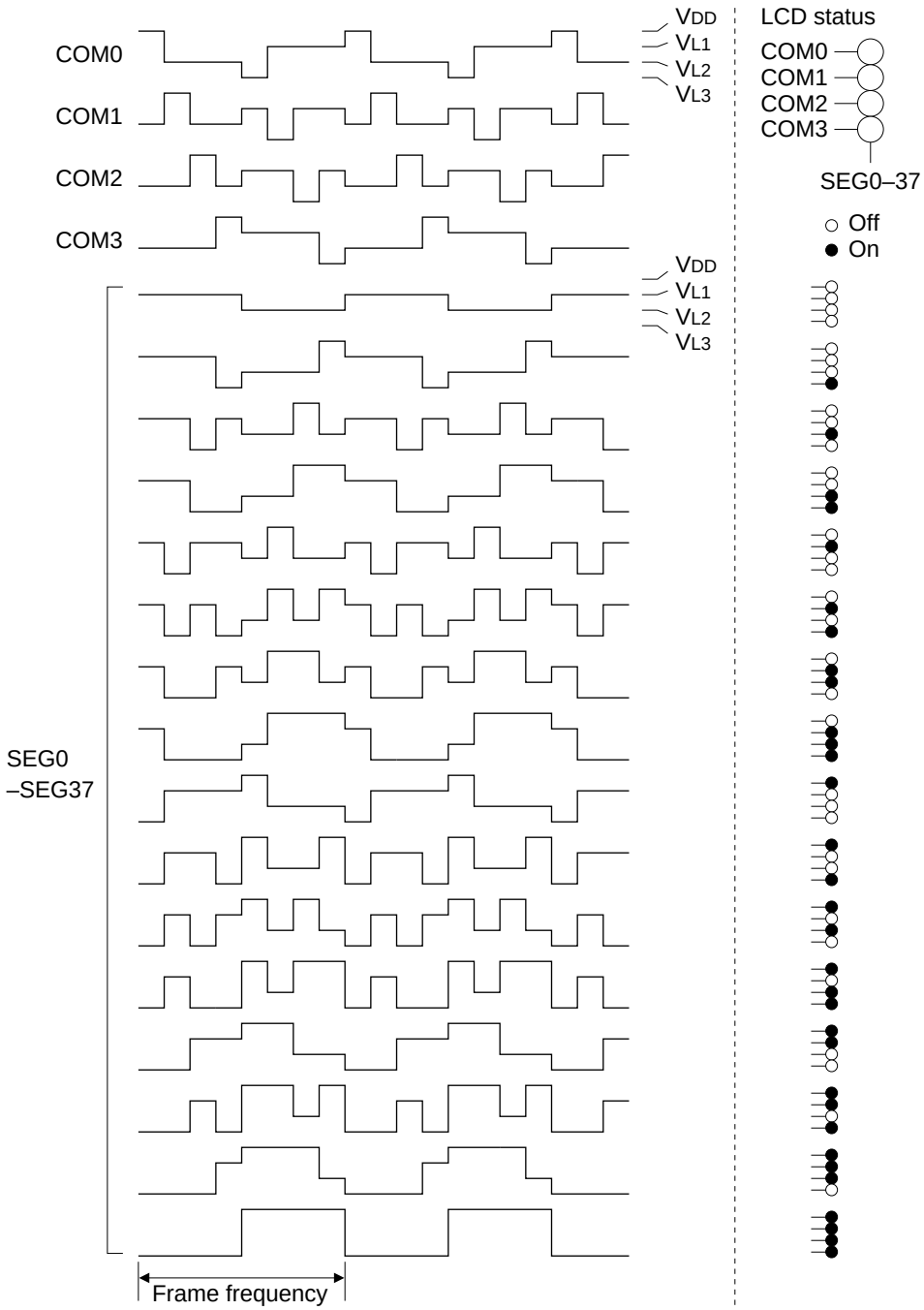


Fig. 4.6.1.1 Drive waveform for 1/4 duty (1/3 bias)

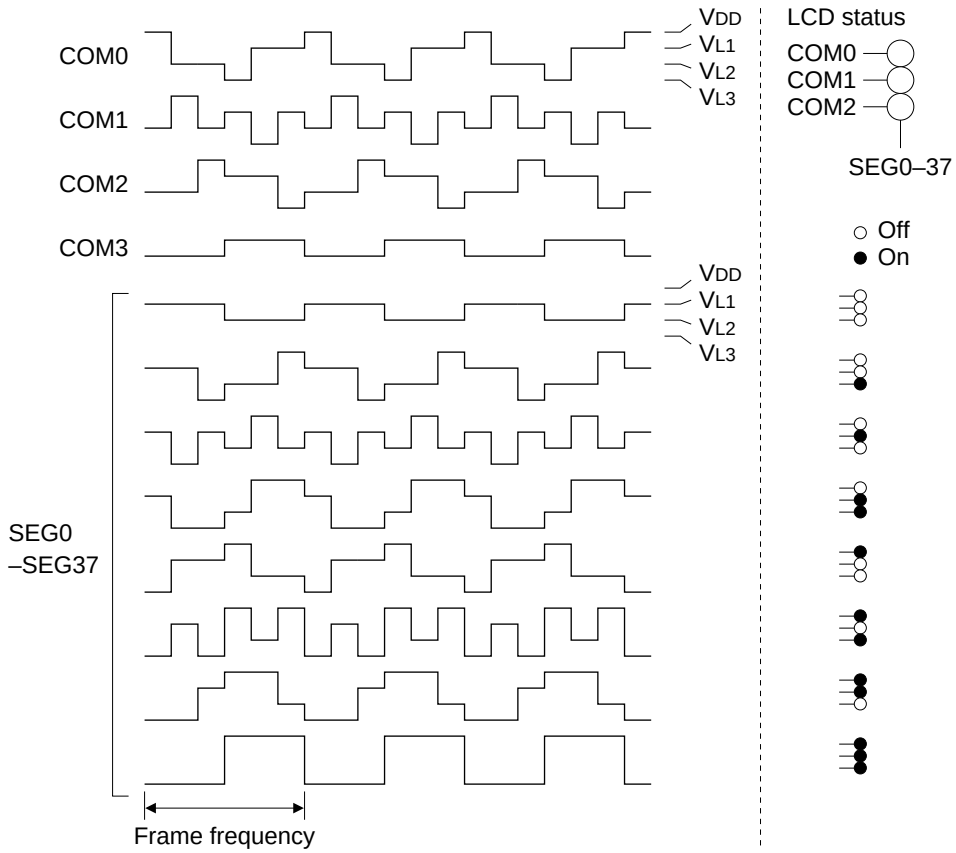


Fig. 4.6.1.2 Drive waveform for 1/3 duty (1/3 bias)

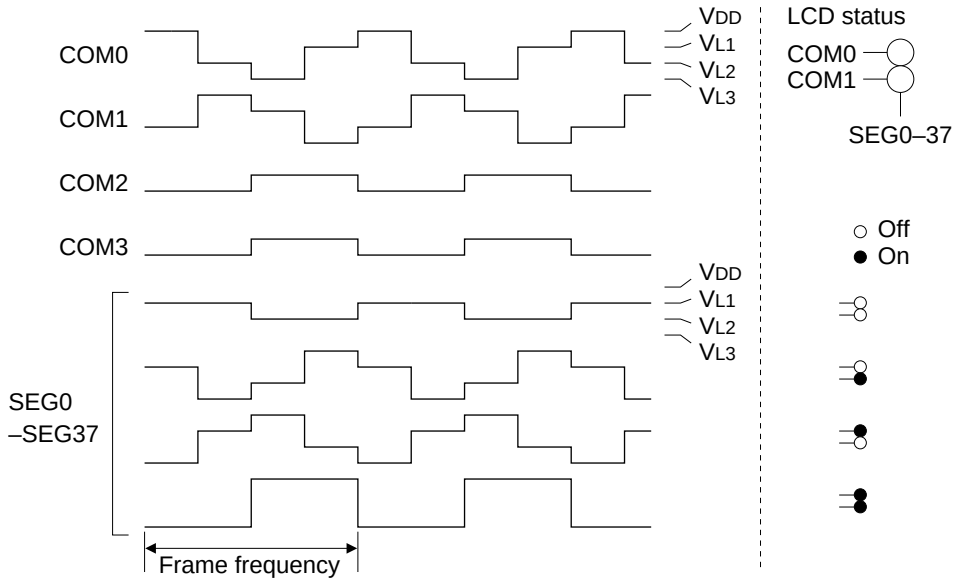


Fig. 4.6.1.3 Drive waveform for 1/2 duty (1/3 bias)

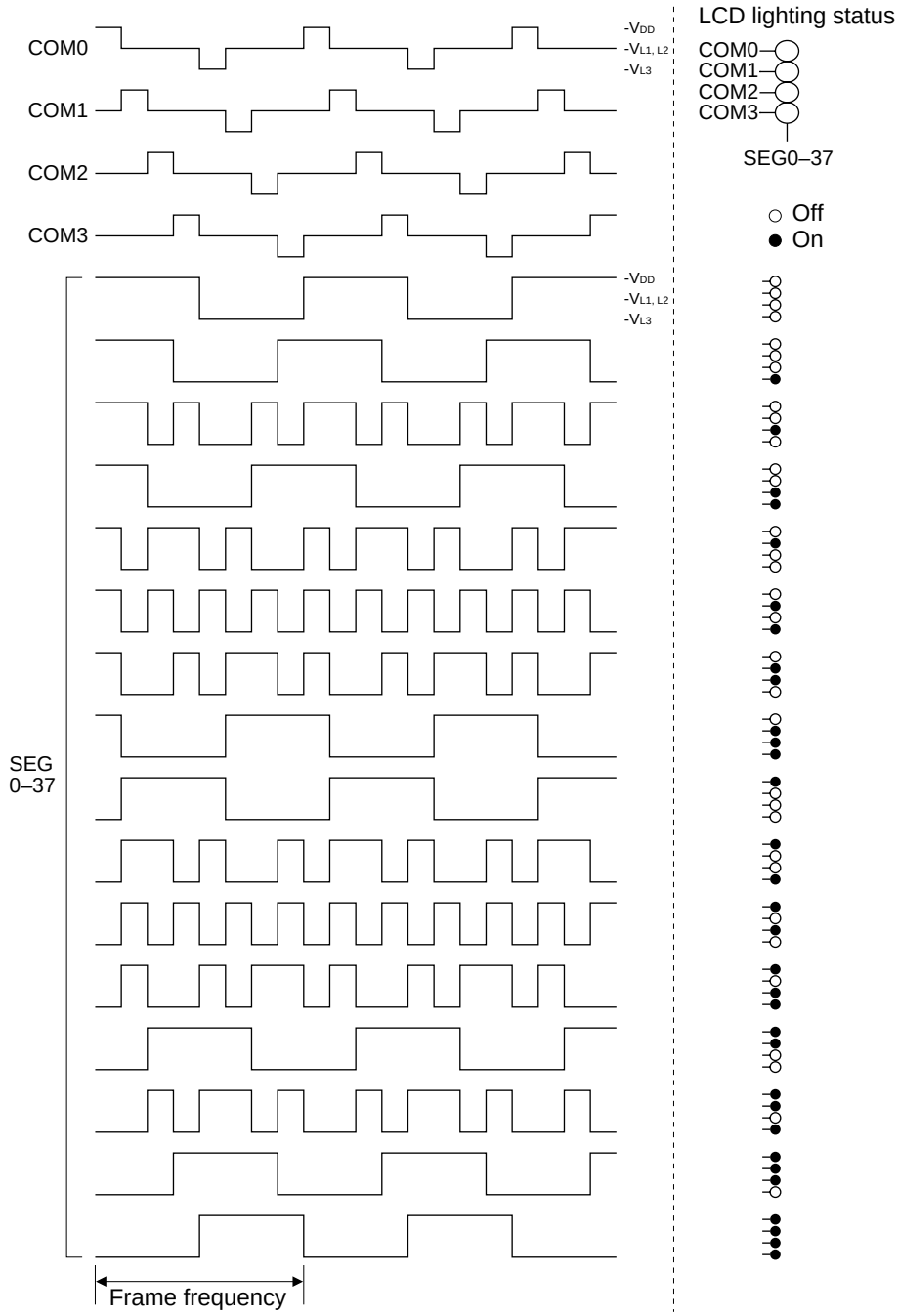


Fig. 4.6.1.4 Drive waveform for 1/4 duty (1/2 bias)

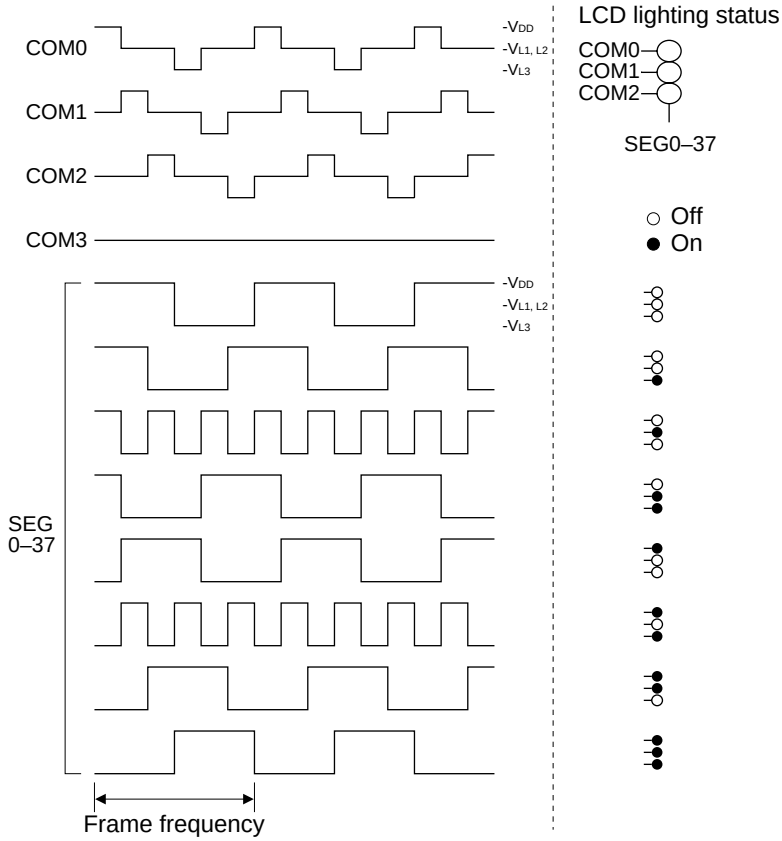


Fig. 4.6.1.5 Drive waveform for 1/3 duty (1/2 bias)

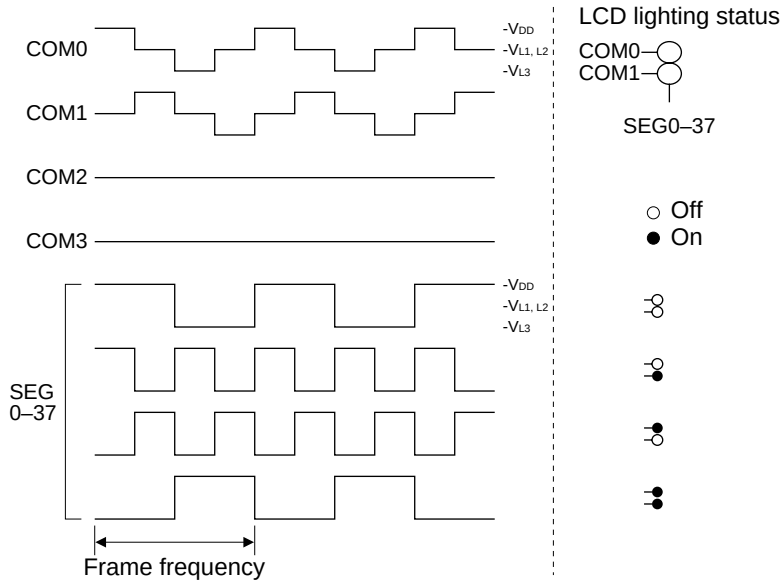


Fig. 4.6.1.6 Drive waveform for 1/2 duty (1/2 bias)

4.6.2 Switching between dynamic and static drive

The E0C6011 provides software setting of the LCD static drive.
This function enables easy adjustment (cadence adjustment) of the oscillation frequency of the oscillation circuit.

The procedure for executing static drive of the LCD is as follows:

(1) Write "1" to register CSDC at address 078H•D3.

(2) Write the same value to all registers corresponding to COM0–COM3 of the display memory.

Notes: • *Even when 1/3 duty is selected, COM3 is valid for static drive. However, the output frequency is the same as for the frame frequency.*

• *For cadence adjustment, set the display data corresponding to COM0–COM3, so that all the LCDs light.*

Figure 4.6.2.1 shows the drive waveform for static drive.

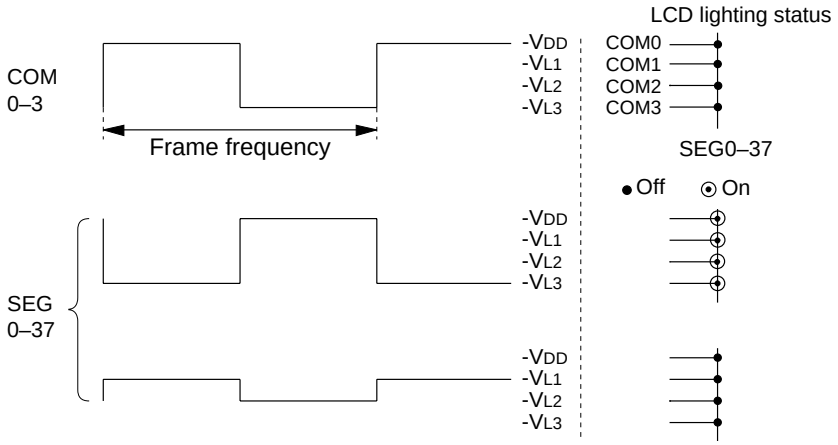


Fig. 4.6.2.1 LCD static drive waveform

4.6.3 Mask option

(1) Segment allocation

As shown in Figure 4.l.1, display data is decided by the data written to the display memory at address 040H–06FH or C0H–EFH.

- The mask option enables the display memory to be allocated entirely to either 040H–06FH (R/W) or C0H–EFH (W only).
- The address and bits of the display memory can be made to correspond to the segment terminals (SEG0–SEG37) in any combination through mask option. This simplifies design by increasing the degree of freedom with which the liquid crystal panel can be designed.

Figure 4.6.3.1 shows an example of the relationship between the LCD segments (on the panel) and the display memory (when 040H–06FH is selected) in the case of 1/3 duty.

Address	Data			
	D3	D2	D1	D0
06AH	d	c	b	a
06BH	p	g	f	e
06CH	d'	c'	b'	a'
06DH	p'	g'	f'	e'

Display data memory allocation

	Common 0	Common 1	Common 2
SEG10	6A, D0 (a)	6B, D1 (f)	6B, D0 (e)
SEG11	6A, D1 (b)	6B, D2 (g)	6A, D3 (d)
SEG12	6D, D1 (f')	6A, D2 (c)	6B, D3 (p)

Pin address allocation

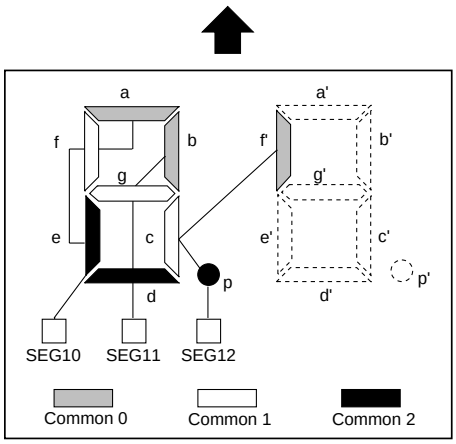


Fig. 4.6.3.1 Segment allocation

(2) Drive duty

According to the mask option, either 1/4, 1/3 or 1/2 duty can be selected as the LCD drive duty. Table 4.6.3.1 shows the differences in the number of segments according to the selected duty.

Table 4.6.3.1 Differences according to selected duty

Duty	COM used	Max. number of segments	Frame frequency *
1/4	COM0–COM3	152 (38 × 4)	f_{CLK}/2,048 (32 Hz)
1/3	COM0–COM2	114 (38 × 3)	f_{CLK}/1,536 (42.7 Hz)
1/2	COM0–COM1	76 (38 × 2)	f_{CLK}/2,048 (32 Hz)

* ( ) indicates the frequency when f_{CLK} = 65 kHz.
f_{CLK} is controlled by the CLKFQ1–CLKFQ0 register.
(f_{CLK} = f_{OSC}, f_{OSC}/2, f_{OSC}/3 or f_{OSC}/4)

(3) Output specification

- The segment terminals (SEG0–SEG37) are selected by mask option in pairs for either segment signal output or DC output (V_{DD} and V_{SS} binary output). When DC output is selected, the data corresponding to COM0 of each segment terminal is output.
- When DC output is selected, either complementary output or Pch open drain output can be selected for each terminal by mask option.

Note: The terminal pairs are the combination of SEG (2∗n) and SEG (2∗n + 1) (where n is an integer from 0 to 18).

(4) Drive bias

For the drive bias, either 1/3 bias or 1/2 bias can be selected by the mask option.

4.6.4 I/O memory of LCD driver

Table 4.6.4.1 shows the control bits of the LCD driver and their addresses. Figure 4.6.4.1 shows the display memory map.

Table 4.6.4.1 Control bits of LCD driver

Address	Register D3	D2	D1	D0	Name	Init ∗1	1	0	Comment
078H	CSDC	EIT2	EIT8	EIT32	CSDC	0	Static	Dynamic	LCD drive switch
					EIT2	0	Enable	Mask	Interrupt mask register (clock timer 2 Hz)
					EIT8	0	Enable	Mask	Interrupt mask register (clock timer 8 Hz)
	R/W				EIT32	0	Enable	Mask	Interrupt mask register (clock timer 32 Hz)
0FFH	CLKFQ1	CLKFQ0	0	LCDON	CLKFQ1	0			Peripheral system clock selection [CLKFQ1, 0]: 00 01 10 11; fCLK: fosc fosc/2 fosc/3 fosc/4
					CLKFQ0	0			
	R/W		R	R/W	0 ∗3	– ∗2	–	–	Unused
					LCDON	1	On	Off	LCD display On/Off conrol

∗1 Initial value at initial reset
∗2 Not set in the circuit
∗3 Always "0" being read
∗4 Reset (0) immediately after being read

Address / Page	Low / High	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	4 or C	Display memory 48 words × 4 bits 40H–6FH = R/W C0H–EFH = W only															
	5 or D																
	6 or E																

Fig. 4.6.4.1 Display memory map

LCDON: LCD display control (0FFH•D0)

Controls the LCD display.

When "1" is written: LCD displayed
When "0" is written: LCD is all off
Reading: Valid

By writing "0" to the LCDON register, all the LCD dots goes off, and when "1" is written, it returns to normal display.
Writing "0" outputs an off waveform to the SEG terminals, and does not affect the content of the display memory.
After an initial reset, this register is set to "1".

CSDC: LCD drive switch (078H•D3)

The LCD drive format can be selected with this switch.

When "1" is written: Static drive
When "0" is written: Dynamic drive
Reading: Valid

After an initial reset, this register is set to "0".

Display memory (040H–06FH or C0H–EFH)

The LCD segments are turned on or off according to this data.

When "1" is written: On
When "0" is written: Off
Reading: Valid for 040H–06FH
Undefined C0H–EFH

By writing data into the display memory allocated to the LCD segment (on the panel), the segment can be turned on or off. After an initial reset, the contents of the display memory are undefined.

4.6.5 Programming notes

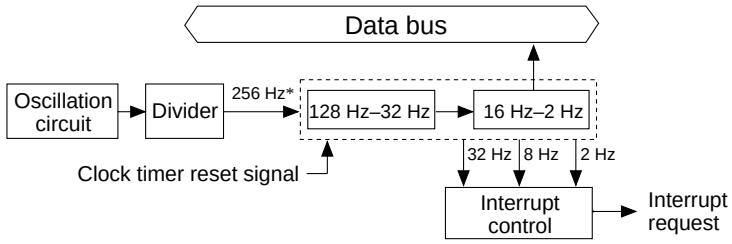
(1) When 040H–06FH is selected for the display memory, the memory data and the display will not match until the area is initialized (through, for instance, memory clear processing by the CPU). Initialize the display memory by executing initial processing.

(2) When 0C0H–0EFH is selected for the display memory, that area becomes write-only. Rewriting the contents with a logical operation instruction (e.g., AND, OR, etc.) which come with read-out operations is not possible. To perform bit operations, a buffer to hold the display data is required on the RAM.

4.7 Clock Timer

4.7.1 Configuration of clock timer

The E0C6011 has a built-in clock timer that uses the oscillation circuit as the clock source. The clock timer is configured as a 7-bit binary counter that counts with a 256 Hz (when fCLK = 65,536 Hz) source clock from the divider. The high-order 4 bits of the counter data can be read by the software.
Figure 4.7.1.1 is the block diagram of the clock timer.



∗When fCLK = 65,536 Hz.
fCLK is controlled by the CLKFQ1–CLKFQ0 register.
(fCLK = fOSC, fOSC/2, fOSC/3 or fOSC/4)

Fig. 4.7.1.1 Block diagram of clock timer

Normally, this clock timer is used for all kinds of timing purpose, such as clocks.

4.7.2 Interrupt function

The clock timer can generate interrupts at the falling edge of the 32 Hz, 8 Hz, and 2 Hz signals (when fCLK = 65,536 Hz). The software can mask any of these interrupt signals.
Figure 4.7.2.1 is the timing chart of the clock timer.

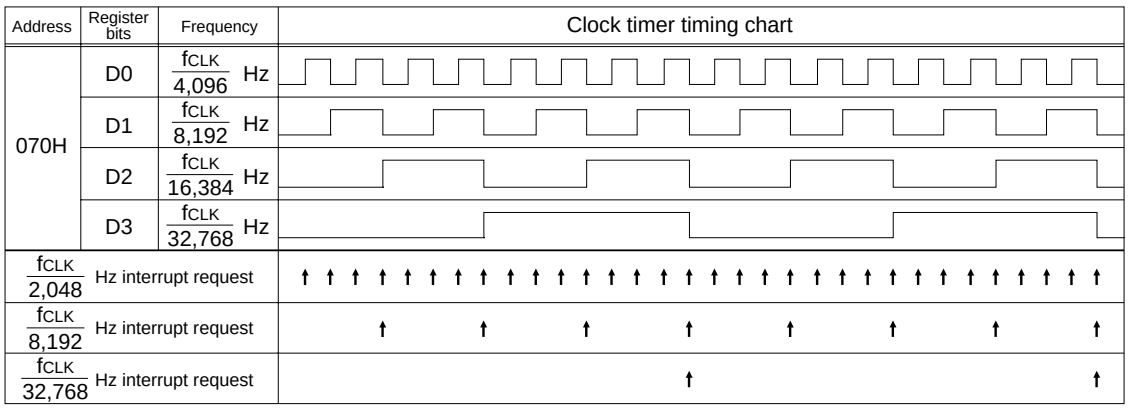


Fig. 4.7.2.1 Timing chart of the clock timer

As shown in Figure 4.7.2.1, an interrupt is generated at the falling edge of the 32 Hz, 8 Hz, and 2 Hz signals (when fCLK = 65,536 Hz). At this point, the corresponding interrupt factor flag (IT32, IT8, IT2) is set to "1". The interrupts can be masked individually with the interrupt mask register (EIT32, EIT8, EIT2). However, regardless of the interrupt mask register setting, the interrupt factor flags will be set to "1" at the falling edge of their corresponding signal (e.g. the falling edge of the 2 Hz signal sets the 2 Hz interrupt factor flag to "1").

4.7.3 I/O memory of clock timer

Table 4.7.3.1 shows the clock timer control bits and their addresses.

Table 4.7.3.1 Control bits of clock timer

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
070H	TM3	TM2	TM1	TM0	TM3	0			Clock timer data (2 Hz) — When f_{CLK} = 65,536 Hz
	R				TM2	0			Clock timer data (4 Hz)
					TM1	0			Clock timer data (8 Hz)
					TM0	0			Clock timer data (16 Hz)
078H	CSDC	EIT2	EIT8	EIT32	CSDC	0	Static	Dynamic	LCD drive switch
	R/W				EIT2	0	Enable	Mask	Interrupt mask register (clock timer 2 Hz) — When f_{CLK} = 65,536 Hz
					EIT8	0	Enable	Mask	Interrupt mask register (clock timer 8 Hz)
					EIT32	0	Enable	Mask	Interrupt mask register (clock timer 32 Hz)
079H	0	IT2	IT8	IT32	0 *3	– *2	–	–	Unused
	R				IT2 *4	0	Yes	No	Interrupt factor flag (clock timer 2 Hz) — When f_{CLK} = 65,536 Hz
					IT8 *4	0	Yes	No	Interrupt factor flag (clock timer 8 Hz)
					IT32 *4	0	Yes	No	Interrupt factor flag (clock timer 32 Hz)
07EH	TMRST	0	0	IOC0	TMRST	Reset	Reset	–	Clock timer reset
	W	R		R/W	0 *3	– *2	–	–	Unused
					0 *3	– *2	–	–	Unused
					IOC0	0	Output	Input	I/O control register 0 (P00–P03)

*1 Initial value at initial reset
*2 Not set in the circuit
*3 Always "0" being read
*4 Reset (0) immediately after being read

TM0–TM3: Timer data (070H)

The l6 Hz to 2 Hz (when f_{CLK} = 65,536 Hz) timer data of the clock timer can be read from this register. These four bits are read-only, and write operations are invalid.
After an initial reset, the timer data is initialized to "0H".

EIT32, EIT8, EIT2: Interrupt mask registers (078H•D0–D2)

These registers are used to mask the clock timer interrupt.

When "1" is written: Enabled
When "0" is written: Masked
Reading: Valid

The interrupt mask registers (EIT32, EIT8, EIT2) mask the corresponding interrupt frequencies (32 Hz, 8 Hz, 2 Hz, when f_{CLK} = 65,536 Hz).
At initial reset, these registers are all set to "0".

IT32, IT8, IT2: Interrupt factor flags (079H•D0–D2)

These flags indicate the status of the clock timer interrupt.

When "1" is read: Interrupt has occurred
When "0" is read: Interrupt has not occurred
Writing: Invalid

The interrupt factor flags (IT32, IT8, IT2) correspond to the clock timer interrupts (32 Hz, 8 Hz, 2 Hz, when f_{CLK} = 65,536 Hz). The software can determine from these flags whether there is a clock timer interrupt. However, even if the interrupt is masked, the flags are set to "1" at the falling edge of the signal. These flags can be reset when the register is read by the software.
Reading of interrupt factor flags is available at EI, but be careful in the following cases.
If the interrupt mask register value corresponding to the interrupt factor flag to be read is set to "1", an interrupt request will be generated by the interrupt factor flag set timing, or an interrupt request will not be generated. Be very careful when interrupt factor flags are in the same address.
At initial reset, these flags are set to "0".

TMRST: Clock timer reset (07EH•D3)

This bit resets the clock timer.

When "1" is written: Clock timer reset
When "0" is written: No operation
Reading: Always "0"

The clock timer is reset by writing "1" to TMRST. The clock timer starts immediately after this. No operation results when "0" is written to TMRST.
This bit is write-only, and so is always "0" when read.

4.7.4 Programming notes

(1) Note that the frequencies and times differ from the description in this section when the peripheral system clock frequency is not 65.536 kHz.

(2) When the clock timer has been reset, the interrupt factor flag (IT) may sometimes be set to "1". Consequently, reset the flag by reading as necessary at reset.

(3) Reading of interrupt factor flags is available at EI, but be careful in the following cases.
If the interrupt mask register value corresponding to the interrupt factor flag to be read is set to 1, an interrupt request will be generated by the interrupt factor flag set timing, or an interrupt request will not be generated. Be very careful when interrupt factor flags are in the same address.

4.8 Interrupt and HALT/SLEEP

Interrupt types

The E0C6011 provides the following interrupt settings, each of which is maskable.

External interrupt: Input port interrupt (one)
Internal interrupt: Timer interrupt (one)

To enable interrupts, the interrupt flag must be set to 1 (EI) and the necessary related interrupt mask registers must be set to 1 (enable). When an interrupt occurs, the interrupt flag is automatically reset to 0 (DI) and interrupts after that are inhibited.
Figure 4.8.1 shows the configuration of the interrupt circuit.

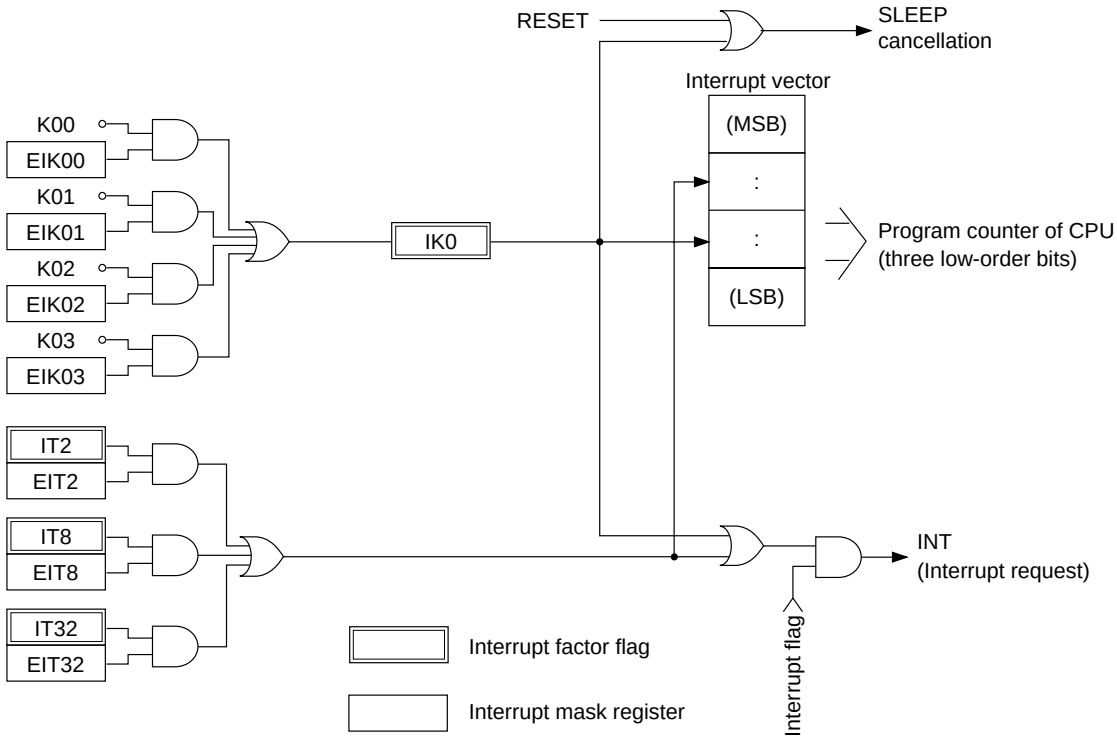


Fig. 4.8.1 Configuration of interrupt circuit

HALT and SLEEP modes

When the HALT instruction is executed, the CPU stops operating and enters the HALT mode. The oscillation circuit and the peripheral circuits operate in the HALT mode. By an interrupt, the CPU exits the HALT mode and resumes operating.

Executing the SLP instruction sets the IC in the SLEEP mode that stops operations of the CPU and oscillation circuit. The SLEEP mode will be canceled by an input interrupt request from the input port K00–K03 or a reset pulse input.
Consequently, at least one input port (K00, K01, K02 or K03) interrupt must be enabled before shifting to the SLEEP status. When the SLEEP status is canceled by a K0n input interrupt, the CPU waits for oscillation to stabilize then restarts operating.

Refer to the "E0C6200/6200A Core CPU Manual" for transition to the HALT/SLEEP status and timing of its cancellation.

Figures 4.8.2 to 4.8.5 show the sequence to enter and cancel the SLEEP mode.

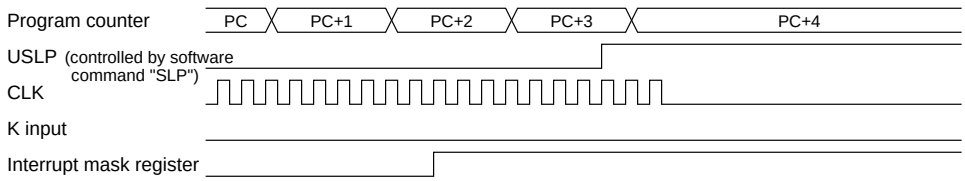


Fig. 4.8.2 Entering SLEEP mode

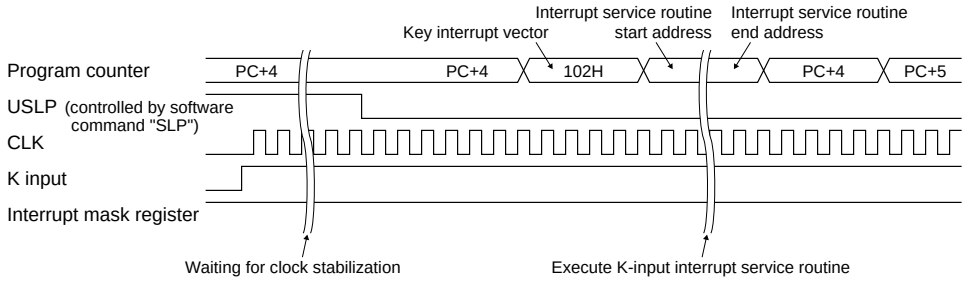


Fig. 4.8.3 Wakeup from SLEEP mode by K-port

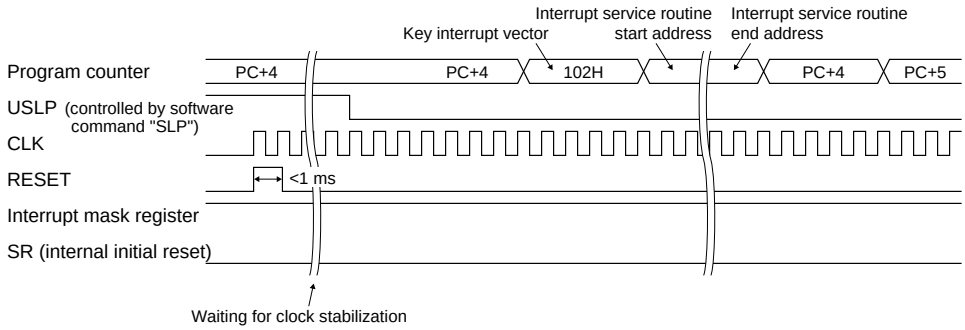


Fig. 4.8.4 Wakeup from SLEEP mode by RESET pulse (<1 ms, for f_{CLK} = 65 kHz)

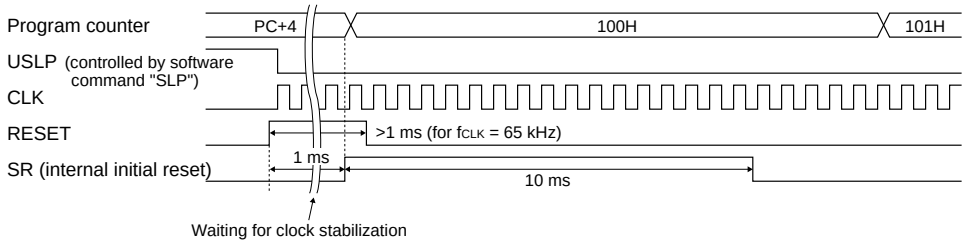


Fig. 4.8.5 Wakeup from SLEEP mode by RESET pulse (>1 ms, for f_{CLK} = 65 kHz)

4.8.1 Interrupt factors

Table 4.8.1.1 shows the factors that generate interrupt requests.

The interrupt factor flags are set to 1 depending on the corresponding interrupt factors.
The CPU is interrupted when the following two conditions occur and an interrupt factor flag is set to 1.

- The corresponding mask register is 1 (enabled)
- The interrupt flag is 1 (EI)

The interrupt factor flag is a read-only register, but can be reset to 0 when the register data is read.
At initial reset, the interrupt factor flags are reset to 0.

Note: Reading of interrupt factor flag is available at EI, but be careful in the following cases. If the interrupt mask register value corresponding to the interrupt factor flag to be read is set to 1, an interrupt request will be generated by the interrupt factor flag set timing, or an interrupt request will not be generated. Be very careful when interrupt factor flags are in the same address.

Table 4.8.1.1 Interrupt factors

Interrupt factor	Interrupt factor flag
Clock timer 2 Hz falling edge (f_{CLK} = 65 kHz)	IT2 (079H•D2)
Clock timer 8 Hz falling edge (f_{CLK} = 65 kHz)	IT8 (079H•D1)
Clock timer 32 Hz falling edge (f_{CLK} = 65 kHz)	IT32 (079H•D0)
Input (K00–K03) port rising edge	IK0 (07AH•D2)

4.8.2 Specific masks for interrupt

The interrupt factor flags can be masked by the corresponding interrupt mask registers. The interrupt mask registers are read/write registers. The interrupts are enabled when 1 is written to them, and masked (interrupt disabled) when 0 is written to them.
At initial reset, the interrupt mask register is set to 0.
Table 4.8.2.1 shows the correspondence between interrupt mask registers and interrupt factor flags.

Table 4.8.2.1 Interrupt mask registers and interrupt factor flags

Interrupt mask register		Interrupt factor flag	
EIT2	(078H•D2)	IT2	(079H•D2)
EIT8	(078H•D1)	IT8	(079H•D1)
EIT32	(078H•D0)	IT32	(079H•D0)
EIK03*	(075H•D3)	IK0	(07AH•D2)
EIK02*	(075H•D2)		
EIK01*	(075H•D1)		
EIK00*	(075H•D0)		

∗ There is an interrupt mask register for each input port pin.

4.8.3 Interrupt vectors

When an interrupt request is input to the CPU, the CPU starts interrupt processing. After the program being executed is suspended, interrupt processing is executed in the following order:

① The address data (value of the program counter) of the program step to be executed next is saved on the stack (RAM).

② The interrupt request causes the value of the interrupt vector (page 1, 01H–07H) to be loaded into the program counter.

③ The program at the specified address is executed (execution of interrupt processing routine).

Note: The processing in steps 1 and 2, above, takes 12 cycles of the CPU system clock.

Table 4.8.3.1 Interrupt vector addresses

Page	Step	Interrupt vector
1	00H	Initial reset
	02H	Input (K00–K03) interrupt
	04H	Clock timer interrupt
	06H	Clock timer & Input (K00–K03) interrupt

4.8.4 I/O memory of interrupt

Table 4.8.4.1 shows the interrupt control bits and their addresses.

Table 4.8.4.1 Control bits of interrupt

Address	Register								Comment
	D3	D2	D1	D0	Name	Init *1	1	0	
075H	EIK03	EIK02	EIK01	EIK00	EIK03	0	Enable	Mask	Interrupt mask register (K00–K03)
					EIK02	0	Enable	Mask	
					EIK01	0	Enable	Mask	
	R/W				EIK00	0	Enable	Mask	
078H	CSDC	EIT2	EIT8	EIT32	CSDC	0	Static	Dynamic	LCD drive switch
					EIT2	0	Enable	Mask	Interrupt mask register (clock timer 2 Hz)
					EIT8	0	Enable	Mask	Interrupt mask register (clock timer 8 Hz)
	R/W				EIT32	0	Enable	Mask	Interrupt mask register (clock timer 32 Hz)
079H	0	IT2	IT8	IT32	0 *3	– *2	–	–	Unused
					IT2 *4	0	Yes	No	Interrupt factor flag (clock timer 2 Hz)
					IT8 *4	0	Yes	No	Interrupt factor flag (clock timer 8 Hz)
	R				IT32 *4	0	Yes	No	Interrupt factor flag (clock timer 32 Hz)
07AH	0	IK0	0	0	0 *3	– *2	–	–	Unused
					IK0 *4	0	Yes	No	Interrupt factor flag (K00–K03)
					0 *3	– *2	–	–	Unused
	R				0 *3	– *2	–	–	Unused

When f_{CLK} = 65,536 Hz (applies to the 078H and 079H rows)

*1 Initial value at initial reset
*2 Not set in the circuit
*3 Always "0" being read
*4 Reset (0) immediately after being read

EIT32, EIT8, EIT2: Interrupt mask registers (078H•D0–D2)
IT32, IT8, IT2: Interrupt factor flags (079H•D0–D2)

...See Section 4.7, "Clock Timer".

EIK00–EIK03: Interrupt mask registers (075H)
IK0: Interrupt factor flag (07AH•D2)

...See Section 4.3, "Input Ports".

4.8.5 Programming notes

(1) Restart from the HALT mode is performed by an interrupt. The return address after completion of the interrupt processing will be the address following the HALT instruction.

(2) Restart from the SLEEP mode is performed by an input interrupt from the input port (K00–K03). The return address after completion of the interrupt processing will be the address following the SLP instruction. At least one input port interrupt must be enabled before shifting to the SLEEP mode.

(3) When an interrupt occurs, the interrupt flag will be reset by the hardware and it will become DI status. After completion of the interrupt processing, set to the EI status through the software as needed.
Moreover, the nesting level may be set to be programmable by setting to the EI state at the beginning of the interrupt processing routine.

(4) The interrupt factor flags must always be reset before setting the EI status. When the interrupt mask register has been set to 1, the same interrupt will occur again if the EI status is set unless of resetting the interrupt factor flag.

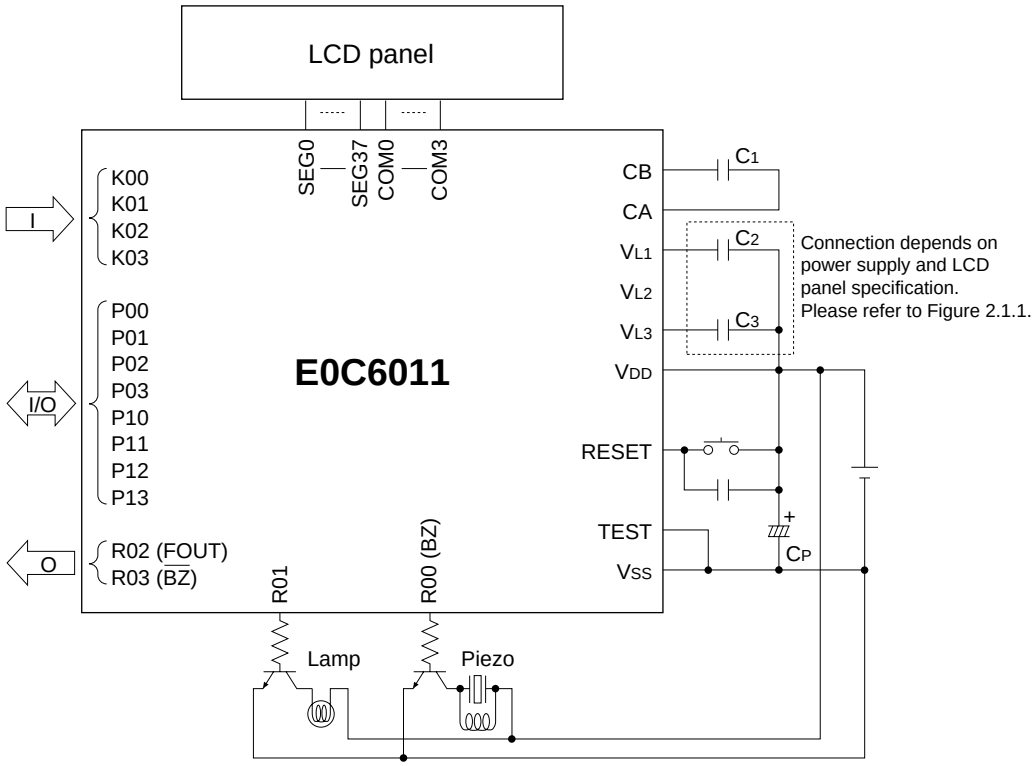
(5) The interrupt factor flag will be reset by reading through the software. Because of this, when multiple interrupt factor flags are to be assigned to the same address, perform the flag check after the contents of the address has been stored in the RAM. Direct checking with the FAN instruction will cause all the interrupt factor flag to be reset.

(6) Reading of interrupt factor flag is available at EI, but be careful in the following cases.
If the interrupt mask register value corresponding to the interrupt factor flag to be read is set to 1, an interrupt request will be generated by the interrupt factor flag set timing, or an interrupt request will not be generated. Be very careful when interrupt factor flags are in the same address.

(7) Restart from SLEEP mode can be performed by an external reset signal.
If the input reset pulse width is more than 1 ms (when f_{CLK} = 65 kHz), the internal system reset signal goes high to reset the system.
If the reset pulse width is less than 1 ms, the system will execute the input interrupt service routine. The return address after completion of the interrupt processing will be the address following the SLP instruction.

CHAPTER 5 BASIC EXTERNAL WIRING DIAGRAM

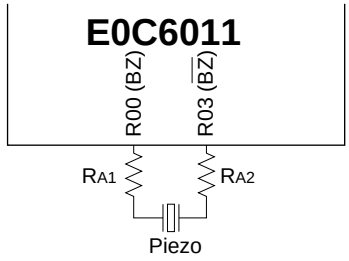
Piezo Buzzer Single Terminal Driving



C_1	Capacitor	0.1 µF
C_2	Capacitor	0.1 µF
C_3	Capacitor	0.1 µF
C_P	Capacitor	3.3 µF

Note: The above table is simply an example, and is not guaranteed to work.

Piezo Buzzer Direct Driving



R_{A1}	Protection resistor	100 Ω
R_{A2}	Protection resistor	100 Ω

CHAPTER 6 ELECTRICAL CHARACTERISTICS

6.1 Absolute Maximum Rating

(V_{DD}=0V)

Item	Symbol	Rated value	Unit
Supply voltage	V_{SS}	-5.0 to 0.5	V
Input voltage (1)	V_I	V_{SS} - 0.3 to 0.5	V
Input voltage (2)	V_{IOSC}	V_{SS} - 0.3 to 0.5	V
Operating temperature	Topr	-20 to 70	°C
Storage temperature	Tstg	-65 to 150	°C
Soldering temperature / time	Tsol	260°C, 10sec (lead section)	–

6.2 Recommended Operating Conditions

(Ta=-20 to 70°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply voltage	V_{SS}	V_{DD}=0V	-1.8	-1.5	-1.2	V
Oscillation frequency	f_{OSC}	CR oscillation		65		kHz
		CR oscillation		130		kHz
		CR oscillation		195		kHz
		CR oscillation		260		kHz
Booster capacitor	C_1		0.1			µF

6.3 DC Characteristics

Unless otherwise specified:
V_{DD}=0V, V_{SS}=-1.5V, f_{CLK}=65kHz, Ta=25°C, V_{L1}–V_{L3} are internal voltage, C_1–C_3=0.1µF

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
High level input voltage (1)	V_{IH1}		K00–03, P00–03, P10–13	0.2·V_{SS}		0	V
High level input voltage (2)	V_{IH2}		RESET, TEST	0.1·V_{SS}		0	V
Low level input voltage (1)	V_{IL1}		K00–03, P00–03, P10–13	V_{SS}		0.8·V_{SS}	V
Low level input voltage (2)	V_{IL2}		RESET, TEST	V_{SS}		0.9·V_{SS}	V
High level input current (1)	I_{IH1}	V_{IH1}=0V, No pull-down	K00–03, P00–03, P10–13	0		0.5	µA
High level input current (2)	I_{IH2}	V_{IH2}=0V, Pull-down	K00–03	5		20	µA
High level input current (3)	I_{IH3}	V_{IH3}=0V, Pull-down	P00–03, P10–13 RESET, TEST	25		100	µA
Low level input current	I_{IL}	V_{IL}=V_{SS}	K00–03, P00–03, P10–13 RESET, TEST	-0.5		0	µA
High level output current (1)	I_{OH1}	V_{OH1}=0.1·V_{SS}	R00, R03			-300	µA
High level output current (2)	I_{OH2}	V_{OH2}=0.1·V_{SS}	R01, R02, P00–03, P10–13			-150	µA
Low level output current (1)	I_{OL1}	V_{OL1}=0.9·V_{SS}	R00, R03	1400			µA
Low level output current (2)	I_{OL2}	V_{OL2}=0.9·V_{SS}	R01, R02, P00–03, P10–13	700			µA
Common output current	I_{OH3}	V_{OH3}=-0.05V	COM0–3			-3	µA
	I_{OL3}	V_{OL3}=V_{L3}+0.05V		3			µA
Segment output current	I_{OH4}	V_{OH4}=-0.05V	SEG0–37			-3	µA
(during LCD output)	I_{OL4}	V_{OL4}=V_{L3}+0.05V		3			µA
Segment output current	I_{OH5}	V_{OH5}=0.1·V_{SS}	SEG0–37			-100	µA
(during DC output)	I_{OL5}	V_{OL5}=0.9·V_{SS}		100			µA

6.4 Analog Circuit Characteristics and Current Consumption

LCD drive voltage

• 4.5 V LCD panel, 1/4, 1/3, 1/2 duty, 1/3 bias (V_{L2} is shorted to V_{SS} inside the IC)

Unless otherwise specified:
V_{DD}=0V, V_{SS}=-1.5V, f_{CLK}=65kHz, Ta=25°C, V_{L1}–V_{L3} are internal voltage, C_1–C_3=0.1µF, Internal CR oscillation circuit

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
LCD drive voltage	V_{L1}	Connect 1 MΩ load resistor between V_{DD} and V_{L1} (without panel load)		V_{SS}		V
	V_{L2}	Connect 1 MΩ load resistor between V_{DD} and V_{L2} (without panel load)	$2 \cdot V_{L1}$ - 0.1		$2 \cdot V_{L1}$ ×0.9	V
	V_{L3}	Connect 1 MΩ load resistor between V_{DD} and V_{L3} (without panel load)	$3 \cdot V_{L1}$ - 0.1		$3 \cdot V_{L1}$ ×0.9	V

• 3 V LCD panel, 1/4, 1/3, 1/2 duty, 1/2 bias (V_{L3} is shorted to V_{SS} inside the IC and V_{L1} is shorted to V_{L2} outside the IC)

Unless otherwise specified:
V_{DD}=0V, V_{SS}=-1.5V, f_{CLK}=65kHz, Ta=25°C, V_{L1}–V_{L3} are internal voltage, C_1–C_3=0.1µF, Internal CR oscillation circuit

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
LCD drive voltage	V_{L1}	Connect 1 MΩ load resistor between V_{DD} and V_{L1} (without panel load)		V_{SS}		V
	V_{L2}	Connect 1 MΩ load resistor between V_{DD} and V_{L2} (without panel load)		V_{SS}		V
	V_{L3}	Connect 1 MΩ load resistor between V_{DD} and V_{L3} (without panel load)	$2 \cdot V_{L1}$ - 0.1		$2 \cdot V_{L1}$ ×0.9	V

Current consumption

Unless otherwise specified:
V_{DD}=0V, V_{SS}=-1.5V, Ta=25°C, V_{L1}–V_{L3} are internal voltage, C_1–C_3=0.1µF, R_{CR} is internal resistor, f_{CLK}=65kHz

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Current consumption (f_{OSC}=65kHz)	I_{OP1}	During HALT	Without panel load		4	6	µA
		During execution			8	11	µA
Current consumption (f_{OSC}=130kHz)	I_{OP2}	During HALT	Without panel load		8	11	µA
		During execution			15	21	µA
Current consumption (f_{OSC}=195kHz)	I_{OP3}	During HALT	Without panel load		11	15	µA
		During execution			20	26	µA
Current consumption (f_{OSC}=260kHz)	I_{OP4}	During HALT	Without panel load		14	19	µA
		During execution			26	34	µA
Current consumption	I_{OP5}	During SLEEP	Without panel load			0.3	µA

6.5 Oscillation Characteristics

Oscillation characteristics will vary according to different conditions (elements used, board pattern). Use the following characteristics are as reference values.

Unless otherwise specified:
VDD=0V, VSS=-1.5V, Ta=25°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation frequency dispersion	fOSC1	VSS=-1.5V	42.3	65	87.8	kHz
Oscillation start time	tsta	VSS=-1.5V			3	mS
Frequency v.s. voltage deviation	df1/dv	VSS=-1.2 to -1.8V	-30		30	%
Frequency v.s. temperature deviation	df1/dta	VSS=-1.5V, Ta=-25 to 75°C	-15		15	%

Unless otherwise specified:
VDD=0V, VSS=-1.5V, Ta=25°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation frequency dispersion	fOSC2		84.5	130	175.5	kHz
Oscillation start time	tsta	VSS=-1.5V			3	mS
Frequency v.s. voltage deviation	df2/dv	VSS=-1.2 to -1.8V	-30		30	%
Frequency v.s. temperature deviation	df2/dta	VSS=-1.5V, Ta=-25 to 75°C	-15		15	%

Unless otherwise specified:
VDD=0V, VSS=-1.5V, Ta=25°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation frequency dispersion	fOSC3		136.5	195	253.5	kHz
Oscillation start time	tsta	VSS=-1.5V			3	mS
Frequency v.s. voltage deviation	df3/dv	VSS=-1.2 to -1.8V	-30		30	%
Frequency v.s. temperature deviation	df3/dta	VSS=-1.5V, Ta=-25 to 75°C	-15		15	%

Unless otherwise specified:
VDD=0V, VSS=-1.5V, Ta=25°C

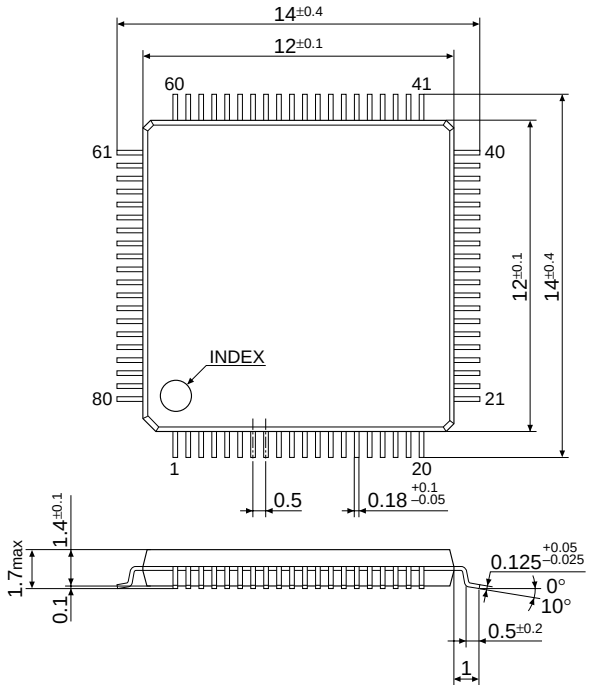
Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation frequency dispersion	fOSC4	VSS=-1.5V	182	260	338	kHz
Oscillation start time	tsta	VSS=-1.5V			3	mS
Frequency v.s. voltage deviation	df4/dv	VSS=-1.2 to -1.8V	-30		30	%
Frequency v.s. temperature deviation	df4/dta	VSS=-1.5V, Ta=-25 to 75°C	-15		15	%

CHAPTER 7 PACKAGE

7.1 Plastic Package

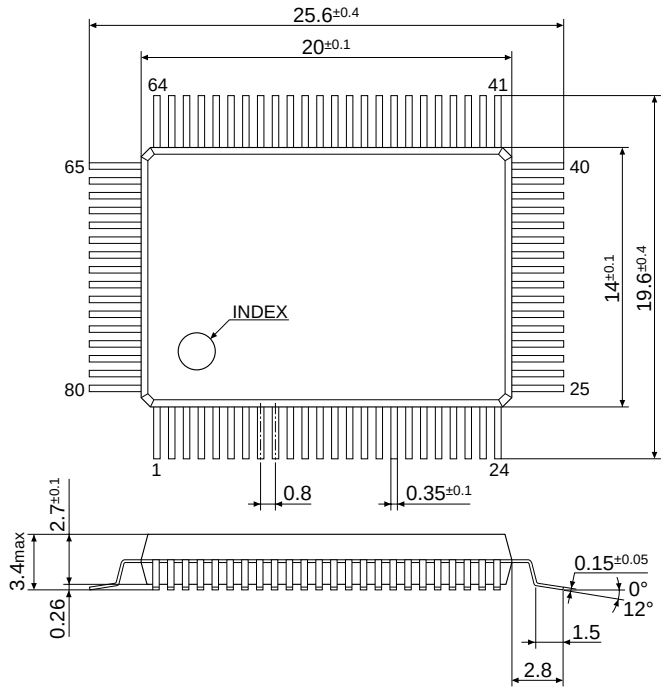
QFP14-80pin

(Unit: mm)



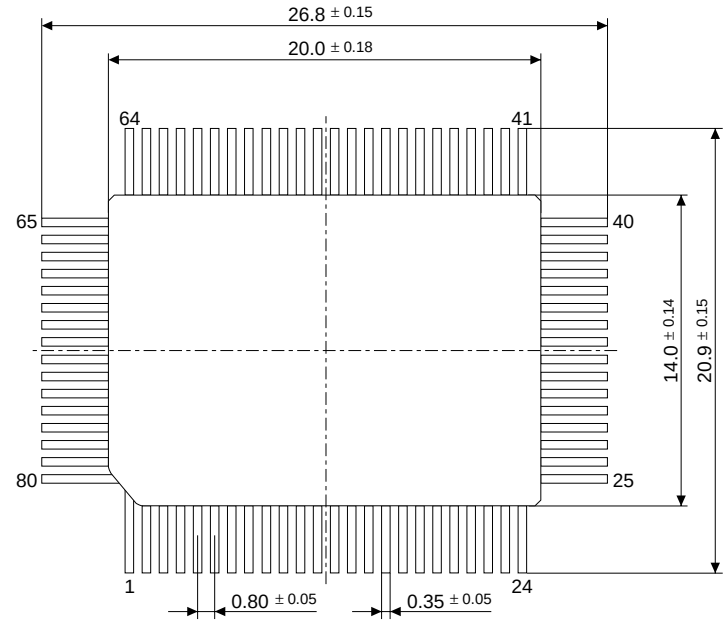
QFP5-80pin

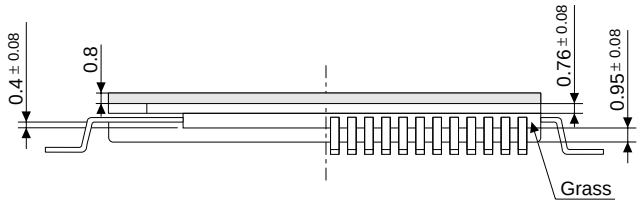
(Unit: mm)



7.2 Ceramic Package for Test Samples

(Unit: mm)



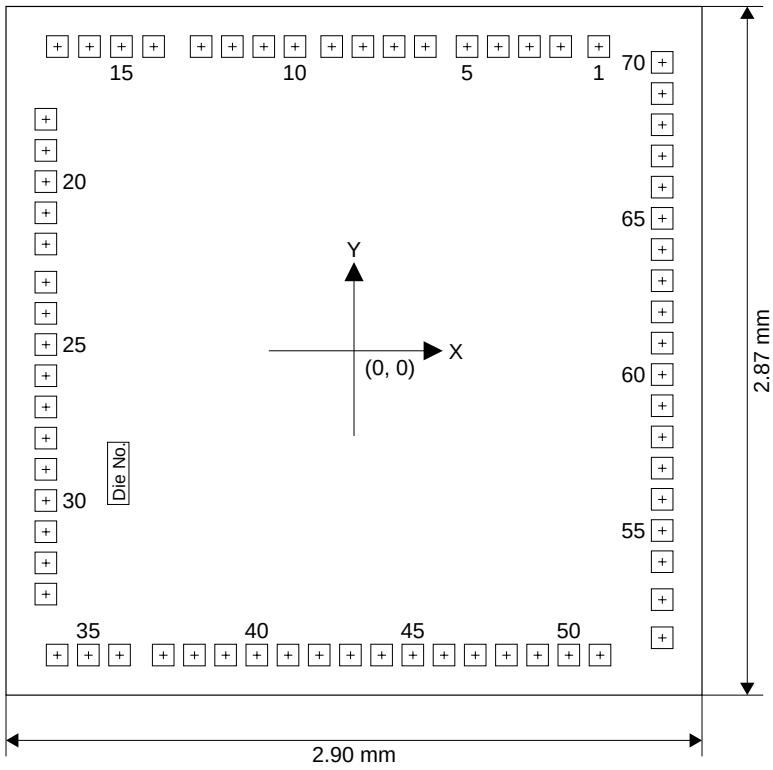


No.	Name	No.	Name	No.	Name	No.	Name
1	SEG35	21	R03	41	N.C.	61	N.C.
2	N.C.	22	N.C.	42	N.C.	62	N.C.
3	N.C.	23	N.C.	43	SEG1	63	N.C.
4	SEG36	24	N.C.	44	SEG2	64	SEG19
5	SEG37	25	V_{SS}	45	SEG3	65	TEST
6	K03	26	RESET	46	SEG4	66	SEG20
7	K02	27	N.C.	47	SEG5	67	SEG21
8	K01	28	N.C.	48	SEG6	68	SEG22
9	K00	29	N.C.	49	SEG7	69	SEG23
10	P13	30	V_{DD}	50	SEG8	70	SEG24
11	P12	31	V_{L3}	51	SEG9	71	SEG25
12	P11	32	V_{L2}	52	SEG10	72	SEG26
13	P10	33	V_{L1}	53	SEG11	73	SEG27
14	P03	34	CB	54	SEG12	74	SEG28
15	P02	35	CA	55	SEG13	75	SEG29
16	P01	36	COM3	56	SEG14	76	SEG30
17	P00	37	COM2	57	SEG15	77	SEG31
18	R02	38	COM1	58	SEG16	78	SEG32
19	R01	39	COM0	59	SEG17	79	SEG33
20	R00	40	SEG0	60	SEG18	80	SEG34

N.C. : No Connection

CHAPTER 8 PAD LAYOUT

8.1 Pad layout diagram



Chip thickness: 400 µm
Pad opening: 95 µm

8.2 Pad coordinates

(unit: µm)

No.	Pad name	X	Y	No.	Pad name	X	Y	No.	Pad name	X	Y
1	SEG37	1,020	1,268	25	V_{L2}	-1,284	26	49	SEG16	765	-1,268
2	K03	861	1,268	26	V_{L1}	-1,284	-104	50	SEG17	895	-1,268
3	K02	731	1,268	27	CB	-1,284	-234	51	SEG18	1,025	-1,268
4	K01	601	1,268	28	CA	-1,284	-364	52	SEG19	1,284	-1,196
5	K00	471	1,268	29	COM3	-1,284	-494	53	TEST	1,284	-1,037
6	P13	297	1,268	30	COM2	-1,284	-624	54	SEG20	1,284	-879
7	P12	167	1,268	31	COM1	-1,284	-754	55	SEG21	1,284	-749
8	P11	37	1,268	32	COM0	-1,284	-884	56	SEG22	1,284	-619
9	P10	-93	1,268	33	SEG0	-1,284	-1,014	57	SEG23	1,284	-489
10	P03	-246	1,268	34	SEG1	-1,237	-1,268	58	SEG24	1,284	-359
11	P02	-376	1,268	35	SEG2	-1,107	-1,268	59	SEG25	1,284	-229
12	P01	-507	1,268	36	SEG3	-977	-1,268	60	SEG26	1,284	-99
13	P00	-637	1,268	37	SEG4	-795	-1,268	61	SEG27	1,284	32
14	R02	-835	1,268	38	SEG5	-665	-1,268	62	SEG28	1,284	162
15	R01	-969	1,268	39	SEG6	-535	-1,268	63	SEG29	1,284	292
16	R00	-1,102	1,268	40	SEG7	-405	-1,268	64	SEG30	1,284	422
17	R03	-1,236	1,268	41	SEG8	-275	-1,268	65	SEG31	1,284	552
18	V_{SS}	-1,284	965	42	SEG9	-145	-1,268	66	SEG32	1,284	682
19	RESET	-1,284	835	43	SEG10	-15	-1,268	67	SEG33	1,284	812
20	N.C.	-1,284	705	44	SEG11	115	-1,268	68	SEG34	1,284	942
21	N.C.	-1,284	575	45	SEG12	245	-1,268	69	SEG35	1,284	1,072
22	N.C.	-1,284	445	46	SEG13	375	-1,268	70	SEG36	1,284	1,202
23	V_{DD}	-1,284	286	47	SEG14	505	-1,268	–			
24	V_{L3}	-1,284	156	48	SEG15	635	-1,268	–			

CHAPTER 9 PRECAUTIONS ON MOUNTING

<Reset Circuit>

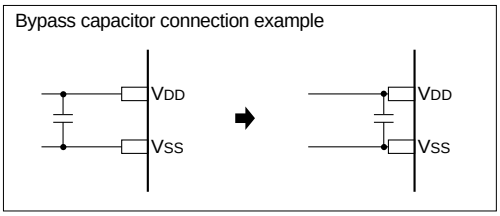
- The power-on reset signal which is input to the RESET terminal changes depending on conditions (power rise time, components used, board pattern, etc.).
  Decide the time constant of the capacitor and resistor after enough tests have been completed with the application product.
  When the built-in pull-down resistor is added to the RESET terminal by mask option, take into consideration dispersion of the resistance for setting the constant.
- In order to prevent any occurrences of unnecessary resetting caused by noise during operating, components such as capacitors and resistors should be connected to the RESET terminal in the shortest line.

<Power Supply Circuit>

- Sudden power supply variation due to noise may cause malfunction. Consider the following points to prevent this:

  (1) The power supply should be connected to the V_{DD} and V_{SS} terminal with patterns as short and large as possible.

  (2) When connecting between the V_{DD} and V_{SS} terminals with a bypass capacitor, the terminals should be connected as short as possible.



  (3) Components which are connected to the V_{L1}, V_{L2}, V_{L3} terminals, such as a capacitor, should be connected in the shortest line.

<Arrangement of Signal Lines>

- In order to prevent generation of electromagnetic induction noise caused by mutual inductance, do not arrange a large current signal line near the circuits that are sensitive to noise.

<Precautions for Visible Radiation (when bare chip is mounted)>

- Visible radiation causes semiconductor devices to change the electrical characteristics. It may cause this IC to malfunction. When developing products which use this IC, consider the following precautions to prevent malfunctions caused by visible radiations.

  (1) Design the product and implement the IC on the board so that it is shielded from visible radiation in actual use.

  (2) The inspection process of the product needs an environment that shields the IC from visible radiation.

  (3) As well as the face of the IC, shield the back and side too.

EPSON International Sales Operations

AMERICA

EPSON ELECTRONICS AMERICA, INC.

- HEADQUARTERS -
1960 E. Grand Avenue
El Segundo, CA 90245, U.S.A.
Phone: +1-310-955-5300 Fax: +1-310-955-5400

- SALES OFFICES -

West
150 River Oaks Parkway
San Jose, CA 95134, U.S.A.
Phone: +1-408-922-0200 Fax: +1-408-922-0238

Central
1450 East American Lane, Suite 1550
Schaumburg, IL 60173, U.S.A.
Phone: +1-847-517-7667 Fax: +1-847-517-7601

101 Virginia Street, Suite 290
Crystal Lake, IL 60014, U.S.A.
Phone: +1-815-455-7630 Fax: +1-815-455-7633

Northeast
301 Edgewater Place, Suite 120
Wakefield, MA 01880, U.S.A.
Phone: +1-781-246-3600 Fax: +1-781-246-5443

Southeast
4300 Six Forks Road, Suite 430
Raleigh, NC 27609, U.S.A.
Phone: +1-919-781-7667 Fax: +1-919-781-6778

1700 Spinnaker Drive
Alpharetta, GA 30005, U.S.A.
Phone: +1-770-754-4872 Fax: +1-770-753-0601

EUROPE

EPSON EUROPE ELECTRONICS GmbH

- HEADQUARTERS -
Riesstrasse 15
80992 Muenchen, GERMANY
Phone: +49-(0)89-14005-0 Fax: +49-(0)89-14005-110

- GERMANY -
SALES OFFICE
Altstadtstrasse 176
51379 Leverkusen, GERMANY
Phone: +49-(0)217-15045-0 Fax: +49-(0)217-15045-10

- UNITED KINGDOM -
UK BRANCH OFFICE
G6 Doncastle House, Doncastle Road
Bracknell, Berkshire RG12 8PE, ENGLAND
Phone: +44-(0)1344-381700 Fax: +44-(0)1344-381701

- FRANCE -
FRENCH BRANCH OFFICE
1 Avenue de l' Atlantique, LP 915 Les Conquerants
Z.A. de Courtaboeuf 2, F-91976 Les Ulis Cedex, FRANCE
Phone: +33-(0)1-64862350 Fax: +33-(0)1-64862355

ASIA

- HONG KONG, CHINA -
EPSON HONG KONG LTD.
20/F., Harbour Centre, 25 Harbour Road
Wanchai, HONG KONG
Phone: +852-2585-4600 Fax: +852-2827-4346
Telex: 65542 EPSCO HX

- CHINA -
SHANGHAI EPSON ELECTRONICS CO., LTD.
4F, Bldg., 27, No. 69, Gui Jing Road
Caohejing, Shanghai, CHINA
Phone: 21-6485-5552 Fax: 21-6485-0775

- TAIWAN, R.O.C. -
EPSON TAIWAN TECHNOLOGY & TRADING LTD.
10F, No. 287, Nanking East Road, Sec. 3
Taipei, TAIWAN, R.O.C.
Phone: 02-2717-7360 Fax: 02-2712-9164
Telex: 24444 EPSONTB

HSINCHU OFFICE
13F-3, No. 295, Kuang-Fu Road, Sec. 2
HsinChu 300, TAIWAN, R.O.C.
Phone: 03-573-9900 Fax: 03-573-9169

- SINGAPORE -
EPSON SINGAPORE PTE., LTD.
No. 1 Temasek Avenue, #36-00
Millenia Tower, SINGAPORE 039192
Phone: +65-337-7911 Fax: +65-334-2716

- KOREA -
SEIKO EPSON CORPORATION
KOREA OFFICE
50F, KLI 63 Bldg., 60 Yoido-Dong
Youngdeungpo-Ku, Seoul, 150-010, KOREA
Phone: 02-784-6027 Fax: 02-767-3677

- JAPAN -
SEIKO EPSON CORPORATION
ELECTRONIC DEVICES MARKETING DIVISION

Electronic Device Marketing Department
IC Marketing & Engineering Group
421-8, Hino, Hino-shi, Tokyo 191-8501, JAPAN
Phone: +81-(0)42-587-5816 Fax: +81-(0)42-587-5624

ED International Marketing Department I
(Europe & U.S.A.)
421-8, Hino, Hino-shi, Tokyo 191-8501, JAPAN
Phone: +81-(0)42-587-5812 Fax: +81-(0)42-587-5564

ED International Marketing Department II
(Asia)
421-8, Hino, Hino-shi, Tokyo 191-8501, JAPAN
Phone: +81-(0)42-587-5814 Fax: +81-(0)42-587-5110

In pursuit of **“Saving” Technology**, Epson electronic devices.
Our lineup of semiconductors, liquid crystal displays and quartz devices
assists in creating the products of our customers’ dreams.
Epson IS energy savings.

EPSON

SEIKO EPSON CORPORATION
ELECTRONIC DEVICES MARKETING DIVISION

■ Electronic devices information on Epson WWW server

http://www.epson.co.jp

Issue APRIL 1999, Printed in Japan Ⓜ A