

E0C6215

4-bit Single Chip Microcomputer



- Core CPU Architecture
- Presetable Timer
- Analog Multiplexer Comparator
- SVD Circuit/Watchdog Timer

■ DESCRIPTION

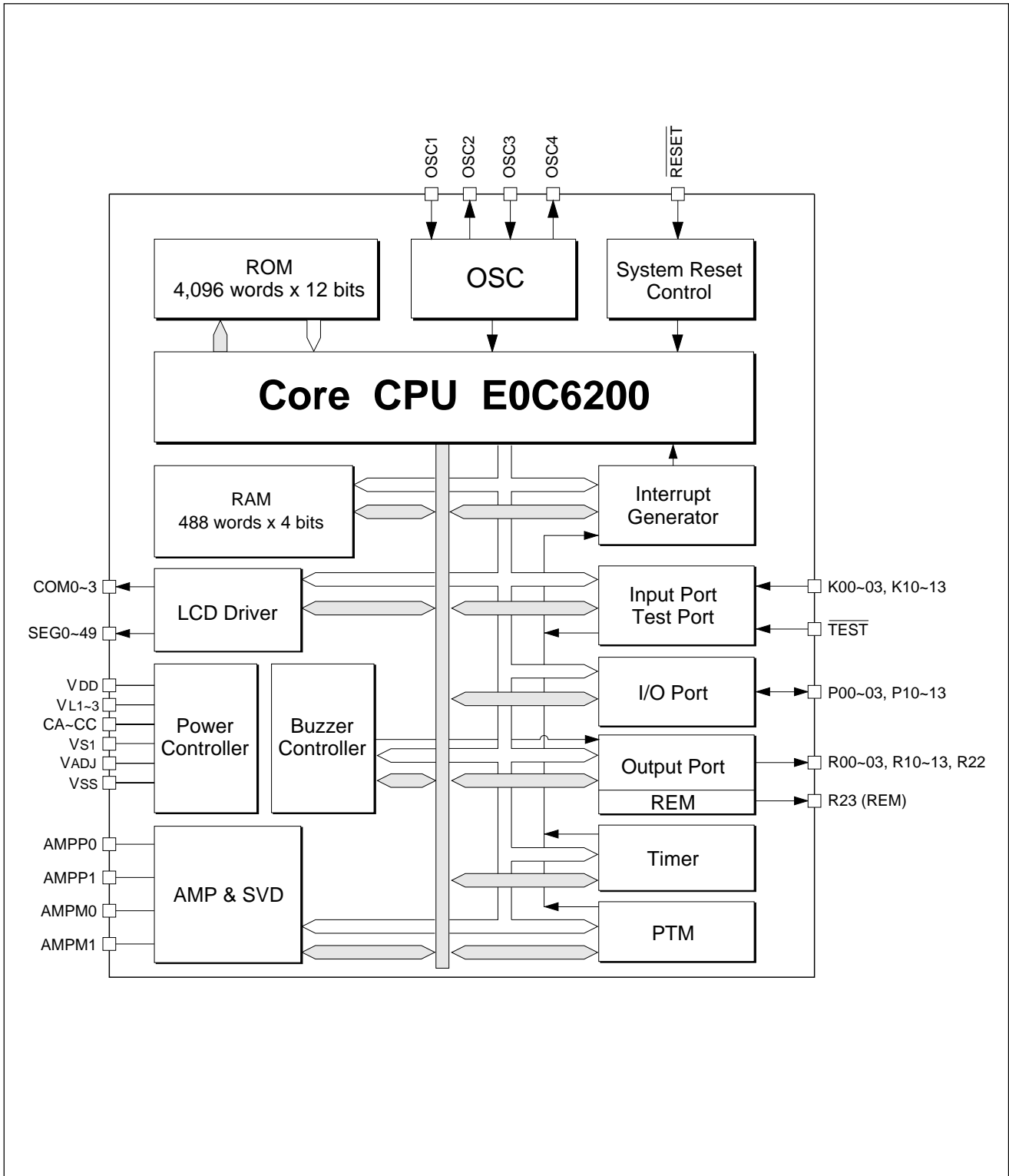
The E0C6215 is an advanced single-chip CMOS 4-bit microcomputer consisting of the E0C6200 CMOS 4-bit core CPU. It also contains the ROM, RAM, LCD driver, dual timers and comparators to provide an excellent solution for various systems requiring low-power consumption.

■ FEATURES

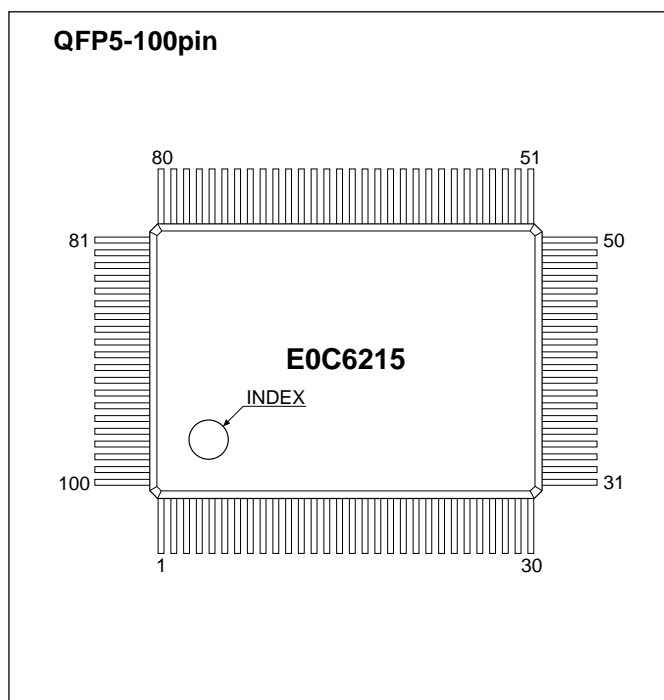
- CMOS LSI 4-bit parallel processing
- Twin clock 32.768kHz (Typ.) Crystal oscillation circuit
455kHz (Typ.) CR or Ceramic oscillation circuit
(selectable by mask option)
- Instruction set 106 instructions
- Instruction cycle time 153μsec, 214μsec or 366μsec at 32kHz
(depending on instruction set)
11μsec, 15μsec or 26μsec at 455kHz
(depending on instruction set)
- ROM capacity 4,096 × 12 bits
- RAM capacity 488 × 4 bits
- Input port 8 bits (pull-up resistors are available by mask option)
- Output port 9 bits (clock output or buzzer output is available by mask option)
- I/O port 8 bits
- Remote control carrier (REM) output 1 bit (hardware/software timer is selectable by software)
- LCD driver 50 segments × 3 commons or 50 segments × 4 commons
(1/3 or 1/4 duty is selectable by mask option)
- Built-in LCD power circuit Voltage regulator (doubler and tripler)
- Built-in SVD circuit 2.3V ± 0.1V (supply voltage detector)
- Built-in Op-amp Op-amp for 2-channel analog multiplexer and analog comparator
- Programmable timer 8-bit presetable count down timer
- Built-in watchdog timer (Mask option)
- Interrupts External : Input interrupt 2 lines
Internal : Timer interrupt 1 line (3ch.)
Presetable timer interrupt 1 line
REM interrupt 1 line
- Supply voltage 3.0V (2.2V to 3.5V)
- Current consumption HALT mode (32.768kHz) : 3μA (Typ.)
OPERATING mode (455kHz) : 150μA (Typ.)
- Package QFP5-100pin (plastic), QFP15-100pin (plastic)
Die form

E0C6215

■ BLOCK DIAGRAM



PIN CONFIGURATION



No.	Pin name	No.	Pin name	No.	Pin name	No.	Pin name
1	SEG0	26	R01	51	R22	76	SEG25
2	COM3	27	R02	52	SEG49	77	SEG24
3	COM2	28	R03	53	SEG48	78	SEG23
4	COM1	29	R23(REM)	54	SEG47	79	SEG22
5	COM0	30	R10	55	SEG46	80	SEG21
6	CC	31	R11	56	SEG45	81	SEG20
7	CB	32	R12	57	SEG44	82	SEG19
8	CA	33	R13	58	SEG43	83	SEG18
9	VL3	34	P00	59	SEG42	84	SEG17
10	VL2	35	P01	60	SEG41	85	SEG16
11	RESET	36	P02	61	SEG40	86	SEG15
12	VADJ	37	P03	62	SEG39	87	SEG14
13	VL1	38	P10	63	SEG38	88	SEG13
14	AMPP1	39	P11	64	SEG37	89	SEG12
15	AMPM1	40	P12	65	SEG36	90	SEG11
16	AMPP0	41	P13	66	SEG35	91	SEG10
17	AMPM0	42	K00	67	SEG34	92	SEG9
18	VDD	43	K01	68	SEG33	93	SEG8
19	OSC1	44	K02	69	SEG32	94	SEG7
20	OSC2	45	K03	70	SEG31	95	SEG6
21	Vs1	46	K10	71	SEG30	96	SEG5
22	OSC3	47	K11	72	SEG29	97	SEG4
23	OSC4	48	K12	73	SEG28	98	SEG3
24	Vss	49	K13	74	SEG27	99	SEG2
25	R00	50	TEST	75	SEG26	100	SEG1

N.C. = No Connection

PIN DESCRIPTION

Pin name	Pin No.	In/Out	Function
VDD	18	I	Power source (+) terminal
VSS	24	I	Power source (-) terminal
Vs1	21	O	Oscillation and internal logic system regulated voltage output terminal
VL1	13	O	LCD system regulated voltage output terminal (VDD-VL)
VL2	10	O	LCD system booster output terminal (VDD-2VL)
VL3	9	O	LCD system booster output terminal (VDD-3VL)
VADJ	12	I	VL input adjustment terminal
CA-CC	8-6	-	Booster capacitor connecting terminal
OSC1	19	I	Crystal oscillation input terminal
OSC2	20	O	Crystal oscillation output terminal
OSC3	22	I	Ceramic or CR oscillation input terminal
OSC4	23	O	Ceramic or CR oscillation output terminal
K00-03, K10-13	42-49	I	Input terminal
P00-03, P10-13	34-41	I/O	I/O terminal
R00-03, R10, R11	25-28, 30, 31	O	Output terminal
R12	32	O	Output terminal (DC, FOUT or BZ output may be selected by mask option)
R13	33	O	Output terminal (DC or BZ output may be selected by mask option)
R22	51	O	Output terminal
R23(REM)	29	O	Remote control carrier output terminal
AMPP1	14	I	Analog comparator 1 non-inverted input terminal
AMPM1	15	I	Analog comparator 1 inverted input terminal
AMPP0	16	I	Analog comparator 0 non-inverted input terminal
AMPM0	17	I	Analog comparator 0 inverted input terminal
SEG0-49	1, 100-52	O	LCD segment output terminal (Convertible to DC output by mask option)
COM0-3	5-2	O	LCD common output terminal
RESET	11	I	Initial reset input terminal
TEST	50	I	Test input terminal

■ ELECTRICAL CHARACTERISTICS

● Absolute Maximum Ratings

(V_{DD}=0V)

Rating	Symbol	Value	Unit
Supply voltage	V _{SS}	-5.2 to 0.5	V
Input voltage (1)	V _I	V _{SS} - 0.3 to 0.3	V
Input voltage (2)	V _{Iosc}	V _{S1} - 0.3 to 0.3	V
Operating temperature	T _{opr}	-20 to 70	°C
Storage temperature	T _{stg}	-65 to 150	°C
Soldering temperature / Time	T _{sol}	260°C, 10sec (lead section)	—
Permissible dissipation *1	P _d	250	mW

*1: In case of plastic package (QFP5-100pin).

● Recommended Operating Conditions

(T_a=-20 to 70°C)

Condition	Symbol	Remark	Min.	Typ.	Max.	Unit
Supply voltage	V _{SS}	V _{DD} =0V	-3.5	-3.0	-2.2	V
Oscillation frequency (1)	f _{osc1}		—	32.768	—	kHz
Oscillation frequency (2)	f _{osc3}	duty 50±5%	50	455	500	kHz

● DC Characteristics

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-2.2 to -3.5V, V_{L3}=3.0V, T_a=-20 to 70°C)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
High level input voltage (1)	V _{IH1}	K00-K03, K10-K13 P00-P03, P10-P13	0.2•V _{SS}		0	V
High level input voltage (2)	V _{IH2}	RESET	0.1•V _{SS}		0	V
Low level input voltage (1)	V _{IL1}	K00-K03, K10-K13 P00-P03, P10-P13	V _{SS}		0.8•V _{SS}	V
Low level input voltage (2)	V _{IL2}	RESET	V _{SS}		0.9•V _{SS}	V
High level input current	I _{IH}	V _{IH} =V _{DD} K00-K03, K10-K13 P00-P03, P10-P13 RESET	—		1	μA
Low level input current (1)	I _{IL1}	V _{IL1} =V _{SS} , No pull up resistor	-1		—	μA
Low level input current (2)	I _{IL2}	V _{IL2} =V _{SS} , With pull up resistor	-5		-0.35	μA
Low level input current (3)	I _{IL3}	V _{IL3} =V _{SS} Pull up, pull up+feedback	-5		-0.35	μA
Low level input current (4)	I _{IL4}	V _{IL4} =0.2•V _{SS} Pull up, pull up+feedback	-30		—	μA
Low level input current (5)	I _{IL5}	V _{IL5} =V _{SS}	-15		-2	μA
High level output current (1)	I _{OH1}	V _{OH1} =0.1•V _{SS}			-250	μA
High level output current (2)	I _{OH2}	V _{OH2} =0.1•V _{SS}			-1.8	mA
High level output current (3)	I _{OH3}	V _{OH3} =0.1•V _{SS}			-1.0	mA
High level output current (4)	I _{OH4}	V _{OH4} =0.1•V _{SS}			-100	μA
Low level output current (1)	I _{OL1}	V _{OL1} =0.9•V _{SS}	1.0			mA
Low level output current (2)	I _{OL2}	V _{OL2} =0.9•V _{SS}	1.0			mA
Low level output current (3)	I _{OL3}	V _{OL3} =0.9•V _{SS}	1.0			mA
Low level output current (4)	I _{OL4}	V _{OL4} =0.9•V _{SS}	140			μA
Common output current	I _{OH5}	V _{OH5} =-0.05V			-3.0	μA
	I _{OL5}	V _{OL5} =V _{L3} +0.05V	3.0			μA
Segment output current (during LCD output)	I _{OH6}	V _{OH6} =-0.05V			-3.0	μA
	I _{OL6}	V _{OL6} =V _{L3} +0.05V	3.0			μA
Segment output current (during DC output)	I _{OH7}	V _{OH7} =0.1•V _{SS}			-50	μA
	I _{OL7}	V _{OL7} =0.9•V _{SS}	70			μA

*1: Only at read cycle using internal program

● Analog Circuit Characteristics and Current Consumption

(Unless otherwise specified: $V_{DD}=0V$, $V_{SS}=-2.2$ to $-3.5V$, $T_a=25^\circ C$)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Internal voltage	VL1	$V_{ADJ}=VL1$, $I_{L1}=5\mu A$	-1.13	-1.05	-0.98	V
	VL2	Connect $1M\Omega$ load resistor between V_{DD} and VL2 (without panel load)	$2 \cdot VL1$		$2 \cdot VL1 + 0.1$	V
	VL3	Connect $1M\Omega$ load resistor between V_{DD} and VL3 (without panel load)	$3 \cdot VL1$		$3 \cdot VL1 + 0.3$	V
SVD voltage	VSVD		-2.4	-2.3	-2.2	V
SVD circuit response time	t_{SVD}				100	μS
AMP offset voltage	VOF	$V_{SS}=-3.0V$, $V_I=V_{DD}-1.1V$ to $V_{SS}+0.1V$			10	mV
AMP response time	t_{AMP}	$V_{SS}=-3.0V$, $V_{AMPP}=-1.5V$, $V_{AMPM}=V_{AMPP} \pm 15mV$			1.2	mS
Current consumption	IOP	During HALT *1		3	7.5	μA
		During operation with OSC1 *2	$V_{ADJ}=VL1$	4	9	μA
		During operation with OSC3 *3	Without panel load	150	300	μA

*1: OSCC="0"

*2: Execution duty: 10% (The SVD and AMP circuits are in the OFF status.), OSCC="0"

*3: Ceramic oscillation (455kHz) or CR oscillation ($R=150k\Omega$), OSCC="1"

● Oscillation Characteristics

The oscillation characteristics change depending on the conditions (components used, board pattern, etc.). Use the following characteristics as reference values.

OSC1 (Crystal)

(Unless otherwise specified: $V_{DD}=0V$, $V_{SS}=-3.0V$, Crystal: C-002R ($C_I=35k\Omega$), $C_G=25pF$, C_D =built-in, $T_a=25^\circ C$)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start time	t_{sta}	$V_{SS}=-2.2$ to $-3.5V$	–	–	5	Sec
Built-in capacitance (drain)	C_D	Package as assembled	–	22	–	pF
		Bare chip	–	21	–	pF
Frequency/voltage deviation	$\partial f/\partial V$	$V_{SS}=-2.2$ to $-3.5V$	–	–	5	ppm
Frequency/IC deviation	$\partial f/\partial IC$		-10	–	10	ppm
Frequency adjustment range	$\partial f/\partial C_G$	$C_G=5$ to $25pF$	40	–	–	ppm
Harmonic oscillation start voltage	V_{hho}	$C_G=5pF$	–	–	-3.5	V
Permitted leak resistance	R_{leak}	Between OSC1 and other pins	200	–	–	$M\Omega$

OSC3 (CR oscillation)

(Unless otherwise specified: $V_{DD}=0V$, $V_{SS}=-3.0V$, $R_{CR}=150k\Omega$, $T_a=25^\circ C$)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation frequency	fosc3		–	280	–	kHz
Oscillation start voltage	V_{sta}	(Vss)	-2.2	–	–	V
Oscillation start time	t_{sta}	$V_{SS}=-2.2$ to $-3.5V$	–	3	–	mS
Oscillation stop voltage	V_{stp}	(Vss)	-2.2	–	–	V

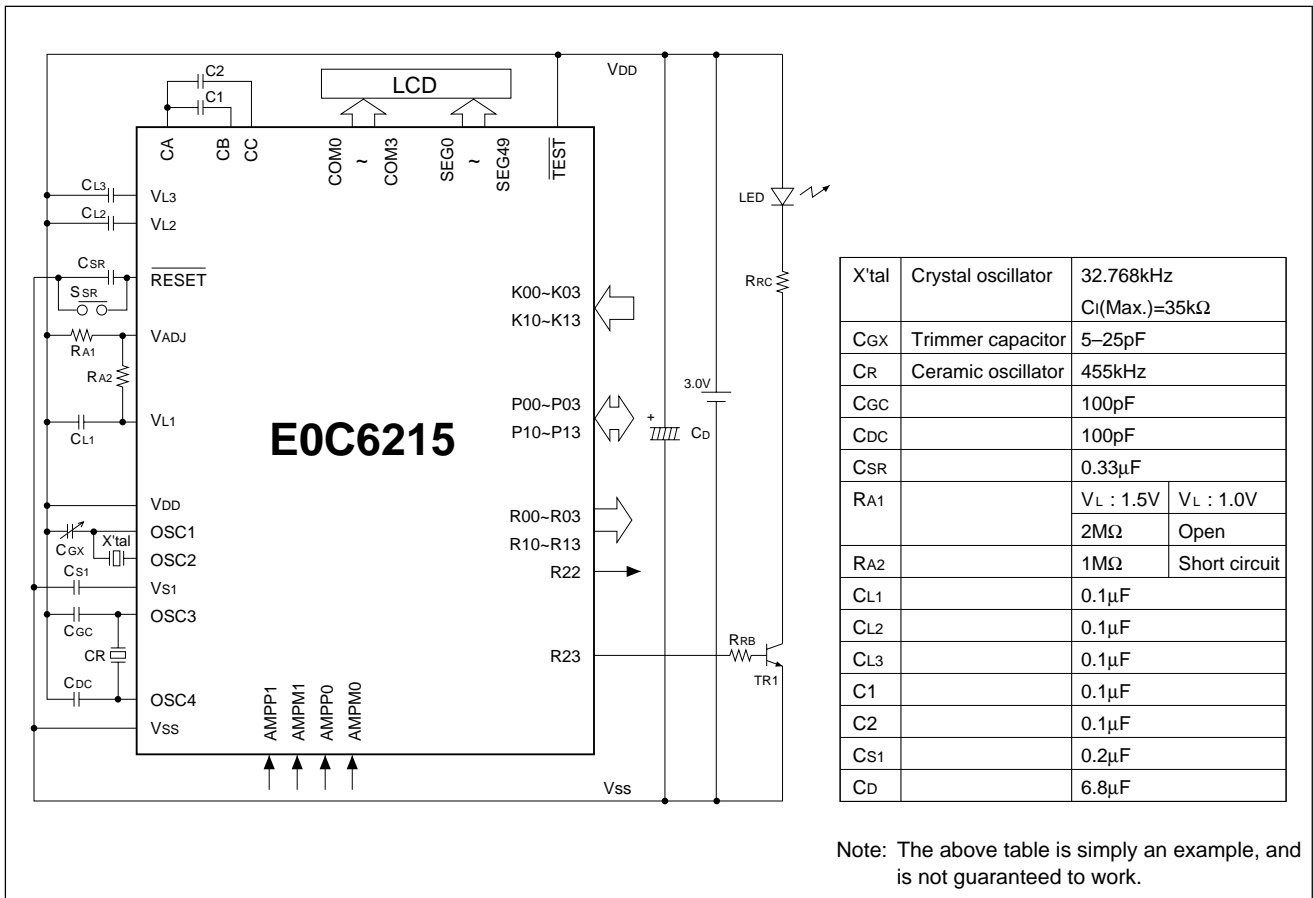
OSC3 (Ceramic)

(Unless otherwise specified: $V_{DD}=0V$, $V_{SS}=-3.0V$, Ceramic: CSB455E (Murata Mfg. Co.), $C_{GC}=C_{DC}=100pF$, $T_a=25^\circ C$)

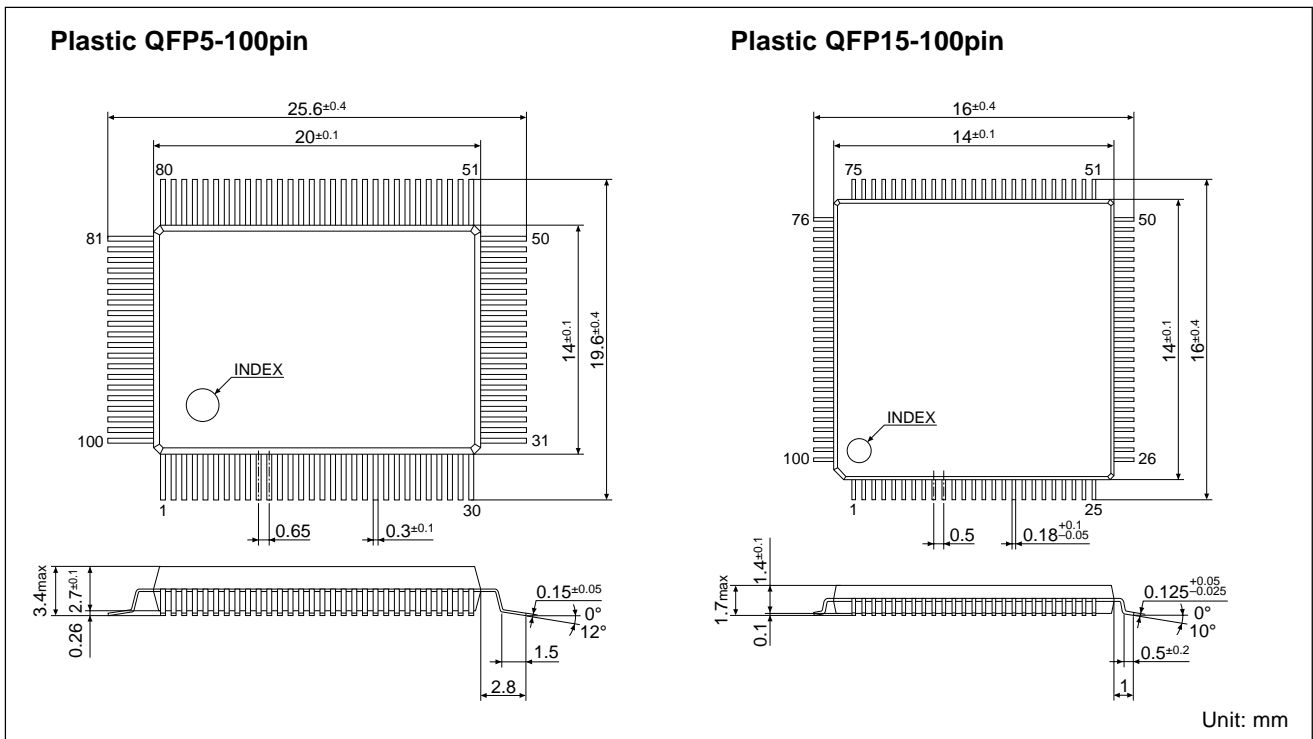
Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start voltage	V_{sta}	(Vss)	-2.2	–	–	V
Oscillation start time	t_{sta}	$V_{SS}=-2.2$ to $-3.5V$	–	3	–	mS
Oscillation stop voltage	V_{stp}	(Vss)	-2.2	–	–	V

E0C6215

■ BASIC EXTERNAL CONNECTION DIAGRAM



■ PACKAGE DIMENSIONS



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