EPSON

E0C6235

4-bit Single Chip Microcomputer

Low Voltage Operation Products

- Core CPU Architecture
- Programmable SVD Circuit
- Event Counter/Sound Generator

■ DESCRIPTION

The E0C6235 is an advanced single-chip CMOS 4-bit microcomputer consisting of the E0C6200 CMOS 4-bit core CPU. It also contains the ROM, RAM, LCD driver, event counter with dial input feature, programmable SVD circuit, stopwatch counter and time base counter. With wide operating voltage range and low power consumption, the E0C6235 provides an excellent solution for the low-power consumption systems with manganese dry cell.

■ FEATURES

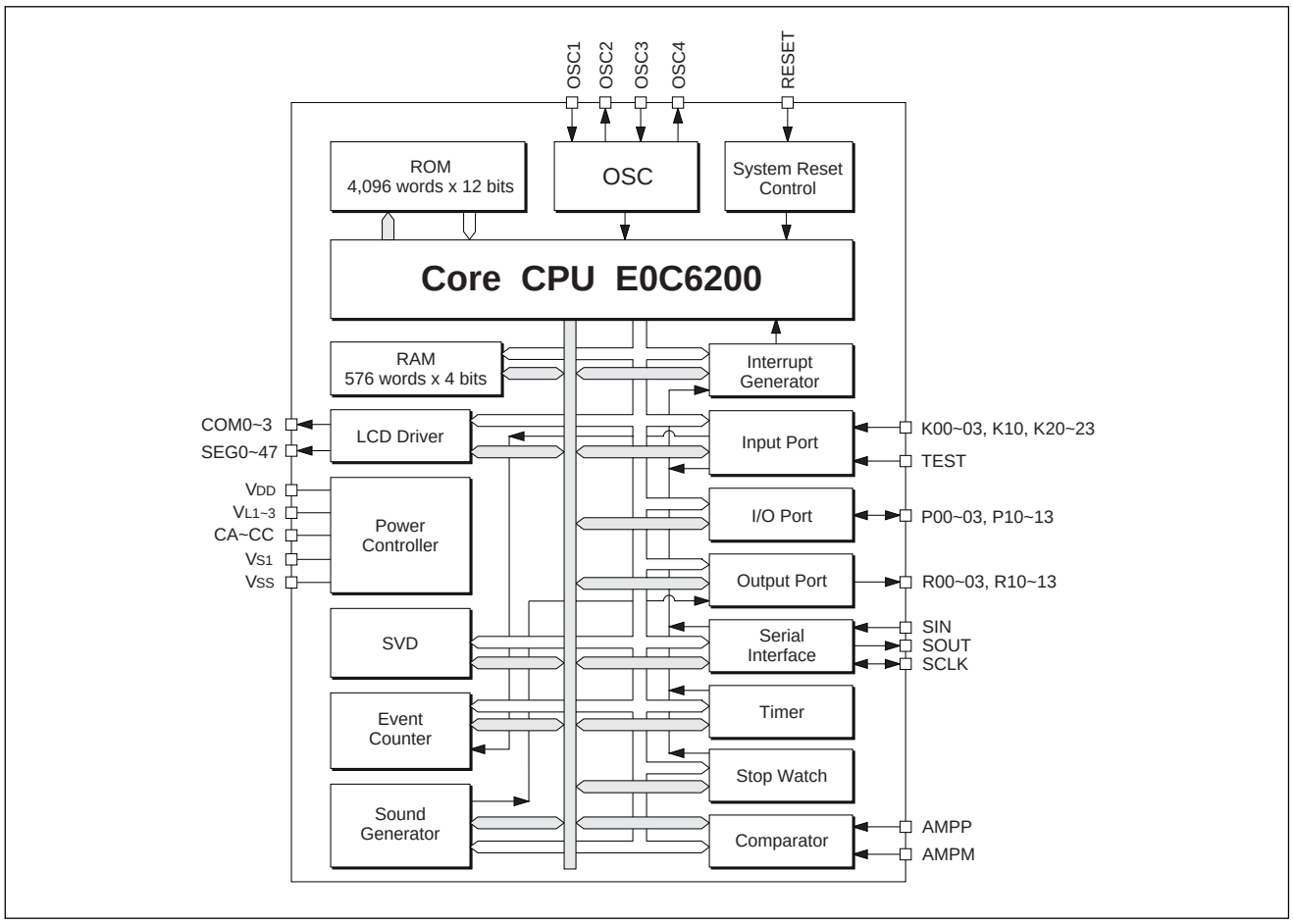
- CMOS LSI 4-bit parallel processing
- Clock ..... 32.768kHz/38.400kHz/500kHz (Typ.)
- Instruction set ..... 108 instructions
- Instruction cycle time ..... 153µsec, 214µsec or 366µsec at 32kHz
  130µsec, 182µsec or 313µsec at 38.4kHz
  10µsec, 14µsec or 24µsec at 500kHz
  (depending on instruction)
- ROM capacity ..... 4,096 × 12 bits
- RAM capacity ..... 576 × 4 bits (LCD segment memory jointly used)
- Input port ..... 9 bits (pull-down resistors are available by mask option)
- Output port ..... 8 bits (clock output or buzzer output is available by mask option)
- I/O port ..... 8 bits (pull-down resistors are available by mask option)
- Serial I/O port ..... 1 port (clock sync.)
- Event counter ..... 8 bits (dial input function)
- LCD driver ..... 48 segments × 3 commons/48 segments × 4 commons
  (1/3 or 1/4 duty is selectable by mask option)
- Built-in LCD power circuit ..... Voltage regulator circuit; doubler or tripler
- Built-in SVD circuit ..... 1.2V fixed (E0C62L35)
  1.05 to 1.40V programmable (E0C62L35)
  2.20 to 2.55V programmable (E0C6235/62A35)
- Built-in AMP ..... Operational AMP for MOS input analog comparator
- Built-in watchdog timer
- Built-in time base counter ..... 2 lines
- Interrupts ..... External : Input interrupt 3 lines
  Internal : Timer interrupt 1 line
  Serial I/O interrupt 1 line
  Stopwatch interrupt 1 line
- Built-in sound generator ..... With digital envelope (8 sounds programmable)
- Current consumption ..... E0C62L35 HALT mode (32kHz) : 1.5µA (Typ.)
  E0C6235 HALT mode (32kHz) : 1.8µA (Typ.)
  E0C62A35 HALT mode (32kHz) : 2.0µA (Typ.)
  OPERATING mode (500kHz) : 130µA (Typ.)
- Package ..... QFP5-100pin (plastic), QFP15-100pin (plastic)
  Die form

■ LINE UP

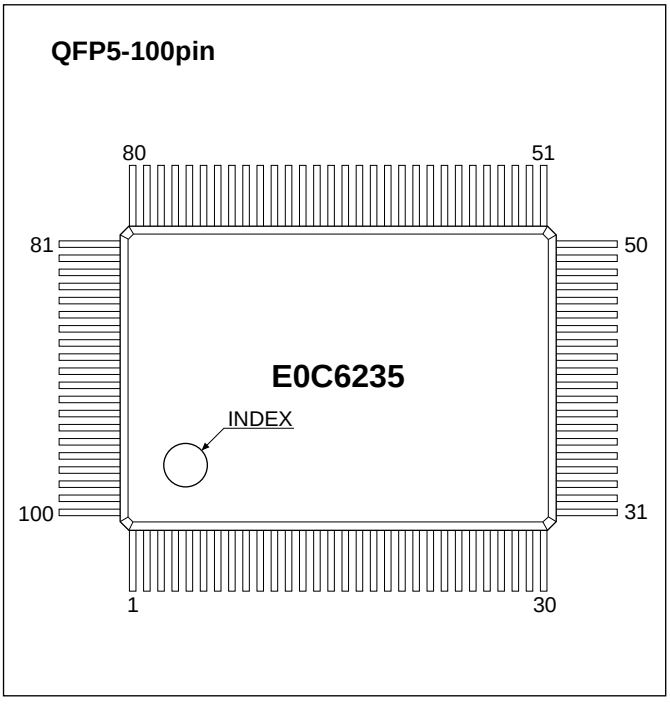
Model	Supply voltage	Clock
E0C62L35	1.5V (0.9V to 1.7V)	32kHz or 38.4kHz (Crystal oscillation)
E0C6235	3.0V (1.8V to 3.5V)	32kHz or 38.4kHz (Crystal oscillation)
E0C62A35	3.0V (2.2V to 3.5V)	32kHz or 38.4kHz (Crystal oscillation) & 500kHz (Ceramic or CR oscillation)

Twin clocks can be used in E0C62A35.

■ BLOCK DIAGRAM



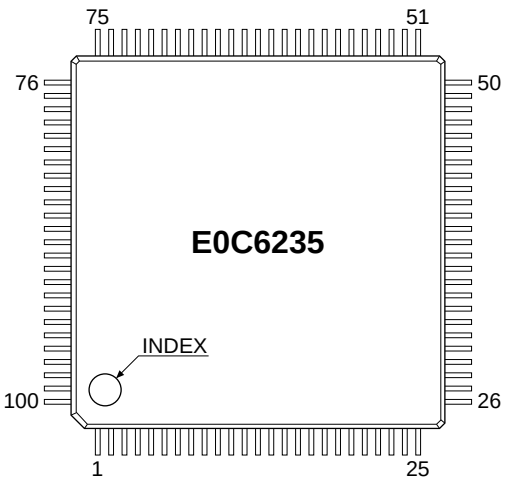
■ PIN CONFIGURATION



No.	Pin name	No.	Pin name	No.	Pin name	No.	Pin name
1	COM1	26	SEG24	51	SEG0	76	P10
2	COM0	27	TEST	52	AMPP	77	R03
3	SEG47	28	SEG23	53	AMPM	78	R02
4	SEG46	29	SEG22	54	K23	79	R01
5	SEG45	30	SEG21	55	K22	80	R00
6	SEG44	31	SEG20	56	K21	81	R12
7	SEG43	32	SEG19	57	K20	82	R11
8	SEG42	33	SEG18	58	K10	83	R10
9	SEG41	34	SEG17	59	K03	84	R13
10	SEG40	35	SEG16	60	K02	85	V_{SS}
11	SEG39	36	SEG15	61	K01	86	RESET
12	SEG38	37	SEG14	62	K00	87	OSC4
13	SEG37	38	SEG13	63	SIN	88	OSC3
14	SEG36	39	SEG12	64	SOUT	89	V_{S1}
15	SEG35	40	SEG11	65	N.C.	90	OSC2
16	SEG34	41	SEG10	66	SCLK	91	OSC1
17	SEG33	42	SEG9	67	P03	92	V_{DD}
18	SEG32	43	SEG8	68	P02	93	V_{L3}
19	SEG31	44	SEG7	69	P01	94	V_{L2}
20	SEG30	45	SEG6	70	P00	95	V_{L1}
21	SEG29	46	SEG5	71	N.C.	96	CA
22	SEG28	47	SEG4	72	N.C.	97	CB
23	SEG27	48	SEG3	73	P13	98	CC
24	SEG26	49	SEG2	74	P12	99	COM3
25	SEG25	50	SEG1	75	P11	100	COM2

N.C. = No Connection

QFP15-100pin



No.	Pin name	No.	Pin name	No.	Pin name	No.	Pin name
1	SEG47	26	SEG23	51	AMPP	76	R02
2	SEG46	27	SEG22	52	AMPM	77	R01
3	SEG45	28	SEG21	53	K23	78	R00
4	SEG44	29	SEG20	54	K22	79	R12
5	SEG43	30	SEG19	55	K21	80	R11
6	SEG42	31	SEG18	56	K20	81	R10
7	SEG41	32	SEG17	57	K10	82	R13
8	SEG40	33	SEG16	58	K03	83	V_{SS}
9	SEG39	34	SEG15	59	K02	84	RESET
10	SEG38	35	SEG14	60	K01	85	OSC4
11	SEG37	36	SEG13	61	K00	86	OSC3
12	SEG36	37	SEG12	62	SIN	87	V_{S1}
13	SEG35	38	N.C.	63	SOUT	88	OSC2
14	SEG34	39	SEG11	64	N.C.	89	OSC1
15	SEG33	40	SEG10	65	SCLK	90	V_{DD}
16	SEG32	41	SEG9	66	N.C.	91	V_{L3}
17	SEG31	42	SEG8	67	P03	92	V_{L2}
18	SEG30	43	SEG7	68	P02	93	V_{L1}
19	SEG29	44	SEG6	69	P01	94	CA
20	SEG28	45	SEG5	70	P00	95	CB
21	SEG27	46	SEG4	71	P13	96	CC
22	SEG26	47	SEG3	72	P12	97	COM3
23	SEG25	48	SEG2	73	P11	98	COM2
24	SEG24	49	SEG1	74	P10	99	COM1
25	TEST	50	SEG0	75	R03	100	COM0

N.C. = No Connection

■ PIN DESCRIPTION

Pin name	Pin No.		In/Out	Function
	QFP5-100	QFP15-100		
V_{DD}	92	90	I	Power source (+) terminal
V_{SS}	85	83	I	Power source (-) terminal
V_{S1}	89	87	O	Oscillation and internal logic system regulated voltage output terminal
V_{L1}	95	93	O	LCD system regulated voltage output terminal (approx. -1.05 V)
V_{L2}	94	92	O	LCD system booster output terminal (V_{L1} x 2)
V_{L3}	93	91	O	LCD system booster output terminal (V_{L1} x 3)
CA–CC	96–98	94–96	–	Booster capacitor connecting terminal
OSC1	91	89	I	Crystal oscillation input terminal
OSC2	90	88	O	Crystal oscillation output terminal
OSC3	88	86	I	Ceramic or CR oscillation input terminal (Switchable by mask option, 62A35 only)
OSC4	87	85	O	Ceramic or CR oscillation output terminal (Switchable by mask option, 62A35 only)
K00–K03, K10 K20–K23	54–62	53–61	I	Input terminal
P00–P03 P10–P13	67–70 73–76	67–74	I/O	I/O terminal
R00–R03	77–80	75–78	O	Output terminal
R10	83	81	O	Output terminal (DC or $\overline{BZ}$ output may be selected by mask option)
R13	84	82	O	Output terminal (DC or $\overline{BZ}$ output may be selected by mask option)
R11	82	80	O	Output terminal (DC or SIOF output may be selected by mask option)
R12	81	79	O	Output terminal (DC or FOUT output may be selected by mask option)
SIN	63	62	I	Serial interface input terminal
SOUT	64	63	O	Serial interface output terminal
SCLK	66	65	I/O	Serial interface clock input/output terminal
AMPP	52	51	I	Analog comparator non-inverted input terminal
AMPM	53	52	I	Analog comparator inverted input terminal
SEG0–47	3–26, 28–51	1–24, 26–50	O	LCD segment output terminal (Convertible to DC output by mask option)
COM0–3	1, 2, 99, 100	97–100	O	LCD common output terminal
RESET	86	84	I	Initial reset input terminal
TEST	27	25	I	Test input terminal

■ ELECTRICAL CHARACTERISTICS

● Absolute Maximum Ratings

E0C6235/62A35

(V_{DD}=0V)

Rating	Symbol	Value	Unit
Supply voltage	V_{SS}	-5.0 to 0.5	V
Input voltage (1)	V_I	V_{SS} - 0.3 to 0.5	V
Input voltage (2)	V_{IOSC}	V_{S1} - 0.3 to 0.5	V
Permissible total output current *1	ΣI_{VSS}	10	mA
Operating temperature	Topr	-20 to 70	°C
Storage temperature	Tstg	-65 to 150	°C
Soldering temperature / Time	Tsol	260°C, 10sec (lead section)	–
Permissible dissipation *2	P_D	250	mW

∗1: The permissible total output current is the sum total of the current (average current) that simultaneously flows from the output pins (or is draw in).
∗2: In case of plastic package (QFP5-100pin, QFP15-100pin).

E0C62L35

(V_{DD}=0V)

Rating	Symbol	Value	Unit
Supply voltage	V_{SS}	-2.0 to 0.5	V
Input voltage (1)	V_I	V_{SS} - 0.3 to 0.5	V
Input voltage (2)	V_{IOSC}	V_{S1} - 0.3 to 0.5	V
Permissible total output current *1	ΣI_{VSS}	10	mA
Operating temperature	Topr	-20 to 70	°C
Storage temperature	Tstg	-65 to 150	°C
Soldering temperature / Time	Tsol	260°C, 10sec (lead section)	–
Permissible dissipation *2	P_D	250	mW

∗1: The permissible total output current is the sum total of the current (average current) that simultaneously flows from the output pins (or is draw in).
∗2: In case of plastic package (QFP5-100pin, QFP15-100pin).

● Recommended Operating Conditions

E0C6235

(Ta=-20 to 70°C)

Condition	Symbol	Remark	Min.	Typ.	Max.	Unit
Supply voltage	V_{SS}	V_{DD}=0V	-3.5	-3.0	-1.8	V
Oscillation frequency	f_{OSC1}	Either one is selected	–	32.768	–	kHz
			–	38.400	–	kHz

E0C62L35

(Ta=-20 to 70°C)

Condition	Symbol	Remark	Min.	Typ.	Max.	Unit
Supply voltage	V_{SS}	V_{DD}=0V	-1.7	-1.5	-1.1	V
		V_{DD}=0V, With software control *1	-1.7	-1.5	-0.9 *2	V
		V_{DD}=0V, When the analog comparator is used	-1.7	-1.5	-1.2	V
Oscillation frequency	f_{OSC1}	Either one is selected	–	32.768	–	kHz
			–	38.400	–	kHz

∗1: When switching to heavy load protection mode.
∗2: The possibility of LCD panel display differs depending on the characteristics of the LCD panel.

E0C62A35

(Ta=-20 to 70°C)

Condition	Symbol	Remark	Min.	Typ.	Max.	Unit
Supply voltage	V_{SS}	V_{DD}=0V	-3.5	-3.0	-2.2	V
Oscillation frequency (1)	f_{OSC1}	Either one is selected	–	32.768	–	kHz
			–	38.400	–	kHz
Oscillation frequency (2)	f_{OSC3}	duty 50±5%	50	500	600	kHz

● DC Characteristics

E0C6235/62A35

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-3.0V, f_{OSC1}=32.768kHz, Ta=25°C, V_{S1}/V_{L1}–V_{L3} are internal voltage, C1–C6=0.1µF)

Characteristic	Symbol	Condition		Min.	Typ.	Max.	Unit
High level input voltage (1)	V_{IH1}		K00–03, K10, K20–23 P00–03, P10–13, SIN	0.2•V_{SS}		0	V
High level input voltage (2)	V_{IH2}		SCLK, RESET, TEST	0.1•V_{SS}		0	V
Low level input voltage (1)	V_{IL1}		K00–03, K10, K20–23 P00–03, P10–13, SIN	V_{SS}		0.8•V_{SS}	V
Low level input voltage (2)	V_{IL2}		SCLK, RESET, TEST	V_{SS}		0.9•V_{SS}	V
High level input current (1)	I_{IH1}	V_{IH1}=0V No pull down resistor	K00–03, K10, K20–23 P00–03, P10–13, SIN, SCLK AMPP, AMPM, RESET	0		0.5	µA
High level input current (2)	I_{IH2}	V_{IH2}=0V With pull down resistor	K00–03, K10, K20–23 SIN, SCLK	4		16	µA
High level input current (3)	I_{IH3}	V_{IH3}=0V With pull down resistor	P00–03, P10–13 RESET, TEST	25		100	µA
Low level input current	I_{IL}	V_{IL}=V_{SS}	K00–03, K10, K20–23 P00–03, P10–13, SIN, SCLK AMPP, AMPM, RESET, TEST	-0.5		0	µA
High level output current (1)	I_{OH1}	V_{OH1}=0.1•V_{SS}	R10, R11, R13			-1.8	mA
High level output current (2)	I_{OH2}	V_{OH2}=0.1•V_{SS}	R00–03, R12, P00–03, P10–13 SOUT, SCLK			-0.9	mA
Low level output current (1)	I_{OL1}	V_{OL1}=0.9•V_{SS}	R10, R11, R13	6.0			mA
Low level output current (2)	I_{OL2}	V_{OL2}=0.9•V_{SS}	R00–03, R12, P00–03, P10–13 SOUT, SCLK	3.0			mA
Common output current	I_{OH3}	V_{OH3}=-0.05V	COM0–COM3			-3	µA
	I_{OL3}	V_{OL3}=V_{L3}+0.05V		3			µA
Segment output current (during LCD output)	I_{OH4}	V_{OH4}=-0.05V	SEG0–SEG47			-3	µA
	I_{OL4}	V_{OL4}=V_{L3}+0.05V		3			µA
Segment output current (during DC output)	I_{OH5}	V_{OH5}=0.1•V_{SS}	SEG0–SEG47			-200	µA
	I_{OL5}	V_{OL5}=0.9•V_{SS}		200			µA

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(Unless otherwise specified: V_{DD}=0V, V_{SS}=-1.5V, f_{OSC1}=32.768kHz, Ta=25°C, V_{S1}/V_{L1}–V_{L3} are internal voltage, C1–C6=0.1µF)

Characteristic	Symbol	Condition		Min.	Typ.	Max.	Unit
High level input voltage (1)	V_{IH1}		K00–03, K10, K20–23 P00–03, P10–13, SIN	0.2•V_{SS}		0	V
High level input voltage (2)	V_{IH2}		SCLK, RESET, TEST	0.1•V_{SS}		0	V
Low level input voltage (1)	V_{IL1}		K00–03, K10, K20–23 P00–03, P10–13, SIN	V_{SS}		0.8•V_{SS}	V
Low level input voltage (2)	V_{IL2}		SCLK, RESET, TEST	V_{SS}		0.9•V_{SS}	V
High level input current (1)	I_{IH1}	V_{IH1}=0V No pull down resistor	K00–03, K10, K20–23 P00–03, P10–13, SIN, SCLK AMPP, AMPM, RESET	0		0.5	µA
High level input current (2)	I_{IH2}	V_{IH2}=0V With pull down resistor	K00–03, K10, K20–23 SIN, SCLK	2		10	µA
High level input current (3)	I_{IH3}	V_{IH3}=0V With pull down resistor	P00–03, P10–13 RESET, TEST	12		60	µA
Low level input current	I_{IL}	V_{IL}=V_{SS}	K00–03, K10, K20–23 P00–03, P10–13, SIN, SCLK AMPP, AMPM, RESET, TEST	-0.5		0	µA
High level output current (1)	I_{OH1}	V_{OH1}=0.1•V_{SS}	R10, R11, R13			-300	µA
High level output current (2)	I_{OH2}	V_{OH2}=0.1•V_{SS}	R00–03, R12, P00–03, P10–13 SOUT, SCLK			-150	µA
Low level output current (1)	I_{OL1}	V_{OL1}=0.9•V_{SS}	R10, R11, R13	1,400			µA
Low level output current (2)	I_{OL2}	V_{OL2}=0.9•V_{SS}	R00–03, R12, P00–03, P10–13 SOUT, SCLK	700			µA
Common output current	I_{OH3}	V_{OH3}=-0.05V	COM0–COM3			-3	µA
	I_{OL3}	V_{OL3}=V_{L3}+0.05V		3			µA
Segment output current (during LCD output)	I_{OH4}	V_{OH4}=-0.05V	SEG0–SEG47			-3	µA
	I_{OL4}	V_{OL4}=V_{L3}+0.05V		3			µA
Segment output current (during DC output)	I_{OH5}	V_{OH5}=0.1•V_{SS}	SEG0–SEG47			-100	µA
	I_{OL5}	V_{OL5}=0.9•V_{SS}		100			µA

● Analog Circuit Characteristics and Current Consumption

E0C6235 (Normal Mode)

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-3.0V, f_{OSC1}=32.768kHz, Ta=25°C, C_G=25pF, V_{S1}/V_{L1}–V_{L3} are internal voltage, C1–C6=0.1µF)

Characteristic	Symbol	Condition		Min.	Typ.	Max.	Unit
Internal voltage	V_{L1}	Connect 1MΩ load resistor between V_{DD} and V_{L1} (without panel load)		-1.15	-1.05	-0.95	V
	V_{L2}	Connect 1MΩ load resistor between V_{DD} and V_{L2} (without panel load)		2•V_{L1} -0.1		2•V_{L1} ×0.9	V
	V_{L3}	Connect 1MΩ load resistor between V_{DD} and V_{L3} (without panel load)		3•V_{L1} -0.1		3•V_{L1} ×0.9	V
BLD voltage *1	V_{B0}	BLC="0"		-2.35	-2.20	-2.05	V
	V_{B1}	BLC="1"		-2.40	-2.25	-2.10	V
	V_{B2}	BLC="2"		-2.45	-2.30	-2.15	V
	V_{B3}	BLC="3"		-2.50	-2.35	-2.20	V
	V_{B4}	BLC="4"		-2.55	-2.40	-2.25	V
	V_{B5}	BLC="5"		-2.60	-2.45	-2.30	V
	V_{B6}	BLC="6"		-2.65	-2.50	-2.35	V
	V_{B7}	BLC="7"		-2.70	-2.55	-2.40	V
BLD circuit response time	t_B					100	µS
Sub-BLD voltage	V_{BS}			-2.55	-2.40	-2.25	V
Sub-BLD circuit response time	t_{BS}					100	µS
Analog comparator input voltage	V_{IP}	Noninverted input (AMPP)		V_{SS}+0.3		V_{DD}-0.9	V
	V_{IM}	Inverted input (AMPM)					
Analog comparator offset voltage	V_{OF}					10	mV
Analog comparator response time	t_{AMP}	V_{IP}=-1.5V, V_{IM}=V_{IP}±15mV				3	mS
Current consumption	I_{OP}	During HALT	Without panel load		1.8	4.0	µA
		During operation *2			6.0	10.0	µA

*1: The relationships among V_{B0}–V_{B7} are V_{B0}>V_{B1}>V_{B2}>...V_{B5}>V_{B6}>V_{B7}.

*2: The BLD circuit, sub-BLD circuit and analog comparator are in the OFF status.

E0C6235 (Heavy Load Protection Mode)

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-3.0V, f_{OSC1}=32.768kHz, Ta=25°C, C_G=25pF, V_{S1}/V_{L1}–V_{L3} are internal voltage, C1–C6=0.1µF)

Characteristic	Symbol	Condition		Min.	Typ.	Max.	Unit
Internal voltage	V_{L1}	Connect 1MΩ load resistor between V_{DD} and V_{L1} (without panel load)		-1.15	-1.05	-0.95	V
	V_{L2}	Connect 1MΩ load resistor between V_{DD} and V_{L2} (without panel load)		2•V_{L1} -0.1		2•V_{L1} ×0.9	V
	V_{L3}	Connect 1MΩ load resistor between V_{DD} and V_{L3} (without panel load)		3•V_{L1} -0.1		3•V_{L1} ×0.9	V
BLD voltage *1	V_{B0}	BLC="0"		-2.35	-2.20	-2.05	V
	V_{B1}	BLC="1"		-2.40	-2.25	-2.10	V
	V_{B2}	BLC="2"		-2.45	-2.30	-2.15	V
	V_{B3}	BLC="3"		-2.50	-2.35	-2.20	V
	V_{B4}	BLC="4"		-2.55	-2.40	-2.25	V
	V_{B5}	BLC="5"		-2.60	-2.45	-2.30	V
	V_{B6}	BLC="6"		-2.65	-2.50	-2.35	V
	V_{B7}	BLC="7"		-2.70	-2.55	-2.40	V
BLD circuit response time	t_B					100	µS
Sub-BLD voltage	V_{BS}			-2.55	-2.40	-2.25	V
Sub-BLD circuit response time	t_{BS}					100	µS
Analog comparator input voltage	V_{IP}	Noninverted input (AMPP)		V_{SS}+0.3		V_{DD}-0.9	V
	V_{IM}	Inverted input (AMPM)					
Analog comparator offset voltage	V_{OF}					10	mV
Analog comparator response time	t_{AMP}	V_{IP}=-1.5V, V_{IM}=V_{IP}±15mV				3	mS
Current consumption	I_{OP}	During HALT	Without panel load		35	90	µA
		During operation *2			40	100	µA

*1: The relationships among V_{B0}–V_{B7} are V_{B0}>V_{B1}>V_{B2}>...V_{B5}>V_{B6}>V_{B7}.

*2: The BLD circuit and sub-BLD circuit are in the ON status (HLMOD="1", BLS="0"). The analog comparator is in the OFF status.

E0C62L35 (Normal Mode)

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-1.5V, f_{OSC1}=32.768kHz, Ta=25°C, C_G=25pF, V_{S1}/V_{L1}–V_{L3} are internal voltage, C1–C6=0.1µF)

Characteristic	Symbol	Condition		Min.	Typ.	Max.	Unit
Internal voltage	V_{L1}	Connect 1MΩ load resistor between V_{DD} and V_{L1} (without panel load)		-1.15	-1.05	-0.95	V
	V_{L2}	Connect 1MΩ load resistor between V_{DD} and V_{L2} (without panel load)		2•V_{L1} -0.1		2•V_{L1} ×0.9	V
	V_{L3}	Connect 1MΩ load resistor between V_{DD} and V_{L3} (without panel load)		3•V_{L1} -0.1		3•V_{L1} ×0.9	V
BLD voltage *1	V_{B0}	BLC="0"		-1.15	-1.05	-0.95	V
	V_{B1}	BLC="1"		-1.20	-1.10	-1.00	V
	V_{B2}	BLC="2"		-1.25	-1.15	-1.05	V
	V_{B3}	BLC="3"		-1.30	-1.20	-1.10	V
	V_{B4}	BLC="4"		-1.35	-1.25	-1.15	V
	V_{B5}	BLC="5"		-1.40	-1.30	-1.20	V
	V_{B6}	BLC="6"		-1.45	-1.35	-1.25	V
	V_{B7}	BLC="7"		-1.50	-1.40	-1.30	V
BLD circuit response time	t_B					100	µS
Sub-BLD voltage	V_{BS}			-1.30	-1.20	-1.10	V
Sub-BLD circuit response time	t_{BS}					100	µS
Analog comparator input voltage	V_{IP}	Noninverted input (AMPP)		V_{SS}+0.3		V_{DD}-0.9	V
	V_{IM}	Inverted input (AMPM)					
Analog comparator offset voltage	V_{OF}					20	mV
Analog comparator response time	t_{AMP}	V_{IP}=-1.1V, V_{IM}=V_{IP}±30mV				3	mS
Current consumption	I_{OP}	During HALT	Without panel load		1.5	3.0	µA
		During operation *2			5.0	8.0	µA

*1: The relationships among V_{B0}–V_{B7} are V_{B0}>V_{B1}>V_{B2}>...V_{B5}>V_{B6}>V_{B7}.

*2: The BLD circuit, sub-BLD circuit and analog comparator are in the OFF status.

E0C62L35 (Heavy Load Protection Mode)

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-1.5V, f_{OSC1}=32.768kHz, Ta=25°C, C_G=25pF, V_{S1}/V_{L1}–V_{L3} are internal voltage, C1–C6=0.1µF)

Characteristic	Symbol	Condition		Min.	Typ.	Max.	Unit
Internal voltage	V_{L1}	Connect 1MΩ load resistor between V_{DD} and V_{L1} (without panel load)		-1.15	-1.05	-0.95	V
	V_{L2}	Connect 1MΩ load resistor between V_{DD} and V_{L2} (without panel load)		2•V_{L1} -0.1		2•V_{L1} ×0.85	V
	V_{L3}	Connect 1MΩ load resistor between V_{DD} and V_{L3} (without panel load)		3•V_{L1} -0.1		3•V_{L1} ×0.85	V
BLD voltage *1	V_{B0}	BLC="0"		-1.15	-1.05	-0.95	V
	V_{B1}	BLC="1"		-1.20	-1.10	-1.00	V
	V_{B2}	BLC="2"		-1.25	-1.15	-1.05	V
	V_{B3}	BLC="3"		-1.30	-1.20	-1.10	V
	V_{B4}	BLC="4"		-1.35	-1.25	-1.15	V
	V_{B5}	BLC="5"		-1.40	-1.30	-1.20	V
	V_{B6}	BLC="6"		-1.45	-1.35	-1.25	V
	V_{B7}	BLC="7"		-1.50	-1.40	-1.30	V
BLD circuit response time	t_B					100	µS
Sub-BLD voltage	V_{BS}			-1.30	-1.20	-1.10	V
Sub-BLD circuit response time	t_{BS}					100	µS
Analog comparator input voltage	V_{IP}	Noninverted input (AMPP)		V_{SS}+0.3		V_{DD}-0.9	V
	V_{IM}	Inverted input (AMPM)					
Analog comparator offset voltage	V_{OF}					20	mV
Analog comparator response time	t_{AMP}	V_{IP}=-1.1V, V_{IM}=V_{IP}±30mV				3	mS
Current consumption	I_{OP}	During HALT	Without panel load		3.0	7.0	µA
		During operation *2			10.0	18.0	µA

*1: The relationships among V_{B0}–V_{B7} are V_{B0}>V_{B1}>V_{B2}>...V_{B5}>V_{B6}>V_{B7}.

*2: The BLD circuit and sub-BLD circuit are in the ON status (HLMOD="1", BLS="0"). The analog comparator is in the OFF status.

E0C62A35 (Normal Mode)

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-3.0V, f_{OSC1}=32.768kHz, Ta=25°C, C_G=25pF, V_{S1}/V_{L1}–V_{L3} are internal voltage, C1–C6=0.1µF)

Characteristic	Symbol	Condition		Min.	Typ.	Max.	Unit
Internal voltage	V_{L1}	Connect 1MΩ load resistor between V_{DD} and V_{L1} (without panel load)		-1.15	-1.05	-0.95	V
	V_{L2}	Connect 1MΩ load resistor between V_{DD} and V_{L2} (without panel load)		2•V_{L1} -0.1		2•V_{L1} ×0.9	V
	V_{L3}	Connect 1MΩ load resistor between V_{DD} and V_{L3} (without panel load)		3•V_{L1} -0.1		3•V_{L1} ×0.9	V
BLD voltage *1	V_{B0}	BLC="0"		-2.35	-2.20	-2.05	V
	V_{B1}	BLC="1"		-2.40	-2.25	-2.10	V
	V_{B2}	BLC="2"		-2.45	-2.30	-2.15	V
	V_{B3}	BLC="3"		-2.50	-2.35	-2.20	V
	V_{B4}	BLC="4"		-2.55	-2.40	-2.25	V
	V_{B5}	BLC="5"		-2.60	-2.45	-2.30	V
	V_{B6}	BLC="6"		-2.65	-2.50	-2.35	V
	V_{B7}	BLC="7"		-2.70	-2.55	-2.40	V
BLD circuit response time	t_B					100	µS
Sub-BLD voltage	V_{BS}			-2.55	-2.40	-2.25	V
Sub-BLD circuit response time	t_{BS}					100	µS
Analog comparator input voltage	V_{IP}	Noninverted input (AMPP)		V_{SS}+0.3		V_{DD}-0.9	V
	V_{IM}	Inverted input (AMPM)					
Analog comparator offset voltage	V_{OF}					10	mV
Analog comparator response time	t_{AMP}	V_{IP}=-1.5V, V_{IM}=V_{IP}±15mV				3	mS
Current consumption	I_{OP}	During HALT	Without panel load		2.0	5.0	µA
		During operation at 32kHz *2			8.0	15	µA
		During operation at 500kHz *2			130	300	µA

*1: The relationships among V_{B0}–V_{B7} are V_{B0}>V_{B1}>V_{B2}>...V_{B5}>V_{B6}>V_{B7}.
*2: The BLD circuit, sub-BLD circuit and analog comparator are in the OFF status.

E0C62A35 (Heavy Load Protection Mode)

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-3.0V, f_{OSC1}=32.768kHz, Ta=25°C, C_G=25pF, V_{S1}/V_{L1}–V_{L3} are internal voltage, C1–C6=0.1µF)

Characteristic	Symbol	Condition		Min.	Typ.	Max.	Unit
Internal voltage	V_{L1}	Connect 1MΩ load resistor between V_{DD} and V_{L1} (without panel load)		-1.15	-1.05	-0.95	V
	V_{L2}	Connect 1MΩ load resistor between V_{DD} and V_{L2} (without panel load)		2•V_{L1} -0.1		2•V_{L1} ×0.9	V
	V_{L3}	Connect 1MΩ load resistor between V_{DD} and V_{L3} (without panel load)		3•V_{L1} -0.1		3•V_{L1} ×0.9	V
BLD voltage *1	V_{B0}	BLC="0"		-2.35	-2.20	-2.05	V
	V_{B1}	BLC="1"		-2.40	-2.25	-2.10	V
	V_{B2}	BLC="2"		-2.45	-2.30	-2.15	V
	V_{B3}	BLC="3"		-2.50	-2.35	-2.20	V
	V_{B4}	BLC="4"		-2.55	-2.40	-2.25	V
	V_{B5}	BLC="5"		-2.60	-2.45	-2.30	V
	V_{B6}	BLC="6"		-2.65	-2.50	-2.35	V
	V_{B7}	BLC="7"		-2.70	-2.55	-2.40	V
BLD circuit response time	t_B					100	µS
Sub-BLD voltage	V_{BS}			-2.55	-2.40	-2.25	V
Sub-BLD circuit response time	t_{BS}					100	µS
Analog comparator input voltage	V_{IP}	Noninverted input (AMPP)		V_{SS}+0.3		V_{DD}-0.9	V
	V_{IM}	Inverted input (AMPM)					
Analog comparator offset voltage	V_{OF}					10	mV
Analog comparator response time	t_{AMP}	V_{IP}=-1.5V, V_{IM}=V_{IP}±15mV				3	mS
Current consumption	I_{OP}	During HALT	Without panel load		22	40	µA
		During operation at 32kHz *2			28	50	µA
		During operation at 500kHz *2			150	350	µA

*1: The relationships among V_{B0}–V_{B7} are V_{B0}>V_{B1}>V_{B2}>...V_{B5}>V_{B6}>V_{B7}.
*2: The BLD circuit and sub-BLD circuit are in the ON status (HLMOD="1", BLS="0"). The analog comparator is in the OFF status.

● Oscillation Characteristics

The oscillation characteristics change depending on the conditions (components used, board pattern, etc.). Use the following characteristics as reference values.

E0C6235 (Crystal oscillation circuit)

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-3.0V, Crystal: C-002R (C_I=35kΩ), C_G=25pF, C_D=built-in, Ta=25°C)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start voltage	Vsta	tsta≤5sec (Vss)	-1.8			V
Oscillation stop voltage	Vstp	tstp≤10sec (Vss)	-1.8			V
Built-in capacitance (drain)	C_D	Including the parasitic capacity inside the IC		20		pF
Frequency/voltage deviation	∂f/∂V	V_{SS}=-1.8 to -3.5V			5	ppm
Frequency/IC deviation	∂f/∂IC		-10		10	ppm
Frequency adjustment range	∂f/∂C_G	C_G=5 to 25pF	35	45		ppm
Harmonic oscillation start voltage	V_{hho}	(Vss)			-3.5	V
Permitted leak resistance	R_{leak}	Between OSC1 and V_{DD}, V_{SS}	200			MΩ

E0C62L35 (Crystal oscillation circuit)

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-1.5V, Crystal: C-002R (C_I=35kΩ), C_G=25pF, C_D=built-in, Ta=25°C)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start voltage	Vsta	tsta≤5sec (Vss)	-1.1			V
Oscillation stop voltage	Vstp	tstp≤10sec (Vss)	-1.1(-0.9)*1			V
Built-in capacitance (drain)	C_D	Including the parasitic capacity inside the IC		20		pF
Frequency/voltage deviation	∂f/∂V	V_{SS}=-1.1 to -1.7V (-0.9) *1			5	ppm
Frequency/IC deviation	∂f/∂IC		-10		10	ppm
Frequency adjustment range	∂f/∂C_G	C_G=5 to 25pF	35	45		ppm
Harmonic oscillation start voltage	V_{hho}	(Vss)			-1.7	V
Permitted leak resistance	R_{leak}	Between OSC1 and V_{DD}, V_{SS}	200			MΩ

*1: Items enclosed in parentheses ( ) are those used when operating at heavy load protection mode.

E0C62A35 (Crystal oscillation circuit)

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-3.0V, Crystal: C-002R (C_I=35kΩ), C_G=25pF, C_D=built-in, Ta=25°C)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start voltage	Vsta	tsta≤5sec (Vss)	-2.2			V
Oscillation stop voltage	Vstp	tstp≤10sec (Vss)	-2.2			V
Built-in capacitance (drain)	C_D	Including the parasitic capacity inside the IC		20		pF
Frequency/voltage deviation	∂f/∂V	V_{SS}=-2.2 to -3.5V			5	ppm
Frequency/IC deviation	∂f/∂IC		-10		10	ppm
Frequency adjustment range	∂f/∂C_G	C_G=5 to 25pF	35	45		ppm
Harmonic oscillation start voltage	V_{hho}	(Vss)			-3.5	V
Permitted leak resistance	R_{leak}	Between OSC1 and V_{DD}, V_{SS}	200			MΩ

E0C62A35 (CR oscillation circuit)

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-3.0V, R_{CR}=82kΩ, Ta=25°C)

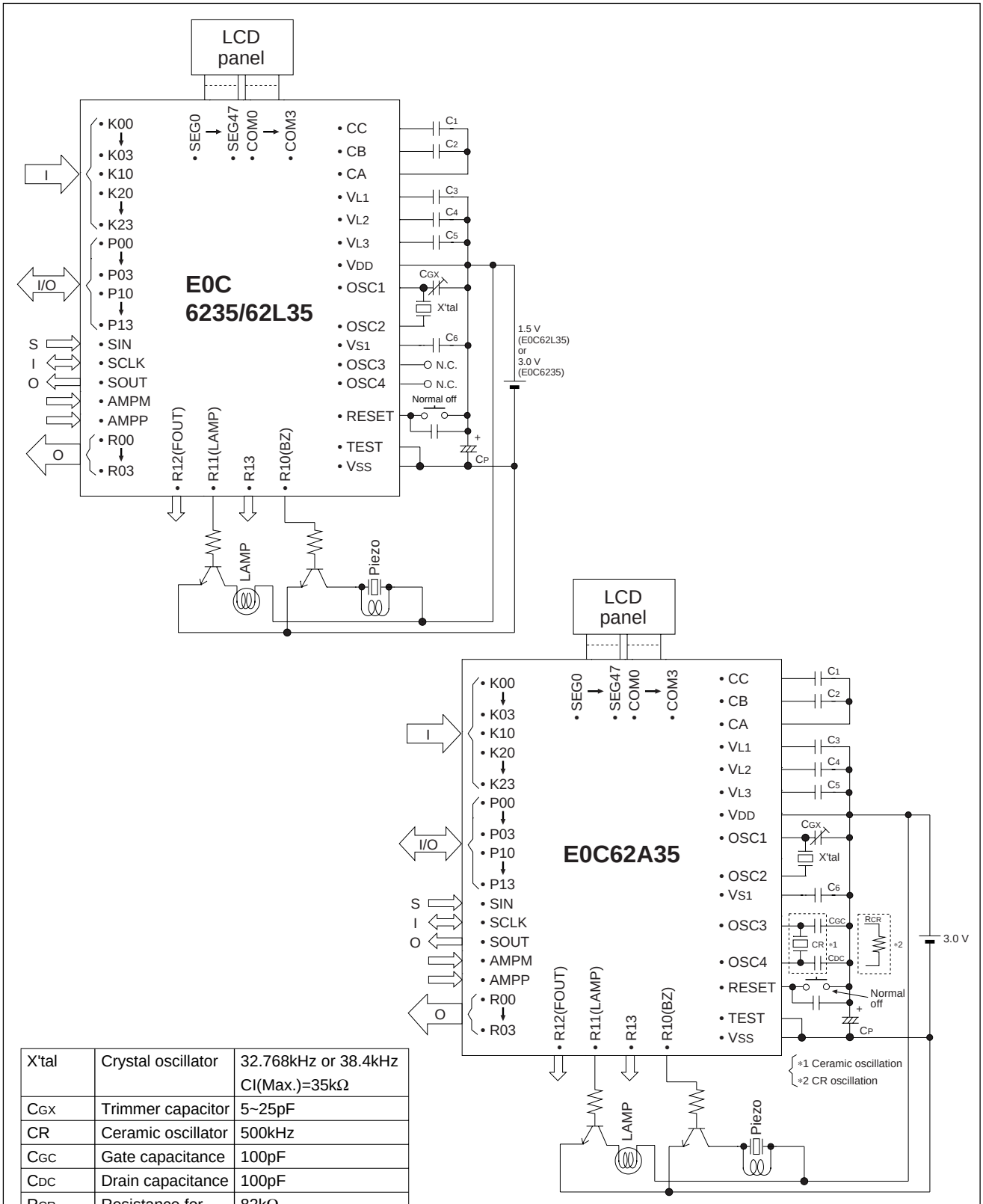
Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation frequency dispersion	f_{OSC3}		-30	480kHz	30	%
Oscillation start voltage	Vsta	(Vss)	-2.2			V
Oscillation start time	tsta	V_{SS}=-2.2 to -3.5V			3	mS
Oscillation stop voltage	Vstp	(Vss)	-2.2			V

E0C62A35 (Ceramic oscillation circuit)

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-3.0V, ceramic oscillation: 500kHz, C_{GC}=C_{DC}=100pF, Ta=25°C)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start voltage	Vsta	(Vss)	-2.2			V
Oscillation start time	tsta	V_{SS}=-2.2 to -3.5V			5	mS
Oscillation stop voltage	Vstp	(Vss)	-2.2			V

■ BASIC EXTERNAL CONNECTION DIAGRAM

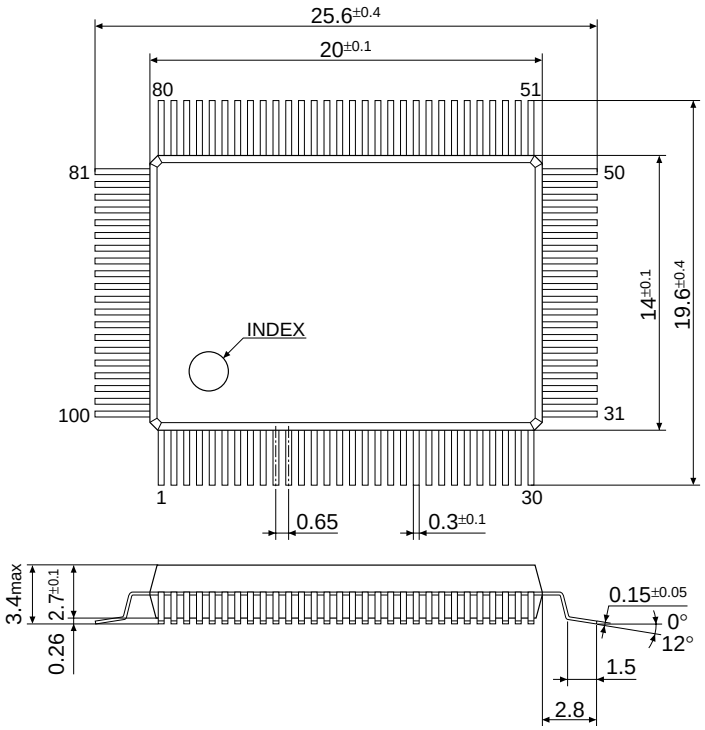


X'tal	Crystal oscillator	32.768kHz or 38.4kHz CI(Max.)=35kΩ
C_{GX}	Trimmer capacitor	5~25pF
CR	Ceramic oscillator	500kHz
C_{GC}	Gate capacitance	100pF
C_{DC}	Drain capacitance	100pF
R_{CR}	Resistance for CR oscillation	82kΩ
C1~C6		0.1µF
CP		3.3µF

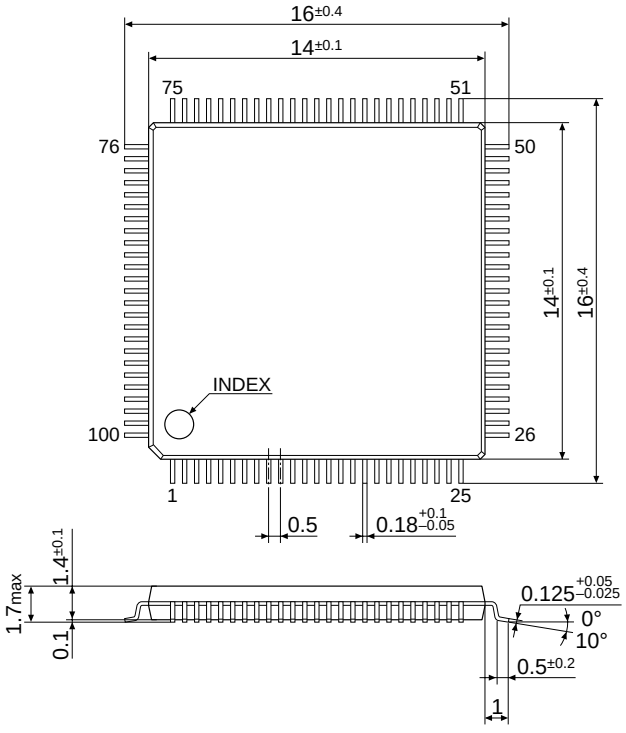
Note: The above table is simply an example, and is not guaranteed to work.

■ PACKAGE DIMENSIONS

Plastic QFP5-100pin



Plastic QFP15-100pin



Unit: mm

SEIKO EPSON CORPORATION
ELECTRONIC DEVICES MARKETING DIVISION
IC Marketing & Engineering Group

ED International Marketing Department I (Europe & U.S.A.)
421-8, Hino, Hino-shi, Tokyo 191-8501, JAPAN
Phone : 042-587-5812 FAX : 042-587-5564

ED International Marketing Department II (Asia)
421-8, Hino, Hino-shi, Tokyo 191-8501, JAPAN
Phone : 042-587-5814 FAX : 042-587-5110

ENERGY SAVING EPSON