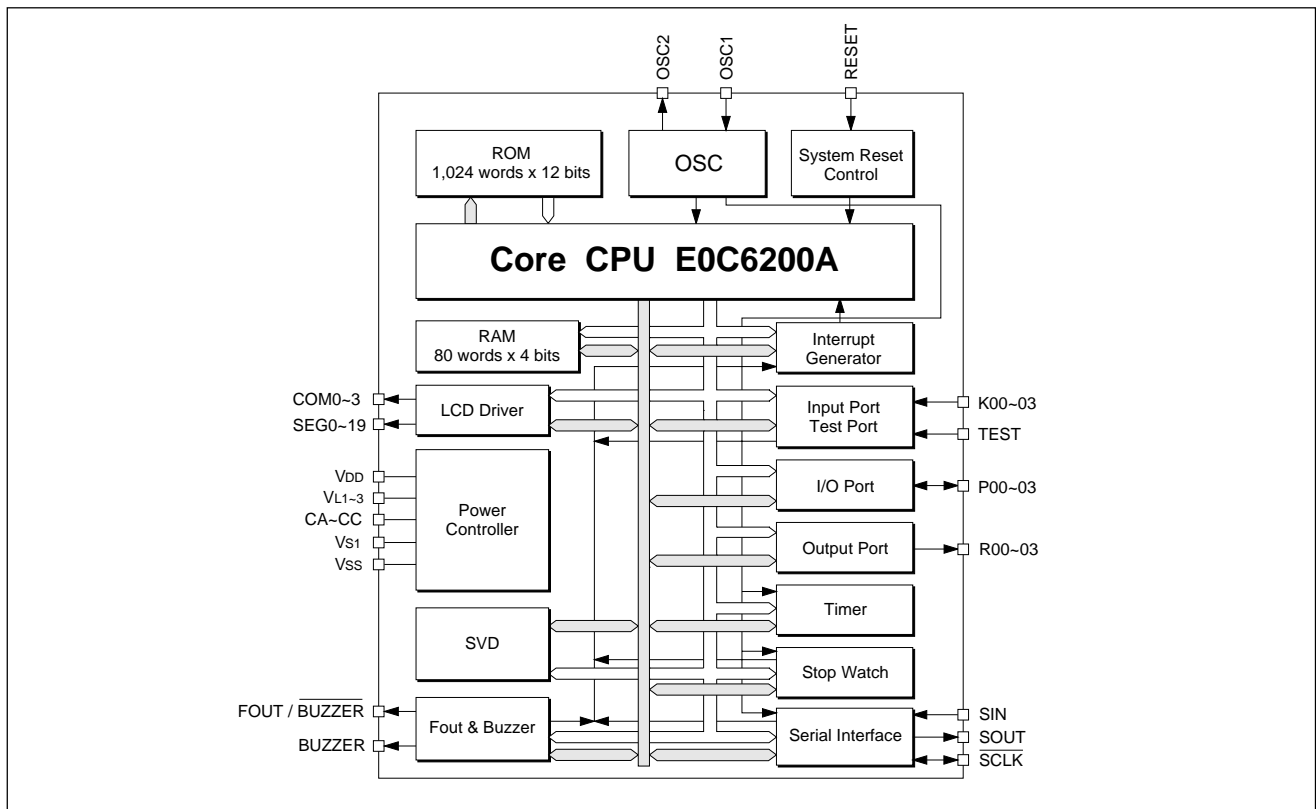
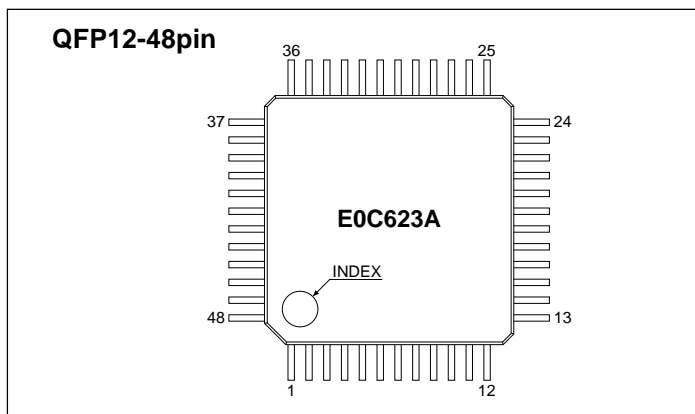


E0C623A

■ BLOCK DIAGRAM

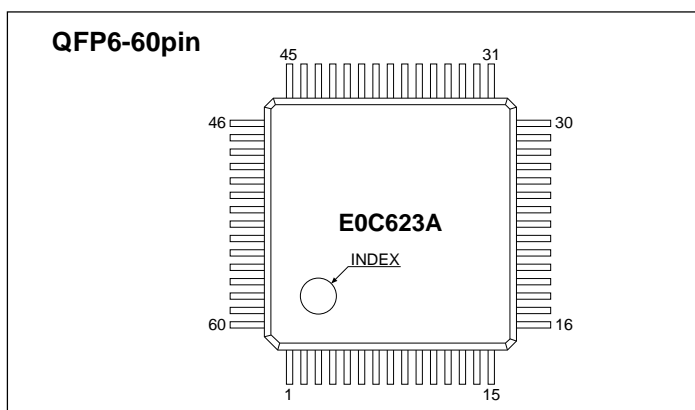


■ PIN CONFIGURATION



| No. | Pin name | No. | Pin name | No. | Pin name | No. | Pin name |
|-----|----------|-----|----------|-----|----------|-----|----------|
| 1 | COM2 | 13 | SEG12 | 25 | P00 | 37 | VDD |
| 2 | COM3 | 14 | SEG13 | 26 | N.C. | 38 | OSC1 |
| 3 | SEG0 | 15 | SEG14 | 27 | RESET | 39 | OSC2 |
| 4 | SEG1 | 16 | SEG15 | 28 | K00 | 40 | VS1 |
| 5 | SEG2 | 17 | SEG16 | 29 | K01 | 41 | CA |
| 6 | SEG3 | 18 | SEG17 | 30 | K02 | 42 | CB |
| 7 | SEG4 | 19 | SEG18 | 31 | K03 | 43 | CC |
| 8 | SEG6 | 20 | SEG19 | 32 | R00 | 44 | VL1 |
| 9 | SEG8 | 21 | TEST | 33 | R01 | 45 | VL2 |
| 10 | SEG9 | 22 | P03 | 34 | R02 | 46 | VL3 |
| 11 | SEG10 | 23 | P02 | 35 | R03 | 47 | COM0 |
| 12 | SEG11 | 24 | P01 | 36 | VSS | 48 | COM1 |

N.C. = No Connection



| No. | Pin name | No. | Pin name | No. | Pin name | No. | Pin name |
|-----|----------|-----|----------|-----|----------|-----|----------|
| 1 | P00 | 16 | OSC1 | 31 | COM3 | 46 | SEG13 |
| 2 | N.C. | 17 | OSC2 | 32 | N.C. | 47 | SEG14 |
| 3 | RESET | 18 | VS1 | 33 | SEG0 | 48 | SEG15 |
| 4 | K00 | 19 | N.C. | 34 | SEG1 | 49 | SEG16 |
| 5 | K01 | 20 | N.C. | 35 | SEG2 | 50 | SEG17 |
| 6 | K02 | 21 | CA | 36 | SEG3 | 51 | SEG18 |
| 7 | K03 | 22 | CB | 37 | SEG4 | 52 | SEG19 |
| 8 | R00 | 23 | CC | 38 | SEG5 | 53 | TEST |
| 9 | R01 | 24 | N.C. | 39 | SEG6 | 54 | N.C. |
| 10 | R02 | 25 | VL1 | 40 | SEG7 | 55 | N.C. |
| 11 | R03 | 26 | VL2 | 41 | SEG8 | 56 | N.C. |
| 12 | N.C. | 27 | VL3 | 42 | SEG9 | 57 | N.C. |
| 13 | N.C. | 28 | COM0 | 43 | SEG10 | 58 | P03 |
| 14 | VSS | 29 | COM1 | 44 | SEG11 | 59 | P02 |
| 15 | VDD | 30 | COM2 | 45 | SEG12 | 60 | P01 |

N.C. = No Connection

PIN DESCRIPTION

| Pin name | Pin No. | | In/Out | Function |
|----------|--------------|------------|--------|--|
| | QFP12-48pin | QFP6-60pin | | |
| VDD | 37 | 15 | I | Power source (+) terminal |
| VSS | 36 | 14 | I | Power source (-) terminal |
| Vs1 | 40 | 18 | O | Oscillation and internal logic system regulated voltage output terminal |
| VL1 | 44 | 25 | O | LCD system regulated voltage output terminal (approx. -1.05 V) |
| VL2 | 45 | 26 | O | LCD system booster output terminal (VL1 x 2) |
| VL3 | 46 | 27 | O | LCD system booster output terminal (VL1 x 3) |
| CA-CC | 41-43 | 21-23 | - | Booster capacitor connecting terminal |
| OSC1 | 38 | 16 | I | Crystal or CR oscillation input terminal |
| OSC2 | 39 | 17 | O | Crystal or CR oscillation output terminal |
| K00-K03 | 28-31 | 4-7 | I | Input terminal |
| P00-P03 | 25-22 | 1, 60-58 | I/O | I/O terminal |
| R00-R03 | 32-35 | 8-11 | O | Output terminal |
| SEG0-4 | 3-7 | 33-37 | O | LCD segment output terminal (Convertible to DC output by mask option) |
| SEG5 | - | 38 | | |
| SEG6 | 8 | 39 | | |
| SEG7 | - | 40 | | |
| SEG8-19 | 9-20 | 41-52 | | |
| COM0-3 | 47, 48, 1, 2 | 28-31 | O | LCD common output terminal |
| RESET | 27 | 3 | I | Initial reset input terminal |
| TEST | 21 | 53 | I | Test input terminal |

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

(VDD=0V)

| Rating | Symbol | Value | Unit |
|------------------------------|--------|-----------------------------|------|
| Supply voltage | Vss | -5.0 to 0.5 | V |
| Input voltage (1) | Vi | Vss - 0.3 to 0.5 | V |
| Input voltage (2) | Viosc | Vss - 0.3 to 0.5 | V |
| Operating temperature | Topr | -20 to 70 | °C |
| Storage temperature | Tstg | -65 to 150 | °C |
| Soldering temperature / Time | Tsol | 260°C, 10sec (lead section) | - |
| Permissible dissipation *1 | Pd | 250 | mW |

*1: In case of plastic package (QFP12-48pin).

Recommended Operating Conditions

E0C623A

(Ta=-20 to 70°C)

| Condition | Symbol | Remark | Min. | Typ. | Max. | Unit |
|-------------------------------|--------|-------------------------|------|--------|------|------|
| Supply voltage | Vss | VDD=0V | -3.5 | -3.0 | -1.8 | V |
| Oscillation frequency | fosc1 | Crystal oscillation | | 32.768 | | kHz |
| | fosc2 | CR oscillation, R=420kΩ | | 65 | 80 | kHz |
| Booster capacitor (1) | C1 | | 0.1 | | | μF |
| Booster capacitor (2) | C2 | | 0.1 | | | μF |
| Capacitor between VDD and VL1 | C3 | | 0.1 | | | μF |
| Capacitor between VDD and VL2 | C4 | | 0.1 | | | μF |
| Capacitor between VDD and VL3 | C5 | | 0.1 | | | μF |
| Capacitor between VDD and Vs1 | C6 | | 0.1 | | | μF |

E0C62L3A

(Ta=-20 to 70°C)

| Condition | Symbol | Remark | Min. | Typ. | Max. | Unit |
|-------------------------------|--------|----------------------------------|------|--------|---------|------|
| Supply voltage | Vss | VDD=0V *3 | -2.0 | -1.5 | -1.1 | V |
| | | VDD=0V, With software control *1 | -2.0 | -1.5 | -0.9 *2 | V |
| Oscillation frequency | fosc1 | Crystal oscillation | | 32.768 | | kHz |
| | fosc2 | CR oscillation, R=420kΩ | | 65 | 80 | kHz |
| Booster capacitor (1) | C1 | | 0.1 | | | μF |
| Booster capacitor (2) | C2 | | 0.1 | | | μF |
| Capacitor between VDD and VL1 | C3 | | 0.1 | | | μF |
| Capacitor between VDD and VL2 | C4 | | 0.1 | | | μF |
| Capacitor between VDD and VL3 | C5 | | 0.1 | | | μF |
| Capacitor between VDD and Vs1 | C6 | | 0.1 | | | μF |

*1: When the heavy load protection mode is set by software and the SVD circuit is turned off.

*2: The voltage which can be displayed on the LCD panel will differ according to the characteristics of the LCD panel.

*3: When there is no software control during CR oscillation or crystal oscillation.

E0C623A

● DC Characteristics

E0C623A

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-3.0V, f_{osc}=32.768kHz, T_a=25°C, V_{S1}/V_{L1}-V_{L3} are internal voltage, C₁-C₆=0.1μF)

| Characteristic | Symbol | Condition | Min. | Typ. | Max. | Unit |
|---|------------------|---|---------------------------------|----------------------|----------------------|------|
| High level input voltage (1) | V _{IH1} | | K00-K03, P00-P03 | 0.2•V _{SS} | 0 | V |
| High level input voltage (2) | V _{IH2} | | RESET, TEST | 0.15•V _{SS} | 0 | V |
| Low level input voltage (1) | V _{IL1} | | K00-K03, P00-P03 | V _{SS} | 0.8•V _{SS} | V |
| Low level input voltage (2) | V _{IL2} | | RESET, TEST | V _{SS} | 0.85•V _{SS} | V |
| High level input current (1) | I _{IH1} | V _{IH1} =0V, No pull down resistor | K00-K03, P00-P03 | 0 | 0.5 | μA |
| High level input current (2) | I _{IH2} | V _{IH2} =0V, With pull down resistor | K00-K03 | 5 | 16 | μA |
| High level input current (3) | I _{IH3} | V _{IH3} =0V, With pull down resistor | P00-P03 | 30 | 100 | μA |
| Low level input current | I _{IL} | V _{IL} =V _{SS} | K00-K03, P00-P03 RESET, TEST | -0.5 | 0 | μA |
| High level output current (1) | I _{OH1} | V _{OH1} =0.1•V _{SS} | R02, R03, P00-P03 | | -1.0 | mA |
| High level output current (2) | I _{OH2} | V _{OH2} =0.1•V _{SS} (built-in protection resistance) | R00, R01 | | -1.0 | mA |
| Low level output current (1) | I _{OL1} | V _{OL1} =0.9•V _{SS} | R02, R03, P00-P03 | 3.0 | | mA |
| Low level output current (2) | I _{OL2} | V _{OL2} =0.9•V _{SS} (built-in protection resistance) | R00, R01 | 3.0 | | mA |
| Common output current | I _{OH3} | V _{OH3} =-0.05V | COM0-COM3 | | -3 | μA |
| | I _{OL3} | V _{OL3} =V _{L3} +0.05V | | 3 | | μA |
| Segment output current (during LCD output) | I _{OH4} | V _{OH4} =-0.05V | SEG0-SEG19 | | -3 | μA |
| | I _{OL4} | V _{OL4} =V _{L3} +0.05V | | 3 | | μA |
| Segment output current (during DC output) | I _{OH5} | V _{OH5} =0.1•V _{SS} | SEG0-SEG19 | | -300 | μA |
| | I _{OL5} | V _{OL5} =0.9•V _{SS} | | 300 | | μA |

E0C62L3A

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-1.5V, f_{osc}=32.768kHz, T_a=25°C, V_{S1}/V_{L1}-V_{L3} are internal voltage, C₁-C₆=0.1μF)

| Characteristic | Symbol | Condition | Min. | Typ. | Max. | Unit |
|---|------------------|---|---------------------------------|----------------------|----------------------|------|
| High level input voltage (1) | V _{IH1} | | K00-K03, P00-P03 | 0.2•V _{SS} | 0 | V |
| High level input voltage (2) | V _{IH2} | | RESET, TEST | 0.15•V _{SS} | 0 | V |
| Low level input voltage (1) | V _{IL1} | | K00-K03, P00-P03 | V _{SS} | 0.8•V _{SS} | V |
| Low level input voltage (2) | V _{IL2} | | RESET, TEST | V _{SS} | 0.85•V _{SS} | V |
| High level input current (1) | I _{IH1} | V _{IH1} =0V, No pull down resistor | K00-K03, P00-P03 | 0 | 0.5 | μA |
| High level input current (2) | I _{IH2} | V _{IH2} =0V, With pull down resistor | K00-K03 | 2.0 | 16 | μA |
| High level input current (3) | I _{IH3} | V _{IH3} =0V, With pull down resistor | P00-P03 | 9.0 | 100 | μA |
| Low level input current | I _{IL} | V _{IL} =V _{SS} | K00-K03, P00-P03 RESET, TEST | -0.5 | 0 | μA |
| High level output current (1) | I _{OH1} | V _{OH1} =0.1•V _{SS} | R02, R03, P00-P03 | | -200 | μA |
| High level output current (2) | I _{OH2} | V _{OH2} =0.1•V _{SS} (built-in protection resistance) | R00, R01 | | -200 | μA |
| Low level output current (1) | I _{OL1} | V _{OL1} =0.9•V _{SS} | R02, R03, P00-P03 | 700 | | μA |
| Low level output current (2) | I _{OL2} | V _{OL2} =0.9•V _{SS} (built-in protection resistance) | R00, R01 | 700 | | μA |
| Common output current | I _{OH3} | V _{OH3} =-0.05V | COM0-COM3 | | -3 | μA |
| | I _{OL3} | V _{OL3} =V _{L3} +0.05V | | 3 | | μA |
| Segment output current (during LCD output) | I _{OH4} | V _{OH4} =-0.05V | SEG0-SEG19 | | -3 | μA |
| | I _{OL4} | V _{OL4} =V _{L3} +0.05V | | 3 | | μA |
| Segment output current (during DC output) | I _{OH5} | V _{OH5} =0.1•V _{SS} | SEG0-SEG19 | | -100 | μA |
| | I _{OL5} | V _{OL5} =0.9•V _{SS} | | 130 | | μA |

● Analog Circuit Characteristics and Current Consumption

E0C623A (Normal Mode)

(Unless otherwise specified: $V_{DD}=0V$, $V_{SS}=-3.0V$, $f_{osc}=32.768kHz$, $T_a=25^{\circ}C$, $C_G=25pF$, $V_{S1}/V_{L1}-V_{L3}$ are internal voltage, $C1-C6=0.1\mu F$)

| Characteristic | Symbol | Condition | Min. | Typ. | Max. | Unit |
|---------------------------|-----------|---|--------------------------|-------|----------------------------------|---------|
| Internal voltage | V_{L1} | Connect $1M\Omega$ load resistor between V_{DD} and V_{L1} (without panel load) | -1.15 | -1.05 | -0.95 | V |
| | V_{L2} | Connect $1M\Omega$ load resistor between V_{DD} and V_{L2} (without panel load) | $2 \cdot V_{L1}$ -0.1 | | $2 \cdot V_{L1}$ $\times 0.9$ | V |
| | V_{L3} | Connect $1M\Omega$ load resistor between V_{DD} and V_{L3} (without panel load) | $3 \cdot V_{L1}$ -0.1 | | $3 \cdot V_{L1}$ $\times 0.9$ | V |
| SVD voltage | V_{SVD} | | -2.55 | -2.40 | -2.25 | V |
| SVD circuit response time | t_{SVD} | | | | 100 | μS |
| Current consumption | IOP | During HALT | | 1.0 | 2.5 | μA |
| | | During execution *1 | Without panel load | 2.5 | 5.0 | μA |

*1: The SVD circuit is turned off.

E0C623A (Heavy Load Protection Mode)

(Unless otherwise specified: $V_{DD}=0V$, $V_{SS}=-3.0V$, $f_{osc}=32.768kHz$, $T_a=25^{\circ}C$, $C_G=25pF$, $V_{S1}/V_{L1}-V_{L3}$ are internal voltage, $C1-C6=0.1\mu F$)

| Characteristic | Symbol | Condition | Min. | Typ. | Max. | Unit |
|---------------------------|-----------|---|--------------------------|-------|-----------------------------------|---------|
| Internal voltage | V_{L1} | Connect $1M\Omega$ load resistor between V_{DD} and V_{L1} (without panel load) | -1.15 | -1.05 | -0.95 | V |
| | V_{L2} | Connect $1M\Omega$ load resistor between V_{DD} and V_{L2} (without panel load) | $2 \cdot V_{L1}$ -0.1 | | $2 \cdot V_{L1}$ $\times 0.85$ | V |
| | V_{L3} | Connect $1M\Omega$ load resistor between V_{DD} and V_{L3} (without panel load) | $3 \cdot V_{L1}$ -0.1 | | $3 \cdot V_{L1}$ $\times 0.85$ | V |
| SVD voltage | V_{SVD} | | -2.55 | -2.40 | -2.25 | V |
| SVD circuit response time | t_{SVD} | | | | 100 | μS |
| Current consumption | IOP | During HALT | | 2.0 | 5.5 | μA |
| | | During execution *1 | Without panel load | 5.5 | 10.0 | μA |

*1: The SVD circuit is turned off.

E0C62L3A (Normal Mode)

(Unless otherwise specified: $V_{DD}=0V$, $V_{SS}=-1.5V$, $f_{osc}=32.768kHz$, $T_a=25^{\circ}C$, $C_G=25pF$, $V_{S1}/V_{L1}-V_{L3}$ are internal voltage, $C1-C6=0.1\mu F$)

| Characteristic | Symbol | Condition | Min. | Typ. | Max. | Unit |
|---------------------------|-----------|---|--------------------------|-------|----------------------------------|---------|
| Internal voltage | V_{L1} | Connect $1M\Omega$ load resistor between V_{DD} and V_{L1} (without panel load) | -1.15 | -1.05 | -0.95 | V |
| | V_{L2} | Connect $1M\Omega$ load resistor between V_{DD} and V_{L2} (without panel load) | $2 \cdot V_{L1}$ -0.1 | | $2 \cdot V_{L1}$ $\times 0.9$ | V |
| | V_{L3} | Connect $1M\Omega$ load resistor between V_{DD} and V_{L3} (without panel load) | $3 \cdot V_{L1}$ -0.1 | | $3 \cdot V_{L1}$ $\times 0.9$ | V |
| SVD voltage | V_{SVD} | | -1.30 | -1.20 | -1.10 | V |
| SVD circuit response time | t_{SVD} | | | | 100 | μS |
| Current consumption | IOP | During HALT | | 1.0 | 2.5 | μA |
| | | During execution *1 | Without panel load | 2.5 | 5.0 | μA |

*1: The SVD circuit is turned off.

E0C62L3A (Heavy Load Protection Mode)

(Unless otherwise specified: $V_{DD}=0V$, $V_{SS}=-1.5V$, $f_{osc}=32.768kHz$, $T_a=25^{\circ}C$, $C_G=25pF$, $V_{S1}/V_{L1}-V_{L3}$ are internal voltage, $C1-C6=0.1\mu F$)

| Characteristic | Symbol | Condition | Min. | Typ. | Max. | Unit |
|---------------------------|-----------|---|--------------------------|-------|-----------------------------------|---------|
| Internal voltage | V_{L1} | Connect $1M\Omega$ load resistor between V_{DD} and V_{L1} (without panel load) | -1.15 | -1.05 | -0.95 | V |
| | V_{L2} | Connect $1M\Omega$ load resistor between V_{DD} and V_{L2} (without panel load) | $2 \cdot V_{L1}$ -0.1 | | $2 \cdot V_{L1}$ $\times 0.85$ | V |
| | V_{L3} | Connect $1M\Omega$ load resistor between V_{DD} and V_{L3} (without panel load) | $3 \cdot V_{L1}$ -0.1 | | $3 \cdot V_{L1}$ $\times 0.85$ | V |
| SVD voltage | V_{SVD} | | -1.30 | -1.20 | -1.10 | V |
| SVD circuit response time | t_{SVD} | | | | 100 | μS |
| Current consumption | IOP | During HALT | | 2.0 | 5.5 | μA |
| | | During execution *1 | Without panel load | 5.5 | 10.0 | μA |

*1: The SVD circuit is turned off.

E0C623A

E0C623A (CR, Normal Mode)

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-3.0V, f_{OSC}=65kHz, R_{CR}=420kΩ, T_a=25°C, V_{S1}/V_{L1}-V_{L3} are internal voltage, C1-C6=0.1μF)

| Characteristic | Symbol | Condition | Min. | Typ. | Max. | Unit |
|---------------------------|------------------|---|---------------------------|-------|---------------------------|------|
| Internal voltage | V _{L1} | Connect 1MΩ load resistor between V _{DD} and V _{L1} (without panel load) | -1.15 | -1.05 | -0.95 | V |
| | V _{L2} | Connect 1MΩ load resistor between V _{DD} and V _{L2} (without panel load) | 2•V _{L1} -0.1 | | 2•V _{L1} ×0.9 | V |
| | V _{L3} | Connect 1MΩ load resistor between V _{DD} and V _{L3} (without panel load) | 3•V _{L1} -0.1 | | 3•V _{L1} ×0.9 | V |
| SVD voltage | V _{SVD} | | -2.55 | -2.40 | -2.25 | V |
| SVD circuit response time | t _{SVD} | | | | 100 | μS |
| Current consumption | I _{OP} | During HALT | | 8.0 | 15.0 | μA |
| | | During execution *1 | Without panel load | 15.0 | 20.0 | μA |

*1: The SVD circuit is turned off.

E0C623A (CR, Heavy Load Protection Mode)

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-3.0V, f_{OSC}=65kHz, R_{CR}=420kΩ, T_a=25°C, V_{S1}/V_{L1}-V_{L3} are internal voltage, C1-C6=0.1μF)

| Characteristic | Symbol | Condition | Min. | Typ. | Max. | Unit |
|---------------------------|------------------|---|---------------------------|-------|----------------------------|------|
| Internal voltage | V _{L1} | Connect 1MΩ load resistor between V _{DD} and V _{L1} (without panel load) | -1.15 | -1.05 | -0.95 | V |
| | V _{L2} | Connect 1MΩ load resistor between V _{DD} and V _{L2} (without panel load) | 2•V _{L1} -0.1 | | 2•V _{L1} ×0.85 | V |
| | V _{L3} | Connect 1MΩ load resistor between V _{DD} and V _{L3} (without panel load) | 3•V _{L1} -0.1 | | 3•V _{L1} ×0.85 | V |
| SVD voltage | V _{SVD} | | -2.55 | -2.40 | -2.25 | V |
| SVD circuit response time | t _{SVD} | | | | 100 | μS |
| Current consumption | I _{OP} | During HALT | | 16.0 | 30.0 | μA |
| | | During execution *1 | Without panel load | 30.0 | 40.0 | μA |

*1: The SVD circuit is turned off.

E0C62L3A (CR, Normal Mode)

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-1.5V, f_{OSC}=65kHz, R_{CR}=420kΩ, T_a=25°C, V_{S1}/V_{L1}-V_{L3} are internal voltage, C1-C6=0.1μF)

| Characteristic | Symbol | Condition | Min. | Typ. | Max. | Unit |
|---------------------------|------------------|---|---------------------------|-------|---------------------------|------|
| Internal voltage | V _{L1} | Connect 1MΩ load resistor between V _{DD} and V _{L1} (without panel load) | -1.15 | -1.05 | -0.95 | V |
| | V _{L2} | Connect 1MΩ load resistor between V _{DD} and V _{L2} (without panel load) | 2•V _{L1} -0.1 | | 2•V _{L1} ×0.9 | V |
| | V _{L3} | Connect 1MΩ load resistor between V _{DD} and V _{L3} (without panel load) | 3•V _{L1} -0.1 | | 3•V _{L1} ×0.9 | V |
| SVD voltage | V _{SVD} | | -1.30 | -1.20 | -1.10 | V |
| SVD circuit response time | t _{SVD} | | | | 100 | μS |
| Current consumption | I _{OP} | During HALT | | 8.0 | 15.0 | μA |
| | | During execution *1 | Without panel load | 15.0 | 20.0 | μA |

*1: The SVD circuit is turned off.

E0C62L3A (CR, Heavy Load Protection Mode)

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-1.5V, f_{OSC}=65kHz, R_{CR}=420kΩ, T_a=25°C, V_{S1}/V_{L1}-V_{L3} are internal voltage, C1-C6=0.1μF)

| Characteristic | Symbol | Condition | Min. | Typ. | Max. | Unit |
|---------------------------|------------------|---|---------------------------|-------|----------------------------|------|
| Internal voltage | V _{L1} | Connect 1MΩ load resistor between V _{DD} and V _{L1} (without panel load) | -1.15 | -1.05 | -0.95 | V |
| | V _{L2} | Connect 1MΩ load resistor between V _{DD} and V _{L2} (without panel load) | 2•V _{L1} -0.1 | | 2•V _{L1} ×0.85 | V |
| | V _{L3} | Connect 1MΩ load resistor between V _{DD} and V _{L3} (without panel load) | 3•V _{L1} -0.1 | | 3•V _{L1} ×0.85 | V |
| SVD voltage | V _{SVD} | | -1.30 | -1.20 | -1.10 | V |
| SVD circuit response time | t _{SVD} | | | | 100 | μS |
| Current consumption | I _{OP} | During HALT | | 16.0 | 30.0 | μA |
| | | During execution *1 | Without panel load | 30.0 | 40.0 | μA |

*1: The SVD circuit is turned off.

● Oscillation Characteristics

The oscillation characteristics change depending on the conditions (components used, board pattern, etc.). Use the following characteristics as reference values.

E0C623A (Crystal oscillation circuit)

(Unless otherwise specified: $V_{DD}=0V$, $V_{SS}=-3.0V$, Crystal: C-002R ($C_1=35k\Omega$), $C_G=25pF$, C_D =built-in, $T_a=25^\circ C$)

| Characteristic | Symbol | Condition | Min. | Typ. | Max. | Unit |
|------------------------------------|---------------------------|--|------|------|------|------------|
| Oscillation start voltage | V_{sta} | $t_{sta} \leq 5sec$ (V _{SS}) | -1.8 | | | V |
| Oscillation stop voltage | V_{stp} | $t_{stp} \leq 10sec$ (V _{SS}) | -1.8 | | | V |
| Built-in capacitance (drain) | C_D | Including the parasitic capacity inside the IC | | 20 | | pF |
| Frequency/voltage deviation | $\partial f/\partial V$ | $V_{SS}=-1.8$ to $-3.5V$ | | | 5 | ppm |
| Frequency/IC deviation | $\partial f/\partial IC$ | | -10 | | 10 | ppm |
| Frequency adjustment range | $\partial f/\partial C_G$ | $C_G=5$ to $25pF$ | 40 | | | ppm |
| Harmonic oscillation start voltage | V_{hho} | $C_G=5pF$ (V _{SS}) | | | -3.5 | V |
| Permitted leak resistance | R_{leak} | Between OSC1 and V_{DD} , V_{SS} | 200 | | | M Ω |

E0C62L3A (Crystal oscillation circuit)

(Unless otherwise specified: $V_{DD}=0V$, $V_{SS}=-1.5V$, Crystal: C-002R ($C_1=35k\Omega$), $C_G=25pF$, C_D =built-in, $T_a=25^\circ C$)

| Characteristic | Symbol | Condition | Min. | Typ. | Max. | Unit |
|------------------------------------|---------------------------|--|--------------|------|------|------------|
| Oscillation start voltage | V_{sta} | $t_{sta} \leq 5sec$ (V _{SS}) | -1.1 | | | V |
| Oscillation stop voltage | V_{stp} | $t_{stp} \leq 10sec$ (V _{SS}) | -1.1(-0.9)*1 | | | V |
| Built-in capacitance (drain) | C_D | Including the parasitic capacity inside the IC | | 20 | | pF |
| Frequency/voltage deviation | $\partial f/\partial V$ | $V_{SS}=-1.1$ to $-2.0V$ (-0.9) *1 | | | 5 | ppm |
| Frequency/IC deviation | $\partial f/\partial IC$ | | -10 | | 10 | ppm |
| Frequency adjustment range | $\partial f/\partial C_G$ | $C_G=5$ to $25pF$ | 40 | | | ppm |
| Harmonic oscillation start voltage | V_{hho} | $C_G=5pF$ (V _{SS}) | | | -2.0 | V |
| Permitted leak resistance | R_{leak} | Between OSC1 and V_{DD} , V_{SS} | 200 | | | M Ω |

*1: Items enclosed in parentheses () are those used when operating at heavy load protection mode.

E0C623A (CR oscillation circuit)

(Unless otherwise specified: $V_{DD}=0V$, $V_{SS}=-3.0V$, $R_{CR}=420k\Omega$, $T_a=25^\circ C$)

| Characteristic | Symbol | Condition | Min. | Typ. | Max. | Unit |
|----------------------------------|-----------|--------------------------|------|-------|------|------|
| Oscillation frequency dispersion | f_{osc} | | -20 | 65kHz | 20 | % |
| Oscillation start voltage | V_{sta} | (V _{SS}) | -1.8 | | | V |
| Oscillation start time | t_{sta} | $V_{SS}=-1.8$ to $-3.5V$ | | 3 | | mS |
| Oscillation stop voltage | V_{stp} | (V _{SS}) | -1.8 | | | V |

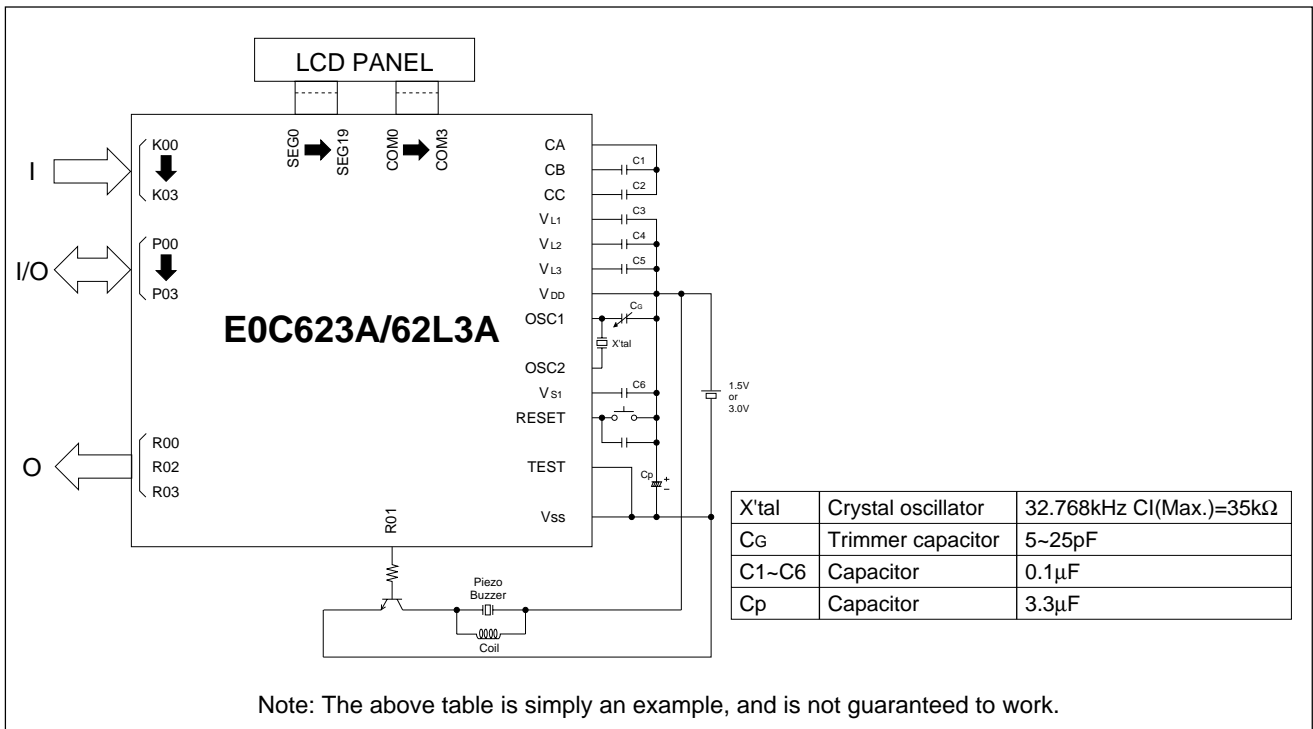
E0C62L3A (CR oscillation circuit)

(Unless otherwise specified: $V_{DD}=0V$, $V_{SS}=-1.5V$, $R_{CR}=420k\Omega$, $T_a=25^\circ C$)

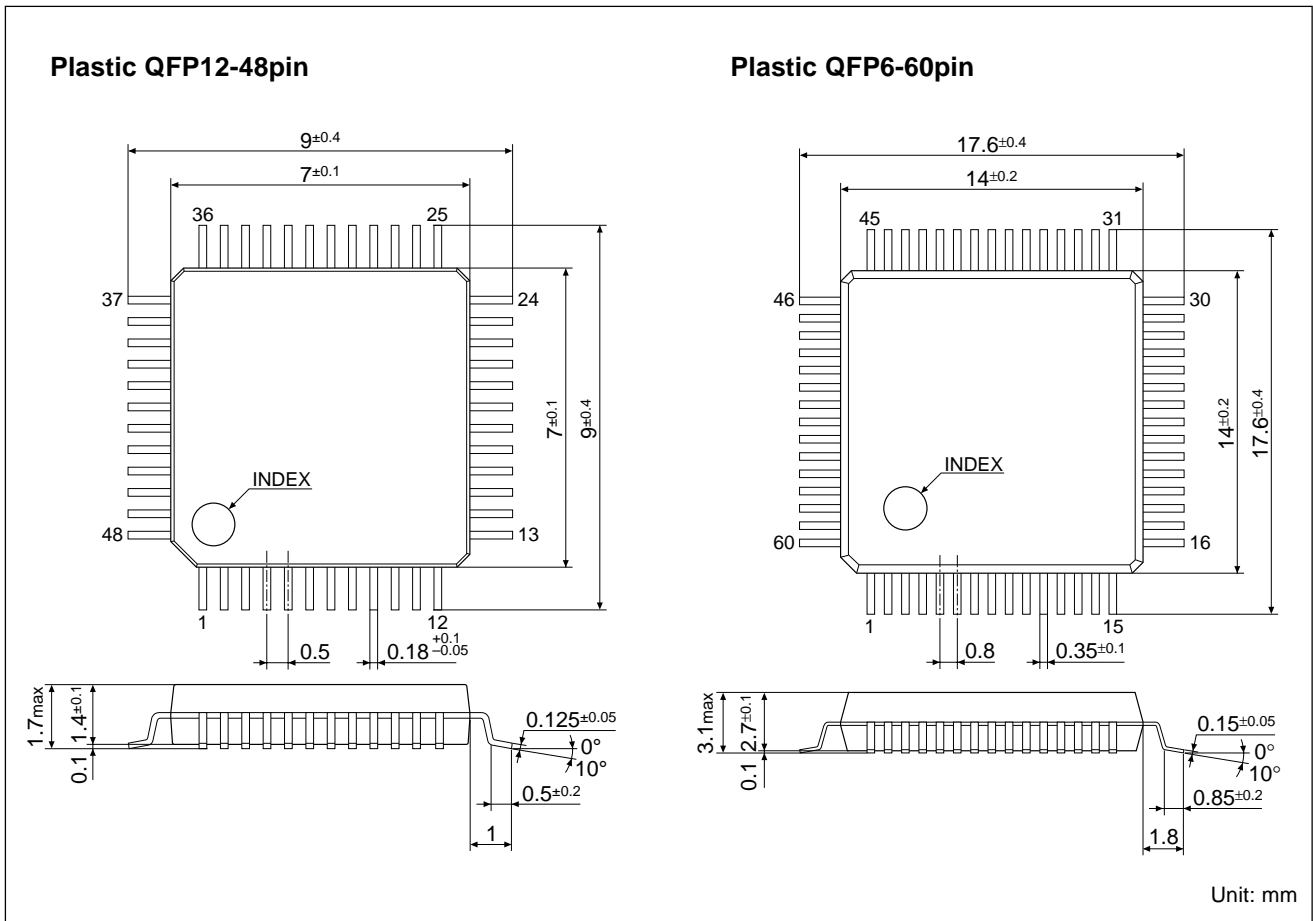
| Characteristic | Symbol | Condition | Min. | Typ. | Max. | Unit |
|----------------------------------|-----------|--------------------------|------|-------|------|------|
| Oscillation frequency dispersion | f_{osc} | | -20 | 65kHz | 20 | % |
| Oscillation start voltage | V_{sta} | (V _{SS}) | -1.1 | | | V |
| Oscillation start time | t_{sta} | $V_{SS}=-1.1$ to $-2.0V$ | | 3 | | mS |
| Oscillation stop voltage | V_{stp} | (V _{SS}) | -1.1 | | | V |

E0C623A

■ BASIC EXTERNAL CONNECTION DIAGRAM



■ PACKAGE DIMENSIONS



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