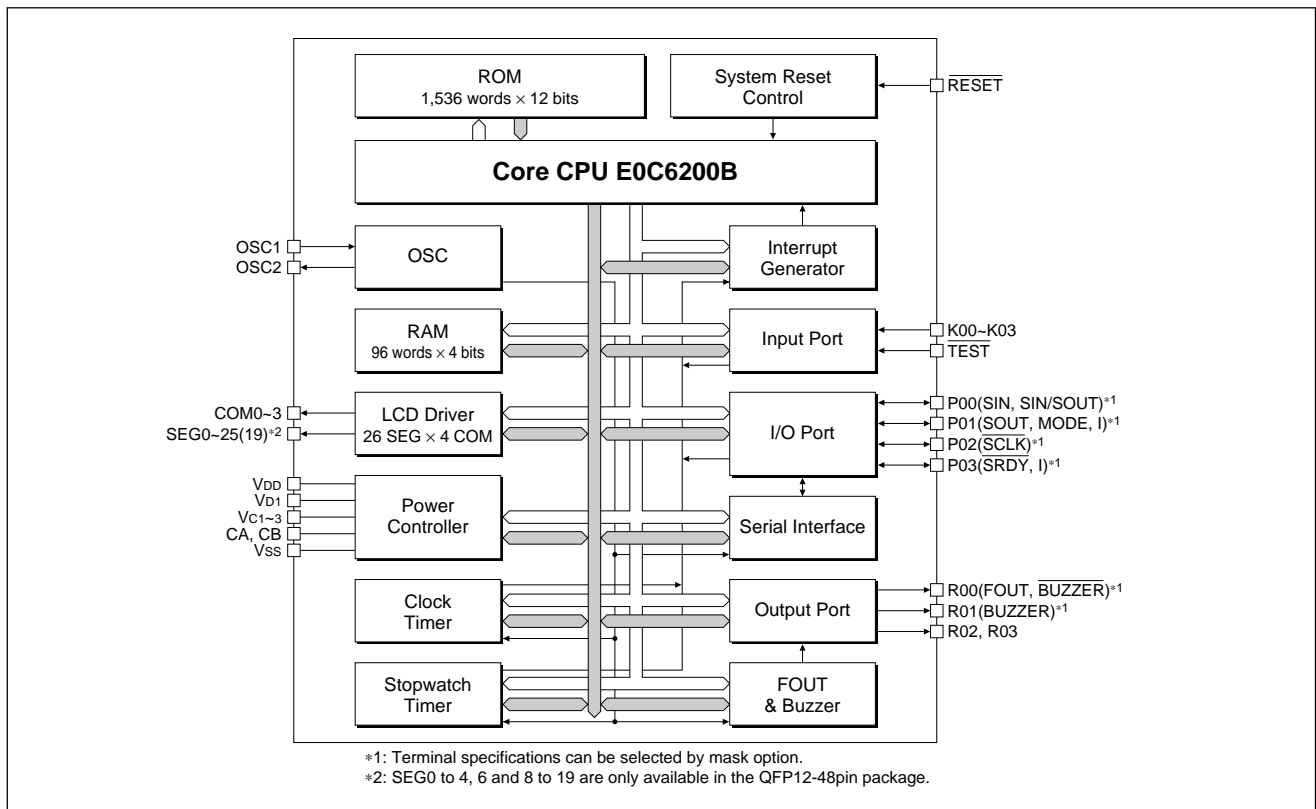


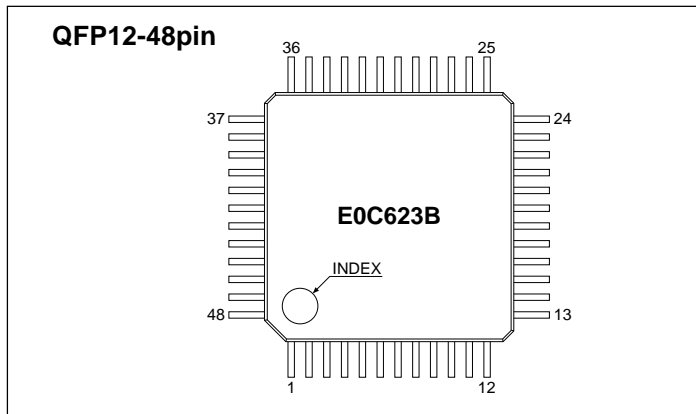


# E0C623B

## ■ BLOCK DIAGRAM

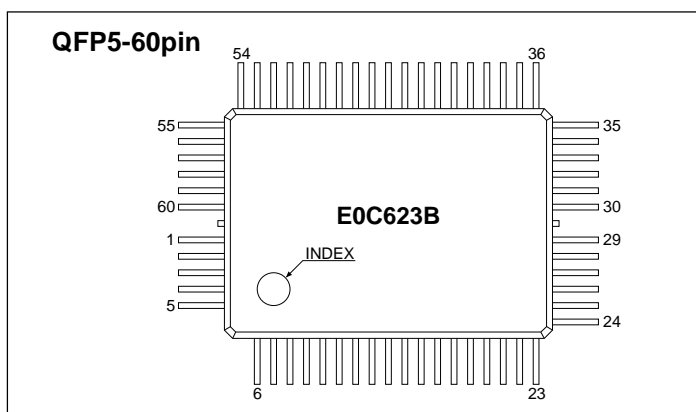


## ■ PIN CONFIGURATION



No.	Pin name	No.	Pin name	No.	Pin name	No.	Pin name
1	COM2	13	SEG12	25	P00	37	VDD
2	COM3	14	SEG13	26	N.C.	38	OSC1
3	SEG0	15	SEG14	27	RESET	39	OSC2
4	SEG1	16	SEG15	28	K00	40	Vd1
5	SEG2	17	SEG16	29	K01	41	CA
6	SEG3	18	SEG17	30	K02	42	CB
7	SEG4	19	SEG18	31	K03	43	N.C.
8	SEG6	20	SEG19	32	R00	44	Vc1
9	SEG8	21	TEST	33	R01	45	Vc2
10	SEG9	22	P03	34	R02	46	Vc3
11	SEG10	23	P02	35	R03	47	COM0
12	SEG11	24	P01	36	VSS	48	COM1

N.C. = No Connection



No.	Pin name	No.	Pin name	No.	Pin name	No.	Pin name
1	Vc2	16	SEG9	31	SEG24	46	K02
2	Vc3	17	SEG10	32	SEG25	47	K03
3	COM0	18	SEG11	33	TEST	48	R00
4	COM1	19	SEG12	34	P03	49	R01
5	COM2	20	SEG13	35	P02	50	R02
6	COM3	21	SEG14	36	P01	51	R03
7	SEG0	22	SEG15	37	P00	52	N.C.
8	SEG1	23	SEG16	38	N.C.	53	VSS
9	SEG2	24	SEG17	39	N.C.	54	VDD
10	SEG3	25	SEG18	40	N.C.	55	OSC1
11	SEG4	26	SEG19	41	N.C.	56	OSC2
12	SEG5	27	SEG20	42	N.C.	57	Vd1
13	SEG6	28	SEG21	43	RESET	58	CA
14	SEG7	29	SEG22	44	K00	59	CB
15	SEG8	30	SEG23	45	K01	60	Vc1

N.C. = No Connection

## PIN DESCRIPTION

Pin name	Pin No.		In/Out	Function
	QFP12-48pin	QFP5-60pin		
V <sub>DD</sub>	37	54	(I)	Power supply pin (+)
V <sub>SS</sub>	36	53	(I)	Power supply pin (-)
V <sub>D1</sub>	40	57	–	Oscillation and internal logic system regulated voltage output pin
V <sub>C1</sub>	44	60	–	LCD system regulated voltage output pin (approx. 1.05 V)
V <sub>C2</sub>	45	1	–	LCD system booster voltage output pin (V <sub>C1</sub> × 2)
V <sub>C3</sub>	46	2	–	LCD system booster voltage output pin (V <sub>C1</sub> × 3)
CA, CB	41, 42	58, 59	–	Boost capacitor connecting pin
OSC1	38	55	I	Oscillation input pin (crystal, CR or ceramic *)
OSC2	39	56	O	Oscillation output pin (crystal, CR or ceramic *)
K00–K03	28–31	44–47	I	Input port pin
P00	25	37	I/O	I/O port pin or serial I/F data input/output pin *
P01	24	36	I/O	I/O port pin, serial I/F data output pin or input-only pin *
P02	23	35	I/O	I/O port pin or serial I/F clock output pin *
P03	22	34	I/O	I/O port pin, serial I/F ready signal output pin or input-only pin *
R00	32	48	O	Output port pin, buzzer or FOUT output pin *
R01	33	49	O	Output port pin or buzzer output pin *
R02, R03	34, 35	50, 51	O	Output port pin
SEG0–4	3–7	7–11	O	LCD segment output pin or DC output pin *
SEG5	–	12	O	LCD segment output pin or DC output pin * (QFP5-60pin only)
SEG6	8	13	O	LCD segment output pin or DC output pin *
SEG7	–	14	O	LCD segment output pin or DC output pin * (QFP5-60pin only)
SEG8–19	9–20	15–26	O	LCD segment output pin or DC output pin *
SEG20–25	–	27–32	O	LCD segment output pin or DC output pin * (QFP5-60pin only)
COM0–3	47, 48, 1, 2	3–6	O	LCD common output pin
RESET	27	43	I	Initial reset input pin
TEST	21	33	I	Input pin for test

\* Selected by mask option

## ELECTRICAL CHARACTERISTICS

### Absolute Maximum Ratings

Rating	Symbol	Value	Unit
Supply voltage	V <sub>DD</sub>	-0.5 to 7.0	V
Input voltage (1)	V <sub>I</sub>	-0.5 to V <sub>DD</sub> + 0.3	V
Input voltage (2)	V <sub>I</sub> OSC	-0.5 to V <sub>D1</sub> + 0.3	V
Permissible total output current *1	ΣI <sub>VDD</sub>	10	mA
Operating temperature	T <sub>opr</sub>	-20 to 70	°C
Storage temperature	T <sub>stg</sub>	-65 to 150	°C
Soldering temperature / time	T <sub>sol</sub>	260°C, 10sec (lead section)	–
Permissible dissipation *2	P <sub>D</sub>	250	mW

(V<sub>SS</sub>=0V)

\*1: The permissible total output current is the sum total of the current (average current) that simultaneously flows from the output pin (or is drawn in).

\*2: In case of plastic package (QFP12-48pin).

### Recommended Operating Conditions

Condition	Symbol	Remark	Min.	Typ.	Max.	Unit
Supply voltage	V <sub>DD</sub>	E0C623B (Crystal oscillation)	1.1		3.6	V
		E0C623B (Crystal oscillation + HVLD*1)	0.8		3.6	V
		E0C623B (CR oscillation)	1.1		3.6	V
		E0C623B (CR oscillation + HVLD*1)	0.8		3.6	V
		E0C62A3B (CR oscillation)	1.7		3.6	V
		E0C62A3B (Ceramic oscillation)	1.7		3.6	V
Oscillation frequency	f <sub>osc</sub>	E0C623B (Crystal oscillation)	–	32.768	–	kHz
		E0C623B (CR oscillation)	30		80	kHz
		E0C62A3B (CR oscillation)			500	kHz
		E0C62A3B (Ceramic oscillation)			1M	Hz

(T<sub>a</sub>=-20 to 70°C)

\*1: HVLD = Heavy load protection mode

# E0C623B

## ● DC Characteristics

(Unless otherwise specified:  $V_{DD}=1.5V$ ,  $V_{SS}=0V$ ,  $f_{osc}=32.768kHz$ ,  $T_a=25^{\circ}C$ ,  $V_{D1}/V_{C1}-V_{C3}$  are internal voltage,  $C_1-C_5=0.1\mu F$ )

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
High level input voltage (1)	$V_{IH1}$	K00-K03, P00-P03	$0.8 \cdot V_{DD}$		$V_{DD}$	V
High level input voltage (2)	$V_{IH2}$	RESET, TEST	$0.9 \cdot V_{DD}$		$V_{DD}$	V
Low level input voltage (1)	$V_{IL1}$	K00-K03, P00-P03	0		$0.1 \cdot V_{DD}$	V
Low level input voltage (2)	$V_{IL2}$	RESET, TEST	0		$0.1 \cdot V_{DD}$	V
High level input current	$I_{IH}$	$V_{IH}=1.5V$ K00-K03, P00-P03, RESET, TEST	0		0.5	$\mu A$
Low level input current (1)	$I_{IL1}$	$V_{IL1}=V_{SS}$ No pull up K00-K03, P00-P03 RESET, TEST	-0.5		0	$\mu A$
Low level input current (2)	$I_{IL2}$	$V_{IL2}=V_{SS}$ With pull up K00-K03, P00-P03 RESET, TEST	-16	-10	-6	$\mu A$
High level output current (1)	$I_{OH1}$	$V_{OH1}=0.9 \cdot V_{DD}$ R00-R03, P00-P03			-0.3	mA
High level output current (2)	$I_{OH2}$	$V_{OH2}=0.9 \cdot V_{DD}$ BZ, $\bar{B}Z$ , FOUT			-0.3	mA
Low level output current (1)	$I_{OL1}$	$V_{OL1}=0.1 \cdot V_{DD}$ R00-R03, P00-P03	0.7			mA
Low level output current (2)	$I_{OL2}$	$V_{OL2}=0.1 \cdot V_{DD}$ BZ, $\bar{B}Z$ , FOUT	0.7			mA
Common output current	$I_{OH3}$	$V_{OH3}=V_{C3}-0.05V$ COM0-COM3			-10	$\mu A$
	$I_{OL3}$	$V_{OL3}=V_{SS}+0.05V$	10			$\mu A$
Segment output current (during LCD output)	$I_{OH4}$	$V_{OH4}=V_{C3}-0.05V$ SEG0-SEG25			-10	$\mu A$
	$I_{OL4}$	$V_{OL4}=V_{SS}+0.05V$	10			$\mu A$
Segment output current (during DC output)	$I_{OH5}$	$V_{OH5}=0.9 \cdot V_{DD}$ SEG0-SEG25			-100	$\mu A$
	$I_{OL5}$	$V_{OL5}=0.1 \cdot V_{DD}$	100			$\mu A$

(Unless otherwise specified:  $V_{DD}=3.0V$ ,  $V_{SS}=0V$ ,  $f_{osc}=32.768kHz$ ,  $T_a=25^{\circ}C$ ,  $V_{D1}/V_{C1}-V_{C3}$  are internal voltage,  $C_1-C_5=0.1\mu F$ )

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
High level input voltage (1)	$V_{IH1}$	K00-K03, P00-P03	$0.8 \cdot V_{DD}$		$V_{DD}$	V
High level input voltage (2)	$V_{IH2}$	RESET, TEST	$0.9 \cdot V_{DD}$		$V_{DD}$	V
Low level input voltage (1)	$V_{IL1}$	K00-K03, P00-P03	0		$0.1 \cdot V_{DD}$	V
Low level input voltage (2)	$V_{IL2}$	RESET, TEST	0		$0.1 \cdot V_{DD}$	V
High level input current	$I_{IH}$	$V_{IH}=3.0V$ K00-K03, P00-P03, RESET, TEST	0		0.5	$\mu A$
Low level input current (1)	$I_{IL1}$	$V_{IL1}=V_{SS}$ No pull up K00-K03, P00-P03 RESET, TEST	-0.5		0	$\mu A$
Low level input current (2)	$I_{IL2}$	$V_{IL2}=V_{SS}$ With pull up K00-K03, P00-P03 RESET, TEST	-32	-20	-12	$\mu A$
High level output current (1)	$I_{OH1}$	$V_{OH1}=0.9 \cdot V_{DD}$ R00-R03, P00-P03			-1.5	mA
High level output current (2)	$I_{OH2}$	$V_{OH2}=0.9 \cdot V_{DD}$ BZ, $\bar{B}Z$ , FOUT			-1.5	mA
Low level output current (1)	$I_{OL1}$	$V_{OL1}=0.1 \cdot V_{DD}$ R00-R03, P00-P03	6			mA
Low level output current (2)	$I_{OL2}$	$V_{OL2}=0.1 \cdot V_{DD}$ BZ, $\bar{B}Z$ , FOUT	6			mA
Common output current	$I_{OH3}$	$V_{OH3}=V_{C3}-0.05V$ COM0-COM3			-10	$\mu A$
	$I_{OL3}$	$V_{OL3}=V_{SS}+0.05V$	10			$\mu A$
Segment output current (during LCD output)	$I_{OH4}$	$V_{OH4}=V_{C3}-0.05V$ SEG0-SEG25			-10	$\mu A$
	$I_{OL4}$	$V_{OL4}=V_{SS}+0.05V$	10			$\mu A$
Segment output current (during DC output)	$I_{OH5}$	$V_{OH5}=0.9 \cdot V_{DD}$ SEG0-SEG25			-300	$\mu A$
	$I_{OL5}$	$V_{OL5}=0.1 \cdot V_{DD}$	300			$\mu A$

## ● Analog Circuit Characteristics and Current Consumption

### LCD drive voltage

(Unless otherwise specified:  $V_{DD}=3.0V$ ,  $V_{SS}=0V$ ,  $f_{osc}=32.768kHz$ ,  $T_a=25^{\circ}C$ ,  $V_{D1}/V_{C1}-V_{C3}$  are internal voltage,  $C_1-C_5=0.1\mu F$ )

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
LCD drive voltage	$V_{C1}$	Connect $1M\Omega$ load resistor between $V_{SS}$ and $V_{C1}$ (no panel load)	0.95	1.05	1.15	V
	$V_{C2}$	Connect $1M\Omega$ load resistor between $V_{SS}$ and $V_{C2}$ (no panel load)	$2 \cdot V_{C1}$ $\times 0.9$		$2 \cdot V_{C1}$ $+0.1$	V
	$V_{C3}$	Connect $1M\Omega$ load resistor between $V_{SS}$ and $V_{C3}$ (no panel load)	$3 \cdot V_{C1}$ $\times 0.9$		$3 \cdot V_{C1}$ $+0.1$	V

## Current consumption

(Unless otherwise specified:  $V_{DD}=3.0V$ ,  $V_{SS}=0V$ ,  $T_a=25^{\circ}C$ ,  $V_{D1}/V_{C1}-V_{C3}$  are internal voltage,  $C_1-C_5=0.1\mu F$ , No panel load)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit	
Current consumption	IOP	HALT mode	623B Crystal oscillation (32.768kHz)	–	2.5	5.0	$\mu A$
			623B Crystal oscillation (32.768kHz)+HVLD*1	–	6.5	9.0	$\mu A$
			623B CR oscillation (40kHz)	–	3.0	6.0	$\mu A$
			623B CR oscillation (40kHz)+HVLD*1	–	7.0	10.0	$\mu A$
			62A3B CR oscillation (250kHz)	–	55	110	$\mu A$
			62A3B Ceramic oscillation (1MHz)	–	80	200	$\mu A$
		RUN mode	623B Crystal oscillation (32.768kHz)	–	3.0	6.0	$\mu A$
			623B Crystal oscillation (32.768kHz)+HVLD*1	–	7.0	10.0	$\mu A$
			623B CR oscillation (40kHz)	–	3.5	7.0	$\mu A$
			623B CR oscillation (40kHz)+HVLD*1	–	7.5	11.0	$\mu A$
			62A3B CR oscillation (250kHz)	–	60	120	$\mu A$
			62A3B Ceramic oscillation (1MHz)	–	100	200	$\mu A$
		SLEEP mode	623B CR oscillation	–	–	1.0	$\mu A$
			62A3B CR oscillation	–	–	1.0	$\mu A$
			62A3B Ceramic oscillation	–	–	1.0	$\mu A$

\*1: HVLD = Heavy load protection mode

## AC Characteristics

### Serial interface

#### Master mode 1

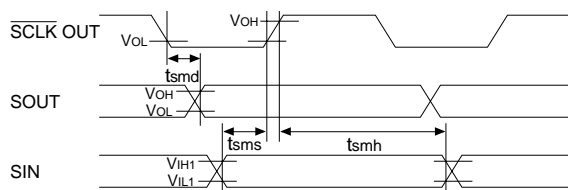
(Unless otherwise specified:  $V_{DD}=1.5V$ ,  $V_{SS}=0V$ ,  $f_{osc}=32.768kHz$ ,  $V_{IH1}=0.8V_{DD}$ ,  $V_{IL1}=0.2V_{DD}$ ,  $V_{OH}=0.8V_{DD}$ ,  $V_{OL}=0.2V_{DD}$ ,  $T_a=-20$  to  $70^{\circ}C$ )

Characteristic	Symbol	Min.	Typ.	Max.	Unit
Transmit data output delay time	$t_{smd}$	–	–	5	$\mu S$
Receive data input set-up time	$t_{sms}$	10	–	–	$\mu S$
Receive data input hold time	$t_{smh}$	5	–	–	$\mu S$

#### Master mode 2

(Unless otherwise specified:  $V_{DD}=3.0V$ ,  $V_{SS}=0V$ ,  $f_{osc}=1MHz$ ,  $V_{IH1}=0.8V_{DD}$ ,  $V_{IL1}=0.2V_{DD}$ ,  $V_{OH}=0.8V_{DD}$ ,  $V_{OL}=0.2V_{DD}$ ,  $T_a=-20$  to  $70^{\circ}C$ )

Characteristic	Symbol	Min.	Typ.	Max.	Unit
Transmit data output delay time	$t_{smd}$	–	–	300	nS
Receive data input set-up time	$t_{sms}$	200	–	–	nS
Receive data input hold time	$t_{smh}$	200	–	–	nS



#### Slave mode 1

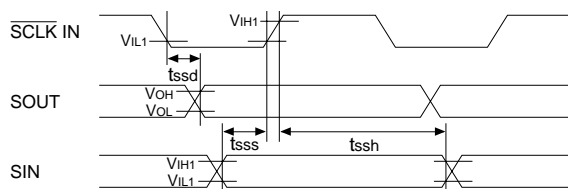
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Characteristic	Symbol	Min.	Typ.	Max.	Unit
Transmit data output delay time	$t_{ssd}$	–	–	5	$\mu S$
Receive data input set-up time	$t_{sss}$	10	–	–	$\mu S$
Receive data input hold time	$t_{ssh}$	5	–	–	$\mu S$

#### Slave mode 2

(Unless otherwise specified:  $V_{DD}=3.0V$ ,  $V_{SS}=0V$ ,  $f_{osc}=1MHz$ ,  $V_{IH1}=0.8V_{DD}$ ,  $V_{IL1}=0.2V_{DD}$ ,  $V_{OH}=0.8V_{DD}$ ,  $V_{OL}=0.2V_{DD}$ ,  $T_a=-20$  to  $70^{\circ}C$ )

Characteristic	Symbol	Min.	Typ.	Max.	Unit
Transmit data output delay time	$t_{ssd}$	–	–	300	nS
Receive data input set-up time	$t_{sss}$	200	–	–	nS
Receive data input hold time	$t_{ssh}$	200	–	–	nS

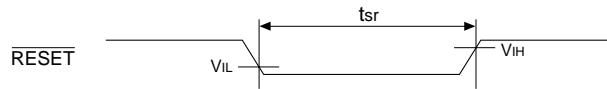


# E0C623B

## RESET input

(Unless otherwise specified:  $V_{DD}=1.5/3.0V$ ,  $V_{SS}=0V$ ,  $V_{IH}=0.5V_{DD}$ ,  $V_{IL}=0.1V_{DD}$ ,  $T_a=-20$  to  $70^{\circ}C$ )

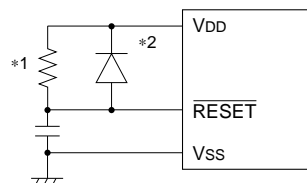
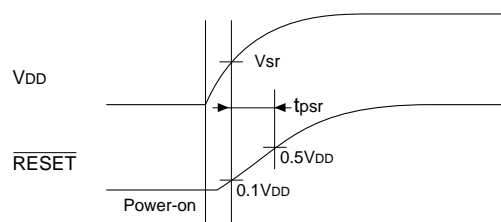
Characteristic	Symbol	Min.	Typ.	Max.	Unit
RESET input time	$t_{sr}$	5.0			mS



## Power-on reset

(Unless otherwise specified:  $V_{DD}=1.5/3.0V$ ,  $T_a=-20$  to  $70^{\circ}C$ )

Characteristic	Symbol	Min.	Typ.	Max.	Unit
Operating supply voltage	$V_{sr}$	$0.8 \cdot V_{DD}$			V
RESET input time	$t_{psr}$	5.0			mS



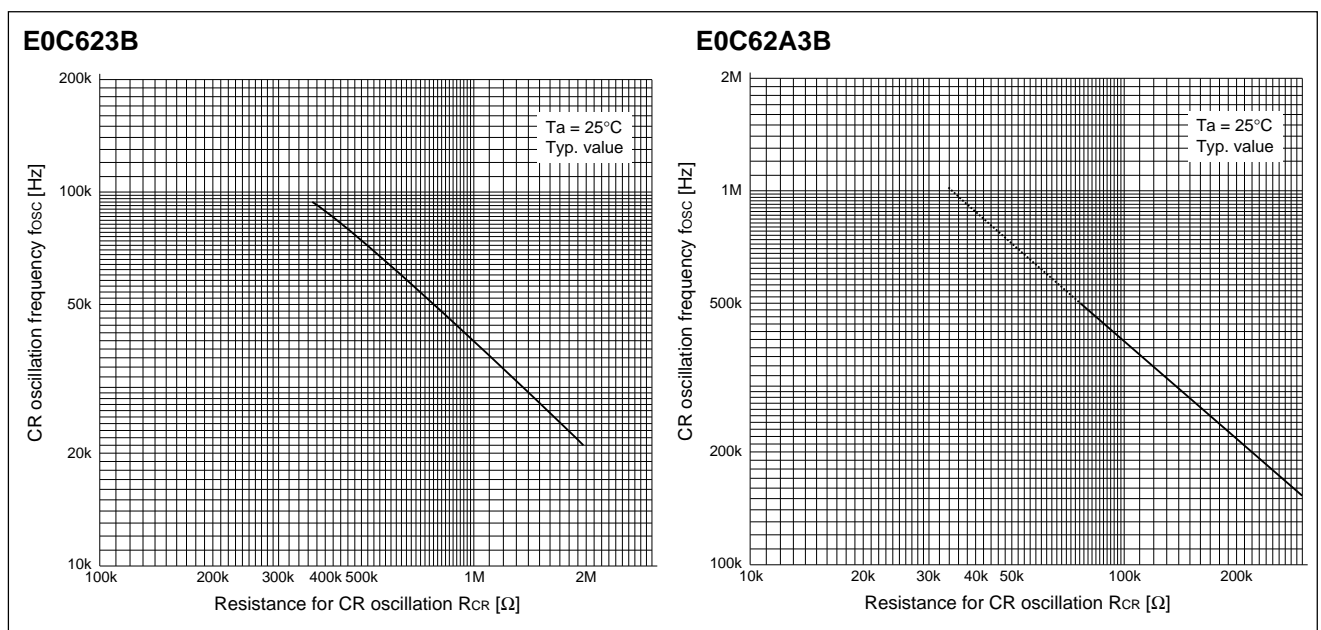
\*1 When the built-in pull-up resistor is not used.

\*2 Because the potential of the RESET terminal not reached  $V_{DD}$  level or higher.

## ● Oscillation Characteristics

Oscillation characteristics will vary according to different conditions (elements used, board pattern). Use the following characteristics are as reference values.

### CR oscillation frequency characteristics (reference value)



## Crystal oscillation

(Unless otherwise specified:  $V_{DD}=3.0V$ ,  $V_{SS}=0V$ ,  $f_{osc}=32.768kHz$ , Crystal: C-002R ( $C_I=35k\Omega$ ),  $C_G=25pF$ ,  $C_D=$ built-in,  $T_a=25^\circ C$ )

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start voltage	$V_{sta}$	$t_{sta} \leq 3sec$ (Heavy load protection mode ON)	0.8			V
		$t_{sta} \leq 3sec$ (Heavy load protection mode OFF)	1.1			V
Oscillation stop voltage	$V_{stp}$	$t_{stp} \leq 10sec$ (Heavy load protection mode ON)	0.8			V
		$t_{stp} \leq 10sec$ (Heavy load protection mode OFF)	1.1			V
Built-in capacitance (drain)	$C_D$	Including the parasitic capacitance inside the IC (in chip)		14		pF
Frequency/voltage deviation	$\partial f/\partial V$	$V_{DD}=0.8$ to $3.6V$ (Heavy load protection mode ON)			5	ppm
		$V_{DD}=1.1$ to $3.6V$ (Heavy load protection mode OFF)			5	ppm
Frequency/IC deviation	$\partial f/\partial IC$		-10		10	ppm
Frequency adjustment range	$\partial f/\partial C_G$	$C_G=5$ to $25pF$	30	40		ppm
Harmonic oscillation start voltage	$V_{hho}$	$C_G=5pF$ ( $V_{DD}$ )	3.6			V
Permitted leak resistance	$R_{leak}$	Between OSC1 and $V_{DD}$ , $V_{SS}$	200			$M\Omega$

## CR oscillation

(Unless otherwise specified:  $V_{DD}=3.0V$ ,  $V_{SS}=0V$ ,  $R_{CR}=1M\Omega$ ,  $T_a=25^\circ C$ )

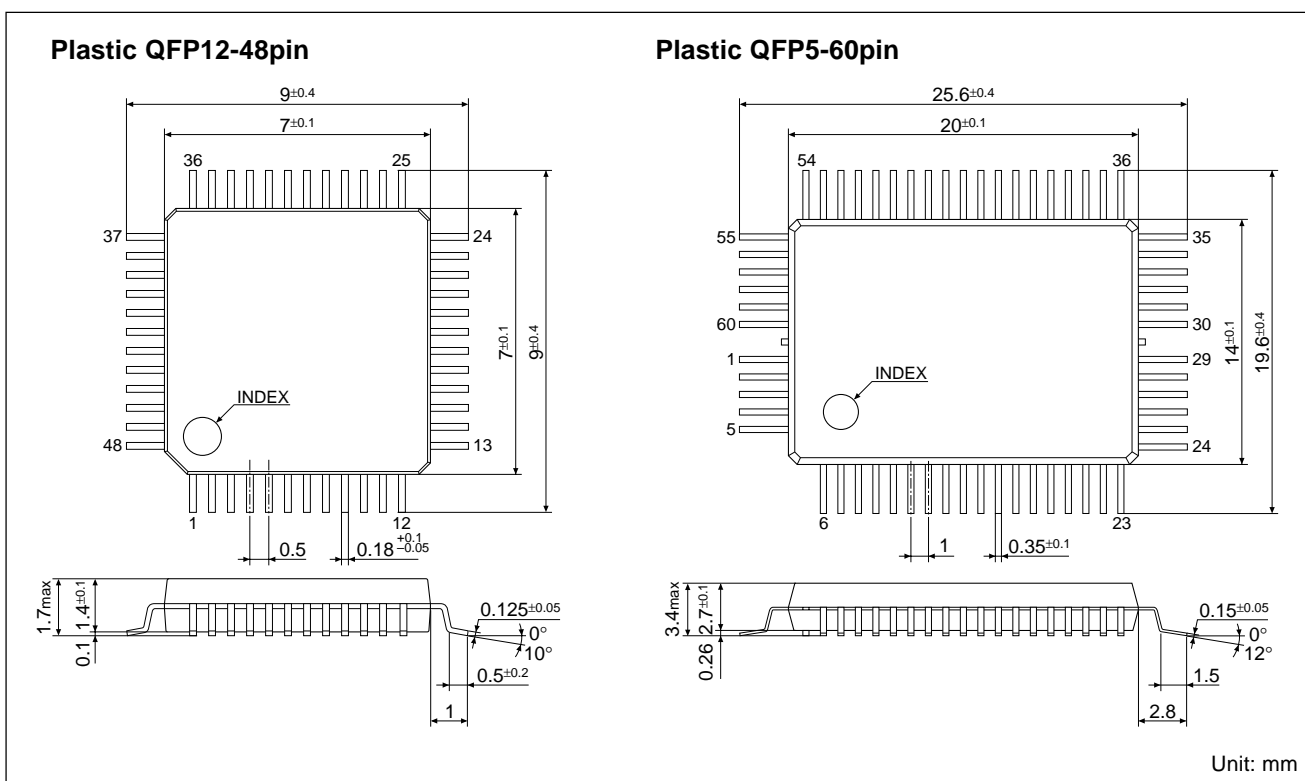
Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation frequency dispersion	$\partial f_{oscCR}$	623B (Heavy load protection ON, $V_{DD}=0.8$ to $3.6V$ )	-20	40kHz	+20	%
		623B (Heavy load protection OFF, $V_{DD}=1.1$ to $3.6V$ )	-20	40kHz	+20	%
		62A3B ( $V_{DD}=1.7$ to $3.6V$ )	-30	500kHz	+30	%
Oscillation start voltage	$V_{sta}$	623B	0.8			V
		62A3B	1.7			V
Oscillation start time	$t_{sta}$				3	mS
Oscillation stop voltage	$V_{stp}$	623B	0.8			V
		62A3B	1.7			V

## Ceramic oscillation

(Unless otherwise specified:  $V_{DD}=3.0V$ ,  $V_{SS}=0V$ , Ceramic oscillator: CSA1.0MG,  $C_{GC}=C_{DC}=100pF$ ,  $T_a=25^\circ C$ )

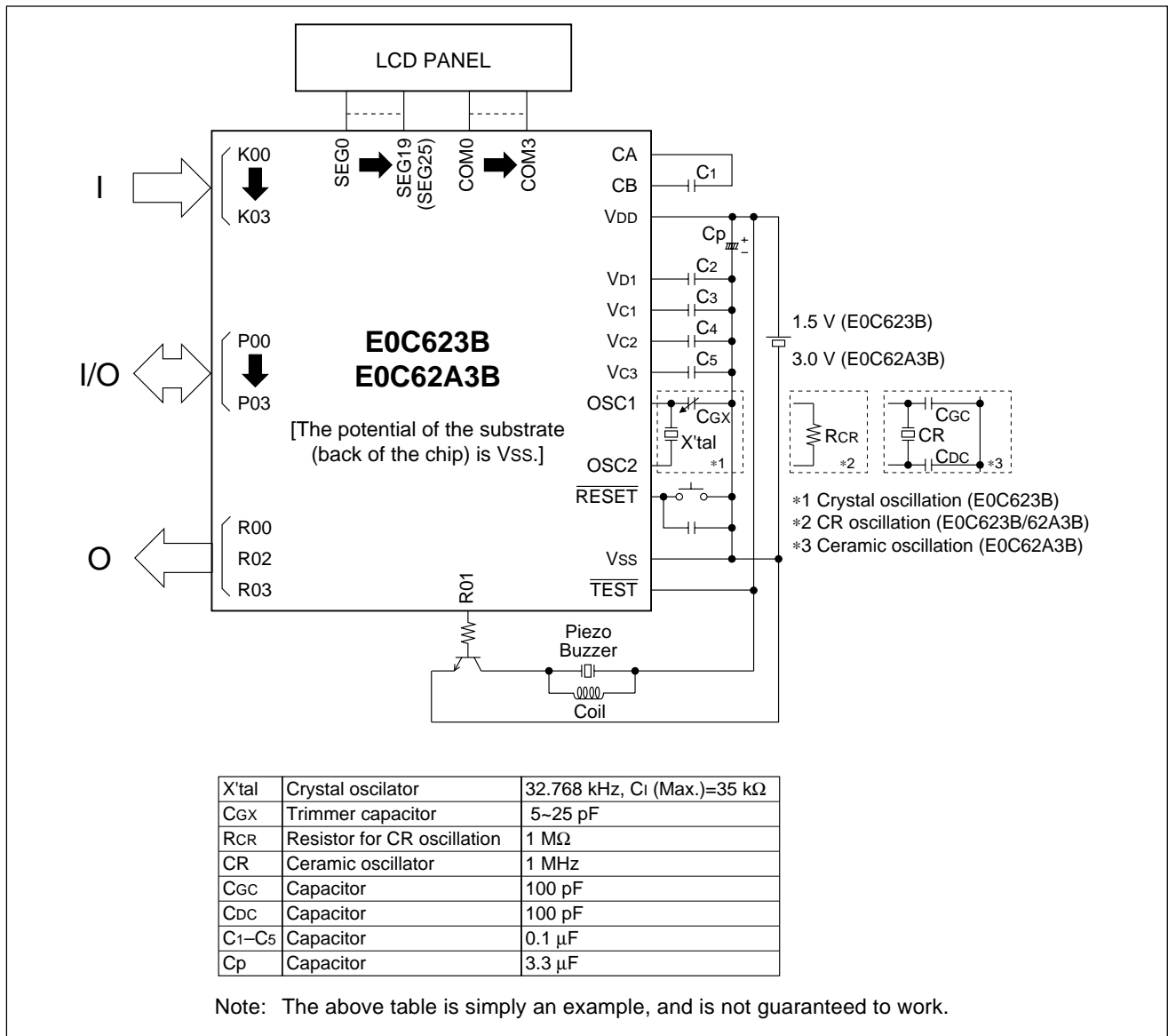
Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start voltage	$V_{sta}$		1.7			V
Oscillation start time	$t_{sta}$				20	mS

## PACKAGE DIMENSIONS



# E0C623B

## ■ BASIC EXTERNAL CONNECTION DIAGRAM



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## SEIKO EPSON CORPORATION

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