

E0C6244

4-bit Single Chip Microcomputer



- Core CPU Architecture
- Dot Matrix LCD Driver
- Programmable SVD Circuit/Sound Generator

■ DESCRIPTION

The E0C6244 is an advanced single-chip CMOS 4-bit microcomputer consisting of the E0C6200 4-bit core CPU. The chip contains the ROM, RAM, dot matrix LCD driver, programmable SVD circuit, time base counter and clock synchronous serial port.

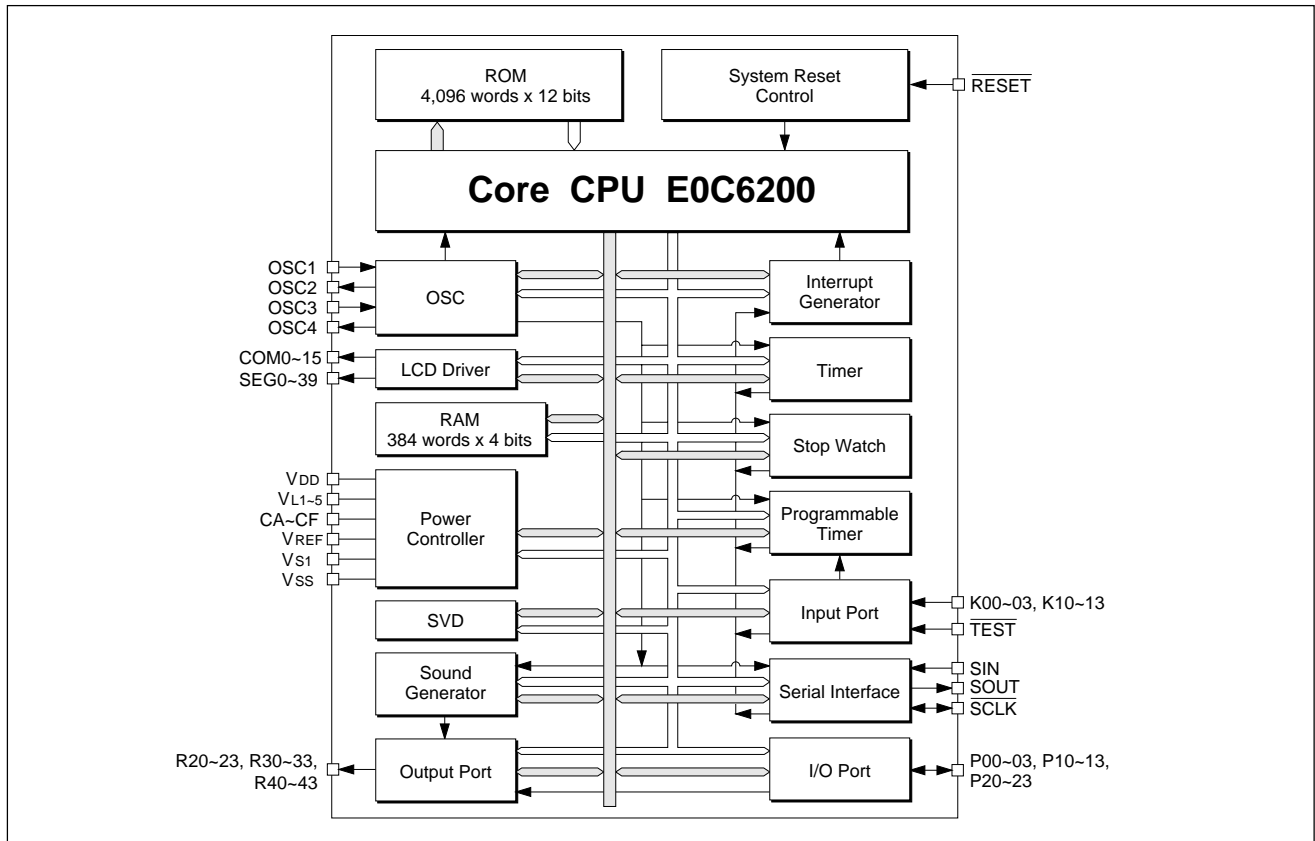
The E0C6244 is suitable for dot matrix display systems.

■ FEATURES

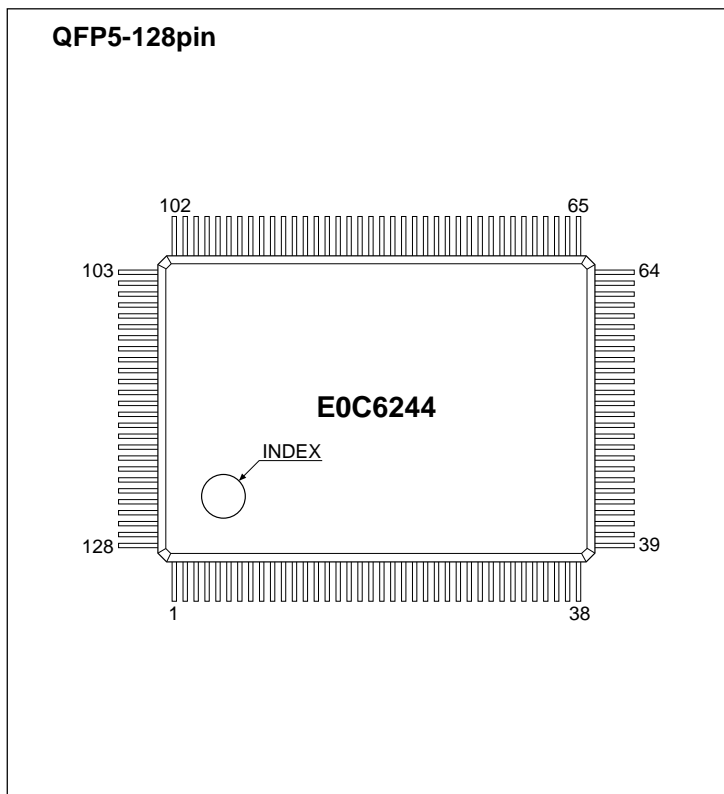
- CMOS LSI 4-bit parallel processing
- Clock 32.768kHz/2MHz (Max.) (selectable by software)
- Instruction set 108 instructions
- Instruction cycle time 153μsec, 214μsec or 366μsec at 32kHz
(depending on instruction)
2μsec, 3μsec or 6μsec at 2MHz
(depending on instruction)
- ROM capacity 4,096 × 12 bits
- RAM capacity 384 × 4 bits
- Input port 8 bits (pull-up resistors are available by mask option)
- Output port 12 bits (clock output or buzzer output is available by mask option)
- I/O port 12 bits (pull-up resistors are available by mask option)
- Serial I/O port 1 port (clock sync.)
- Dot matrix LCD driver 40 segments × 8 commons/40 segments × 16 commons
(1/8 or 1/16 duty is selectable by mask option)
- Built-in SVD circuit Programmable
- Built-in stopwatch timer
- Built-in watchdog timer
- Built-in time base counter 3 lines
- Interrupts External : Input interrupt 2 lines
Internal : Timer interrupt 3 lines
Serial I/O interrupt 1 line
- Built-in sound generator With digital envelope (8 sounds programmable)
- Supply voltage 2.2V to 5.5V
- Current consumption HALT mode (32kHz) : 2.5μA (Typ.)
OPERATING mode (1MHz) : 400μA (Typ.)
- Package QFP5-128pin-S1 (plastic)
Die form

E0C6244

■ BLOCK DIAGRAM



■ PIN CONFIGURATION



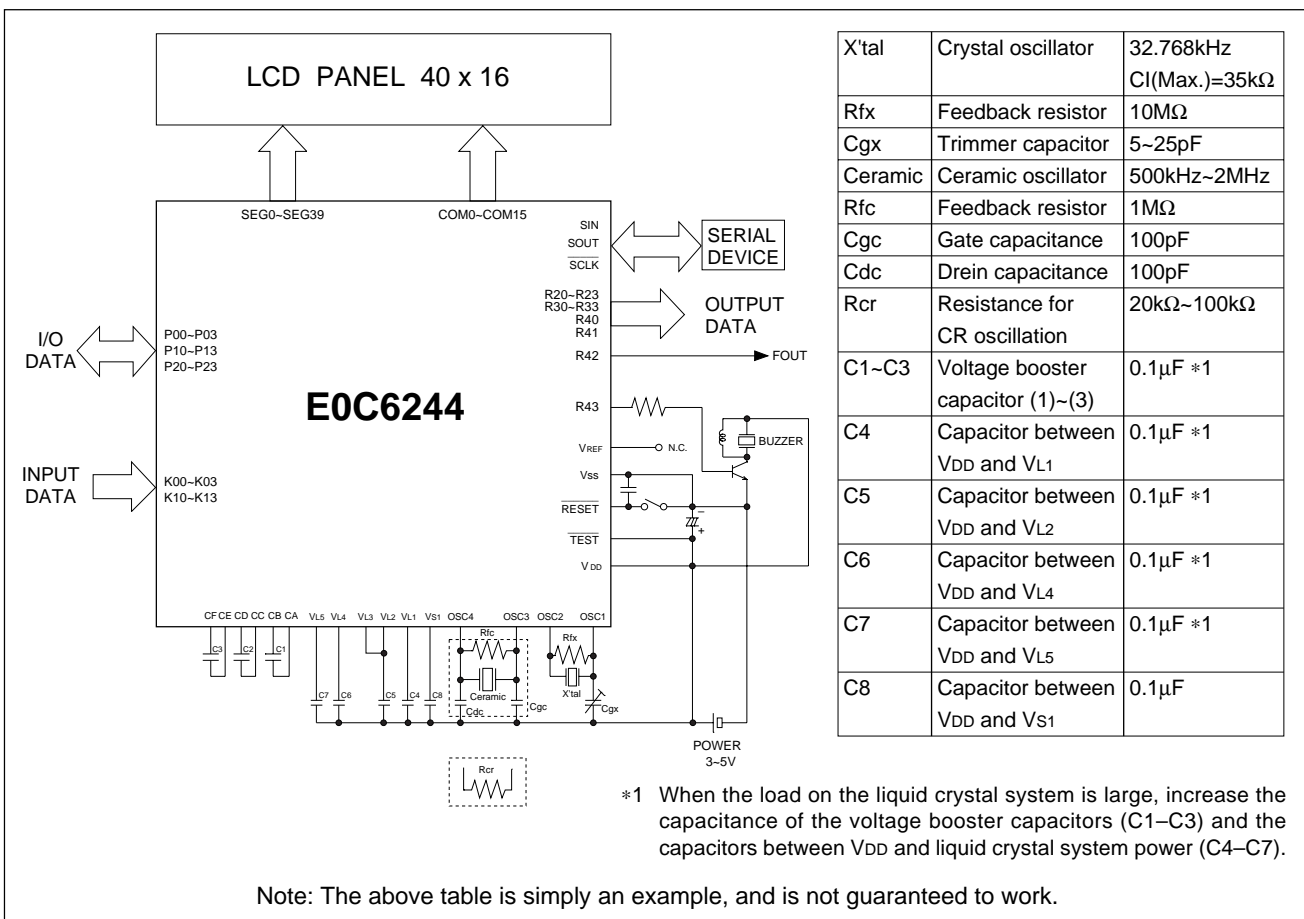
No.	Pin name	No.	Pin name	No.	Pin name	No.	Pin name
1	N.C.	33	SEG30	65	SEG1	97	R40
2	CC	34	SEG29	66	N.C.	98	N.C.
3	N.C.	35	N.C.	67	SEG0	99	N.C.
4	CB	36	SEG28	68	N.C.	100	N.C.
5	CA	37	N.C.	69	N.C.	101	R33
6	N.C.	38	SEG27	70	SCLK	102	R32
7	COM0	39	N.C.	71	SOUT	103	R31
8	COM1	40	SEG26	72	SIN	104	R30
9	COM2	41	SEG25	73	K13	105	R23
10	COM3	42	SEG24	74	K12	106	R22
11	COM4	43	SEG23	75	K11	107	R21
12	COM5	44	SEG22	76	K10	108	R20
13	COM6	45	SEG21	77	K03	109	Vss
14	COM7	46	SEG20	78	K02	110	RESET
15	COM8	47	SEG19	79	K01	111	TEST
16	COM9	48	SEG18	80	K00	112	OSC4
17	COM10	49	SEG17	81	P23	113	OSC3
18	COM11	50	SEG16	82	P22	114	N.C.
19	COM12	51	SEG15	83	P21	115	Vs1
20	COM13	52	SEG14	84	P20	116	OSC2
21	COM14	53	SEG13	85	P13	117	OSC1
22	COM15	54	SEG12	86	P12	118	N.C.
23	N.C.	55	SEG11	87	P11	119	VDD
24	SEG39	56	SEG10	88	P10	120	VREF
25	SEG38	57	SEG9	89	P03	121	VL1
26	SEG37	58	SEG8	90	P02	122	VL2
27	SEG36	59	SEG7	91	P01	123	VL3
28	SEG35	60	SEG6	92	P00	124	VL4
29	SEG34	61	SEG5	93	R43	125	VL5
30	SEG33	62	SEG4	94	R42	126	CF
31	SEG32	63	SEG3	95	N.C.	127	CE
32	SEG31	64	SEG2	96	R41	128	CD

N.C. = No Connection

PIN DESCRIPTION

Pin name	Pin No.	In/Out	Function
VDD	119	I	Power source (+) terminal
VSS	109	I	Power source (-) terminal
Vs1	115	-	Oscillation and internal logic system regulated voltage
VL1-VL5	121-125	-	LCD system power (1/4 or 1/5 bias may be selected by mask option)
VREF	120	O	LCD system power test terminal
CA-CF	5, 4, 2, 128-126	-	Booster capacitor connecting terminal
OSC1	117	I	Crystal or CR oscillation input terminal (selected by mask option)
OSC2	116	O	Crystal or CR oscillation output terminal (selected by mask option)
OSC3	113	I	Ceramic or CR oscillation input terminal (selected by mask option)
OSC4	112	O	Ceramic or CR oscillation output terminal (selected by mask option)
K00-K03, K10-K13	80-73	I	Input terminal (Use of pull up resistor is selected by mask option)
P00-P03, P10-P13 P20-P23	92-81	I/O	I/O terminal
R20-R23, R30-R32	108-102	O	Output terminal
R33	101	O	Output terminal (DC or SRDY output may be selected by mask option)
R40	97	O	Output terminal (DC, CL or FOUT output may be selected by mask option)
R41	96	O	Output terminal (DC or FR output may be selected by mask option)
R42	94	O	Output terminal (DC, BZ or FOUT output may be selected by mask option)
R43	93	O	Output terminal (DC or BZ output may be selected by mask option)
SIN	72	I	Serial interface input terminal
SOUT	71	O	Serial interface output terminal
SCLK	70	I/O	Serial interface clock input/output terminal
SEG0-39	67, 65-40, 38 36, 34-24	O	LCD segment output terminal
COM0-15	7-22	O	LCD common output terminal
RESET	110	I	Initial reset input terminal
TEST	111	I	Test input terminal

BASIC EXTERNAL CONNECTION DIAGRAM



■ ELECTRICAL CHARACTERISTICS

● Absolute Maximum Ratings

(V_{DD}=0V)

Rating	Symbol	Value	Unit
Supply voltage	V _{SS}	-7.0 to 0.5	V
Input voltage (1)	V _I	V _{SS} - 0.3 to 0.5	V
Input voltage (2)	V _{IOSC}	V _{S1} - 0.3 to 0.5	V
Operating temperature	T _{opr}	-20 to 70	°C
Storage temperature	T _{stg}	-65 to 150	°C
Soldering temperature / Time	T _{sol}	260°C, 10sec (lead section)	—
Permissible dissipation *1	P _D	250	mW

*1: In case of plastic package (QFP5-128pin).

● Recommended Operating Conditions

(T_a=-20 to 70°C)

Condition	Symbol	Remark	Min.	Typ.	Max.	Unit	
Supply voltage	V _{SS}	V _{DD} =0V	V _{SC} ="0"	-3.8	-3.0	-1.8	V
			V _{SC} ="1"	-5.5	-3.0	-2.2	V
			V _{SC} ="2"	-5.5	-3.0	-3.5	V
Oscillation frequency (1)	f _{osc1}		20	32.768	50	kHz	
Oscillation frequency (2)	f _{osc3}	V _{SC} ="1"	50	1,000	1,200	kHz	
Oscillation frequency (3)	f _{osc3}	V _{SC} ="2"	50	2,000	2,300	kHz	
Voltage booster capacitor (1)	C1			0.1		μF	
Voltage booster capacitor (2)	C2			0.1		μF	
Voltage booster capacitor (3)	C3			0.1		μF	
Capacitor between V _{DD} and VL1	C4			0.1		μF	
Capacitor between V _{DD} and VL2	C5			0.1		μF	
Capacitor between V _{DD} and VL4	C6			0.1		μF	
Capacitor between V _{DD} and VL5	C7			0.1		μF	
Capacitor between V _{DD} and VS1	C8			0.1		μF	

● DC Characteristics

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-3.0V, V_{L1}=-1.0V, V_{L2}=-2.0V, V_{L4}=-3.0V, V_{L5}=-4.0V, f_{osc1}=32.768kHz, f_{osc3}=1MHz, T_a=25°C, C1-C8=0.047μF)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
High level input voltage	V _{HIN}	V _{SS} =-2.2 to -5.5V	0.2•V _{SS}		0	V
Low level input voltage	V _{LIN}	T _a =25°C	V _{SS}		0.8•V _{SS}	V
High level input voltage	V _{HIN}	V _{SS} =-2.2 to -5.5V	-0.2		0	V
Low level input voltage	V _{LIN}	T _a =25°C	V _{SS}		V _{SS} +0.2	V
High level input current	I _{IH}	V _{SS} =-3.0V V _{IH} =0V	0		0.5	μA
Low level input current (1)	I _{IL1}	V _{SS} =-3.0V V _{IL1} =V _{SS} With pull-up resistor	-45		-15	μA
Low level input current (2)	I _{IL2}	V _{SS} =-3.0V V _{IL2} =V _{SS} No pull-up resistor	-0.5		0	μA
High level output current (1)	I _{OH1}	V _{SS} =-2.2V V _{OH1} =-0.5V			-1.0	mA
Low level output current (1)	I _{OL1}	V _{SS} =-2.2V V _{OL1} =V _{SS} +0.5V	4.0			mA
High level output current (2)	I _{OH2}	V _{SS} =-2.2V V _{OH2} =-0.5V			-2.0	mA
Low level output current (2)	I _{OL2}	V _{SS} =-2.2V V _{OL1} =V _{SS} +0.5V	8.0			mA
Common output current	I _{OH3}	V _{OH3} =-0.05V			-30	μA
	I _{OL3}	V _{OL3} =V _{L5} +0.05V	30			μA
Segment output current	I _{OH4}	V _{OH4} =-0.05V			-10	μA
	I _{OL4}	V _{OL4} =V _{L5} +0.05V	10			μA

● Analog Circuit Characteristics and Current Consumption

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-3.0V, V_{L1}=-1.0V, V_{L2}=-2.0V, V_{L4}=-3.0V, V_{L5}=-4.0V, f_{osc1}=32.768kHz, f_{osc3}=1MHz, T_a=25°C, C₁-C₈=0.047μF)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit	
Liquid crystal drive voltage (Normal mode)	VL1	Connect 1MΩ load resistor between V _{DD} and VL1 (No panel load)	1/2•VL2		1/2•VL2	V	
			-0.1		×0.95		
	VL2	Connect 1MΩ load resistor between V _{DD} and VL2 (No panel load)	LC="0"	Typ.×1.12	-1.80	Typ.×0.88	V
			LC="1"		-1.85		
			LC="2"		-1.90		
			LC="3"		-1.95		
			LC="4"		-2.01		
			LC="5"		-2.06		
			LC="6"		-2.11		
			LC="7"		-2.17		
			LC="8"		-2.22		
			LC="9"		-2.27		
			LC="10"		-2.32		
			LC="11"		-2.38		
			LC="12"		-2.43		
LC="13"	-2.48						
LC="14"	-2.53						
LC="15"	-2.59						
VL4	Connect 1MΩ load resistor between V _{DD} and VL4 (No panel load)	3/2•VL2		3/2•VL2	V		
VL5	Connect 1MΩ load resistor between V _{DD} and VL5 (No panel load)	2•VL2		2•VL2	V		
Liquid crystal drive voltage (Heavy load protection mode)	VL1	Connect 1MΩ load resistor between V _{DD} and VL1 (No panel load)	LC="0"	Typ.×1.12	-0.92	Typ.×0.88	V
			LC="1"		-0.95		
			LC="2"		-0.97		
			LC="3"		-1.00		
			LC="4"		-1.03		
			LC="5"		-1.05		
			LC="6"		-1.08		
			LC="7"		-1.11		
			LC="8"		-1.13		
			LC="9"		-1.16		
			LC="10"		-1.18		
			LC="11"		-1.21		
			LC="12"		-1.24		
	LC="13"	-1.26					
	LC="14"	-1.29					
LC="15"	-1.32						
VL2	Connect 1MΩ load resistor between V _{DD} and VL2 (No panel load)	2•VL1		2•VL1	V		
VL4	Connect 1MΩ load resistor between V _{DD} and VL4 (No panel load)	3•VL1		3•VL1	V		
VL5	Connect 1MΩ load resistor between V _{DD} and VL5 (No panel load)	4•VL1		4•VL1	V		
SVD voltage	V _{SVD0}	SVC="0"	-2.35	-2.20	-2.05	V	
	V _{SVD1}	SVC="1"	-2.70	-2.50	-2.30	V	
	V _{SVD2}	SVC="2"	-3.30	-3.10	-2.90	V	
	V _{SVD3}	SVC="3"	-4.50	-4.20	-3.90	V	
SVD circuit response time	t _{SVD}			100	μS		
Current consumption	I _{hlt}	During HALT	No panel load *1	2.5	5.0	μA	
	I _{EX1}	During operation at 32kHz		6.5	9.0	μA	
	I _{EX2}	During operation at 1MHz	No panel load *2	400	600	μA	
	I _{EX3}	During operation at 2MHz	No panel load *3	1,000	1,500	μA	
Current consumption (OSC1•CR oscillation)	I _{hlt}	During HALT	No panel load *4	20	70	μA	
	I _{EX1}	During operation at f _{osc1}		25	80	μA	
	I _{EX2}	During operation at 1MHz		420	600	μA	
	I _{EX3}	During operation at 2MHz	No panel load *5	1,000	1,500	μA	

*1: SVD circuit: OFF status, VSC = "0", OSC1: oscillating with crystal, OSCC = "0"

*2: SVD circuit: OFF status, VSC = "1", OSC1: oscillating with crystal

*3: SVD circuit: OFF status, VSC = "2", OSC1: oscillating with crystal, V_{SS} = -5.0V

*4: SVD circuit: OFF status, VSC = "0" or "1", OSC1: oscillating with CR, OSCC = "0", R_{osc} for OSC1 = 1.6MΩ

*5: SVD circuit: OFF status, VSC = "2", OSC1: oscillating with CR, OSCC = "0", R_{osc} for OSC1 = 1.6MΩ

● Oscillation Characteristics

The oscillation characteristics change depending on the conditions (components used, board pattern, etc.). Use the following characteristics as reference values.

OSC1 crystal oscillation circuit

(Unless otherwise specified: $V_{DD}=0V$, $V_{SS}=-3.0V$, Crystal: C-002R ($C_i=35k\Omega$), $C_{Gx}=25pF$, C_{Dx} =built-in, $R_{fx}=10M\Omega$, $VSC="0"$, $T_a=25^\circ C$)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start time	t_{sta}	$V_{SS}=-2.2$ to $-5.5V$			5	Sec
Built-in capacitance (drain)	C_D	Package as assembled		22		pF
		Bare chip		21		pF
Frequency/voltage deviation	$\partial f/\partial V$	$V_{SS}=-2.2$ to $-5.5V$			5	ppm
Frequency/IC deviation	$\partial f/\partial IC$		-10		10	ppm
Frequency adjustment range	$\partial f/\partial C_G$	$C_G=5$ to $25pF$	35	45		ppm
Harmonic oscillation start voltage	V_{hho}	$C_G=5pF$			-5.5	V
Permitted leak resistance	R_{leak}	Between OSC1 and V_{DD} , V_{S1}	200			$M\Omega$

OSC1 CR oscillation circuit

(Unless otherwise specified: $V_{DD}=0V$, $V_{SS}=-3.0V$, $VSC="0"$ or $"1"$, $T_a=25^\circ C$)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start time	t_{sta}	$V_{SS}=-2.2$ to $-5.5V$			3	mS
Frequency/voltage deviation	$\partial f/\partial V$	$V_{SS}=-2.2$ to $-5.5V$	-5		5	%
Oscillation frequency	f_{CR}	$R_{osc}=1.6M\Omega$	$32\times 70\%$	32	$32\times 130\%$	kHz

OSC3 CR oscillation circuit (1)

(Unless otherwise specified: $V_{DD}=0V$, $V_{SS}=-3.0V$, $VSC="1"$, $T_a=25^\circ C$)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start time	t_{sta}	$V_{SS}=-2.2$ to $-5.5V$			3	mS
Frequency/voltage deviation	$\partial f/\partial V$	$V_{SS}=-2.2$ to $-5.5V$	-5		5	%
Oscillation frequency	f_{CR}	$R_{osc}=40k\Omega$	$860\times 70\%$	860	$860\times 130\%$	kHz

OSC3 CR oscillation circuit (2)

(Unless otherwise specified: $V_{DD}=0V$, $V_{SS}=-5.0V$, $VSC="2"$, $T_a=25^\circ C$)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start time	t_{sta}	$V_{SS}=-3.5$ to $-5.5V$			3	mS
Frequency/voltage deviation	$\partial f/\partial V$	$V_{SS}=-3.5$ to $-5.5V$	-5		5	%
Oscillation frequency	f_{CR}	$R_{osc}=20k\Omega$	$1.7\times 70\%$	1.7	$1.7\times 130\%$	MHz

OSC3 ceramic oscillation circuit (1)

(Unless otherwise specified: $V_{DD}=0V$, $V_{SS}=-3.0V$, $VSC="1"$, Ceramic: CSB 1000J (Murata Mfg. Co.), $C_{Gc}=C_{Dc}=100pF$, $R_{rc}=1M\Omega$, $T_a=25^\circ C$)

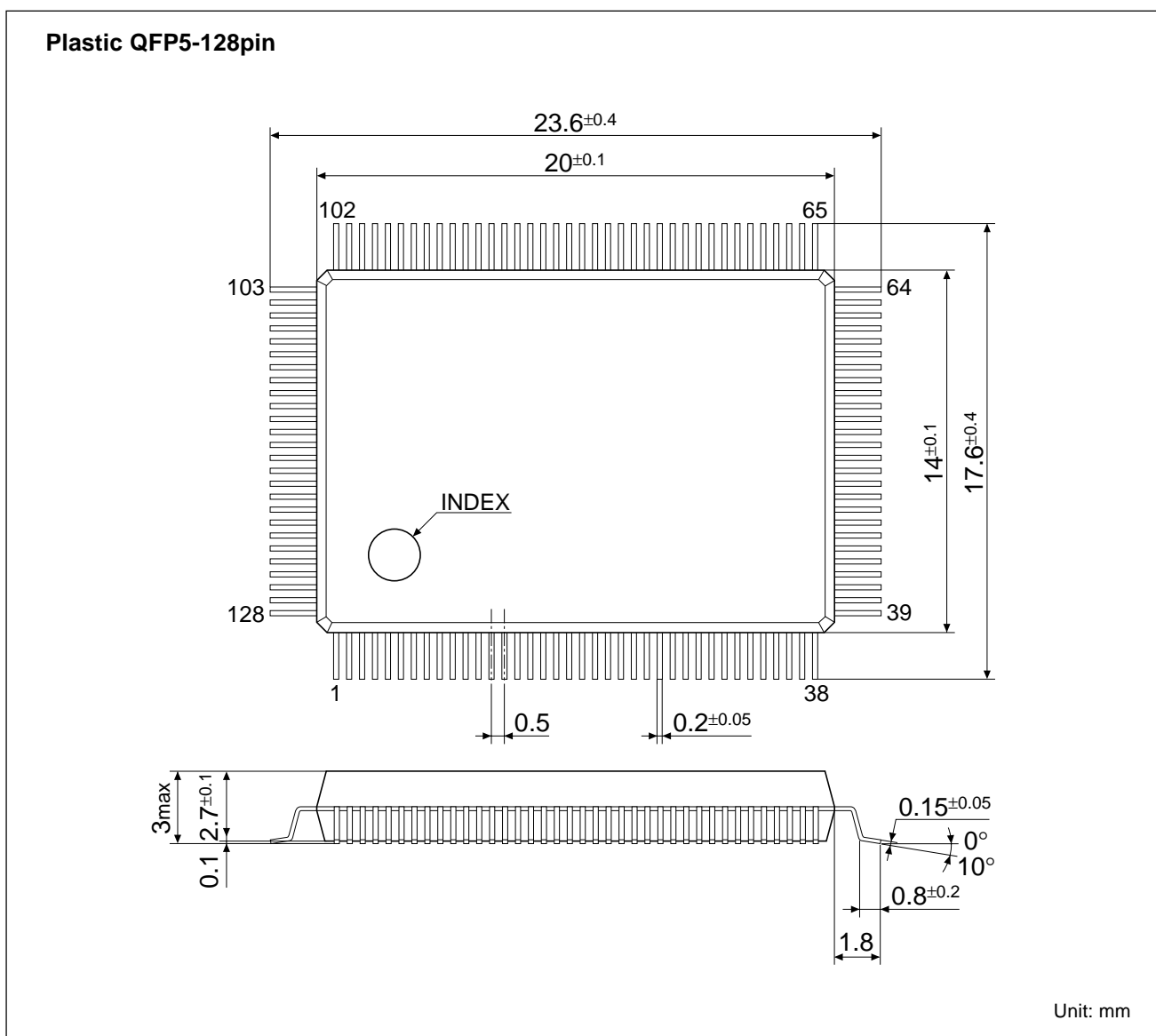
Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start time	t_{sta}	$V_{SS}=-2.2$ to $-5.5V$			3	mS
Frequency/voltage deviation	$\partial f/\partial V$	$V_{SS}=-2.2$ to $-5.5V$	-3		3	%

OSC3 ceramic oscillation circuit (2)

(Unless otherwise specified: $V_{DD}=0V$, $V_{SS}=-5.0V$, $VSC="2"$, Ceramic: CSA 2.00MG (Murata Mfg. Co.), $C_{Gc}=C_{Dc}=100pF$, $R_{rc}=1M\Omega$, $T_a=25^\circ C$)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start time	t_{sta}	$V_{SS}=-3.5$ to $-5.5V$			3	mS
Frequency/voltage deviation	$\partial f/\partial V$	$V_{SS}=-3.5$ to $-5.5V$	-3		3	%

■ PACKAGE DIMENSIONS



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SEIKO EPSON CORPORATION

ELECTRONIC DEVICES MARKETING DIVISION

IC Marketing & Engineering Group

ED International Marketing Department I (Europe & U.S.A.)

421-8, Hino, Hino-shi, Tokyo 191-8501, JAPAN
Phone : 042-587-5812 FAX : 042-587-5564

ED International Marketing Department II (Asia)

421-8, Hino, Hino-shi, Tokyo 191-8501, JAPAN
Phone : 042-587-5814 FAX : 042-587-5110

