

## 4-bit Single Chip Microcomputer



- Core CPU Architecture
- Dot Matrix LCD Driver
- Programmable SVD Circuit/Sound Generator

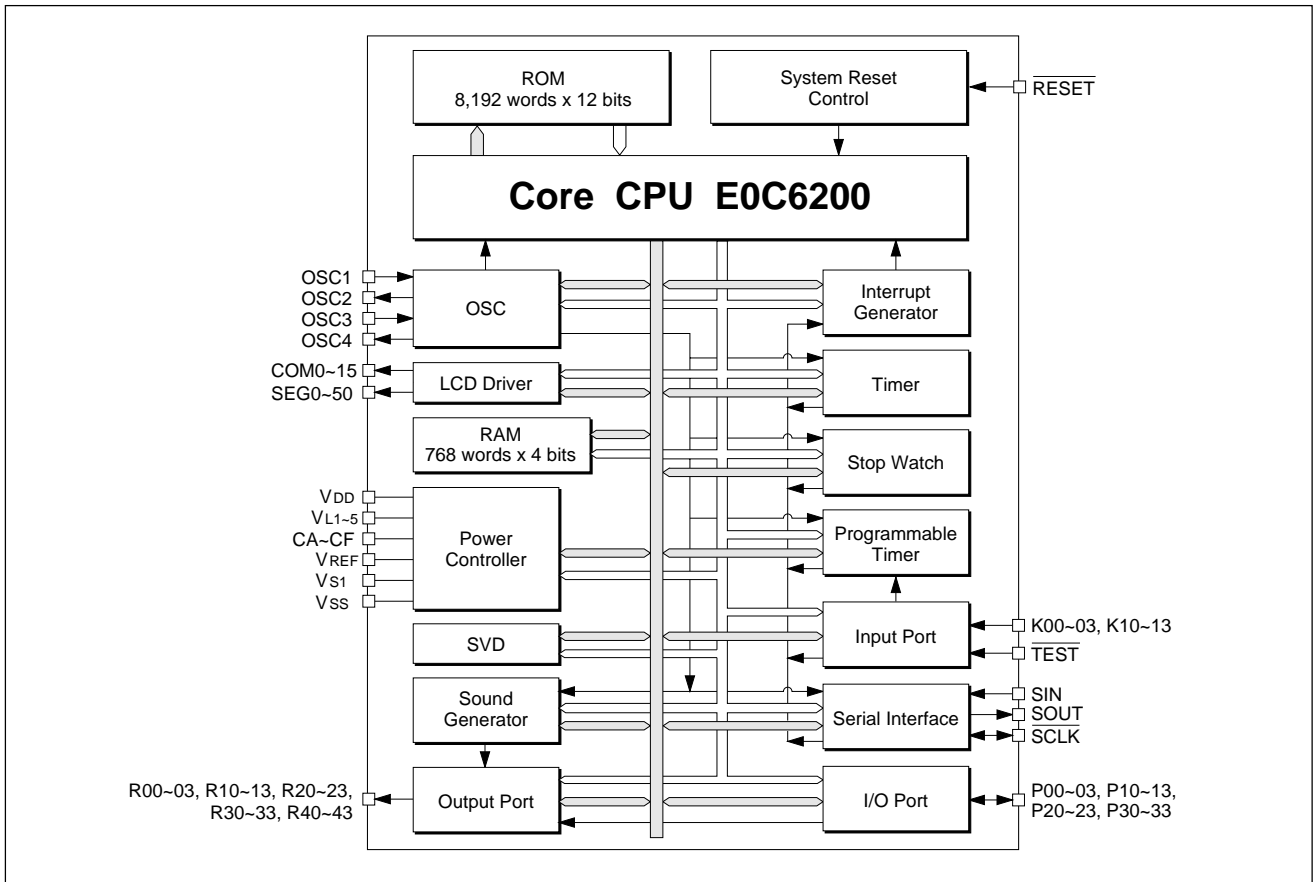
### ■ DESCRIPTION

The E0C6248 is a single-chip microcomputer made up of the 4-bit core CPU E0C6200, ROM, RAM, dot matrix LCD driver, input ports, output ports, I/O ports, clock timer, stopwatch timer, programmable timer, clock-synchronized serial interface, sound generator and watchdog timer. Moreover, external memory device control is possible, and is most suitable for applications with equipment requiring large memory and dot matrix display functions such as a highly functional electronic notebook.

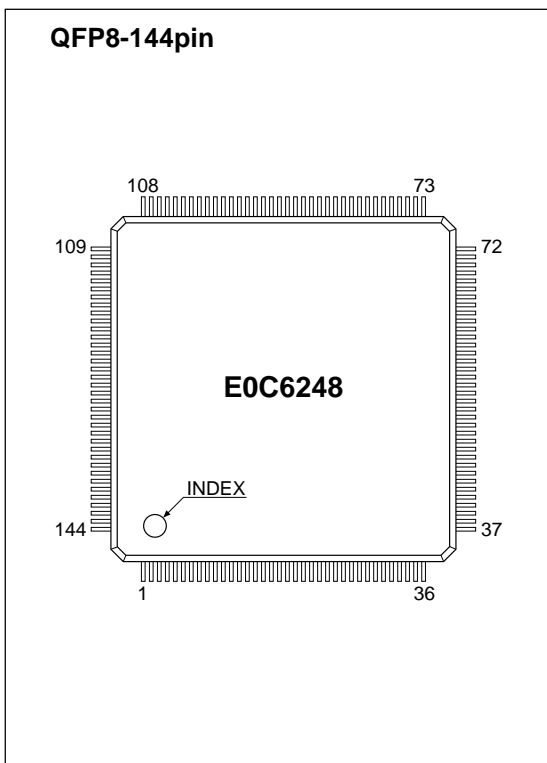
### ■ FEATURES

- CMOS LSI 4-bit parallel processing
- Clock ..... 32.768kHz/2MHz (Max.) (selectable by software)
- Instruction set ..... 108 instructions
- Instruction cycle time ..... 153μsec, 214μsec or 366μsec at 32kHz  
(depending on instruction)  
2μsec, 3μsec or 6μsec at 2MHz  
(depending on instruction)
- ROM capacity ..... 8,192 × 12 bits
- RAM capacity ..... 768 × 4 bits
- External memory capacity ..... Read/Write 512K bits (Max.)  
Read only 1M bits (Max.)
- Input port ..... 8 bits (pull-up resistors are available by mask option)
- Output port ..... 20 bits (clock output or buzzer output is available by mask option)
- I/O port ..... 16 bits (pull-up resistors are available by mask option)
- Serial I/O port ..... 1 port (clock sync.)
- Dot matrix LCD driver ..... 51 segments × 8 commons/51 segments × 16 commons  
(1/8 or 1/16 duty is selectable by mask option)
- Built-in SVD circuit ..... Programmable
- Built-in stopwatch timer
- Built-in watchdog timer
- Built-in time base counter ..... 3 lines
- Interrupts ..... External : Input interrupt 2 lines  
Internal : Timer interrupt 3 lines  
Serial I/O interrupt 1 line
- Built-in sound generator ..... With digital envelope (8 sounds programmable)
- Supply voltage ..... 2.2V to 5.5V
- Current consumption ..... HALT mode (32kHz) : 2.5μA (Typ.)  
OPERATING mode (1MHz) : 400μA (Typ.)
- Package ..... QFP8-144pin (plastic)  
Die form

■ BLOCK DIAGRAM



■ PIN CONFIGURATION



No.	Pin name	No.	Pin name	No.	Pin name	No.	Pin name	No.	Pin name
1	CB	30	SEG41	59	SEG15	88	P33	117	R13
2	CA	31	SEG40	60	SEG14	89	P32	118	R12
3	N.C.	32	SEG39	61	SEG13	90	P31	119	R11
4	COM0	33	SEG38	62	SEG12	91	P30	120	R10
5	COM1	34	SEG37	63	SEG11	92	P23	121	R03
6	COM2	35	N.C.	64	SEG10	93	P22	122	R02
7	COM3	36	N.C.	65	SEG9	94	P21	123	R01
8	COM4	37	SEG36	66	SEG8	95	P20	124	R00
9	COM5	38	SEG35	67	SEG7	96	P13	125	VSS
10	COM6	39	SEG34	68	SEG6	97	N.C.	126	RESET
11	COM7	40	SEG33	69	SEG5	98	P12	127	TEST
12	COM8	41	SEG32	70	SEG4	99	P11	128	OSC4
13	COM9	42	SEG31	71	SEG3	100	P10	129	OSC3
14	COM10	43	SEG30	72	SEG2	101	P03	130	VS1
15	COM11	44	SEG29	73	SEG1	102	P02	131	OSC2
16	COM12	45	SEG28	74	SEG0	103	P01	132	OSC1
17	COM13	46	SEG27	75	N.C.	104	P00	133	N.C.
18	COM14	47	SEG26	76	SCLK	105	R43	134	VDD
19	N.C.	48	SEG25	77	SOUT	106	R42	135	VREF
20	COM15	49	SEG24	78	SIN	107	R41	136	VL1
21	SEG50	50	N.C.	79	K13	108	R40	137	VL2
22	SEG49	51	SEG23	80	K12	109	R33	138	VL3
23	SEG48	52	SEG22	81	K11	110	R32	139	VL4
24	SEG47	53	SEG21	82	K10	111	R31	140	VL5
25	SEG46	54	SEG20	83	K03	112	R30	141	CF
26	SEG45	55	SEG19	84	N.C.	113	R23	142	CE
27	SEG44	56	SEG18	85	K02	114	R22	143	CD
28	SEG43	57	SEG17	86	K01	115	R21	144	CC
29	SEG42	58	SEG16	87	K00	116	R20		

N.C. = No Connection

**PIN DESCRIPTION**

Pin name	Pin No.	In/Out	Function
VDD	134	I	Power source (+) terminal
VSS	125	I	Power source (-) terminal
Vs1	130	-	Oscillation and internal logic system regulated voltage
VL1-VL5	136-140	-	LCD system power (1/4 or 1/5 bias may be selected by mask option)
VREF	135	O	LCD system power test terminal
CA-CF	2, 1, 144-141	-	Booster capacitor connecting terminal
OSC1	132	I	Crystal or CR oscillation input terminal (selected by mask option)
OSC2	131	O	Crystal or CR oscillation output terminal (selected by mask option)
OSC3	129	I	Ceramic or CR oscillation input terminal (selected by mask option)
OSC4	128	O	Ceramic or CR oscillation output terminal (selected by mask option)
K00-K03, K10-K13	87-85, 83-79	I	Input terminal (Use of pull up resistor is selected by mask option)
P00-P03, P10-P13	104-98, 96	I/O	I/O terminal (Setting for data bus may be selected by mask option)
P20-P23	95-92	I/O	I/O terminal (CS output may be selected by mask option)
P30-P33	91-88	I/O	I/O terminal
R00-R03, R10-R13 R20-R23, R30	124-112	O	Output terminal (Setting for address bus may be selected by mask option)
R31	111	O	Output terminal (DC, address or WR output may be selected by mask option)
R32	110	O	Output terminal (DC or RD output may be selected by mask option)
R33	109	O	Output terminal (DC or SRDY output may be selected by mask option)
R40	108	O	Output terminal (DC, CL or FOUT output may be selected by mask option)
R41	107	O	Output terminal (DC or FR output may be selected by mask option)
R42	106	O	Output terminal (DC, BZ or FOUT output may be selected by mask option)
R43	105	O	Output terminal (DC or BZ output may be selected by mask option)
SIN	78	I	Serial interface input terminal
SOUT	77	O	Serial interface output terminal
SCLK	76	I/O	Serial interface clock input/output terminal
SEG0-50	74-51, 49-37 34-21	O	LCD segment output terminal
COM0-15	4-18, 20	O	LCD common output terminal
RESET	126	I	Initial reset input terminal
TEST	127	I	Test input terminal

**BASIC EXTERNAL CONNECTION DIAGRAM**

X'tal	Crystal oscillator	32.768kHz CI(Max.)=35kΩ
Rfx	Feedback resistor	10MΩ
Cgx	Trimmer capacitor	5~25pF
Ceramic	Ceramic oscillator	500kHz~2MHz
Rfc	Feedback resistor	1MΩ
Cgc	Gate capacitance	100pF
Cdc	Drein capacitance	100pF
Rcr	Resistance for CR oscillation	20kΩ~100kΩ
C1-C3	Voltage booster capacitor (1)-(3)	0.1μF *1
C4	Capacitor between VDD and VL1	0.1μF *1
C5	Capacitor between VDD and VL2	0.1μF *1
C6	Capacitor between VDD and VL4	0.1μF *1
C7	Capacitor between VDD and VL5	0.1μF *1
C8	Capacitor between VDD and Vs1	0.1μF

\*1 When the load on the liquid crystal system is large, increase the capacitance of the voltage booster capacitors (C1-C3) and the capacitors between VDD and liquid crystal system power (C4-C7).

Note: The above table is simply an example, and is not guaranteed to work.

■ ELECTRICAL CHARACTERISTICS

● Absolute Maximum Ratings

(VDD=0V)

Rating	Symbol	Value	Unit
Supply voltage	Vss	-7.0 to 0.5	V
Input voltage (1)	Vi	Vss - 0.3 to 0.5	V
Input voltage (2)	Viosc	Vs1 - 0.3 to 0.5	V
Operating temperature	Topr	-20 to 70	°C
Storage temperature	Tstg	-65 to 150	°C
Soldering temperature / Time	Tsol	260°C, 10sec (lead section)	—
Permissible dissipation *1	Pd	250	mW

\*1: In case of plastic package (QFP8-144pin).

● Recommended Operating Conditions

(Ta=-20 to 70°C)

Condition	Symbol	Remark	Min.	Typ.	Max.	Unit	
Supply voltage	Vss	VDD=0V	VSC="0"	-3.8	-3.0	-1.8	V
			VSC="1"	-5.5	-3.0	-2.2	V
			VSC="2"	-5.5	-3.0	-3.5	V
Oscillation frequency (1)	fosc1		20	32.768	50	kHz	
Oscillation frequency (2)	fosc3	VSC="1"	50	1,000	1,200	kHz	
Oscillation frequency (3)	fosc3	VSC="2"	50	2,000	2,300	kHz	
Voltage booster capacitor (1)	C1			0.1		μF	
Voltage booster capacitor (2)	C2			0.1		μF	
Voltage booster capacitor (3)	C3			0.1		μF	
Capacitor between VDD and VL1	C4			0.1		μF	
Capacitor between VDD and VL2	C5			0.1		μF	
Capacitor between VDD and VL4	C6			0.1		μF	
Capacitor between VDD and VL5	C7			0.1		μF	
Capacitor between VDD and Vs1	C8			0.1		μF	

● DC Characteristics

(Unless otherwise specified: VDD=0V, VSS=-3.0V, VL1=-1.0V, VL2=-2.0V, VL4=-3.0V, VL5=-4.0V, fosc1=32.768kHz, fosc3=1MHz, Ta=25°C, C1-C8=0.047μF)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
High level input voltage	VHIN	VSS=-2.2 to -5.5V	0.2•Vss		0	V
Low level input voltage	VLIN	Ta=25°C	Vss		0.8•Vss	V
High level input voltage	VHIN	VSS=-2.2 to -5.5V	-0.2		0	V
Low level input voltage	VLIN	Ta=25°C	Vss		Vss+0.2	V
High level input current	IiH	VSS=-3.0V ViH=0V	0		0.5	μA
Low level input current (1)	IiL1	VSS=-3.0V ViL1=Vss With pull-up resistor	-45		-15	μA
Low level input current (2)	IiL2	VSS=-3.0V ViL2=Vss No pull-up resistor	-0.5		0	μA
High level output current (1)	IoH1	VSS=-2.2V VoH1=-0.5V			-1.0	mA
Low level output current (1)	IoL1	VSS=-2.2V VoL1=Vss+0.5V	4.0			mA
High level output current (2)	IoH2	VSS=-2.2V VoH2=-0.5V			-2.0	mA
Low level output current (2)	IoL2	VSS=-2.2V VoL1=Vss+0.5V	8.0			mA
Common output current	IoH3	VoH3=-0.05V			-30	μA
	IoL3	VoL3=VL5+0.05V	30			μA
Segment output current	IoH4	VoH4=-0.05V			-10	μA
	IoL4	VoL4=VL5+0.05V	10			μA

● Analog Circuit Characteristics and Current Consumption

(Unless otherwise specified: V<sub>DD</sub>=0V, V<sub>SS</sub>=-3.0V, V<sub>L1</sub>=-1.0V, V<sub>L2</sub>=-2.0V, V<sub>L4</sub>=-3.0V, V<sub>L5</sub>=-4.0V, f<sub>osc1</sub>=32.768kHz, f<sub>osc3</sub>=1MHz, T<sub>a</sub>=25°C, C<sub>1</sub>-C<sub>8</sub>=0.047μF)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit	
Liquid crystal drive voltage (Normal mode)	VL1	Connect 1MΩ load resistor between V <sub>DD</sub> and VL1 (No panel load)	1/2•VL2		1/2•VL2	V	
			-0.1		×0.95		
	VL2	Connect 1MΩ load resistor between V <sub>DD</sub> and VL2 (No panel load)	LC="0"	Typ.×1.12	-1.80	Typ.×0.88	V
			LC="1"		-1.85		
			LC="2"		-1.90		
			LC="3"		-1.95		
			LC="4"		-2.01		
			LC="5"		-2.06		
			LC="6"		-2.11		
			LC="7"		-2.17		
			LC="8"		-2.22		
			LC="9"		-2.27		
			LC="10"		-2.32		
			LC="11"		-2.38		
			LC="12"		-2.43		
LC="13"	-2.48						
LC="14"	-2.53						
LC="15"	-2.59						
VL4	Connect 1MΩ load resistor between V <sub>DD</sub> and VL4 (No panel load)	3/2•VL2		3/2•VL2	V		
VL5	Connect 1MΩ load resistor between V <sub>DD</sub> and VL5 (No panel load)	2•VL2		2•VL2	V		
				×0.95			
Liquid crystal drive voltage (Heavy load protection mode)	VL1	Connect 1MΩ load resistor between V <sub>DD</sub> and VL1 (No panel load)	Typ.×1.12	-0.92	Typ.×0.88	V	
				LC="1"			-0.95
				LC="2"			-0.97
				LC="3"			-1.00
				LC="4"			-1.03
				LC="5"			-1.05
				LC="6"			-1.08
				LC="7"			-1.11
				LC="8"			-1.13
				LC="9"			-1.16
				LC="10"			-1.18
				LC="11"			-1.21
				LC="12"			-1.24
	LC="13"	-1.26					
	LC="14"	-1.29					
	LC="15"	-1.32					
	VL2	Connect 1MΩ load resistor between V <sub>DD</sub> and VL2 (No panel load)	2•VL1		2•VL1	V	
VL4	Connect 1MΩ load resistor between V <sub>DD</sub> and VL4 (No panel load)	3•VL1		3•VL1	V		
VL5	Connect 1MΩ load resistor between V <sub>DD</sub> and VL5 (No panel load)	4•VL1		4•VL1	V		
				×0.90			
SVD voltage	V <sub>SVD0</sub>	SVC="0"	-2.35	-2.20	-2.05	V	
	V <sub>SVD1</sub>	SVC="1"	-2.70	-2.50	-2.30	V	
	V <sub>SVD2</sub>	SVC="2"	-3.30	-3.10	-2.90	V	
	V <sub>SVD3</sub>	SVC="3"	-4.50	-4.20	-3.90	V	
SVD circuit response time	t <sub>SVD</sub>			100	μS		
Current consumption	I <sub>hlt</sub>	During HALT	No panel load *1	2.5	5.0	μA	
	I <sub>EX1</sub>	During operation at 32kHz		6.5	9.0	μA	
	I <sub>EX2</sub>	During operation at 1MHz	No panel load *2	400	600	μA	
	I <sub>EX3</sub>	During operation at 2MHz	No panel load *3	1,000	1,500	μA	
Current consumption (OSC1•CR oscillation)	I <sub>hlt</sub>	During HALT	No panel load *4	20	70	μA	
	I <sub>EX1</sub>	During operation at f <sub>osc1</sub>		25	80	μA	
	I <sub>EX2</sub>	During operation at 1MHz		420	600	μA	
	I <sub>EX3</sub>	During operation at 2MHz	No panel load *5	1,000	1,500	μA	

\*1: SVD circuit: OFF status, VSC = "0", OSC1: oscillating with crystal, OSCC = "0"

\*2: SVD circuit: OFF status, VSC = "1", OSC1: oscillating with crystal

\*3: SVD circuit: OFF status, VSC = "2", OSC1: oscillating with crystal, V<sub>SS</sub> = -5.0V

\*4: SVD circuit: OFF status, VSC = "0" or "1", OSC1: oscillating with CR, OSCC = "0", R<sub>osc</sub> for OSC1 = 1.6MΩ

\*5: SVD circuit: OFF status, VSC = "2", OSC1: oscillating with CR, OSCC = "0", R<sub>osc</sub> for OSC1 = 1.6MΩ

● Oscillation Characteristics

The oscillation characteristics change depending on the conditions (components used, board pattern, etc.). Use the following characteristics as reference values.

**OSC1 crystal oscillation circuit**

(Unless otherwise specified:  $V_{DD}=0V$ ,  $V_{SS}=-3.0V$ , Crystal: C-002R ( $C_I=35k\Omega$ ),  $C_{Gx}=25pF$ ,  $C_{Dx}=\text{built-in}$ ,  $R_{fX}=10M\Omega$ ,  $V_{SC}="0"$ ,  $T_a=25^\circ C$ )

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start time	$t_{sta}$	$V_{SS}=-2.2$ to $-5.5V$			5	Sec
Built-in capacitance (drain)	$C_D$	Package as assembled		22		pF
		Bare chip		21		pF
Frequency/voltage deviation	$\partial f/\partial V$	$V_{SS}=-2.2$ to $-5.5V$			5	ppm
Frequency/IC deviation	$\partial f/\partial IC$		-10		10	ppm
Frequency adjustment range	$\partial f/\partial C_G$	$C_G=5$ to $25pF$	35	45		ppm
Harmonic oscillation start voltage	$V_{hho}$	$C_G=5pF$			-5.5	V
Permitted leak resistance	$R_{leak}$	Between OSC1 and $V_{DD}$ , $V_{S1}$	200			$M\Omega$

**OSC1 CR oscillation circuit**

(Unless otherwise specified:  $V_{DD}=0V$ ,  $V_{SS}=-3.0V$ ,  $V_{SC}="0"$  or  $"1"$ ,  $T_a=25^\circ C$ )

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start time	$t_{sta}$	$V_{SS}=-2.2$ to $-5.5V$			3	mS
Frequency/voltage deviation	$\partial f/\partial V$	$V_{SS}=-2.2$ to $-5.5V$	-5		5	%
Oscillation frequency	$f_{CR}$	$R_{osc}=1.6M\Omega$	$32\times 70\%$	32	$32\times 130\%$	kHz

**OSC3 CR oscillation circuit (1)**

(Unless otherwise specified:  $V_{DD}=0V$ ,  $V_{SS}=-3.0V$ ,  $V_{SC}="1"$ ,  $T_a=25^\circ C$ )

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start time	$t_{sta}$	$V_{SS}=-2.2$ to $-5.5V$			3	mS
Frequency/voltage deviation	$\partial f/\partial V$	$V_{SS}=-2.2$ to $-5.5V$	-5		5	%
Oscillation frequency	$f_{CR}$	$R_{osc}=40k\Omega$	$860\times 70\%$	860	$860\times 130\%$	kHz

**OSC3 CR oscillation circuit (2)**

(Unless otherwise specified:  $V_{DD}=0V$ ,  $V_{SS}=-5.0V$ ,  $V_{SC}="2"$ ,  $T_a=25^\circ C$ )

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start time	$t_{sta}$	$V_{SS}=-3.5$ to $-5.5V$			3	mS
Frequency/voltage deviation	$\partial f/\partial V$	$V_{SS}=-3.5$ to $-5.5V$	-5		5	%
Oscillation frequency	$f_{CR}$	$R_{osc}=20k\Omega$	$1.7\times 70\%$	1.7	$1.7\times 130\%$	MHz

**OSC3 ceramic oscillation circuit (1)**

(Unless otherwise specified:  $V_{DD}=0V$ ,  $V_{SS}=-3.0V$ ,  $V_{SC}="1"$ , Ceramic: CSB 1000J (Murata Mfg. Co.),  $C_{Gc}=C_{Dc}=100pF$ ,  $R_{fC}=1M\Omega$ ,  $T_a=25^\circ C$ )

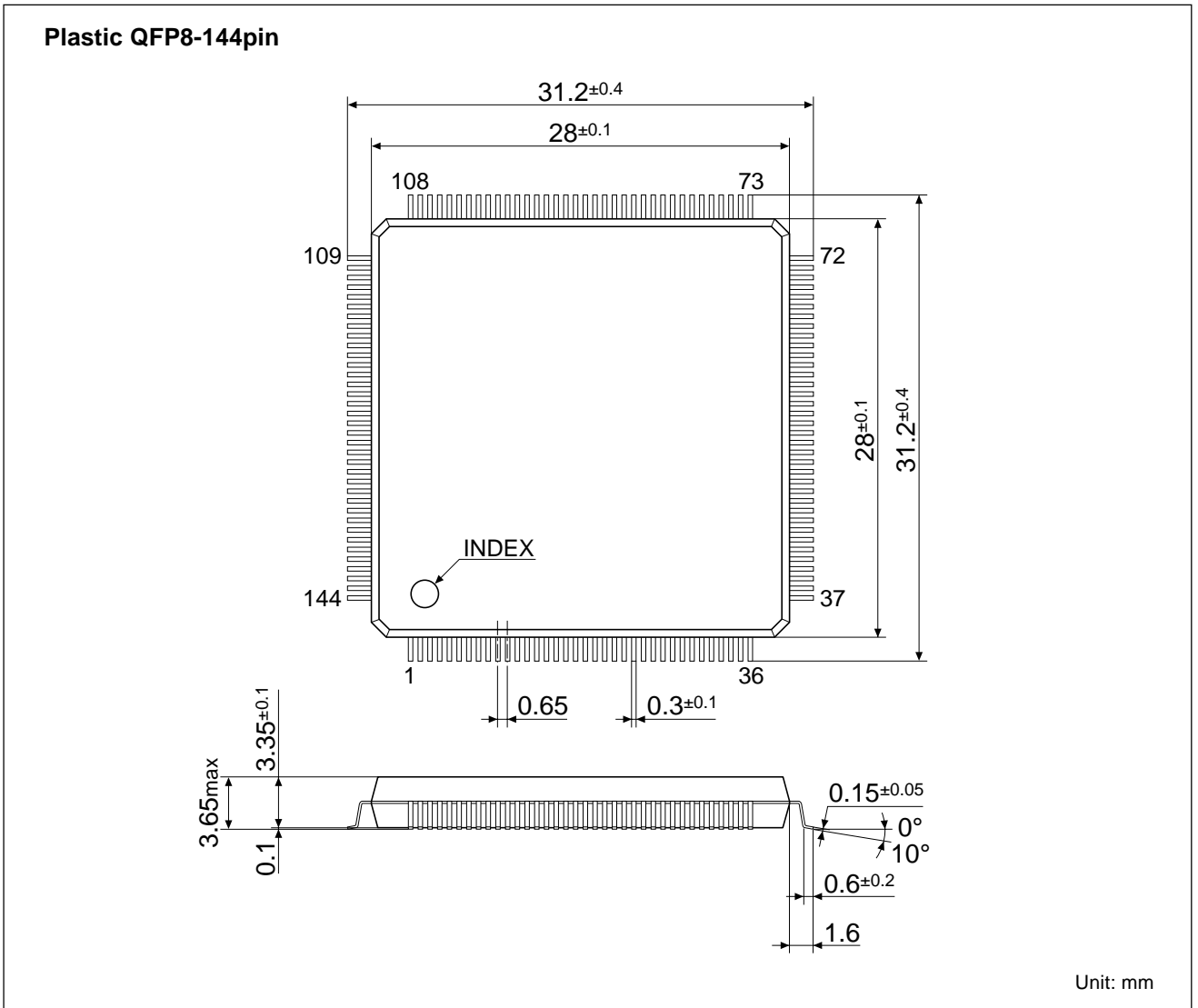
Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start time	$t_{sta}$	$V_{SS}=-2.2$ to $-5.5V$			3	mS
Frequency/voltage deviation	$\partial f/\partial V$	$V_{SS}=-2.2$ to $-5.5V$	-3		3	%

**OSC3 ceramic oscillation circuit (2)**

(Unless otherwise specified:  $V_{DD}=0V$ ,  $V_{SS}=-5.0V$ ,  $V_{SC}="2"$ , Ceramic: CSA 2.00MG (Murata Mfg. Co.),  $C_{Gc}=C_{Dc}=100pF$ ,  $R_{fC}=1M\Omega$ ,  $T_a=25^\circ C$ )

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start time	$t_{sta}$	$V_{SS}=-3.5$ to $-5.5V$			3	mS
Frequency/voltage deviation	$\partial f/\partial V$	$V_{SS}=-3.5$ to $-5.5V$	-3		3	%

■ PACKAGE DIMENSIONS



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