EPSON

E0C6262

4-bit Single Chip Microcomputer

Wide Voltage Operation Products

- Core CPU
- 3 ⇔ 5V Level Shifter
- SVD Circuit
- Serial Interface

■ DESCRIPTION

The E0C6262 is a CMOS 4-bit microcomputer with 4-bit core CPU (E0C6200A), ROM, RAM, time base counter, serial interface, supply voltage detection (SVD) circuit and a programmable timer/event counter.
The E0C6262 features low power dissipation and is ideal for battery-powered equipment.

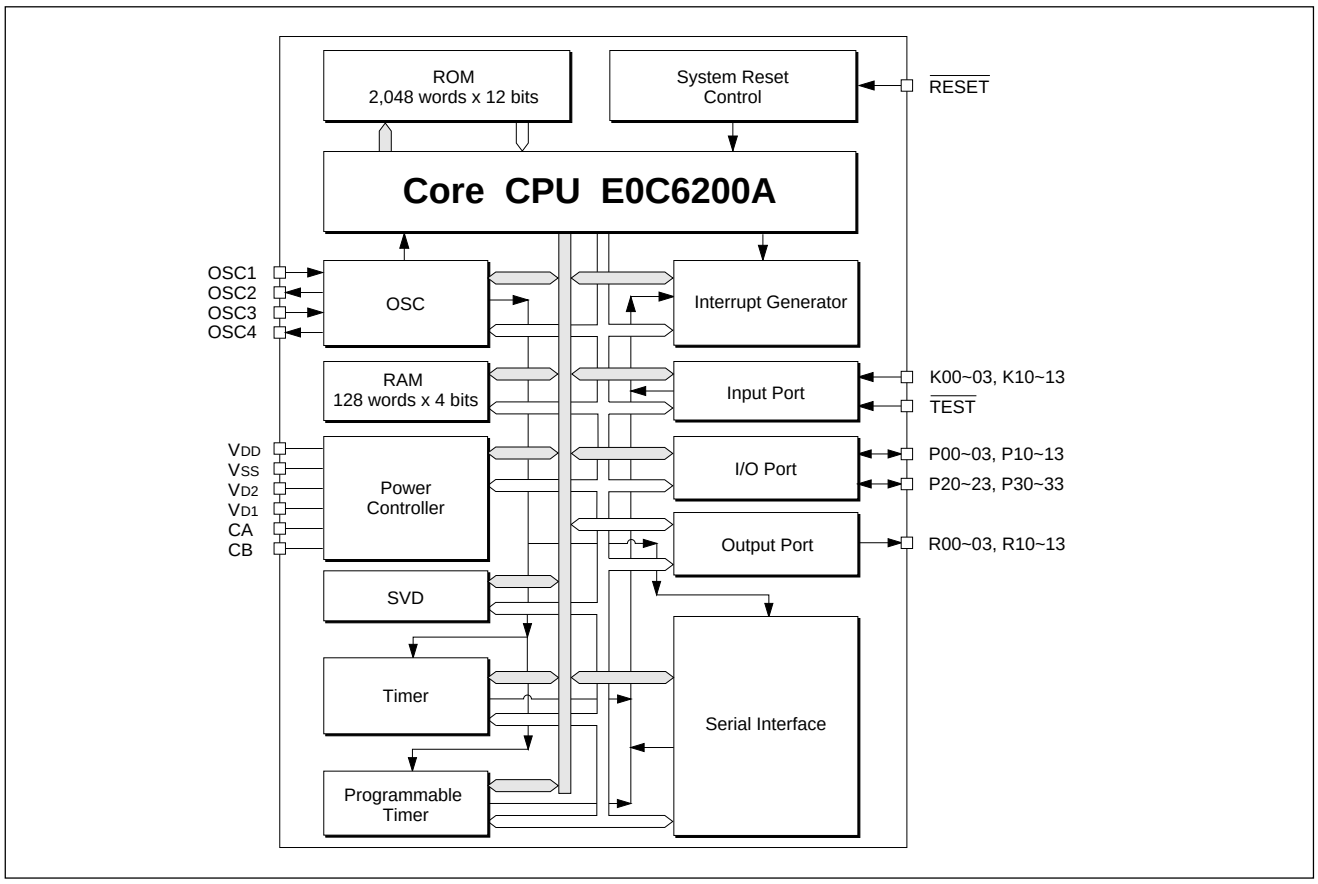
■ FEATURES

- CMOS LSI 4-bit parallel processing
- Clock ..... 32.768kHz (Typ.) and 1MHz (Typ.) (software selectable)
- Instruction set ..... 100 instructions
- Instruction execution time ..... 153µsec, 214µsec or 366µsec at 32kHz (depending on instruction)
  5µsec, 7µsec or 12µsec at 1MHz (depending on instruction)
- ROM capacity ..... 2,048 × 12 bits
- RAM capacity ..... 128 × 4 bits
- Input port ..... 8 bits (pull-up resistors are available by mask option)
- Output port ..... 8 bits (clock/alarm output is available by mask option)
- I/O port ..... 16 bits (serial I/O is available by mask option)
- Synchronized serial I/O port ..... 1 port (optional)
- Clock timer
- Watchdog timer
- Programmable timer
- Event counter ..... 8 bits
- 5V level-shifter interface
- Supply voltage detection (SVD) circuit .. Two-level detection
  1.1V to 1.2V ± 50mV, 2.2V to 2.4V ± 100mV
- Interrupts ..... External : Input interrupt 2 lines
  Internal : Timer interrupt 2 lines
  Serial I/O interrupt 1 line
- Oscillator startup voltage ..... 0.9V minimum (OSC1)
- Current consumption ..... E0C62L62 HALT mode (32kHz) : 2.0µA
  OPERATING mode (32kHz) : 5.0µA
  E0C6262 HALT mode (32kHz) : 3.0µA
  OPERATING mode (32kHz) : 7.0µA
  E0C62A62 OPERATING mode (1MHz) : 300µA
- Package ..... QFP6-44pin (plastic), QFP12-48pin (plastic)
  Die form

■ LINE UP

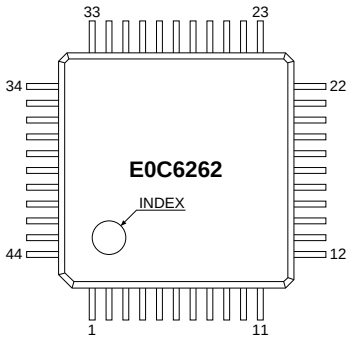
Model	Supply voltage	Clock
E0C62L62	1.5V (0.8V to 2.2V)	32kHz (Crystal oscillation)
E0C6262	3.0V (2.2V to 5.0V)	32kHz (Crystal oscillation)
E0C62A62	3.0V (2.2V to 5.0V)	32kHz (Crystal oscillation) & 1MHz (Ceramic or CR oscillation)

■ BLOCK DIAGRAM



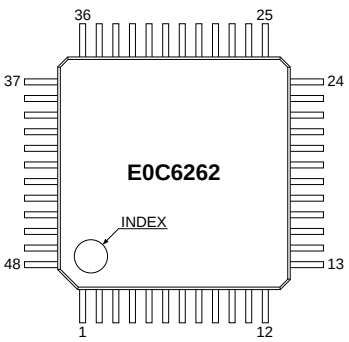
■ PIN CONFIGURATION

QFP6-44pin



No.	Pin name	No.	Pin name	No.	Pin name	No.	Pin name
1	P10	12	R13	23	V_{D2}	34	K01
2	P11	13	P20	24	OSC4	35	K02
3	P12	14	P21	25	OSC3	36	K03
4	P13	15	P22	26	V_{D1}	37	R00
5	K10	16	P23	27	OSC2	38	R01
6	K11	17	P30	28	OSC1	39	R02
7	K12	18	P31	29	V_{DD}	40	R03
8	K13	19	P32	30	V_{SS}	41	P00
9	R10	20	P33	31	$\overline{TEST}$	42	P01
10	R11	21	CA	32	$\overline{RESET}$	43	P02
11	R12	22	CB	33	K00	44	P03

QFP12-48pin



No.	Pin name	No.	Pin name	No.	Pin name	No.	Pin name
1	K01	13	P10	25	R13	37	V_{D2}
2	K02	14	P11	26	P20	38	OSC4
3	K03	15	P12	27	P21	39	OSC3
4	R00	16	P13	28	P22	40	V_{D1}
5	R01	17	K10	29	P23	41	OSC2
6	R02	18	K11	30	P30	42	OSC1
7	N.C.	19	N.C.	31	N.C.	43	V_{DD}
8	R03	20	K12	32	P31	44	V_{SS}
9	P00	21	K13	33	P32	45	N.C.
10	P01	22	R10	34	P33	46	$\overline{TEST}$
11	P02	23	R11	35	CA	47	$\overline{RESET}$
12	P03	24	R12	36	CB	48	K00

N.C. = No Connection

■ PIN DESCRIPTION

Pin name	Pin No.		In/Out	Function
	QFP6-44pin	QFP12-48pin		
V_{DD}	29	43	I	Power source (+) terminal
V_{SS}	30	44	I	Power source (-) terminal
V_{D1}	26	40	–	Oscillation and internal logic system regulated voltage
V_{D2}	23	37	–	Oscillation and internal logic system boosted voltage (At 6262/62A62 this is connected to V_{DD})
CA, CB	21, 22	35, 36	–	Booster capacitor connecting terminal (At 6262/62A62 this is connected to V_{DD})
OSC1	28	42	I	Crystal oscillation input terminal
OSC2	27	41	O	Crystal oscillation output terminal
OSC3	25	39	I	Ceramic or CR oscillation input terminal (selected by mask option, 62A62 only)
OSC4	24	38	O	Ceramic or CR oscillation output terminal (selected by mask option, 62A62 only)
K00–K03	33–36	48, 1–3	I	Input terminal
K10–K13	5–8	17, 18, 20, 21	I	
P00–P03	41–44	9–12	I/O	I/O terminal
P10–P13	1–4	13–16	I/O	
P20–P23	13–16	26–29	I/O	
P30–P33	17–20	30, 32–34	I/O	I/O terminal (Serial I/O function is selected by mask option)
R00–R03	37–40	4–6, 8	O	Output terminal
R10–R13	9–12	22–25	O	Output terminal (DC, buzzer, clock and $\overline{SRDY}$ output may be selected by mask option)
$\overline{RESET}$	32	47	I	Initial reset input terminal
$\overline{TEST}$	31	46	I	Test input terminal

■ ELECTRICAL CHARACTERISTICS

● Absolute Maximum Ratings

E0C6262/62A62

(V_{SS}=0V)

Rating	Symbol	Value	Unit
Supply voltage	V_{DD}	-0.5 to 5.5	V
Input voltage (1)	V_I	-0.5 to V_{DD} + 0.3	V
Input voltage (2)	V_{IOSC}	-0.5 to V_{D1} + 0.3	V
Permissible total output current *1	ΣI_{VDD}	5	mA
Operating temperature	Topr	-20 to 70	°C
Storage temperature	Tstg	-65 to 150	°C
Soldering temperature / Time	Tsol	260°C, 10sec (lead section)	–
Permissible dissipation *2	P_D	250	mW

∗1: The permissible total output current is the sum total of the current (average current) that simultaneously flows from the output pins (or is draw in).
∗2: In case of plastic package (QFP6-44pin, QFP12-48pin).

E0C62L62

(V_{SS}=0V)

Rating	Symbol	Value	Unit
Supply voltage	V_{DD}	-0.5 to 2.5	V
Input voltage (1)	V_I	-0.5 to V_{DD} + 0.3	V
Input voltage (2)	V_{IOSC}	-0.5 to V_{D1} + 0.3	V
Permissible total output current *1	ΣI_{VDD}	5	mA
Operating temperature	Topr	-20 to 70	°C
Storage temperature	Tstg	-65 to 150	°C
Soldering temperature / Time	Tsol	260°C, 10sec (lead section)	–
Permissible dissipation *2	P_D	250	mW

∗1: The permissible total output current is the sum total of the current (average current) that simultaneously flows from the output pins (or is draw in).
∗2: In case of plastic package (QFP6-44pin, QFP12-48pin).

● Recommended Operating Conditions

E0C6262

(Ta=-20 to 70°C)

Condition	Symbol	Remark	Min.	Typ.	Max.	Unit
Supply voltage	V_{DD}	V_{SS}=0V	2.2	3.0	5.0	V
Oscillation frequency	f_{OSC1}		–	32.768	–	kHz

E0C62L62

(Ta=-20 to 70°C)

Condition	Symbol	Remark	Min.	Typ.	Max.	Unit
Supply voltage	V_{DD}	V_{SS}=0V, Normal mode	1.1	1.5	2.2	V
		V_{SS}=0V, Heavy load protection mode	0.8	1.5	2.2	V
Oscillation frequency	f_{OSC1}		–	32.768	–	kHz

E0C62A62

(Ta=-20 to 70°C)

Condition	Symbol	Remark	Min.	Typ.	Max.	Unit
Supply voltage	V_{DD}	V_{SS}=0V	2.2	3.0	5.0	V
Oscillation frequency (1)	f_{OSC1}		–	32.768	–	kHz
Oscillation frequency (2)	f_{OSC3}	duty 50±5%	–	1,000	–	kHz

● DC Characteristics

E0C6262/62A62

(Unless otherwise specified:
V_{DD}=3.0V, V_{SS}=0V, f_{OSC1}=32.768kHz, f_{OSC3}=1MHz(E0C62A62), Ta=-20 to 70°C, C1–C3=0.1µF, V_{DE}=1.5 to 5.0V, V_{D1} is internal voltage)
(V_{DD} (V) used in the table means voltage supplied by V_{DD} or V_{DE}, use of V_{DD} or V_{DE} for Pads as positive power supply is selected by mask option)

Characteristic	Symbol	Condition		V_{DD} (V)	Min.	Typ.	Max.	Unit
High level input voltage (1)	V_{IH1}		K00–03•10–13, P00–03 P10–13•20–23•30–33	1.5 3.0 5.0	0.8•V_{DD}		V_{DD}	V
High level input voltage (2)	V_{IH2}		$\overline{RESET}$, $\overline{TEST}$	↑	0.9•V_{DD}		V_{DD}	V
Low level input voltage (1)	V_{IL1}		K00–03•10–13, P00–03 P10–13•20–23•30–33	↑	0		0.2•V_{DD}	V
Low level input voltage (2)	V_{IL2}		$\overline{RESET}$, $\overline{TEST}$	↑	0		0.1•V_{DD}	V
High level input current	I_{IH}	V_{IH}=V_{DD}	K00–03•10–13, P00–03 P10–13•20–23•30–33 $\overline{RESET}$, $\overline{TEST}$	↑	0		0.5	µA
Low level input current (1)	I_{IL1}	V_{IL1}=0V No pull-up resistor	K00–03•10–13, P00–03 P10–13•20–23•30–33 $\overline{RESET}$	↑	-0.5		0	µA
Low level input current (2)	I_{IL2}	V_{IL2}=0V With pull-up resistor	K00–03•10–13 $\overline{RESET}$, $\overline{TEST}$	1.5 3.0 5.0	-10 -20 -32		-6 -12 -18	µA
Low level input current (3)	I_{IL3}	V_{IL3}=0V With pull-up resistor (small)	P00–03•10–13 P20–23•30–33	1.5 3.0 5.0	-45 -85 -130		-25 -45 -70	µA
Low level input current (4)	I_{IL4}	V_{IL4}=0V With pull-up resistor (large)	P00–03•10–13 P20–23•30–33	1.5 3.0 5.0	-15 -30 -45		-8 -16 -25	µA
High level output current (1)	I_{OH1}	V_{OH1}=-0.9•V_{DD}	R00–03•10•11 P00–03•10–13 P20–23•30–33	1.5 3.0 5.0			-50 -0.3 -1.0	µA mA
High level output current (2)	I_{OH2}	V_{OH2}=-0.9•V_{DD}	R12•13	1.5 3.0 5.0			-100 -0.6 -2.0	µA mA
Low level output current (1)	I_{OL1}	V_{OL1}=-0.1•V_{DD}	R00–03•10•11 P00–03•10–13 P20–23•30–33	1.5 3.0 5.0	150 1.0 3.0			µA mA
Low level output current (2)	I_{OL2}	V_{OL2}=-0.1•V_{DD}	R12•13	1.5 3.0 5.0	200 1.5 4.5			µA mA

E0C62L62

(Unless otherwise specified: V_{DD}=1.5V, V_{SS}=0V, f_{OSC1}=32.768kHz, Ta=-20 to 70°C, C1–C3=0.1µF, V_{DE}=1.5 to 5.0V, V_{D1} is internal voltage)
(V_{DD} (V) used in the table means voltage supplied by V_{DD} or V_{DE}, use of V_{DD} or V_{DE} for Pads as positive power supply is selected by mask option)

Characteristic	Symbol	Condition		V_{DD} (V)	Min.	Typ.	Max.	Unit
High level input voltage (1)	V_{IH1}		K00–03•10–13, P00–03 P10–13•20–23•30–33	0.8 1.5 3.0 5.0	0.8•V_{DD}		V_{DD}	V
High level input voltage (2)	V_{IH2}		$\overline{RESET}$, $\overline{TEST}$	↑	0.9•V_{DD}		V_{DD}	V
Low level input voltage (1)	V_{IL1}		K00–03•10–13, P00–03 P10–13•20–23•30–33	↑	0		0.2•V_{DD}	V
Low level input voltage (2)	V_{IL2}		$\overline{RESET}$, $\overline{TEST}$	↑	0		0.1•V_{DD}	V
High level input current	I_{IH}	V_{IH}=V_{DD}	K00–03•10–13, P00–03 P10–13•20–23•30–33 $\overline{RESET}$, $\overline{TEST}$	↑	0		0.5	µA
Low level input current (1)	I_{IL1}	V_{IL1}=0V No pull-up resistor	K00–03•10–13, P00–03 P10–13•20–23•30–33 $\overline{RESET}$	↑	-0.5		0	µA
Low level input current (2)	I_{IL2}	V_{IL2}=0V With pull-up resistor	K00–03•10–13 $\overline{RESET}$, $\overline{TEST}$	0.8	-6		-3	µA
				1.5	-10		-6	
				3.0	-20		-12	
				5.0	-32		-18	
Low level input current (3)	I_{IL3}	V_{IL3}=0V With pull-up resistor	P00–03•10–13 P20–23•30–33	0.8	-10		-5	µA
				1.5	-15		-8	
				3.0	-30		-16	
				5.0	-45		-25	
High level output current (1)	I_{OH1}	V_{OH1}=-0.9•V_{DD}	R00–03•10•11 P00–03•10–13 P20–23•30–33	0.8			-5	µA
				1.5			-150	
				3.0			-1.0	mA
				5.0			-3.0	
High level output current (2)	I_{OH2}	V_{OH2}=-0.9•V_{DD}	R12•13	0.8			-10	µA
				1.5			-300	
				3.0			-2.0	mA
				5.0			-4.0	
Low level output current (1)	I_{OL1}	V_{OL1}=-0.1•V_{DD}	R00–03•10•11 P00–03•10–13 P20–23•30–33	0.8	20			µA
				1.5	500			
				3.0	3.0			mA
				5.0	9.0			
Low level output current (2)	I_{OL2}	V_{OL2}=-0.1•V_{DD}	R12•13	0.8	30			µA
				1.5	750			
				3.0	4.5			mA
				5.0	13.5			

● Analog Circuit Characteristics and Current Consumption

E0C6262

(Unless otherwise specified: V_{DD}=3.0V, V_{SS}=0V, f_{OSC1}=32.768kHz, Ta=25°C, C_G=25pF, V_{D1} is internal voltage, C1=0.1µF)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
SVD voltage	V_{SVD}	Level 1	2.10	2.20	2.30	V
		Level 2	2.30	2.40	2.50	V
SVD circuit response time	t_{SVD}				100	µS
Current consumption	I_{OP}	During HALT *1		3.0	5.0	µA
		During operation *1		7.0	10.0	µA

*1: The SVD circuit is turned off.

E0C62L62

(Unless otherwise specified: V_{DD}=1.5V, V_{SS}=0V, f_{OSC1}=32.768kHz, Ta=25°C, C_G=25pF, V_{D1} and V_{D2} are internal voltage, C1–C3=0.1µF)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
SVD voltage	V_{SVD}	Level 1	1.05	1.10	1.15	V
		Level 2	1.15	1.20	1.25	V
SVD circuit response time	t_{SVD}				100	µS
Current consumption	I_{OP}	During HALT *1		2.0	4.0	µA
		During operation *1		5.0	7.5	µA

*1: The SVD circuit is turned off.

E0C62A62

(Unless otherwise specified: V_{DD}=3.0V, V_{SS}=0V, f_{OSC1}=32.768kHz, Ta=25°C, C_G=25pF, V_{D1} is internal voltage, C1=0.1µF)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
SVD voltage	V_{SVD}	Level 1	2.10	2.20	2.30	V
		Level 2	2.30	2.40	2.50	V
SVD circuit response time	t_{SVD}				100	µS
Current consumption	I_{OP}	During HALT *1		3.0	5.0	µA
		During operation at 32kHz *1		7.0	10.0	µA
		During operation at 1MHz *1		300	450	µA

*1: The SVD circuit is turned off.

● Oscillation Characteristics

The oscillation characteristics change depending on the conditions (components used, board pattern, etc.). Use the following characteristics as reference values.

E0C6262/62A62 (Crystal oscillation circuit)

(Unless otherwise specified: V_{DD}=3.0V, V_{SS}=0V, Crystal: C-002R (C_I=35kΩ), C_G=25pF, C_D=built-in, Ta=25°C)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start voltage	Vsta	tsta≤3sec (V_{DD})	2.2			V
Oscillation stop voltage	Vstp	tstp≤10sec (V_{DD})	2.2			V
Built-in capacitance (drain)	C_D	Including the parasitic capacity inside the IC		20		pF
Frequency/voltage deviation	∂f/∂V	V_{DD}=2.2 to 5.0V			5	ppm
Frequency/IC deviation	∂f/∂IC		-10		10	ppm
Frequency adjustment range	∂f/∂C_G	C_G=5 to 25pF	35	45		ppm
Harmonic oscillation start voltage	V_{hho}	(V_{DD})	5.0			V
Permitted leak resistance	R_{leak}	Between OSC1 and V_{DD}, V_{SS}	200			MΩ

E0C62L62 (Crystal oscillation circuit)

(Unless otherwise specified: V_{DD}=1.5V, V_{SS}=0V, Crystal: C-002R (C_I=35kΩ), C_G=25pF, C_D=built-in, Ta=25°C)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start voltage	Vsta	tsta≤3sec (V_{DD})	0.9			V
Oscillation stop voltage	Vstp	tstp≤10sec (V_{DD})	0.8			V
Built-in capacitance (drain)	C_D	Including the parasitic capacity inside the IC		20		pF
Frequency/voltage deviation	∂f/∂V	V_{DD}=0.9 to 2.2V			5	ppm
Frequency/IC deviation	∂f/∂IC		-10		10	ppm
Frequency adjustment range	∂f/∂C_G	C_G=5 to 25pF	35	45		ppm
Harmonic oscillation start voltage	V_{hho}	(V_{DD})	2.2			V
Permitted leak resistance	R_{leak}	Between OSC1 and V_{DD}, V_{SS}	200			MΩ

E0C62A62 (CR oscillation circuit)

(Unless otherwise specified: V_{DD}=3.0V, V_{SS}=0V, R_{CR}=35kΩ, Ta=25°C)

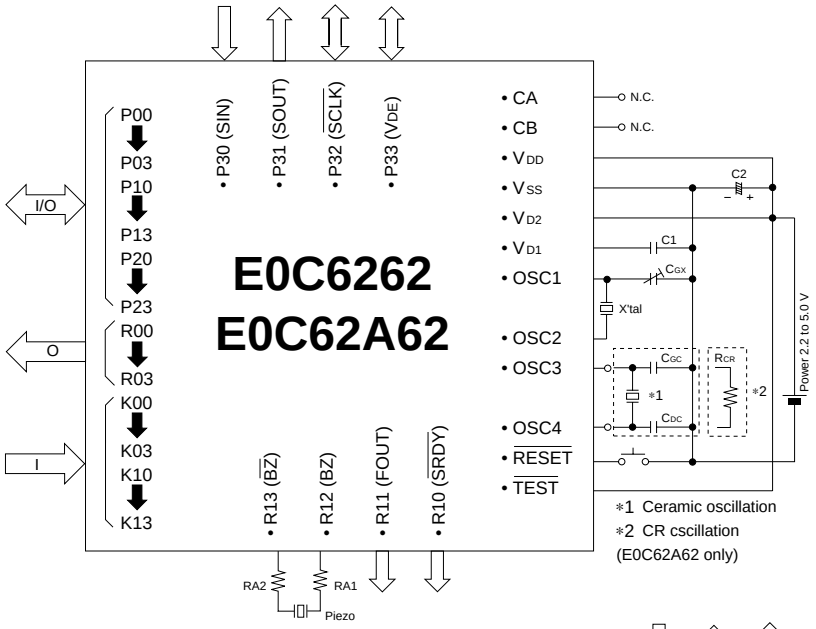
Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation frequency dispersion	f_{OSC3}		-30	1000kHz	30	%
Oscillation start voltage	Vsta	(V_{DD})	2.2			V
Oscillation start time	tsta	V_{DD}=2.2 to 5.0V			3	mS
Oscillation stop voltage	Vstp	(V_{DD})	2.2			V

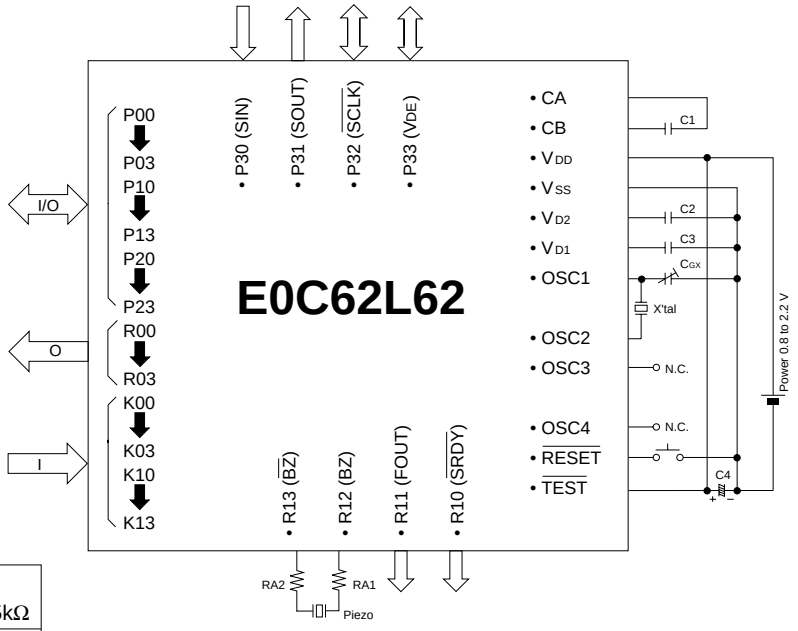
E0C62A62 (Ceramic oscillation circuit)

(Unless otherwise specified: V_{DD}=3.0V, V_{SS}=0V, Ceramic oscillation: 1MHz, C_{GC}=C_{DC}=100pF, Ta=25°C)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start voltage	Vsta	(V_{DD})	2.2			V
Oscillation start time	tsta	V_{DD}=2.2 to 5.0V			5	mS
Oscillation stop voltage	Vstp	(V_{DD})	2.2			V

■ BASIC EXTERNAL CONNECTION DIAGRAM



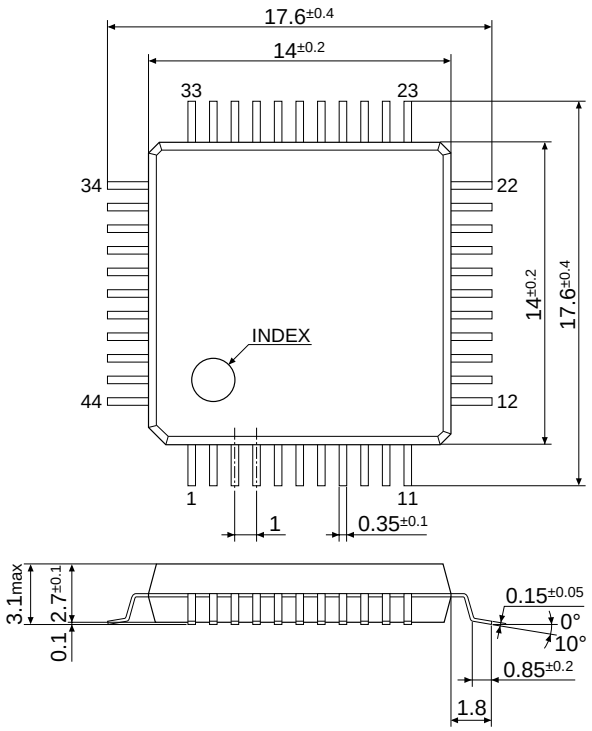


X'tal	Crystal oscillator	32.768kHz, CI(Max.)=35kΩ
CGX	Trimmer capacitor	5~25pF
CR	Ceramic oscillator	500kHz~1MHz
CGC	Gate capacitance	100pF
CDC	Drain capacitance	100pF
RCR	Resistance for CR oscillation	35kΩ
C1		0.1µF
C2		3.3µF
RA1, RA2		100Ω

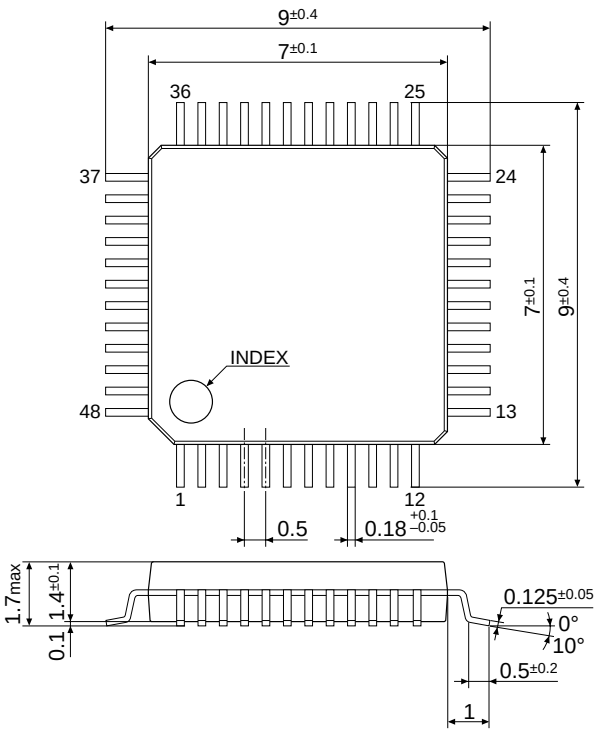
Note: The above table is simply an example, and is not guaranteed to work.

■ PACKAGE DIMENSIONS

Plastic QFP6-44pin



Plastic QFP12-48pin



Unit: mm

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ENERGY SAVING EPSON