

4-bit Single Chip Microcomputer



- Core CPU Architecture
- 38.4kHz/500kHz Twin Clock Operation
- Built-in, 2-ch. Serial Ports
- SVD Circuit/2-ch. Analog Comparators

■ DESCRIPTION

The E0C6266 is an advanced single-chip CMOS 4-bit microcomputer consisting of the E0C6200 CMOS 4-bit core CPU. It also contains the ROM, RAM, 2-channel timer, event counter, start-stop serial ports, clock sync serial ports and 40 I/O ports.

The E0C6266 provides an excellent solution for low-power consumption systems with clock functions.

■ FEATURES

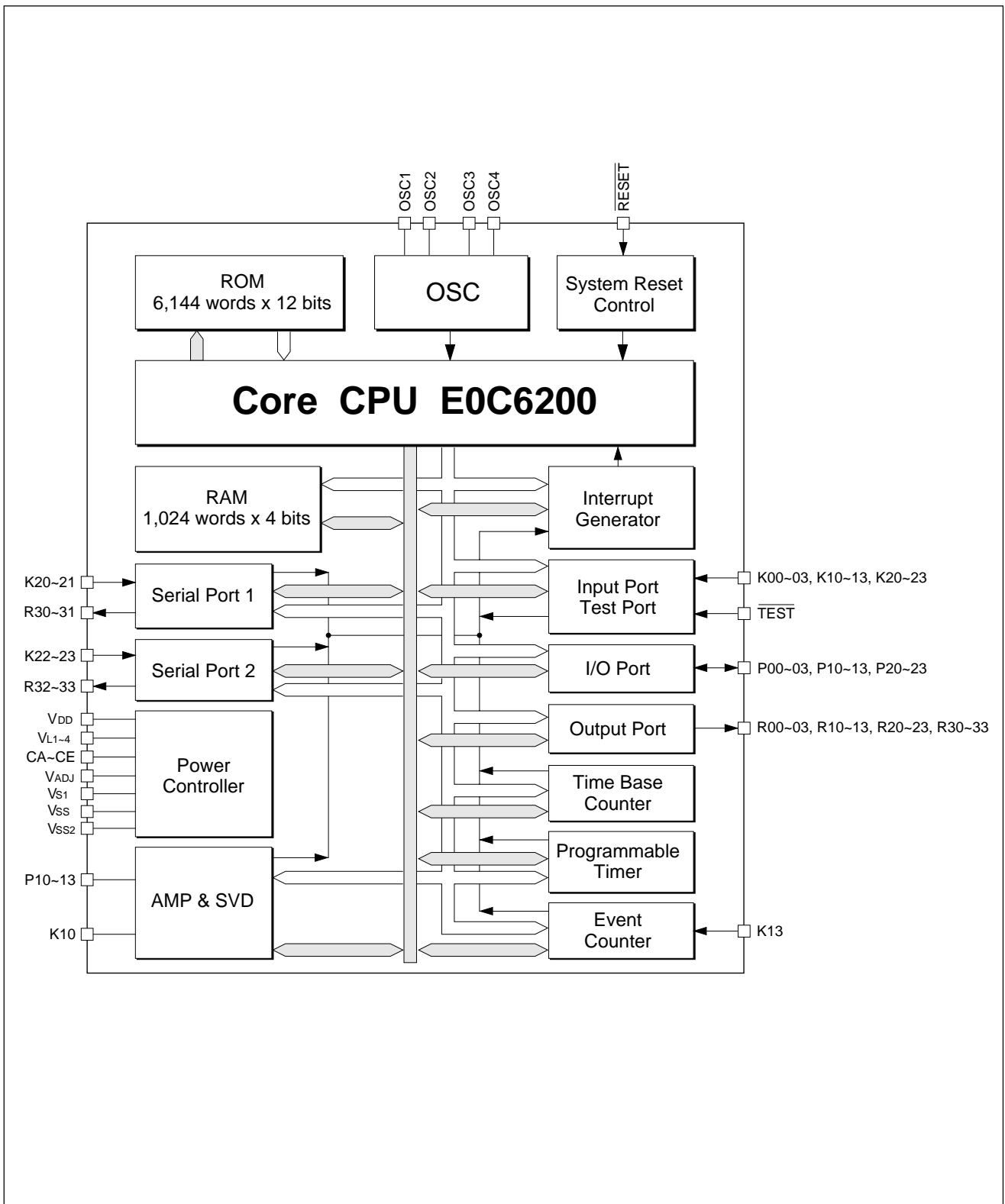
- CMOS LSI 4-bit parallel processing
- Clock 38.4kHz (Typ.)/500kHz (Max.) (selectable by software)
- Instruction set 108 instructions
- Instruction cycle time 130μsec, 182μsec or 312μsec at 38kHz
(depending on instruction)
10μsec, 14μsec or 24μsec at 500kHz
(depending on instruction)
- ROM capacity 6,144 × 12 bits
- RAM capacity 1,024 × 4 bits
- Input port 12 bits
- Output port 16 bits
- I/O port 12 bits
- Serial I/O port 2 ports
 - Async; half-duplex, start-stop; transmission speed at 200, 300, 600, 1200, 2400 or 4800 bps; 6 to 8-bit data length; built-in error detect circuit and built-in send/receive buffer register.
 - Clock sync.; operating by external clock; start-stop can be set by mask option.
- Built-in time base counter, programmable timer, event counter, and watchdog timer
- Built-in SVD circuit, 2 channels (internal voltage detection)
- Built-in comparator, 2 channels
- Built-in LCD drive power supply, double boosting, external adjustment of output voltage
- Interrupts

External :	Input interrupt	3 lines
Internal :	Timer interrupt	2 lines (4ch.)
	Comparator interrupt	2 lines
	Event counter interrupt	1 line
	Serial I/O interrupt	2 lines
- Supply voltage 2.2V to 5.5V
- Current consumption

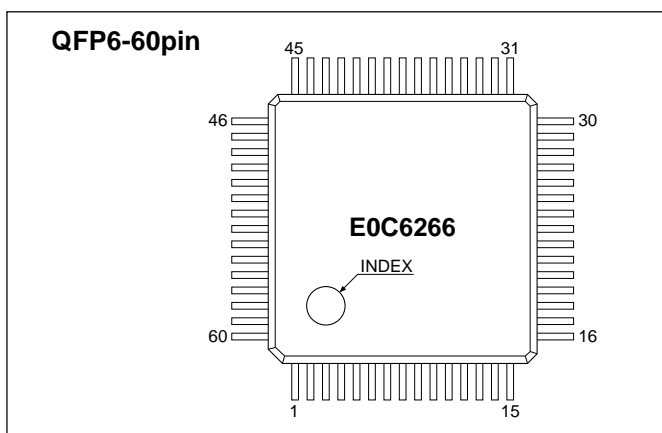
HALT mode (38.4kHz)	:	1.8μA (Typ.)
OPERATING mode (500kHz)	:	110μA (Typ.)/150μA (Max.)
- Package QFP6-60pin (plastic)
Die form

E0C6266

■ BLOCK DIAGRAM



PIN CONFIGURATION



No.	Pin name	No.	Pin name	No.	Pin name	No.	Pin name
1	P13	16	VSS2	31	K20	46	VL1
2	P20	17	R22	32	K21	47	VDD
3	P21	18	R23	33	K22	48	OSC1
4	P22	19	R30	34	K23	49	OSC2
5	P23	20	R31	35	RESET	50	Vs1
6	R00	21	R32	36	TEST	51	OSC3
7	R01	22	R33	37	CE	52	OSC4
8	R02	23	K00	38	CD	53	VSS
9	R03	24	K01	39	CC	54	P00
10	R10	25	K02	40	CB	55	P01
11	R11	26	K03	41	CA	56	P02
12	R12	27	K10	42	VL4	57	P03
13	R13	28	K11	43	VL3	58	P10
14	R20	29	K12	44	VL2	59	P11
15	R21	30	K13	45	VADJ	60	P12

PIN DESCRIPTION

Pin name	Pin No.	In/Out	Function
VDD	47	I	Power source (+) terminal
VSS	53	I	Power source (-) terminal ...analog power source
VSS2	16	I	Power source (-) terminal ...power source for output ports (R20–R23)
Vs1	50	–	Power source for oscillation circuit
VL1	46	–	Reduction power source for LCD
VL2	44	–	Power source for LCD
VL3	43	–	Booster power source for LCD
VL4	42	–	Booster power source for LCD
VADJ	45	I	Input terminal for setting VL
CA–CE	41–37	–	Booster/reduction capacitor connecting terminals for LCD
OSC1	48	I	Crystal oscillation input terminal
OSC2	49	O	Crystal oscillation output terminal
OSC3	51	I	Ceramic oscillation input terminal
OSC4	52	O	Ceramic oscillation output terminal
RESET	35	I	Initial reset input terminal
K00–K03	23–26	I	Input terminal
K10/VBLD	27	I	Input terminal (Input terminal for setting SVD detection voltage)
K11–K12	28–29	I	Input terminal
K13/EVN	30	I	Input terminal (Event counter input terminal)
K20/SI1A	31	I	Input terminal (Serial port 1 data input terminal)
K21/SI1B	32	I	Input terminal (Serial port 1 data input terminal)
K22/SI2	33	I	Input terminal (Serial port 2 data input terminal)
K23/SCLK	34	I	Input terminal (Serial port 2 clock input terminal)
P00–P03	54–57	I/O	I/O terminal
P10/CMPP1	58	I/O	I/O terminal (Comparator 1 non-inverted input terminal)
P11/CMPP1	59	I/O	I/O terminal (Comparator 1 inverted input terminal)
P12/CMPP2	60	I/O	I/O terminal (Comparator 2 non-inverted input terminal)
P13/CMPP2	1	I/O	I/O terminal (Comparator 2 inverted input terminal)
P20–P23	2–5	I/O	I/O terminal
R00–R03	6–9	O	Output terminal
R10, R11	10, 11	O	Output terminal
R12/FOUT	12	O	Output terminal (FOUT or BZ output terminal)
R13/BZ	13	O	Output terminal (BZ or OSC3 clock output terminal)
R20–R23	14, 15, 17, 18	O	Output terminal (10 mA output available)
R30/SO1A	19	O	Output terminal (Serial port 1 data output terminal)
R31/SO1B	20	O	Output terminal (Serial port 1 data output terminal)
R32/SO2	21	O	Output terminal (Serial port 2 data output terminal)
R33/SRDY	22	O	Output terminal (Serial port 2 status output terminal)
TEST	36	I	Test input terminal

■ ELECTRICAL CHARACTERISTICS

● Absolute Maximum Ratings

(V_{DD}=0V)

Rating	Symbol	Value	Unit
Supply voltage (1)	V _{SS}	-7.0 to 0.5	V
Supply voltage (2)	V _{SS2}	-7.0 to V _{SS}	V
Supply voltage (3)	V _{L1} -V _{L4}	-7.0 to 0.5	V
Input voltage (1)	V _I	V _{SS} - 0.3 to 0.3	V
Input voltage (2) *1	V _{OSC}	-2.0 to 0.3	V
Permissible total output current (1)*2	ΣI _{VSS}	15	mA
Permissible total output current (2)*2	ΣI _{VSS2}	40	mA
Operating temperature	T _{opr}	-20 to 70	°C
Storage temperature	T _{stg}	-65 to 150	°C
Soldering temperature / Time	T _{sol}	260°C, 10sec (lead section)	-
Permissible dissipation *3	P _d	250	mW

*1: OSC1, OSC2 pin

*2: The permissible total output current is the sum total of the current (average current) that simultaneously flows from the output pins (or is draw in).

*3: In case of plastic package (QFP6-60pin).

● Recommended Operating Conditions

(T_a=-20 to 70°C)

Condition	Symbol	Remark	Min.	Typ.	Max.	Unit
Supply voltage (1)	V _{SS}	V _{DD} =0V	-5.5		-2.2	V
Supply voltage (2) *1	V _{SS2}	V _{DD} =0V	-5.5		V _{SS}	V
Oscillation frequency (1)	f _{OSC1}		-	38.400	-	kHz
Oscillation frequency (2) *2	f _{OSC3}	duty: 50±5%	50		500	kHz
Capacitor between V _{DD} and V _{S1}	C _{S1}		0.1			μF
Capacitor between V _{DD} and V _{L1} *3	C _{L1}		0.1			μF
Capacitor between V _{DD} and V _{L2} *3	C _{L2}		0.1			μF
Capacitor between V _{DD} and V _{L3} *3	C _{L3}		0.1			μF
Capacitor between V _{DD} and V _{L4} *3	C _{L4}		0.1			μF
Capacitor between CA and CB *3	C ₁		0.1			μF
Capacitor between CA and CC *3	C ₂		0.1			μF
Capacitor between CD and CE *3	C ₃		0.1			μF

*1: When selecting not to use V_{SS2} power by option, you can release the V_{SS2} terminal.

*2: When selecting not to use OSC3 oscillation circuit by option, you can release the OSC3 terminal.

*3: When selecting not to use LCD drive power by option, you can release the above capacitors are not required. However, you should connect V_{L1}-V_{L4} terminals with the V_{DD} and release the CA-CE and V_{ADJ} terminals.

● DC Characteristics

(Unless otherwise specified: V_{DD}=0V, V_{SS}(V_{SS2})=-2.2 to -5.5V, T_a=25°C)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
High level input voltage (1)	V _{IH1}	K00-03•10-13•20-23 P00-03•10-13•20-23	0.2•V _{SS}		0	V
High level input voltage (2)	V _{IH2}	RESET	0.1•V _{SS}		0	V
Low level input voltage (1)	V _{IL1}	K00-03•10-13•20-23 P00-03•10-13•20-23	V _{SS}		0.8•V _{SS}	V
Low level input voltage (2)	V _{IL2}	RESET	V _{SS}		0.9•V _{SS}	V
High level input current	I _{IH}	V _{IH} =V _{DD} K00-03•10-13•20-23 P00-03•10-13•20-23 RESET, TEST			0.5	μA
Low level input current (1)	I _{IL1}	V _{IL1} =V _{SS} No pull up resistor K00-03•10-13•20-23 P00-03•10-13•20-23	-0.5			μA
Low level input current (2)	I _{IL2}	V _{IL2} =V _{SS} With pull up resistor K00-03•10-13•20-23	-20		-3	μA
Low level input current (3)	I _{IL3}	V _{IL3} =V _{SS} With pull up resistor P00-03•10-13•20-23	-30		-3	μA
Low level input current (4)	I _{IL4}	V _{IL4} =V _{SS} RESET	-20		-0.5	μA
Low level input current (5)	I _{IL5}	V _{IL5} =0.1•V _{SS} RESET	-100			μA
High level output current (1)	I _{OH1}	V _{OH1} =0.1•V _{SS} R00-03•10-13•30-33•40-43 P00-03•10-13•20-23			-300	μA
High level output current (2)	I _{OH2}	V _{OH2} =0.1•V _{SS2} R20-23			-300	μA
Low level output current (1)	I _{OL1}	V _{OL1} =0.9•V _{SS} R00-03•10-13•30-33•40-43 P00-03•10-13•20-23	500			μA
Low level output current (2)	I _{OL2}	V _{OL2} =0.9•V _{SS2} R20-23	5			mA

● Analog Circuit Characteristics and Current Consumption

(Unless otherwise specified: $V_{DD}=0V$, $V_{SS}=-2.2$ to $-5.5V$, $f_{osc1}=38.4kHz$ (crystal), $f_{osc3}=500kHz$ (ceramic), $T_a=25^{\circ}C$, $C_G=10pF$, $C_{GC}/C_{DC}=108pF$, $V_{ADJ}=V_{L2}$, $RA1/RA2=1M\Omega$, $CS1/CL1-CL4/C1-C3=0.1\mu F$)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit	
LCD drive voltage *1	VL1	Connect 1M Ω load resistor between V _{DD} and VL1 (No panel load), V _{SS} =-2.5 to -5.5V	0.50 ×VL2		0.45 ×VL2	V	
	VL2	Connect 1M Ω load resistor between V _{DD} and VL2 (No panel load), V _{SS} =-2.5 to -5.5V	-2.25	-2.10	-1.95	V	
	VL3	Connect 1M Ω load resistor between V _{DD} and VL3 (No panel load), V _{SS} =-2.5 to -5.5V	1.50 ×VL2		1.45 ×VL2	V	
	VL4	Connect 1M Ω load resistor between V _{DD} and VL4 (No panel load), V _{SS} =-2.5 to -5.5V	2.00 ×VL2		1.95 ×VL2	V	
BLD voltage (internal)	V _{BLD1}		-2.50	-2.35	-2.20	V	
BLD voltage (external)	V _{BLD2}		-1.13	-1.05	-0.97	V	
BLD circuit stability time *2	t _{BLD}				100	μ S	
BLD circuit current consumption	I _{BLD}	V _{SS} =-3.0V		10	20	μ A	
Analog comparator input voltage	V _{IP}	Noninverted input (CMPP)	V _{SS} +0.3		-1.0	V	
	V _{IM}	Inverted input (CMPM)					
Analog comparator offset voltage	V _{OF}	V _{IP} =-1.0 to V _{SS} +0.3V V _{IM} =-1.0 to V _{SS} +0.3V			50	mV	
Analog comparator stabilizing time *2	t _{CMP1}	V _{IP} =-1.0 to V _{SS} +0.3V V _{IM} =-1.0 to V _{SS} +0.3V			100	μ S	
Analog comparator response time	t _{CMP2}	V _{SS} =-2.2V V _{IP} =-1.1V, V _{IM} =-1.1±0.1V			100	μ S	
Analog comparator current consumption (1)	I _{CMP1}	V _{SS} =-3.0V V _{IP} =-1.4V, V _{IM} =-1.6V		4	10	μ A	
Analog comparator current consumption (2)	I _{CMP2}	V _{SS} =-3.0V V _{IP} =-1.6V, V _{IM} =-1.4V		8	15	μ A	
Current consumption	I _{OP}	During HALT (1) *3	OSCC="0" No panel load		1.8	4.0	μ A
		During HALT (2) *4			1.3	3.0	μ A
		During operation at 38.4kHz *3			9	15	μ A
		During operation at 500kHz *5			110	150	μ A

*1: When selecting not to use LCD drive power by option, V_{DD} (=0V) is output to VL2.

*2: The stabilizing time is the time from turning the circuit on until the output data stabilizes.

*3: The time base counter is RUN status, programmable timer, BLD circuit and analog comparator are OFF status, and the input and output terminals are static status.

*4: The same status as *1 and is when not using LCD drive power by option, and selecting DC output to the R12 port output form.

*5: The BLD circuit and analog comparator are OFF status and the input and output terminals are static status.

● Oscillation Characteristics

The oscillation characteristics change depending on the conditions (components used, board pattern, etc.). Use the following characteristics as reference values.

OSC1 crystal oscillation circuit

(Unless otherwise specified: $V_{DD}=0V$, $V_{SS}=-2.2$ to $-5.5V$, Crystal: C2-TYPE(Seiko Epson), $C_G=25pF$, C_D =built-in, $T_a=25^{\circ}C$)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start time	t _{sta}	V _{SS} =-2.2 to -5.5V			3	Sec
Built-in capacitance (drain)	C _D	For 60 pin plastic package	—	20	—	pF
Frequency/voltage deviation	$\partial f/\partial V$	V _{SS} =-2.2 to -5.5V			5	ppm
Frequency/IC deviation	$\partial f/\partial IC$		-10		10	ppm
Frequency adjustment range	$\partial f/\partial C_G$	C _G =5 to 25pF	40			ppm
Permitted leak resistance	R _{leak}	Between OSC1 and V _{DD} , V _{S1}	200			M Ω

OSC3 ceramic oscillation circuit

(Unless otherwise specified: $V_{DD}=0V$, $V_{SS}=-2.2$ to $-5.5V$, Ceramic: CSB500E(Murata Mfg. Co.), $C_{GC}=C_{DC}=108pF$, $T_a=25^{\circ}C$)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start time	t _{sta}	V _{SS} =-2.2 to -5.5V		4	10	mS

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