EPSON

E0C6281

4-bit Single Chip Microcomputer

Low Voltage Operation Products

- Core CPU Architecture
- SVD Circuit/Comparator
- Melody Circuit

■ DESCRIPTION

The E0C6281 is an advanced single-chip CMOS 4-bit microcomputer consisting of the E0C6200 CMOS 4-bit core CPU. It also contains the ROM, RAM, LCD driver, time base counter and melody generation circuit. The E0C6281 provides an excellent solution for low-power consumption systems with clock functions.

■ FEATURES

- CMOS LSI ..... 4-bit parallel processing
- Clock ..... 32.768kHz (Typ.)
- Instruction set ..... 100 instructions
- Instruction cycle time ..... 153µsec, 214µsec or 366µsec (depending on instruction)
- ROM capacity ..... 1,024 × 12 bits
- RAM capacity ..... 96 × 4 bits
- Input port ..... 5 bits
  (pull-down resistors are available by mask option)
- Output port ..... 4 bits (general purpose port)
  2 bits (for melody output): MO, $\overline{\text{MO}}$ (also used as the external CR connecting terminal for envelope)
  1 bit (for lamp output)
  1 bit (for clock output: frequency can be selected from 256Hz through 32kHz by mask option)
- I/O port ..... 4 bits
- LCD driver ..... 26 segments × 3 commons, 1/3 duty or 4 commons, 1/4 duty
- Built-in stopwatch timer
- Built-in supply voltage detection (SVD) circuit
- Built-in comparator ..... 1 ch.
- Built-in melody generation circuit ..... Equivalent to SVM7500 (80-word melody ROM is built in)
- Interrupts ..... External : Input interrupt 2 lines
  Internal : Timer interrupt 1 line
  Stopwatch interrupt 1 line
  Melody completion interrupt 1 line
- Supply voltage ..... 1.5V/3.0V (Minimum operating voltage: 0.9V/1.8V)
- Current consumption ..... E0C6281/62L81 HALT mode : 1.0µA (Typ.)
  OPERATING mode : 2.5µA (Typ.)
  E0C62A81/62B81 HALT mode : 5.5µA (Typ.)
  OPERATING mode : 7.2µA (Typ.)
- Package ..... QFP6-64pin-S1 (plastic)
  Die form

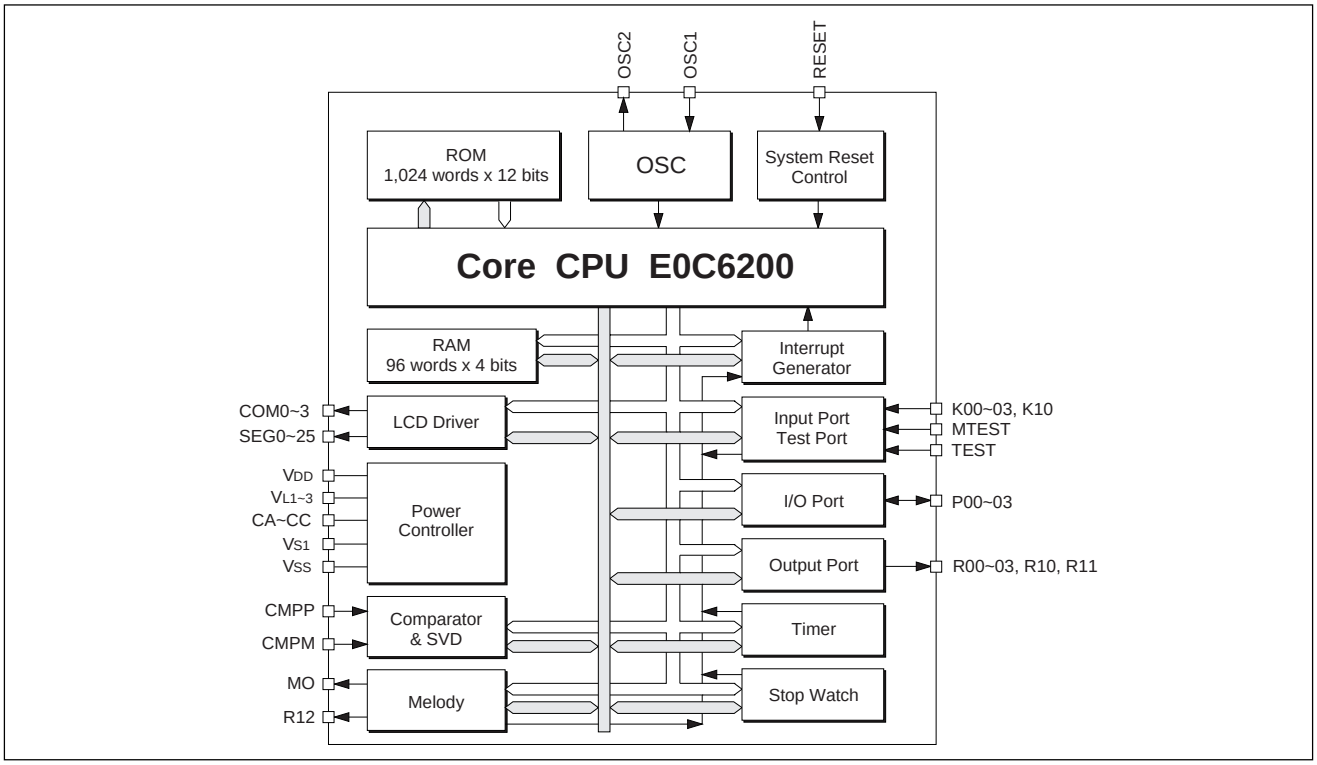
■ LINE UP

Model	Supply voltage	Clock
E0C6281	3.0V (1.8V to 3.5V)	32kHz (Crystal oscillation)
E0C62L81	1.5V (0.9V to 3.5V)	32kHz (Crystal oscillation)
E0C62A81	3.0V (1.8V to 3.5V)	32kHz (CR oscillation)
E0C62B81	1.5V (0.9V to 3.5V)	32kHz (CR oscillation)

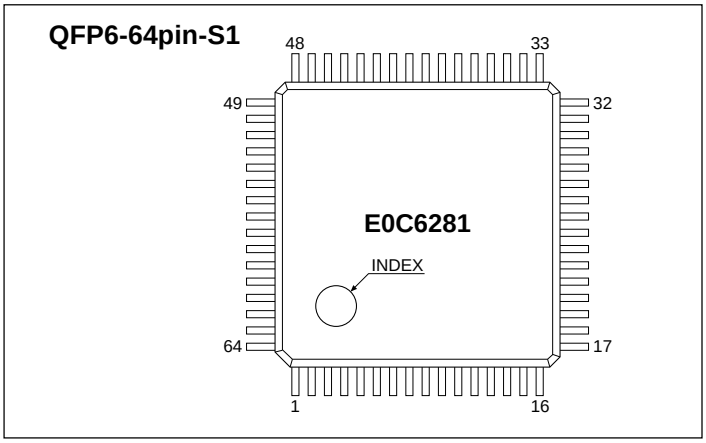
< Detail of Melody Function >

- Melody memory capacity ..... 80 words
- Interval memory capacity ..... 16 words (including one pause note)
- Interval generated ..... C3 to C6#, or C4 to C7# (mask option)
- Useful note ..... 8 (from sixteenth note to a half note)
- Tempo ..... Basic: Select 2 tempos out of 16 tempos (30 to 480) (mask option)
  (The tempo selected is changed by the software control.)
  The tempo having 8 times, 16 times or 32 times the basic tempo is available by software.
- Envelope ..... External CR is required. (not available for the piezoelectic direct drive type)
- Piezoelectic direct drive ..... Envelope not available
- Melody control function ..... (1) 1 music: Melody start address is controlled by the software.
  (2) Repeating: The address is controlled by the software when repeated.
  (3) Forcible music change: The new music address is designated with the software while a music is now played.

■ BLOCK DIAGRAM



■ PIN CONFIGURATION



No.	Pin name	No.	Pin name	No.	Pin name	No.	Pin name
1	COM1	17	SEG12	33	P01	49	R00
2	COM2	18	TEST	34	P02	50	R01
3	COM3	19	SEG13	35	P03	51	R02
4	SEG25	20	SEG14	36	CMPM	52	R03
5	SEG0	21	SEG15	37	CMPP	53	V_{S1}
6	SEG1	22	SEG16	38	MTEST	54	V_{DD}
7	SEG2	23	SEG17	39	RESET	55	V_{SS}
8	SEG3	24	SEG18	40	K00	56	OSC2
9	SEG4	25	SEG19	41	K01	57	OSC1
10	SEG5	26	SEG20	42	K02	58	V_{L3}
11	SEG6	27	SEG21	43	K03	59	V_{L2}
12	SEG7	28	SEG22	44	K10	60	V_{L1}
13	SEG8	29	SEG23	45	R10	61	CC
14	SEG9	30	SEG24	46	R11	62	CB
15	SEG10	31	N.C.	47	R12	63	CA
16	SEG11	32	P00	48	MO	64	COM0

N.C. = No Connection

■ PIN DESCRIPTION

Pin name	Pin No.	In/Out	Function
V_{DD}	54	I	Power source (+) terminal
V_{SS}	55	I	Power source (-) terminal
V_{S1}	53	O	Oscillation and internal logic system regulated voltage output terminal
V_{L1}	60	O	LCD system regulated voltage output terminal (approx. -1.05 V)
V_{L2}	59	O	LCD system booster output terminal (V_{L1} x 2)
V_{L3}	58	O	LCD system booster output terminal (V_{L1} x 3)
CA–CC	61–63	–	Booster capacitor connecting terminal
OSC1	57	I	Crystal or CR oscillation input terminal
OSC2	56	O	Crystal or CR oscillation output terminal
K00–K03, K10	40–44	I	Input terminal
P00–P03	32–35	I/O	I/O terminal
R00–R03	49–52	O	Output terminal
R10	45	O	Output terminal (FOUT output available by mask option)
R11	46	O	Output terminal
R12	47	O	Output terminal (Melody inverted output and envelope function available by mask option)
MO	48	O	Melody signal output terminal
CMPP	37	I	Analog comparator non-inverted input terminal
CMPM	36	I	Analog comparator inverted input terminal
SEG0–25	4–17, 19–30	O	LCD segment output terminal (Convertible to DC output by mask option)
COM0–3	64, 1–3	O	LCD common output terminal
RESET	39	I	Initial reset input terminal
TEST	18	I	Test input terminal
MTEST	38	I	Melody test input terminal

■ ELECTRICAL CHARACTERISTICS

● Absolute Maximum Ratings

(V_{DD}=0V)

Rating	Symbol	Value	Unit
Supply voltage	V_{SS}	-5.0 to 0.5	V
Input voltage (1)	V_I	V_{SS} - 0.3 to 0.5	V
Input voltage (2)	V_{IOSC}	V_{SS} - 0.3 to 0.5	V
Permissible total output current *1	ΣI_{VSS}	10	mA
Operating temperature	Topr	-20 to 70	°C
Storage temperature	Tstg	-65 to 150	°C
Soldering temperature / Time	Tsol	260°C, 10sec (lead section)	–
Permissible dissipation *2	P_D	250	mW

∗1: The permissible total output current is the sum total of the current (average current) that simultaneously flows from the output pins (or is draw in).
∗2: In case of plastic package (QFP6-64pin).

● Recommended Operating Conditions

E0C6281/62A81

(Ta=-20 to 70°C)

Condition	Symbol	Remark	Min.	Typ.	Max.	Unit
Supply voltage	V_{SS}	V_{DD}=0V	-3.5	-3.0	-1.8	V
Oscillation frequency	f_{OSC}		–	32.768	–	kHz

E0C62L81/62B81

(Ta=-20 to 70°C)

Condition	Symbol	Remark	Min.	Typ.	Max.	Unit
Supply voltage	V_{SS}	V_{DD}=0V	-3.5	-1.5	-1.1	V
		V_{DD}=0V, With software control *1	-3.5	-1.5	-0.9 *2	V
		V_{DD}=0V, When the analog comparator is used	-3.5	-1.5	-1.3	V
Oscillation frequency	f_{OSC}		–	32.768	–	kHz

∗1: When switching to heavy load protection mode. The SVD circuit and analog voltage comparator are turned OFF.
∗2: The possibility of LCD panel display differs depending on the characteristics of the LCD panel.

● DC Characteristics

E0C6281/62A81

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-3.0V, f_{OSC}=32.768kHz, Ta=25°C, V_{S1}/V_{L1}–V_{L3} are internal voltage, C1–C6=0.1µF)

Characteristic	Symbol	Condition		Min.	Typ.	Max.	Unit
High level input voltage (1)	V_{IH1}		K00–K03, K10, P00–P03 MTEST	0.2•V_{SS}		0	V
High level input voltage (2)	V_{IH2}		RESET, TEST	0.10•V_{SS}		0	V
Low level input voltage (1)	V_{IL1}		K00–K03, K10, P00–P03 MTEST	V_{SS}		0.8•V_{SS}	V
Low level input voltage (2)	V_{IL2}		RESET, TEST	V_{SS}		0.90•V_{SS}	V
High level input current (1)	I_{IH1}	V_{IH1}=0V No pull down resistor	K00–K03, K10, P00–P03 CMPP, CMPM	0		0.5	µA
High level input current (2)	I_{IH2}	V_{IH2}=0V With pull down resistor	K00–K03, K10	5		16	µA
High level input current (3)	I_{IH3}	V_{IH3}=0V With pull down resistor	P00–P03 RESET, TEST, MTEST	30		100	µA
Low level input current	I_{IL}	V_{IL}=V_{SS}	K00–K03, K10, P00–P03 CMPP, CMPM RESET, TEST, MTEST	-0.5		0	µA
High level output current (1)	I_{OH1}	V_{OH1}=0.1•V_{SS}	R11			-1.0	mA
High level output current (2)	I_{OH2}	V_{OH2}=0.1•V_{SS}	R00–R03, R10, P00–P03			-1.0	mA
High level output current (3)	I_{OH3}	V_{OH3}=0.1•V_{SS}	MO, R12			-2.0	mA
Low level output current (1)	I_{OL1}	V_{OL1}=0.9•V_{SS}	R11	3.0			mA
Low level output current (2)	I_{OL2}	V_{OL2}=0.9•V_{SS}	R00–R03, R10, P00–P03	3.0			mA
Low level output current (3)	I_{OL3}	V_{OL3}=0.9•V_{SS}	MO, R12	4.5			mA
Common output current	I_{OH4}	V_{OH4}=-0.05V	COM0–COM3			-3	µA
	I_{OL4}	V_{OL4}=V_{L3}+0.05V		3			µA
Segment output current (during LCD output)	I_{OH5}	V_{OH5}=-0.05V	SEG0–SEG25			-3	µA
	I_{OL5}	V_{OL5}=V_{L3}+0.05V		3			µA
Segment output current (during DC output)	I_{OH6}	V_{OH6}=0.1•V_{SS}	SEG0–SEG25			-300	µA
	I_{OL6}	V_{OL6}=0.9•V_{SS}		300			µA

E0C62L81/62B81

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-1.5V, f_{OSC}=32.768kHz, Ta=25°C, V_{S1}/V_{L1}–V_{L3} are internal voltage, C1–C6=0.1µF)

Characteristic	Symbol	Condition		Min.	Typ.	Max.	Unit
High level input voltage (1)	V_{IH1}		K00–K03, K10, P00–P03 MTEST	0.2•V_{SS}		0	V
High level input voltage (2)	V_{IH2}		RESET, TEST	0.10•V_{SS}		0	V
Low level input voltage (1)	V_{IL1}		K00–K03, K10, P00–P03 MTEST	V_{SS}		0.8•V_{SS}	V
Low level input voltage (2)	V_{IL2}		RESET, TEST	V_{SS}		0.90•V_{SS}	V
High level input current (1)	I_{IH1}	V_{IH1}=0V No pull down resistor	K00–K03, K10, P00–P03 CMPP, CMPM	0		0.5	µA
High level input current (2)	I_{IH2}	V_{IH2}=0V With pull down resistor	K00–K03, K10	2.0		10	µA
High level input current (3)	I_{IH3}	V_{IH3}=0V With pull down resistor	P00–P03 RESET, TEST, MTEST	9.0		60	µA
Low level input current	I_{IL}	V_{IL}=V_{SS}	K00–K03, K10, P00–P03 CMPP, CMPM RESET, TEST, MTEST	-0.5		0	µA
High level output current (1)	I_{OH1}	V_{OH1}=0.1•V_{SS}	R11			-450	µA
High level output current (2)	I_{OH2}	V_{OH2}=0.1•V_{SS}	R00–R03, R10, P00–P03			-200	µA
High level output current (3)	I_{OH3}	V_{OH3}=0.1•V_{SS}	MO, R12			-0.8	mA
High level output current (4)	I_{OH4}	V_{OH4}=0.1•V_{SS} When envelope is used	MO (R12=Normal H level)			-0.4	mA
Low level output current (1)	I_{OL1}	V_{OL1}=0.9•V_{SS}	R11	1,300			µA
Low level output current (2)	I_{OL2}	V_{OL2}=0.9•V_{SS}	R00–R03, R10, P00–P03	700			µA
Low level output current (3)	I_{OL3}	V_{OL3}=0.9•V_{SS}	MO, R12	1.5			mA
Low level output current (4)	I_{OL4}	V_{OL4}=0.9•V_{SS} When envelope is used	MO (R12=Normal L level)	750			µA
Common output current	I_{OH5}	V_{OH5}=-0.05V	COM0–COM3			-3	µA
	I_{OL5}	V_{OL5}=V_{L3}+0.05V		3			µA
Segment output current (during LCD output)	I_{OH6}	V_{OH6}=-0.05V	SEG0–SEG25			-3	µA
	I_{OL6}	V_{OL6}=V_{L3}+0.05V		3			µA
Segment output current (during DC output)	I_{OH7}	V_{OH7}=0.1•V_{SS}	SEG0–SEG25			-100	µA
	I_{OL7}	V_{OL7}=0.9•V_{SS}		130			µA

● Analog Circuit Characteristics and Current Consumption

E0C6281 (Normal Operating Mode)

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-3.0V, f_{OSC}=32.768kHz, Ta=25°C, C_G=25pF, V_{S1}/V_{L1}–V_{L3} are internal voltage, C1–C6=0.1µF)

Characteristic	Symbol	Condition		Min.	Typ.	Max.	Unit
Internal voltage	V_{L1}	Connect 1MΩ load resistor between V_{DD} and V_{L1} (without panel load)		-1.15	-1.05	-0.95	V
	V_{L2}	Connect 1MΩ load resistor between V_{DD} and V_{L2} (without panel load)		2•V_{L1} -0.1		2•V_{L1} ×0.9	V
	V_{L3}	Connect 1MΩ load resistor between V_{DD} and V_{L3} (without panel load)		3•V_{L1} -0.1		3•V_{L1} ×0.9	V
SVD voltage	V_{SVD}			-2.55	-2.40	-2.25	V
SVD circuit response time	t_{SVD}					100	µS
Analog comparator input voltage	V_{IP}	Noninverted input (CMPP)		V_{SS}+0.3		V_{DD}-0.9	V
	V_{IM}	Inverted input (CMPM)					
Analog comparator offset voltage	V_{OF}					10	mV
Analog comparator response time	t_{CMP}	V_{IP}=-1.5V, V_{IM}=V_{IP}±15mV				3	mS
Current consumption	I_{OP}	During HALT	Without panel load		1.0	2.5	µA
		During operation *1			2.5	5.0	µA

*1: The SVD circuit and analog voltage comparator are turned OFF.

E0C6281 (Heavy Load Protection Mode)

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-3.0V, f_{OSC}=32.768kHz, Ta=25°C, C_G=25pF, V_{S1}/V_{L1}–V_{L3} are internal voltage, C1–C6=0.1µF)

Characteristic	Symbol	Condition		Min.	Typ.	Max.	Unit
Internal voltage	V_{L1}	Connect 1MΩ load resistor between V_{DD} and V_{L1} (without panel load)		-1.15	-1.05	-0.95	V
	V_{L2}	Connect 1MΩ load resistor between V_{DD} and V_{L2} (without panel load)		2•V_{L1} -0.1		2•V_{L1} ×0.85	V
	V_{L3}	Connect 1MΩ load resistor between V_{DD} and V_{L3} (without panel load)		3•V_{L1} -0.1		3•V_{L1} ×0.85	V
SVD voltage	V_{SVD}			-2.55	-2.40	-2.25	V
SVD circuit response time	t_{SVD}					100	µS
Analog comparator input voltage	V_{IP}	Noninverted input (CMPP)		V_{SS}+0.3		V_{DD}-0.9	V
	V_{IM}	Inverted input (CMPM)					
Analog comparator offset voltage	V_{OF}					10	mV
Analog comparator response time	t_{CMP}	V_{IP}=-1.5V, V_{IM}=V_{IP}±15mV				3	mS
Current consumption	I_{OP}	During HALT	Without panel load		2.0	5.5	µA
		During operation *1			5.5	10.0	µA

*1: The SVD circuit and analog voltage comparator are turned OFF.

E0C62L81 (Normal Operating Mode)

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-1.5V, f_{OSC}=32.768kHz, Ta=25°C, C_G=25pF, V_{S1}/V_{L1}–V_{L3} are internal voltage, C1–C6=0.1µF)

Characteristic	Symbol	Condition		Min.	Typ.	Max.	Unit
Internal voltage	V_{L1}	Connect 1MΩ load resistor between V_{DD} and V_{L1} (without panel load)		-1.15	-1.05	-0.95	V
	V_{L2}	Connect 1MΩ load resistor between V_{DD} and V_{L2} (without panel load)		2•V_{L1} -0.1		2•V_{L1} ×0.9	V
	V_{L3}	Connect 1MΩ load resistor between V_{DD} and V_{L3} (without panel load)		3•V_{L1} -0.1		3•V_{L1} ×0.9	V
SVD voltage	V_{SVD}			-1.30	-1.20	-1.10	V
SVD circuit response time	t_{SVD}					100	µS
Analog comparator input voltage	V_{IP}	Noninverted input (CMPP)		V_{SS}+0.3		V_{DD}-0.9	V
	V_{IM}	Inverted input (CMPM)					
Analog comparator offset voltage	V_{OF}					20	mV
Analog comparator response time	t_{CMP}	V_{IP}=-1.1V, V_{IM}=V_{IP}±30mV				3	mS
Current consumption	I_{OP}	During HALT	Without panel load		1.0	2.5	µA
		During operation *1			2.5	5.0	µA

*1: The SVD circuit and analog voltage comparator are turned OFF.

E0C62L81 (Heavy Load Protection Mode)

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-1.5V, f_{OSC}=32.768kHz, Ta=25°C, C_G=25pF, V_{S1}/V_{L1}–V_{L3} are internal voltage, C1–C6=0.1µF)

Characteristic	Symbol	Condition		Min.	Typ.	Max.	Unit
Internal voltage	V_{L1}	Connect 1MΩ load resistor between V_{DD} and V_{L1} (without panel load)		-1.15	-1.05	-0.95	V
	V_{L2}	Connect 1MΩ load resistor between V_{DD} and V_{L2} (without panel load)		2•V_{L1} -0.1		2•V_{L1} ×0.85	V
	V_{L3}	Connect 1MΩ load resistor between V_{DD} and V_{L3} (without panel load)		3•V_{L1} -0.1		3•V_{L1} ×0.85	V
SVD voltage	V_{SVD}			-1.30	-1.20	-1.10	V
SVD circuit response time	t_{SVD}					100	µS
Analog comparator input voltage	V_{IP}	Noninverted input (CMPP)		V_{SS}+0.3		V_{DD}-0.9	V
	V_{IM}	Inverted input (CMPM)					
Analog comparator offset voltage	V_{OF}					20	mV
Analog comparator response time	t_{CMP}	V_{IP}=-1.1V, V_{IM}=V_{IP}±30mV				3	mS
Current consumption	I_{OP}	During HALT	Without panel load		2.0	5.5	µA
		During operation *1			5.5	10.0	µA

*1: The SVD circuit and analog voltage comparator are turned OFF.

E0C62A81 (Normal Operating Mode)

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-3.0V, f_{OSC}=32.768kHz, Ta=25°C, C_G=25pF, V_{S1}/V_{L1}–V_{L3} are internal voltage, C1–C6=0.1µF)

Characteristic	Symbol	Condition		Min.	Typ.	Max.	Unit
Internal voltage	V_{L1}	Connect 1MΩ load resistor between V_{DD} and V_{L1} (without panel load)		-1.15	-1.05	-0.95	V
	V_{L2}	Connect 1MΩ load resistor between V_{DD} and V_{L2} (without panel load)		2•V_{L1} -0.1		2•V_{L1} ×0.9	V
	V_{L3}	Connect 1MΩ load resistor between V_{DD} and V_{L3} (without panel load)		3•V_{L1} -0.1		3•V_{L1} ×0.9	V
SVD voltage	V_{SVD}			-2.55	-2.40	-2.25	V
SVD circuit response time	t_{SVD}					100	µS
Analog comparator input voltage	V_{IP}	Noninverted input (CMPP)		V_{SS}+0.3		V_{DD}-0.9	V
	V_{IM}	Inverted input (CMPM)					
Analog comparator offset voltage	V_{OF}					10	mV
Analog comparator response time	t_{CMP}	V_{IP}=-1.5V, V_{IM}=V_{IP}±15mV				3	mS
Current consumption	I_{OP}	During HALT	Without panel load		5.5	10.0	µA
		During operation *1			7.2	12.0	µA

*1: The SVD circuit and analog voltage comparator are turned OFF.

E0C62A81 (Heavy Load Protection Mode)

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-3.0V, f_{OSC}=32.768kHz, Ta=25°C, C_G=25pF, V_{S1}/V_{L1}–V_{L3} are internal voltage, C1–C6=0.1µF)

Characteristic	Symbol	Condition		Min.	Typ.	Max.	Unit
Internal voltage	V_{L1}	Connect 1MΩ load resistor between V_{DD} and V_{L1} (without panel load)		-1.15	-1.05	-0.95	V
	V_{L2}	Connect 1MΩ load resistor between V_{DD} and V_{L2} (without panel load)		2•V_{L1} -0.1		2•V_{L1} ×0.85	V
	V_{L3}	Connect 1MΩ load resistor between V_{DD} and V_{L3} (without panel load)		3•V_{L1} -0.1		3•V_{L1} ×0.85	V
SVD voltage	V_{SVD}			-2.55	-2.40	-2.25	V
SVD circuit response time	t_{SVD}					100	µS
Analog comparator input voltage	V_{IP}	Noninverted input (CMPP)		V_{SS}+0.3		V_{DD}-0.9	V
	V_{IM}	Inverted input (CMPM)					
Analog comparator offset voltage	V_{OF}					10	mV
Analog comparator response time	t_{CMP}	V_{IP}=-1.5V, V_{IM}=V_{IP}±15mV				3	mS
Current consumption	I_{OP}	During HALT	Without panel load		11.0	20.0	µA
		During operation *1			15.0	25.0	µA

*1: The SVD circuit and analog voltage comparator are turned OFF.

E0C62B81 (Normal Operating Mode)

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-1.5V, f_{OSC}=32.768kHz, Ta=25°C, C_G=25pF, V_{S1}/V_{L1}–V_{L3} are internal voltage, C1–C6=0.1µF)

Characteristic	Symbol	Condition		Min.	Typ.	Max.	Unit
Internal voltage	V_{L1}	Connect 1MΩ load resistor between V_{DD} and V_{L1} (without panel load)		-1.15	-1.05	-0.95	V
	V_{L2}	Connect 1MΩ load resistor between V_{DD} and V_{L2} (without panel load)		2•V_{L1} -0.1		2•V_{L1} ×0.9	V
	V_{L3}	Connect 1MΩ load resistor between V_{DD} and V_{L3} (without panel load)		3•V_{L1} -0.1		3•V_{L1} ×0.9	V
SVD voltage	V_{SVD}			-1.30	-1.20	-1.10	V
SVD circuit response time	t_{SVD}					100	µS
Analog comparator input voltage	V_{IP}	Noninverted input (CMPP)		V_{SS}+0.3		V_{DD}-0.9	V
	V_{IM}	Inverted input (CMPM)					
Analog comparator offset voltage	V_{OF}					20	mV
Analog comparator response time	t_{CMP}	V_{IP}=-1.1V, V_{IM}=V_{IP}±30mV				3	mS
Current consumption	I_{OP}	During HALT	Without panel load		5.5	10.0	µA
		During operation *1			7.2	12.0	µA

*1: The SVD circuit and analog voltage comparator are turned OFF.

E0C62B81 (Heavy Load Protection Mode)

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-1.5V, f_{OSC}=32.768kHz, Ta=25°C, C_G=25pF, V_{S1}/V_{L1}–V_{L3} are internal voltage, C1–C6=0.1µF)

Characteristic	Symbol	Condition		Min.	Typ.	Max.	Unit
Internal voltage	V_{L1}	Connect 1MΩ load resistor between V_{DD} and V_{L1} (without panel load)		-1.15	-1.05	-0.95	V
	V_{L2}	Connect 1MΩ load resistor between V_{DD} and V_{L2} (without panel load)		2•V_{L1} -0.1		2•V_{L1} ×0.85	V
	V_{L3}	Connect 1MΩ load resistor between V_{DD} and V_{L3} (without panel load)		3•V_{L1} -0.1		3•V_{L1} ×0.85	V
SVD voltage	V_{SVD}			-1.30	-1.20	-1.10	V
SVD circuit response time	t_{SVD}					100	µS
Analog comparator input voltage	V_{IP}	Noninverted input (CMPP)		V_{SS}+0.3		V_{DD}-0.9	V
	V_{IM}	Inverted input (CMPM)					
Analog comparator offset voltage	V_{OF}					20	mV
Analog comparator response time	t_{CMP}	V_{IP}=-1.1V, V_{IM}=V_{IP}±30mV				3	mS
Current consumption	I_{OP}	During HALT	Without panel load		11.0	20.0	µA
		During operation *1			15.0	25.0	µA

*1: The SVD circuit and analog voltage comparator are turned OFF.

● Oscillation Characteristics

The oscillation characteristics change depending on the conditions (components used, board pattern, etc.). Use the following characteristics as reference values.

E0C6281 (Crystal)

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-3.0V, Crystal: C-002R (C_I=35kΩ), C_G=25pF, C_D=built-in, Ta=25°C)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start voltage	Vsta	tsta≤3sec (Vss)	-1.8			V
Oscillation stop voltage	Vstp	tstp≤10sec (Vss)	-1.8			V
Built-in capacitance (drain)	C_D	Including the parasitic capacity inside the IC		20		pF
Frequency/voltage deviation	∂f/∂V	V_{SS}=-1.8 to -3.5V			5	ppm
Frequency/IC deviation	∂f/∂IC		-10		10	ppm
Frequency adjustment range	∂f/∂C_G	C_G=5 to 25pF	40			ppm
Harmonic oscillation start voltage	V_{hho}	(Vss)			-3.5	V
Permitted leak resistance	R_{leak}	Between OSC1 and V_{DD}, V_{SS}	200			MΩ

E0C62L81 (Crystal)

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-1.5V, Crystal: C-002R (C_I=35kΩ), C_G=25pF, C_D=built-in, Ta=25°C)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start voltage	Vsta	tsta≤3sec (Vss)	-1.1			V
Oscillation stop voltage	Vstp	tstp≤10sec (Vss)	-1.1(-0.9)*1			V
Built-in capacitance (drain)	C_D	Including the parasitic capacity inside the IC		20		pF
Frequency/voltage deviation	∂f/∂V	V_{SS}=-1.1 to -3.5V (-0.9) *1			5	ppm
Frequency/IC deviation	∂f/∂IC		-10		10	ppm
Frequency adjustment range	∂f/∂C_G	C_G=5 to 25pF	40			ppm
Harmonic oscillation start voltage	V_{hho}	(Vss)			-3.5	V
Permitted leak resistance	R_{leak}	Between OSC1 and V_{DD}, V_{SS}	200			MΩ

*1: Items enclosed in parentheses ( ) are those used when operating at heavy load protection mode.

E0C62A81 (CR)

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-3.0V, R_{CR}=850kΩ, Ta=25°C)

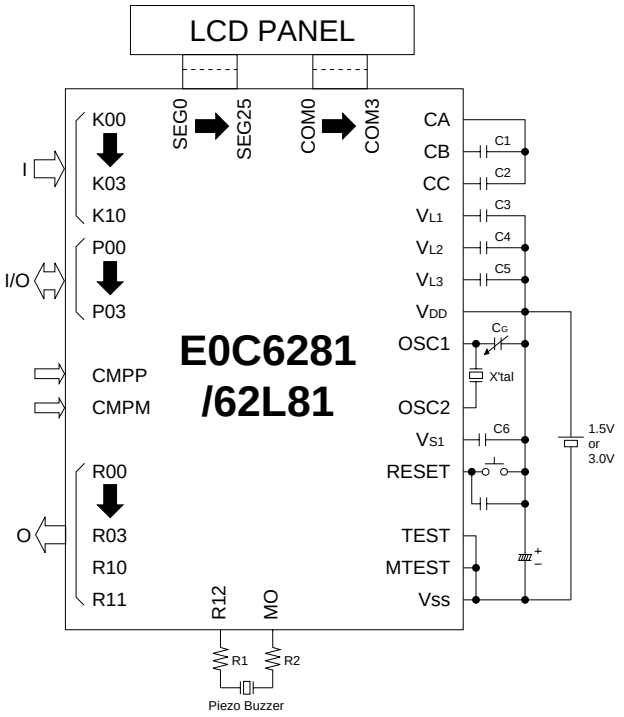
Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation frequency dispersion	f_{OSC}		-20	32.768kHz	20	%
Oscillation start voltage	Vsta	(Vss)	-1.8			V
Oscillation start time	tsta	V_{SS}=-1.8 to -3.5V		3		mS
Oscillation stop voltage	Vstp	(Vss)	-1.8			V

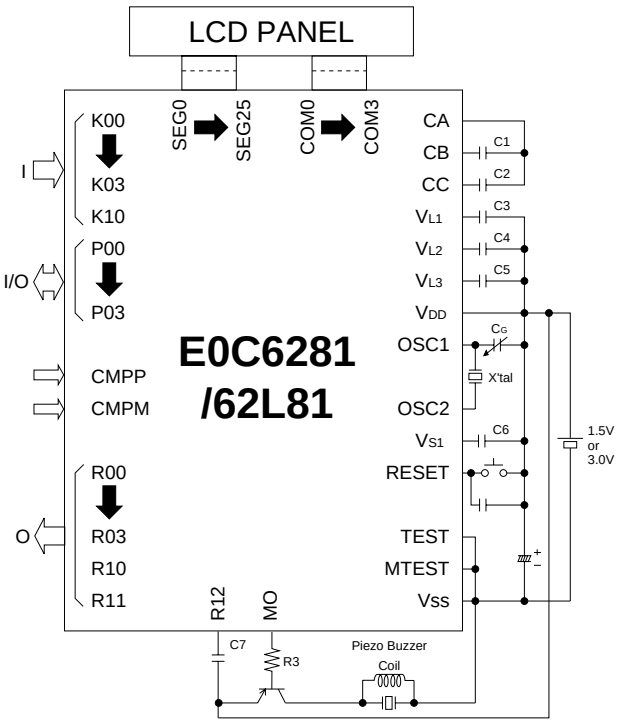
E0C62B81 (CR)

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-1.5V, R_{CR}=850kΩ, Ta=25°C)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation frequency dispersion	f_{OSC}		-20	32.768kHz	20	%
Oscillation start voltage	Vsta	(Vss)	-0.9			V
Oscillation start time	tsta	V_{SS}=-0.9 to -3.5V		3		mS
Oscillation stop voltage	Vstp	(Vss)	-0.9			V

■ BASIC EXTERNAL CONNECTION DIAGRAM





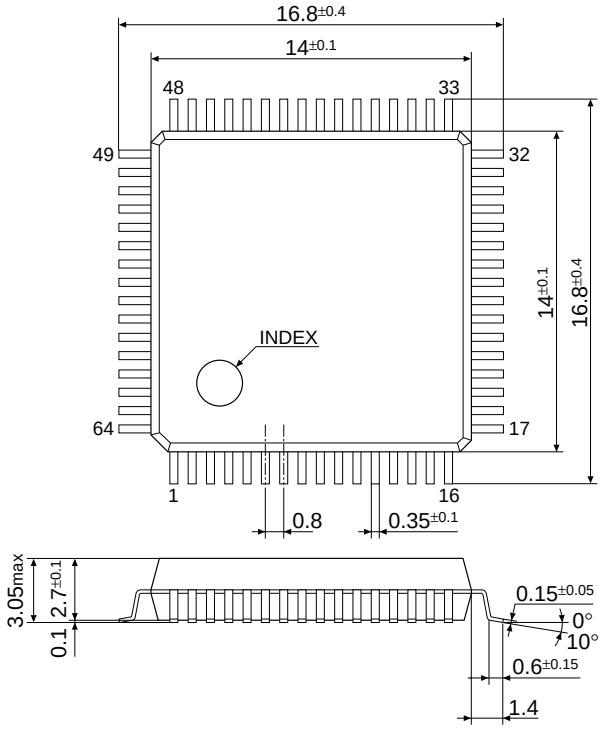
X'tal	Crystal oscillator	32.768kHz, CI(Max.)=35kΩ
CG	Trimmer capacitor	5–25pF
C1–C6	Capacitor	0.1µF
Cp	Capacitor	3.3µF
R1, R2	Protection resistor	100Ω

X'tal	Crystal oscillator	32.768kHz, CI(Max.)=35kΩ
CG	Trimmer capacitor	5–25pF
C1–C6	Capacitor	0.1µF
C7	Capacitor	1µF–10µF
Cp	Capacitor	3.3µF
R3	Resistor	1kΩ or more

Note: The above tables are simply an example, and are not guaranteed to work.

■ PACKAGE DIMENSIONS

Plastic QFP6-64pin-S1



Unit: mm

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