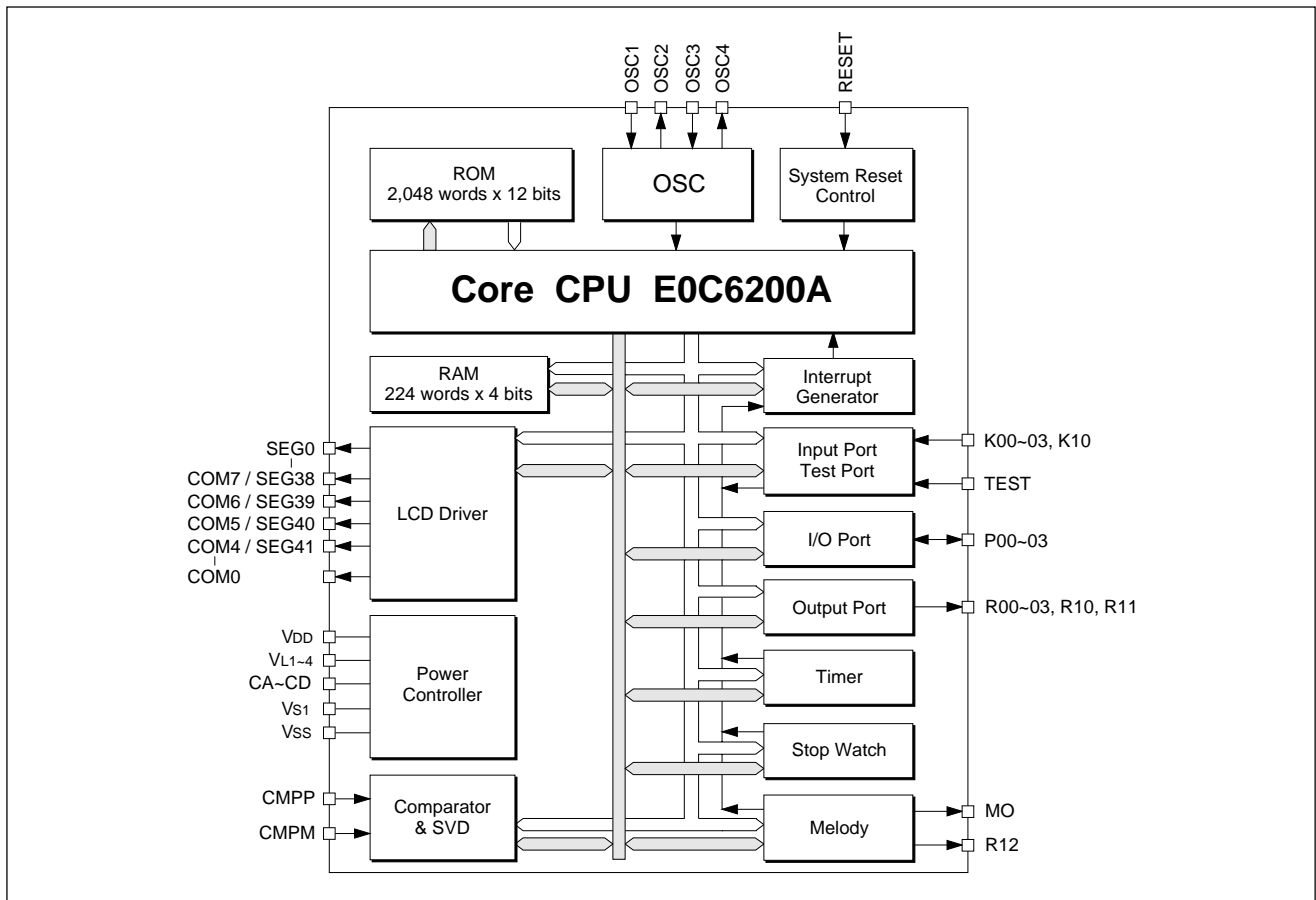


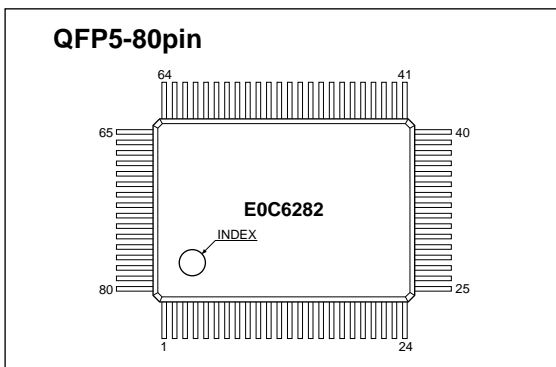


# E0C6282

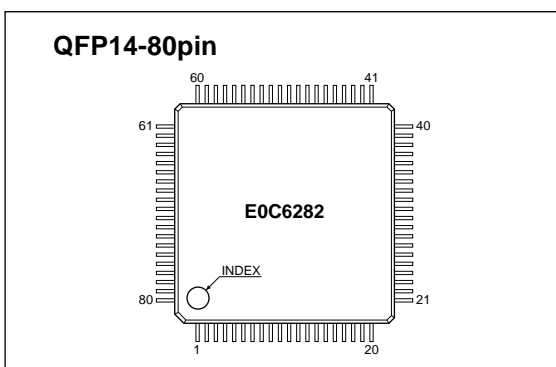
## ■ BLOCK DIAGRAM



## ■ PIN CONFIGURATION



No.	Pin name	No.	Pin name	No.	Pin name	No.	Pin name	No.	Pin name
1	VDD	17	SEG14	33	K02	49	SEG28	65	P01
2	TEST	18	SEG15	34	K01	50	SEG29	66	P00
3	SEG0	19	SEG16	35	K00	51	SEG30	67	CD
4	SEG1	20	SEG17	36	RESET	52	SEG31	68	CC
5	SEG2	21	SEG18	37	CMPP	53	SEG32	69	CB
6	SEG3	22	SEG19	38	CMPP	54	SEG33	70	CA
7	SEG4	23	R03	39	COM3	55	SEG34	71	VL4
8	SEG5	24	R02	40	COM2	56	SEG35	72	VL3
9	SEG6	25	R01	41	COM1	57	SEG36	73	VL2
10	SEG7	26	R00	42	COM0	58	SEG37	74	VL1
11	SEG8	27	MO	43	SEG22	59	SEG38/COM7	75	Vss
12	SEG9	28	R12	44	SEG23	60	SEG39/COM6	76	OSC4
13	SEG10	29	R11	45	SEG24	61	SEG40/COM5	77	OSC3
14	SEG11	30	R10	46	SEG25	62	SEG41/COM4	78	Vs1
15	SEG12	31	K10	47	SEG26	63	P03	79	OSC2
16	SEG13	32	K03	48	SEG27	64	P02	80	OSC1



No.	Pin name	No.	Pin name	No.	Pin name	No.	Pin name	No.	Pin name
1	SEG0	17	SEG16	33	K00	49	SEG30	65	CD
2	SEG1	18	SEG17	34	RESET	50	SEG31	66	CC
3	SEG2	19	SEG18	35	CMPP	51	SEG32	67	CB
4	SEG3	20	SEG19	36	CMPP	52	SEG33	68	CA
5	SEG4	21	R03	37	COM3	53	SEG34	69	VL4
6	SEG5	22	R02	38	COM2	54	SEG35	70	VL3
7	SEG6	23	R01	39	COM1	55	SEG36	71	VL2
8	SEG7	24	R00	40	COM0	56	SEG37	72	VL1
9	SEG8	25	MO	41	SEG22	57	SEG38/COM7	73	Vss
10	SEG9	26	R12	42	SEG23	58	SEG39/COM6	74	OSC4
11	SEG10	27	R11	43	SEG24	59	SEG40/COM5	75	OSC3
12	SEG11	28	R10	44	SEG25	60	SEG41/COM4	76	Vs1
13	SEG12	29	K10	45	SEG26	61	P03	77	OSC2
14	SEG13	30	K03	46	SEG27	62	P02	78	OSC1
15	SEG14	31	K02	47	SEG28	63	P01	79	VDD
16	SEG15	32	K01	48	SEG29	64	P00	80	TEST

## PIN DESCRIPTION

Pin name	Pin No.		In/Out	Function
	QFP5-80pin	QFP14-80pin		
VDD	1	79	I	Power source (+) terminal
VSS	75	73	I	Power source (-) terminal
Vs1	78	76	-	Oscillation and internal logic system regulated voltage output terminal
VL1-VL4	71-74	69-72	-	LCD system power source terminal
CA-CD	67-70	65-68	-	LCD system booster capacitor connecting terminal
OSC1	80	78	I	Crystal or CR oscillation input terminal
OSC2	79	77	O	Crystal or CR oscillation output terminal
OSC3	77	75	I	Ceramic or CR oscillation input terminal (62A82 only)
OSC4	76	74	O	Ceramic or CR oscillation output terminal (62A82 only)
K00-K00, K10	32-35, 31	30-33, 29	I	Input terminal
P00-P03	63-66	61-64	I/O	I/O terminal
R00-R03	23-26	21-24	O	Output terminal
R10	30	28	O	Output terminal (FOUT output available by mask option)
R11	29	27	O	Output terminal
R12	28	26	O	Output terminal (Melody inverted output and envelope function available by mask option)
MO	27	25	O	Melody signal output terminal
CMPP	37	35	I	Analog comparator non-inverted input terminal
CMPM	38	36	I	Analog comparator inverted input terminal
SEG0-37	3-22, 43-58	1-20, 41-56	O	LCD segment output terminal (Convertible to DC output by mask option) SEG20 and 21 may be used only when the chip has been supplied
COM0-3	39-42	37-40	O	LCD common output terminal
SEG38-41 COM4-7	59-62	57-60	O	LCD segment output terminal when 1/4 duty is selected LCD common output terminal when 1/8 duty is selected
RESET	36	34	I	Initial reset input terminal
TEST	2	80	I	Test input terminal

## ELECTRICAL CHARACTERISTICS

### Absolute Maximum Ratings

(V<sub>DD</sub>=0V)

Rating	Symbol	Value	Unit
Supply voltage	V <sub>SS</sub>	-6.0 to 0.5	V
Input voltage (1)	V <sub>I</sub>	V <sub>SS</sub> - 0.3 to 0.5	V
Input voltage (2)	V <sub>I</sub> osc	V <sub>S1</sub> - 0.3 to 0.5	V
Permissible total output current *1	ΣI <sub>vss</sub>	10	mA
Operating temperature	T <sub>opr</sub>	-20 to 70	°C
Storage temperature	T <sub>stg</sub>	-65 to 150	°C
Soldering temperature / Time	T <sub>sol</sub>	260°C, 10sec (lead section)	-
Permissible dissipation *2	P <sub>D</sub>	250	mW

\*1: The permissible total output current is the sum total of the current (average current) that simultaneously flows from the output pins (or is draw in).

\*2: In case of plastic package (QFP5-80pin, QFP14-80pin).

### Recommended Operating Conditions

#### E0C6282

(T<sub>a</sub>=-20 to 70°C)

Condition	Symbol	Remark	Min.	Typ.	Max.	Unit
Supply voltage	V <sub>SS</sub>	V <sub>DD</sub> =0V	-5.5	-3.0	-2.2	V
Oscillation frequency	fosc1		-	32.768	-	kHz

#### E0C62L82

(T<sub>a</sub>=-20 to 70°C)

Condition	Symbol	Remark	Min.	Typ.	Max.	Unit
Supply voltage	V <sub>SS</sub>	V <sub>DD</sub> =0V	-3.5	-1.5	-1.1	V
		V <sub>DD</sub> =0V, With software control *1	-3.5	-1.5	-0.9 *2	V
		V <sub>DD</sub> =0V, When the analog comparator is used	-3.5	-1.5	-1.3	V
Oscillation frequency	fosc1		-	32.768	-	kHz

\*1: When switching to heavy load protection mode. The SVD circuit and analog voltage comparator are turned OFF.

\*2: The possibility of LCD panel display differs depending on the characteristics of the LCD panel.

#### E0C62A82

(T<sub>a</sub>=-20 to 70°C)

Condition	Symbol	Remark	Min.	Typ.	Max.	Unit
Supply voltage	V <sub>SS</sub>	V <sub>DD</sub> =0V	-5.5	-3.0	-2.2	V
Oscillation frequency (1)	fosc1		-	32.768	-	kHz
Oscillation frequency (2)	fosc3	duty 50±5%	-	1,000	-	kHz

# E0C6282

## ● DC Characteristics

### E0C6282/62A82

(Unless otherwise specified:  $V_{DD}=0V$ ,  $V_{SS}=-3.0V$ ,  $f_{osc1}=32.768kHz$ ,  $T_a=25^\circ C$ ,  $V_{S1}/V_{L1}-V_{L4}$  are internal voltage,  $C_1-C_6=0.1\mu F$ )

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
High level input voltage (1)	$V_{IH1}$	K00-K03, K10, P00-P03	$0.2 \cdot V_{SS}$		0	V
High level input voltage (2)	$V_{IH2}$	RESET, TEST	$0.10 \cdot V_{SS}$		0	V
Low level input voltage (1)	$V_{IL1}$	K00-K03, K10, P00-P03	$V_{SS}$		$0.8 \cdot V_{SS}$	V
Low level input voltage (2)	$V_{IL2}$	RESET, TEST	$V_{SS}$		$0.90 \cdot V_{SS}$	V
High level input current (1)	$I_{IH1}$	$V_{IH1}=0V$ No pull down resistor K00-K03, K10, P00-P03 CMPP, CMPM	0		0.5	$\mu A$
High level input current (2)	$I_{IH2}$	$V_{IH2}=0V$ With pull down resistor K00-K03, K10	5		16	$\mu A$
High level input current (3)	$I_{IH3}$	$V_{IH3}=0V$ With pull down resistor P00-P03 RESET, TEST	30		100	$\mu A$
Low level input current	$I_{IL}$	$V_{IL}=V_{SS}$ K00-K03, K10, P00-P03 CMPP, CMPM RESET, TEST	-0.5		0	$\mu A$
High level output current (1)	$I_{OH1}$	$V_{OH1}=0.1 \cdot V_{SS}$ R11			-1.0	mA
High level output current (2)	$I_{OH2}$	$V_{OH2}=0.1 \cdot V_{SS}$ R00-R03, R10, P00-P03			-1.0	mA
High level output current (3)	$I_{OH3}$	$V_{OH3}=0.1 \cdot V_{SS}$ MO, R12			-2.0	mA
Low level output current (1)	$I_{OL1}$	$V_{OL1}=0.9 \cdot V_{SS}$ R11	3.0			mA
Low level output current (2)	$I_{OL2}$	$V_{OL2}=0.9 \cdot V_{SS}$ R00-R03, R10, P00-P03	3.0			mA
Low level output current (3)	$I_{OL3}$	$V_{OL3}=0.9 \cdot V_{SS}$ MO, R12	4.5			mA
Common output current 1/4 duty	$I_{OH4}$	$V_{OH4}=-0.05V$ COM0-COM3			-3	$\mu A$
Segment output current (during LCD output) 1/4 duty	$I_{OL4}$	$V_{OL4}=V_{L3}+0.05V$	3			$\mu A$
Segment output current (during DC output) 1/4 duty	$I_{OH5}$	$V_{OH5}=-0.05V$ SEG0-SEG41			-3	$\mu A$
Common output current 1/8 duty	$I_{OL5}$	$V_{OL5}=V_{L3}+0.05V$	3			$\mu A$
Segment output current (during LCD output) 1/8 duty	$I_{OH6}$	$V_{OH6}=0.1 \cdot V_{SS}$ SEG0-SEG41			-300	$\mu A$
Segment output current (during DC output) 1/8 duty	$I_{OL6}$	$V_{OL6}=0.9 \cdot V_{SS}$	300			$\mu A$
Common output current 1/8 duty	$I_{OH7}$	$V_{OH7}=-0.05V$ COM0-COM7			-3	$\mu A$
Segment output current (during LCD output) 1/8 duty	$I_{OL7}$	$V_{OL7}=V_{L4}+0.05V$	3			$\mu A$
Segment output current (during DC output) 1/8 duty	$I_{OH8}$	$V_{OH8}=-0.05V$ SEG0-SEG37			-3	$\mu A$
Segment output current (during DC output) 1/8 duty	$I_{OL8}$	$V_{OL8}=V_{L4}+0.05V$	3			$\mu A$
Segment output current (during DC output) 1/8 duty	$I_{OH9}$	$V_{OH9}=0.1 \cdot V_{SS}$ SEG0-SEG37			-300	$\mu A$
Segment output current (during DC output) 1/8 duty	$I_{OL9}$	$V_{OL9}=0.9 \cdot V_{SS}$	300			$\mu A$

### E0C62L82

(Unless otherwise specified:  $V_{DD}=0V$ ,  $V_{SS}=-1.5V$ ,  $f_{osc1}=32.768kHz$ ,  $T_a=25^\circ C$ ,  $V_{S1}/V_{L1}-V_{L4}$  are internal voltage,  $C_1-C_6=0.1\mu F$ )

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
High level input voltage (1)	$V_{IH1}$	K00-K03, K10, P00-P03	$0.2 \cdot V_{SS}$		0	V
High level input voltage (2)	$V_{IH2}$	RESET, TEST	$0.10 \cdot V_{SS}$		0	V
Low level input voltage (1)	$V_{IL1}$	K00-K03, K10, P00-P03	$V_{SS}$		$0.8 \cdot V_{SS}$	V
Low level input voltage (2)	$V_{IL2}$	RESET, TEST	$V_{SS}$		$0.90 \cdot V_{SS}$	V
High level input current (1)	$I_{IH1}$	$V_{IH1}=0V$ No pull down resistor K00-K03, K10, P00-P03 CMPP, CMPM	0		0.5	$\mu A$
High level input current (2)	$I_{IH2}$	$V_{IH2}=0V$ With pull down resistor K00-K03, K10	2.0		10	$\mu A$
High level input current (3)	$I_{IH3}$	$V_{IH3}=0V$ With pull down resistor P00-P03 RESET, TEST	9.0		60	$\mu A$
Low level input current	$I_{IL}$	$V_{IL}=V_{SS}$ K00-K03, K10, P00-P03 CMPP, CMPM RESET, TEST	-0.5		0	$\mu A$
High level output current (1)	$I_{OH1}$	$V_{OH1}=0.1 \cdot V_{SS}$ R11			-450	$\mu A$
High level output current (2)	$I_{OH2}$	$V_{OH2}=0.1 \cdot V_{SS}$ R00-R03, R10, P00-P03			-200	$\mu A$
High level output current (3)	$I_{OH3}$	$V_{OH3}=0.1 \cdot V_{SS}$ MO, R12			-0.8	mA
High level output current (4)	$I_{OH4}$	$V_{OH4}=0.1 \cdot V_{SS}$ When envelope is used MO (R12=Normal H level)			-0.4	mA
Low level output current (1)	$I_{OL1}$	$V_{OL1}=0.9 \cdot V_{SS}$ R11	1,300			$\mu A$
Low level output current (2)	$I_{OL2}$	$V_{OL2}=0.9 \cdot V_{SS}$ R00-R03, R10, P00-P03	700			$\mu A$
Low level output current (3)	$I_{OL3}$	$V_{OL3}=0.9 \cdot V_{SS}$ MO, R12	1.5			mA
Low level output current (4)	$I_{OL4}$	$V_{OL4}=0.9 \cdot V_{SS}$ When envelope is used MO (R12=Normal L level)	750			$\mu A$
Common output current 1/4 duty	$I_{OH5}$	$V_{OH5}=-0.05V$ COM0-COM3			-3	$\mu A$
Segment output current (during LCD output) 1/4 duty	$I_{OL5}$	$V_{OL5}=V_{L3}+0.05V$	3			$\mu A$
Segment output current (during DC output) 1/4 duty	$I_{OH6}$	$V_{OH6}=-0.05V$ SEG0-SEG41			-3	$\mu A$
Segment output current (during DC output) 1/4 duty	$I_{OL6}$	$V_{OL6}=V_{L3}+0.05V$	3			$\mu A$
Common output current 1/8 duty	$I_{OH7}$	$V_{OH7}=0.1 \cdot V_{SS}$ SEG0-SEG41			-100	$\mu A$
Segment output current (during LCD output) 1/8 duty	$I_{OL7}$	$V_{OL7}=0.9 \cdot V_{SS}$	130			$\mu A$
Segment output current (during DC output) 1/8 duty	$I_{OH8}$	$V_{OH8}=-0.05V$ COM0-COM7			-3	$\mu A$
Segment output current (during DC output) 1/8 duty	$I_{OL8}$	$V_{OL8}=V_{L4}+0.05V$	3			$\mu A$
Segment output current (during DC output) 1/8 duty	$I_{OH9}$	$V_{OH9}=-0.05V$ SEG0-SEG37			-3	$\mu A$
Segment output current (during DC output) 1/8 duty	$I_{OL9}$	$V_{OL9}=V_{L4}+0.05V$	3			$\mu A$
Segment output current (during DC output) 1/8 duty	$I_{OH10}$	$V_{OH10}=0.1 \cdot V_{SS}$ SEG0-SEG37			-100	$\mu A$
Segment output current (during DC output) 1/8 duty	$I_{OL10}$	$V_{OL10}=0.9 \cdot V_{SS}$	130			$\mu A$

## ● Analog Circuit Characteristics and Current Consumption

### E0C6282 (Normal Operating Mode)

(Unless otherwise specified:  $V_{DD}=0V$ ,  $V_{SS}=-3.0V$ ,  $f_{OSC1}=32.768kHz$ ,  $T_a=25^{\circ}C$ ,  $C_G=25pF$ ,  $V_{S1}/V_{L1}-V_{L4}$  are internal voltage,  $C1-C6=0.1\mu F$ )

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Internal voltage	$V_{L1}$	Connect 1M $\Omega$ load resistor between $V_{DD}$ and $V_{L1}$ (without panel load)	0.5• $V_{L2}$ -0.1		0.5• $V_{L2}$ +0.1	V
	$V_{L2}$	Connect 1M $\Omega$ load resistor between $V_{DD}$ and $V_{L2}$ (without panel load)	-2.25	-2.10	-1.95	V
	$V_{L3}$	Connect 1M $\Omega$ load resistor between $V_{DD}$ and $V_{L3}$ (without panel load)	3• $V_{L1}$ -0.1		3• $V_{L1}$ $\times 0.9$	V
	$V_{L4}$	Connect 1M $\Omega$ load resistor between $V_{DD}$ and $V_{L4}$ (without panel load)	4• $V_{L1}$ -0.1		4• $V_{L1}$ $\times 0.9$	V
SVD voltage	$V_{SVD}$		-2.55	-2.40	-2.25	V
SVD circuit response time	$t_{SVD}$				100	$\mu S$
Analog comparator input voltage	$V_{IP}$	Noninverted input (CMPP)	$V_{SS}+0.3$		$V_{DD}-0.9$	V
	$V_{IM}$	Inverted input (CMPM)				
Analog comparator offset voltage	$V_{OF}$				10	mV
Analog comparator response time	$t_{CMP}$	$V_{IP}=-1.5V$ , $V_{IM}=V_{IP}\pm 15mV$			1	mS
Current consumption	IOP1	During HALT *1	Without panel load	1.5	3.0	$\mu A$
		During operation *1	OSC1 is crystal oscillation	4.0	7.0	$\mu A$
	IOP2	During HALT *1	Without panel load	6.0	10.5	$\mu A$
		During operation *1	OSC1 is CR oscillation	8.7	14.0	$\mu A$

\*1: The SVD circuit and analog voltage comparator are turned OFF.

### E0C6282 (Heavy Load Protection Mode)

(Unless otherwise specified:  $V_{DD}=0V$ ,  $V_{SS}=-3.0V$ ,  $f_{OSC1}=32.768kHz$ ,  $T_a=25^{\circ}C$ ,  $C_G=25pF$ ,  $V_{S1}/V_{L1}-V_{L4}$  are internal voltage,  $C1-C6=0.1\mu F$ )

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Internal voltage	$V_{L1}$	Connect 1M $\Omega$ load resistor between $V_{DD}$ and $V_{L1}$ (without panel load)	0.5• $V_{L2}$ -0.1		0.5• $V_{L2}$ +0.1	V
	$V_{L2}$	Connect 1M $\Omega$ load resistor between $V_{DD}$ and $V_{L2}$ (without panel load)	-2.25	-2.10	-1.95	V
	$V_{L3}$	Connect 1M $\Omega$ load resistor between $V_{DD}$ and $V_{L3}$ (without panel load)	3• $V_{L1}$ -0.1		3• $V_{L1}$ $\times 0.9$	V
	$V_{L4}$	Connect 1M $\Omega$ load resistor between $V_{DD}$ and $V_{L4}$ (without panel load)	4• $V_{L1}$ -0.1		4• $V_{L1}$ $\times 0.9$	V
SVD voltage	$V_{SVD}$		-2.55	-2.40	-2.25	V
SVD circuit response time	$t_{SVD}$				100	$\mu S$
Analog comparator input voltage	$V_{IP}$	Noninverted input (CMPP)	$V_{SS}+0.3$		$V_{DD}-0.9$	V
	$V_{IM}$	Inverted input (CMPM)				
Analog comparator offset voltage	$V_{OF}$				10	mV
Analog comparator response time	$t_{CMP}$	$V_{IP}=-1.5V$ , $V_{IM}=V_{IP}\pm 15mV$			1	mS
Current consumption	IOP1	During HALT *1	Without panel load	11.5	33.0	$\mu A$
		During operation *1	OSC1 is crystal oscillation	14.0	37.0	$\mu A$
	IOP2	During HALT *1	Without panel load	16.0	40.5	$\mu A$
		During operation *1	OSC1 is CR oscillation	18.7	44.0	$\mu A$

\*1: The SVD circuit and analog voltage comparator are turned OFF.

### E0C62L82 (Normal Operating Mode)

(Unless otherwise specified:  $V_{DD}=0V$ ,  $V_{SS}=-1.5V$ ,  $f_{OSC1}=32.768kHz$ ,  $T_a=25^{\circ}C$ ,  $C_G=25pF$ ,  $V_{S1}/V_{L1}-V_{L4}$  are internal voltage,  $C1-C6=0.1\mu F$ )

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Internal voltage	$V_{L1}$	Connect 1M $\Omega$ load resistor between $V_{DD}$ and $V_{L1}$ (without panel load)	-1.15	-1.05	-0.95	V
	$V_{L2}$	Connect 1M $\Omega$ load resistor between $V_{DD}$ and $V_{L2}$ (without panel load)	2• $V_{L1}$ -0.1		2• $V_{L1}$ $\times 0.9$	V
	$V_{L3}$	Connect 1M $\Omega$ load resistor between $V_{DD}$ and $V_{L3}$ (without panel load)	3• $V_{L1}$ -0.1		3• $V_{L1}$ $\times 0.9$	V
	$V_{L4}$	Connect 1M $\Omega$ load resistor between $V_{DD}$ and $V_{L4}$ (without panel load)	4• $V_{L1}$ -0.1		4• $V_{L1}$ $\times 0.9$	V
SVD voltage	$V_{SVD}$		-1.30	-1.20	-1.10	V
SVD circuit response time	$t_{SVD}$				100	$\mu S$
Analog comparator input voltage	$V_{IP}$	Noninverted input (CMPP)	$V_{SS}+0.3$		$V_{DD}-0.9$	V
	$V_{IM}$	Inverted input (CMPM)				
Analog comparator offset voltage	$V_{OF}$				20	mV
Analog comparator response time	$t_{CMP}$	$V_{IP}=-1.1V$ , $V_{IM}=V_{IP}\pm 30mV$			1	mS
Current consumption	IOP1	During HALT *1	Without panel load	1.5	3.0	$\mu A$
		During operation *1	OSC1 is crystal oscillation	4.0	7.0	$\mu A$
	IOP2	During HALT *1	Without panel load	6.0	10.5	$\mu A$
		During operation *1	OSC1 is CR oscillation	8.7	14.0	$\mu A$

\*1: The SVD circuit and analog voltage comparator are turned OFF.

## E0C62L82 (Heavy Load Protection Mode)

(Unless otherwise specified: V<sub>DD</sub>=0V, V<sub>SS</sub>=-1.5V, f<sub>OSC1</sub>=32.768kHz, T<sub>a</sub>=25°C, C<sub>G</sub>=25pF, V<sub>S1</sub>/V<sub>L1</sub>–V<sub>L4</sub> are internal voltage, C<sub>1</sub>–C<sub>6</sub>=0.1μF)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Internal voltage	V <sub>L1</sub>	Connect 1MΩ load resistor between V <sub>DD</sub> and V <sub>L1</sub> (without panel load)	-1.15	-1.05	-0.95	V
	V <sub>L2</sub>	Connect 1MΩ load resistor between V <sub>DD</sub> and V <sub>L2</sub> (without panel load)	2•V <sub>L1</sub> -0.1		2•V <sub>L1</sub> ×0.85	V
	V <sub>L3</sub>	Connect 1MΩ load resistor between V <sub>DD</sub> and V <sub>L3</sub> (without panel load)	3•V <sub>L1</sub> -0.1		3•V <sub>L1</sub> ×0.85	V
	V <sub>L4</sub>	Connect 1MΩ load resistor between V <sub>DD</sub> and V <sub>L4</sub> (without panel load)	4•V <sub>L1</sub> -0.1		4•V <sub>L1</sub> ×0.85	V
SVD voltage	V <sub>SVD</sub>		-1.30	-1.20	-1.10	V
SVD circuit response time	t <sub>SVD</sub>				100	μS
Analog comparator input voltage	V <sub>IP</sub>	Noninverted input (CMPP)	V <sub>SS</sub> +0.3		V <sub>DD</sub> -0.9	V
	V <sub>IM</sub>	Inverted input (CMPM)				
Analog comparator offset voltage	V <sub>OF</sub>				20	mV
Analog comparator response time	t <sub>CMP</sub>	V <sub>IP</sub> =-1.1V, V <sub>IM</sub> =V <sub>IP</sub> ±30mV			1	mS
Current consumption	IOP1	During HALT *1	Without panel load	2.5	6.0	μA
		During operation *1	OSC1 is crystal oscillation	7.0	12.0	μA
	IOP2	During HALT *1	Without panel load	11.5	20.5	μA
		During operation *1	OSC1 is CR oscillation	16.5	27.0	μA

\*1: The SVD circuit and analog voltage comparator are turned OFF.

## E0C62A82 (Normal Operating Mode)

(Unless otherwise specified: V<sub>DD</sub>=0V, V<sub>SS</sub>=-3.0V, f<sub>OSC1</sub>=32.768kHz, T<sub>a</sub>=25°C, C<sub>G</sub>=25pF, V<sub>S1</sub>/V<sub>L1</sub>–V<sub>L4</sub> are internal voltage, C<sub>1</sub>–C<sub>6</sub>=0.1μF)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Internal voltage	V <sub>L1</sub>	Connect 1MΩ load resistor between V <sub>DD</sub> and V <sub>L1</sub> (without panel load)	0.5•V <sub>L2</sub> -0.1		0.5•V <sub>L2</sub> +0.1	V
	V <sub>L2</sub>	Connect 1MΩ load resistor between V <sub>DD</sub> and V <sub>L2</sub> (without panel load)	-2.25	-2.10	-1.95	V
	V <sub>L3</sub>	Connect 1MΩ load resistor between V <sub>DD</sub> and V <sub>L3</sub> (without panel load)	3•V <sub>L1</sub> -0.1		3•V <sub>L1</sub> ×0.9	V
	V <sub>L4</sub>	Connect 1MΩ load resistor between V <sub>DD</sub> and V <sub>L4</sub> (without panel load)	4•V <sub>L1</sub> -0.1		4•V <sub>L1</sub> ×0.9	V
SVD voltage	V <sub>SVD</sub>		-2.55	-2.40	-2.25	V
SVD circuit response time	t <sub>SVD</sub>				100	μS
Analog comparator input voltage	V <sub>IP</sub>	Noninverted input (CMPP)	V <sub>SS</sub> +0.3		V <sub>DD</sub> -0.9	V
	V <sub>IM</sub>	Inverted input (CMPM)				
Analog comparator offset voltage	V <sub>OF</sub>				10	mV
Analog comparator response time	t <sub>CMP</sub>	V <sub>IP</sub> =-1.5V, V <sub>IM</sub> =V <sub>IP</sub> ±15mV			1	mS
Current consumption	IOP1	During HALT *1	Without panel load	1.70	3.0	μA
		During operation at 32kHz *1	OSC1 is crystal oscillation	4.0	7.0	μA
		During operation at 1MHz *2	OSC1 is CR oscillation	150.0	300.0	μA
	IOP2	During HALT *1	Without panel load	30	60	μA
		During operation at 32kHz *1	OSC1 is CR oscillation	30	60	μA
		During operation at 1MHz *2	OSC1 is CR oscillation	160	300	μA

\*1: The OSC3 circuit, SVD circuit and analog voltage comparator are turned OFF.

\*2: The SVD circuit and analog voltage comparator are turned OFF.

## E0C62A82 (Heavy Load Protection Mode)

(Unless otherwise specified: V<sub>DD</sub>=0V, V<sub>SS</sub>=-3.0V, f<sub>OSC1</sub>=32.768kHz, T<sub>a</sub>=25°C, C<sub>G</sub>=25pF, V<sub>S1</sub>/V<sub>L1</sub>–V<sub>L4</sub> are internal voltage, C<sub>1</sub>–C<sub>6</sub>=0.1μF)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Internal voltage	V <sub>L1</sub>	Connect 1MΩ load resistor between V <sub>DD</sub> and V <sub>L1</sub> (without panel load)	0.5•V <sub>L2</sub> -0.1		0.5•V <sub>L2</sub> +0.1	V
	V <sub>L2</sub>	Connect 1MΩ load resistor between V <sub>DD</sub> and V <sub>L2</sub> (without panel load)	-2.25	-2.10	-1.95	V
	V <sub>L3</sub>	Connect 1MΩ load resistor between V <sub>DD</sub> and V <sub>L3</sub> (without panel load)	3•V <sub>L1</sub> -0.1		3•V <sub>L1</sub> ×0.9	V
	V <sub>L4</sub>	Connect 1MΩ load resistor between V <sub>DD</sub> and V <sub>L4</sub> (without panel load)	4•V <sub>L1</sub> -0.1		4•V <sub>L1</sub> ×0.9	V
SVD voltage	V <sub>SVD</sub>		-2.55	-2.40	-2.25	V
SVD circuit response time	t <sub>SVD</sub>				100	μS
Analog comparator input voltage	V <sub>IP</sub>	Noninverted input (CMPP)	V <sub>SS</sub> +0.3		V <sub>DD</sub> -0.9	V
	V <sub>IM</sub>	Inverted input (CMPM)				
Analog comparator offset voltage	V <sub>OF</sub>				10	mV
Analog comparator response time	t <sub>CMP</sub>	V <sub>IP</sub> =-1.5V, V <sub>IM</sub> =V <sub>IP</sub> ±15mV			1	mS
Current consumption	IOP1	During HALT *1	Without panel load	11.7	33.0	μA
		During operation at 32kHz *1	OSC1 is crystal oscillation	14.0	37.0	μA
		During operation at 1MHz *2	OSC1 is CR oscillation	160.0	330.0	μA
	IOP2	During HALT *1	Without panel load	40	90	μA
		During operation at 32kHz *1	OSC1 is CR oscillation	40	90	μA
		During operation at 1MHz *2	OSC1 is CR oscillation	200	420	μA

\*1: The OSC3 circuit, SVD circuit and analog voltage comparator are turned OFF.

\*2: The SVD circuit and analog voltage comparator are turned OFF.

## ● Oscillation Characteristics

The oscillation characteristics change depending on the conditions (components used, board pattern, etc.). Use the following characteristics as reference values.

### E0C6282/62A82 (OSC1 Crystal oscillation)

(Unless otherwise specified:  $V_{DD}=0V$ ,  $V_{SS}=-3.0V$ , Crystal: C-002R ( $C_1=35k\Omega$ ),  $C_G=25pF$ ,  $C_D$ =built-in,  $T_a=25^\circ C$ )

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start voltage	Vsta	$t_{sta} \leq 3sec$ (Vss)	-2.2			V
Oscillation stop voltage	Vstp	$t_{stp} \leq 10sec$ (Vss)	-2.2			V
Built-in capacitance (drain)	$C_D$	Including the parasitic capacity inside the IC		20		pF
Frequency/voltage deviation	$\partial f/\partial V$	$V_{SS}=-2.2$ to $-5.5V$			5	ppm
Frequency/IC deviation	$\partial f/\partial IC$		-10		10	ppm
Frequency adjustment range	$\partial f/\partial C_G$	$C_G=5$ to $25pF$	40			ppm
Harmonic oscillation start voltage	Vhho	(Vss)			-5.5	V
Permitted leak resistance	Rleak	Between OSC1 and $V_{DD}$ , $V_{SS}$	200			M $\Omega$

### E0C62L82 (OSC1 Crystal oscillation)

(Unless otherwise specified:  $V_{DD}=0V$ ,  $V_{SS}=-1.5V$ , Crystal: C-002R ( $C_1=35k\Omega$ ),  $C_G=25pF$ ,  $C_D$ =built-in,  $T_a=25^\circ C$ )

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start voltage	Vsta	$t_{sta} \leq 3sec$ (Vss)	-1.1			V
Oscillation stop voltage	Vstp	$t_{stp} \leq 10sec$ (Vss)	-1.1(-0.9)*1			V
Built-in capacitance (drain)	$C_D$	Including the parasitic capacity inside the IC		20		pF
Frequency/voltage deviation	$\partial f/\partial V$	$V_{SS}=-1.1$ to $-3.5V$ (-0.9) *1			5	ppm
Frequency/IC deviation	$\partial f/\partial IC$		-10		10	ppm
Frequency adjustment range	$\partial f/\partial C_G$	$C_G=5$ to $25pF$	40			ppm
Harmonic oscillation start voltage	Vhho	(Vss)			-3.5	V
Permitted leak resistance	Rleak	Between OSC1 and $V_{DD}$ , $V_{SS}$	200			M $\Omega$

\*1: Items enclosed in parentheses ( ) are those used when operating at heavy load protection mode.

### E0C6282/62A82 (OSC1 CR oscillation)

(Unless otherwise specified:  $V_{DD}=0V$ ,  $V_{SS}=-3.0V$ ,  $R_{CR}=850k\Omega$ ,  $T_a=25^\circ C$ )

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation frequency dispersion	fosc1		-20	32.768kHz	20	%
Oscillation start voltage	Vsta	(Vss)	-2.2			V
Oscillation start time	tsta	$V_{SS}=-2.2$ to $-5.5V$		3		mS
Oscillation stop voltage	Vstp	(Vss)	-2.2			V

### E0C62L82 (OSC1 CR oscillation)

(Unless otherwise specified:  $V_{DD}=0V$ ,  $V_{SS}=-1.5V$ ,  $R_{CR}=850k\Omega$ ,  $T_a=25^\circ C$ )

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation frequency dispersion	fosc1		-20	32.768kHz	20	%
Oscillation start voltage	Vsta	(Vss)	-0.9			V
Oscillation start time	tsta	$V_{SS}=0.9$ to $-3.5V$		3		mS
Oscillation stop voltage	Vstp	(Vss)	-0.9			V

### E0C62A82 (OSC3 CR oscillation)

(Unless otherwise specified:  $V_{DD}=0V$ ,  $V_{SS}=-3.0V$ ,  $R_{CR}=35k\Omega$ ,  $T_a=25^\circ C$ )

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation frequency dispersion	fosc3		-30	1MHz	30	%
Oscillation start voltage	Vsta	(Vss)	-2.2			V
Oscillation start time	tsta	$V_{SS}=-2.2$ to $-5.5V$			3	mS
Oscillation stop voltage	Vstp	(Vss)	-2.2			V

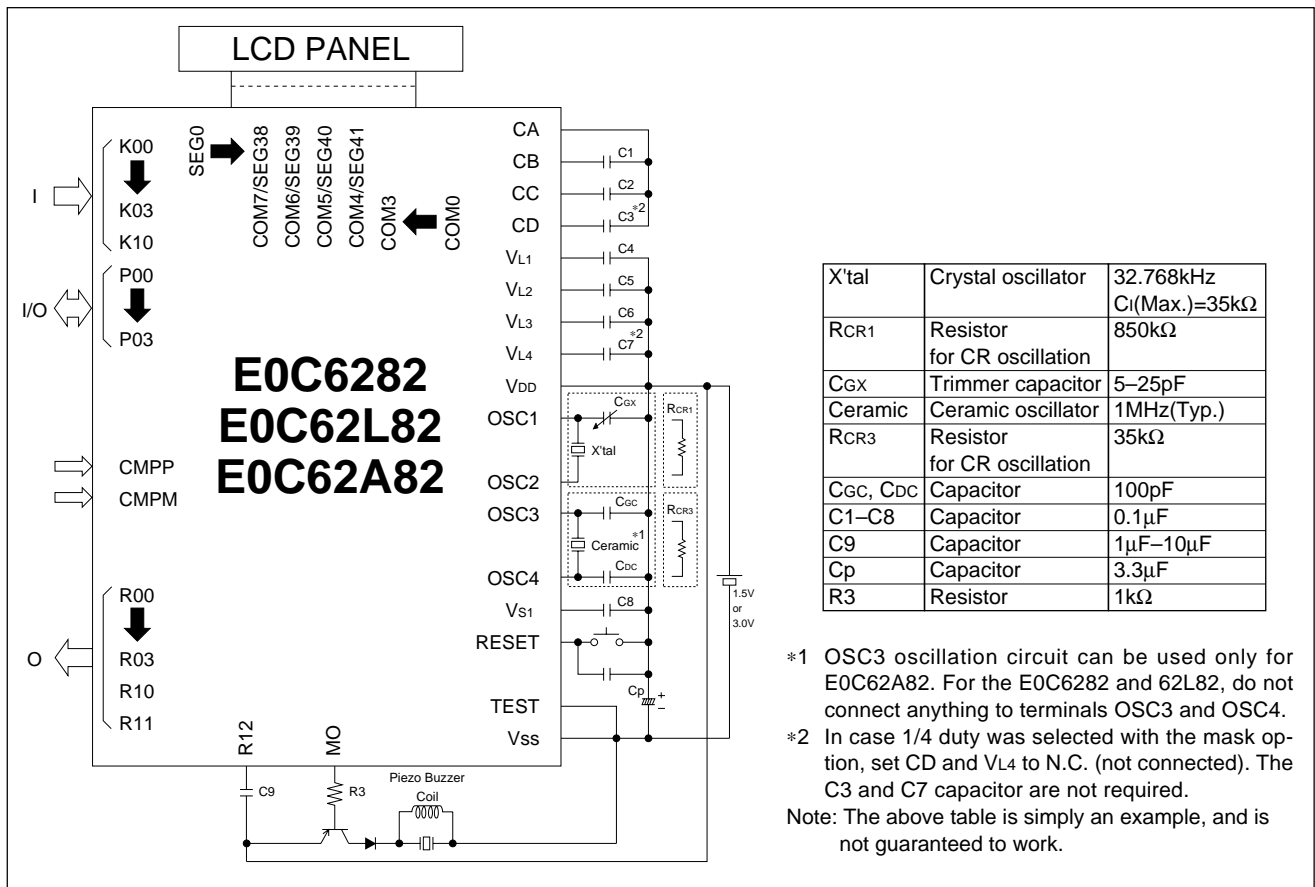
### E0C62A82 (OSC1 Ceramic oscillation)

(Unless otherwise specified:  $V_{DD}=0V$ ,  $V_{SS}=-3.0V$ , ceramic oscillation: 1MHz,  $C_{GC}=C_{DC}=100pF$ ,  $T_a=25^\circ C$ )

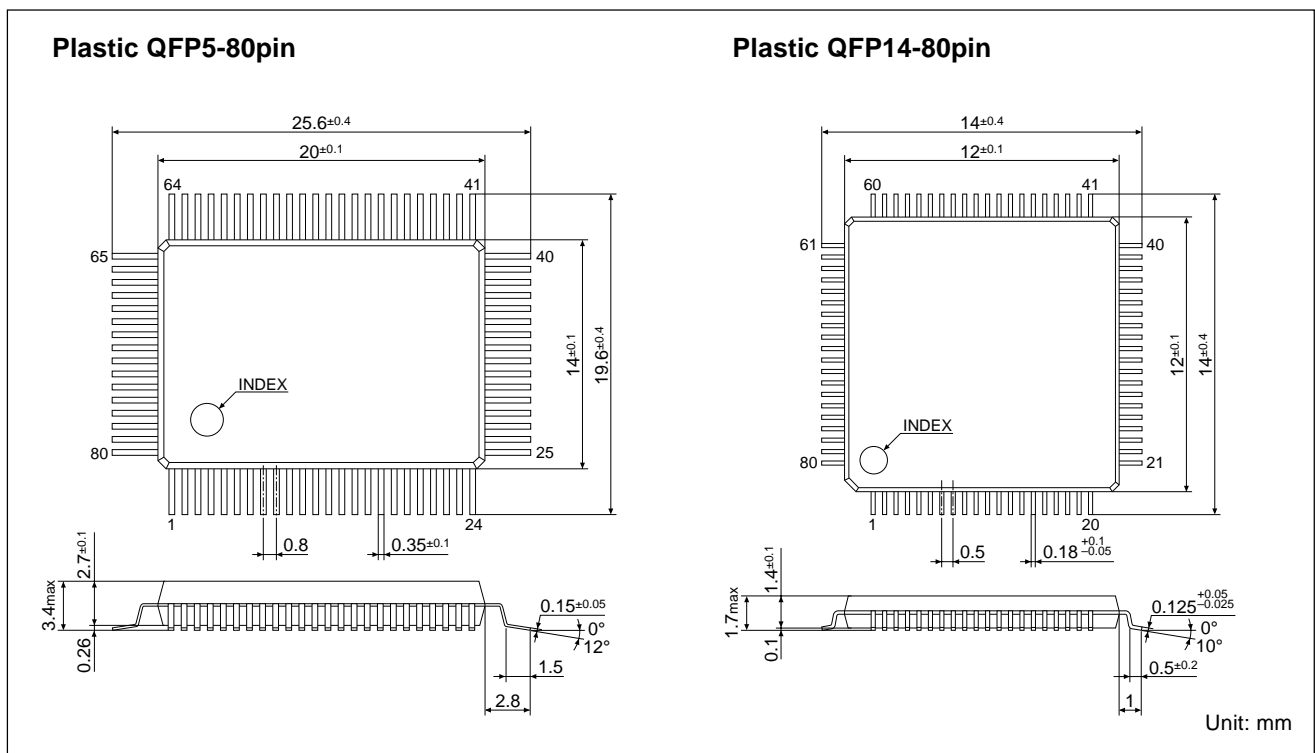
Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start voltage	Vsta	(Vss)	-2.2			V
Oscillation start time	tsta	$V_{SS}=-2.2$ to $-5.5V$			5	mS
Oscillation stop voltage	Vstp	(Vss)	-2.2			V

# E0C6282

## ■ BASIC EXTERNAL CONNECTION DIAGRAM



## ■ PACKAGE DIMENSIONS





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**SEIKO EPSON CORPORATION**

**ELECTRONIC DEVICES MARKETING DIVISION**

**IC Marketing & Engineering Group**

**ED International Marketing Department I (Europe & U.S.A.)**

421-8, Hino, Hino-shi, Tokyo 191-8501, JAPAN  
Phone : 042-587-5812 FAX : 042-587-5564

**ED International Marketing Department II (Asia)**

421-8, Hino, Hino-shi, Tokyo 191-8501, JAPAN  
Phone : 042-587-5814 FAX : 042-587-5110

