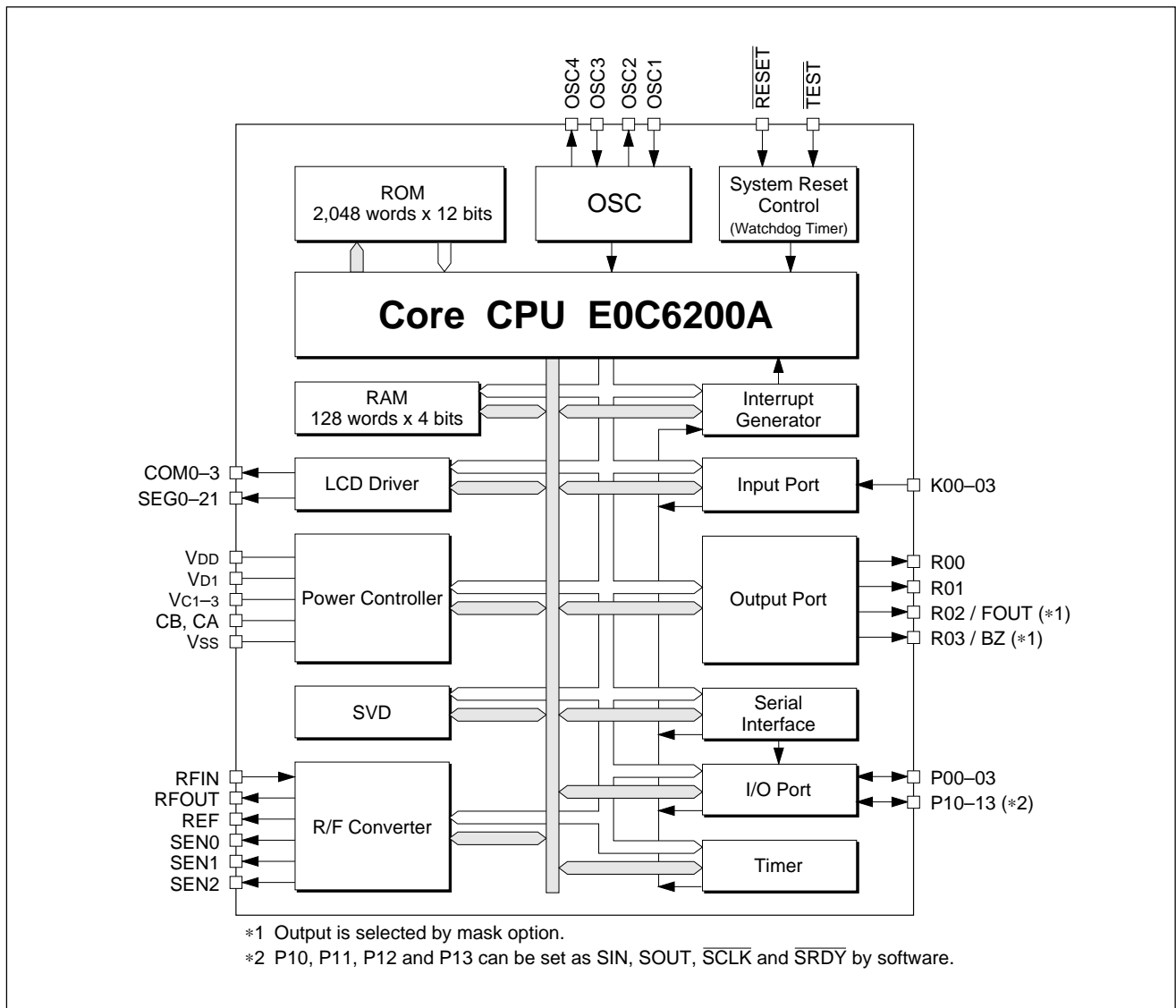


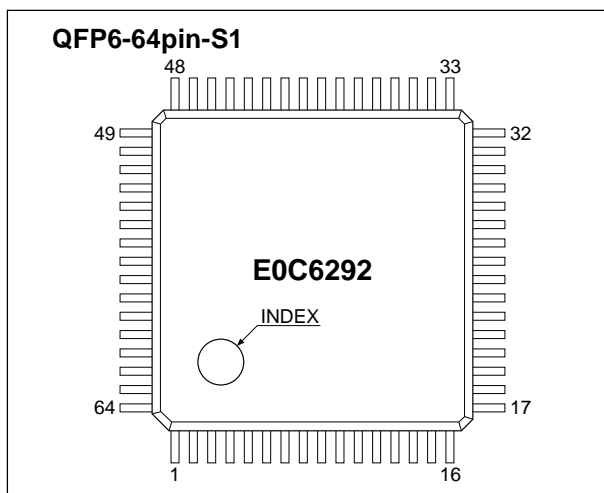


# E0C6292

## ■ BLOCK DIAGRAM

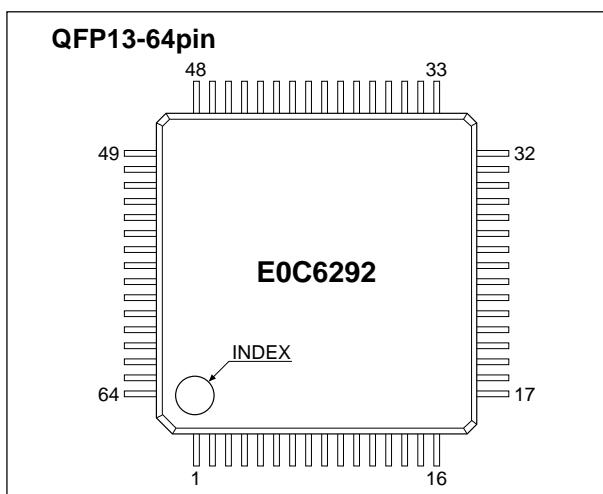


## ■ PIN CONFIGURATION



Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name
1	R03	17	P13	33	Vc2	49	SEG6
2	R02	18	P12	34	Vc1	50	SEG7
3	R01	19	P11	35	Vc3	51	SEG8
4	R00	20	P10	36	CA	52	SEG9
5	K03	21	P03	37	CB	53	SEG10
6	K02	22	P02	38	COM3	54	SEG11
7	K01	23	P01	39	COM2	55	SEG12
8	K00	24	P00	40	COM1	56	SEG13
9	N.C.	25	$\overline{\text{RESET}}$	41	COM0	57	SEG14
10	REF	26	Vss	42	SEG0	58	SEG15
11	SEN0	27	OSC1	43	SEG1	59	SEG16
12	SEN1	28	OSC2	44	SEG2	60	SEG17
13	SEN2	29	VdD	45	SEG3	61	SEG18
14	RFIN	30	OSC4	46	SEG4	62	SEG19
15	RFOUT	31	OSC3	47	SEG5	63	SEG20
16	N.C.	32	Vd1	48	$\overline{\text{TEST}}$	64	SEG21

N.C. : No Connection



Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name
1	R03	17	P13	33	Vc2	49	SEG6
2	R02	18	P12	34	Vc1	50	SEG7
3	R01	19	P11	35	Vc3	51	SEG8
4	R00	20	P10	36	CA	52	SEG9
5	K03	21	P03	37	CB	53	SEG10
6	K02	22	P02	38	COM3	54	SEG11
7	K01	23	P01	39	COM2	55	SEG12
8	K00	24	P00	40	COM1	56	SEG13
9	N.C.	25	RESET	41	COM0	57	SEG14
10	REF	26	Vss	42	SEG0	58	SEG15
11	SEN0	27	OSC1	43	SEG1	59	SEG16
12	SEN1	28	OSC2	44	SEG2	60	SEG17
13	SEN2	29	VDD	45	SEG3	61	SEG18
14	RFIN	30	OSC4	46	SEG4	62	SEG19
15	RFOUT	31	OSC3	47	SEG5	63	SEG20
16	N.C.	32	VD1	48	TEST	64	SEG21

N.C. : No Connection

## PIN DESCRIPTION

Pin name	Pin No.	I/O	Function
VDD	29	(I)	Power supply pin (+)
VSS	26	(I)	Power supply pin (-)
VD1	32	O	Oscillation and internal logic system regulated voltage output pin
Vc1	34	O	LCD system reduced voltage output pin ( $Vc2 \times 1/2$ )
Vc2	33	I	LCD system supply voltage input pin ( $Vc2 = VD1$ or $Vc2 = VDD$ )
Vc3	35	O	LCD system booster voltage output pin ( $Vc1 \times 3/2$ )
CA, CB	36, 37	-	Voltage booster capacitor connecting pin
OSC1	27	I	Crystal oscillation input pin
OSC2	28	O	Crystal oscillation output pin
OSC3	31	I	Ceramic or CR oscillation input pin (selected by mask option)
OSC4	30	O	Ceramic or CR oscillation output pin (selected by mask option)
COM0-COM3	41-38	O	LCD common output pin (drive duty may be selected from 1/2-1/4 by mask option)
SEG0-SEG21	42-47, 49-64	O	LCD segment output pin (DC output may be selected by mask option)
K00-K03	8-5	I	Input port pin
P00-P03	24-21	I/O	I/O port pin
P10-P13	20-17	I/O	I/O port pin (serial I/O port may be selected by software)
R00, R01	4, 3	O	Output port pin
R02	2	O	Output port pin (DC or FOUT output may be selected by mask option)
R03	1	O	Output port pin (DC or BZ output may be selected by mask option)
REF	10	O	Reference resistance connecting pin for R/F converter
SEN0, SEN1, SEN2	11, 12, 13	O	Sensor connecting pin for R/F converter
RFIN	14	I	R/F converter CR oscillation input pin
RFOUT	15	O	R/F converter oscillation frequency output pin
RESET	25	I	Initial reset input pin
TEST	48	I	Testing input pin

## ELECTRICAL CHARACTERISTICS

### Absolute Maximum Ratings

(Vss=0V)

Rating	Symbol	Value	Unit
Supply voltage	VDD	-0.5 to 7.0	V
Input voltage (1)	Vi	-0.5 to VDD+0.5	V
Input voltage (2)	VIosc	-0.5 to VD1+0.5	V
Permissible total output current *1	$\Sigma I_{VDD}$	10	mA
Operating temperature	Topr	-40 to 85	°C
Storage temperature	Tstg	-65 to 150	°C
Soldering temperature / Time	Tsol	260°C, 10sec (lead section)	-
Allowable dissipation *2	Pd	250	mW

\*1 The permissible total output current is the sum total of the current (average current) that simultaneously flows from the output pins (or is drawn in).

\*2 In case of plastic package (QFP6-64pin, QFP13-64pin).

## ● Recommended Operating Conditions

(Ta=-40 to 85°C)

Condition	Symbol	Remark	Min.	Typ.	Max.	Unit	
Supply voltage	VDD	VSS = 0V	When Vc2 is connected to Vd1	2.2	3.0	5.5	V
			When Vc2 is connected to VDD	2.2	3.0	3.6	V
Oscillation frequency	fosc1		-	32.768	-	kHz	
	fosc3	Duty 50±5%	300	1,000	1,300	kHz	

## ● DC Characteristics

(Unless otherwise specified: VSS=0V, VDD=3.0V, fosc1=32.768kHz, Ta=25°C, VD1/VC1-VC3 are internal voltage, C1-C5=0.1μF)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit	
Input threshold voltage	VINH	L→H		1.80	2.25	2.70	V
	VINL	H→L		0.35	0.60	0.85	V
High level input voltage (1)	VIH1			0.8•VDD	VDD	V	
High level input voltage (2)	VIH2			0.9•VDD	VDD	V	
Low level input voltage (1)	VIL1			0	0.2•VDD	V	
Low level input voltage (2)	VIL2			0	0.1•VDD	V	
High level input current (1)	IiH1	VIH1=3.0V		0	0.5	μA	
High level input current (2)	IiH2	VIH2=3.0V		0	0.5	μA	
Low level input current (1)	IiL1	VIL1=VSS, no pull up resistor		-0.5	0	μA	
Low level input current (2)	IiL2	VIL2=VSS, no pull up resistor		-0.5	0	μA	
Low level input current (3)	IiL3	VIL3=VSS, with pull up resistor		-15	-8	-5	μA
Low level input current (4)	IiL4	VIL4=VSS, with pull up resistor		-15	-8	-5	μA
High level output current (1)	IOH1	VOH1=0.9•VDD			-4.0	mA	
High level output current (2)	IOH2	VOH2=0.9•VDD			-1.5	mA	
Low level output current (1)	IOL1	VOL1=0.1•VDD		6		mA	
Low level output current (2)	IOL2	VOL2=0.1•VDD		6		mA	
Common output current	IOH3	VOH3=VDD-0.05V			-3	μA	
	IOL3	VOL3=VC3+0.05V		3		μA	
Segment output current (during LCD output)	IOH4	VOH4=VDD-0.05V			-3	μA	
	IOL4	VOL4=VC3+0.05V		3		μA	
Segment output current (during DC output)	IOH5	VOH5=0.9•VDD			-200	μA	
	IOL5	VOL5=0.1•VDD		200		μA	

## ● Analog Circuit Characteristics and Current Consumption

(Unless otherwise specified: VSS=0V, VDD=3.0V, fosc1=32.768kHz, CG=25pF, Ta=25°C, VD1/VC1-VC3 are internal voltage, C1-C5=0.1μF, CRF=2,200pF, RREF=50kΩ)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit	
LCD drive voltage	VC1	VC2=VDD	Connect 1MΩ load resistor between VSS and VC1 (no panel load)	1/2 VDD×0.9	1/2 VDD	1/2 VDD+0.1	V
		VC2=VD1		1/2 VD1×0.9	1/2 VD1	1/2 VD1+0.1	V
	VC2	VC2=VDD	Connect 1MΩ load resistor between VSS and Vc2 (no panel load)		VDD		V
		VC2=VD1		1.9	2.1	2.3	V
VC3	VC2=VDD	Connect 1MΩ load resistor between VSS and Vc3 (no panel load)	3/2 VDD×0.9	3/2 VDD	3/2 VDD+0.1	V	
	VC2=VD1		3/2 VD1×0.9	3/2 VD1	3/2 VD1+0.1	V	
SVD voltage	VSVD	2.4V (selected by mask option)		2.22	2.4	2.58	V
		2.5V (selected by mask option)		2.30	2.5	2.70	V
		2.6V (selected by mask option)		2.38	2.6	2.82	V
		2.7V (selected by mask option)		2.46	2.7	2.94	V
SVD circuit response time	tsvd				100	μS	
Power current consumption	IOP	During HALT (32kHz)	no panel load		2	6	μA
		During execution (32kHz) *1			5	9	μA
		During execution (1MHz) *1			270	500	μA
		During execution (32kHz) *2			40	120	μA
		During execution (32kHz) *3			11	30	μA

\*1 The R/F converter and SVD circuit are OFF status.

\*2 The R/F converter is ON status. The SVD circuit is OFF status.

\*3 The R/F converter is OFF status. The SVD circuit is ON status.

## ● Oscillation Characteristics

The oscillation characteristics change depending on the conditions (components used, board pattern, etc.). Use the following characteristics as reference values.

### OSC1 crystal oscillation circuit

(Unless otherwise specified:  $V_{SS}=0V$ ,  $V_{DD}=3.0V$ , Crystal: C-002R ( $C_1=35k\Omega$ ),  $C_G=25pF$ ,  $C_D$ =built-in,  $T_a=25^\circ C$ )

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start voltage	$V_{sta}$	$t_{sta} \leq 3sec$	2.2			V
Oscillation stop voltage	$V_{stp}$	$t_{stp} \leq 10sec$	2.2			V
Built-in capacitance (drain)	$C_D$	Including the parasitic capacitance inside the IC		20		pF
Frequency/voltage deviation	$\partial f/\partial V$	$V_{DD} = 2.2$ to $5.5V$			5	ppm
Frequency/IC deviation	$\partial f/\partial IC$		-10		10	ppm
Frequency adjustment range	$\partial f/\partial C_G$	$C_G = 5$ to $25pF$	35			ppm
Harmonic oscillation start voltage	$V_{hho}$	$C_G = 5pF$			7	V
Permitted leak resistance	$R_{leak}$	Between OSC1 terminal and $V_{DD}$ , $V_{SS}$	200			$M\Omega$

### OSC3 ceramic oscillation circuit

(Unless otherwise specified:  $V_{SS}=0V$ ,  $V_{DD}=3.0V$ , Ceramic oscillator: 1MHz,  $C_{Gc}=C_{Dc}=100pF$ ,  $T_a=25^\circ C$ )

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start voltage	$V_{sta}$		-2.2			V
Oscillation start time	$t_{sta}$	$V_{DD}=2.2$ to $5.5V$			3	mS
Oscillation stop voltage	$V_{stp}$		-2.2			V

### OSC3 CR oscillation circuit

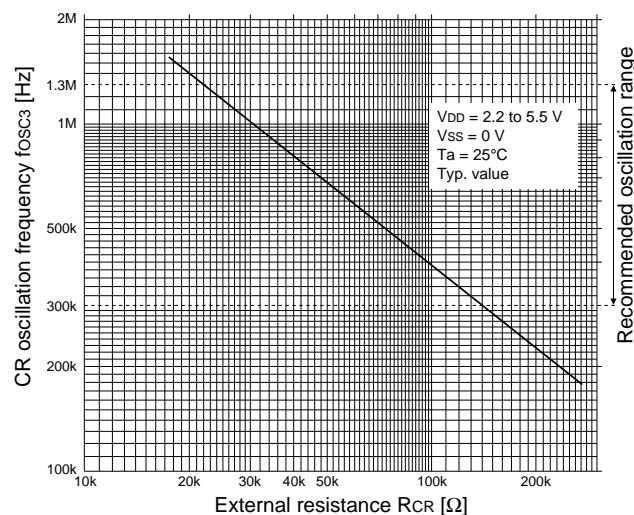
(Unless otherwise specified:  $V_{SS}=0V$ ,  $V_{DD}=3.0V$ ,  $R_{CR}=33k\Omega$ ,  $T_a=25^\circ C$ )

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation frequency dispersion	$f_{osc3}$		-30	(1MHz)	30	%
Oscillation start voltage	$V_{sta}$		-2.2			V
Oscillation start time	$t_{sta}$	$V_{DD}=2.2$ to $5.5V$			3	mS
Oscillation stop voltage	$V_{stp}$		-2.2			V

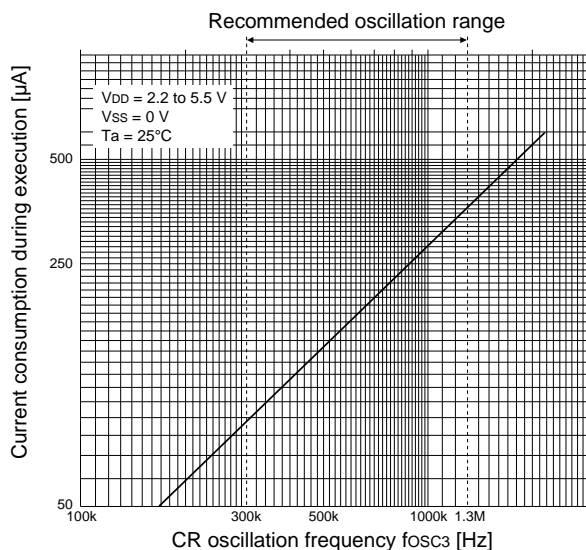
## ● Characteristic Curves

The following characteristics change depending on the conditions (components used, board pattern, etc.). Use the following characteristics as reference values and evaluate the characteristics on the actual product.

### • CR oscillation frequency characteristic - current consumption characteristic



### • CR oscillation frequency - current consumption characteristic

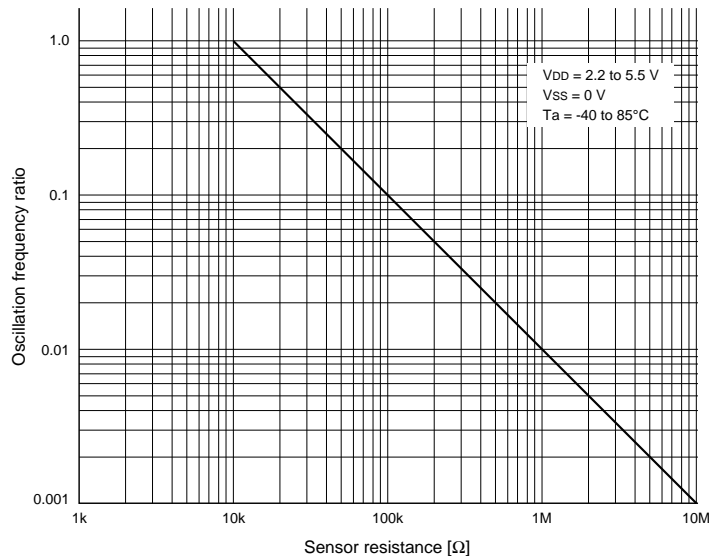


**• R/F converter sensor resistance - oscillation frequency ratio characteristic**

The following figure shows the oscillation frequency ratio (ratio of oscillation frequency by the reference resistance to oscillation frequency by the sensor resistance) when the following elements are connected. (Typ.)

If the R/F conversion uses SEN0, SEN1 or SEN2, both characteristics will be the same.

- Reference resistance (RREF) ..... 10kΩ
- Sensor resistance (RSEN0, RSEN1, RSEN2) ..... 10kΩ to 20MΩ
- Oscillating capacitor (CRF) ..... 2,200pF

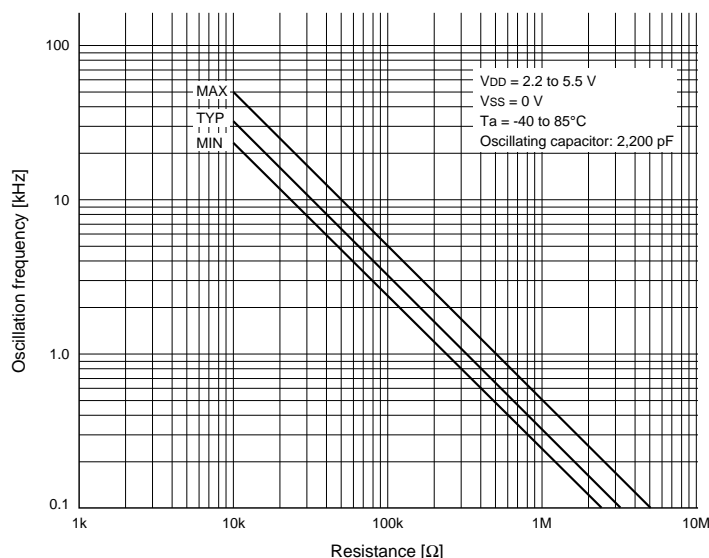


Oscillation frequency ratio - resistance curve

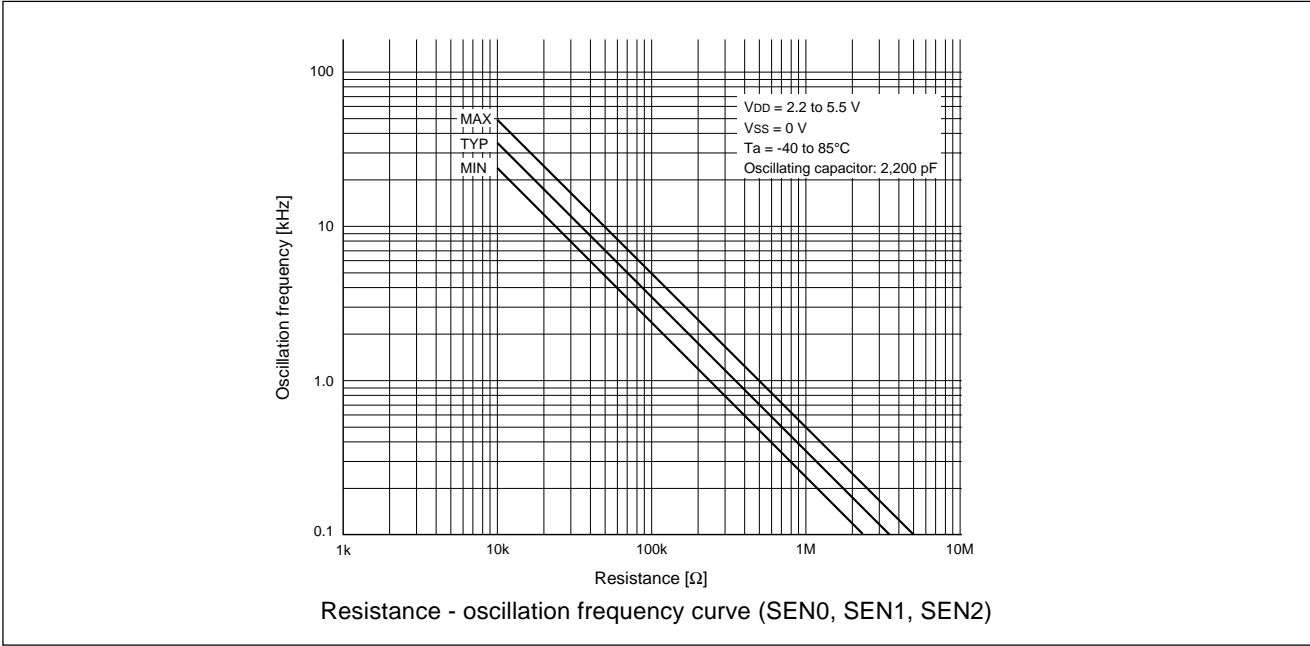
**• R/F converter resistance - oscillation frequency characteristic**

CR oscillation frequency of the R/F converter disperses in each sampling. Therefore, the initial setting value of the measurement counter should be decided after considering the fluctuation margin of the CR oscillation frequency by the reference resistance and sensor resistance to be used for the measurement.

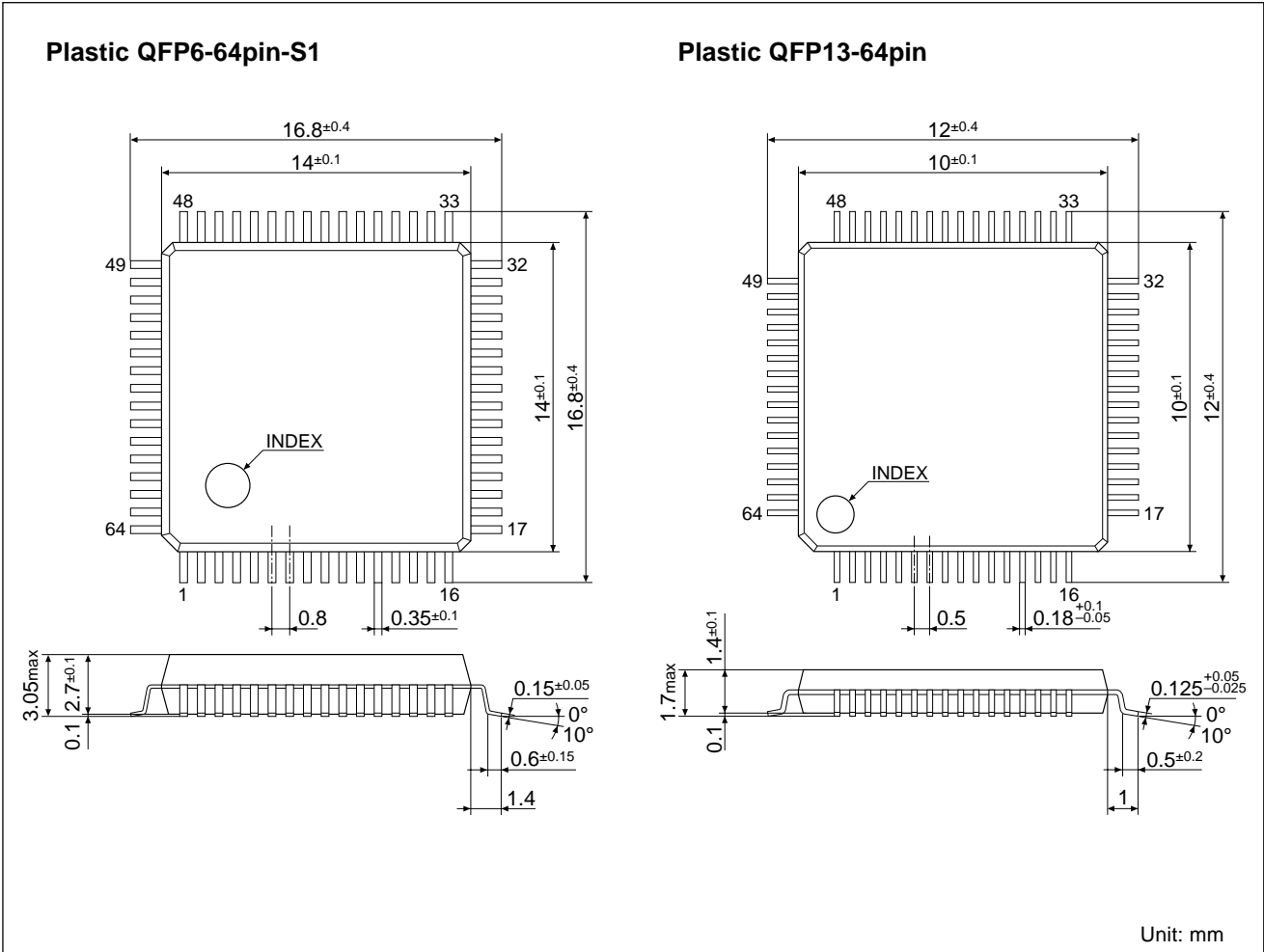
- Note:
- The following curves are characteristic when the oscillating capacitor is 2,200pF.
  - Typical oscillation frequency is characteristic when VDD = 3.0V and Ta = 25°C.



Resistance - oscillation frequency curve (REF)

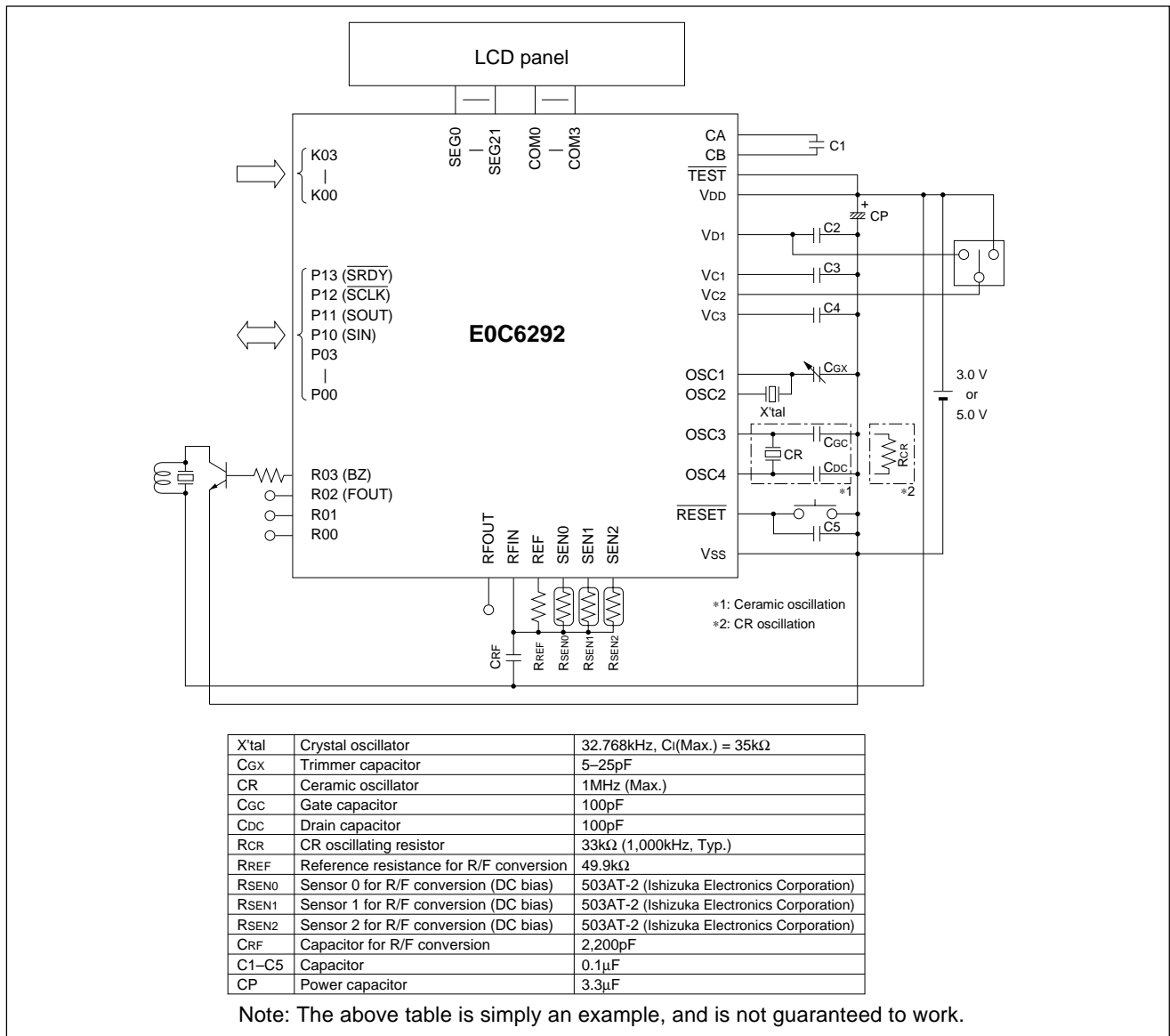


■ PACKAGE DIMENSIONS



# E0C6292

## ■ BASIC EXTERNAL CONNECTION DIAGRAM



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