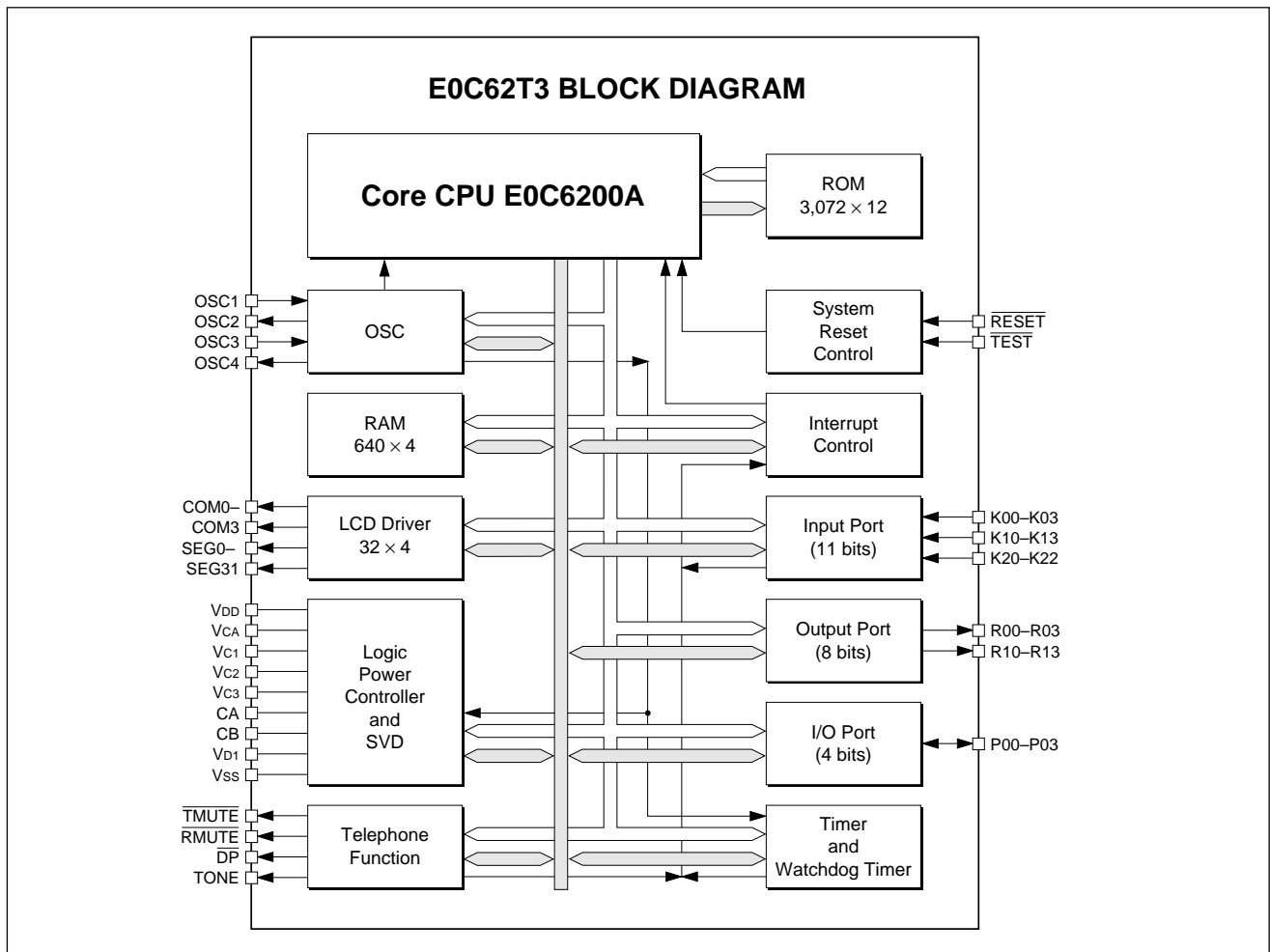


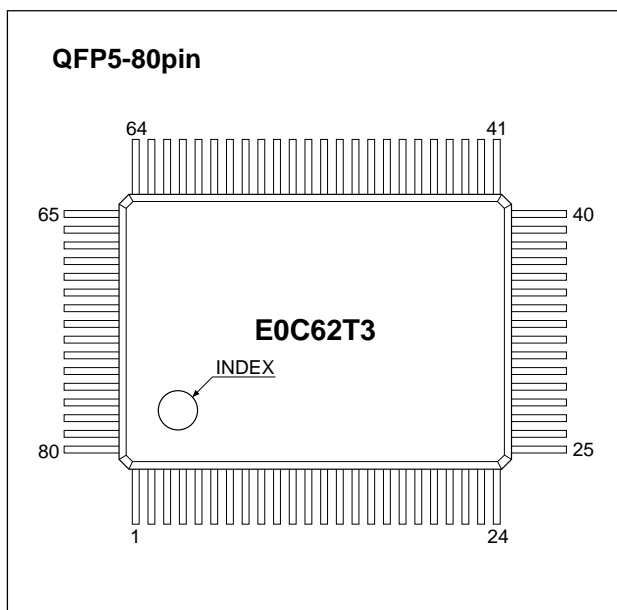


# E0C62T3

## ■ BLOCK DIAGRAM

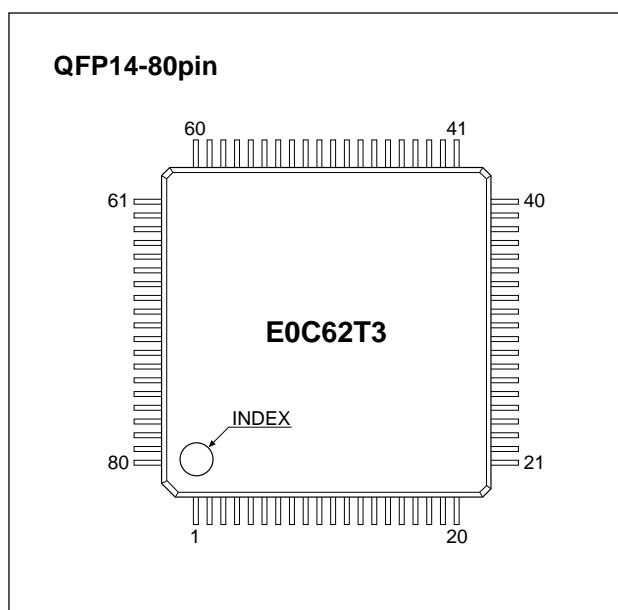


## ■ PIN CONFIGURATION



Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	SEG14	21	P02	41	R12	61	Vc3
2	SEG15	22	P03	42	R13	62	Vc2
3	SEG16	23	TEST	43	RESET	63	COM0
4	SEG17	24	K00	44	VDD	64	COM1
5	SEG18	25	K01	45	RMUTE	65	COM2
6	SEG19	26	K02	46	TMUTE	66	COM3
7	SEG20	27	K03	47	DP	67	SEG0
8	SEG21	28	K10	48	VSS	68	SEG1
9	SEG22	29	K11	49	OSC1	69	SEG2
10	SEG23	30	K12	50	OSC2	70	SEG3
11	SEG24	31	K13	51	OSC3	71	SEG4
12	SEG25	32	K20	52	OSC4	72	SEG5
13	SEG26	33	K21	53	Vd1	73	SEG6
14	SEG27	34	K22	54	TONE	74	SEG7
15	SEG28	35	R00	55	N.C.	75	SEG8
16	SEG29	36	R01	56	N.C.	76	SEG9
17	SEG30	37	R02	57	CA	77	SEG10
18	SEG31	38	R03	58	CB	78	SEG11
19	P00	39	R10	59	Vc1	79	SEG12
20	P01	40	R11	60	VCA	80	SEG13

N.C. : No Connection



Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	N.C.	21	COM0	41	SEG16	61	TEST
2	RESET	22	COM1	42	SEG17	62	K00
3	V <sub>DD</sub>	23	COM2	43	SEG18	63	K01
4	RMUTE	24	COM3	44	SEG19	64	K02
5	TMUTE	25	SEG0	45	SEG20	65	K03
6	DP	26	SEG1	46	SEG21	66	K10
7	V <sub>SS</sub>	27	SEG2	47	SEG22	67	K11
8	OSC1	28	SEG3	48	SEG23	68	K12
9	OSC2	29	SEG4	49	SEG24	69	K13
10	OSC3	30	SEG5	50	SEG25	70	K20
11	OSC4	31	SEG6	51	SEG26	71	K21
12	V <sub>D1</sub>	32	SEG7	52	SEG27	72	K22
13	TONE	33	SEG8	53	SEG28	73	R00
14	N.C.	34	SEG9	54	SEG29	74	R01
15	CA	35	SEG10	55	SEG30	75	R02
16	CB	36	SEG11	56	SEG31	76	R03
17	V <sub>C1</sub>	37	SEG12	57	P00	77	R10
18	V <sub>CA</sub>	38	SEG13	58	P01	78	R11
19	V <sub>C3</sub>	39	SEG14	59	P02	79	R12
20	V <sub>C2</sub>	40	SEG15	60	P03	80	R13

N.C. : No Connection

## PIN DESCRIPTION

Pin name	Pin No.		I/O	Function
	QFP5-80	QFP14-80		
V <sub>DD</sub>	44	3		Power supply (+)
V <sub>SS</sub>	48	7		Power supply (-)
V <sub>D1</sub>	53	12	O	Internal logic system regulated voltage output terminal
V <sub>CA</sub>	60	18	I	LCD system voltage adjustment terminal
V <sub>C1</sub>	59	17	O	LCD system regulated voltage output terminal
V <sub>C2</sub>	62	20	O	LCD system booster voltage output terminal (V <sub>C1</sub> ×2)
V <sub>C3</sub>	61	19	O	LCD system booster voltage output terminal (V <sub>C1</sub> ×3)
CA, CB	57, 58	15, 16	-	LCD system voltage booster capacitor connecting terminals
OSC1	49	8	I	32.768kHz crystal oscillator input terminal
OSC2	50	9	O	32.768kHz crystal oscillator output terminal
OSC3	51	10	I	3.58MHz crystal or ceramic oscillator input terminal (selected by mask option)
OSC4	52	11	O	3.58MHz crystal or ceramic oscillator output terminal (selected by mask option)
K00-K03	24-27	62-65	I	Input terminals
K10-K13	28-31	66-69	I	Input terminals
K20-K22	32-34	70-72	I	Input terminals
P00-P03	19-22	57-60	I/O	I/O terminals (at input mode, pull-up resistors are selected by software)
R00-R03	35-38	73-76	O	Output terminals
R10-R13	39-42	77-80	O	Output terminals (buzzer, hold-line and handfree are selected by software)
SEG0-SEG31	67-18	25-56	O	LCD segment output terminals (DC output is selected by mask option)
COM0-COM3	63-66	21-24	O	LCD common output terminals (1/4, 1/3, 1/2, 1/1 duty programmable)
RESET	43	2	I	Initial setting input terminal
TEST	23	61	I	Test input terminal
RMUTE	45	4	O	Receiver mute output terminal
TMUTE	46	5	O	Transmitter mute output terminal
DP	47	6	O	Dialing pulse output terminal
TONE	54	13	O	DTMF output terminal

# E0C62T3

## ■ ELECTRICAL CHARACTERISTICS

### ● Absolute Maximum Ratings

(V<sub>SS</sub>=0V)

Rating	Symbol	Value	Unit
Supply voltage	V <sub>DD</sub>	-0.5 to 7.0	V
Input voltage (1)	V <sub>I</sub>	-0.5 to V <sub>DD</sub> + 0.3	V
Input voltage (2)	V <sub>I</sub> OSC	-0.5 to V <sub>D1</sub> + 0.3	V
Permissible total output current *1	ΣI <sub>VDD</sub>	10	mA
Operating temperature	T <sub>OP</sub>	-20 to 70	°C
Storage temperature	T <sub>STG</sub>	-65 to 150	°C
Soldering temperature / Time	T <sub>SOL</sub>	260°C, 10sec (lead section)	—
Permissible dissipation *2	P <sub>D</sub>	250	mW

\*1: The permissible total output current is the sum total of the current (average current) that simultaneously flows from the output pins (or is drawn in).

\*2: In case of plastic package (QFP5-80pin, QFP14-80pin).

### ● Recommended Operating Conditions

Condition	Symbol	Remark	Min.	Typ.	Max.	Unit
Supply voltage	V <sub>DD</sub>	V <sub>SS</sub> =0V, OSC1=32kHz, OSC3=stop	1.6	3.0	5.5	V
		V <sub>SS</sub> =0V, when DTMF is used	2.5		5.5	V
Oscillation frequency (1)	f <sub>OSC1</sub>			32.768		kHz
Oscillation frequency (2)	f <sub>OSC3</sub>			3.579545		MHz

### ● DC Characteristics

(Unless otherwise specified: V<sub>SS</sub>=0V, V<sub>DD</sub>=3.0V, f<sub>OSC1</sub>=32.768kHz, T<sub>a</sub>=25°C, V<sub>D1</sub>/V<sub>C1</sub>-V<sub>C3</sub> are internal voltage, C<sub>1</sub>-C<sub>5</sub>=0.1μF)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
High level input voltage (1)	V <sub>IH1</sub>	K00-K03, K10-K13, K20-K22 P00-P03	0.8·V <sub>DD</sub>		V <sub>DD</sub>	V
High level input voltage (2)	V <sub>IH2</sub>	RESET, TEST	0.9·V <sub>DD</sub>		V <sub>DD</sub>	V
Low level input voltage (1)	V <sub>IL1</sub>	K00-K03, K10-K13, K20-K22 P00-P03	0		0.2·V <sub>DD</sub>	V
Low level input voltage (2)	V <sub>IL2</sub>	RESET, TEST	0		0.1·V <sub>DD</sub>	V
High level input current (1)	I <sub>IH1</sub>	V <sub>IH1</sub> =3.0V No pull-up resistor	0		0.5	μA
High level input current (2)	I <sub>IH2</sub>	V <sub>IH2</sub> =3.0V With pull-up resistor			0.5	μA
Low level input current (1)	I <sub>IL1</sub>	V <sub>IL1</sub> =V <sub>SS</sub> No pull-up resistor	-0.5		0	μA
Low level input current (2)	I <sub>IL2</sub>	V <sub>IL1</sub> =V <sub>SS</sub> With pull-up resistor	-20	-10	-5	μA
High level output current (1)	I <sub>OH1</sub>	V <sub>OH1</sub> =0.9·V <sub>DD</sub>			-1	mA
High level output current (2)	I <sub>OH2</sub>	V <sub>OH2</sub> =0.9·V <sub>DD</sub>			-1	mA
Low level output current (1)	I <sub>OL1</sub>	V <sub>OL1</sub> =0.1·V <sub>DD</sub>	3			mA
Low level output current (2)	I <sub>OL2</sub>	V <sub>OL2</sub> =0.1·V <sub>DD</sub>	3			mA
Common output current	I <sub>OH3</sub>	V <sub>OH3</sub> =V <sub>C3</sub> -0.05V			-3	μA
	I <sub>OL3</sub>	V <sub>OL3</sub> =V <sub>SS</sub> +0.05V	3			μA
Segment output current (during LCD output)	I <sub>OH4</sub>	V <sub>OH4</sub> =V <sub>C3</sub> -0.05V			-3	μA
	I <sub>OL4</sub>	V <sub>OL4</sub> =V <sub>SS</sub> +0.05V	3			μA
Segment output current (during DC output)	I <sub>OH5</sub>	V <sub>OH5</sub> =0.9·V <sub>DD</sub>			-300	μA
	I <sub>OL5</sub>	V <sub>OL5</sub> =0.1·V <sub>DD</sub>	300			μA

### ● Analog Circuit Characteristics and Current Consumption

(Unless otherwise specified: V<sub>SS</sub>=0V, V<sub>DD</sub>=3.0V, f<sub>OSC1</sub>=32.768kHz, f<sub>OSC3</sub>=3.579545MHz/crystal, C<sub>G</sub>=25pF, T<sub>a</sub>=25°C, V<sub>D1</sub>/V<sub>C1</sub>-V<sub>C3</sub> are internal voltage, C<sub>1</sub>-C<sub>5</sub>=0.1μF)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
LCD drive voltage	V <sub>C1</sub>	Connect 1MΩ load resistor between V <sub>SS</sub> and V <sub>C1</sub> V <sub>CA</sub> =V <sub>C1</sub> , (without panel load)	0.95	1.05	1.15	V
	V <sub>C2</sub>	Connect 1MΩ load resistor between V <sub>SS</sub> and V <sub>C2</sub> (without panel load)	2·V <sub>C1</sub> ×0.9		2·V <sub>C1</sub> +0.1	V
	V <sub>C3</sub>	Connect 1MΩ load resistor between V <sub>SS</sub> and V <sub>C3</sub> (without panel load)	3·V <sub>C1</sub> ×0.9		3·V <sub>C1</sub> +0.1	V
SVD voltage	V <sub>SVD</sub>		1.65	1.8	1.95	V
SVD circuit response time	t <sub>SVD</sub>				100	μS
Current consumption	I <sub>OP</sub>	During HALT (32kHz)		2	5	μA
		During execution (32kHz) *1	Without panel load	5	12	μA
		During execution (3.58MHz) *1		200	500	μA
		During execution (3.58MHz) *2		1.3	4	mA

\*1: The SVD and DTMF generator are OFF status.

\*2: The DTMF generator is ON status. The SVD is OFF status.

## ● Oscillation Characteristics

The oscillation characteristics change depending on the conditions (components used, board pattern, etc.). Use the following characteristics as reference values.

### OSC1 crystal oscillation circuit

(Unless otherwise specified:  $V_{SS}=0V$ ,  $V_{DD}=3.0V$ , Crystal: C-002R,  $C_1=35k\Omega$ ,  $C_G=25pF$ ,  $C_D$ =built-in,  $T_a=25^\circ C$ )

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start voltage	$V_{sta}$	$t_{sta} \leq 3sec$ ( $V_{DD}$ )	1.6			V
Oscillation stop voltage	$V_{stp}$	$t_{stp} \leq 10sec$ ( $V_{DD}$ )	1.6			V
Built-in capacitance (drain)	$C_D$	Including the parasitic capacity inside the IC		18.5		pF
Frequency/voltage deviation	$\partial f/\partial V$	$V_{DD}=2.0$ to $5.5V$			5	ppm
Frequency/IC deviation	$\partial f/\partial IC$		-10		10	ppm
Frequency adjustment range	$\partial f/\partial C_G$	$C_G=5$ to $25pF$	35			ppm
Harmonic oscillation start voltage	$V_{hho}$	$C_G=5pF$ ( $V_{DD}$ )			5.5	V
Permitted leak resistance *	$R_{leak}$	Between OSC1 and $V_{SS}$	200			$M\Omega$

\*: The shielding plate for OSC1 and OSC2 should be connected to  $V_{SS}$ .

### OSC3 crystal oscillation circuit

(Unless otherwise specified:  $V_{SS}=0V$ ,  $V_{DD}=3.0V$ , Crystal: CA-301,  $C_G=5pF$ ,  $C_D$ =built-in,  $T_a=25^\circ C$ )

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start voltage	$V_{sta}$	$t_{sta} \leq 30msec$ ( $V_{DD}$ )	1.6			V
Oscillation stop voltage	$V_{stp}$	$t_{stp} \leq 10sec$ ( $V_{DD}$ )	1.6			V
Built-in capacitance (drain)	$C_D$	Including the parasitic capacity inside the IC		14		pF
Frequency/voltage deviation	$\partial f/\partial V$	$V_{DD}=2.0$ to $5.5V$			5	ppm
Frequency/IC deviation	$\partial f/\partial IC$		-10		10	ppm
Frequency adjustment range	$\partial f/\partial C_G$	$C_G=5$ to $25pF$		35		ppm
Harmonic oscillation start voltage	$V_{hho}$	$C_G=5pF$ ( $V_{DD}$ )			5.5	V
Permitted leak resistance	$R_{leak}$	Between OSC3 and $V_{DD}$ , $V_{SS}$	200			$M\Omega$

### OSC3 ceramic oscillation circuit

(Unless otherwise specified:  $V_{SS}=0V$ ,  $V_{DD}=3.0V$ , Ceramic oscillator: 3.579545MHz,  $C_{GC}=C_{DC}=30pF$ ,  $R_F=1M\Omega$ ,  $T_a=25^\circ C$ )

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start voltage	$V_{sta}$	( $V_{DD}$ )	2.0			V
Oscillation start time	$t_{sta}$				3	mS
Oscillation stop voltage	$V_{stp}$	( $V_{DD}$ )	2.0			V

## ● Telephone Function Characteristics

(Unless otherwise specified:  $V_{SS}=0V$ ,  $V_{DD}=3.0V$ ,  $f_{osc1}=32.768kHz$ ,  $f_{osc3}=3.579545MHz$ ,  $T_a=25^\circ C$ ,  $V_{D1}/V_{C1}-V_{C3}$  are internal voltage,  $C_1-C_5=0.1\mu F$ )

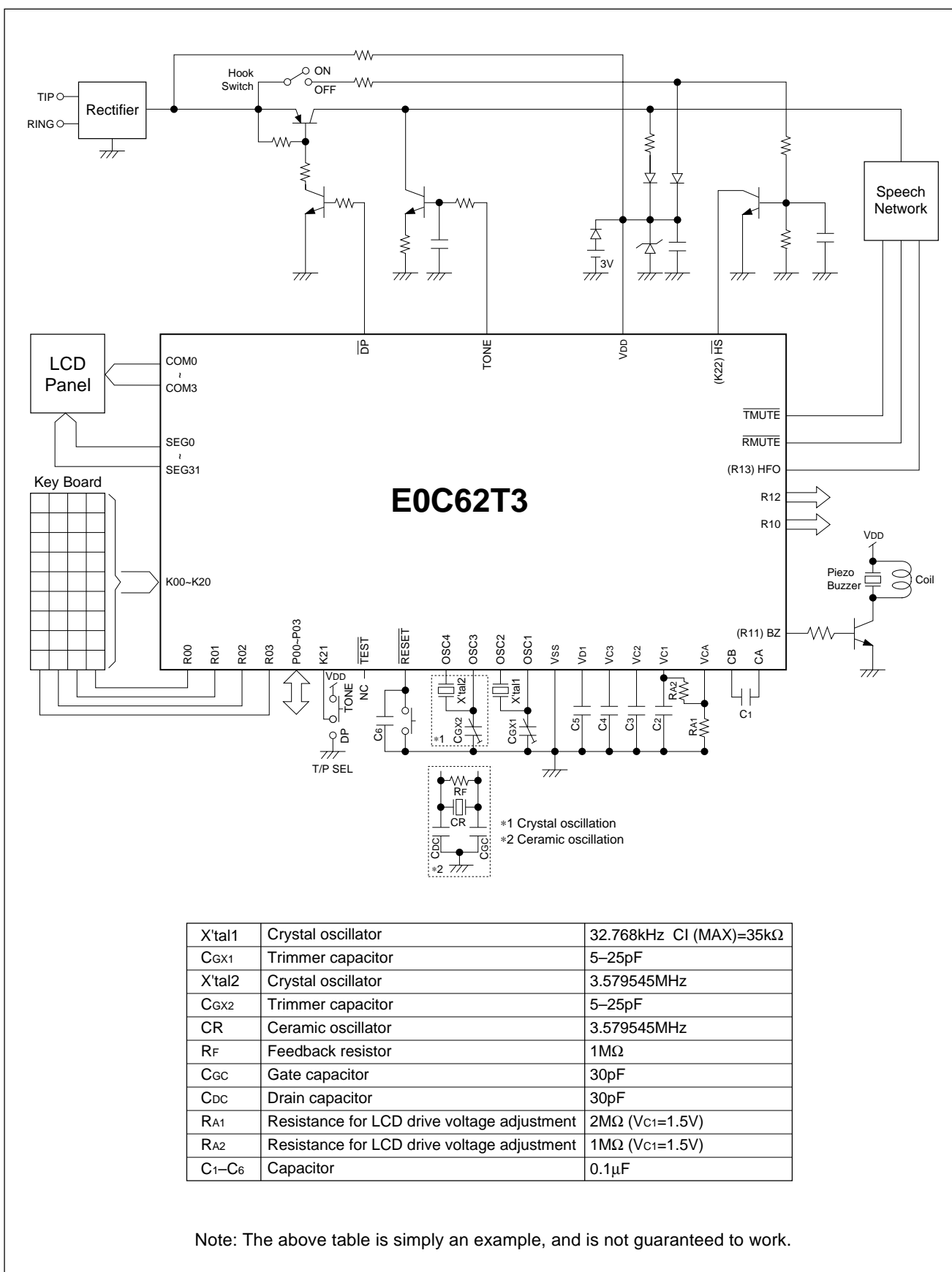
Characteristic	Symbol	Condition				Min.	Typ.	Max.	Unit
		FTS3	FTS2	FTS1	FTS0				
Flash time	$t_{FL}$						-		mS
		0	0	0	1		94		
		0	0	1	0		188		
		0	0	1	1		281		
		0	1	0	0		375		
		0	1	0	1		469		
		0	1	1	0		563		
		0	1	1	1		656		
		1	0	0	0		750		
		1	0	0	1		844		
		1	0	1	0		938		
		1	0	1	1		1031		
		1	1	0	0		1125		
		1	1	0	1		1219		
1	1	1	0		1313				
1	1	1	1		1406				
Flash pause time	$t_{FLP}$					938		mS	

# E0C62T3

(Unless otherwise specified: V<sub>SS</sub>=0V, V<sub>DD</sub>=3.0V, f<sub>osc1</sub>=32.768kHz, f<sub>osc3</sub>=3.579545MHz, T<sub>a</sub>=25°C, V<sub>D1</sub>/V<sub>C1</sub>-V<sub>C3</sub> are internal voltage, C<sub>1</sub>-C<sub>5</sub>=0.1μF)

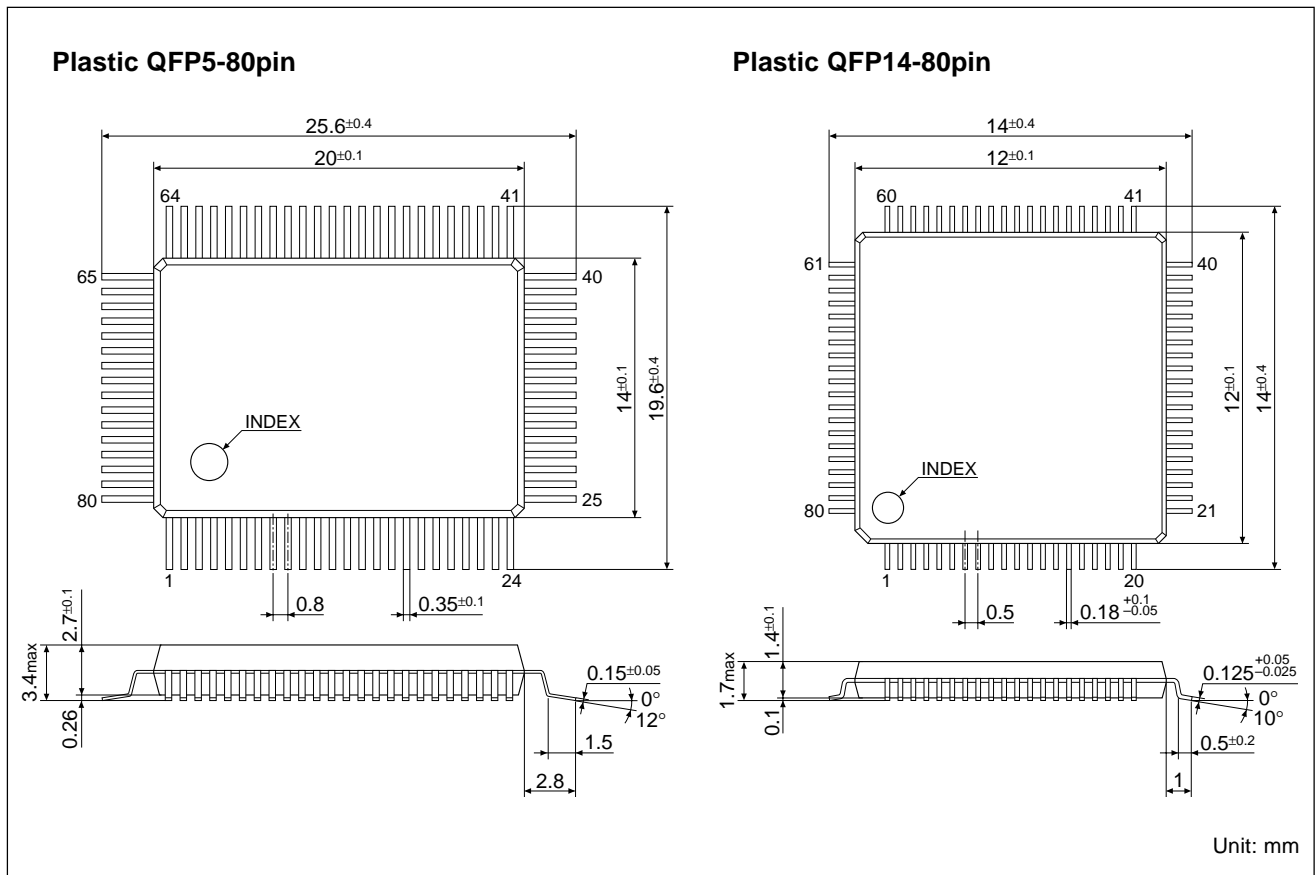
Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Pause time	t <sub>PS</sub>	PTS3 PTS2 PTS1 PTS0		–		sec
		0 0 0 1		1		
		0 0 1 0		2		
		0 0 1 1		3		
		0 1 0 0		4		
		0 1 0 1		5		
		0 1 1 0		6		
		0 1 1 1		7		
		1 0 0 0		8		
		1 0 0 1		9		
		1 0 1 0		10		
		1 0 1 1		11		
		1 1 0 0		12		
		1 1 0 1		13		
1 1 1 0		14				
1 1 1 1		15				
Mute hold time	t <sub>MH</sub>		–	4	–	mS
Inter-digit pause time	t <sub>IDP</sub>	IDP3 IDP2 IDP1 IDP0		–		mS
		0 0 0 1		94		
		0 0 1 0		188		
		0 0 1 1		281		
		0 1 0 0		375		
		0 1 0 1		469		
		0 1 1 0		563		
		0 1 1 1		656		
		1 0 0 0		750		
		1 0 0 1		844		
		1 0 1 0		938		
		1 0 1 1		1031		
		1 1 0 0		1125		
		1 1 0 1		1219		
1 1 1 0		1313				
1 1 1 1		1406				
Make/Break ratio	M/B	Software–selected	–	1/2 2/3	–	–
Dialing pulse rate	DR	Software–selected	–	10 20	–	pps
Make time	t <sub>M</sub>	10pps, M/B=1/2	–	33.2	–	mS
		20pps, M/B=1/2	–	16.6	–	
		10pps, M/B=2/3	–	39.1	–	
		20pps, M/B=2/3	–	19.5	–	
Break time	t <sub>B</sub>	10pps, M/B=1/2	–	66.4	–	mS
		20pps, M/B=1/2	–	33.2	–	
		10pps, M/B=2/3	–	58.6	–	
		20pps, M/B=2/3	–	29.3	–	
Tone output DC level	V <sub>TDC</sub>		–	0.5(V <sub>DD</sub> -V <sub>SS</sub> )	–	V
Single Row tone output amplitude	V <sub>R</sub>	V <sub>DD</sub> =3V, R <sub>L</sub> =10kΩ	–	92	–	mVrms
		V <sub>DD</sub> =5.5V, R <sub>L</sub> =10kΩ	–	168	–	mVrms
Single Column tone output amplitude	V <sub>C</sub>	V <sub>DD</sub> =3V, R <sub>L</sub> =10kΩ	–	122	–	mVrms
		V <sub>DD</sub> =5.5V, R <sub>L</sub> =10kΩ	–	224	–	mVrms
Tone output voltage ratio	dB <sub>CR</sub>	V <sub>DD</sub> =3V, R <sub>L</sub> =10kΩ	–	2.5	–	dB
		V <sub>DD</sub> =5.5V, R <sub>L</sub> =10kΩ	–	2.5	–	dB
Tone load impedance	R <sub>TL</sub>	V <sub>DD</sub> =2–5.5V	7	–	–	kΩ
Total harmonic distortion	THD	V <sub>DD</sub> =2–5.5V, R <sub>L</sub> =10kΩ	–	–	6	%
Tone output frequency	f <sub>ROW1</sub>		–	701.32	–	Hz
	f <sub>ROW2</sub>		–	771.45	–	
	f <sub>ROW3</sub>		–	857.17	–	
	f <sub>ROW4</sub>		–	935.10	–	
	f <sub>COL1</sub>		–	1215.88	–	
	f <sub>COL2</sub>		–	1331.68	–	
	f <sub>COL3</sub>		–	1471.85	–	
	f <sub>COL4</sub>		–	1645.01	–	
Tone duration time	t <sub>TD</sub>		94	–	–	mS
Tone inter-digit pause	t <sub>TIP</sub>		–	94	–	mS
Maximum dial rate	t <sub>T</sub>	t <sub>TD</sub> + t <sub>TIP</sub>	188	–	–	mS

## ■ BASIC EXTERNAL CONNECTION DIAGRAM



# E0C62T3

## ■ PACKAGE DIMENSIONS



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