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EPSON

CMOS 4-BIT SINGLE CHIP MICROCOMPUTER **E0C6244/4A/4C/48**

DEVELOPMENT TOOL MANUAL

ENERGY SAVING EPSON

SEIKO EPSON CORPORATION

E0C6244/4A/4C/48 Development Tool Manual

PREFACE

This manual mainly explains the outline of the development support tool for the 4-bit Single Chip Microcomputers E0C6244, E0C624A, E0C624C and E0C6248.

Refer to the "E0C62 Family Development Tool Reference Manual" for the details (common to all models) of each development support tool. Manuals for hardware development tools are separate, so you should also refer to the below manuals.

Development tools	☞ E0C62 Family Development Tool Reference Manual EVA6248 Manual ICE62R (ICE6200) Hardware Manual
Development procedure	☞ E0C62 Family Technical Guide
Device (E0C6244/4A/4C/48)	☞ E0C6244/4A/4C/48 Technical Manual
Instructions	☞ E0C6200/6200A Core CPU Manual

In this manual, the model name being denoted "44/4A/4C/48" or "4✻". Read this manual, replacing it with "44", "4A", "4C" or "48" that has been used.

CONTENTS

1 COMPOSITION OF DEVELOPMENT SUPPORT TOOL

Here we will explain the composition of the software for the development support tools, developmental envilonment and how to generate the execution disk.

1.1 Configuration of DEV6244/4A/4C/48

The below software are included in the product of the E0C6244/4A/4C/48 development support tool DEV6244/4A/4C/48.

1. Development Tool Management System DMS6200 ..... Menu selection for each software / start-up software
2. Cross Assembler ASM6244/4A/4C/48 ..... Cross assembler for program preparation
3. Function Option Generator FOG6244/4A/4C/48 ..... Function option data preparation program
4. ICE Control Software ICS6244/4A/4C/48 ..... ICE control program
5. Mask Data Checker MDC6244/4A/4C/48 ..... Mask data preparation program

1.2 Developmental Environment

The software product of the development support tool DEV6244/4A/4C/48 operates on the following host systems:

- IBM PC/AT (at least PC-DOS Ver. 2.0)
- NEC PC-9801 Series (at least MS-DOS Ver. 3.1)

When developing the E0C6244/4A/4C/48, the above-mentioned host computer, editor, P-ROM writer, printer, etc. must be prepared by the user in addition to the development tool which is normally supported by Seiko Epson.

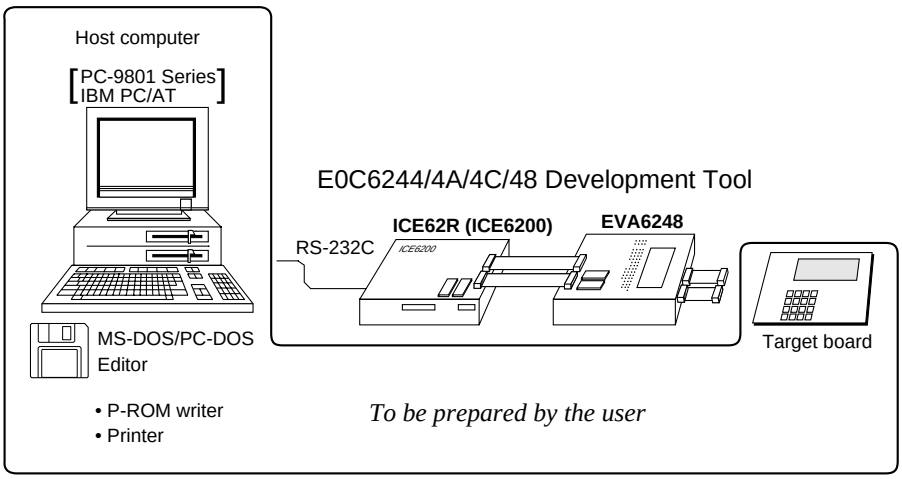

Fig. 1.2.1 System configuration

Note The DEV6244/4A/4C/48 system requires a host computer with a RAM capacity of about 140K bytes. Since the ICE62R (ICE6200) is connected to the host computer with a RS-232C serial interface, adapter board for asynchronous communication will be required depending on the host computer used.

1.3 Development Flow

Figure 1.3.1 shows the development flow through the DEV6244/4A/4C/48.

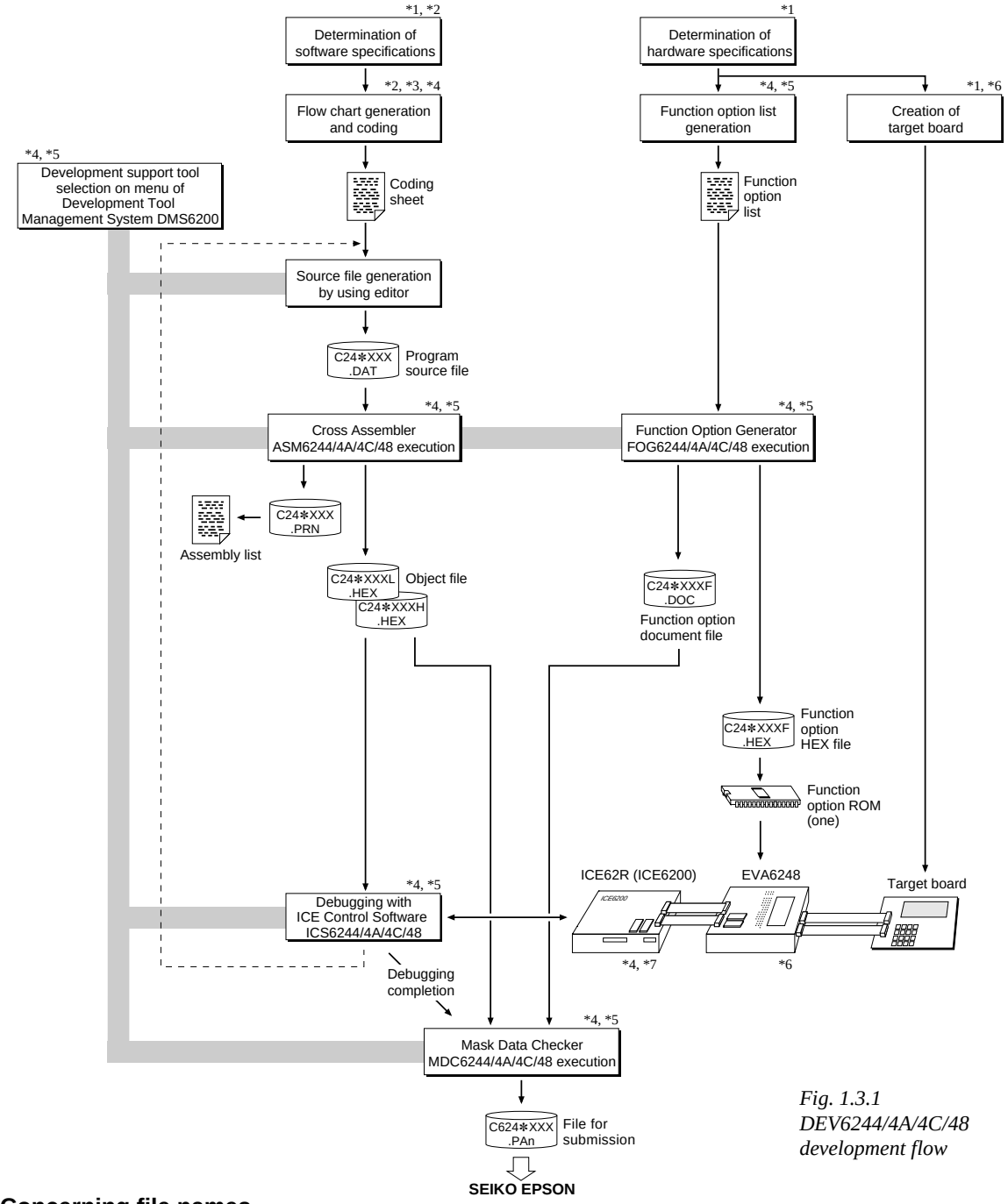

Fig. 1.3.1 DEV6244/4A/4C/48 development flow

Concerning file names

All the input-output file name for the each development support tool commonly use "C24✻XXX" (✻ = 4, A, C or 8). In principle each file should be produced in this manner. Seiko Epson will designate the "XXX" for each customer.

☞ Reference Manual

*1 E0C6244/4A/4C/48 Technical Hardware Manual
*2 E0C6244/4A/4C/48 Technical Software Manual
*3 E0C6200/6200A Core CPU Manual
*4 E0C62 Family Development Tool Reference Manual
*5 E0C6244/4A/4C/48 Development Tool Manual (this manual)
*6 EVA6248 Manual
*7 ICE62R (ICE6200) Hardware Manual

1.4 Production of Execution Disk

Execution files for each software development support tool and batch and parameter files for the ICE62R (ICE6200) are recorded in the DEV6244/4A/4C/48 floppy disk.
The content of the files contained in the DEV6244/4A/4C/48 floppy disk are shown below.

PC-DOS version	MS-DOS version	Contents
ASM6244/4A/4C/48.EXE	ASM6244/4A/4C/48.EXE	Cross Assembler execution file
DMS6200.EXE	DMS6200.EXE	Development Tool Management System execution file
FOG6244/4A/4C/48.EXE	FOG6244/4A/4C/48.EXE	Function Option Generator execution file
ICS6244/4A/4C/48B.BAT	ICS6244/4A/4C/48.BAT	ICE Control Software batch file
ICS6244/4A/4C/48W.EXE	ICS6244/4A/4C/48J.EXE	ICE Control Software execution file
ICS6244/4A/4C/48P.PAR	ICS6244/4A/4C/48P.PAR	ICE Control Software parameter file
MDC6244/4A/4C/48.EXE	MDC6244/4A/4C/48.EXE	Mask Data Checker execution file

- First copy the entire content of this disk using commands such as DISKCOPY then make the execution disk. Carefully conserve the original floppy disk for storage purposes.
  When copying into a hard disk, make a sub-directory with an appropriate name (DEV6244/4A/4C/48, etc.) then copy the content of the floppy disk into that subdirectory using the COPY command.

Example:

Copying into a floppy disk

Insert the original disk into the A drive and the formatted disk to be copied into B drive, then execute the DISKCOPY command.

```
A>DISKCOPY  A:  B:↵
```

Copying into a hard disk (C drive)

Make a subdirectory (example: DEV6244), then insert the original disk into the A drive and execute the COPY command.

```
C\>MD DEV6244↵
C\>CD DEV6244↵
C\DEV6244\>COPY A:*.*↵
```

- Next make a CONFIG.SYS file using Editor or the like. When a CONFIG.SYS has previously been made using a hard disk system, check the setting of the FILES within it. (If there is none add it.)
  Set the number of files to be described in CONFIG.SYS at 10 or more, so that the Mask Data Checker MDC6244/4A/4C/48 will handle many files.

Example:

Setting of FILES (CONFIG.SYS)

```
C\>TYPE  CONFIG.SYS↵
     :
FILES=20
     :
```

Note *The driver for the RS-232C must be included in CONFIG.SYS by the host computer.*

- It is a good idea to copy the editor into the disk to be copied and the subdirectory so you can also select the editor from the DMS6200 menu.

- In "ICS6244/4A/4C/48(B).BAT" the batch process is indicated such that the ICS6244/4A/4C/48J(W).EXE is executed after the execution of the command for the setting of the RS-232C communication parameters. When first executing the ICE Control Software after resetting the host computer, select then activate this batch file from the DMS6200 menu.
  The SPEED (MS-DOS) or MODE (PC-DOS) command is used for setting the RS-232C, so you should copy these commands into the disk to be executed or specify a disk or directory with the command using the PATH command.

RS-232C Setting (PC-DOS version)

```
MODE  COM1:  4800, n, 8, 1, p
```

RS-232C Setting (MS-DOS version)

```
SPEED  R0  9600  B8  PN  S1
```

Note *The DMS6200 prepares a menu from files that are in the current directory. Consequently, be sure to arrange the above mentioned files in the same disk or the same directory.*

2 DEVELOPMENT TOOL MANAGEMENT SYSTEM DMS6200

2.1 DMS6200 Outline

The DMS6200 (Development Tool Management System) is a software which selects the DEV6244/4A/4C/48 software development support tool and the program such as an editor in menu form and starts it.
In this way the various software frequently executed during debugging can be effectively activated.

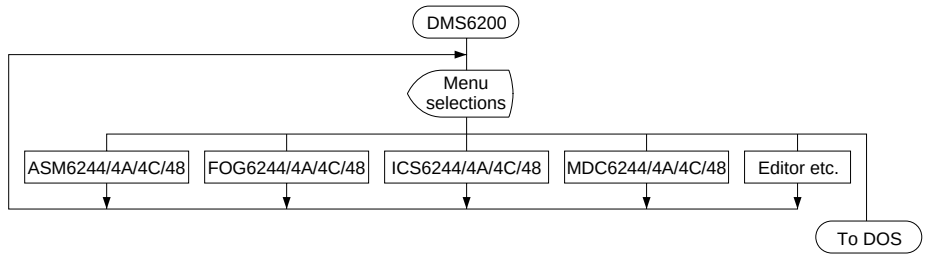

Fig. 2.1.1 DMS6200 execution flow

Refer to the "E0C62 Family Development Tool Reference Manual" for detailes of the operation.

2.2 DMS6200 Quick Reference

■ Starting command

Execution file: **DMS6200.EXE** ***Starting command:*** **DMS6200↵** ↵ *indicates the Return key.*

■ Display examples

```
   *** E0C6200 Development tool Management System. --- Ver 1.0 ***

EEEEEEEEEE   PPPPPPPP        SSSSSSS       OOOOOOOO     NNN      NNN
EEEEEEEEEE   PPPPPPPPPP     SSS   SSSS    OOO    OOO    NNNN     NNN
EEE          PPP     PPP   SSS     SSS   OOO      OOO   NNNNN    NNN
EEE          PPP     PPP    SSS          OOO      OOO   NNNNNN   NNN
EEEEEEEEEE   PPPPPPPPPP      SSSSSS      OOO      OOO   NNN NNN NNN
EEEEEEEEEE   PPPPPPPP          SSSS      OOO      OOO   NNN  NNNNNN
EEE          PPP                SSS     OOO      OOO   NNN   NNNNN
EEE          PPP            SSS   SSS   OOO      OOO   NNN    NNNN
EEEEEEEEEE   PPP            SSSS   SSS    OOO    OOO    NNN     NNN
EEEEEEEEEE   PPP              SSSSSSS       OOOOOOOO     NNN      NN

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                          STRIKE ANY KEY.
```

Start message
When DMS6200 is started, the following message is displayed. For "STRIKE ANY KEY.", press any key to advance the program execution.
To suspend execution, press the "CTRL" and "C" keys together: the sequence returns to the DOS command level.

(In case of DEV6244)

```
      DMS6200 Version 1.0     Copyright(C) SEIKO EPSON CORP. 1991.

1) ASM6244 .EXE
2) FOG6244 .EXE
3) ICS6244B.BAT
4) ICS6244W.EXE
5) MDC6244 .EXE

Input Number ? [1  ]
```

Menu screen (PC-DOS Version)
A list of all executable files will appear on this menu screen.
Input the number of the development support tool you wish to start and then press the "RETURN" key. To return to DOS at this point, press the "ESC" key.

```
      DMS6200 Version 1.0     Copyright(C) SEIKO EPSON CORP. 1991.

 1) C244XXX .DAT
 2) C244XXX .PRN
 3) C244XXX .SEG
 :     :
 7) C6244XXX.PA0

 Input Number ? [1  ]

   Edit > [ASM6244 C244XXX                                        ]
```

Source file selection screen
To starting ASM6244/4A/4C/48, select the source file on this screen. When the source file is selected by number, the edit line enclosed in [ ] will appear; enter the option parameter if necessary. Press the "RETURN" key when input is completed.When starting, press the "RETURN" key twice particularly for the support tools which do not require source files. To return to DOS at this point, press the "ESC" key.

3 CROSS ASSEMBLER ASM6244/4A/4C/48

3.1 ASM6244/4A/4C/48 Outline

The ASM6244/4A/4C/48 cross assembler is an assembler program for generating the machine code used by the E0C6244/4A/4C/48 4-bit, single-chip microcomputers. The Cross Assembler ASM6244/4A/4C/48 will assemble the program source files which have been input by the user's editor and will generate an object file in Intel-Hex format and assembly list file.
In this assembler, program modularization has been made possible through macro definition functions and programming independent of the ROM page structure has been made possible through the auto page set function. In addition, consideration has also been given to precise error checks for program capacity (ROM capacity) overflows, undefined codes and the like, and for debugging of such things as label tables for assembly list files and cross reference table supplements.

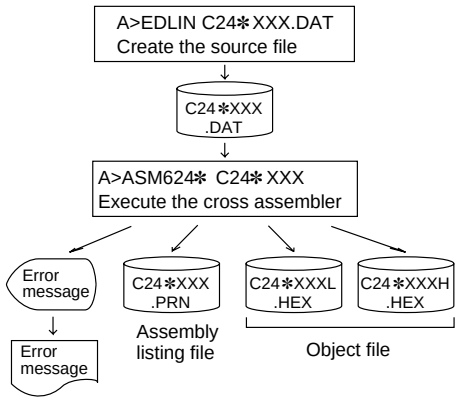

Fig. 3.1.1 ASM6244/4A/4C/48 execution flow

☞ *The format of the source file and its operating method are same as for the E0C62 Family. Refer to the "E0C62 Family Development Tool Reference Manual" for details.*

3.2 E0C6244/4A/4C/48 Restrictions

Note the following when generating a program by the E0C6244/4A/4C/48:

■ E0C6244

- **ROM area**
  The capacity of the E0C6244 ROM is 4K steps (0000H–0FFFH).
  Therefore, the specification range of the memory setting pseudo-instructions and PSET instruction is restricted.

Memory configuration:
Bank: Only bank 0
Page: 16 pages (00H–0FH), each 256 steps

Significant specification range:

ORG	pseudo-instruction:	0000H–0FFFH
PAGE	pseudo-instruction:	00H–0FH
BANK	pseudo-instruction:	Only 0H
PSET	instruction:	00H–0FH

- **RAM area**
  The capacity of the E0C6244 RAM is 590 words (000H–17FH, E00H–E4FH, E80H–ECFH, F00H–F05H, F10H–F15H, F20H–F27H, F30H, F31H, F40H–F42H, F52H–F54H, F60H–F62H and F70H–F7EH, 4 bits/word).
  Memory access is invalid when the unused area of the index register is specified.

Example:

```
LD  A,02H
LD  XP,A
LD  X,40H
```

240H is loaded into the IX register, but an unused area has been specified so that the memory accessible with the IX register (MX) is invalid.

```
LD  B,0FH
LD  YP,B
LD  Y,50H
```

F50H is loaded into the IY register, but an unused area has been specified so that the memory accessible with the IY register (MY) is invalid.

- **Undefined codes**
  The SLP instruction has not been defined in the E0C6244 instruction sets.

■ E0C624A

- **ROM area**
  The capacity of the E0C624A ROM is 6K steps (0000H–17FFH).
  Therefore, the specification range of the memory setting pseudo-instructions and PSET instruction is restricted.

Memory configuration:
Bank: bank 0 and bank 1
Page: bank 0…16 pages (00H–0FH), bank 1…8 pages (00H–07H)

Significant specification range:

ORG	pseudo-instruction:	0000H–17FFH
PAGE	pseudo-instruction:	bank 0…00H–0FH, bank 1…00H–07H
BANK	pseudo-instruction:	0H and 1H
PSET	instruction:	bank 0…00H–0FH, bank 1…00H–07H

- **RAM area**
  The capacity of the E0C624A RAM is 913 words (000H–27FH, E00H–E4FH, E80H–ECFH, F00H–F05H, F10H–F15H, F20H–F27H, F30H, F31H, F40H–F42H, F50H–F54H, F60H–F63H, F70H–F7EH and FC0H–FFFH, 4 bits/word). Memory access is invalid when the unused area of the index register is specified.

Example:

```
LD   A,02H
LD   XP,A
LD   X,80H
```

280H is loaded into the IX register, but an unused area has been specified so that the memory accessible with the IX register (MX) is invalid.

```
LD   B,0AH
LD   YP,B
LD   Y,80H
```

A80H is loaded into the IY register, but an unused area has been specified so that the memory accessible with the IY register (MY) is invalid.

- **Undefined codes**
  The SLP instruction has not been defined in the E0C624A instruction sets.

■ E0C624C

- **ROM area**
  The capacity of the E0C624C ROM is 5K steps (0000H–13FFH).
  Therefore, the specification range of the memory setting pseudo-instructions and PSET instruction is restricted.

Memory configuration:
Bank: bank 0 and bank 1
Page: bank 0…16 pages (00H–0FH), bank 1…4 pages (00H–03H)

Significant specification range:

ORG	pseudo-instruction:	0000H–13FFH
PAGE	pseudo-instruction:	00H–0FH
BANK	pseudo-instruction:	0H and 1H
PSET	instruction:	00H–0FH

- **RAM area**
  The capacity of the E0C624C RAM is 1,469 words (000H–47FH, E00H–E65H, E80H–EE5H, F00H–F05H, F10H–F15H, F20H–F27H, F30H, F31H, F40H–F42H, F50H–F54H, F60H–F63H, F70H–F7EH and FC0H–FFFH, 4 bits/word). Memory access is invalid when the unused area of the index register is specified.

Example:

```
LD   A,04H
LD   XP,A
LD   X,80H
```

480H is loaded into the IX register, but an unused area has been specified so that the memory accessible with the IX register (MX) is invalid.

```
LD   B,0AH
LD   YP,B
LD   Y,80H
```

A80H is loaded into the IY register, but an unused area has been specified so that the memory accessible with the IY register (MY) is invalid.

- **Undefined codes**
  The SLP instruction has not been defined in the E0C624C instruction sets.

■ E0C6248

• ROM area

The capacity of the E0C6248 ROM is 8K steps (0000H–1FFFH).
Therefore, the specification range of the memory setting pseudo-instructions and PSET instruction is restricted.

• RAM area

The capacity of the E0C6248 RAM is 1,085 words (000H–2FFH, E00H–E65H, E80H–EE5H, F00H–F05H, F10H–F15H, F20H–F27H, F30H, F31H, F40H–F42H, F50H–F54H, F60H–F63H, F70H–F7EH and FC0H–FFFH, 4 bits/word). Memory access is invalid when the unused area of the index register is specified.

Memory configuration:

Bank: bank 0 and bank 1
Page: bank 0…16 pages (00H–0FH), bank 1…16 pages (00H–0FH)

Significant specification range:

ORG	pseudo-instruction:	0000H–1FFFH
PAGE	pseudo-instruction:	00H–0FH
BANK	pseudo-instruction:	0H and 1H
PSET	instruction:	00H–0FH

Example:

```
LD    A,03H
LD    XP,A
LD    X,80H
```

380H is loaded into the IX register, but an unused area has been specified so that the memory accessible with the IX register (MX) is invalid.

```
LD    B,0AH
LD    YP,B
LD    Y,80H
```

A80H is loaded into the IY register, but an unused area has been specified so that the memory accessible with the IY register (MY) is invalid.

• Undefined codes

The SLP instruction has not been defined in the E0C6248 instruction sets.

3.3 ASM6244/4A/4C/48 Quick Reference

■ Starting command and input/output files

_ indicates a blank.
↵ indicates the Return key.
A parameter enclosed by [ ] can be omitted.
4✻ indicates the model name (44, 4A, 4C or 48).

Execution file: ASM6244/4A/4C/48.EXE

Starting command: **ASM624✻_ [drive-name:] source-file-name [.shp] _ [-N]↵**

Option:
- .shp Specifies the file I/O drives.
  - s Specifies the drive from which the source file is to be input. (A–P, @)
  - h Specifies the drive to which the object file is to be output. (A–P, @, Z)
  - p Specifies the drive to which the assembly listing file is to be output. (A–P, @, Z)
    @: Current drive, Z: File is not generated
- -N The code (FFH) in the undefined area of program memory is not created.

Input file: C24✻XXX.DAT (Source file)

Output file:
C24✻XXXL.HEX (Object file, low-order)
C24✻XXXH.HEX (Object file, high-order)
C24✻XXX.PRN (Assembly listing file)

■ Display example (In case of ASM6244)

```
          *** E0C6244 CROSS ASSEMBLER. --- Ver 2.00 ***

EEEEEEEEEE   PPPPPPPP        SSSSSSS       OOOOOOOO     NNN     NNN
EEEEEEEEEE   PPPPPPPPPP     SSS    SSSS    OOO    OOO    NNNN    NNN
EEE          PPP     PPP   SSS     SSS   OOO      OOO   NNNNN   NNN
EEE          PPP     PPP    SSS          OOO      OOO   NNNNNN  NNN
EEEEEEEEEE   PPPPPPPPPP      SSSSSS      OOO      OOO   NNN NNN NNN
EEEEEEEEEE   PPPPPPPP           SSSS     OOO      OOO   NNN  NNNNNN
EEE          PPP                 SSS    OOO      OOO   NNN   NNNNN
EEE          PPP           SSS    SSS   OOO      OOO   NNN    NNNN
EEEEEEEEEE   PPP           SSSS   SSS    OOO    OOO    NNN     NNN
EEEEEEEEEE   PPP            SSSSSSS       OOOOOOOO     NNN      NN

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          SOURCE FILE NAME IS " C244XXX.DAT "

          THIS SOFTWARE MAKES NEXT FILES.

             C244XXXH.HEX  ...  HIGH BYTE OBJECT FILE.
             C244XXXL.HEX  ...  LOW BYTE OBJECT FILE.
             C244XXX .PRN  ...  ASSEMBLY LIST FILE.

DO YOU NEED AUTO PAGE SET? (Y/N) Y                              ...(1)

DO YOU NEED CROSS REFERENCE TABLE? (Y/N) Y                      ...(2)
```

When ASM6244/4A/4C/48 is started, the start-up message is displayed.
At (1), select whether or not the auto-page-set function will be used.
Use ..... Y↵
Not use ..... N↵
If the assembly listing file output is specified, message (2) is displayed. At this stage, cross-reference table generation may be selected.
Generating ..... Y↵
Not generating ..... N↵
When the above operation is completed, ASM6244/4A/4C/48 assembles the source file.
To suspend execution, press the "CTRL" and "C" keys together at stage (1) or (2).

■ Operators

Arithmetic operators		Logical operators	
+a	Monadic positive	a_AND_b	Logical product
-a	Monadic negative	a_OR_b	Logical sum
a+b	Addition	a_XOR_b	Exclusive logical sum
a-b	Subtraction	NOT_a	Logical negation
a*b	Multiplication	Relational operators	
a/b	Division	a_EQ_b	True when a is equal to b
a_MOD_b	Remainder of a/b	a_NE_b	True when a is not equal to b
a_SHL_b	Shifts a b bits to the left	a_LT_b	True when a is less than b
a_SHR_b	Shifts a b bits to the right	a_LE_b	True when a is less than or equal to b
HIGH_a	Separates the high-order eight bits from a	a_GT_b	True when a is greater than b
LOW_a	Separates the low-order eight bits from a	a_GE_b	True when a is greater than or equal to b

■ Pseudo-instructions

Pseudo-instruction	Meaning	Example of Use
EQU (Equation)	To allocate data to label	`ABC EQU 9` `BCD EQU ABC+1`
SET (Set)	To allocate data to label (data can be changed)	`ABC SET 0001H` `ABC SET 0002H`
DW (Define Word)	To define ROM data	`ABC DW 'AB'` `BCD DW 0FFBH`
ORG (Origin)	To define location counter	`ORG 100H` `ORG 256`
BANK (Bank)	To define boundary of bank	`BANK 0` `BANK 1H`
PAGE (Page)	To define boundary of page	`PAGE 1H` `PAGE 11`
SECTION (Section)	To define boundary of section	`SECTION`
END (End)	To terminate assembly	`END`

MACRO (Macro)	To define macro	`CHECK MACRO DATA`
		`LOCAL LOOP`
		`LOOP CP MX,DATA`
		`JP NZ,LOOP`
		`ENDM`
		
		`CHECK 1`

LOCAL (Local)	To make local specification of label during macro definition	
ENDM (End Macro)	To end macro definition	

■ Error messages

Error message	Explanation
S (Syntax Error)	An unrecoverable syntax error was encountered.
U (Undefined Error)	The label or symbol of the operand has not been defined.
M (Missing Label)	The label field has been omitted.
O (Operand Error)	A syntax error was encountered in the operand, or the operand could not be evaluated.
P (Phase Error)	The same label or symbol was defined more than once.
R (Range Error)	• A statement exceeded a page boundary although its location was not specified. • The location counter value exceeded the upper limit of the program memory, or a location exceeding the upper limit was specified. • A value greater than that which the number of significant digits of the operand will accommodate was specified.
! (Warning)	• Memory areas overlapped because of a "PAGE" or "ORG" pseudo-instruction or both.
FILE NAME ERROR	The source file name was longer than 8 characters.
FILE NOT PRESENT	The specified source file was not found.
DIRECTORY FULL	No space was left in the directory of the specified disk.
FATAL DISK WRITE ERROR	The file could not be written to the disk.
LABEL TABLE OVERFLOW	The number of defined labels and symbols exceeded the label table capacity (4000).
CROSS REFERENCE TABLE OVERFLOW	The label/symbol reference count exceeded the cross-reference table capacity (only when the cross-reference table is generated).

4 FUNCTION OPTION GENERATOR FOG6244/4A/4C/48

4.1 FOG6244/4A/4C/48 Outline

With the 4-bit single-chip E0C6244/4A/4C/48 microcomputers, the customer may select the hardware options. By modifying the mask patterns of the E0C6244/4A/4C/48 according to the selected options, the system can be customized to meet the specifications of the target system.
The Function Option Generator FOG6244/4A/4C/48 is a software tool for generating data files used to generate mask patterns. It enables the customer to interactively select and specify pertinent items for each hardware option. From the data file created with FOG6244/4A/4C/48, the E0C6244/4A/4C/48 mask pattern is automatically generated by a general purpose computer.
The HEX file for the evaluation board (EVA6248) hardware option ROM is simultaneously generated with the data file.

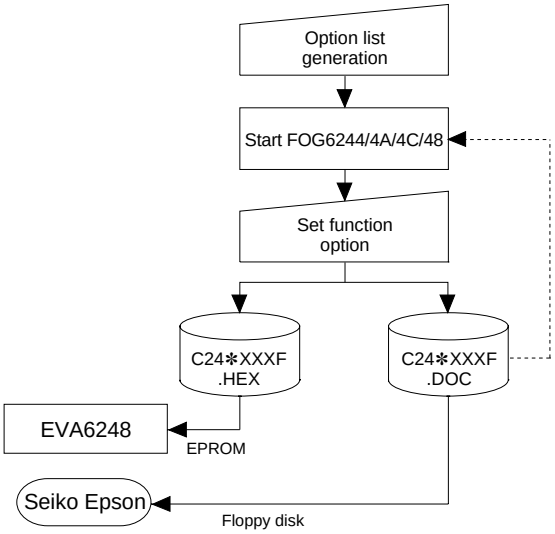

Fig. 4.1.1 FOG6244/4A/4C/48 execution flow

☞ *The operating method is same as for the E0C62 Family. Refer to the "E0C62 Family Development Tool Reference Manual" for details.*

4.2 E0C6244 Option List

Multiple specifications are available in each option item as indicated in the Option List. Using "4.5 E0C6244 Option Specifications and Selection Message" as reference, select the specifications that meet the target system. Be sure to record the specifications for unused ports too, according to the instructions provided.

44-1. OSC1 OSCILLATOR

☐ 1. Crystal ☐ 2. CR

44-2. OSC3 OSCILLATOR

☐ 1. CR ☐ 2. Ceramic

44-3. MULTIPLE KEY ENTRY RESET

☐ 1. Not Use
☐ 2. Use K00, K01
☐ 3. Use K00, K01, K02
☐ 4. Use K00, K01, K02, K03

44-4. INPUT PORTS PULL UP RESISTOR

- K00 ..... ☐ 1. With Resistor ☐ 2. Gate Direct
- K01 ..... ☐ 1. With Resistor ☐ 2. Gate Direct
- K02 ..... ☐ 1. With Resistor ☐ 2. Gate Direct
- K03 ..... ☐ 1. With Resistor ☐ 2. Gate Direct
- K10 ..... ☐ 1. With Resistor ☐ 2. Gate Direct
- K11 ..... ☐ 1. With Resistor ☐ 2. Gate Direct
- K12 ..... ☐ 1. With Resistor ☐ 2. Gate Direct
- K13 ..... ☐ 1. With Resistor ☐ 2. Gate Direct

(E0C6244 option list)

44-5. OUTPUT PORTS OUTPUT SPECIFICATION

- R20–R23 ..... ☐ 1. Complementary ☐ 2. Nch-OpenDrain
- R30 ..... ☐ 1. Complementary ☐ 2. Nch-OpenDrain
- R31 ..... ☐ 1. Complementary ☐ 2. Nch-OpenDrain
- R32 ..... ☐ 1. Complementary ☐ 2. Nch-OpenDrain

44-6. R33 OUTPUT PORT SPECIFICATION

- OUTPUT SPECIFICATION ..... ☐ 1. Complementary ☐ 2. Nch-OpenDrain
- OUTPUT TYPE ..... ☐ 1. DC (PTCLK) Output ☐ 2. /SRDY Output
- OUTPUT CONTROL ..... ☐ 1. 3 States ☐ 2. 2 States

44-7. R40 OUTPUT PORT SPECIFICATION

- OUTPUT SPECIFICATION ..... ☐ 1. Complementary ☐ 2. Nch-OpenDrain
- OUTPUT TYPE ..... ☐ 1. DC Output
  ☐ 2. CL-16 (For SED1521FAA)
  ☐ 3. CL-8 (For SED1521FAA)
  ☐ 4. /FOUT 256 [Hz]
  ☐ 5. /FOUT 512 [Hz]
  ☐ 6. /FOUT 1024 [Hz]
  ☐ 7. /FOUT 2048 [Hz]
  ☐ 8. /FOUT 4096 [Hz]
  ☐ 9. /FOUT 8192 [Hz]
  ☐ 10. /FOUT 16384 [Hz]
  ☐ 11. /FOUT 32768 [Hz]
  ☐ 12. /FOUT OSC3

44-8. R41 OUTPUT PORT SPECIFICATION

- OUTPUT SPECIFICATION ..... ☐ 1. Complementary ☐ 2. Nch-OpenDrain
- OUTPUT TYPE ..... ☐ 1. DC Output ☐ 2. FR (FOR SED1521FAA)

44-9. R42 OUTPUT PORT SPECIFICATION

- OUTPUT SPECIFICATION ..... ☐ 1. Complementary ☐ 2. Nch-OpenDrain
- OUTPUT TYPE ..... ☐ 1. DC Output
  ☐ 2. Buzzer Inverted Output (R43 Control)
  ☐ 3. FOUT 256 [Hz]
  ☐ 4. FOUT 512 [Hz]
  ☐ 5. FOUT 1024 [Hz]
  ☐ 6. FOUT 2048 [Hz]
  ☐ 7. FOUT 4096 [Hz]
  ☐ 8. FOUT 8192 [Hz]
  ☐ 9. FOUT 16384 [Hz]
  ☐ 10. FOUT 32768 [Hz]
  ☐ 11. FOUT OSC3

44-10. R43 OUTPUT PORT SPECIFICATION

- OUTPUT SPECIFICATION ..... ☐ 1. Complementary ☐ 2. Nch-OpenDrain
- OUTPUT TYPE ..... ☐ 1. DC Output ☐ 2. Buzzer Output

44-11. I/O PORTS OUTPUT SPECIFICATION

- P00–P03 ..... ☐ 1. Complementary ☐ 2. Nch-OpenDrain
- P10–P13 ..... ☐ 1. Complementary ☐ 2. Nch-OpenDrain
- P20 ..... ☐ 1. Complementary ☐ 2. Nch-OpenDrain
- P21 ..... ☐ 1. Complementary ☐ 2. Nch-OpenDrain
- P22 ..... ☐ 1. Complementary ☐ 2. Nch-OpenDrain
- P23 ..... ☐ 1. Complementary ☐ 2. Nch-OpenDrain

(E0C6244 option list)

44-12. P20–P23 I/O PORTS OUTPUT TYPE

- P20 ..... ☐ 1. I/O Port ☐ 2. Output Port
- P21 ..... ☐ 1. I/O Port ☐ 2. Output Port
- P22 ..... ☐ 1. I/O Port ☐ 2. Output Port
- P23 ..... ☐ 1. I/O Port ☐ 2. Output Port

44-13. SIN PULL UP RESISTOR

☐ 1. With Resistor ☐ 2. Gate Direct

44-14. SOUT OUTPUT SPECIFICATION

☐ 1. Complementary ☐ 2. Nch-OpenDrain

44-15. $\overline{\text{SCLK}}$ SPECIFICATION

- PULL UP RESISTOR ..... ☐ 1. With Resistor ☐ 2. Gate Direct
- OUTPUT SPECIFICATION ..... ☐ 1. Complementary ☐ 2. Nch-OpenDrain

44-16. SIO DATA PERMUTATION

☐ 1. MSB First ☐ 2. LSB First

44-17. LCD POWER VOLTAGE MODE

☐ 1. Internal Voltage ☐ 2. External Voltage

4.3 E0C624A Option List

Multiple specifications are available in each option item as indicated in the Option List. Using "4.6 E0C624A Option Specifications and Selection Message" as reference, select the specifications that meet the target system. Be sure to record the specifications for unused ports too, according to the instructions provided.

4A-1. OSC3 OSCILLATOR

☐ 1. CR ☐ 2. Ceramic

4A-2. MULTIPLE KEY ENTRY RESET

☐ 1. Not Use
☐ 2. Use K00, K01
☐ 3. Use K00, K01, K02
☐ 4. Use K00, K01, K02, K03

4A-3. INPUT PORTS PULL UP RESISTOR

- K00 ..... ☐ 1. With Resistor ☐ 2. Gate Direct
- K01 ..... ☐ 1. With Resistor ☐ 2. Gate Direct
- K02 ..... ☐ 1. With Resistor ☐ 2. Gate Direct
- K03 ..... ☐ 1. With Resistor ☐ 2. Gate Direct
- K10 ..... ☐ 1. With Resistor ☐ 2. Gate Direct
- K11 ..... ☐ 1. With Resistor ☐ 2. Gate Direct
- K12 ..... ☐ 1. With Resistor ☐ 2. Gate Direct
- K13 ..... ☐ 1. With Resistor ☐ 2. Gate Direct

4A-4. OUTPUT PORTS OUTPUT SPECIFICATION

- R00–R03 ..... ☐ 1. Complementary ☐ 2. Nch-OpenDrain
- R10–R13 ..... ☐ 1. Complementary ☐ 2. Nch-OpenDrain
- R20–R22 ..... ☐ 1. Complementary ☐ 2. Nch-OpenDrain
- R23 ..... ☐ 1. Complementary ☐ 2. Nch-OpenDrain
- R30 ..... ☐ 1. Complementary ☐ 2. Nch-OpenDrain
- R31 ..... ☐ 1. Complementary ☐ 2. Nch-OpenDrain
- R32 ..... ☐ 1. Complementary ☐ 2. Nch-OpenDrain

(E0C624A option list)

4A-5. OUTPUT PORTS OUTPUT TYPE

- R00–R03 ..... ☐ 1. DC Output ☐ 2. Address Bus (A0–A3)
- R10–R13 ..... ☐ 1. DC Output ☐ 2. Address Bus (A4–A7)
- R20–R22 ..... ☐ 1. DC Output ☐ 2. Address Bus (A8–A10)
- R23 ..... ☐ 1. DC Output ☐ 2. Address Bus (A11)
- R30 ..... ☐ 1. DC Output ☐ 2. Address Bus (A12)
- R31 ..... ☐ 1. DC Output ☐ 2. Address Bus (A13)
  ☐ 3. Write (/WR)
- R32 ..... ☐ 1. DC Output ☐ 2. Read (/RD)

4A-6. R33 OUTPUT PORT SPECIFICATION

- OUTPUT SPECIFICATION ..... ☐ 1. Complementary ☐ 2. Nch-OpenDrain
- OUTPUT TYPE ..... ☐ 1. DC (PTCLK) Output ☐ 2. /SRDY Output
- OUTPUT CONTROL ..... ☐ 1. 3 States ☐ 2. 2 States

4A-7. R40 OUTPUT PORT SPECIFICATION

- OUTPUT SPECIFICATION ..... ☐ 1. Complementary ☐ 2. Nch-OpenDrain
- OUTPUT TYPE ..... ☐ 1. DC Output
  ☐ 2. CL-16 (For SED1521FAA)
  ☐ 3. CL-8 (For SED1521FAA)
  ☐ 4. /FOUT 256 [Hz]
  ☐ 5. /FOUT 512 [Hz]
  ☐ 6. /FOUT 1024 [Hz]
  ☐ 7. /FOUT 2048 [Hz]
  ☐ 8. /FOUT 4096 [Hz]
  ☐ 9. /FOUT 8192 [Hz]
  ☐ 10. /FOUT 16384 [Hz]
  ☐ 11. /FOUT 32768 [Hz]
  ☐ 12. /FOUT OSC3

4A-8. R41 OUTPUT PORT SPECIFICATION

- OUTPUT SPECIFICATION ..... ☐ 1. Complementary ☐ 2. Nch-OpenDrain
- OUTPUT TYPE ..... ☐ 1. DC Output ☐ 2. FR (FOR SED1521FAA)

4A-9. R42 OUTPUT PORT SPECIFICATION

- OUTPUT SPECIFICATION ..... ☐ 1. Complementary ☐ 2. Nch-OpenDrain
- OUTPUT TYPE ..... ☐ 1. DC Output
  ☐ 2. Buzzer Inverted Output (R43 Control)
  ☐ 3. FOUT 256 [Hz]
  ☐ 4. FOUT 512 [Hz]
  ☐ 5. FOUT 1024 [Hz]
  ☐ 6. FOUT 2048 [Hz]
  ☐ 7. FOUT 4096 [Hz]
  ☐ 8. FOUT 8192 [Hz]
  ☐ 9. FOUT 16384 [Hz]
  ☐ 10. FOUT 32768 [Hz]
  ☐ 11. FOUT OSC3

4A-10. R43 OUTPUT PORT SPECIFICATION

- OUTPUT SPECIFICATION ..... ☐ 1. Complementary ☐ 2. Nch-OpenDrain
- OUTPUT TYPE ..... ☐ 1. DC Output ☐ 2. Buzzer Output

(E0C624A option list)

4A-11. I/O PORTS OUTPUT SPECIFICATION

• P00–P03	☐ 1. Complementary	☐ 2. Nch-OpenDrain
• P10–P13	☐ 1. Complementary	☐ 2. Nch-OpenDrain
• P20	☐ 1. Complementary	☐ 2. Nch-OpenDrain
• P21	☐ 1. Complementary	☐ 2. Nch-OpenDrain
• P22	☐ 1. Complementary	☐ 2. Nch-OpenDrain
• P23	☐ 1. Complementary	☐ 2. Nch-OpenDrain
• P30	☐ 1. Complementary	☐ 2. Nch-OpenDrain
• P31	☐ 1. Complementary	☐ 2. Nch-OpenDrain
• P32	☐ 1. Complementary	☐ 2. Nch-OpenDrain
• P33	☐ 1. Complementary	☐ 2. Nch-OpenDrain

4A-12. P00–P03, P10–P13 I/O PORTS OUTPUT TYPE

☐ 1. DC Output ☐ 2. Data Bus (D0–D7)

4A-13. P20–P23 I/O PORTS OUTPUT TYPE

• P20	☐ 1. DC Output	☐ 2. Chip Select (/CS0)
• P21	☐ 1. DC Output	☐ 2. Chip Select (/CS1)
• P22	☐ 1. DC Output	☐ 2. Chip Select (/CS2)
• P23	☐ 1. DC Output	☐ 2. Chip Select (/CS3)

4A-14. P30–P33 I/O PORTS OUTPUT TYPE

• P30	☐ 1. I/O Port	☐ 2. Output Port
• P31	☐ 1. I/O Port	☐ 2. Output Port
• P32	☐ 1. I/O Port	☐ 2. Output Port
• P33	☐ 1. I/O Port	☐ 2. Output Port

4A-15. SIN PULL UP RESISTOR

☐ 1. With Resistor ☐ 2. Gate Direct

4A-16. SOUT OUTPUT SPECIFICATION

☐ 1. Complementary ☐ 2. Nch-OpenDrain

4A-17. $\overline{\text{SCLK}}$ SPECIFICATION

• PULL UP RESISTOR	☐ 1. With Resistor	☐ 2. Gate Direct
• OUTPUT SPECIFICATION	☐ 1. Complementary	☐ 2. Nch-OpenDrain

4A-18. SIO DATA PERMUTATION

☐ 1. MSB First ☐ 2. LSB First

4A-19. LCD POWER VOLTAGE MODE

☐ 1. Internal Voltage ☐ 2. External Voltage

4.4 E0C624C/48 Option List

Multiple specifications are available in each option item as indicated in the Option List. Using "4.7 E0C624C/48 Option Specifications and Selection Message" as reference, select the specifications that meet the target system. Be sure to record the specifications for unused ports too, according to the instructions provided.

4C/48-1. OSC1 OSCILLATOR

☐ 1. Crystal ☐ 2. CR

4C/48-2. OSC3 OSCILLATOR

☐ 1. CR ☐ 2. Ceramic

4C/48-3. MULTIPLE KEY ENTRY RESET

☐ 1. Not Use
☐ 2. Use K00, K01
☐ 3. Use K00, K01, K02
☐ 4. Use K00, K01, K02, K03

4C/48-4. INPUT PORTS PULL UP RESISTOR

• K00	☐ 1. With Resistor	☐ 2. Gate Direct
• K01	☐ 1. With Resistor	☐ 2. Gate Direct
• K02	☐ 1. With Resistor	☐ 2. Gate Direct
• K03	☐ 1. With Resistor	☐ 2. Gate Direct
• K10	☐ 1. With Resistor	☐ 2. Gate Direct
• K11	☐ 1. With Resistor	☐ 2. Gate Direct
• K12	☐ 1. With Resistor	☐ 2. Gate Direct
• K13	☐ 1. With Resistor	☐ 2. Gate Direct

4C/48-5. OUTPUT PORTS OUTPUT SPECIFICATION

• R00–R03	☐ 1. Complementary	☐ 2. Nch-OpenDrain
• R10–R13	☐ 1. Complementary	☐ 2. Nch-OpenDrain
• R20–R22	☐ 1. Complementary	☐ 2. Nch-OpenDrain
• R23	☐ 1. Complementary	☐ 2. Nch-OpenDrain
• R30	☐ 1. Complementary	☐ 2. Nch-OpenDrain
• R31	☐ 1. Complementary	☐ 2. Nch-OpenDrain
• R32	☐ 1. Complementary	☐ 2. Nch-OpenDrain

4C/48-6. OUTPUT PORTS OUTPUT TYPE

• R00–R03	☐ 1. DC Output	☐ 2. Address Bus (A0–A3)
• R10–R13	☐ 1. DC Output	☐ 2. Address Bus (A4–A7)
• R20–R22	☐ 1. DC Output	☐ 2. Address Bus (A8–A10)
• R23	☐ 1. DC Output	☐ 2. Address Bus (A11)
• R30	☐ 1. DC Output	☐ 2. Address Bus (A12)
• R31	☐ 1. DC Output	☐ 2. Address Bus (A13)
		☐ 3. Write (/WR)
• R32	☐ 1. DC Output	☐ 2. Read (/RD)

4C/48-7. R33 OUTPUT PORT SPECIFICATION

• OUTPUT SPECIFICATION	☐ 1. Complementary	☐ 2. Nch-OpenDrain
• OUTPUT TYPE	☐ 1. DC (PTCLK) Output	☐ 2. /SRDY Output
• OUTPUT CONTROL	☐ 1. 3 States	☐ 2. 2 States

(E0C624C/48 option list)

4C/48-8. R40 OUTPUT PORT SPECIFICATION

- OUTPUT SPECIFICATION ..... ☐ 1. Complementary ☐ 2. Nch-OpenDrain
- OUTPUT TYPE ..... ☐ 1. DC Output
  ☐ 2. CL-16 (For SED1521FAA)
  ☐ 3. CL-8 (For SED1521FAA)
  ☐ 4. /FOUT 256 [Hz]
  ☐ 5. /FOUT 512 [Hz]
  ☐ 6. /FOUT 1024 [Hz]
  ☐ 7. /FOUT 2048 [Hz]
  ☐ 8. /FOUT 4096 [Hz]
  ☐ 9. /FOUT 8192 [Hz]
  ☐ 10. /FOUT 16384 [Hz]
  ☐ 11. /FOUT 32768 [Hz]
  ☐ 12. /FOUT OSC3

4C/48-9. R41 OUTPUT PORT SPECIFICATION

- OUTPUT SPECIFICATION ..... ☐ 1. Complementary ☐ 2. Nch-OpenDrain
- OUTPUT TYPE ..... ☐ 1. DC Output ☐ 2. FR (FOR SED1521FAA)

4C/48-10. R42 OUTPUT PORT SPECIFICATION

- OUTPUT SPECIFICATION ..... ☐ 1. Complementary ☐ 2. Nch-OpenDrain
- OUTPUT TYPE ..... ☐ 1. DC Output
  ☐ 2. Buzzer Inverted Output (R43 Control)
  ☐ 3. FOUT 256 [Hz]
  ☐ 4. FOUT 512 [Hz]
  ☐ 5. FOUT 1024 [Hz]
  ☐ 6. FOUT 2048 [Hz]
  ☐ 7. FOUT 4096 [Hz]
  ☐ 8. FOUT 8192 [Hz]
  ☐ 9. FOUT 16384 [Hz]
  ☐ 10. FOUT 32768 [Hz]
  ☐ 11. FOUT OSC3

4C/48-11. R43 OUTPUT PORT SPECIFICATION

- OUTPUT SPECIFICATION ..... ☐ 1. Complementary ☐ 2. Nch-OpenDrain
- OUTPUT TYPE ..... ☐ 1. DC Output ☐ 2. Buzzer Output

4C/48-12. I/O PORTS OUTPUT SPECIFICATION

- P00–P03 ..... ☐ 1. Complementary ☐ 2. Nch-OpenDrain
- P10–P13 ..... ☐ 1. Complementary ☐ 2. Nch-OpenDrain
- P20 ..... ☐ 1. Complementary ☐ 2. Nch-OpenDrain
- P21 ..... ☐ 1. Complementary ☐ 2. Nch-OpenDrain
- P22 ..... ☐ 1. Complementary ☐ 2. Nch-OpenDrain
- P23 ..... ☐ 1. Complementary ☐ 2. Nch-OpenDrain
- P30 ..... ☐ 1. Complementary ☐ 2. Nch-OpenDrain
- P31 ..... ☐ 1. Complementary ☐ 2. Nch-OpenDrain
- P32 ..... ☐ 1. Complementary ☐ 2. Nch-OpenDrain
- P33 ..... ☐ 1. Complementary ☐ 2. Nch-OpenDrain

4C/48-13. P00–P03, P10–P13 I/O PORTS OUTPUT TYPE

☐ 1. DC Output ☐ 2. Data Bus (D0–D7)

4C/48-14. P20–P23 I/O PORTS OUTPUT TYPE

- P20 ..... ☐ 1. DC Output ☐ 2. Chip Select (/CS0)
- P21 ..... ☐ 1. DC Output ☐ 2. Chip Select (/CS1)
- P22 ..... ☐ 1. DC Output ☐ 2. Chip Select (/CS2)
- P23 ..... ☐ 1. DC Output ☐ 2. Chip Select (/CS3)

(E0C624C/48 option list)

4C/48-15. P30–P33 I/O PORTS OUTPUT TYPE

- P30 ..... ☐ 1. I/O Port ☐ 2. Output Port
- P31 ..... ☐ 1. I/O Port ☐ 2. Output Port
- P32 ..... ☐ 1. I/O Port ☐ 2. Output Port
- P33 ..... ☐ 1. I/O Port ☐ 2. Output Port

4C/48-16. SIN PULL UP RESISTOR

☐ 1. With Resistor ☐ 2. Gate Direct

4C/48-17. SOUT OUTPUT SPECIFICATION

☐ 1. Complementary ☐ 2. Nch-OpenDrain

4C/48-18. $\overline{\text{SCLK}}$ SPECIFICATION

- PULL UP RESISTOR ..... ☐ 1. With Resistor ☐ 2. Gate Direct
- OUTPUT SPECIFICATION ..... ☐ 1. Complementary ☐ 2. Nch-OpenDrain

4C/48-19. SIO DATA PERMUTATION

☐ 1. MSB First ☐ 2. LSB First

4C/48-20. LCD POWER VOLTAGE MODE

☐ 1. Internal Voltage ☐ 2. External Voltage

4.5 E0C6244 Option Specifications and Selection Message

Screen that can be selected as function options set on the E0C6244 are shown below, and their specifications are also described.

44-1 OSC1 oscillator

```
*** OPTION  NO.1 ***

--- OSC1 OSCILLATOR ---

                          1. CRYSTAL
                          2. CR

PLEASE SELECT NO.(1) ? 1↲

                          1. CRYSTAL  SELECTED
```

Select oscillation circuit that uses OSC1 and OSC2. To minimize external components, CR oscillation circuit would be suitable; to obtain a stable oscillation frequency, crystal oscillation circuit would be suitable. When CR oscillation circuit is selected, only resistor is needed as external components since capacities are built-in.
On the other hand, when crystal oscillation circuit is selected, crystal oscillator and trimmer capacity are needed as external components. Although when crystal oscillation circuit is selected, it is fixed at 32.768 kHz, when CR oscillation circuit is selected, frequency may be modified to a certain extent depending on the resistance of external components.

44-2 OSC3 oscillator

```
*** OPTION  NO.2 ***

--- OSC3 OSCILLATOR ---

                          1. CR
                          2. CERAMIC

PLEASE SELECT NO.(1) ? 1↲

                          1. CR  SELECTED
```

Select oscillation circuit that uses OSC3 and OSC4. To minimize external components, CR oscillation circuit would be suitable; to obtain a stable oscillation frequency, ceramic oscillation circuit would be suitable. When CR oscillation circuit is selected, only resistor is needed as external components since capacities are built-in.
On the other hand, when ceramic oscillation circuit is selected, ceramic oscillator, feedback resistor, gate capacity and drain capacity are needed as external components.
Select CR oscillation circuit for unused OSC3 system clock.

44-3 Multiple key entry reset

```
*** OPTION  NO.3 ***

--- MULTIPLE KEY ENTRY RESET ---

                          1. NOT USE
                          2. USE K00,K01
                          3. USE K00,K01,K02
                          4. USE K00,K01,K02,K03

PLEASE SELECT NO.(1) ? 1↲

                          1. NOT USE  SELECTED
```

The reset function is set when K00 through K03 are entered.
When "Not Use" is selected, the reset function is not activated even if K00 through K03 are entered.
When "Use K00, K01" is selected, the system is reset immediately the K00 and K01 inputs go low at the same time. Similarly, the system is reset as soon as the K00 through K02 inputs or the K00 through K03 inputs go low.

The system is reset when a low signal is input for more than 2 seconds.

The system reset circuit is shown in Figure 4.5.1.

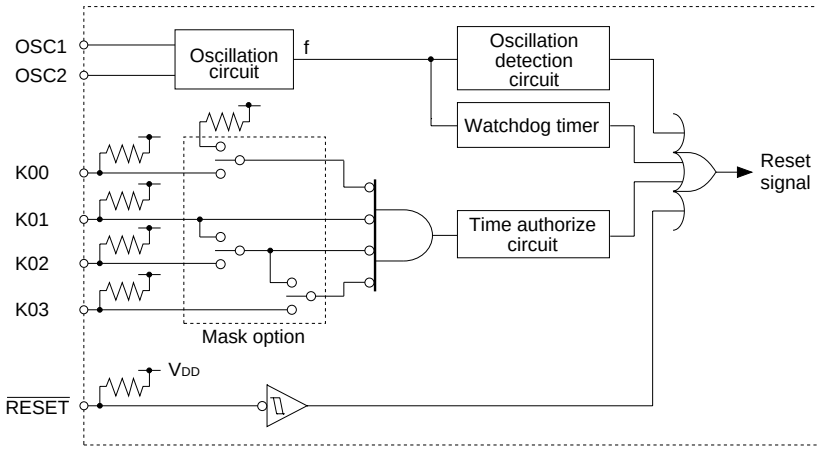

Fig. 4.5.1 System reset circuit

44-4 Input ports pull up resistor

```
*** OPTION  NO.4 ***

--- INPUT PORTS PULL UP RESISTOR ---

       K00              1. WITH RESISTOR
                        2. GATE DIRECT

PLEASE SELECT NO.(1) ? 1↵

       K01              1. WITH RESISTOR
                        2. GATE DIRECT

PLEASE SELECT NO.(1) ? 1↵

       K02              1. WITH RESISTOR
                        2. GATE DIRECT

PLEASE SELECT NO.(1) ? 1↵

       K03              1. WITH RESISTOR
                        2. GATE DIRECT

PLEASE SELECT NO.(1) ? 1↵

       K10              1. WITH RESISTOR
                        2. GATE DIRECT

PLEASE SELECT NO.(1) ? 1↵

       K11              1. WITH RESISTOR
                        2. GATE DIRECT

PLEASE SELECT NO.(1) ? 1↵

       K12              1. WITH RESISTOR
                        2. GATE DIRECT

PLEASE SELECT NO.(1) ? 1↵

       K13              1. WITH RESISTOR
                        2. GATE DIRECT

PLEASE SELECT NO.(1) ? 1↵

       K00              1. WITH RESISTOR  SELECTED
       K01              1. WITH RESISTOR  SELECTED
       K02              1. WITH RESISTOR  SELECTED
       K03              1. WITH RESISTOR  SELECTED
       K10              1. WITH RESISTOR  SELECTED
       K11              1. WITH RESISTOR  SELECTED
       K12              1. WITH RESISTOR  SELECTED
       K13              1. WITH RESISTOR  SELECTED
```

Select whether input ports (K00–K03 and K10–K13) will each be supplemented with pull up resistors or not. When "Gate Direct" is selected, see to it that entry floating state does not occur. Select "With Resistor" pull up resistor for unused ports. Moreover, the input port status is changed from low level (VSS) to high (VDD) with pull up resistors, a delay of approximately 500 µsec in waveform rise time will occur depending on the pull up resistor and entry load time constant. Because of this, when input reading is to be conducted, ensure the appropriate wait time with the program.
The configuration of the pull up resistor circuit is shown in Figure 4.5.2.

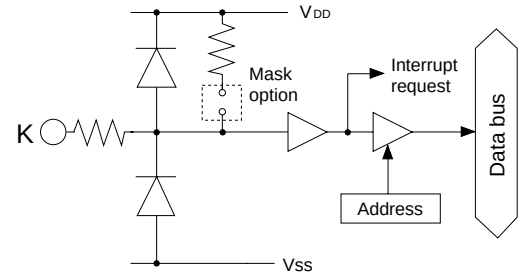

Fig. 4.5.2 Configuration of pull up resistor circuit

44-5 Output ports output specification

```
*** OPTION  NO.5 ***

--- OUTPUT PORTS OUTPUT SPECIFICATION ---

        R20-R23         1. COMPLEMENTARY
                        2. NCH-OPENDRAIN

PLEASE SELECT NO.(1) ? 1↵

        R30             1. COMPLEMENTARY
                        2. NCH-OPENDRAIN

PLEASE SELECT NO.(1) ? 1↵

        R31             1. COMPLEMENTARY
                        2. NCH-OPENDRAIN

PLEASE SELECT NO.(1) ? 1↵

        R32             1. COMPLEMENTARY
                        2. NCH-OPENDRAIN

PLEASE SELECT NO.(1) ? 1↵

        R20-R23         1. COMPLEMENTARY  SELECTED
        R30             1. COMPLEMENTARY  SELECTED
        R31             1. COMPLEMENTARY  SELECTED
        R32             1. COMPLEMENTARY  SELECTED
```

Select the output specification for the output ports (R20–R32).
Either complementary output or Nch open drain output may be selected.
When output port is to be used on key matrix configuration, select Nch open drain output.
For unused output ports, select complementary output.
The output circuit configuration is shown in Figure 4.5.3.

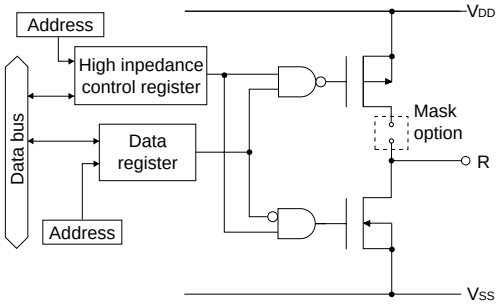

Fig. 4.5.3 Configuration of output circuit

44-6 R33 output port specification

```
*** OPTION  NO.6 ***

--- R33 OUTPUT PORT SPECIFICATION ---

    OUTPUT SPECIFICATION 1. COMPLEMENTARY
                         2. NCH-OPENDRAIN

PLEASE SELECT NO.(1) ? 1↵

    OUTPUT TYPE          1. DC (PTCLK)
                         2. /SRDY

PLEASE SELECT NO.(1) ? 1↵

    OUTPUT CONTROL       1. 3 STATE
                         2. 2 STATE

PLEASE SELECT NO.(1) ? 1↵

    OUTPUT SPECIFICATION 1. COMPLEMENTARY  SELECTED
    OUTPUT TYPE          1. DC (PTCLK)  SELECTED
    OUTPUT CONTROL       1. 3 STATE  SELECTED
```

Select the specification for R33 terminal.
Either complementary output or Nch open drain output may be selected for the output specification.
Either DC output (or PTCLK output) or /SRDY output may be selected for the output type.
When DC (PTCLK) output is selected, R33 will either become a regular output port terminal (PTCOUT = "0") or an operating clock output terminal for the programmable timer (PTCOUT = "1").
When /SRDY is selected, a Ready signal indicating whether the serial interface is available for receiving or transmitting is output from R33.
For the output control, either 3-state or 2-state may be selected.
When /SRDY is selected for the output type, 2-state is normally selected for the output control.
When DC (PTCLK) is selected, 2-state may also be selected but caution is required because output becomes insufficient during initial reset.
The circuit configuration is the same as that of output ports (Figure 4.5.3).

44-7 R40 output port specification

```
*** OPTION  NO.7 ***

--- R40 OUTPUT PORT SPECIFICATION ---

    OUTPUT SPECIFICATION 1. COMPLEMENTARY
                         2. NCH-OPENDRAIN

PLEASE SELECT NO.(1) ? 1↵

    OUTPUT TYPE          1. DC
                         2. CL-16 (FOR SED1521FAA)
                         3. CL-8  (FOR SED1521FAA)
                         4. /FOUT   256 [HZ]
                         5. /FOUT   512 [HZ]
                         6. /FOUT  1024 [HZ]
                         7. /FOUT  2048 [HZ]
                         8. /FOUT  4096 [HZ]
                         9. /FOUT  8192 [HZ]
                        10./FOUT 16384 [HZ]
                        11./FOUT 32768 [HZ]
                        12./FOUT OSC3

PLEASE SELECT NO.(1) ? 1↵

    OUTPUT SPECIFICATION 1. COMPLEMENTARY  SELECTED
    OUTPUT TYPE          1. DC  SELECTED
```

Select the specification for R40 terminal.
Either complementary output or Nch open drain output may be selected for the output specification.
Any one of the following may be selected for the output type: DC output, CL output or /FOUT output.
The output circuit configuration of R4 port is shown in Figure 4.5.4.

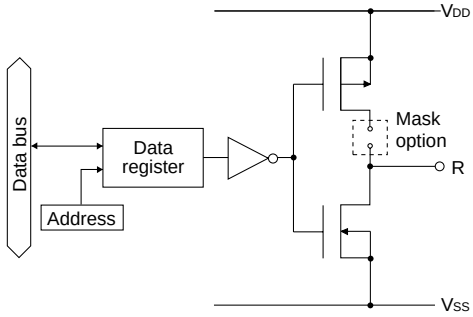

Fig. 4.5.4 Output circuit configuration of R4 port

When DC output is selected

When DC output is selected, R40 becomes a regular output port. By writing "1" on R40 register, the R40 terminal output goes high (V_{DD}), and goes low (V_{SS}) by writing "0".
The output waveform is shown in Figure 4.5.5.

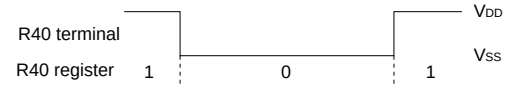

Fig. 4.5.5 Output waveform at DC output selection

When CL output is selected

When expansion LCD driver (SED1521FAA) is externally connected, selection of the CL output will cause R40 terminal to output LCD synchronous signal. The CL signal can select from one of two types, the CL-16 for 1/16 duty or the CL-8 for 1/8 duty. The respective frequency of CL-16 signal and CL-8 signal are 1024 Hz and 512 Hz. The CL signal can be output to R40 terminal by writing "0" on R40 register. Moreover, FR signal (LCD frame signal, 32 Hz) may be selected through mask option of the R41 terminal.
The CL signal and FR signal output waveforms are shown in Figure 4.5.6.

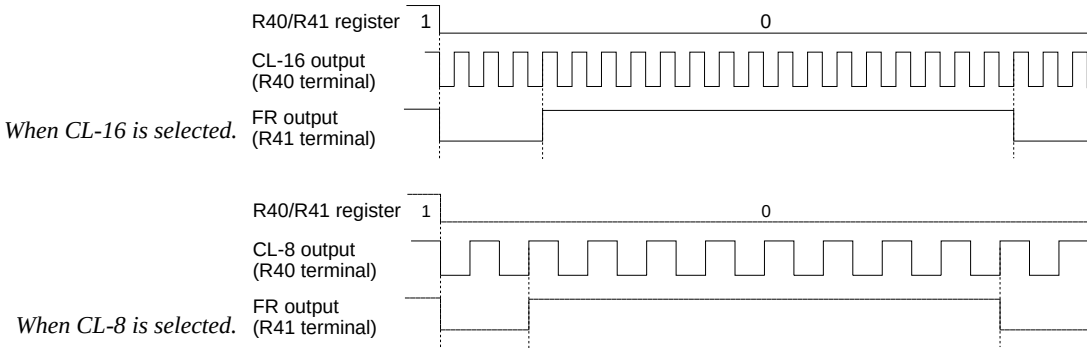

Fig. 4.5.6 CL signal and FR signal output waveforms

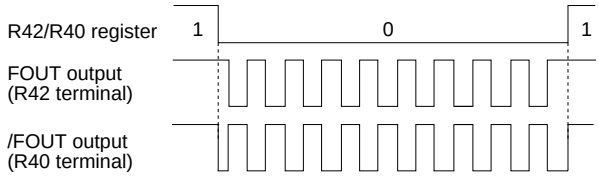

Fig. 4.5.7 FOUT signal and /FOUT signal output waveforms

When /FOUT output is selected

When /FOUT output is selected, signal with frequency selected from among nine types, ranging from 256 Hz to 32768 Hz and OSC3 may be output from R40 terminal.
In this case, by writing "0" on R40 register, 50% duty and V_{DD}–V_{SS} amplitude square wave is output from R40 terminal at the specified frequency. Writing "1" will cause the R40 terminal to go high (V_{DD}).
The /FOUT output is normally used to supply clock to other devices but since hazard occurs when R40 register is re-written, great caution must be observed when using it.
Moreover, FOUT output may be selected in the same manner through the R42 terminal mask option. Note, however, that FOUT signal becomes antiphase to /FOUT signal.
The output waveform is shown in Figure 4.5.7.

44-8 R41 output port specification

```
*** OPTION  NO.8 ***

--- R41 OUTPUT PORT SPECIFICATION ---

    OUTPUT SPECIFICATION 1. COMPLEMENTARY
                         2. NCH-OPENDRAIN

PLEASE SELECT NO.(1) ? 1↲

    OUTPUT TYPE          1. DC
                         2. FR (FOR SED1521FAA)

PLEASE SELECT NO.(1) ? 1↲

    OUTPUT SPECIFICATION 1. COMPLEMENTARY  SELECTED
    OUTPUT TYPE          1. DC  SELECTED
```

Select the specification for R41 terminal.
Either complementary output or Nch open drain output may be selected for the output specification.
For the output type, either DC output or FR output may be selected.
The circuit configuration is the same as that of the R40 output port (Figure 4.5.4).

When DC output is selected, R41 becomes a regular output port. By writing "1" on R41 register, the R41 terminal output goes high (V_{DD}), and goes low (V_{SS}) by writing "0".

When expansion LCD driver (SED1521FAA) is externally connected, selection of the FR output will cause R41 terminal to output LCD frame signal (32 Hz).
In this case, FR signal can be output from R41 terminal by writing "0" on R41 register.
Refer to Figure 4.5.6 for FR signal output.

44-9 R42 output port specification

```
*** OPTION  NO.9 ***

--- R42 OUTPUT PORT SPECIFICATION ---

    OUTPUT SPECIFICATION 1. COMPLEMENTARY
                         2. NCH-OPENDRAIN

PLEASE SELECT NO.(1) ? 1↲
```

Select the specification for R42 terminal.
Either complementary output or Nch open drain output may be selected for the output specification.
Any one of the following may be selected for the output type: DC output, /BUZZER output or /FOUT output.
The circuit configuration is the same as that of the R40 output port (Figure 4.5.4).

```
    OUTPUT TYPE          1. DC
                         2. /BUZZER (R43 CONT)
                         3. FOUT   256 [HZ]
                         4. FOUT   512 [HZ]
                         5. FOUT  1024 [HZ]
                         6. FOUT  2048 [HZ]
                         7. FOUT  4096 [HZ]
                         8. FOUT  8192 [HZ]
                         9. FOUT 16384 [HZ]
                         10.FOUT 32768 [HZ]
                         11.FOUT OSC3

PLEASE SELECT NO.(1) ? 1↵

    OUTPUT SPECIFICATION 1. COMPLEMENTARY  SELECTED
    OUTPUT TYPE          1. DC  SELECTED
```

When DC output is selected, R42 becomes a regular output port. By writing "1" on R42 register, the R42 terminal output goes high (V_{DD}), and goes low (V_{SS}) by writing "0".

When BUZZER output is selected with the R43 mask option, /BUZZER output becomes a buzzer inverted signal for direct driving of the piezoelectric buzzer together with the BUZZER output. The control of the buzzer signal output is accomplished through R43 register even if R42 has been set to /BUZZER.
Because of this, R42 cannot be set to /BUZZER output when R43 is set to DC output.
Refer to Figure 4.5.8 for the /BUZZER output waveform.

When FOUT output is selected, signal with frequency selected from among nine types, ranging from 256 Hz to 32768 Hz and OSC3 may be output from R42 terminal.
FOUT output is the same as that of /FOUT signal. Note, however, that /FOUT signal becomes antiphase to FOUT signal.

44-10 R43 output port specification

```
*** OPTION  NO.10 ***

--- R43 OUTPUT PORT SPECIFICATION ---

    OUTPUT SPECIFICATION 1. COMPLEMENTARY
                         2. NCH-OPENDRAIN

PLEASE SELECT NO.(1) ? 1↵

    OUTPUT TYPE          1. DC
                         2. BUZZER

PLEASE SELECT NO.(1) ? 1↵

    OUTPUT SPECIFICATION 1. COMPLEMENTARY  SELECTED
    OUTPUT TYPE          1. DC  SELECTED
```

* When "R42 OUTPUT TYPE" is set to /BUZZER", "DC" option may not be selected.

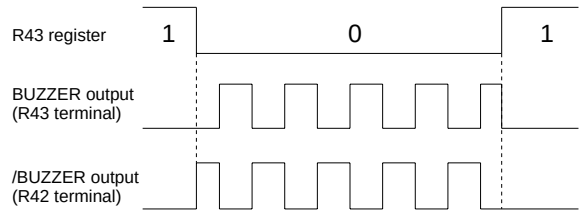

Fig. 4.5.8 Buzzer signal output waveform

Select the specification for R43 terminal.
Either complementary output or Nch open drain output may be selected for the output specification.
For the output type, either DC output or BUZZER output may be selected.
The circuit configuration is the same as that of the R40 output port (Figure 4.5.4).

When DC output is selected, R43 becomes a regular output port. By writing "1" on R43 register, the R43 terminal output goes high (V_{DD}), and goes low (V_{SS}) by writing "0".

When BUZZER output is selected, by writing "0" on R43 register, buzzer signal is output from the R43 terminal, low (V_{SS}) is output by writing "1". When /BUZZER output (buzzer inverted output) is selected for R42 together with R43, it can be directly driven together with piezoelectric buzzer. The control of the /BUZZER output is also accomplished through R43 register.
The BUZZER signal and /BUZZER signal output waveforms are shown in Figure 4.5.8.

44-11 I/O ports output specification

```
*** OPTION  NO.11 ***

--- I/O PORTS OUTPUT SPECIFICATION ---

        P00-P03          1. COMPLEMENTARY
                         2. NCH-OPENDRAIN

PLEASE SELECT NO.(1) ? 1↵

        P10-P13          1. COMPLEMENTARY
                         2. NCH-OPENDRAIN

PLEASE SELECT NO.(1) ? 1↵

        P20              1. COMPLEMENTARY
                         2. NCH-OPENDRAIN

PLEASE SELECT NO.(1) ? 1↵

        P21              1. COMPLEMENTARY
                         2. NCH-OPENDRAIN

PLEASE SELECT NO.(1) ? 1↵

        P22              1. COMPLEMENTARY
                         2. NCH-OPENDRAIN

PLEASE SELECT NO.(1) ? 1↵

        P23              1. COMPLEMENTARY
                         2. NCH-OPENDRAIN

PLEASE SELECT NO.(1) ? 1↵

        P00-P03          1. COMPLEMENTARY  SELECTED
        P10-P13          1. COMPLEMENTARY  SELECTED
        P20              1. COMPLEMENTARY  SELECTED
        P21              1. COMPLEMENTARY  SELECTED
        P22              1. COMPLEMENTARY  SELECTED
        P23              1. COMPLEMENTARY  SELECTED
```

Select the output specification to be used during I/O ports (P00–P23) output mode selection. Either complementary output or Nch open drain output may be selected.
The circuit configuration of the output driver is the same as that of output ports (Figure 4.5.3).
Select complementary output for unused ports.

The I/O port circuit configuration is shown in Figure 4.5.9.

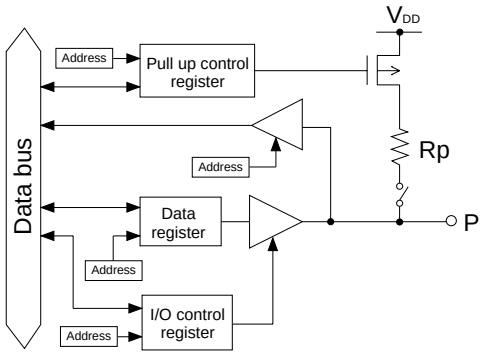

Fig. 4.5.9 Circuit configuration of I/O port

44-12 P20–P23 I/O ports output type

```
*** OPTION  NO.12 ***

--- P20-P23 I/O PORTS OUTPUT TYPE ---

        P20              1. I/O PORT
                         2. OUTPUT PORT

PLEASE SELECT NO.(1) ? 1↵

        P21              1. I/O PORT
                         2. OUTPUT PORT

PLEASE SELECT NO.(1) ? 1↵

        P22              1. I/O PORT
                         2. OUTPUT PORT

PLEASE SELECT NO.(1) ? 1↵

        P23              1. I/O PORT
                         2. OUTPUT PORT

PLEASE SELECT NO.(1) ? 1↵

        P20              1. I/O PORT  SELECTED
        P21              1. I/O PORT  SELECTED
        P22              1. I/O PORT  SELECTED
        P23              1. I/O PORT  SELECTED
```

Select the output type for P20–P23 terminals.

The I/O ports can control the input/output direction according to the I/O control register (IOC2); at "1" and "0" settings, it is set to output port and input port, respectively.

Moreover, when selected as an output port, the I/O port functions as only output port and is not affected by the I/O control register.
In this case, pull up resistors cannot be added.

44-13 SIN pull up resistor

```
*** OPTION  NO.13 ***

--- SIN PULL UP RESISTOR ---

                        1. WITH RESISTOR
                        2. GATE DIRECT

PLEASE SELECT NO.(1) ? 1↵

                        1. WITH RESISTOR  SELECTED
```

Select whether pull up resistor will be supplemented to SIN terminal of the serial interface. When "Gate Direct" is selected, take care that input floating state does not occur. Select "With Resistor" for SIN terminal that will not be used.

44-14 SOUT output specification

```
*** OPTION  NO.14 ***

--- SOUT OUTPUT SPECIFICATION ---

                        1. COMPLEMENTARY
                        2. NCH-OPENDRAIN

PLEASE SELECT NO.(1) ? 1↵

                        1. COMPLEMENTARY  SELECTED
```

Select the output specification for SOUT terminal of the serial interface.
Either complementary output or Nch open drain output may be selected.
Select "Complementary" for SOUT terminal that will not be used.

44-15 $\overline{SCLK}$ specification

```
*** OPTION  NO.15 ***

--- /SCLK SPECIFICATION ---

    PULL UP RESISTOR     1. WITH RESISTOR
                         2. GATE DIRECT

PLEASE SELECT NO.(1) ? 1↵

    OUTPUT SPECIFICATION 1. COMPLEMENTARY
                         2. NCH-OPENDRAIN

PLEASE SELECT NO.(1) ? 1↵

    PULL UP RESISTOR     1. WITH RESISTOR  SELECTED
    OUTPUT SPECIFICATION 1. COMPLEMENTARY  SELECTED
```

Select the specification for the $\overline{SCLK}$ terminal of the serial interface.

For the pull up resistor, select whether to supplement or not a built-in pull up resistor which will turn ON when in the input mode (external clock mode).

For the output specification, either complementary output or Nch open drain output may be selected. Select "With Resistor" and "Complementary" for $\overline{SCLK}$ terminal that will not be used.

44-16 SIO data permutation

```
*** OPTION  NO.16 ***

--- SIO DATA PERMUTATION ---

                        1. MSB FIRST
                        2. LSB FIRST

PLEASE SELECT NO.(1) ? 1↵

                        1. MSB FIRST  SELECTED
```

Select whether the serial interface input/output (SIN or SOUT) data bit permutation will be MSB first or LSB first.
Select the one suitable to your programming needs.
Input/output data permutation is shown in Figure 4.5.10.

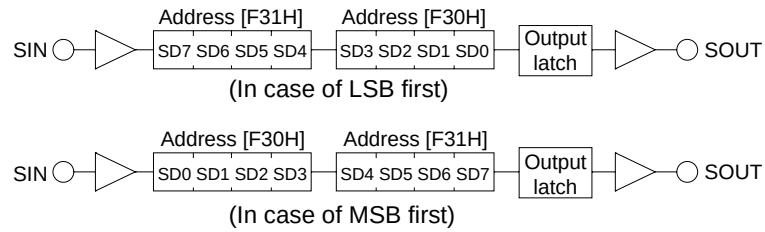

Fig. 4.5.10
Input/output data permutation

44-17 LCD power voltage mode

```
*** OPTION  NO.17 ***

--- LCD POWER VOLTAGE MODE ---

                          1. INTERNAL VOLTAGE
                          2. EXTERNAL VOLTAGE

PLEASE SELECT NO.(1) ? 1↵

                          1. INTERNAL VOLTAGE  SELECTED
```

Select the power mode for the LCD driver.
When internal voltage is selected, the LCD power source built in the E0C6244 is used and driving is fixed at 1/4 bias. In this case, the LCD contrast may be adjusted through the software.
When external voltage is selected, the LCD driving voltage is externally supplied. Aside from 1/4 bias, driving may also be set at 1/5 bias. Adjustment of the LCD contrast in this case requires setting up of external components.

4.6 E0C624A Option Specifications and Selection Message

Screen that can be selected as function options set on the E0C624A are shown below, and their specifications are also described.

4A-1 OSC3 oscillator

```
*** OPTION  NO.1 ***

--- OSC3 OSCILLATOR ---

                        1. CR
                        2. CERAMIC

PLEASE SELECT NO.(1) ? 1↵

                        1. CR  SELECTED
```

Select oscillation circuit that uses OSC3 and OSC4. To minimize external components, CR oscillation circuit would be suitable; to obtain a stable oscillation frequency, ceramic oscillation circuit would be suitable. When CR oscillation circuit is selected, only resistor is needed as external components since capacities are built-in.
On the other hand, when ceramic oscillation circuit is selected, ceramic oscillator, feedback resistor, gate capacity and drain capacity are needed as external components.
Select CR oscillation circuit for unused OSC3 system clock.

4A-2 Multiple key entry reset

```
*** OPTION  NO.2 ***

--- MULTIPLE KEY ENTRY RESET ---

                        1. NOT USE
                        2. USE K00,K01
                        3. USE K00,K01,K02
                        4. USE K00,K01,K02,K03

PLEASE SELECT NO.(1) ? 2↵

                        2. USE K00,K01  SELECTED
```

The reset function is set when K00 through K03 are entered.
When "Not Use" is selected, the reset function is not activated even if K00 through K03 are entered.
When "Use K00, K01" is selected, the system is reset immediately the K00 and K01 inputs go low at the same time. Similarly, the system is reset as soon as the K00 through K02 inputs or the K00 through K03 inputs go low.

The system is reset when a low signal is input for more than 2 seconds.

The system reset circuit is shown in Figure 4.6.1.

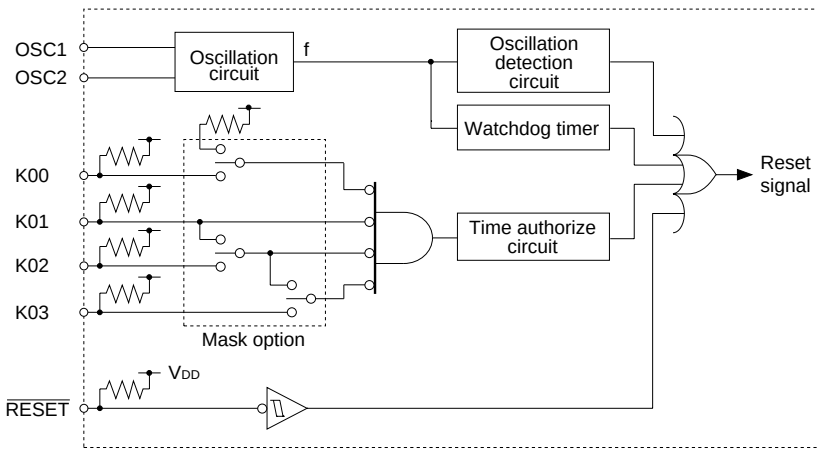

Fig. 4.6.1 System reset circuit

4A-3 Input ports pull up resistor

```
*** OPTION  NO.3 ***

--- INPUT PORTS PULL UP RESISTOR ---

        K00             1. WITH RESISTOR
                        2. GATE DIRECT

PLEASE SELECT NO.(1) ? 2↲

        K01             1. WITH RESISTOR
                        2. GATE DIRECT

PLEASE SELECT NO.(1) ? 2↲

        K02             1. WITH RESISTOR
                        2. GATE DIRECT

PLEASE SELECT NO.(1) ? 2↲

        K03             1. WITH RESISTOR
                        2. GATE DIRECT

PLEASE SELECT NO.(1) ? 2↲

        K10             1. WITH RESISTOR
                        2. GATE DIRECT

PLEASE SELECT NO.(1) ? 1↲

        K11             1. WITH RESISTOR
                        2. GATE DIRECT

PLEASE SELECT NO.(1) ? 1↲

        K12             1. WITH RESISTOR
                        2. GATE DIRECT

PLEASE SELECT NO.(1) ? 1↲

        K13             1. WITH RESISTOR
                        2. GATE DIRECT

PLEASE SELECT NO.(1) ? 1↲

        K00             2. GATE DIRECT  SELECTED
        K01             2. GATE DIRECT  SELECTED
        K02             2. GATE DIRECT  SELECTED
        K03             2. GATE DIRECT  SELECTED
        K10             1. WITH RESISTOR  SELECTED
        K11             1. WITH RESISTOR  SELECTED
        K12             1. WITH RESISTOR  SELECTED
        K13             1. WITH RESISTOR  SELECTED
```

Select whether input ports (K00–K03 and K10–K13) will each be supplemented with pull up resistors or not. When "Gate Direct" is selected, see to it that entry floating state does not occur. Select "With Resistor" pull up resistor for unused ports. Moreover, the input port status is changed from low level (V_{SS}) to high (V_{DD}) with pull up resistors, a delay of approximately 500 µsec in waveform rise time will occur depending on the pull up resistor and entry load time constant. Because of this, when input reading is to be conducted, ensure the appropriate wait time with the program.
The configuration of the pull up resistor circuit is shown in Figure 4.6.2.

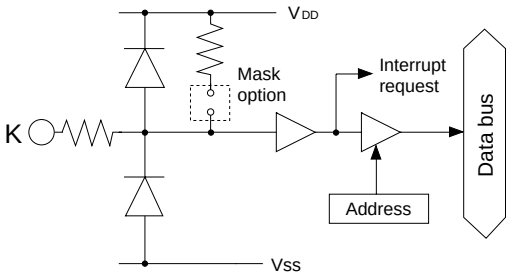

Fig. 4.6.2 Configuration of pull up resistor circuit

4A-4 Output ports output specification

```
*** OPTION  NO.4 ***
--- OUTPUT PORTS OUTPUT SPECIFICATION ---
        R00-R03         1. COMPLEMENTARY
                        2. NCH-OPENDRAIN
PLEASE SELECT NO.(1) ? 1↵
        R10-R13         1. COMPLEMENTARY
                        2. NCH-OPENDRAIN
PLEASE SELECT NO.(1) ? 1↵
        R20-R22         1. COMPLEMENTARY
                        2. NCH-OPENDRAIN
PLEASE SELECT NO.(1) ? 1↵
        R23             1. COMPLEMENTARY
                        2. NCH-OPENDRAIN
PLEASE SELECT NO.(1) ? 2↵
        R30             1. COMPLEMENTARY
                        2. NCH-OPENDRAIN
PLEASE SELECT NO.(1) ? 2↵
        R31             1. COMPLEMENTARY
                        2. NCH-OPENDRAIN
PLEASE SELECT NO.(1) ? 1↵
        R32             1. COMPLEMENTARY
                        2. NCH-OPENDRAIN
PLEASE SELECT NO.(1) ? 1↵
        R00-R03         1. COMPLEMENTARY  SELECTED
        R10-R13         1. COMPLEMENTARY  SELECTED
        R20-R22         1. COMPLEMENTARY  SELECTED
        R23             2. NCH-OPENDRAIN  SELECTED
        R30             2. NCH-OPENDRAIN  SELECTED
        R31             1. COMPLEMENTARY  SELECTED
        R32             1. COMPLEMENTARY  SELECTED
```

Select the output specification for the output ports (R00–R32).
Either complementary output or Nch open drain output may be selected.
When output port is to be used on key matrix configuration, select Nch open drain output.
For unused output ports, select complementary output.
The output circuit configuration is shown in Figure 4.6.3.

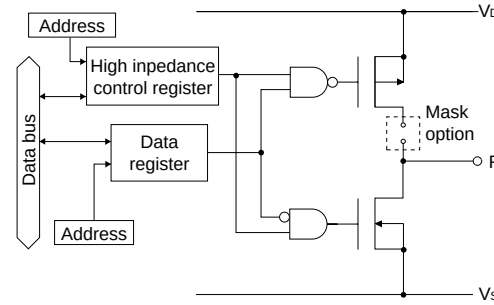

Fig. 4.6.3 Configuration of output circuit

4A-5 Output ports output type

```
*** OPTION  NO.5 ***
--- OUTPUT PORTS OUTPUT TYPE ---
        R00-R03       1. DC
                      2. ADDRESS BUS (A0-A3)
PLEASE SELECT NO.(1) ? 2↵
        R10-R13       1. DC
                      2. ADDRESS BUS (A4-A7)
PLEASE SELECT NO.(1) ? 2↵
        R20-R22       1. DC
                      2. ADDRESS BUS (A8-A10)
PLEASE SELECT NO.(1) ? 2↵
        R23           1. DC
                      2. ADDRESS BUS (A11)
```

Select the output type of the output ports.
When DC output is selected, the output port becomes a regular output port.
When address bus is selected, the output port becomes the address bus to the external memory device and the writing data to the register is output to the address bus.

```
PLEASE SELECT NO.(1) ? 1↵
        R30           1. DC
                      2. ADDRESS BUS (A12)*
PLEASE SELECT NO.(1) ? 1↵
        R31           1. DC
                      2. WRITE (/WR)
PLEASE SELECT NO.(1) ? 2↵
        R32           1. DC
                      2. READ (/RD)
PLEASE SELECT NO.(1) ? 2↵
        R00-R03       2. ADDRESS BUS (A0-A3) SELECTED
        R10-R13       2. ADDRESS BUS (A4-A7) SELECTED
        R20-R22       2. ADDRESS BUS (A8-A10) SELECTED
        R23           1. DC SELECTED
        R30           1. DC SELECTED
        R31           2. WRITE (/WR) SELECTED
        R32           2. READ (/RD) SELECTED
```

When /WR is selected for R31, /WR (write) signal is output from R31 terminal by writing the high order 4 bits (P10–P13) of the data bus.
When /RD is selected for R32, /RD (read) signal is output from R32 terminal by reading the low order 4 bits (P00–P03) of the data bus.
When /WR and /RD are selected, R31 and R32 registers may be used as a 1 bit general purpose register capable of read/write functions.

For details on external memory access, refer to the "E0C6244/4A/4C/48 Technical Manual".

* When DC output is designated for low-order ports, ports of higher orders cannot be given address bus selections.

4A-6 R33 output port specification

```
*** OPTION  NO.6 ***

--- R33 OUTPUT PORT SPECIFICATION ---

    OUTPUT SPECIFICATION 1. COMPLEMENTARY
                         2. NCH-OPENDRAIN

PLEASE SELECT NO.(1) ? 1↵

    OUTPUT TYPE          1. DC (PTCLK)
                         2. /SRDY

PLEASE SELECT NO.(1) ? 2↵

    OUTPUT CONTROL       1. 3 STATE
                         2. 2 STATE

PLEASE SELECT NO.(1) ? 2↵

    OUTPUT SPECIFICATION 1. COMPLEMENTARY  SELECTED
    OUTPUT TYPE          2. /SRDY  SELECTED
    OUTPUT CONTROL       2. 2 STATE  SELECTED
```

Select the specification for R33 terminal.
Either complementary output or Nch open drain output may be selected for the output specification.
Either DC output (or PTCLK output) or /SRDY output may be selected for the output type.
When DC (PTCLK) output is selected, R33 will either become a regular output port terminal (PTCOUT = "0") or an operating clock output terminal for the programmable timer (PTCOUT = "1").
When /SRDY is selected, a Ready signal indicating whether the serial interface is available for receiving or transmitting is output from R33.
For the output control, either 3-state or 2-state may be selected.
When /SRDY is selected for the output type, 2-state is normally selected for the output control.
When DC (PTCLK) is selected, 2-state may also be selected but caution is required because output becomes insufficient during initial reset.
The circuit configuration is the same as that of output ports (Figure 4.6.3).

4A-7 R40 output port specification

```
*** OPTION  NO.7 ***

--- R40 OUTPUT PORT SPECIFICATION ---

    OUTPUT SPECIFICATION 1. COMPLEMENTARY
                         2. NCH-OPENDRAIN

PLEASE SELECT NO.(1) ? 1↵

    OUTPUT TYPE          1. DC
                         2. CL-16 (FOR SED1521FAA)
                         3. CL-8  (FOR SED1521FAA)
                         4. /FOUT   256 [HZ]
                         5. /FOUT   512 [HZ]
                         6. /FOUT  1024 [HZ]
                         7. /FOUT  2048 [HZ]
                         8. /FOUT  4096 [HZ]
                         9. /FOUT  8192 [HZ]
                        10./FOUT 16384 [HZ]
                        11./FOUT 32768 [HZ]
                        12./FOUT OSC3

PLEASE SELECT NO.(1) ? 1↵

    OUTPUT SPECIFICATION 1. COMPLEMENTARY  SELECTED
    OUTPUT TYPE          1. DC  SELECTED
```

Select the specification for R40 terminal.
Either complementary output or Nch open drain output may be selected for the output specification.
Any one of the following may be selected for the output type: DC output, CL output or /FOUT output.
The output circuit configuration of R4 port is shown in Figure 4.6.4.

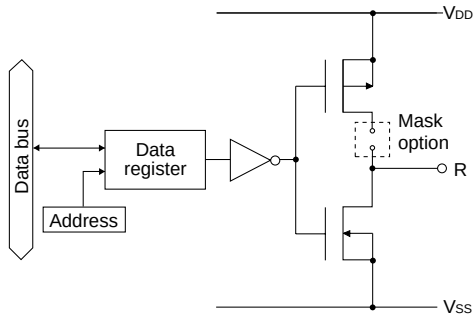

Fig. 4.6.4 Output circuit configuration of R4 port

When DC output is selected

When DC output is selected, R40 becomes a regular output port. By writing "1" on R40 register, the R40 terminal output goes high (V_{DD}), and goes low (V_{SS}) by writing "0".
The output waveform is shown in Figure 4.6.5.

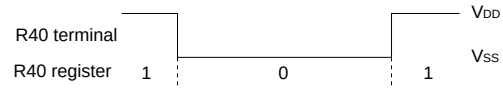

Fig. 4.6.5 Output waveform at DC output selection

When CL output is selected

When expansion LCD driver (SED1521FAA) is externally connected, selection of the CL output will cause R40 terminal to output LCD synchronous signal. The CL signal can select from one of two types, the CL-16 for 1/16 duty or the CL-8 for 1/8 duty. The respective frequency of CL-16 signal and CL-8 signal are 1024 Hz and 512 Hz. The CL signal can be output to R40 terminal by writing "0" on R40 register. Moreover, FR signal (LCD frame signal, 32 Hz) may be selected through mask option of the R41 terminal.
The CL signal and FR signal output waveforms are shown in Figure 4.6.6.

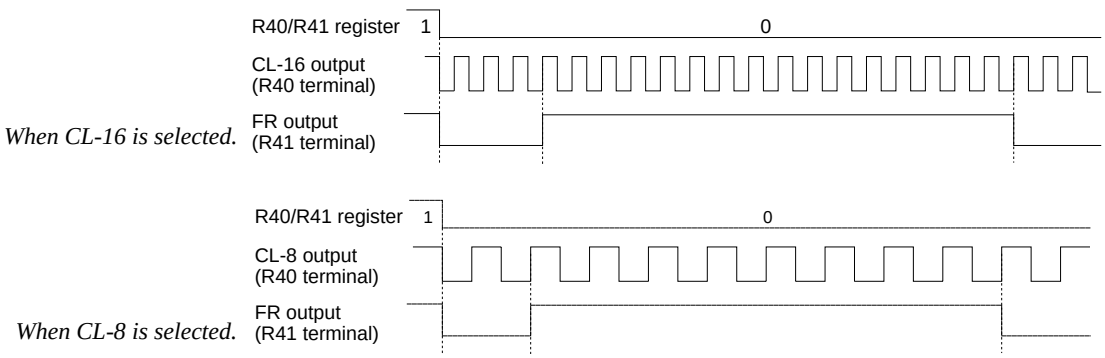

Fig. 4.6.6 CL signal and FR signal output waveforms

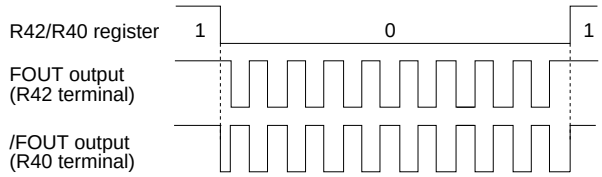

Fig. 4.6.7 FOUT signal and /FOUT signal output waveforms

When /FOUT output is selected

When /FOUT output is selected, signal with frequency selected from among nine types, ranging from 256 Hz to 32768 Hz and OSC3 may be output from R40 terminal.
In this case, by writing "0" on R40 register, 50% duty and V_{DD}–V_{SS} amplitude square wave is output from R40 terminal at the specified frequency. Writing "1" will cause the R40 terminal to go high (V_{DD}).
The /FOUT output is normally used to supply clock to other devices but since hazard occurs when R40 register is re-written, great caution must be observed when using it.
Moreover, FOUT output may be selected in the same manner through the R42 terminal mask option. Note, however, that FOUT signal becomes antiphase to /FOUT signal.
The output waveform is shown in Figure 4.6.7.

4A-8 R41 output port specification

```
*** OPTION  NO.8 ***

--- R41 OUTPUT PORT SPECIFICATION ---

    OUTPUT SPECIFICATION 1. COMPLEMENTARY
                         2. NCH-OPENDRAIN

PLEASE SELECT NO.(1) ? 1↲

    OUTPUT TYPE          1. DC
                         2. FR (FOR SED1521FAA)

PLEASE SELECT NO.(1) ? 1↲

    OUTPUT SPECIFICATION 1. COMPLEMENTARY  SELECTED
    OUTPUT TYPE          1. DC  SELECTED
```

Select the specification for R41 terminal.
Either complementary output or Nch open drain output may be selected for the output specification.
For the output type, either DC output or FR output may be selected.
The circuit configuration is the same as that of the R40 output port (Figure 4.6.4).

When DC output is selected, R41 becomes a regular output port. By writing "1" on R41 register, the R41 terminal output goes high (V_{DD}), and goes low (V_{SS}) by writing "0".

When expansion LCD driver (SED1521FAA) is externally connected, selection of the FR output will cause R41 terminal to output LCD frame signal (32 Hz).
In this case, FR signal can be output from R41 terminal by writing "0" on R41 register.
Refer to Figure 4.6.6 for FR signal output.

4A-9 R42 output port specification

```
*** OPTION  NO.9 ***

--- R42 OUTPUT PORT SPECIFICATION ---

    OUTPUT SPECIFICATION 1. COMPLEMENTARY
                         2. NCH-OPENDRAIN

PLEASE SELECT NO.(1) ? 1↲
```

Select the specification for R42 terminal.
Either complementary output or Nch open drain output may be selected for the output specification.
Any one of the following may be selected for the output type: DC output, /BUZZER output or /FOUT output.
The circuit configuration is the same as that of the R40 output port (Figure 4.6.4).

```
    OUTPUT TYPE          1. DC
                         2. /BUZZER (R43 CONT)
                         3. FOUT   256 [HZ]
                         4. FOUT   512 [HZ]
                         5. FOUT  1024 [HZ]
                         6. FOUT  2048 [HZ]
                         7. FOUT  4096 [HZ]
                         8. FOUT  8192 [HZ]
                         9. FOUT 16384 [HZ]
                         10.FOUT 32768 [HZ]
                         11.FOUT OSC3

PLEASE SELECT NO.(1) ? 11↵

    OUTPUT SPECIFICATION 1. COMPLEMENTARY  SELECTED
    OUTPUT TYPE          11.FOUT OSC3  SELECTED
```

When DC output is selected, R42 becomes a regular output port. By writing "1" on R42 register, the R42 terminal output goes high (V_{DD}), and goes low (V_{SS}) by writing "0".

When BUZZER output is selected with the R43 mask option, /BUZZER output becomes a buzzer inverted signal for direct driving of the piezoelectric buzzer together with the BUZZER output. The control of the buzzer signal output is accomplished through R43 register even if R42 has been set to /BUZZER.
Because of this, R42 cannot be set to /BUZZER output when R43 is set to DC output.
Refer to Figure 4.6.8 for the /BUZZER output waveform.

When FOUT output is selected, signal with frequency selected from among nine types, ranging from 256 Hz to 32768 Hz and OSC3 may be output from R42 terminal.
FOUT output is the same as that of /FOUT signal. Note, however, that /FOUT signal becomes antiphase to FOUT signal.

4A-10 R43 output port specification

```
*** OPTION  NO.10 ***

--- R43 OUTPUT PORT SPECIFICATION ---

    OUTPUT SPECIFICATION 1. COMPLEMENTARY
                         2. NCH-OPENDRAIN

PLEASE SELECT NO.(1) ? 1↵

    OUTPUT TYPE          1. DC
                         2. BUZZER

PLEASE SELECT NO.(1) ? 2↵

    OUTPUT SPECIFICATION 1. COMPLEMENTARY  SELECTED
    OUTPUT TYPE          2. BUZZER  SELECTED
```

* When "R42 OUTPUT TYPE" is set to /BUZZER", "DC" option may not be selected.

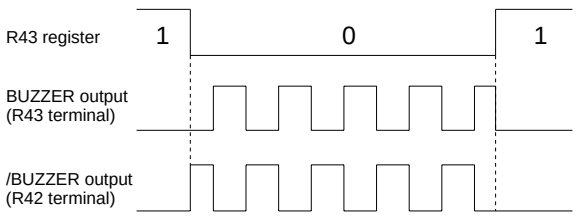

Fig. 4.6.8 Buzzer signal output waveform

Select the specification for R43 terminal.
Either complementary output or Nch open drain output may be selected for the output specification.
For the output type, either DC output or BUZZER output may be selected.
The circuit configuration is the same as that of the R40 output port (Figure 4.6.4).

When DC output is selected, R43 becomes a regular output port. By writing "1" on R43 register, the R43 terminal output goes high (V_{DD}), and goes low (V_{SS}) by writing "0".

When BUZZER output is selected, by writing "0" on R43 register, buzzer signal is output from the R43 terminal, low (V_{SS}) is output by writing "1". When /BUZZER output (buzzer inverted output) is selected for R42 together with R43, it can be directly driven together with piezoelectric buzzer. The control of the /BUZZER output is also accomplished through R43 register.
The BUZZER signal and /BUZZER signal output waveforms are shown in Figure 4.6.8.

4A-11 I/O ports output specification

```
*** OPTION  NO.11 ***
--- I/O PORTS OUTPUT SPECIFICATION ---
        P00-P03          1. COMPLEMENTARY
                         2. NCH-OPENDRAIN
PLEASE SELECT NO.(1) ? 1↵
        P10-P13          1. COMPLEMENTARY
                         2. NCH-OPENDRAIN
PLEASE SELECT NO.(1) ? 1↵
        P20              1. COMPLEMENTARY
                         2. NCH-OPENDRAIN
PLEASE SELECT NO.(1) ? 1↵
        P21              1. COMPLEMENTARY
                         2. NCH-OPENDRAIN
PLEASE SELECT NO.(1) ? 1↵
        P22              1. COMPLEMENTARY
                         2. NCH-OPENDRAIN
PLEASE SELECT NO.(1) ? 1↵
        P23              1. COMPLEMENTARY
                         2. NCH-OPENDRAIN
PLEASE SELECT NO.(1) ? 1↵
        P30              1. COMPLEMENTARY
                         2. NCH-OPENDRAIN
PLEASE SELECT NO.(1) ? 1↵
        P31              1. COMPLEMENTARY
                         2. NCH-OPENDRAIN
PLEASE SELECT NO.(1) ? 1↵
        P32              1. COMPLEMENTARY
                         2. NCH-OPENDRAIN
PLEASE SELECT NO.(1) ? 1↵
        P33              1. COMPLEMENTARY
                         2. NCH-OPENDRAIN
PLEASE SELECT NO.(1) ? 1↵
        P00-P03          1. COMPLEMENTARY  SELECTED
        P10-P13          1. COMPLEMENTARY  SELECTED
        P20              1. COMPLEMENTARY  SELECTED
        P21              1. COMPLEMENTARY  SELECTED
        P22              1. COMPLEMENTARY  SELECTED
        P23              1. COMPLEMENTARY  SELECTED
        P30              1. COMPLEMENTARY  SELECTED
        P31              1. COMPLEMENTARY  SELECTED
        P32              1. COMPLEMENTARY  SELECTED
        P33              1. COMPLEMENTARY  SELECTED
```

Select the output specification to be used during I/O ports (P00–P33) output mode selection.
Either complementary output or Nch open drain output may be selected.
The circuit configuration of the output driver is the same as that of output ports (Figure 4.6.3).
Select complementary output for unused ports.

The I/O port circuit configuration is shown in Figure 4.6.9.

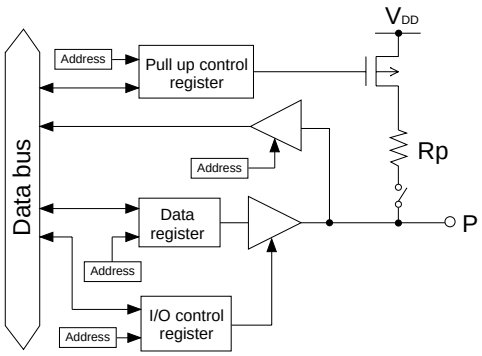

Fig. 4.6.9 Circuit configuration of I/O port

4A-12 P00–P03, P10–P13 I/O ports output type

```
*** OPTION  NO.12 ***
--- P00-P03,P10-P13 I/O PORTS OUTPUT TYPE ---
                      1. DC
                      2. DATA BUS (D0-D7)
PLEASE SELECT NO.(1) ? 2↵
                      2. DATA BUS (D0-D7)  SELECTED
```

Select the output type for P00–P03 and P10–P13 terminals.
When DC output is selected, the terminal becomes a regular I/O port.
When data bus is selected, the I/O port becomes the data bus to external memory device for data output and input. P00–P03 and P10–P13 correspond to D0–D3 and D4–D7, respectively.
For details on external memory access, refer to "E0C6244/4A/4C/48 Technical Manual".

4A-13 P20–P23 I/O ports output type

```
*** OPTION  NO.13 ***

--- P20-P23 I/O PORTS OUTPUT TYPE ---

        P20             1. DC
                        2. CHIP SELECT (/CS0)

PLEASE SELECT NO.(1) ? 2↵

        P21             1. DC
                        2. CHIP SELECT (/CS1)

PLEASE SELECT NO.(1) ? 2↵

        P22             1. DC
                        2. CHIP SELECT (/CS2)

PLEASE SELECT NO.(1) ? 1↵

        P23             1. DC
                        2. CHIP SELECT (/CS3)

PLEASE SELECT NO.(1) ? 1↵

        P20             2. CHIP SELECT (/CS0)  SELECTED
        P21             2. CHIP SELECT (/CS1)  SELECTED
        P22             1. DC  SELECTED
        P23             1. DC  SELECTED
```

Select the output type for P20–P23 terminals.
When DC output is selected, the terminal becomes a regular I/O port.
When chip select is selected, the I/O port becomes a chip select signal for the external memory device. With the "0" written on the corresponding P2x register, the /CS signal goes active when data reading or writing to the external data bus (P00–P03 and P10–P13) is performed.

For details on external memory access, refer to "E0C6244/4A/4C/48 Technical Manual".

4A-14 P30–P33 I/O ports output type

```
*** OPTION  NO.14 ***

--- P30-P33 I/O PORTS OUTPUT TYPE ---

        P20              1. I/O PORT
                         2. OUTPUT PORT

PLEASE SELECT NO.(1) ? 1↵

        P21              1. I/O PORT
                         2. OUTPUT PORT

PLEASE SELECT NO.(1) ? 1↵

        P22              1. I/O PORT
                         2. OUTPUT PORT

PLEASE SELECT NO.(1) ? 1↵

        P23              1. I/O PORT
                         2. OUTPUT PORT

PLEASE SELECT NO.(1) ? 1↵

        P20              1. I/O PORT  SELECTED
        P21              1. I/O PORT  SELECTED
        P22              1. I/O PORT  SELECTED
        P23              1. I/O PORT  SELECTED
```

Select the output type for P30–P33 terminals.
The I/O ports can control the input/output direction according to the I/O control register (IOC3); at "1" and "0" settings, it is set to output port and input port, respectively.
Moreover, when selected as an output port, the I/O port functions as only output port and is not affected by the I/O control register.
In this case, pull up resistors cannot be added.

4A-15 SIN pull up resistor

```
*** OPTION  NO.15 ***

--- SIN PULL UP RESISTOR ---

                         1. WITH RESISTOR
                         2. GATE DIRECT

PLEASE SELECT NO.(1) ? 1↵

                         1. WITH RESISTOR  SELECTED
```

Select whether pull up resistor will be supplemented to SIN terminal of the serial interface.
When "Gate Direct" is selected, take care that input floating state does not occur. Select "With Resistor" for SIN terminal that will not be used.

4A-16 SOUT output specification

```
*** OPTION  NO.16 ***

--- SOUT OUTPUT SPECIFICATION ---

                          1. COMPLEMENTARY
                          2. NCH-OPENDRAIN

PLEASE SELECT NO.(1) ? 1↵

                          1. COMPLEMENTARY  SELECTED
```

Select the output specification for SOUT terminal of the serial interface.
Either complementary output or Nch open drain output may be selected.
Select "Complementary" for SOUT terminal that will not be used.

4A-17 $\overline{SCLK}$ specification

```
*** OPTION  NO.17 ***

--- /SCLK SPECIFICATION ---

    PULL UP RESISTOR      1. WITH RESISTOR
                          2. GATE DIRECT

PLEASE SELECT NO.(1) ? 1↵

    OUTPUT SPECIFICATION 1. COMPLEMENTARY
                          2. NCH-OPENDRAIN

PLEASE SELECT NO.(1) ? 1↵

    PULL UP RESISTOR      1. WITH RESISTOR  SELECTED
    OUTPUT SPECIFICATION 1. COMPLEMENTARY  SELECTED
```

Select the specification for the $\overline{SCLK}$ terminal of the serial interface.

For the pull up resistor, select whether to supplement or not a built-in pull up resistor which will turn ON when in the input mode (external clock mode).

For the output specification, either complementary output or Nch open drain output may be selected.
Select "With Resistor" and "Complementary" for $\overline{SCLK}$ terminal that will not be used.

4A-18 SIO data permutation

```
*** OPTION  NO.18 ***

--- SIO DATA PERMUTATION ---

                          1. MSB FIRST
                          2. LSB FIRST

PLEASE SELECT NO.(1) ? 1↵

                          1. MSB FIRST  SELECTED
```

Select whether the serial interface input/output (SIN or SOUT) data bit permutation will be MSB first or LSB first.
Select the one suitable to your programming needs.
Input/output data permutation is shown in Figure 4.6.10.

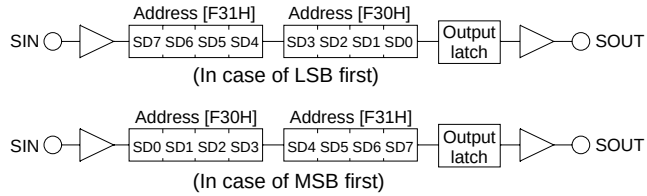

Fig. 4.6.10
Input/output data permutation

4A-19 LCD power voltage mode

```
*** OPTION  NO.19 ***

--- LCD POWER VOLTAGE MODE ---

                          1. INTERNAL VOLTAGE
                          2. EXTERNAL VOLTAGE

PLEASE SELECT NO.(1) ? 1↵

                          1. INTERNAL VOLTAGE  SELECTED
```

Select the power mode for the LCD driver.
When internal voltage is selected, the LCD power source built in the E0C624A is used and driving is fixed at 1/4 bias. In this case, the LCD contrast may be adjusted through the software.
When external voltage is selected, the LCD driving voltage is externally supplied. Aside from 1/4 bias, driving may also be set at 1/5 bias. Adjustment of the LCD contrast in this case requires setting up of external components.

4.7 E0C624C/48 Option Specifications and Selection Message

Screen that can be selected as function options set on the E0C624C/48 are shown below, and their specifications are also described.

4C/48-1 OSC1 oscillator

```
*** OPTION  NO.1 ***

--- OSC1 OSCILLATOR ---

                          1. CRYSTAL
                          2. CR

PLEASE SELECT NO.(1) ? 1↵

                          1. CRYSTAL  SELECTED
```

Select oscillation circuit that uses OSC1 and OSC2. To minimize external components, CR oscillation circuit would be suitable; to obtain a stable oscillation frequency, crystal oscillation circuit would be suitable. When CR oscillation circuit is selected, only resistor is needed as external components since capacities are built-in.
On the other hand, when crystal oscillation circuit is selected, crystal oscillator and trimmer capacity are needed as external components. Although when crystal oscillation circuit is selected, it is fixed at 32.768 kHz, when CR oscillation circuit is selected, frequency may be modified to a certain extent depending on the resistance of external components.

4C/48-2 OSC3 oscillator

```
*** OPTION  NO.2 ***

--- OSC3 OSCILLATOR ---

                          1. CR
                          2. CERAMIC

PLEASE SELECT NO.(1) ? 1↵

                          1. CR  SELECTED
```

Select oscillation circuit that uses OSC3 and OSC4. To minimize external components, CR oscillation circuit would be suitable; to obtain a stable oscillation frequency, ceramic oscillation circuit would be suitable. When CR oscillation circuit is selected, only resistor is needed as external components since capacities are built-in.
On the other hand, when ceramic oscillation circuit is selected, ceramic oscillator, feedback resistor, gate capacity and drain capacity are needed as external components.
Select CR oscillation circuit for unused OSC3 system clock.

4C/48-3 Multiple key entry reset

```
*** OPTION  NO.3 ***

--- MULTIPLE KEY ENTRY RESET ---

                          1. NOT USE
                          2. USE K00,K01
                          3. USE K00,K01,K02
                          4. USE K00,K01,K02,K03

PLEASE SELECT NO.(1) ? 2↵

                          2. USE K00,K01  SELECTED
```

The reset function is set when K00 through K03 are entered.
When "Not Use" is selected, the reset function is not activated even if K00 through K03 are entered.
When "Use K00, K01" is selected, the system is reset immediately the K00 and K01 inputs go low at the same time. Similarly, the system is reset as soon as the K00 through K02 inputs or the K00 through K03 inputs go low.

The system is reset when a low signal is input for more than 2 seconds.

The system reset circuit is shown in Figure 4.7.1.

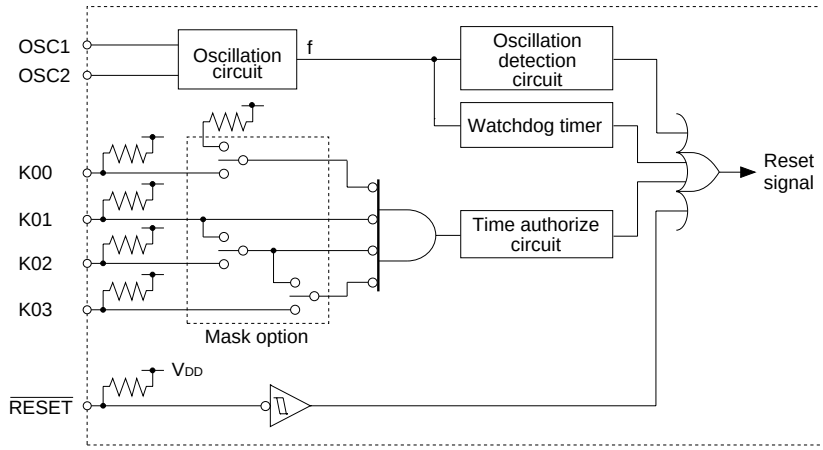

Fig. 4.7.1 System reset circuit

4C/48-4 Input ports pull up resistor

```
*** OPTION  NO.4 ***

--- INPUT PORTS PULL UP RESISTOR ---

        K00             1. WITH RESISTOR
                        2. GATE DIRECT

PLEASE SELECT NO.(1) ? 2↵

        K01             1. WITH RESISTOR
                        2. GATE DIRECT

PLEASE SELECT NO.(1) ? 2↵

        K02             1. WITH RESISTOR
                        2. GATE DIRECT

PLEASE SELECT NO.(1) ? 2↵

        K03             1. WITH RESISTOR
                        2. GATE DIRECT

PLEASE SELECT NO.(1) ? 2↵

        K10             1. WITH RESISTOR
                        2. GATE DIRECT

PLEASE SELECT NO.(1) ? 1↵

        K11             1. WITH RESISTOR
                        2. GATE DIRECT

PLEASE SELECT NO.(1) ? 1↵

        K12             1. WITH RESISTOR
                        2. GATE DIRECT

PLEASE SELECT NO.(1) ? 1↵

        K13             1. WITH RESISTOR
                        2. GATE DIRECT

PLEASE SELECT NO.(1) ? 1↵

        K00             2. GATE DIRECT  SELECTED
        K01             2. GATE DIRECT  SELECTED
        K02             2. GATE DIRECT  SELECTED
        K03             2. GATE DIRECT  SELECTED
        K10             1. WITH RESISTOR  SELECTED
        K11             1. WITH RESISTOR  SELECTED
        K12             1. WITH RESISTOR  SELECTED
        K13             1. WITH RESISTOR  SELECTED
```

Select whether input ports (K00–K03 and K10–K13) will each be supplemented with pull up resistors or not. When "Gate Direct" is selected, see to it that entry floating state does not occur. Select "With Resistor" pull up resistor for unused ports. Moreover, the input port status is changed from low level (VSS) to high (VDD) with pull up resistors, a delay of approximately 500 µsec in waveform rise time will occur depending on the pull up resistor and entry load time constant. Because of this, when input reading is to be conducted, ensure the appropriate wait time with the program.
The configuration of the pull up resistor circuit is shown in Figure 4.7.2.

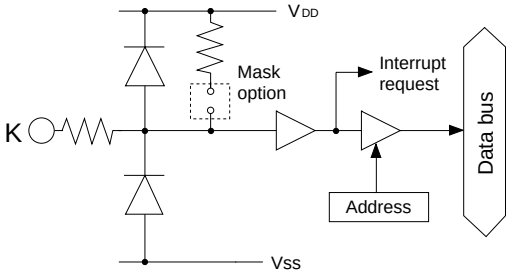

Fig. 4.7.2 Configuration of pull up resistor circuit

4C/48-5 Output ports output specification

```
*** OPTION  NO.5 ***
--- OUTPUT PORTS OUTPUT SPECIFICATION ---
        R00-R03         1. COMPLEMENTARY
                        2. NCH-OPENDRAIN
PLEASE SELECT NO.(1) ? 1↵
        R10-R13         1. COMPLEMENTARY
                        2. NCH-OPENDRAIN
PLEASE SELECT NO.(1) ? 1↵
        R20-R22         1. COMPLEMENTARY
                        2. NCH-OPENDRAIN
PLEASE SELECT NO.(1) ? 1↵
        R23             1. COMPLEMENTARY
                        2. NCH-OPENDRAIN
PLEASE SELECT NO.(1) ? 2↵
        R30             1. COMPLEMENTARY
                        2. NCH-OPENDRAIN
PLEASE SELECT NO.(1) ? 2↵
        R31             1. COMPLEMENTARY
                        2. NCH-OPENDRAIN
PLEASE SELECT NO.(1) ? 1↵
        R32             1. COMPLEMENTARY
                        2. NCH-OPENDRAIN
PLEASE SELECT NO.(1) ? 1↵
        R00-R03         1. COMPLEMENTARY  SELECTED
        R10-R13         1. COMPLEMENTARY  SELECTED
        R20-R22         1. COMPLEMENTARY  SELECTED
        R23             2. NCH-OPENDRAIN  SELECTED
        R30             2. NCH-OPENDRAIN  SELECTED
        R31             1. COMPLEMENTARY  SELECTED
        R32             1. COMPLEMENTARY  SELECTED
```

Select the output specification for the output ports (R00–R32).
Either complementary output or Nch open drain output may be selected.
When output port is to be used on key matrix configuration, select Nch open drain output.
For unused output ports, select complementary output.
The output circuit configuration is shown in Figure 4.7.3.

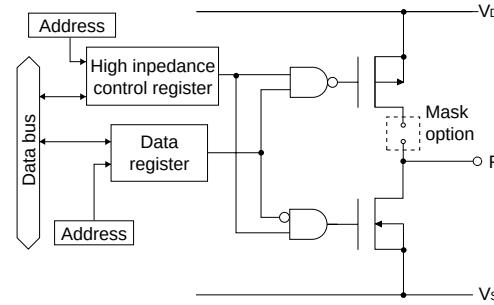

Fig. 4.7.3 Configuration of output circuit

4C/48-6 Output ports output type

```
*** OPTION  NO.6 ***
--- OUTPUT PORTS OUTPUT TYPE ---
        R00-R03       1. DC
                      2. ADDRESS BUS (A0-A3)
PLEASE SELECT NO.(1) ? 2↵
        R10-R13       1. DC
                      2. ADDRESS BUS (A4-A7)
PLEASE SELECT NO.(1) ? 2↵
        R20-R22       1. DC
                      2. ADDRESS BUS (A8-A10)
PLEASE SELECT NO.(1) ? 2↵
        R23           1. DC
                      2. ADDRESS BUS (A11)
```

Select the output type of the output ports.
When DC output is selected, the output port becomes a regular output port.
When address bus is selected, the output port becomes the address bus to the external memory device and the writing data to the register is output to the address bus.

```
PLEASE SELECT NO.(1) ? 1↵
        R30           1. DC
                      2. ADDRESS BUS (A12)*
PLEASE SELECT NO.(1) ? 1↵
        R31           1. DC
                      2. WRITE (/WR)
PLEASE SELECT NO.(1) ? 2↵
        R32           1. DC
                      2. READ (/RD)
PLEASE SELECT NO.(1) ? 2↵
        R00-R03       2. ADDRESS BUS (A0-A3) SELECTED
        R10-R13       2. ADDRESS BUS (A4-A7) SELECTED
        R20-R22       2. ADDRESS BUS (A8-A10) SELECTED
        R23           1. DC SELECTED
        R30           1. DC SELECTED
        R31           2. WRITE (/WR) SELECTED
        R32           2. READ (/RD) SELECTED
```

When /WR is selected for R31, /WR (write) signal is output from R31 terminal by writing the high order 4 bits (P10–P13) of the data bus.
When /RD is selected for R32, /RD (read) signal is output from R32 terminal by reading the low order 4 bits (P00–P03) of the data bus.
When /WR and /RD are selected, R31 and R32 registers may be used as a 1 bit general purpose register capable of read/write functions.

For details on external memory access, refer to the "E0C6244/4A/4C/48 Technical Manual".

* When DC output is designated for low-order ports, ports of higher orders cannot be given address bus selections.

4C/48-7 R33 output port specification

```
*** OPTION  NO.7 ***

--- R33 OUTPUT PORT SPECIFICATION ---

    OUTPUT SPECIFICATION 1. COMPLEMENTARY
                         2. NCH-OPENDRAIN

PLEASE SELECT NO.(1) ? 1↵

    OUTPUT TYPE          1. DC (PTCLK)
                         2. /SRDY

PLEASE SELECT NO.(1) ? 2↵

    OUTPUT CONTROL       1. 3 STATE
                         2. 2 STATE

PLEASE SELECT NO.(1) ? 2↵

    OUTPUT SPECIFICATION 1. COMPLEMENTARY  SELECTED
    OUTPUT TYPE          2. /SRDY  SELECTED
    OUTPUT CONTROL       2. 2 STATE  SELECTED
```

Select the specification for R33 terminal.
Either complementary output or Nch open drain output may be selected for the output specification.
Either DC output (or PTCLK output) or /SRDY output may be selected for the output type.
When DC (PTCLK) output is selected, R33 will either become a regular output port terminal (PTCOUT = "0") or an operating clock output terminal for the programmable timer (PTCOUT = "1").
When /SRDY is selected, a Ready signal indicating whether the serial interface is available for receiving or transmitting is output from R33.
For the output control, either 3-state or 2-state may be selected.
When /SRDY is selected for the output type, 2-state is normally selected for the output control.
When DC (PTCLK) is selected, 2-state may also be selected but caution is required because output becomes insufficient during initial reset.
The circuit configuration is the same as that of output ports (Figure 4.7.3).

4C/48-8 R40 output port specification

```
*** OPTION  NO.8 ***

--- R40 OUTPUT PORT SPECIFICATION ---

    OUTPUT SPECIFICATION 1. COMPLEMENTARY
                         2. NCH-OPENDRAIN

PLEASE SELECT NO.(1) ? 1↵

    OUTPUT TYPE          1. DC
                         2. CL-16 (FOR SED1521FAA)
                         3. CL-8  (FOR SED1521FAA)
                         4. /FOUT   256 [HZ]
                         5. /FOUT   512 [HZ]
                         6. /FOUT  1024 [HZ]
                         7. /FOUT  2048 [HZ]
                         8. /FOUT  4096 [HZ]
                         9. /FOUT  8192 [HZ]
                         10./FOUT 16384 [HZ]
                         11./FOUT 32768 [HZ]
                         12./FOUT OSC3

PLEASE SELECT NO.(1) ? 1↵

    OUTPUT SPECIFICATION 1. COMPLEMENTARY  SELECTED
    OUTPUT TYPE          1. DC  SELECTED
```

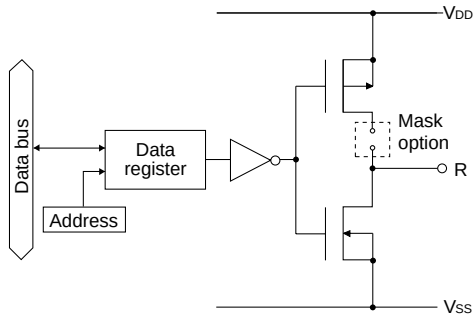

Fig. 4.7.4 Output circuit configuration of R4 port

Select the specification for R40 terminal.
Either complementary output or Nch open drain output may be selected for the output specification.
Any one of the following may be selected for the output type: DC output, CL output or /FOUT output.
The output circuit configuration of R4 port is shown in Figure 4.7.4.

When DC output is selected

When DC output is selected, R40 becomes a regular output port. By writing "1" on R40 register, the R40 terminal output goes high (V_{DD}), and goes low (V_{SS}) by writing "0".
The output waveform is shown in Figure 4.7.5.

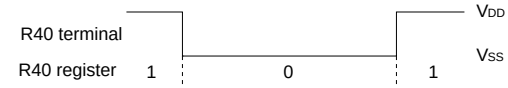

Fig. 4.7.5 Output waveform at DC output selection

When CL output is selected

When expansion LCD driver (SED1521FAA) is externally connected, selection of the CL output will cause R40 terminal to output LCD synchronous signal. The CL signal can select from one of two types, the CL-16 for 1/16 duty or the CL-8 for 1/8 duty. The respective frequency of CL-16 signal and CL-8 signal are 1024 Hz and 512 Hz. The CL signal can be output to R40 terminal by writing "0" on R40 register. Moreover, FR signal (LCD frame signal, 32 Hz) may be selected through mask option of the R41 terminal.
The CL signal and FR signal output waveforms are shown in Figure 4.7.6.

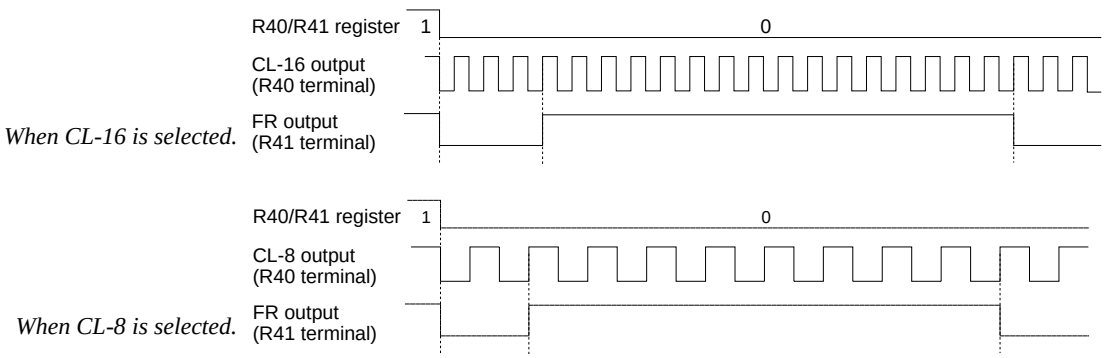

Fig. 4.7.6 CL signal and FR signal output waveforms

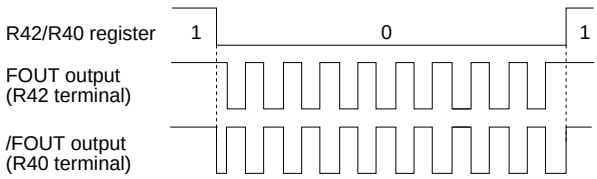

Fig. 4.7.7 FOUT signal and /FOUT signal output waveforms

When /FOUT output is selected

When /FOUT output is selected, signal with frequency selected from among nine types, ranging from 256 Hz to 32768 Hz and OSC3 may be output from R40 terminal.
In this case, by writing "0" on R40 register, 50% duty and V_{DD}–V_{SS} amplitude square wave is output from R40 terminal at the specified frequency. Writing "1" will cause the R40 terminal to go high (V_{DD}).
The /FOUT output is normally used to supply clock to other devices but since hazard occurs when R40 register is re-written, great caution must be observed when using it.
Moreover, FOUT output may be selected in the same manner through the R42 terminal mask option. Note, however, that FOUT signal becomes antiphase to /FOUT signal.
The output waveform is shown in Figure 4.7.7.

4C/48-9 R41 output port specification

```
*** OPTION  NO.9 ***

--- R41 OUTPUT PORT SPECIFICATION ---

    OUTPUT SPECIFICATION 1. COMPLEMENTARY
                         2. NCH-OPENDRAIN

PLEASE SELECT NO.(1) ? 1↲

    OUTPUT TYPE          1. DC
                         2. FR (FOR SED1521FAA)

PLEASE SELECT NO.(1) ? 1↲

    OUTPUT SPECIFICATION 1. COMPLEMENTARY  SELECTED
    OUTPUT TYPE          1. DC  SELECTED
```

Select the specification for R41 terminal.
Either complementary output or Nch open drain output may be selected for the output specification.
For the output type, either DC output or FR output may be selected.
The circuit configuration is the same as that of the R40 output port (Figure 4.7.4).

When DC output is selected, R41 becomes a regular output port. By writing "1" on R41 register, the R41 terminal output goes high (V_{DD}), and goes low (V_{SS}) by writing "0".

When expansion LCD driver (SED1521FAA) is externally connected, selection of the FR output will cause R41 terminal to output LCD frame signal (32 Hz).
In this case, FR signal can be output from R41 terminal by writing "0" on R41 register.
Refer to Figure 4.7.6 for FR signal output.

4C/48-10 R42 output port specification

```
*** OPTION  NO.10 ***

--- R42 OUTPUT PORT SPECIFICATION ---

    OUTPUT SPECIFICATION 1. COMPLEMENTARY
                         2. NCH-OPENDRAIN

PLEASE SELECT NO.(1) ? 1↲
```

Select the specification for R42 terminal.
Either complementary output or Nch open drain output may be selected for the output specification.
Any one of the following may be selected for the output type: DC output, /BUZZER output or /FOUT output.
The circuit configuration is the same as that of the R40 output port (Figure 4.7.4).

```
    OUTPUT TYPE          1. DC
                         2. /BUZZER (R43 CONT)
                         3. FOUT   256 [HZ]
                         4. FOUT   512 [HZ]
                         5. FOUT  1024 [HZ]
                         6. FOUT  2048 [HZ]
                         7. FOUT  4096 [HZ]
                         8. FOUT  8192 [HZ]
                         9. FOUT 16384 [HZ]
                         10.FOUT 32768 [HZ]
                         11.FOUT OSC3

PLEASE SELECT NO.(1) ? 11↵

    OUTPUT SPECIFICATION 1. COMPLEMENTARY  SELECTED
    OUTPUT TYPE          11.FOUT OSC3  SELECTED
```

When DC output is selected, R42 becomes a regular output port. By writing "1" on R42 register, the R42 terminal output goes high (V_{DD}), and goes low (V_{SS}) by writing "0".

When BUZZER output is selected with the R43 mask option, /BUZZER output becomes a buzzer inverted signal for direct driving of the piezoelectric buzzer together with the BUZZER output. The control of the buzzer signal output is accomplished through R43 register even if R42 has been set to /BUZZER.
Because of this, R42 cannot be set to /BUZZER output when R43 is set to DC output.
Refer to Figure 4.7.8 for the /BUZZER output waveform.

When FOUT output is selected, signal with frequency selected from among nine types, ranging from 256 Hz to 32768 Hz and OSC3 may be output from R42 terminal.
FOUT output is the same as that of /FOUT signal. Note, however, that /FOUT signal becomes antiphase to FOUT signal.

4C/48-11 R43 output port specification

```
*** OPTION  NO.11 ***

--- R43 OUTPUT PORT SPECIFICATION ---

    OUTPUT SPECIFICATION 1. COMPLEMENTARY
                         2. NCH-OPENDRAIN

PLEASE SELECT NO.(1) ? 1↵

    OUTPUT TYPE          1. DC
                         2. BUZZER

PLEASE SELECT NO.(1) ? 2↵

    OUTPUT SPECIFICATION 1. COMPLEMENTARY  SELECTED
    OUTPUT TYPE          2. BUZZER  SELECTED
```

* When "R42 OUTPUT TYPE" is set to /BUZZER", "DC" option may not be selected.

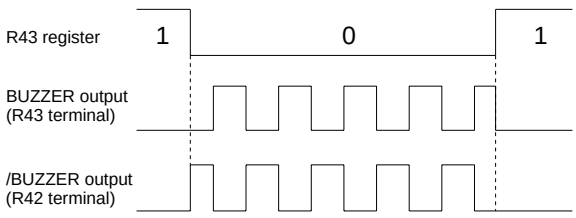

Fig. 4.7.8 Buzzer signal output waveform

Select the specification for R43 terminal.
Either complementary output or Nch open drain output may be selected for the output specification.
For the output type, either DC output or BUZZER output may be selected.
The circuit configuration is the same as that of the R40 output port (Figure 4.7.4).

When DC output is selected, R43 becomes a regular output port. By writing "1" on R43 register, the R43 terminal output goes high (V_{DD}), and goes low (V_{SS}) by writing "0".

When BUZZER output is selected, by writing "0" on R43 register, buzzer signal is output from the R43 terminal, low (V_{SS}) is output by writing "1". When /BUZZER output (buzzer inverted output) is selected for R42 together with R43, it can be directly driven together with piezoelectric buzzer. The control of the /BUZZER output is also accomplished through R43 register.
The BUZZER signal and /BUZZER signal output waveforms are shown in Figure 4.7.8.

4C/48-12 I/O ports output specification

```
*** OPTION  NO.12 ***
--- I/O PORTS OUTPUT SPECIFICATION ---
        P00-P03          1. COMPLEMENTARY
                         2. NCH-OPENDRAIN
PLEASE SELECT NO.(1) ? 1↵
        P10-P13          1. COMPLEMENTARY
                         2. NCH-OPENDRAIN
PLEASE SELECT NO.(1) ? 1↵
        P20              1. COMPLEMENTARY
                         2. NCH-OPENDRAIN
PLEASE SELECT NO.(1) ? 1↵
        P21              1. COMPLEMENTARY
                         2. NCH-OPENDRAIN
PLEASE SELECT NO.(1) ? 1↵
        P22              1. COMPLEMENTARY
                         2. NCH-OPENDRAIN
PLEASE SELECT NO.(1) ? 1↵
        P23              1. COMPLEMENTARY
                         2. NCH-OPENDRAIN
PLEASE SELECT NO.(1) ? 1↵
        P30              1. COMPLEMENTARY
                         2. NCH-OPENDRAIN
PLEASE SELECT NO.(1) ? 1↵
        P31              1. COMPLEMENTARY
                         2. NCH-OPENDRAIN
PLEASE SELECT NO.(1) ? 1↵
        P32              1. COMPLEMENTARY
                         2. NCH-OPENDRAIN
PLEASE SELECT NO.(1) ? 1↵
        P33              1. COMPLEMENTARY
                         2. NCH-OPENDRAIN
PLEASE SELECT NO.(1) ? 1↵
        P00-P03          1. COMPLEMENTARY  SELECTED
        P10-P13          1. COMPLEMENTARY  SELECTED
        P20              1. COMPLEMENTARY  SELECTED
        P21              1. COMPLEMENTARY  SELECTED
        P22              1. COMPLEMENTARY  SELECTED
        P23              1. COMPLEMENTARY  SELECTED
        P30              1. COMPLEMENTARY  SELECTED
        P31              1. COMPLEMENTARY  SELECTED
        P32              1. COMPLEMENTARY  SELECTED
        P33              1. COMPLEMENTARY  SELECTED
```

Select the output specification to be used during I/O ports (P00–P33) output mode selection.
Either complementary output or Nch open drain output may be selected.
The circuit configuration of the output driver is the same as that of output ports (Figure 4.7.3).
Select complementary output for unused ports.

The I/O port circuit configuration is shown in Figure 4.7.9.

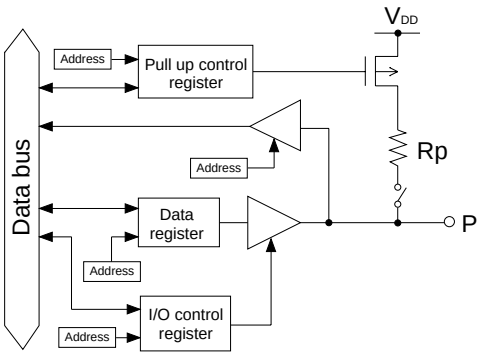

Fig. 4.7.9 Circuit configuration of I/O port

4C/48-13 P00–P03, P10–P13 I/O ports output type

```
*** OPTION  NO.13 ***
--- P00-P03,P10-P13 I/O PORTS OUTPUT TYPE ---
                      1. DC
                      2. DATA BUS (D0-D7)
PLEASE SELECT NO.(1) ? 2↵
                      2. DATA BUS (D0-D7)  SELECTED
```

Select the output type for P00–P03 and P10–P13 terminals.
When DC output is selected, the terminal becomes a regular I/O port.
When data bus is selected, the I/O port becomes the data bus to external memory device for data output and input. P00–P03 and P10–P13 correspond to D0–D3 and D4–D7, respectively.
For details on external memory access, refer to "E0C6244/4A/4C/48 Technical Manual".

4C/48-14 P20–P23 I/O ports output type

```
*** OPTION  NO.14 ***

--- P20-P23 I/O PORTS OUTPUT TYPE ---

       P20            1. DC
                      2. CHIP SELECT (/CS0)

PLEASE SELECT NO.(1) ? 2↵

       P21            1. DC
                      2. CHIP SELECT (/CS1)

PLEASE SELECT NO.(1) ? 2↵

       P22            1. DC
                      2. CHIP SELECT (/CS2)

PLEASE SELECT NO.(1) ? 1↵

       P23            1. DC
                      2. CHIP SELECT (/CS3)

PLEASE SELECT NO.(1) ? 1↵

       P20            2. CHIP SELECT (/CS0)  SELECTED
       P21            2. CHIP SELECT (/CS1)  SELECTED
       P22            1. DC  SELECTED
       P23            1. DC  SELECTED
```

Select the output type for P20–P23 terminals.
When DC output is selected, the terminal becomes a regular I/O port.
When chip select is selected, the I/O port becomes a chip select signal for the external memory device. With the "0" written on the corresponding P2x register, the /CS signal goes active when data reading or writing to the external data bus (P00–P03 and P10–P13) is performed.

For details on external memory access, refer to "E0C6244/4A/4C/48 Technical Manual".

4C/48-15 P30–P33 I/O ports output type

```
*** OPTION  NO.15 ***

--- P30-P33 I/O PORTS OUTPUT TYPE ---

       P20             1. I/O PORT
                       2. OUTPUT PORT

PLEASE SELECT NO.(1) ? 1↵

       P21             1. I/O PORT
                       2. OUTPUT PORT

PLEASE SELECT NO.(1) ? 1↵

       P22             1. I/O PORT
                       2. OUTPUT PORT

PLEASE SELECT NO.(1) ? 1↵

       P23             1. I/O PORT
                       2. OUTPUT PORT

PLEASE SELECT NO.(1) ? 1↵

       P20             1. I/O PORT  SELECTED
       P21             1. I/O PORT  SELECTED
       P22             1. I/O PORT  SELECTED
       P23             1. I/O PORT  SELECTED
```

Select the output type for P30–P33 terminals.
The I/O ports can control the input/output direction according to the I/O control register (IOC3); at "1" and "0" settings, it is set to output port and input port, respectively.
Moreover, when selected as an output port, the I/O port functions as only output port and is not affected by the I/O control register.
In this case, pull up resistors cannot be added.

4C/48-16 SIN pull up resistor

```
*** OPTION  NO.16 ***

--- SIN PULL UP RESISTOR ---

                       1. WITH RESISTOR
                       2. GATE DIRECT

PLEASE SELECT NO.(1) ? 1↵

                       1. WITH RESISTOR  SELECTED
```

Select whether pull up resistor will be supplemented to SIN terminal of the serial interface.
When "Gate Direct" is selected, take care that input floating state does not occur. Select "With Resistor" for SIN terminal that will not be used.

4C/48-17 SOUT output specification

```
*** OPTION  NO.17 ***

--- SOUT OUTPUT SPECIFICATION ---

                          1. COMPLEMENTARY
                          2. NCH-OPENDRAIN

PLEASE SELECT NO.(1) ? 1↵

                          1. COMPLEMENTARY  SELECTED
```

Select the output specification for SOUT terminal of the serial interface.
Either complementary output or Nch open drain output may be selected.
Select "Complementary" for SOUT terminal that will not be used.

4C/48-18 $\overline{SCLK}$ specification

```
*** OPTION  NO.18 ***

--- /SCLK SPECIFICATION ---

    PULL UP RESISTOR      1. WITH RESISTOR
                          2. GATE DIRECT

PLEASE SELECT NO.(1) ? 1↵

    OUTPUT SPECIFICATION 1. COMPLEMENTARY
                          2. NCH-OPENDRAIN

PLEASE SELECT NO.(1) ? 1↵

    PULL UP RESISTOR      1. WITH RESISTOR  SELECTED
    OUTPUT SPECIFICATION 1. COMPLEMENTARY  SELECTED
```

Select the specification for the $\overline{SCLK}$ terminal of the serial interface.

For the pull up resistor, select whether to supplement or not a built-in pull up resistor which will turn ON when in the input mode (external clock mode).

For the output specification, either complementary output or Nch open drain output may be selected.
Select "With Resistor" and "Complementary" for $\overline{SCLK}$ terminal that will not be used.

4C/48-19 SIO data permutation

```
*** OPTION  NO.19 ***

--- SIO DATA PERMUTATION ---

                          1. MSB FIRST
                          2. LSB FIRST

PLEASE SELECT NO.(1) ? 1↵

                          1. MSB FIRST  SELECTED
```

Select whether the serial interface input/output (SIN or SOUT) data bit permutation will be MSB first or LSB first.
Select the one suitable to your programming needs.
Input/output data permutation is shown in Figure 4.7.10.

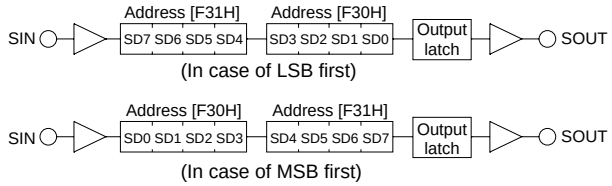

Fig. 4.7.10
Input/output data permutation

4C/48-20 LCD power voltage mode

```
*** OPTION  NO.20 ***

--- LCD POWER VOLTAGE MODE ---

                          1. INTERNAL VOLTAGE
                          2. EXTERNAL VOLTAGE

PLEASE SELECT NO.(1) ? 1↵

                          1. INTERNAL VOLTAGE  SELECTED
```

Select the power mode for the LCD driver.
When internal voltage is selected, the LCD power source built in the E0C624C/48 is used and driving is fixed at 1/4 bias. In this case, the LCD contrast may be adjusted through the software.
When external voltage is selected, the LCD driving voltage is externally supplied. Aside from 1/4 bias, driving may also be set at 1/5 bias. Adjustment of the LCD contrast in this case requires setting up of external components.

4.8 FOG6244/4A/4C/48 Quick Reference

■ Starting command and input/output files

Execution file: FOG6244/4A/4C/48.EXE

Starting command: **FOG624✻↵**

↵ indicates the Return key.
4✻ indicates the model name (44, 4A, 4C or 48).

Input file: C24✻XXXF.DOC (Function option document file, when modifying)

Output file: C24✻XXXF.DOC (Function option document file)
C24✻XXXF.HEX (Function option HEX file)

■ Display example (In case of E0C6244)

```
     ***  E0C6244 FUNCTION OPTION GENERATOR. --- Ver 3.12  ***

EEEEEEEEEE   PPPPPPPP        SSSSSSS       OOOOOOOO      NNN      NNN
EEEEEEEEEE   PPPPPPPPPP     SSS   SSSS    OOO    OOO     NNNN     NNN
EEE          PPP     PPP   SSS     SSS   OOO      OOO    NNNNN    NNN
EEE          PPP     PPP    SSS          OOO      OOO    NNNNNN   NNN
EEEEEEEEEE   PPPPPPPPPP      SSSSSS      OOO      OOO    NNN NNN NNN
EEEEEEEEEE   PPPPPPPP           SSSS     OOO      OOO    NNN  NNNNNN
EEE          PPP                 SSS    OOO      OOO    NNN   NNNNN
EEE          PPP           SSS     SSS   OOO      OOO    NNN    NNNN
EEEEEEEEEE   PPP           SSSS    SSS    OOO    OOO     NNN     NNN
EEEEEEEEEE   PPP             SSSSSSS       OOOOOOOO      NNN      NN

             (C) COPYRIGHT 1991  SEIKO EPSON CORP.

        THIS SOFTWARE MAKES NEXT FILES.

           C244XXXF.HEX  ...  FUNCTION OPTION HEX FILE.
           C244XXXF.DOC  ...  FUNCTION OPTION DOCUMENT FILE.

                      STRIKE ANY KEY.
```

Start-up message
When FOG6244/4A/4C/48 is started, the start-up message is displayed.
For "STRIKE ANY KEY.", press any key to advance the program execution.

To suspend execution, press the "CTRL" and "C" keys together: the sequence returns to the DOS command level.

```
*** E0C6244 USER'S OPTION SETTING. --- Ver 3.12 ***

CURRENT DATE IS  92/02/14
PLEASE INPUT NEW DATE  :   92/02/17↵
```

Date input
Enter the 2-digit year, month, and day of the month by delimiting them with a slash ("/"). When not modifying the date, press the RETURN key "↵" to continue.

```
*** OPERATION SELECT MENU ***

       1. INPUT NEW FILE
       2. EDIT FILE
       3. RETURN TO DOS

PLEASE SELECT NO.?
```

Operation selection menu
Enter a number from 1 to 3 to select a subsequent operation.
1. To set new function options.
2. To modify the document file.
3. To terminate FOG6244/4A/4C/48.

```
*** OPERATION SELECT MENU ***

       1. INPUT NEW FILE
       2. EDIT FILE
       3. RETURN TO DOS

PLEASE SELECT NO.? 1↵
PLEASE INPUT FILE NAME? C2440A0↵                              ..(1)
PLEASE INPUT USER'S NAME? SEIKO EPSON CORP.↵                  ..(2)
PLEASE INPUT ANY COMMENT
(ONE LINE IS 50 CHR)? ED MARKETING DEPARTMENT↵                ..(3)
                    ? 421-8 HINO HINO-SHI TOKYO 191-8501 JAPAN↵
                    ? TEL 042-587-5816↵
                    ? FAX 042-587-5624↵
                    ? ↵
```

Setting new function options
Select "1" on the operation selection menu.
(1) Enter the file name.
(2) Enter the customer's company name.
(3) Enter any comment.
(Within 50 characters x 10 lines)
Next, start function option setting from option No. 1.

```
PLEASE INPUT FILE NAME? C2440A0↵
EXISTS OVERWRITE(Y/N)? N↵
PLEASE INPUT FILE NAME? C2440B0↵
PLEASE INPUT USER'S NAME?
```

In case a function option document file with the same name as the file name specified in the current drive exists, the user is asked whether overwrition is desired. Enter "Y" or "N" accordingly.

```
*** OPERATION SELECT MENU ***

        1. INPUT NEW FILE
        2. EDIT FILE
        3. RETURN TO DOS

PLEASE SELECT NO.? 2↵

*** SOURCE FILE(S) ***

C2440A0         C2440B0         C2440C0                 ..(1)

PLEASE INPUT FILE NAME? C2440A0↵                        ..(2)
PLEASE INPUT USER'S NAME?↵                              ..(3)
PLEASE INPUT ANY COMMENT
(ONE LINE IS 50 CHR)?↵                                  ..(4)
PLEASE INPUT EDIT NO.? 4↵                               ..(5)
            :
(Modifying function option settings)
            :
PLEASE INPUT EDIT NO.? E↵
```

In step (1), if no modifiable source exists, the following message is displayed and the sequence returns to the operation selection menu.

```
*** SOURCE FILE(S) ***

FUNCTION OPTION DOCUMENT FILE IS NOT FOUND.
```

In step (2), if the function option document file is not in the current drive, the following message is displayed, prompting entry of other file name.

```
PLEASE INPUT FILE NAME? C2440N0↵
FUNCTION OPTION DOCUMENT FILE IS NOT FOUND.
PLEASE INPUT FILE NAME?
```

```
BAD FUNCTION OPTION DOCUMENT FILE
```

```
*** OPTION  NO.3 ***

— MULTIPLE KEY ENTRY RESET —

                      1. Not Use
                      2. Use  K00,K01
                      3. Use  K00,K01,K02
                      4. Use  K00,K01,K02,K03

PLEASE SELECT  NO.(1) ? 2↵

                      2. Use  K00,K01  SELECTED
```

```
END OF OPTION SETTING.
DO YOU MAKE HEX FILE (Y/N) ? Y↵                         ..(1)

*** OPTION EPROM SELECT MENU ***

        1. 27C64
        2. 27C128
        3. 27C256
        4. 27C512

PLEASE SELECT NO.? 2↵                                   ..(2)

        2. 27C128   SELECTED

MAKING FILE(S) IS COMPLETED.

*** OPERATION SELECT MENU ***

        1. INPUT NEW FILE
        2. EDIT FILE
        3. RETURN TO DOS

PLEASE SELECT NO.?
```

Modifying function option settings

Select "2" on the operation selection menu.

(1) Will display the files on the current drive.
(2) Enter the file name.
(3) Enter the customer's company name.
(4) Enter any comment.
    Previously entered data can be used by pressing the RETURN key "↵" at (3) and (4).
(5) Enter the number of the function option to be modified. When selection of one option is complete, the system prompts entry of another function option number. Repeat selection until all options to be modified are selected.
    Enter "E↵" to end option setting. Then, move to the confirmation procedure for HEX file generation.

In case of the file format specified by step (2) is not corrent (such as document file of other model), the message will be displayed and the FOG6244/4A/4C/48 program will be terminated.

Option selection

The selections for each option correspond one to one to the option list. Enter the selection number. The value in parentheses ( ) indicates the default value, and is set when only the RETURN key "↵" is pressed.
In return, the confirmation is displayed.
When you wish to modify previously set function options in the new setting process, enter "B↵" to return 1 step back to the previous function option setting operation.

EPROM selection

When setting function options setting is completed, the following message is output to ask the operator whether to generate the HEX file.

(1) When debugging the program with EVA6248, HEX file is needed, so enter "Y↵". If "N↵" is entered, no HEX file is generated and only document file is generated.
(2) For the option ROM selection menu displayed when "Y↵" is entered in Step (1), select the EPROM to be used for setting EVA6248 options.

When a series of operations are complete, the sequence returns to the operation selection menu.

4.9 Sample Files

■ Example of E0C6244 function option document file

```
* E0C6244 FUNCTION OPTION DOCUMENT  V 3.12
*
* FILE NAME    C2440A0F.DOC
* USER'S NAME  SEIKO EPSON CORP.
* INPUT DATE   92/02/14
*
* COMMENT      ED MARKETING DEPARTMENT
*              421-8 HINO HINO-SHI TOKYO 191-8501 JAPAN
*              TEL 042-587-5816
*              FAX 042-587-5624
*
*
* OPTION NO.1
* < OSC1 OSCILLATOR >
*                              CRYSTAL  ----------------------  SELECTED
 OPT0101 01
 OPT0102 01
*
* OPTION NO.2
* < OSC3 OSCILLATOR >
*                              CR  --------------------------  SELECTED
 OPT0201 01
*
* OPTION NO.3
* < MULTIPLE KEY ENTRY RESET >
*                              NOT USE  ---------------------  SELECTED
 OPT0301 01
*
* OPTION NO.4
* < INPUT PORTS PULL UP RESISTOR >
*     K00                      WITH RESISTOR  ---------------  SELECTED
*     K01                      WITH RESISTOR  ---------------  SELECTED
*     K02                      WITH RESISTOR  ---------------  SELECTED
*     K03                      WITH RESISTOR  ---------------  SELECTED
*     K10                      WITH RESISTOR  ---------------  SELECTED
*     K11                      WITH RESISTOR  ---------------  SELECTED
*     K12                      WITH RESISTOR  ---------------  SELECTED
*     K13                      WITH RESISTOR  ---------------  SELECTED
 OPT0401 01
 OPT0402 01
 OPT0403 01
 OPT0404 01
 OPT0405 01
 OPT0406 01
 OPT0407 01
 OPT0408 01
*
* OPTION NO.5
* < OUTPUT PORTS OUTPUT SPECIFICATION >
*     R20-R23                  COMPLEMENTARY  ---------------  SELECTED
*     R30                      COMPLEMENTARY  ---------------  SELECTED
*     R31                      COMPLEMENTARY  ---------------  SELECTED
*     R32                      COMPLEMENTARY  ---------------  SELECTED
 OPT0501 01
 OPT0502 01
 OPT0503 01
 OPT0504 01
*
* OPTION NO.6
* < R33 OUTPUT PORT SPECIFICATION >
*     OUTPUT SPECIFICATION     COMPLEMENTARY  ---------------  SELECTED
*     OUTPUT TYPE              DC (PTCLK)  ------------------  SELECTED
*     OUTPUT CONTROL           3 STATE  ---------------------  SELECTED
 OPT0601 01
 OPT0602 01
 OPT0603 01
*
* OPTION NO.7
* < R40 OUTPUT PORT SPECIFICATION >
*     OUTPUT SPECIFICATION     COMPLEMENTARY  ---------------  SELECTED
```

(C2440A0F.DOC)

```
*     OUTPUT TYPE            DC  -------------------------  SELECTED
 OPT0701 01
 OPT0702 01
 OPT0703 01
*
* OPTION NO.8
* < R41 OUTPUT PORT SPECIFICATION >
*     OUTPUT SPECIFICATION   COMPLEMENTARY  ---------------  SELECTED
*     OUTPUT TYPE            DC  -------------------------  SELECTED
 OPT0801 01
 OPT0802 01
*
* OPTION NO.9
* < R42 OUTPUT PORT SPECIFICATION >
*     OUTPUT SPECIFICATION   COMPLEMENTARY  ---------------  SELECTED
*     OUTPUT TYPE            DC  -------------------------  SELECTED
 OPT0901 01
 OPT0902 01
 OPT0903 01
*
* OPTION NO.10
* < R43 OUTPUT PORT SPECIFICATION >
*     OUTPUT SPECIFICATION   COMPLEMENTARY  ---------------  SELECTED
*     OUTPUT TYPE            DC  -------------------------  SELECTED
 OPT1001 01
 OPT1002 01
*
* OPTION NO.11
* < I/O PORT OUTPUT SPECIFICATION >
*     P00-P03                COMPLEMENTARY  ---------------  SELECTED
*     P10-P13                COMPLEMENTARY  ---------------  SELECTED
*     P20                    COMPLEMENTARY  ---------------  SELECTED
*     P21                    COMPLEMENTARY  ---------------  SELECTED
*     P22                    COMPLEMENTARY  ---------------  SELECTED
*     P23                    COMPLEMENTARY  ---------------  SELECTED
 OPT1101 01
 OPT1102 01
 OPT1103 01
 OPT1104 01
 OPT1105 01
 OPT1106 01
*
* OPTION NO.12
* < P20-P23 I/O PORTS OUTPUT TYPE >
*     P20                    I/O PORT  --------------------  SELECTED
*     P21                    I/O PORT  --------------------  SELECTED
*     P22                    I/O PORT  --------------------  SELECTED
*     P23                    I/O PORT  --------------------  SELECTED
 OPT1201 01
 OPT1202 01
 OPT1203 01
 OPT1204 01
*
* OPTION NO.13
* < SIN PULL UP RESISTOR >
*                            WITH RESISTOR  ---------------  SELECTED
 OPT1301 01
*
* OPTION NO.14
* < SOUT OUTPUT SPECIFICATION >
*                            COMPLEMENTARY  ---------------  SELECTED
 OPT1401 01
*
* OPTION NO.15
* < /SCLK SPECIFICATION >
*     PULL UP RESISTOR       WITH RESISTOR  ---------------  SELECTED
*     OUTPUT SPECIFICATION   COMPLEMENTARY  ---------------  SELECTED
 OPT1501 01
 OPT1502 01
*
* OPTION NO.16
* < SIO DATA PERMUTATION >
*                            MSB FIRST  -------------------  SELECTED
 OPT1601 01
```

(C2440A0F.DOC)

```
*
* OPTION NO.17
* < LCD POWER VOLTAGE MODE >
*                            INTERNAL VOLTAGE  ------------  SELECTED
 OPT1701 01
*
*
*
* SEIKO EPSON'S AREA
*
*
*
* OPTION NO.18
 OPT1801 01
*
* OPTION NO.19
 OPT1901 01
*
* OPTION NO.20
 OPT2001 01
 OPT2002 01
*
* OPTION NO.21
 OPT2101 01
\\END
```

Note End mark "¥¥END" may be used instead of "\\END" depending on the PC used. (The code of \ and ¥ is 5CH.)

■ Example of E0C624A function option document file

```
* E0C624A FUNCTION OPTION DOCUMENT  V 3.12
*
* FILE NAME    C24A0A0F.DOC
* USER'S NAME  SEIKO EPSON CORP.
* INPUT DATE   92/02/14
*
* COMMENT      ED MARKETING DEPARTMENT
*              421-8 HINO HINO-SHI TOKYO 191-8501 JAPAN
*              TEL 042-587-5816
*              FAX 042-587-5624
*
*
* OPTION NO.1
* < OSC3 OSCILLATOR >
*                           CR  -------------------------  SELECTED
 OPT0101 01
*
* OPTION NO.2
* < MULTIPLE KEY ENTRY RESET >
*                           USE K00,K01  -----------------  SELECTED
 OPT0201 02
*
* OPTION NO.3
* < INPUT PORTS PULL UP RESISTOR >
*     K00                   GATE DIRECT  -----------------  SELECTED
*     K01                   GATE DIRECT  -----------------  SELECTED
*     K02                   GATE DIRECT  -----------------  SELECTED
*     K03                   GATE DIRECT  -----------------  SELECTED
*     K10                   WITH RESISTOR  ---------------  SELECTED
*     K11                   WITH RESISTOR  ---------------  SELECTED
*     K12                   WITH RESISTOR  ---------------  SELECTED
*     K13                   WITH RESISTOR  ---------------  SELECTED
 OPT0301 02
 OPT0302 02
 OPT0303 02
 OPT0304 02
 OPT0305 01
 OPT0306 01
 OPT0307 01
 OPT0308 01
*
* OPTION NO.4
* < OUTPUT PORTS OUTPUT SPECIFICATION >
*     R00-R03               COMPLEMENTARY  ---------------  SELECTED
*     R10-R13               COMPLEMENTARY  ---------------  SELECTED
*     R20-R22               COMPLEMENTARY  ---------------  SELECTED
*     R23                   NCH-OPENDRAIN  ---------------  SELECTED
*     R30                   NCH-OPENDRAIN  ---------------  SELECTED
*     R31                   COMPLEMENTARY  ---------------  SELECTED
*     R32                   COMPLEMENTARY  ---------------  SELECTED
 OPT0401 01
 OPT0402 01
 OPT0403 01
 OPT0404 02
 OPT0405 02
 OPT0406 01
 OPT0407 01
*
* OPTION NO.5
* < OUTPUT PORTS OUTPUT TYPE >
*     R00-R03               ADDRESS BUS (A0-A3)  ---------  SELECTED
*     R10-R13               ADDRESS BUS (A4-A7)  ---------  SELECTED
*     R20-R22               ADDRESS BUS (A8-A10)  --------  SELECTED
*     R23                   DC  -------------------------  SELECTED
*     R30                   DC  -------------------------  SELECTED
*     R31                   WRITE (/WR)  -----------------  SELECTED
*     R32                   READ (/RD)  ------------------  SELECTED
 OPT0501 02
 OPT0502 02
 OPT0503 02
 OPT0504 01
 OPT0505 01
 OPT0506 03
```

(C24A0A0F.DOC)

```
 OPT0507 02
*
* OPTION NO.6
* < R33 OUTPUT PORT SPECIFICATION >
*     OUTPUT SPECIFICATION   COMPLEMENTARY  ---------------  SELECTED
*     OUTPUT TYPE            /SRDY  ----------------------  SELECTED
*     OUTPUT CONTROL         2 STATE  --------------------  SELECTED
 OPT0601 01
 OPT0602 02
 OPT0603 02
*
* OPTION NO.7
* < R40 OUTPUT PORT SPECIFICATION >
*     OUTPUT SPECIFICATION   COMPLEMENTARY  ---------------  SELECTED
*     OUTPUT TYPE            DC  --------------------------  SELECTED
 OPT0701 01
 OPT0702 01
 OPT0703 01
*
* OPTION NO.8
* < R41 OUTPUT PORT SPECIFICATION >
*     OUTPUT SPECIFICATION   COMPLEMENTARY  ---------------  SELECTED
*     OUTPUT TYPE            DC  --------------------------  SELECTED
 OPT0801 01
 OPT0802 01
*
* OPTION NO.9
* < R42 OUTPUT PORT SPECIFICATION >
*     OUTPUT SPECIFICATION   COMPLEMENTARY  ---------------  SELECTED
*     OUTPUT TYPE            FOUT OSC3  ------------------  SELECTED
 OPT0901 01
 OPT0902 03
 OPT0903 09
*
* OPTION NO.10
* < R43 OUTPUT PORT SPECIFICATION >
*     OUTPUT SPECIFICATION   COMPLEMENTARY  ---------------  SELECTED
*     OUTPUT TYPE            BUZZER  ---------------------  SELECTED
 OPT1001 01
 OPT1002 02
*
* OPTION NO.11
* < I/O PORT OUTPUT SPECIFICATION >
*     P00-P03                COMPLEMENTARY  ---------------  SELECTED
*     P10-P13                COMPLEMENTARY  ---------------  SELECTED
*     P20                    COMPLEMENTARY  ---------------  SELECTED
*     P21                    COMPLEMENTARY  ---------------  SELECTED
*     P22                    COMPLEMENTARY  ---------------  SELECTED
*     P23                    COMPLEMENTARY  ---------------  SELECTED
*     P30                    COMPLEMENTARY  ---------------  SELECTED
*     P31                    COMPLEMENTARY  ---------------  SELECTED
*     P32                    COMPLEMENTARY  ---------------  SELECTED
*     P33                    COMPLEMENTARY  ---------------  SELECTED
 OPT1101 01
 OPT1102 01
 OPT1103 01
 OPT1104 01
 OPT1105 01
 OPT1106 01
 OPT1107 01
 OPT1108 01
 OPT1109 01
 OPT1110 01
*
* OPTION NO.12
* < P00-P03,P10-P13 I/O PORTS OUTPUT TYPE >
*                            DATA BUS (D0-D7)  ------------  SELECTED
 OPT1201 02
*
* OPTION NO.13
* < P20-P23 I/O PORTS OUTPUT TYPE >
*     P20                    CHIP SELECT (/CS0)  ----------  SELECTED
*     P21                    CHIP SELECT (/CS1)  ----------  SELECTED
*     P22                    DC  --------------------------  SELECTED
```

(C24A0A0F.DOC)

```
*     P23                   DC  -------------------------  SELECTED
 OPT1301 02
 OPT1302 02
 OPT1303 01
 OPT1304 01
*
* OPTION NO.14
* < P30-P33 I/O PORTS OUTPUT TYPE >
*     P30                   I/O PORT  --------------------  SELECTED
*     P31                   I/O PORT  --------------------  SELECTED
*     P32                   I/O PORT  --------------------  SELECTED
*     P33                   I/O PORT  --------------------  SELECTED
 OPT1401 01
 OPT1402 01
 OPT1403 01
 OPT1404 01
*
* OPTION NO.15
* < SIN PULL UP RESISTOR >
*                           WITH RESISTOR  ---------------  SELECTED
 OPT1501 01
*
* OPTION NO.16
* < SOUT OUTPUT SPECIFICATION >
*                           COMPLEMENTARY  ---------------  SELECTED
 OPT1601 01
*
* OPTION NO.17
* < /SCLK SPECIFICATION >
*     PULL UP RESISTOR      WITH RESISTOR  ---------------  SELECTED
*     OUTPUT SPECIFICATION  COMPLEMENTARY  ---------------  SELECTED
 OPT1701 01
 OPT1702 01
*
* OPTION NO.18
* < SIO DATA PERMUTATION >
*                           LSB FIRST  -------------------  SELECTED
 OPT1801 02
*
* OPTION NO.19
* < LCD POWER VOLTAGE MODE >
*                           INTERNAL VOLTAGE  ------------  SELECTED
 OPT1901 01
*
*
*
* SEIKO EPSON'S AREA
*
*
*
* OPTION NO.20
 OPT2001 01
*
* OPTION NO.21
 OPT2101 01
*
* OPTION NO.22
 OPT2201 01
 OPT2202 01
*
* OPTION NO.23
 OPT2301 01
\\END
```

Note End mark "¥¥END" may be used instead of "\\END" depending on the PC used. (The code of \ and ¥ is 5CH.)

■ Example of E0C624C/48 function option document file

In the case of the E0C624C:
E0C624C FUNCTION OPTION DOCUMENT V 3.13
The option items are the same as the E0C6248.

```
* E0C6248 FUNCTION OPTION DOCUMENT  V 3.12
*
* FILE NAME    C2480A0F.DOC
* USER'S NAME  SEIKO EPSON CORP.
* INPUT DATE   92/02/14
*
* COMMENT      ED MARKETING DEPARTMENT
*              421-8 HINO HINO-SHI TOKYO 191-8501 JAPAN
*              TEL 042-587-5816
*              FAX 042-587-5624
*
*
* OPTION NO.1
* < OSC1 OSCILLATOR >
*                            CRYSTAL  ---------------------  SELECTED
 OPT0101 01
 OPT0102 01
*
* OPTION NO.2
* < OSC3 OSCILLATOR >
*                            CR  --------------------------  SELECTED
 OPT0201 01
*
* OPTION NO.3
* < MULTIPLE KEY ENTRY RESET >
*                            USE K00,K01  -----------------  SELECTED
 OPT0301 02
*
* OPTION NO.4
* < INPUT PORTS PULL UP RESISTOR >
*     K00                    GATE DIRECT  -----------------  SELECTED
*     K01                    GATE DIRECT  -----------------  SELECTED
*     K02                    GATE DIRECT  -----------------  SELECTED
*     K03                    GATE DIRECT  -----------------  SELECTED
*     K10                    WITH RESISTOR  ---------------  SELECTED
*     K11                    WITH RESISTOR  ---------------  SELECTED
*     K12                    WITH RESISTOR  ---------------  SELECTED
*     K13                    WITH RESISTOR  ---------------  SELECTED
 OPT0401 02
 OPT0402 02
 OPT0403 02
 OPT0404 02
 OPT0405 01
 OPT0406 01
 OPT0407 01
 OPT0408 01
*
* OPTION NO.5
* < OUTPUT PORTS OUTPUT SPECIFICATION >
*     R00-R03                COMPLEMENTARY  ---------------  SELECTED
*     R10-R13                COMPLEMENTARY  ---------------  SELECTED
*     R20-R22                COMPLEMENTARY  ---------------  SELECTED
*     R23                    NCH-OPENDRAIN  ---------------  SELECTED
*     R30                    NCH-OPENDRAIN  ---------------  SELECTED
*     R31                    COMPLEMENTARY  ---------------  SELECTED
*     R32                    COMPLEMENTARY  ---------------  SELECTED
 OPT0501 01
 OPT0502 01
 OPT0503 01
 OPT0504 02
 OPT0505 02
 OPT0506 01
 OPT0507 01
*
* OPTION NO.6
* < OUTPUT PORTS OUTPUT TYPE >
*     R00-R03                ADDRESS BUS (A0-A3)  ---------  SELECTED
*     R10-R13                ADDRESS BUS (A4-A7)  ---------  SELECTED
*     R20-R22                ADDRESS BUS (A8-A10)  --------  SELECTED
*     R23                    DC  --------------------------  SELECTED
*     R30                    DC  --------------------------  SELECTED
*     R31                    WRITE (/WR)  -----------------  SELECTED
*     R32                    READ (/RD)  ------------------  SELECTED
```

(C2480A0F.DOC)

```
 OPT0601 02
 OPT0602 02
 OPT0603 02
 OPT0604 01
 OPT0605 01
 OPT0606 03
 OPT0607 02
*
* OPTION NO.7
* < R33 OUTPUT PORT SPECIFICATION >
*     OUTPUT SPECIFICATION   COMPLEMENTARY  ---------------  SELECTED
*     OUTPUT TYPE            /SRDY  -----------------------  SELECTED
*     OUTPUT CONTROL         2 STATE  ---------------------  SELECTED
 OPT0701 01
 OPT0702 02
 OPT0703 02
*
* OPTION NO.8
* < R40 OUTPUT PORT SPECIFICATION >
*     OUTPUT SPECIFICATION   COMPLEMENTARY  ---------------  SELECTED
*     OUTPUT TYPE            DC  --------------------------  SELECTED
 OPT0801 01
 OPT0802 01
 OPT0803 01
*
* OPTION NO.9
* < R41 OUTPUT PORT SPECIFICATION >
*     OUTPUT SPECIFICATION   COMPLEMENTARY  ---------------  SELECTED
*     OUTPUT TYPE            DC  --------------------------  SELECTED
 OPT0901 01
 OPT0902 01
*
* OPTION NO.10
* < R42 OUTPUT PORT SPECIFICATION >
*     OUTPUT SPECIFICATION   COMPLEMENTARY  ---------------  SELECTED
*     OUTPUT TYPE            FOUT OSC3  -------------------  SELECTED
 OPT1001 01
 OPT1002 03
 OPT1003 09
*
* OPTION NO.11
* < R43 OUTPUT PORT SPECIFICATION >
*     OUTPUT SPECIFICATION   COMPLEMENTARY  ---------------  SELECTED
*     OUTPUT TYPE            BUZZER  ----------------------  SELECTED
 OPT1101 01
 OPT1102 02
*
* OPTION NO.12
* < I/O PORT OUTPUT SPECIFICATION >
*     P00-P03                COMPLEMENTARY  ---------------  SELECTED
*     P10-P13                COMPLEMENTARY  ---------------  SELECTED
*     P20                    COMPLEMENTARY  ---------------  SELECTED
*     P21                    COMPLEMENTARY  ---------------  SELECTED
*     P22                    COMPLEMENTARY  ---------------  SELECTED
*     P23                    COMPLEMENTARY  ---------------  SELECTED
*     P30                    COMPLEMENTARY  ---------------  SELECTED
*     P31                    COMPLEMENTARY  ---------------  SELECTED
*     P32                    COMPLEMENTARY  ---------------  SELECTED
*     P33                    COMPLEMENTARY  ---------------  SELECTED
 OPT1201 01
 OPT1202 01
 OPT1203 01
 OPT1204 01
 OPT1205 01
 OPT1206 01
 OPT1207 01
 OPT1208 01
 OPT1209 01
 OPT1210 01
*
* OPTION NO.13
* < P00-P03,P10-P13 I/O PORTS OUTPUT TYPE >
*                        DATA BUS (D0-D7)  ------------  SELECTED
 OPT1301 02
```

(C2480A0F.DOC)

```
*
* OPTION NO.14
* < P20-P23 I/O PORTS OUTPUT TYPE >
*     P20                   CHIP SELECT (/CS0)  ----------  SELECTED
*     P21                   CHIP SELECT (/CS1)  ----------  SELECTED
*     P22                   DC  --------------------------  SELECTED
*     P23                   DC  --------------------------  SELECTED
 OPT1401 02
 OPT1402 02
 OPT1403 01
 OPT1404 01
*
* OPTION NO.15
* < P30-P33 I/O PORTS OUTPUT TYPE >
*     P30                   I/O PORT  --------------------  SELECTED
*     P31                   I/O PORT  --------------------  SELECTED
*     P32                   I/O PORT  --------------------  SELECTED
*     P33                   I/O PORT  --------------------  SELECTED
 OPT1501 01
 OPT1502 01
 OPT1503 01
 OPT1504 01
*
* OPTION NO.16
* < SIN PULL UP RESISTOR >
*                           WITH RESISTOR  ---------------  SELECTED
 OPT1601 01
*
* OPTION NO.17
* < SOUT OUTPUT SPECIFICATION >
*                           COMPLEMENTARY  ---------------  SELECTED
 OPT1701 01
*
* OPTION NO.18
* < /SCLK SPECIFICATION >
*     PULL UP RESISTOR      WITH RESISTOR  ---------------  SELECTED
*     OUTPUT SPECIFICATION  COMPLEMENTARY  ---------------  SELECTED
 OPT1801 01
 OPT1802 01
*
* OPTION NO.19
* < SIO DATA PERMUTATION >
*                           MSB FIRST  -------------------  SELECTED
 OPT1901 01
*
* OPTION NO.20
* < LCD POWER VOLTAGE MODE >
*                           INTERNAL VOLTAGE  ------------  SELECTED
 OPT2001 01
*
*
*
* SEIKO EPSON'S AREA
*
*
*
* OPTION NO.21
 OPT2101 01
*
* OPTION NO.22
 OPT2201 01
*
* OPTION NO.23
 OPT2301 01
 OPT2302 01
*
* OPTION NO.24
 OPT2401 01
\\END
```

Note End mark "¥¥END" may be used instead of "\\END" depending on the PC used. (The code of \ and ¥ is 5CH.)

5 ICE CONTROL SOFTWARE ICS6244/4A/4C/48

5.1 ICS6244/4A/4C/48 Outline

The In-circuit Emulator ICE62R (ICE6200) connects the target board produced by the user via the EVA6248 and performs real time target system evaluation and debugging by passing through the RS-232C from the host computer and controlling it. The operation on the host computer side and ICE62R (ICE6200) control is done through the ICE Control Software ICS6244/4A/4C/48.
The ICS6244/4A/4C/48 has a set of numerous and highly functional emulation commands which provide sophisticated break function, on-the-fly data display, history display, etc., and so perform a higher level of debugging.

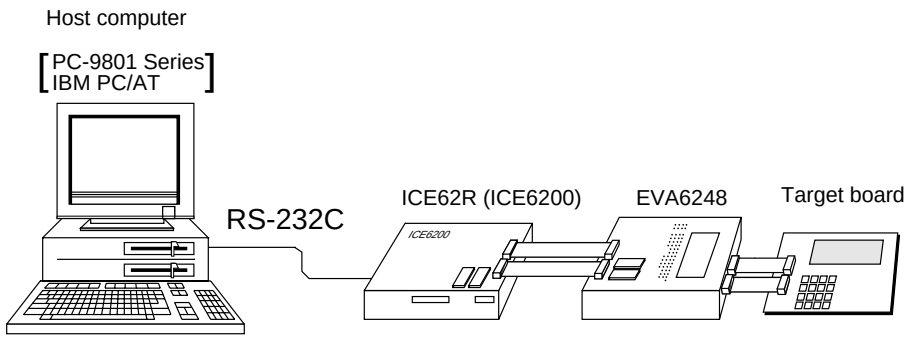

Fig. 5.1.1 Debugging system using ICE62R (ICE6200)

☞ *The functions of the ICE62R (ICE6200) and commands are same as for the E0C62 Family. Refer to the "E0C62 Family Development Tool Reference Manual" for details.*

5.2 ICS6244/4A/4C/48 Restrictions

Take the following precautions when using the ICS6244/4A/4C/48.

■ E0C6244

- **ROM Area**
  The ROM area is limited to a maximum address of 0FFFH. Assigning data above the 0FFFH address causes an error.

- **RAM Area**
  The RAM area is limited to a maximum address of F7EH. However, as the following addresses are in the unused area, designation of this area with the ICE commands produces an error.

  Unused area: 180H–DFFH, E50H–E7FH, ED0H–EFFH, F06H–F0FH, F16H–F1FH, F28H–F2FH, F32H–F3FH, F43H–F51H, F55H–F5FH, F63H–F6FH

  (Refer to the "E0C6244/4A/4C/48 Technical Manual" for details.)

- **Undefined Code**
  The SLP instruction is not specified for the E0C6244 and so cannot be used.

- **OPTLD Command**
  In the ICS6244, OPTLD command cannot be used.

■ E0C624A

- **ROM Area**
  The ROM area is limited to a maximum address of 17FFH. Assigning data above the 17FFH address causes an error.

- **RAM Area**
  The RAM area is limited to a maximum address of FFFH. However, as the following addresses are in the unused area, designation of this area with the ICE commands produces an error.

  Unused area: 280H–DFFH, E50H–E7FH, ED0H–EFFH, F06H–F0FH, F16H–F1FH, F28H–F2FH, F32H–F3FH, F43H–F4FH, F55H–F5FH, F64H–F6FH, F7FH–FBFH

  (Refer to the "E0C6244/4A/4C/48 Technical Manual" for details.)

- **Undefined Code**
  The SLP instruction is not specified for the E0C624A and so cannot be used.

- **OPTLD Command**
  In the ICS624A, OPTLD command cannot be used.

■ E0C624C

- **ROM Area**
  The ROM area is limited to a maximum address of 13FFH.

- **RAM Area**
  The RAM area is limited to a maximum address of FFFH. However, as the following addresses are in the unused area, designation of this area with the ICE commands produces an error.

  Unused area: 480H–DFFH, E66H–E7FH, EE6H–EFFH, F06H–F0FH, F16H–F1FH, F28H–F2FH, F32H–F3FH, F43H–F4FH, F55H–F5FH, F64H–F6FH, F7FH–FBFH

  (Refer to the "E0C6244/4A/4C/48 Technical Manual" for details.)

- **Undefined Code**
  The SLP instruction is not specified for the E0C624C and so cannot be used.

- **OPTLD Command**
  In the ICS624C, OPTLD command cannot be used.

■ E0C6248

- **ROM Area**
  The ROM area is limited to a maximum address of 1FFFH.

- **RAM Area**
  The RAM area is limited to a maximum address of FFFH. However, as the following addresses are in the unused area, designation of this area with the ICE commands produces an error.

  Unused area: 300H–DFFH, E66H–E7FH, EE6H–EFFH, F06H–F0FH, F16H–F1FH, F28H–F2FH, F32H–F3FH, F43H–F4FH, F55H–F5FH, F64H–F6FH, F7FH–FBFH

  (Refer to the "E0C6244/4A/4C/48 Technical Manual" for details.)

- **Undefined Code**
  The SLP instruction is not specified for the E0C6248 and so cannot be used.

- **OPTLD Command**
  In the ICS6248, OPTLD command cannot be used.

5.3 ICS6244/4A/4C/48 Quick Reference

■ Starting command and input/output files

Execution file:

ICS6244/4A/4C/48.BAT	(ICS6244/4A/4C/48J.EXE)	. . . for MS-DOS
ICS6244/4A/4C/48B.BAT	(ICS6244/4A/4C/48W.EXE)	. . . for PC-DOS

Starting command:

ICS624✻ (ICS624✻J)↵ . . . for MS-DOS

ICS624✻B (ICS624✻W)↵ . . . for PC-DOS

Input file:

C24✻XXXL.HEX (Object file, low-order)
C24✻XXXH.HEX (Object file, high-order)
C24✻XXXD.HEX (Data RAM file)
C24✻XXXC.HEX (Control file)

Output file:

C24✻XXXL.HEX (Object file, low-order)
C24✻XXXH.HEX (Object file, high-order)
C24✻XXXD.HEX (Data RAM file)
C24✻XXXC.HEX (Control file)

↵ *indicates the Return key.*
4✻ indicates the model name (44, 4A, 4C or 48).

■ Display example (In case of E0C6244)

```
          *** E0C6244 ICE CONTROL SOFTWARE. --- Ver 3.01 ***

 EEEEEEEEEE   PPPPPPPP        SSSSSSS       00000000     NNN      NNN
 EEEEEEEEEE   PPPPPPPPPP     SSS    SSSS    000    000    NNNN     NNN
 EEE          PPP     PPP   SSS     SSS   000      000   NNNNN    NNN
 EEE          PPP     PPP    SSS          000      000   NNNNNN   NNN
 EEEEEEEEEE   PPPPPPPPP      SSSSSS       000      000   NNN NNN NNN
 EEEEEEEEEE   PPPPPPPP           SSSS     000      000   NNN  NNNNNN
 EEE          PPP                SSS     000      000   NNN   NNNNN
 EEE          PPP           SSS     SSS   000      000   NNN    NNNN
 EEEEEEEEEE   PPP           SSSS   SSS     000    000    NNN     NNN
 EEEEEEEEEE   PPP             SSSSSSS       00000000     NNN      NN

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 * ICE POWER ON RESET *
 * DIAGNOSTIC TEST OK *
 #
```

Start-up message

When ICS6244/4A/4C/48 is started, the start-up message is displayed, and a self-test is automatically performed. ICS6244/4A/4C/48 commands are awaited when the program is properly loaded and the # mark is displayed.
Debugging can be done by entering command after the # mark.
The ICS6244/4A/4C/48 program is terminated by entering the Q (Quit) command.

Note *Confirm that the cables connected properly, then operate the ICS6244/4A/4C/48.*

■ Error messages

Error message	Meaning	Recover procedure
* COMMUNICATION ERROR OR ICE NOT READY *	ICE62R (ICE6200) is disconnected or power is OFF.	Switch OFF the host power supply, connect cable, and reapply power. Or switch ON power to ICE62R (ICE6200).
* TARGET DOWN (1) *	Evaluation board is disconnected. (Check at power ON)	Switch OFF power to ICE, and connect the evaluation board. Then, apply power to ICE62R (ICE6200).
* TARGET DOWN (2) *	Evaluation board is disconnected. (Check at command execution)	Switch OFF power to ICE, and connect the evaluation board. Then, apply power to ICE62R (ICE6200).
* UNDEFINED PROGRAM CODE EXIST *	Undefined code is detected in the program loaded from ROM or FD.	Convert ROM and FD data with the cross assembler, then restart the ICE62R (ICE6200).
* COMMAND ERROR *	A miss occurs by command input.	Reenter the proper command.
(No response after power on)	The ICE-to-HOST cable is disconnected on the host side.	Switch OFF the host power supply, connect cable, and reapply power.

■ Command list

Item No.	Function	Command Format	Outline of Operation
1	Assemble	#A,a ↵	Assemble command mnemonic code and store at address "a"
2	Disassemble	#L,a1,a2 ↵	Contents of addresses a1 to a2 are disassembled and displayed
3	Dump	#DP,a1,a2 ↵	Contents of program area a1 to a2 are displayed
		#DD,a1,a2 ↵	Content of data area a1 to a2 are displayed
4	Fill	#FP,a1,a2,d ↵	Data d is set in addresses a1 to a2 (program area)
		#FD,a1,a2,d ↵	Data d is set in addresses a1 to a2 (data area)
5	Set Run Mode	#G,a ↵	Program is executed from the "a" address
		#TIM ↵	Execution time and step counter selection
		#OTF ↵	On-the-fly display selection
6	Trace	#T,a,n ↵	Executes program while displaying results of step instruction from "a" address
		#U,a,n ↵	Displays only the final step of #T,a,n
7	Break	#BA,a ↵ #BAR,a ↵	Sets Break at program address "a" Breakpoint is canceled
		#BD ↵ #BDR ↵	Break condition is set for data RAM Breakpoint is canceled
		#BR ↵ #BRR ↵	Break condition is set for EVA6248 CPU internal registers Breakpoint is canceled
		#BM ↵ #BMR ↵	Combined break conditions set for program data RAM address and registers Cancel combined break conditions for program data ROM address and registers
		#BRES ↵	All break conditions canceled
		#BC ↵	Break condition displayed
		#BE ↵	Enter break enable mode
		#BSYN ↵	Enter break disable mode
		#BT ↵	Set break stop/trace modes
		#BRKSEL,REM ↵	Set BA condition clear/remain modes
8	Move	#MP,a1,a2,a3 ↵	Contents of program area addresses a1 to a2 are moved to addresses a3 and after
		#MD,a1,a2,a3 ↵	Contents of data area addresses a1 to a2 are moved to addresses a3 and after
9	Data Set	#SP,a ↵	Data from program area address "a" are written to memory
		#SD,a ↵	Data from data area address "a" are written to memory
10	Change CPU Internal Registers	#DR ↵	Display EVA6248 CPU internal registers
		#SR ↵	Set EVA6248 CPU internal registers
		#I ↵	Reset EVA6248 CPU
		#DXY ↵	Display X, Y, MX and MY
		#SXY ↵	Set data for X and Y display and MX, MY

Item No.	Function	Command Format	Outline of Operation
11	History	#H,p1,p2 ↵	Display history data for pointer 1 and pointer 2
		#HB ↵	Display upstream history data
		#HG ↵	Display 21 line history data
		#HP ↵	Display history pointer
		#HPS,a ↵	Set history pointer
		#HC,S/C/E ↵	Sets up the history information acquisition before (S), before/after (C) and after (E)
		#HA,a1,a2 ↵	Sets up the history information acquisition from program area a1 to a2
		#HAR,a1,a2 ↵	Sets up the prohibition of the history information acquisition from program area a1 to a2
		#HAD ↵	Indicates history acquisition program area
		#HS,a ↵	Retrieves and indicates the history information which executed a program address "a"
		#HSW,a ↵ #HSR,a ↵	Retrieves and indicates the history information which wrote or read the data area address "a"
12	File	#RF,file ↵	Move program file to memory
		#RFD,file ↵	Move data file to memory
		#VF,file ↵	Compare program file and contents of memory
		#VFD,file ↵	Compare data file and contents of memory
		#WF,file ↵	Save contents of memory to program file
		#WFD,file ↵	Save contents of memory to data file
		#CL,file ↵	Load ICE62R (ICE6200) set condition from file
		#CS,file ↵	Save ICE62R (ICE6200) set condition to file
13	Coverage	#CVD ↵	Indicates coverage information
		#CVR ↵	Clears coverage information
14	ROM Access	#RP ↵	Move contents of ROM to program memory
		#VP ↵	Compare contents of ROM with contents of program memory
		#ROM ↵	Set ROM type
15	Terminate ICE	#Q ↵	Terminate ICE and return to operating system control
16	Command Display	#HELP ↵	Display ICE62R (ICE6200) instruction
17	Self Diagnosis	#CHK ↵	Report results of ICE62R (ICE6200) self diagnostic test

↵ means press the RETURN key.

6 MASK DATA CHECKER MDC6244/4A/4C/48

6.1 MDC6244/4A/4C/48 Outline

The Mask Data Checker MDC6244/4A/4C/48 is a software tool which checks the program data (C24✻XXXH.HEX and C24✻XXXL.HEX) and option data (C24✻XXXF.DOC) created by the user and creates the data file (C624✻XXX.PAn) for generating mask patterns. The user must send the file generated through this software tool to Seiko Epson.

Moreover, MDC6244/4A/4C/48 has the capability to restore the generated data file (C624✻XXX.PA0) to the original file format.

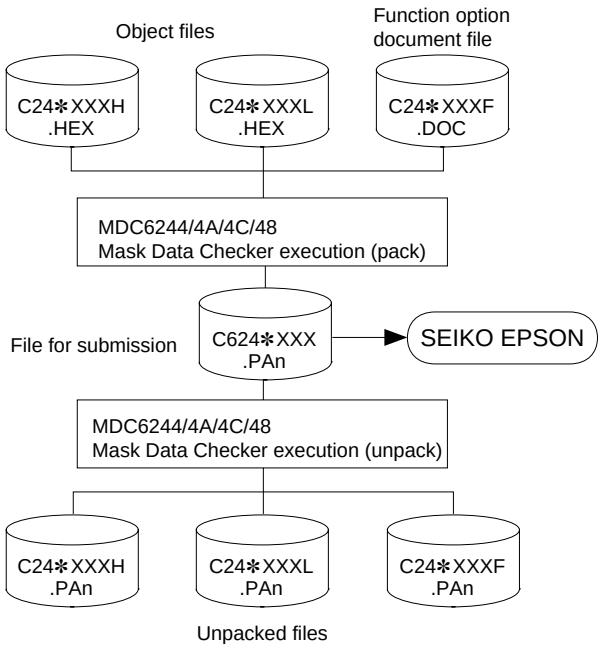

Fig. 6.1.1 MDC6244/4A/4C/48 execution flow

☞ *The operating method is same as for the E0C62 Family. Refer to the "E0C62 Family Development Tool Reference Manual" for details.*

6.2 MDC6244/4A/4C/48 Quick Reference

■ Starting command and input/output files

Execution file: MDC6244/4A/4C/48.EXE

Starting command: **MDC624✻↵**

↵ *indicates the Return key.*
4✻ indicates the model name (44, 4A, 4C or 48).

Input file:

C24✻XXXL.HEX	(Object file, low-order)	When packing
C24✻XXXH.HEX	(Object file, high-order)	
C24✻XXXF.DOC	(Function option document file)	
C624✻XXX.PAn	(Packed file)	When unpacking

Output file:

C624✻XXX.PAn	(Packed file)	When packing
C24✻XXXL.PAn	(Object file, low-order)	When unpacking
C24✻XXXH.PAn	(Object file, high-order)	
C24✻XXXF.PAn	(Function option document file)	

■ Display examples (In case of E0C6244)

```
          *** E0C6244 PACK / UNPACK PROGRAM Ver 2.000 ***

EEEEEEEEEE   PPPPPPPP        SSSSSSS       OOOOOOOO     NNN     NNN
EEEEEEEEEE   PPPPPPPPPP     SSS   SSSS    OOO    OOO    NNNN    NNN
EEE          PPP     PPP   SSS     SSS   OOO      OOO   NNNNN   NNN
EEE          PPP     PPP    SSS          OOO      OOO   NNNNNN  NNN
EEEEEEEEEE   PPPPPPPPPP      SSSSSS      OOO      OOO   NNN NNN NNN
EEEEEEEEEE   PPPPPPPP           SSSS     OOO      OOO   NNN  NNNNNN
EEE          PPP                 SSS     OOO      OOO   NNN   NNNNN
EEE          PPP            SSS     SSS   OOO      OOO   NNN    NNNN
EEEEEEEEEE   PPP            SSSS   SSS     OOO    OOO    NNN     NNN
EEEEEEEEEE   PPP              SSSSSSS       OOOOOOOO     NNN      NN

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                    --- OPERATION MENU ---

                           1. PACK
                           2. UNPACK

                    PLEASE SELECT NO.?
```

Start-up message

When MDC6244/4A/4C/48 is started, the start-up message and operation menu are displayed.
Here, the user is prompted to select operation options.

```
                    --- OPERATION MENU ---

                           1. PACK
                           2. UNPACK

                    PLEASE SELECT NO.? 1↵                          ...(1)

       C244XXXH.HEX --------+
                            |
       C244XXXL.HEX --------+-------- C244XXX.PAn (PACK FILE)
                            |
       C244XXXF.DOC --------+

PLEASE INPUT PACK FILE NAME (C6244XXX.PAn) ?  C62440A0.PA0↵   ...(2)

       C2440A0H.HEX --------+
                            |
       C2440A0L.HEX --------+-------- C2440A0.PA0
                            |
       C2440A0F.DOC --------+
```

Packing of data

(1) Select "1. PACK" in the operation menu.
(2) Enter the file name.
After submitting the data to Seiko Epson and there is a need to re-submit the data, increase the numeric value of "n" by one when the input is made.
(Example: When re-submitting data after "C624✻XXX.PA0" has been submitted, the pack file name should be entered as "C624✻XXX.PA1".)

With this, the mask file (C624✻XXX.PAn) is generated, and the MDC6244/4A/4C/48 program will be terminated.
Submit this file to Seiko Epson.

Note *Don't use the data generated with the -N option of the Cross Assembler (ASM6244/4A/4C/48) as program data. If the program data generated with the -N option of the Cross Assembler is packed, following message is displayed.*

```
HEX DATA ERROR : DATA (NO FFh)
```

```
                    --- OPERATION MENU ---

                           1. PACK
                           2. UNPACK

                    PLEASE SELECT NO.? 2↵                          ...(1)

PLEASE INPUT PACKED FILE NAME (C6244XXX.PAn) ?  C62440A0.PA0↵...(2)

                            +-------- C2440A0H.PA0
                            |
       C62440A0.PA0 --------+-------- C2440A0L.PA0
                            |
                            +-------- C2440A0F.PA0
```

Unpacking of data

(1) Select "2. UNPACK" in the operation menu.
(2) Enter the packed file name.

With this, the mask data file (C624✻XXX.PAn) is restored to the original file format, and the MDC6244/4A/4C/48 program will be terminated.

Since the extension of the file name remains as "PAn", it must be renamed back to its original form ("HEX" and "DOC") in order to re-debug or modify the restored file.

■ Error messages

Program data error

Error Message	Explanation
1. HEX DATA ERROR : NOT COLON.	There is no colon.
2. HEX DATA ERROR : DATA LENGTH. (NOT 00-20h)	The data length of 1 line is not in the 00–20H range.
3. HEX DATA ERROR : ADDRESS.	The address is beyond the valid range of the program ROM.
4. HEX DATA ERROR : RECORD TYPE. (NOT 00)	The record type of 1 line is not 00.
5. HEX DATA ERROR : DATA. (NOT 00-FFh)	The data is not in the range between 00H and 0FFH.
6. HEX DATA ERROR : TOO MANY DATA IN ONE LINE.	There are too many data in 1 line.
7. HEX DATA ERROR : CHECK SUM.	The checksum is not correct.
8. HEX DATA ERROR : END MARK.	The end mark is not : 00000001FF.
9. HEX DATA ERROR : DUPLICATE.	There is duplicate definition of data in the same address.
10. HEX DATA ERROR : DATA (NO FFh)	There is an undefined field in the HEX data.

Function option data error

Error Message	Explanation
1. OPTION DATA ERROR : START MARK.	The start mark is not "\OPTION". (during unpacking) *
2. OPTION DATA ERROR : OPTION NUMBER.	The option number is not correct.
3. OPTION DATA ERROR : SELECT NUMBER.	The option selection number is not correct.
4. OPTION DATA ERROR : END MARK.	The end mark is not "\\END" (packing) or "\END" (unpacking).*

File error

Error Message	Explanation
1. <File_name> FILE IS NOT FOUND.	The file is not found or the file number set in CONFIG.SYS is less than 10.
2. PACK FILE NAME (File_name) ERROR.	The packed input format for the file name is wrong.
3. PACKED FILE NAME (File_name) ERROR.	The unpacked input format for the file name is wrong.
4. VERSION NUMBER ERROR : X.DOC	FOG6244/4A/4C/48 different from the version No. has been used.

System error

Error Message	Explanation
1. DIRECTORY FULL.	The directory is full.
2. DISK WRITE ERROR.	Writing on the disk is failed.

* \ *sometimes appears as ¥, depending on the personal computer being used.*

APPENDIX A. E0C6244/4A/4C/48 INSTRUCTION SET

Classification	Mnemonic	Operand	Operation Code												Flag				Clock	Operation
			B	A	9	8	7	6	5	4	3	2	1	0	I	D	Z	C		
Branch instructions	PSET	p	1	1	1	0	0	1	0	p4	p3	p2	p1	p0					5	NBP ← p4, NPP ← p3~p0
	JP	s	0	0	0	0	s7	s6	s5	s4	s3	s2	s1	s0					5	PCB ← NBP, PCP ← NPP, PCS ← s7~s0
		C, s	0	0	1	0	s7	s6	s5	s4	s3	s2	s1	s0					5	PCB ← NBP, PCP ← NPP, PCS ← s7~s0 if C=1
		NC, s	0	0	1	1	s7	s6	s5	s4	s3	s2	s1	s0					5	PCB ← NBP, PCP ← NPP, PCS ← s7~s0 if C=0
		Z, s	0	1	1	0	s7	s6	s5	s4	s3	s2	s1	s0					5	PCB ← NBP, PCP ← NPP, PCS ← s7~s0 if Z=1
		NZ, s	0	1	1	1	s7	s6	s5	s4	s3	s2	s1	s0					5	PCB ← NBP, PCP ← NPP, PCS ← s7~s0 if Z=0
	JPBA		1	1	1	1	1	1	1	0	1	0	0	0					5	PCB ← NBP, PCP ← NPP, PCSH ← B, PCSL ← A
	CALL	s	0	1	0	0	s7	s6	s5	s4	s3	s2	s1	s0					7	M(SP-1) ← PCP, M(SP-2) ← PCSH, M(SP-3) ← PCSL+1 SP ← SP-3, PCP ← NPP, PCS ← s7~s0
	CALZ	s	0	1	0	1	s7	s6	s5	s4	s3	s2	s1	s0					7	M(SP-1) ← PCP, M(SP-2) ← PCSH, M(SP-3) ← PCSL+1 SP ← SP-3, PCP ← 0, PCS ← s7~s0
	RET		1	1	1	1	1	1	0	1	1	1	1	1					7	PCSL ← M(SP), PCSH ← M(SP+1), PCP ← M(SP+2) SP ← SP+3
	RETS		1	1	1	1	1	1	0	1	1	1	1	0					12	PCSL ← M(SP), PCSH ← M(SP+1), PCP ← M(SP+2) SP ← SP+3, PC ← PC+1
	RETD	*l*	0	0	0	1	*l*7	*l*6	*l*5	*l*4	*l*3	*l*2	*l*1	*l*0					12	PCSL ← M(SP), PCSH ← M(SP+1), PCP ← M(SP+2) SP ← SP+3, M(X) ← *l*3~*l*0, M(X+1) ← *l*7~*l*4, X ← X+2
System control instructions	NOP5		1	1	1	1	1	1	1	1	1	0	1	1					5	No operation (5 clock cycles)
	NOP7		1	1	1	1	1	1	1	1	1	1	1	1					7	No operation (7 clock cycles)
	HALT		1	1	1	1	1	1	1	1	1	0	0	0					5	Halt (stop clock)
Index operation instructions	INC	X	1	1	1	0	1	1	1	0	0	0	0	0					5	X ← X+1
		Y	1	1	1	0	1	1	1	1	0	0	0	0					5	Y ← Y+1
	LD	X, x	1	0	1	1	x7	x6	x5	x4	x3	x2	x1	x0					5	XH ← x7~x4, XL ← x3~x0
		Y, y	1	0	0	0	y7	y6	y5	y4	y3	y2	y1	y0					5	YH ← y7~y4, YL ← y3~y0
		XP, r	1	1	1	0	1	0	0	0	0	0	r1	r0					5	XP ← r
		XH, r	1	1	1	0	1	0	0	0	0	1	r1	r0					5	XH ← r
		XL, r	1	1	1	0	1	0	0	0	1	0	r1	r0					5	XL ← r
		YP, r	1	1	1	0	1	0	0	1	0	0	r1	r0					5	YP ← r
		YH, r	1	1	1	0	1	0	0	1	0	1	r1	r0					5	YH ← r
		YL, r	1	1	1	0	1	0	0	1	1	0	r1	r0					5	YL ← r
		r, XP	1	1	1	0	1	0	1	0	0	0	r1	r0					5	r ← XP
		r, XH	1	1	1	0	1	0	1	0	0	1	r1	r0					5	r ← XH
		r, XL	1	1	1	0	1	0	1	0	1	0	r1	r0					5	r ← XL
		r, YP	1	1	1	0	1	0	1	1	0	0	r1	r0					5	r ← YP
		r, YH	1	1	1	0	1	0	1	1	0	1	r1	r0					5	r ← YH
		r, YL	1	1	1	0	1	0	1	1	1	0	r1	r0					5	r ← YL
	ADC	XH, i	1	0	1	0	0	0	0	0	i3	i2	i1	i0			↕	↕	7	XH ← XH+i3~i0+C
		XL, i	1	0	1	0	0	0	0	1	i3	i2	i1	i0			↕	↕	7	XL ← XL+i3~i0+C
		YH, i	1	0	1	0	0	0	1	0	i3	i2	i1	i0			↕	↕	7	YH ← YH+i3~i0+C
		YL, i	1	0	1	0	0	0	1	1	i3	i2	i1	i0			↕	↕	7	YL ← YL+i3~i0+C

Classification	Mnemonic	Operand	Operation Code												Flag				Clock	Operation
			B	A	9	8	7	6	5	4	3	2	1	0	I	D	Z	C		
Index operation instructions	CP	XH, i	1	0	1	0	0	1	0	0	i3	i2	i1	i0			↕	↕	7	XH-i3~i0
		XL, i	1	0	1	0	0	1	0	1	i3	i2	i1	i0			↕	↕	7	XL-i3~i0
		YH, i	1	0	1	0	0	1	1	0	i3	i2	i1	i0			↕	↕	7	YH-i3~i0
		YL, i	1	0	1	0	0	1	1	1	i3	i2	i1	i0			↕	↕	7	YL-i3~i0
Data transfer instructions	LD	r, i	1	1	1	0	0	0	r1	r0	i3	i2	i1	i0					5	r←i3~i0
		r, q	1	1	1	0	1	1	0	0	r1	r0	q1	q0					5	r←q
		A, Mn	1	1	1	1	1	0	1	0	n3	n2	n1	n0					5	A←M(n3~n0)
		B, Mn	1	1	1	1	1	0	1	1	n3	n2	n1	n0					5	B←M(n3~n0)
		Mn, A	1	1	1	1	1	0	0	0	n3	n2	n1	n0					5	M(n3~n0)←A
		Mn, B	1	1	1	1	1	0	0	1	n3	n2	n1	n0					5	M(n3~n0)←B
	LDPX	MX, i	1	1	1	0	0	1	1	0	i3	i2	i1	i0					5	M(X)←i3~i0, X←X+1
		r, q	1	1	1	0	1	1	1	0	r1	r0	q1	q0					5	r←q, X←X+1
	LDPY	MY, i	1	1	1	0	0	1	1	1	i3	i2	i1	i0					5	M(Y)←i3~i0, Y←Y+1
		r, q	1	1	1	0	1	1	1	1	r1	r0	q1	q0					5	r←q, Y←Y+1
	LBPX	MX, *l*	1	0	0	1	*l*7	*l*6	*l*5	*l*4	*l*3	*l*2	*l*1	*l*0					5	M(X)←*l*3~*l*0, M(X+1)←*l*7~*l*4, X←X+2
Flag operation instructions	SET	F, i	1	1	1	1	0	1	0	0	i3	i2	i1	i0	↑	↑	↑	↑	7	F←F∨i3~i0
	RST	F, i	1	1	1	1	0	1	0	1	i3	i2	i1	i0	↓	↓	↓	↓	7	F←F∧i3~i0
	SCF		1	1	1	1	0	1	0	0	0	0	0	1				↑	7	C←1
	RCF		1	1	1	1	0	1	0	1	1	1	1	0				↓	7	C←0
	SZF		1	1	1	1	0	1	0	0	0	0	1	0			↑		7	Z←1
	RZF		1	1	1	1	0	1	0	1	1	1	0	1			↓		7	Z←0
	SDF		1	1	1	1	0	1	0	0	0	1	0	0		↑			7	D←1 (Decimal Adjuster ON)
	RDF		1	1	1	1	0	1	0	1	1	0	1	1		↓			7	D←0 (Decimal Adjuster OFF)
	EI		1	1	1	1	0	1	0	0	1	0	0	0	↑				7	I ←1 (Enables Interrupt)
	DI		1	1	1	1	0	1	0	1	0	1	1	1	↓				7	I ←0 (Disables Interrupt)
Stack operation instructions	INC	SP	1	1	1	1	1	1	0	1	1	0	1	1					5	SP← SP+1
	DEC	SP	1	1	1	1	1	1	0	0	1	0	1	1					5	SP← SP-1
	PUSH	r	1	1	1	1	1	1	0	0	0	0	r1	r0					5	SP← SP-1, M(SP)←r
		XP	1	1	1	1	1	1	0	0	0	1	0	0					5	SP← SP-1, M(SP)←XP
		XH	1	1	1	1	1	1	0	0	0	1	0	1					5	SP← SP-1, M(SP)←XH
		XL	1	1	1	1	1	1	0	0	0	1	1	0					5	SP← SP-1, M(SP)←XL
		YP	1	1	1	1	1	1	0	0	0	1	1	1					5	SP← SP-1, M(SP)←YP
		YH	1	1	1	1	1	1	0	0	1	0	0	0					5	SP← SP-1, M(SP)←YH
		YL	1	1	1	1	1	1	0	0	1	0	0	1					5	SP← SP-1, M(SP)←YL
		F	1	1	1	1	1	1	0	0	1	0	1	0					5	SP← SP-1, M(SP)←F
	POP	r	1	1	1	1	1	1	0	1	0	0	r1	r0					5	r←M(SP), SP←SP+1
		XP	1	1	1	1	1	1	0	1	0	1	0	0					5	XP←M(SP), SP←SP+1
		XH	1	1	1	1	1	1	0	1	0	1	0	1					5	XH←M(SP), SP←SP+1
		XL	1	1	1	1	1	1	0	1	0	1	1	0					5	XL←M(SP), SP←SP+1
		YP	1	1	1	1	1	1	0	1	0	1	1	1					5	YP←M(SP), SP←SP+1

Classification	Mnemonic	Operand	Operation Code												Flag				Clock	Operation
			B	A	9	8	7	6	5	4	3	2	1	0	I	D	Z	C		
Stack operation instructions	POP	YH	1	1	1	1	1	1	0	1	1	0	0	0					5	YH← M(SP), SP ← SP+1
		YL	1	1	1	1	1	1	0	1	1	0	0	1					5	YL ← M(SP), SP ← SP+1
		F	1	1	1	1	1	1	0	1	1	0	1	0	↕	↕	↕	↕	5	F ← M(SP), SP ← SP+1
	LD	SPH, r	1	1	1	1	1	1	1	0	0	0	r1	r0					5	SPH ← r
		SPL, r	1	1	1	1	1	1	1	1	0	0	r1	r0					5	SPL ← r
		r, SPH	1	1	1	1	1	1	1	0	0	1	r1	r0					5	r ← SPH
		r, SPL	1	1	1	1	1	1	1	1	0	1	r1	r0					5	r ← SPL
Arithmetic instructions	ADD	r, i	1	1	0	0	0	0	r1	r0	i3	i2	i1	i0	★	↕	↕		7	r ← r+i3~i0
		r, q	1	0	1	0	1	0	0	0	r1	r0	q1	q0	★	↕	↕		7	r ← r+q
	ADC	r, i	1	1	0	0	0	1	r1	r0	i3	i2	i1	i0	★	↕	↕		7	r ← r+i3~i0+C
		r, q	1	0	1	0	1	0	0	1	r1	r0	q1	q0	★	↕	↕		7	r ← r+q+C
	SUB	r, q	1	0	1	0	1	0	1	0	r1	r0	q1	q0	★	↕	↕		7	r ← r-q
	SBC	r, i	1	1	0	1	0	1	r1	r0	i3	i2	i1	i0	★	↕	↕		7	r ← r-i3~i0-C
		r, q	1	0	1	0	1	0	1	1	r1	r0	q1	q0	★	↕	↕		7	r ← r-q-C
	AND	r, i	1	1	0	0	1	0	r1	r0	i3	i2	i1	i0		↕			7	r ← r∧i3~i0
		r, q	1	0	1	0	1	1	0	0	r1	r0	q1	q0		↕			7	r ← r∧q
	OR	r, i	1	1	0	0	1	1	r1	r0	i3	i2	i1	i0		↕			7	r ← r∨i3~i0
		r, q	1	0	1	0	1	1	0	1	r1	r0	q1	q0		↕			7	r ← r∨q
	XOR	r, i	1	1	0	1	0	0	r1	r0	i3	i2	i1	i0		↕			7	r ← r∀i3~i0
		r, q	1	0	1	0	1	1	1	0	r1	r0	q1	q0		↕			7	r ← r∀q
	CP	r, i	1	1	0	1	1	1	r1	r0	i3	i2	i1	i0		↕	↕		7	r-i3~i0
		r, q	1	1	1	1	0	0	0	0	r1	r0	q1	q0		↕	↕		7	r-q
	FAN	r, i	1	1	0	1	1	0	r1	r0	i3	i2	i1	i0		↕			7	r∧i3~i0
		r, q	1	1	1	1	0	0	0	1	r1	r0	q1	q0		↕			7	r∧q
	RLC	r	1	0	1	0	1	1	1	1	r1	r0	r1	r0		↕	↕		7	d3 ← d2, d2 ← d1, d1 ← d0, d0 ← C, C ← d3
	RRC	r	1	1	1	0	1	0	0	0	1	1	r1	r0		↕	↕		5	d3 ← C, d2 ← d3, d1 ← d2, d0 ← d1, C ← d0
	INC	Mn	1	1	1	1	0	1	1	0	n3	n2	n1	n0		↕	↕		7	M(n3~n0) ← M(n3~n0)+1
	DEC	Mn	1	1	1	1	0	1	1	1	n3	n2	n1	n0		↕	↕		7	M(n3~n0) ← M(n3~n0)-1
	ACPX	MX, r	1	1	1	1	0	0	1	0	1	0	r1	r0	★	↕	↕		7	M(X) ← M(X)+r+C, X ← X+1
	ACPY	MY, r	1	1	1	1	0	0	1	0	1	1	r1	r0	★	↕	↕		7	M(Y) ← M(Y)+r+C, Y ← Y+1
	SCPX	MX, r	1	1	1	1	0	0	1	1	1	0	r1	r0	★	↕	↕		7	M(X) ← M(X)-r-C, X ← X+1
	SCPY	MY, r	1	1	1	1	0	0	1	1	1	1	r1	r0	★	↕	↕		7	M(Y) ← M(Y)-r-C, Y ← Y+1
	NOT	r	1	1	0	1	0	0	r1	r0	1	1	1	1		↕			7	r ← $\bar{r}$

Abbreviations used in the explanations have the following meanings.

Symbols associated with registers and memory

A A register
B B register
X XHL register
(low order eight bits of index register IX)
Y YHL register
(low order eight bits of index register IY)
XH XH register
(high order four bits of XHL register)
XL XL register
(low order four bits of XHL register)
YH YH register
(high order four bits of YHL register)
YL YL register
(low order four bits of YHL register)
XP XP register
(high order four bits of index register IX)
YP YP register
(high order four bits of index register IY)
SP Stack pointer SP
SPH High-order four bits of stack pointer SP
SPL Low-order four bits of stack pointer SP
MX, M(X) Data memory whose address is specified with index register IX
MY, M(Y) Data memory whose address is specified with index register IY
Mn, M(n) Data memory address 000H–00FH (address specified with immediate data n of 00H–0FH)
M(SP) Data memory whose address is specified with stack pointer SP
r, q Two-bit register code
r, q is two-bit immediate data; according to the contents of these bits, they indicate registers A, B, and MX and MY (data memory whose addresses are specified with index registers IX and IY)

r		q		Register specified
r1	r0	q1	q0	
0	0	0	0	A
0	1	0	1	B
1	0	1	0	MX
1	1	1	1	MY

Symbols associated with program counter

NBP New bank pointer
NPP New page pointer
PCB Program counter bank
PCP Program counter page
PCS Program counter step
PCSH Four high order bits of PCS
PCSL Four low order bits of PCS

Symbols associated with flags

F Flag register (I, D, Z, C)
C Carry flag
Z Zero flag
D Decimal flag
I Interrupt flag
↓ Flag reset
↑ Flag set
↕ Flag set or reset

Associated with immediate data

p Five-bit immediate data or label 00H–1FH
s Eight-bit immediate data or label 00H–0FFH
l Eight-bit immediate data 00H–0FFH
i Four-bit immediate data 00H–0FH

Associated with arithmetic and other operations

+ Add
- Subtract
∧ Logical AND
∨ Logical OR
∀ Exclusive-OR
★ Add-subtract instruction for decimal operation when the D flag is set

APPENDIX B. E0C6244/4A/4C/48 RAM MAP

RAM (000H–07FH)

PROGRAM NAME : C244/4A/4C/48																	
P	H	L	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	0	NAME																
		MSB																
		LSB																
	1	NAME																
		MSB																
		LSB																
	2	NAME																
		MSB																
		LSB																
	3	NAME																
		MSB																
		LSB																
	4	NAME																
		MSB																
		LSB																
	5	NAME																
		MSB																
		LSB																
	6	NAME																
		MSB																
		LSB																
	7	NAME																
		MSB																
		LSB																

RAM (080H–0FFH)

PROGRAM NAME : C244/4A/4C/48																		
P	H	L	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	8	NAME																
		MSB																
		LSB																
	9	NAME																
		MSB																
		LSB																
	A	NAME																
		MSB																
		LSB																
	B	NAME																
		MSB																
		LSB																
	C	NAME																
		MSB																
		LSB																
	D	NAME																
		MSB																
		LSB																
	E	NAME																
		MSB																
		LSB																
	F	NAME																
		MSB																
		LSB																

RAM (100H–17FH)

PROGRAM NAME : C244/4A/4C/48																	
P	H	L	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
1	0	NAME																
		MSB																
		LSB																
	1	NAME																
		MSB																
		LSB																
	2	NAME																
		MSB																
		LSB																
	3	NAME																
		MSB																
		LSB																
	4	NAME																
		MSB																
		LSB																
	5	NAME																
		MSB																
		LSB																
	6	NAME																
		MSB																
		LSB																
	7	NAME																
		MSB																
		LSB																

RAM (180H–1FFH) <E0C624A/4C/48 only>

PROGRAM NAME : C24A/4C/48																		
P	H	L	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
1	8	NAME																
		MSB																
		LSB																
	9	NAME																
		MSB																
		LSB																
	A	NAME																
		MSB																
		LSB																
	B	NAME																
		MSB																
		LSB																
	C	NAME																
		MSB																
		LSB																
	D	NAME																
		MSB																
		LSB																
	E	NAME																
		MSB																
		LSB																
	F	NAME																
		MSB																
		LSB																

RAM (200H–27FH) <E0C624A/4C/48 only>

PROGRAM NAME : C24A/4C/48																	
P	H	L	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
2	0	NAME																
		MSB																
		LSB																
	1	NAME																
		MSB																
		LSB																
	2	NAME																
		MSB																
		LSB																
	3	NAME																
		MSB																
		LSB																
	4	NAME																
		MSB																
		LSB																
	5	NAME																
		MSB																
		LSB																
	6	NAME																
		MSB																
		LSB																
	7	NAME																
		MSB																
		LSB																

RAM (280H–2FFH) <E0C624C/48 only>

PROGRAM NAME : C24C/48																		
P	H	L	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
2	8	NAME																
		MSB																
		LSB																
	9	NAME																
		MSB																
		LSB																
	A	NAME																
		MSB																
		LSB																
	B	NAME																
		MSB																
		LSB																
	C	NAME																
		MSB																
		LSB																
	D	NAME																
		MSB																
		LSB																
	E	NAME																
		MSB																
		LSB																
	F	NAME																
		MSB																
		LSB																

RAM (300H–37FH) <E0C624C only>

PROGRAM NAME : C24C																	
P	H	L	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
3	0	NAME																
		MSB																
		LSB																
	1	NAME																
		MSB																
		LSB																
	2	NAME																
		MSB																
		LSB																
	3	NAME																
		MSB																
		LSB																
	4	NAME																
		MSB																
		LSB																
	5	NAME																
		MSB																
		LSB																
	6	NAME																
		MSB																
		LSB																
	7	NAME																
		MSB																
		LSB																

RAM (380H–3FFH) <E0C624C only>

PROGRAM NAME : C24C																		
P	H	L	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
3	8	NAME																
		MSB																
		LSB																
	9	NAME																
		MSB																
		LSB																
	A	NAME																
		MSB																
		LSB																
	B	NAME																
		MSB																
		LSB																
	C	NAME																
		MSB																
		LSB																
	D	NAME																
		MSB																
		LSB																
	E	NAME																
		MSB																
		LSB																
	F	NAME																
		MSB																
		LSB																

RAM (400H–47FH) <E0C624C only>

PROGRAM NAME : C24C																	
P	H	L	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
4	0	NAME																
		MSB																
		LSB																
	1	NAME																
		MSB																
		LSB																
	2	NAME																
		MSB																
		LSB																
	3	NAME																
		MSB																
		LSB																
	4	NAME																
		MSB																
		LSB																
	5	NAME																
		MSB																
		LSB																
	6	NAME																
		MSB																
		LSB																
	7	NAME																
		MSB																
		LSB																

Display memory (E00H–E4FH)

PROGRAM NAME : C244/4A/4C/48																		
P	H	L	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
E	0	NAME																
		MSB	[3,0]	[7,0]	[3,1]	[7,1]	[3,2]	[7,2]	[3,3]	[7,3]	[3,4]	[7,4]	[3,5]	[7,5]	[3,6]	[7,6]	[3,7]	[7,7]
			[2,0]	[6,0]	[2,1]	[6,1]	[2,2]	[6,2]	[2,3]	[6,3]	[2,4]	[6,4]	[2,5]	[6,5]	[2,6]	[6,6]	[2,7]	[6,7]
			[1,0]	[5,0]	[1,1]	[5,1]	[1,2]	[5,2]	[1,3]	[5,3]	[1,4]	[5,4]	[1,5]	[5,5]	[1,6]	[5,6]	[1,7]	[5,7]
		LSB	[0,0]	[4,0]	[0,1]	[4,1]	[0,2]	[4,2]	[0,3]	[4,3]	[0,4]	[4,4]	[0,5]	[4,5]	[0,6]	[4,6]	[0,7]	[4,7]
	1	NAME																
		MSB	[3,8]	[7,8]	[3,9]	[7,9]	[3,10]	[7,10]	[3,11]	[7,11]	[3,12]	[7,12]	[3,13]	[7,13]	[3,14]	[7,14]	[3,15]	[7,15]
			[2,8]	[6,8]	[2,9]	[6,9]	[2,10]	[6,10]	[2,11]	[6,11]	[2,12]	[6,12]	[2,13]	[6,13]	[2,14]	[6,14]	[2,15]	[6,15]
			[1,8]	[5,8]	[1,9]	[5,9]	[1,10]	[5,10]	[1,11]	[5,11]	[1,12]	[5,12]	[1,13]	[5,13]	[1,14]	[5,14]	[1,15]	[5,15]
		LSB	[0,8]	[4,8]	[0,9]	[4,9]	[0,10]	[4,10]	[0,11]	[4,11]	[0,12]	[4,12]	[0,13]	[4,13]	[0,14]	[4,14]	[0,15]	[4,15]
	2	NAME																
		MSB	[3,16]	[7,16]	[3,17]	[7,17]	[3,18]	[7,18]	[3,19]	[7,19]	[3,20]	[7,20]	[3,21]	[7,21]	[3,22]	[7,22]	[3,23]	[7,23]
			[2,16]	[6,16]	[2,17]	[6,17]	[2,18]	[6,18]	[2,19]	[6,19]	[2,20]	[6,20]	[2,21]	[6,21]	[2,22]	[6,22]	[2,23]	[6,23]
			[1,16]	[5,16]	[1,17]	[5,17]	[1,18]	[5,18]	[1,19]	[5,19]	[1,20]	[5,20]	[1,21]	[5,21]	[1,22]	[5,22]	[1,23]	[5,23]
		LSB	[0,16]	[4,16]	[0,17]	[4,17]	[0,18]	[4,18]	[0,19]	[4,19]	[0,20]	[4,20]	[0,21]	[4,21]	[0,22]	[4,22]	[0,23]	[4,23]
	3	NAME																
		MSB	[3,24]	[7,24]	[3,25]	[7,25]	[3,26]	[7,26]	[3,27]	[7,27]	[3,28]	[7,28]	[3,29]	[7,29]	[3,30]	[7,30]	[3,31]	[7,31]
			[2,24]	[6,24]	[2,25]	[6,25]	[2,26]	[6,26]	[2,27]	[6,27]	[2,28]	[6,28]	[2,29]	[6,29]	[2,30]	[6,30]	[2,31]	[6,31]
			[1,24]	[5,24]	[1,25]	[5,25]	[1,26]	[5,26]	[1,27]	[5,27]	[1,28]	[5,28]	[1,29]	[5,29]	[1,30]	[5,30]	[1,31]	[5,31]
		LSB	[0,24]	[4,24]	[0,25]	[4,25]	[0,26]	[4,26]	[0,27]	[4,27]	[0,28]	[4,28]	[0,29]	[4,29]	[0,30]	[4,30]	[0,31]	[4,31]
	4	NAME																
		MSB	[3,32]	[7,32]	[3,33]	[7,33]	[3,34]	[7,34]	[3,35]	[7,35]	[3,36]	[7,36]	[3,37]	[7,37]	[3,38]	[7,38]	[3,39]	[7,39]
			[2,32]	[6,32]	[2,33]	[6,33]	[2,34]	[6,34]	[2,35]	[6,35]	[2,36]	[6,36]	[2,37]	[6,37]	[2,38]	[6,38]	[2,39]	[6,39]
			[1,32]	[5,32]	[1,33]	[5,33]	[1,34]	[5,34]	[1,35]	[5,35]	[1,36]	[5,36]	[1,37]	[5,37]	[1,38]	[5,38]	[1,39]	[5,39]
		LSB	[0,32]	[4,32]	[0,33]	[4,33]	[0,34]	[4,34]	[0,35]	[4,35]	[0,36]	[4,36]	[0,37]	[4,37]	[0,38]	[4,38]	[0,39]	[4,39]

Display memory (E50H–E65H) <E0C624C/48 only>

PROGRAM NAME : C24C/48																		
P	H	L	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
E	5	NAME																
		MSB	[3,40]	[7,40]	[3,41]	[7,41]	[3,42]	[7,42]	[3,43]	[7,43]	[3,44]	[7,44]	[3,45]	[7,45]	[3,46]	[7,46]	[3,47]	[7,47]
			[2,40]	[6,40]	[2,41]	[6,41]	[2,42]	[6,42]	[2,43]	[6,43]	[2,44]	[6,44]	[2,45]	[6,45]	[2,46]	[6,46]	[2,47]	[6,47]
			[1,40]	[5,40]	[1,41]	[5,41]	[1,42]	[5,42]	[1,43]	[5,43]	[1,44]	[5,44]	[1,45]	[5,45]	[1,46]	[5,46]	[1,47]	[5,47]
		LSB	[0,40]	[4,40]	[0,41]	[4,41]	[0,42]	[4,42]	[0,43]	[4,43]	[0,44]	[4,44]	[0,45]	[4,45]	[0,46]	[4,46]	[0,47]	[4,47]
	6	NAME																
		MSB	[3,48]	[7,48]	[3,49]	[7,49]	[3,50]	[7,50]										
			[2,48]	[6,48]	[2,49]	[6,49]	[2,50]	[6,50]										
			[1,48]	[5,48]	[1,49]	[5,49]	[1,50]	[5,50]										
		LSB	[0,48]	[4,48]	[0,49]	[4,49]	[0,50]	[4,50]										

Display memory (E80H–ECFH)

PROGRAM NAME : C244/4A/4C/48																		
P	H	L	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
E	8	NAME																
		MSB	[11,0]	[15,0]	[11,1]	[15,1]	[11,2]	[15,2]	[11,3]	[15,3]	[11,4]	[15,4]	[11,5]	[15,5]	[11,6]	[15,6]	[11,7]	[15,7]
			[10,0]	[14,0]	[10,1]	[14,1]	[10,2]	[14,2]	[10,3]	[14,3]	[10,4]	[14,4]	[10,5]	[14,5]	[10,6]	[14,6]	[10,7]	[14,7]
			[9,0]	[13,0]	[9,1]	[13,1]	[9,2]	[13,2]	[9,3]	[13,3]	[9,4]	[13,4]	[9,5]	[13,5]	[9,6]	[13,6]	[9,7]	[13,7]
		LSB	[8,0]	[12,0]	[8,1]	[12,1]	[8,2]	[12,2]	[8,3]	[12,3]	[8,4]	[12,4]	[8,5]	[12,5]	[8,6]	[12,6]	[8,7]	[12,7]
	9	NAME																
		MSB	[11,8]	[15,8]	[11,9]	[15,9]	[11,10]	[15,10]	[11,11]	[15,11]	[11,12]	[15,12]	[11,13]	[15,13]	[11,14]	[15,14]	[11,15]	[15,15]
			[10,8]	[14,8]	[10,9]	[14,9]	[10,10]	[14,10]	[10,11]	[14,11]	[10,12]	[14,12]	[10,13]	[14,13]	[10,14]	[14,14]	[10,15]	[14,15]
			[9,8]	[13,8]	[9,9]	[13,9]	[9,10]	[13,10]	[9,11]	[13,11]	[9,12]	[13,12]	[9,13]	[13,13]	[9,14]	[13,14]	[9,15]	[13,15]
		LSB	[8,8]	[12,8]	[8,9]	[12,9]	[8,10]	[12,10]	[8,11]	[12,11]	[8,12]	[12,12]	[8,13]	[12,13]	[8,14]	[12,14]	[8,15]	[12,15]
	A	NAME																
		MSB	[11,16]	[15,16]	[11,17]	[15,17]	[11,18]	[15,18]	[11,19]	[15,19]	[11,20]	[15,20]	[11,21]	[15,21]	[11,22]	[15,22]	[11,23]	[15,23]
			[10,16]	[14,16]	[10,17]	[14,17]	[10,18]	[14,18]	[10,19]	[14,19]	[10,20]	[14,20]	[10,21]	[14,21]	[10,22]	[14,22]	[10,23]	[14,23]
			[9,16]	[13,16]	[9,17]	[13,17]	[9,18]	[13,18]	[9,19]	[13,19]	[9,20]	[13,20]	[9,21]	[13,21]	[9,22]	[13,22]	[9,23]	[13,23]
		LSB	[8,16]	[12,16]	[8,17]	[12,17]	[8,18]	[12,18]	[8,19]	[12,19]	[8,20]	[12,20]	[8,21]	[12,21]	[8,22]	[12,22]	[8,23]	[12,23]
	B	NAME																
		MSB	[11,24]	[15,24]	[11,25]	[15,25]	[11,26]	[15,26]	[11,27]	[15,27]	[11,28]	[15,28]	[11,29]	[15,29]	[11,30]	[15,30]	[11,31]	[15,31]
			[10,24]	[14,24]	[10,25]	[14,25]	[10,26]	[14,26]	[10,27]	[14,27]	[10,28]	[14,28]	[10,29]	[14,29]	[10,30]	[14,30]	[10,31]	[14,31]
			[9,24]	[13,24]	[9,25]	[13,25]	[9,26]	[13,26]	[9,27]	[13,27]	[9,28]	[13,28]	[9,29]	[13,29]	[9,30]	[13,30]	[9,31]	[13,31]
		LSB	[8,24]	[12,24]	[8,25]	[12,25]	[8,26]	[12,26]	[8,27]	[12,27]	[8,28]	[12,28]	[8,29]	[12,29]	[8,30]	[12,30]	[8,31]	[12,31]
	C	NAME																
		MSB	[11,32]	[15,32]	[11,33]	[15,33]	[11,34]	[15,34]	[11,35]	[15,35]	[11,36]	[15,36]	[11,37]	[15,37]	[11,38]	[15,38]	[11,39]	[15,39]
			[10,32]	[14,32]	[10,33]	[14,33]	[10,34]	[14,34]	[10,35]	[14,35]	[10,36]	[14,36]	[10,37]	[14,37]	[10,38]	[14,38]	[10,39]	[14,39]
			[9,32]	[13,32]	[9,33]	[13,33]	[9,34]	[13,34]	[9,35]	[13,35]	[9,36]	[13,36]	[9,37]	[13,37]	[9,38]	[13,38]	[9,39]	[13,39]
		LSB	[8,32]	[12,32]	[8,33]	[12,33]	[8,34]	[12,34]	[8,35]	[12,35]	[8,36]	[12,36]	[8,37]	[12,37]	[8,38]	[12,38]	[8,39]	[12,39]

Display memory (ED0H–EE5H) <E0C624C/48 only>

PROGRAM NAME : C24C/48																		
P	H	L	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
E	D	NAME																
		MSB	[11,40]	[15,40]	[11,41]	[15,41]	[11,42]	[15,42]	[11,43]	[15,43]	[11,44]	[15,44]	[11,45]	[15,45]	[11,46]	[15,46]	[11,47]	[15,47]
			[10,40]	[14,40]	[10,41]	[14,41]	[10,42]	[14,42]	[10,43]	[14,43]	[10,44]	[14,44]	[10,45]	[14,45]	[10,46]	[14,46]	[10,47]	[14,47]
			[9,40]	[13,40]	[9,41]	[13,41]	[9,42]	[13,42]	[9,43]	[13,43]	[9,44]	[13,44]	[9,45]	[13,45]	[9,46]	[13,46]	[9,47]	[13,47]
		LSB	[8,40]	[12,40]	[8,41]	[12,41]	[8,42]	[12,42]	[8,43]	[12,43]	[8,44]	[12,44]	[8,45]	[12,45]	[8,46]	[12,46]	[8,47]	[12,47]
	E	NAME																
		MSB	[11,48]	[15,48]	[11,49]	[15,49]	[11,50]	[15,50]										
			[10,48]	[14,48]	[10,49]	[14,49]	[10,50]	[14,50]										
			[9,48]	[13,48]	[9,49]	[13,49]	[9,50]	[13,50]										
		LSB	[8,48]	[12,48]	[8,49]	[12,49]	[8,50]	[12,50]										

I/O memory (F00H–F7EH) <E0C6244>

PROGRAM NAME : C244																		
P	H	L	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
F	0	NAME	ZTI	ZISW	ZIPT	ZISIO	ZIK0	ZIK1										
		MSB	IT1	0	0	0	0	0										
			IT2	0	0	0	0	0										
			IT8	ISW1	0	0	0	0										
		LSB	IT32	ISW0	IPT	ISIO	IK0	IK1										
	1	NAME	ZEIT	ZEISW	ZEIPT	ZEISIO	ZEIK0	ZEIK1										
		MSB	EIT1	0	0	0	EIK03	EIK13										
			EIT2	0	0	0	EIK02	EIK12										
			EIT8	EISW1	0	0	EIK01	EIK11										
		LSB	EIT32	EISW0	EIPT	EISIO	EIK00	EIK10										
	2	NAME	ZTML	ZTMH	ZSWL	ZSWH	ZPTL	ZPTH	ZRDL	ZRDH								
		MSB	TM3	TM7	SWL3	SWH3	PT3	PT7	RD3	RD7								
			TM2	TM6	SWL2	SWH2	PT2	PT6	RD2	RD6								
			TM1	TM5	SWL1	SWH1	PT1	PT5	RD1	RD5								
		LSB	TM0	TM4	SWL0	SWH0	PT0	PT4	RD0	RD4								
	3	NAME	ZSDL	ZSDH														
		MSB	SD3	SD7														
			SD2	SD6														
			SD1	SD5														
		LSB	SD0	SD4														
	4	NAME	ZK0	ZDFK0	ZK1													
		MSB	K03	DFK03	K13													
			K02	DFK02	K12													
			K01	DFK01	K11													
		LSB	K00	DFK00	K10													
	5	NAME			ZR2	ZR3	ZR4											
		MSB			R23	R33	R43											
					R22	R32	R42											
					R21	R31	R41											
		LSB			R20	R30	R40											
	6	NAME	ZP0	ZP1	ZP2													
		MSB	P03	P13	P23													
			P02	P12	P22													
			P01	P11	P21													
		LSB	P00	P10	P20													
	7	NAME	ZOSC	ZLCD	ZLC	ZSVD	ZBZ	ZENV	ZTRST	ZSWR	ZPTR	ZPTC	ZSC	ZHZR	ZEMA	ZIOC	ZPUP	
		MSB	CLKCHG	ALOFF	LC3	SVDDT	SHOTPW	BZSHOT	0	0	0	PTCOUT	SCTRG	HZR3	0			
			OSCC	ALON	LC2	SVDON	BZFQ2	ENVRST	0	0	0	PTC2	SEN	HZR2	HZCS	IOC2	PUP2	
			VSC1	LDUTY	LC1	SVC1	BZFQ1	ENVRT	TMRST	SWRST	PTRST	PTC1	SCS1		ADINC	IOC1	PUP1	
		LSB	VSC0	HLMOD	LC0	SVC0	BZFQ0	ENVON	WDRST	SWRUN	PTRUN	PTC0	SCS0		PICON	IOC0	PUP0	

I/O memory (F00H–F7EH) <E0C624A/4C/48>

PROGRAM NAME : C24A/4C/48																		
P	H	L	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
F	0	NAME	ZTI	ZISW	ZIPT	ZISIO	ZIK0	ZIK1										
		MSB	IT1	0	0	0	0	0										
			IT2	0	0	0	0	0										
			IT8	ISW1	0	0	0	0										
		LSB	IT32	ISW0	IPT	ISIO	IK0	IK1										
	1	NAME	ZEIT	ZEISW	ZEIPT	ZEISIO	ZEIK0	ZEIK1										
		MSB	EIT1	0	0	0	EIK03	EIK13										
			EIT2	0	0	0	EIK02	EIK12										
			EIT8	EISW1	0	0	EIK01	EIK11										
		LSB	EIT32	EISW0	EIPT	EISIO	EIK00	EIK10										
	2	NAME	ZTML	ZTMH	ZSWL	ZSWH	ZPTL	ZPTH	ZRDL	ZRDH								
		MSB	TM3	TM7	SWL3	SWH3	PT3	PT7	RD3	RD7								
			TM2	TM6	SWL2	SWH2	PT2	PT6	RD2	RD6								
			TM1	TM5	SWL1	SWH1	PT1	PT5	RD1	RD5								
		LSB	TM0	TM4	SWL0	SWH0	PT0	PT4	RD0	RD4								
	3	NAME	ZSDL	ZSDH														
		MSB	SD3	SD7														
			SD2	SD6														
			SD1	SD5														
		LSB	SD0	SD4														
	4	NAME	ZK0	ZDFK0	ZK1													
		MSB	K03	DFK03	K13													
			K02	DFK02	K12													
			K01	DFK01	K11													
		LSB	K00	DFK00	K10													
	5	NAME	ZR0	ZR1	ZR2	ZR3	ZR4											
		MSB	R03	R13	R23	R33	R43											
			R02	R12	R22	R32	R42											
			R01	R11	R21	R31	R41											
		LSB	R00	R10	R20	R30	R40											
	6	NAME	ZP0	ZP1	ZP2	ZP3												
		MSB	P03	P13	P23	P33												
			P02	P12	P22	P32												
			P01	P11	P21	P31												
		LSB	P00	P10	P20	P30												
	7	NAME	ZOSC	ZLCD	ZLC	ZSVD	ZBZ	ZENV	ZTRST	ZSWR	ZPTR	ZPTC	ZSC	ZHZR	ZEMA	ZIOC	ZPUP	
		MSB	CLKCHG	ALOFF	LC3	SVDDT	SHOTPW	BZSHOT	0	0	0	PTCOUT	SCTRG	HZR3	0	IOC3	PUP3	
			OSCC	ALON	LC2	SVDON	BZFQ2	ENVRST	0	0	0	PTC2	SEN	HZR2	HZCS	IOC2	PUP2	
			VSC1	LDUTY	LC1	SVC1	BZFQ1	ENVRT	TMRST	SWRST	PTRST	PTC1	SCS1	HZR1	ADINC	IOC1	PUP1	
		LSB	VSC0	HLMOD	LC0	SVC0	BZFQ0	ENVON	WDRST	SWRUN	PTRUN	PTC0	SCS0	HZR0	PICON	IOC0	PUP0	

I/O memory (FC0H–FFFH) <E0C624A/4C/48 only>

PROGRAM NAME : C24A/4C/48																		
P	H	L	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
F	C	NAME																
		MSB	P03'	P13'	P03'	P13'	P03'	P13'	P03'	P13'	P03'	P13'	P03'	P13'	P03'	P13'	P03'	P13'
			P02'	P12'	P02'	P12'	P02'	P12'	P02'	P12'	P02'	P12'	P02'	P12'	P02'	P12'	P02'	P12'
			P01'	P11'	P01'	P11'	P01'	P11'	P01'	P11'	P01'	P11'	P01'	P11'	P01'	P11'	P01'	P11'
		LSB	P00'	P10'	P00'	P10'	P00'	P10'	P00'	P10'	P00'	P10'	P00'	P10'	P00'	P10'	P00'	P10'
	D	NAME																
		MSB	P03'	P13'	P03'	P13'	P03'	P13'	P03'	P13'	P03'	P13'	P03'	P13'	P03'	P13'	P03'	P13'
			P02'	P12'	P02'	P12'	P02'	P12'	P02'	P12'	P02'	P12'	P02'	P12'	P02'	P12'	P02'	P12'
			P01'	P11'	P01'	P11'	P01'	P11'	P01'	P11'	P01'	P11'	P01'	P11'	P01'	P11'	P01'	P11'
		LSB	P00'	P10'	P00'	P10'	P00'	P10'	P00'	P10'	P00'	P10'	P00'	P10'	P00'	P10'	P00'	P10'
	E	NAME																
		MSB	P03'	P13'	P03'	P13'	P03'	P13'	P03'	P13'	P03'	P13'	P03'	P13'	P03'	P13'	P03'	P13'
			P02'	P12'	P02'	P12'	P02'	P12'	P02'	P12'	P02'	P12'	P02'	P12'	P02'	P12'	P02'	P12'
			P01'	P11'	P01'	P11'	P01'	P11'	P01'	P11'	P01'	P11'	P01'	P11'	P01'	P11'	P01'	P11'
		LSB	P00'	P10'	P00'	P10'	P00'	P10'	P00'	P10'	P00'	P10'	P00'	P10'	P00'	P10'	P00'	P10'
	F	NAME																
		MSB	P03'	P13'	P03'	P13'	P03'	P13'	P03'	P13'	P03'	P13'	P03'	P13'	P03'	P13'	P03'	P13'
			P02'	P12'	P02'	P12'	P02'	P12'	P02'	P12'	P02'	P12'	P02'	P12'	P02'	P12'	P02'	P12'
			P01'	P11'	P01'	P11'	P01'	P11'	P01'	P11'	P01'	P11'	P01'	P11'	P01'	P11'	P01'	P11'
		LSB	P00'	P10'	P00'	P10'	P00'	P10'	P00'	P10'	P00'	P10'	P00'	P10'	P00'	P10'	P00'	P10'

APPENDIX C. E0C6244/4A/4C/48 I/O MEMORY MAP

I/O memory (F00H–F15H)

Address	Register								Comment
	D3	D2	D1	D0	Name	Init *1	1	0	
F00H	IT1	IT2	IT8	IT32	IT1 *3	0	Yes	No	Interrupt factor flag (clock timer 1 Hz)
					IT2 *3	0	Yes	No	Interrupt factor flag (clock timer 2 Hz)
	R				IT8 *3	0	Yes	No	Interrupt factor flag (clock timer 8 Hz)
					IT32 *3	0	Yes	No	Interrupt factor flag (clock timer 32 Hz)
F01H	0	0	ISW1	ISW0	0 *4	– *2			
					0 *4	– *2			
	R				ISW1 *3	0	Yes	No	Interrupt factor flag (stopwatch 1 Hz)
					ISW0 *3	0	Yes	No	Interrupt factor flag (stopwatch 10 Hz)
F02H	0	0	0	IPT	0 *4	– *2			
					0 *4	– *2			
	R				0 *4	– *2			
					IPT *3	0	Yes	No	Interrupt factor flag (programmable timer)
F03H	0	0	0	ISIO	0 *4	– *2			
					0 *4	– *2			
	R				0 *4	– *2			
					ISIO *3	0	Yes	No	Interrupt factor flag (serial interface)
F04H	0	0	0	IK0	0 *4	– *2			
					0 *4	– *2			
	R				0 *4	– *2			
					IK0 *3	0	Yes	No	Interrupt factor flag (K00–K03)
F05H	0	0	0	IK1	0 *3	– *2			
					0 *3	– *2			
	R				0 *3	– *2			
					IK1 *4	0	Yes	No	Interrupt factor flag (K10–K13)
F10H	EIT1	EIT2	EIT8	EIT32	EIT1	0	Enable	Mask	Interrupt mask register (clock timer 1 Hz)
					EIT2	0	Enable	Mask	Interrupt mask register (clock timer 2 Hz)
	R/W				EIT8	0	Enable	Mask	Interrupt mask register (clock timer 8 Hz)
					EIT32	0	Enable	Mask	Interrupt mask register (clock timer 32 Hz)
F11H	0	0	EISW1	EISW0	0 *3	– *2			
					0 *3	– *2			
	R		R/W		EISW1	0	Enable	Mask	Interrupt mask register (stopwatch 1 Hz)
					EISW0	0	Enable	Mask	Interrupt mask register (stopwatch 10 Hz)
F12H	0	0	0	EIPT	0 *3	– *2			
					0 *3	– *2			
	R			R/W	0 *3	– *2			
					EIPT	0	Enable	Mask	Interrupt mask register (programmble timer)
F13H	0	0	0	EISIO	0 *3	– *2			
					0 *3	– *2			
	R			R/W	0 *3	– *2			
					EISIO	0	Enable	Mask	Interrupt mask register (serial interface)
F14H	EIK03	EIK02	EIK01	EIK00	EIK03	0	Enable	Mask	Interrupt mask register (K03)
					EIK02	0	Enable	Mask	Interrupt mask register (K02)
	R/W				EIK01	0	Enable	Mask	Interrupt mask register (K01)
					EIK00	0	Enable	Mask	Interrupt mask register (K00)
F15H	EIK13	EIK12	EIK11	EIK10	EIK13	0	Enable	Mask	Interrupt mask register (K13)
					EIK12	0	Enable	Mask	Interrupt mask register (K12)
	R/W				EIK11	0	Enable	Mask	Interrupt mask register (K11)
					EIK10	0	Enable	Mask	Interrupt mask register (K10)

*1 Initial value following initial reset
*2 Not set in the circuit
*3 Reset (0) immediately after being read
*4 Always "0" when being read

I/O memory (F20H–F42H)

Address	Register								Comment
	D3	D2	D1	D0	Name	Init *1	1	0	
F20H	TM3	TM2	TM1	TM0	TM3	0			Clock timer data (16 Hz)
					TM2	0			Clock timer data (32 Hz)
	R				TM1	0			Clock timer data (64 Hz)
					TM0	0			Clock timer data (128 Hz)
F21H	TM7	TM6	TM5	TM4	TM7	0			Clock timer data (1 Hz)
					TM6	0			Clock timer data (2 Hz)
	R				TM5	0			Clock timer data (4 Hz)
					TM4	0			Clock timer data (8 Hz)
F22H	SWL3	SWL2	SWL1	SWL0	SWL3	0			MSB
					SWL2	0			Stopwatch timer
	R				SWL1	0			1/100 sec data (BCD)
					SWL0	0			LSB
F23H	SWH3	SWH2	SWH1	SWH0	SWH3	0			MSB
					SWH2	0			Stopwatch timer
	R				SWH1	0			1/10 sec data (BCD)
					SWH0	0			LSB
F24H	PT3	PT2	PT1	PT0	PT3	X *3			MSB
					PT2	X *3			Programmable timer data (low-order)
	R				PT1	X *3			
					PT0	X *3			LSB
F25H	PT7	PT6	PT5	PT4	PT7	X *3			MSB
					PT6	X *3			Programmable timer data (high-order)
	R				PT5	X *3			
					PT4	X *3			LSB
F26H	RD3	RD2	RD1	RD0	RD3	X *3			MSB
					RD2	X *3			Programmable timer
	R/W				RD1	X *3			reload data (low-order)
					RD0	X *3			LSB
F27H	RD7	RD6	RD5	RD4	RD7	X *3			MSB
					RD6	X *3			Programmable timer
	R/W				RD5	X *3			reload data (high-order)
					RD4	X *3			LSB
F30H	SD3	SD2	SD1	SD0	SD3	X *3			MSB
					SD2	X *3			Serial interface
	R/W				SD1	X *3			data register (low-order)
					SD0	X *3			LSB
F31H	SD7	SD6	SD5	SD4	SD7	X *3			MSB
					SD6	X *3			Serial interface
	R/W				SD5	X *3			data register (high-order)
					SD4	X *3			LSB
F40H	K03	K02	K01	K00	K03	– *2	High	Low	Input port (K00–K03)
					K02	– *2	High	Low	
	R				K01	– *2	High	Low	
					K00	– *2	High	Low	
F41H	DFK03	DFK02	DFK01	DFK00	DFK03	1	↓	↑	Input relation register (DFK00–DFK03)
					DFK02	1	↓	↑	
	R/W				DFK01	1	↓	↑	
					DFK00	1	↓	↑	
F42H	K13	K12	K11	K10	K13	– *2	High	Low	Input port (K10–K13)
					K12	– *2	High	Low	
	R				K11	– *2	High	Low	
					K10	– *2	High	Low	

*1 Initial value following initial reset
*2 Not set in the circuit
*3 Undefined

I/O memory (F50H–F63H)

Address	Register								Comment
	D3	D2	D1	D0	Name	Init *1	1	0	
F50H *6	R03	R02	R01	R00	R03	X *2	High	Low	Output port (R03) / External memory address (A3)
					R02	X *2	High	Low	Output port (R02) / External memory address (A2)
	R/W				R01	X *2	High	Low	Output port (R01) / External memory address (A1)
					R00	X *2	High	Low	Output port (R00) / External memory address (A0)
F51H *6	R13	R12	R11	R10	R13	X *2	High	Low	Output port (R13) / External memory address (A7)
					R12	X *2	High	Low	Output port (R12) / External memory address (A6)
	R/W				R11	X *2	High	Low	Output port (R11) / External memory address (A5)
					R10	X *2	High	Low	Output port (R10) / External memory address (A4)
F52H	R23	R22	R21	R20	R23	X *2	High	Low	Output port (R23) / External memory address (A11) *4
					R22	X *2	High	Low	Output port (R22) / External memory address (A10) *4
	R/W				R21	X *2	High	Low	Output port (R21) / External memory address (A9) *4
					R20	X *2	High	Low	Output port (R20) / External memory address (A8) *4
F53H	R33	R32	R31	R30	R33	X *2	High	Low	Output port (R33)
							Off	On	PTCLK output
	R/W						*3	*3	[$\overline{\text{SRDY}}$ (SIO READY)]
					R32	X *2	High	Low	Output port (R32)
							*3	*3	[External memory read ($\overline{\text{RD}}$)] *4
					R31	X *2	High	Low	Output port (R31) / External memory address (A13) *4
							*3	*3	[External memory write ($\overline{\text{WR}}$)] *4
					R30	X *2	High	Low	Output port (R30) / External memory address (A12) *4
F54H	R43	R42	R41	R40	R43	1	High	Low	Output port (R43)
							Off	On	Buzzer output (BZ)
	R/W				R42	1	High	Low	Output port (R42)
							Off	On	Clock output (FOUT)
							*3	*3	[Buzzer inverted output ($\overline{\text{BZ}}$)]
					R41	1	High	Low	Output port (R41)
							Off	On	LCD frame signal (FR)
					R40	1	High	Low	Output port (R40)
							Off	On	Clock inverted output ($\overline{\text{FOUT}}$)
							Off	On	LCD synchronous signal (CL)
F60H	P03	P02	P01	P00	P03	X *2	High	Low	I/O port (P03) / External memory data (D3) *5
					P02	X *2	High	Low	I/O port (P02) / External memory data (D2) *5
	R/W				P01	X *2	High	Low	I/O port (P01) / External memory data (D1) *5
					P00	X *2	High	Low	I/O port (P00) / External memory data (D0) *5
F61H	P13	P12	P11	P10	P13	X *2	High	Low	I/O port (P13) / External memory data (D7) *5
					P12	X *2	High	Low	I/O port (P12) / External memory data (D6) *5
	R/W				P11	X *2	High	Low	I/O port (P11) / External memory data (D5) *5
					P10	X *2	High	Low	I/O port (P10) / External memory data (D4) *5
F62H	P23	P22	P21	P20	P23	X *2	High	Low	I/O port (P23) / External memory CS ($\overline{\text{CS3}}$) *5
					P22	X *2	High	Low	I/O port (P22) / External memory CS ($\overline{\text{CS2}}$) *5
	R/W				P21	X *2	High	Low	I/O port (P21) / External memory CS ($\overline{\text{CS1}}$) *5
	W				P20	X *2	High	Low	I/O port (P20) / External memory CS ($\overline{\text{CS0}}$) *5
F63H *6	P33	P32	P31	P30	P33	X *2	High	Low	I/O port / Dedicated output port (P33)
					P32	X *2	High	Low	I/O port / Dedicated output port (P32)
	R/W				P31	X *2	High	Low	I/O port / Dedicated output port (P31)
					P30	X *2	High	Low	I/O port / Dedicated output port (P30)

*1 Initial value following initial reset
*2 Undefined
*3 When selecting options enclosed in brackets [ ] as output option, the output register will function as register only and will not affect the individual outputs
*4 In the E0C6244, it can be used only as a port for output
*5 In the E0C6244, it can be used only as a port for I/O port
*6 In the E0C6244, the F50H, F51H and F63H cannot be used

I/O memory (F70H–F79H)

Address	Register								Comment
	D3	D2	D1	D0	Name	Init *1	1	0	
F70H	CLKCHG	OSCC	VSC1	VSC0	CLKCHG	0	OSC3	OSC1	CPU system clock switch
					OSCC	0	On	Off	OSC3 oscillation On/Off
	R/W				VSC1	0			CPU operating voltage switch
					VSC0	0			
F71H	ALOFF	ALON	LDUTY	HLMOD	ALOFF	1	All off	Normal	All LCD dots fade out control
					ALON	0	All on	Normal	All LCD dots displayed control
	R/W				LDUTY	0	1/8	1/16	LCD drive duty switch
					HLMOD	0	HLMOD	Normal	Heavy load protection mode
F72H	LC3	LC2	LC1	LC0	LC3	X *4			LCD contrast adjustment
					LC2	X *4			LC3–LC0 = 0 light
	R/W				LC1	X *4			:
					LC0	X *4			LC3–LC0 = 15 dark
F73H	SVDDT	SVDON	SVC1	SVC0	SVDDT	1 *5	Low	Normal	SVD evaluation data
					SVDON	0	On	Off	SVD circuit On/Off
	R	R/W			SVC1	X *4			SVD criteria voltage setting
					SVC0	X *4			
F74H	SHOTPW	BZFQ2	BZFQ1	BZFQ0	SHOTPW	0	62.5 ms	31.25 ms	1-shot buzzer pulse width
					BZFQ2	0			Buzzer frequency selection
	R/W				BZFQ1	0			
					BZFQ0	0			
F75H	BZSHOT	ENVRST	ENVRT	ENVON	BZSHOT	0	Trigger	–	1-shot buzzer trigger (W)
							BUSY	READY	Status (R)
	W	W	R/W		ENVRST	RESET	Reset	–	Envelope reset
	R				ENVRT	0	1.0 sec	0.5 sec	Envelope cycle selection
					ENVON	0	On	Off	Envelope On/Off
F76H	0	0	TMRST	WDRST	0 *3	– *2			
					0 *3	– *2			
	R		W		TMRST *3	Reset	Reset	–	Clock timer reset
					WDRST	Reset	Reset	–	Watchdog timer reset
F77H	0	0	SWRST	SWRUN	0 *3	– *2			
					0 *3	– *2			
	R		W	R/W	SWRST *3	Reset	Reset	–	Stopwatch timer reset
					SWRUN	0	Run	Stop	Stopwatch timer Run/Stop
F78H	0	0	PTRST	PTRUN	0 *3	– *2			
					0 *3	– *2			
	R		W	R/W	PTRST *3	Reset	Reset	–	Programmable timer reset
					PTRUN	0	Run	Stop	Programmable timer Run/Stop
F79H	PTCOUT	PTC2	PTC1	PTC0	PTCOUT	0	On	Off	Programmable timer clock output
					PTC2	0			Programmable timer input clock selection
	R/W				PTC1	0			
					PTC0	0			

*1 Initial value following initial reset
*2 Not set in the circuit
*3 Always "0" when being read
*4 Undefined
*5 When SVD is off, "1" is read out

I/O memory (F7AH–F7EH)

Address	Register								Comment
	D3	D2	D1	D0	Name	Init *1	1	0	
F7AH	SCTRG	SEN	SCS1	SCS0	SCTRG*3	–	Trigger	–	Serial interface clock trigger
					SEN	0	⌐└	└⌐	Serial interface clock edge selection
	W	R/W			SCS1	0			⌐ ⌐ Serial interface clock mode selection
					SCS0	0			⌐ ⌐
F7BH	HZR3	HZR2	HZR1	HZR0	HZR3*3	0	Output	High-Z	R30–R33 output high-impedance control
					HZR2	0	Output	High-Z	R20–R23 output high-impedance control
	R/W				HZR1*6	0	Output	High-Z	R10–R13 output high-impedance control
					HZR0*6	0	Output	High-Z	R00–R03 output high-impedance control
F7CH	0	HZCS	ADINC	PICON	0 *3 *5, 7	– *2			
					HZCS	0	Output	High-Z	$\overline{CS0}$–$\overline{CS3}$ output high-impedance control
	R	R/W	W	R/W	ADINC *3, 4, 6	– *2	Increment	–	External memory address increment (A0–A13)
					PICON *4, 7	0	Auto Inc.	Normal	External memory address auto increment mode
F7DH	IOC3	IOC2	IOC1	IOC0	IOC3*6	0	Output	Input	I/O control (P30–P33)
					IOC2	0	Output	Input	I/O control (P20–P23)
	R/W				IOC1	0	Output	Input	I/O control (P10–P13)
					IOC0	0	Output	Input	I/O control (P00–P03)
F7EH	PUP3	PUP2	PUP1	PUP0	PUP3*6	0	Off	On	I/O pull up resistor On/Off (P30–P33)
					PUP2	0	Off	On	I/O pull up resistor On/Off (P20–P23)
	R/W				PUP1	0	Off	On	I/O pull up resistor On/Off (P10–P13)
					PUP0	0	Off	On	I/O pull up resistor On/Off (P00–P03)

*1 Initial value following initial reset
*2 Not set in the circuit
*3 Always "0" when being read
*4 These control bits are only valid during selection of external memory/address output as output port option
*5 These control bits are only valid during selection of external memory/chip select output as I/O port option
*6 In the E0C6244, it is a register that becomes invalid and during reading it is always "0"
*7 In the E0C6244, it is used as a general purpose register that does not have a function

I/O memory (FC0H–FFFH)

Address	Register								Comment
	D3	D2	D1	D0	Name	Init *1	1	0	
FC0H | FFEH (even)*3	P03	P02	P01	P00	P03	X *2	High	Low	I/O port (P03) / External memory data bus (D3)
					P02	X *2	High	Low	I/O port (P02) / External memory data bus (D2)
	R/W				P01	X *2	High	Low	I/O port (P01) / External memory data bus (D1)
					P00	X *2	High	Low	I/O port (P00) / External memory data bus (D0)
FC1H | FFFH (odd)*3	P13	P12	P11	P10	P13	X *2	High	Low	I/O port (P13) / External memory data bus (D7)
					P12	X *2	High	Low	I/O port (P12) / External memory data bus (D6)
	R/W				P11	X *2	High	Low	I/O port (P11) / External memory data bus (D5)
					P10	X *2	High	Low	I/O port (P10) / External memory data bus (D4)

*1 Initial value following initial reset
*2 Undefined
*3 Image area of I/O ports (P00–P03, P10–P13) E0C624A/4C/48 only

APPENDIX D. TROUBLESHOOTING

Tool	Problem	Remedy measures
ICE62R (ICE6200)	Nothing appears on the screen, or nothing works, after activation.	Check the following and remedy if necessary: • Is the RS-232C cable connected correctly? • Is the RS-232C driver installed? • Is SPEED.COM or MODE.COM on the disk? • Is the execution file correct? MS-DOS ICS6244/4A/4C/48J.EXE PC-DOS ICS6244/4A/4C/48W.EXE • Is the DOS version correct? MS-DOS Ver. 3.1 or later PC-DOS Ver. 2.1 or later • Is the DIP switches that set the baud rate of the main ICE62R (ICE6200) unit set correctly? • Is the breaker of the ICE62R (ICE6200) set to ON?
	The ICE6200 breaker tripped or the ICE62R fuse cut immediately after activation.	Check the following and remedy if necessary: • Are connectors F1 and F5 connected to the EVA6248 correctly? • Is the target board power short-circuiting?
	<ILLEGAL VERSION ICE6200> appears on the screen immediately after activation.	The wrong version of ICE is being used. Use the latest version.
	<ILLEGAL VERSION PARAMETER FILE> appears on the screen immediately after activation.	The wrong version of ICS6244/4A/4C/48P.PAR is being used. Use the latest version.
	Immediate values A (10) and B (11) cannot be entered correctly with the A command.	The A and B registers are reserved for the entry of A and B. Write 0A and 0B when entering A (10) and B (11). *Example:* `LD A, B` Data in the B register is loaded into the A register. `LD B, 0A` Immediate value A is loaded into the B register.
	<UNUSED AREA> is displayed by the SD command.	This message is output when the address following one in which data is written is unused. It does not indicates problem. Data is correctly set in areas other than the read-only area.
	You can not do a real-time run in break-trace mode.	Since the CPU stops temporarily when breaking conditions are met, executing in a real-time is not performed.
	Output from the EVA is impossible when data is written to the I/O memory for Buzzer and Fout output with the ICE command.	Output is possible only in the real-time run mode.

Tool	Problem	Remedy measures
ASM6244 ASM624A ASM624C ASM6248	An R error occurs although the final page is passed.	The cross assembler is designed to output "R error" every time the page is changed. Use a pseudo-instruction to set the memory, such as ORG or PAGE, to change the page. See "Memory setting pseudo-instructions" in the cross assembler manual.
MDC6244 MDC624A MDC624C MDC6248	Activation is impossible.	Check the following and remedy if necessary: • Is the number of files set at ten or more in OS environment file CONFIG.SYS?
EVA6248	The EVA6248 does not work when it is used independently.	Check the following and remedy if necessary: • Has the EPROM for F.HEX been replaced by the EPROM for the target? • Is the EPROM for F.HEX installed correctly? • Is the appropriate voltage being supplied? (5V DC, 3A, or more) • Are the program ROMs (H and L) installed correctly? • Is data written from address 4000H? (When the 27C256 is used as the program ROM) • Is the EN/DIS switch on the EVA6248 set to EN?
	Target segment does not light.	Check the following and remedy if necessary: • Has the VADJ VR inside the EVA6248 top cover been turned to a lower setting?

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