MF436-06

EPSON

CMOS 4-BIT SINGLE CHIP MICROCOMPUTER

E0C6235 TECHNICAL MANUAL

E0C6235 Technical Hardware

E0C6235 Technical Software

ENERGY SAVING EPSON

SEIKO EPSON CORPORATION

PREFACE

This manual is individualy described about the hardware and the software of the E0C6235.

I. E0C6235 Technical Hardware

This part explains the function of the E0C6235, the circuit configurations, and details the controlling method.

II. E0C6235 Technical Software

This part explains the programming method of the E0C6235.

I. E0C6235 Technical Hardware

CONTENTS

CHAPTER 1 OVERVIEW

The E0C6235 Series is a single-chip microcomputer made up of the 4-bit core CPU E0C6200, ROM (4,096 words, 12 bits to a word), RAM (576 words, 4 bits to a word) LCD driver, serial interface, event counter with dial input function, watchdog timer, and two types of time base counter. Because of its low-voltage operation and low power consumption, this series is ideal for a wide range of applications, and is especially suitable for battery-driven systems.

1.1 Configuration

The E0C6235 Series is configured as follows, depending on supply voltage and oscillation circuits.

Model	E0C6235	E0C62L35	E0C62A35
Supply voltage	3.0 V	1.5 V	3.0 V
Oscillation circuits	OSC1 only (Single clock)	OSC1 only (Single clock)	OSC1 and OSC3 (Twin clock)

1.2 Features

		E0C6235	E0C62L35	E0C62A35
OSC1 oscillation circuit		Crystal oscillation circuit 32,768 Hz (Typ.), 38,400 Hz (Typ.)		
OSC3 oscillation circuit		No setting		CR or Ceramic oscillation circuit (selected by mask option) 500 kHz (Typ.)
Instruction set		108 types		
Instruction execution time (differs depending on instruction) (CLK: CPU operation frequency)		153 µsec, 214 µsec, 366 µsec (CLK = 32,768 Hz)		
		130 µsec, 182 µsec, 313 µsec (CLK = 38,400 Hz)		
				10 µsec, 14 µsec, 24 µsec (CLK = 500 kHz)
ROM capacity		4,096 words, 12 bits per word		
RAM capacity		576 words, 4 bits per word		
Input ports		9 bits (pull-down resistor can be added through mask option)		
Output ports		8 bits (BZ, $\overline{BZ}$, FOUT and SIOF outputs are available through mask option)		
I/O ports		8 bits (pull-down resistor is added during input data read-out)		
Serial interface		1 port (serial 8 bits, clock synchronized)		
LCD driver		Either 48 segments x 4 or 3 common (selected through mask option) V-3 V 1/4 or 1/3 duty (regulated voltage circut and booster voltage circuit built-in)		
Time base counter		Two types (timer and stopwatch)		
Watchdog timer		Built-in (can be disabled through mask option)		
Event counter		Two 8-bit inputs (dial input evaluation or independent)		
Sound generator		Programmable in 8 sounds (8 frequencies) Digital envelope built-in (can be disabled through mask option)		
Analog comparator		Inverted input x 1, noninverted input x 1		
Battery life detection circuit (BLD)		Dual system (programmable in octal values and fixed values)		
		2.4 V, 2.2–2.55 V	1.2 V, 1.05–1.4 V	2.4 V, 2.2–2.55 V
External interrupt		Input interrupt; triple system		
Internal interrupt		Time base counter interrupt; dual system		
		Serial interface interrupt; single system		
Supply voltage		3.0 V (1.8–3.5 V)	1.5 V (0.9–1.7 V)	3.0 V (2.2–3.5 V)
Consumed current (Typ. value)	CLK = 32,768 Hz (when halted)	1.8 µA	1.5 µA	2.0 µA
	CLK = 32,768 Hz (when executed)	6.0 µA	5.0 µA	8.0 µA
	CLK = 500 kHz (when halted)	–	–	130 µA
Form when shipped		100-pin QFP (plastic) or chip		

1.3 Block Diagram

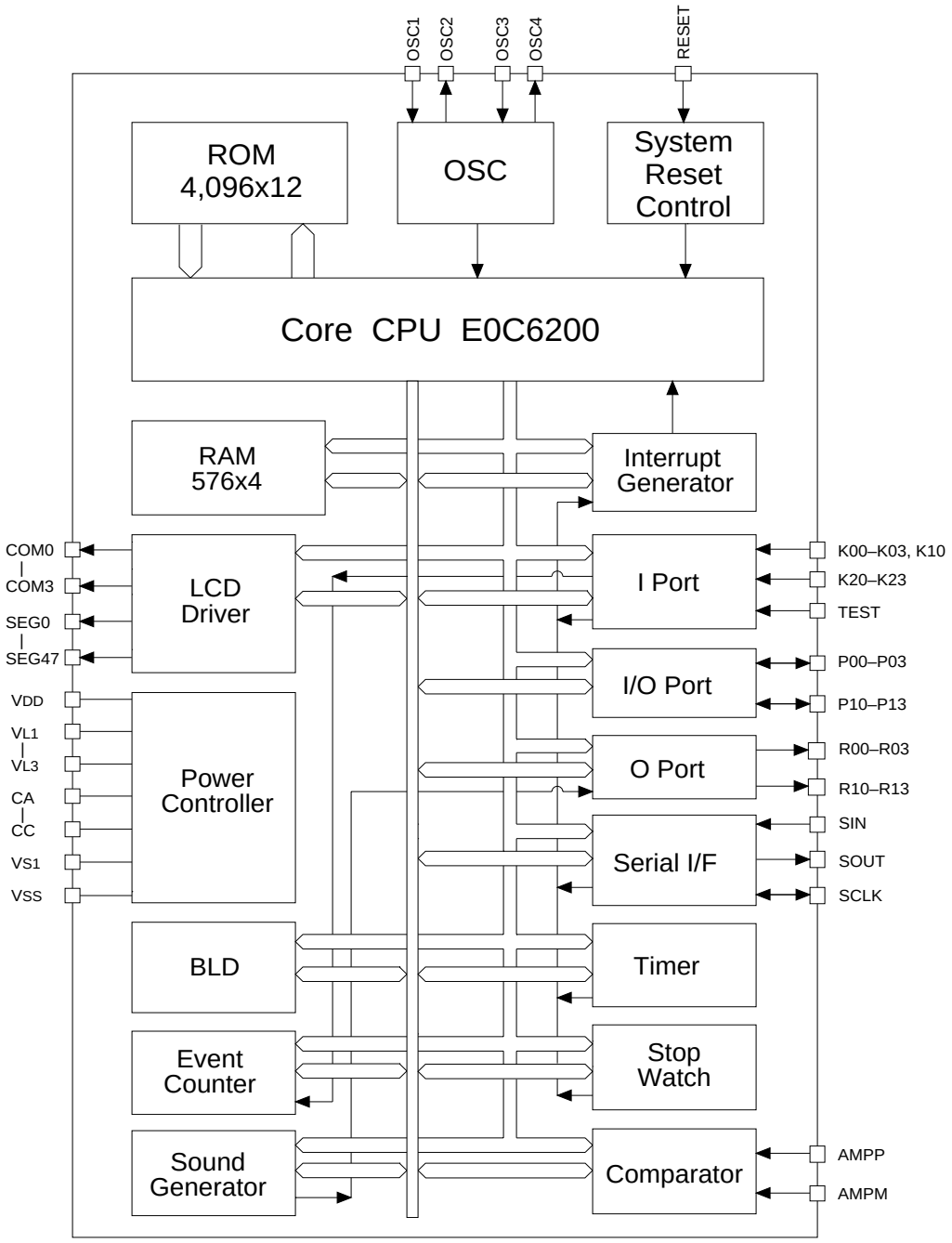
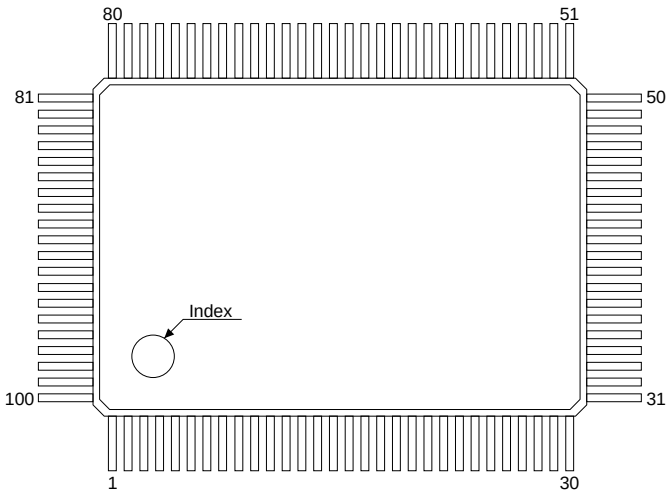


Fig. 1.3.1
Block diagram

1.4 Pin Layout Diagram

F100-5

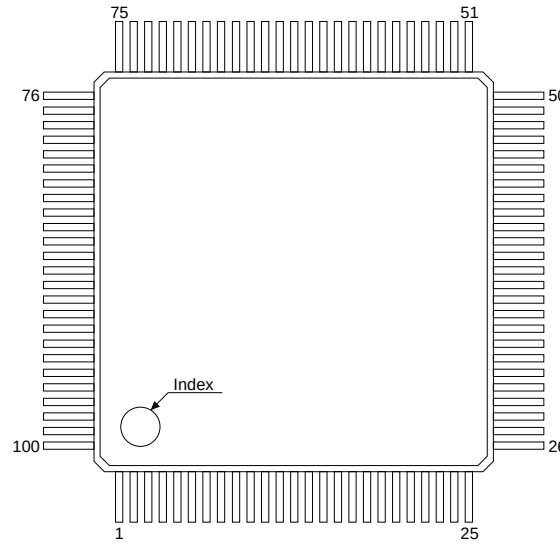


Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	COM1	26	SEG24	51	SEG0	76	P10
2	COM0	27	TEST	52	AMPP	77	R03
3	SEG47	28	SEG23	53	AMPM	78	R02
4	SEG46	29	SEG22	54	K23	79	R01
5	SEG45	30	SEG21	55	K22	80	R00
6	SEG44	31	SEG20	56	K21	81	R12
7	SEG43	32	SEG19	57	K20	82	R11
8	SEG42	33	SEG18	58	K10	83	R10
9	SEG41	34	SEG17	59	K03	84	R13
10	SEG40	35	SEG16	60	K02	85	V_{SS}
11	SEG39	36	SEG15	61	K01	86	RESET
12	SEG38	37	SEG14	62	K00	87	OSC4
13	SEG37	38	SEG13	63	SIN	88	OSC3
14	SEG36	39	SEG12	64	SOUT	89	V_{S1}
15	SEG35	40	SEG11	65	N.C.	90	OSC2
16	SEG34	41	SEG10	66	SCLK	91	OSC1
17	SEG33	42	SEG9	67	P03	92	V_{DD}
18	SEG32	43	SEG8	68	P02	93	V_{L3}
19	SEG31	44	SEG7	69	P01	94	V_{L2}
20	SEG30	45	SEG6	70	P00	95	V_{L1}
21	SEG29	46	SEG5	71	N.C.	96	CA
22	SEG28	47	SEG4	72	N.C.	97	CB
23	SEG27	48	SEG3	73	P13	98	CC
24	SEG26	49	SEG2	74	P12	99	COM3
25	SEG25	50	SEG1	75	P11	100	COM2

N.C.=No Connection

Fig. 1.4.1 Pin assignment (F100-5)

F100-15



Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	SEG47	26	SEG23	51	AMPP	76	R02
2	SEG46	27	SEG22	52	AMPM	77	R01
3	SEG45	28	SEG21	53	K23	78	R00
4	SEG44	29	SEG20	54	K22	79	R12
5	SEG43	30	SEG19	55	K21	80	R11
6	SEG42	31	SEG18	56	K20	81	R10
7	SEG41	32	SEG17	57	K10	82	R13
8	SEG40	33	SEG16	58	K03	83	V_{SS}
9	SEG39	34	SEG15	59	K02	84	RESET
10	SEG38	35	SEG14	60	K01	85	OSC4
11	SEG37	36	SEG13	61	K00	86	OSC3
12	SEG36	37	SEG12	62	SIN	87	V_{S1}
13	SEG35	38	N.C.	63	SOUT	88	OSC2
14	SEG34	39	SEG11	64	N.C.	89	OSC1
15	SEG33	40	SEG10	65	SCLK	90	V_{DD}
16	SEG32	41	SEG9	66	N.C.	91	V_{L3}
17	SEG31	42	SEG8	67	P03	92	V_{L2}
18	SEG30	43	SEG7	68	P02	93	V_{L1}
19	SEG29	44	SEG6	69	P01	94	CA
20	SEG28	45	SEG5	70	P00	95	CB
21	SEG27	46	SEG4	71	P13	96	CC
22	SEG26	47	SEG3	72	P12	97	COM3
23	SEG25	48	SEG2	73	P11	98	COM2
24	SEG24	49	SEG1	74	P10	99	COM1
25	TEST	50	SEG0	75	R03	100	COM0

N.C.=No Connection

Fig. 1.4.2
Pin assignment
(F100-15)

1.5 Pin Description

F100-5

Table 1.5.1 Pin description (F100-5)

Pin Name	Pin Number	Input/output	Function
V_{DD}	92	(I)	Power source positive terminal
V_{SS}	85	(I)	Power source negative terminal
V_{S1}	89	–	Constant voltage output terminal for oscillation
V_{L1}	95	–	Constant voltage output terminal for LCD (approx. -1.05 V)
V_{L2}	94	–	Booster output terminal for LCD ($V_{L1} \times 2$)
V_{L3}	93	–	Booster output terminal for LCD ($V_{L1} \times 3$)
CA–CC	96–98	–	Booster condenser connector terminal
OSC1	91	I	Crystal oscillator input terminal
OSC2	90	O	Crystal oscillator output terminal
OSC3	88	I	*1
OSC4	87	O	*1
K00–23	54–62	I	Input terminal
P00–13	67–70, 73–76	I/O	Input/output terminal
R00–03	77–80	O	Output terminal
R10	83	O	Output terminal (Can output BZ through mask option)
R13	84	O	Output terminal (Can output $\overline{BZ}$ through mask option)
R11	82	O	Output terminal (Can output SIOF through mask option)
R12	81	O	Output terminal (Can output FOUT through mask option)
SIN	63	I	Serial interface input terminal
SOUT	64	O	Serial interface output terminal
SCLK	66	I/O	Input/output terminal for serial interface clock
AMPP	52	I	Analog comparator noninverted input terminal
AMPM	53	I	Analog comparator inverted input terminal
SEG0–47	3–26, 28–51	O	LCD segment output terminal (DC output available through mask option)
COM0–3	1, 2, 99, 100	O	LCD common output terminal
RESET	86	I	Initial resetting input terminal
TEST	27	I	Test input terminal

*1 6235/62L35: N.C. (Not connected)
62A35: CR or ceramic oscillation input terminal
(Switchable through mask option)

F100-15

Table 1.5.2 Pin description (F100-15)

Pin Name	Pin Number	Input/output	Function
V_{DD}	90	(I)	Power source positive terminal
V_{SS}	83	(I)	Power source negative terminal
V_{S1}	87	–	Constant voltage output terminal for oscillation
V_{L1}	93	–	Constant voltage output terminal for LCD (approx. -1.05 V)
V_{L2}	92	–	Booster output terminal for LCD ($V_{L1} \times 2$)
V_{L3}	91	–	Booster output terminal for LCD ($V_{L1} \times 3$)
CA–CC	94–96	–	Booster condenser connector terminal
OSC1	89	I	Crystal oscillator input terminal
OSC2	88	O	Crystal oscillator output terminal
OSC3	86	I	*1
OSC4	85	O	*1
K00–23	53–61	I	Input terminal
P00–13	67–74	I/O	Input/output terminal
R00–03	75–78	O	Output terminal
R10	81	O	Output terminal (Can output BZ through mask option)
R13	82	O	Output terminal (Can output $\overline{BZ}$ through mask option)
R11	80	O	Output terminal (Can output SIOF through mask option)
R12	79	O	Output terminal (Can output FOUT through mask option)
SIN	62	I	Serial interface input terminal
SOUT	63	O	Serial interface output terminal
SCLK	65	I/O	Input/output terminal for serial interface clock
AMPP	51	I	Analog comparator noninverted input terminal
AMPM	52	I	Analog comparator inverted input terminal
SEG0–47	1–24, 26–50	O	LCD segment output terminal (DC output available through mask option)
COM0–3	97–100	O	LCD common output terminal
RESET	84	I	Initial resetting input terminal
TEST	25	I	Test input terminal

*1 6235/62L35: N.C. (Not connected)
62A35: CR or ceramic oscillation input terminal
(Switchable through mask option)

CHAPTER 2 POWER SUPPLY AND INITIAL RESET

2.1 Power Supply

With a single external power supply (*1) supplied to VDD through VSS, the E0C6235 Series generates the necessary internal voltage with the regulated voltage circuit (<VS1> for oscillators, <VL1> for LCDs) and the voltage booster circuit (<VL2, VL3> for LCDs).

Figure 2.1.1 shows the configuration of power supply.

*1 Supply voltage: 6235/62A35 .. 3 V, 62L35 .. 1.5 V

Notes
- *External loads cannot be driven by the regulated voltage and voltage booster circuit's output voltage.*
- *See "7 ELECTRICAL CHARACTERISTICS" for voltage values.*

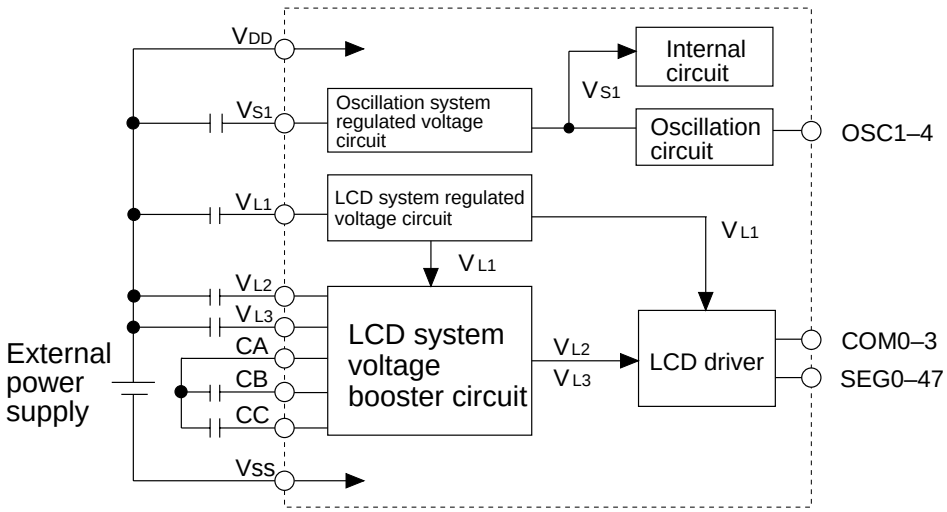


Fig. 2.1.1 Configuration of power supply

2.2 Initial Reset

To initialize the E0C6235 Series circuits, initial reset must be executed. There are four ways of doing this.

(1) Initial reset by the oscillation detection circuit

(2) External initial reset by the RESET terminal

(3) External initial reset by simultaneous high input to terminals K00–K03

(4) Initial reset by watchdog timer

Figure 2.2.1 shows the configuration of the initial reset circuit.

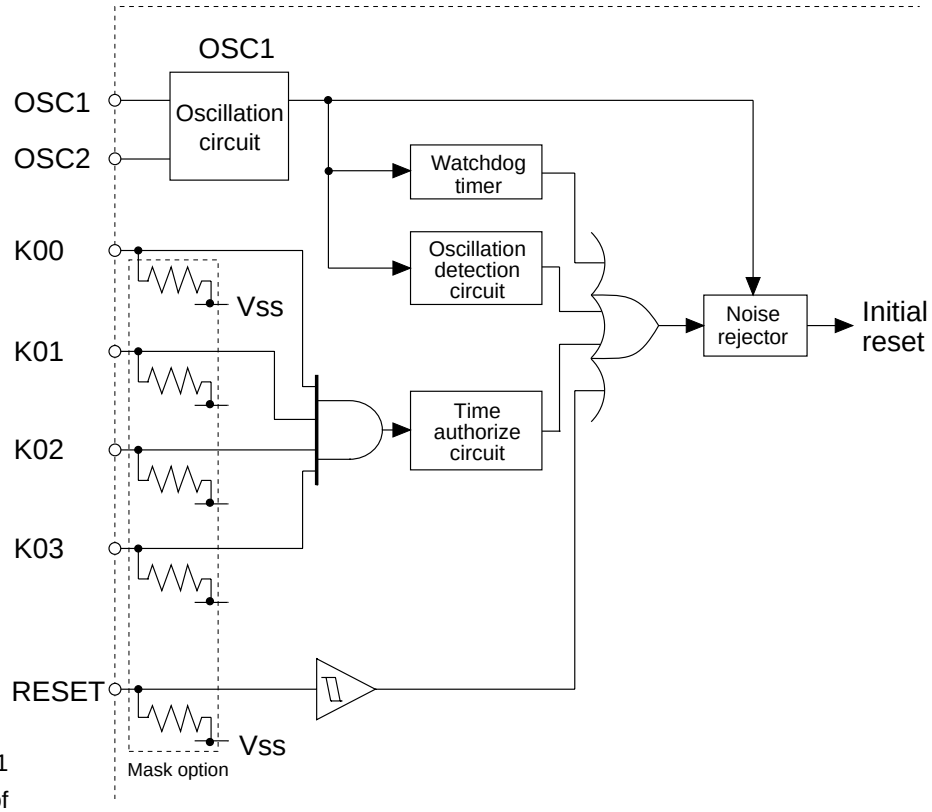


Fig. 2.2.1
Configuration of initial reset circuit

Oscillation detection circuit

The oscillation detection circuit outputs the initial reset signal at power-on until the crystal oscillation circuit (OSC1) begins oscillating, or when this crystal oscillation circuit (OSC1) halts oscillating for some reason.
However, depending on the power-on sequence (voltage rise timing), the circuit may not work properly. Therefore, use the reset terminal or reset by simultaneous high input to the input port (K00–K03) for initial reset after turning power on.

Reset terminal (RESET)

Initial reset can be executed externally by setting the reset terminal to the high level. This high level must be maintained for at least 5 msec (when oscillating frequency is f_{OSC1} = 32 kHz), because the initial reset circuit contains a noise rejector. When the reset terminal goes low the CPU begins to operate.

Simultaneous high input to input ports (K00–K03)

Another way of executing initial reset externally is to input a high signal simultaneously to the input ports (K00–K03) selected with the mask option. The specified input port terminals must be kept high for at least 5 msec (when oscillating frequency is f_{OSC1} = 32 kHz), because the initial reset circuit contains a noise rejector. Table 2.2.1 shows the combinations of input ports (K00–K03) that can be selected with the mask option.

Table 2.2.1
Input port combinations

A	Not used
B	K00*K01
C	K00*K01*K02
D	K00*K01*K02*K03

When, for instance, mask option D (K00*K01*K02*K03) is selected, initial reset is executed when the signals input to the four ports K00–K03 are all high at the same time.

Further, the time authorize circuit can be selected with the mask option. The time authorize circuit performs initial reset, when the input time of the simultaneous high input is authorized and found to be the same or more than the defined time (1 to 2 sec).

If you use this function, make sure that the specified ports do not go high at the same time during ordinary operation.

Watchdog timer

If the CPU runs away for some reason, the watchdog timer will detect this situation and output an initial reset signal. See "4.2 Resetting Watchdog Timer" for details.

Internal register at initial reset

Initial reset initializes the CPU as shown in the table below.

Table 2.2.2 Initial values

CPU Core			
Name	Symbol	Number of bits	Setting value
Program counter step	PCS	8	00H
Program counter page	PCP	4	1H
New page pointer	NPP	4	1H
Stack pointer	SP	8	Undefined
Index register X	X	10	Undefined
Index register Y	Y	10	Undefined
Register pointer	RP	4	Undefined
General-purpose register A	A	4	Undefined
General-purpose register B	B	4	Undefined
Interrupt flag	I	1	0
Decimal flag	D	1	Undefined
Zero flag	Z	1	Undefined
Carry flag	C	1	Undefined

Peripheral circuits		
Name	Number of bits	Setting value
RAM	4	Undefined
Segment data	4	Undefined
Other peripheral circuit	4	*1

*1 See "4.1 Memory Map"

2.3 Test Terminal (TEST)

This terminal is used when the IC load is being detected. During ordinary operation be certain to connect this terminal to Vss.

CHAPTER 3 CPU, ROM, RAM

3.1 CPU

The E0C6235 Series employs the core CPU E0C6200 for the CPU, so that register configuration, instructions and so forth are virtually identical to those in other family processors using the E0C6200.
Refer to "E0C6200 Core CPU Manual" for details about the E0C6200.
Note the following points with regard to the E0C6235 Series:

(1) The SLEEP operation is not assumed, so the SLP instruction cannot be used.

(2) Because the ROM capacity is 4,096 words, bank bits are unnecessary and PCB and NBP are not used.

(3) RAM is set up to two pages, so only the two low-order bits are valid for the page portion (XP, YP) of the index register that specifies addresses.
(The two high-order bits are ignored.)

3.2 ROM

The built-in ROM, a mask ROM for loading the program, has a capacity of 4,096 steps, 12 bits each. The program area is 16 pages (0–15), each of 256 steps (00H–FFH). After initial reset, the program beginning address is page 1, step 00H. The interrupt vector is allocated to page 1, steps 01H–0FH.

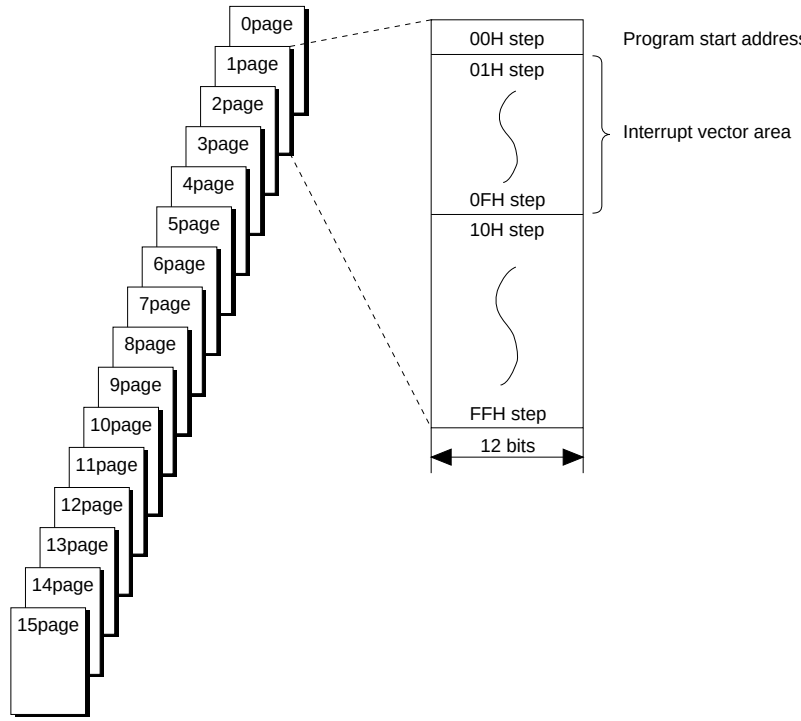


Fig. 3.2.1
ROM configuration

3.3 RAM

The RAM, a data memory storing a variety of data, has a capacity of 576 words, each of four bits. When programming, keep the following points in mind.

(1) Part of the data memory can be used as stack area when subroutine calls and saving registers, so be careful not to overlap the data area and stack area.

(2) Subroutine calls and interrupts take up three words of the stack area.

(3) The data memory 000H–00FH is for the register pointers (RP), and is the addressable memory register area.

See "4.1 Memory Map" for details.

CHAPTER 4 PERIPHERAL CIRCUITS AND OPERATION

Peripheral circuits (timer, I/O, and so on) of the E0C6235 Series are memory mapped, and interfaced with the CPU. Thus, all the peripheral circuits can be controlled by using the memory operation command to access the I/O memory in the memory map.
The following sections describe how the peripheral circuits operation.

4.1 Memory Map

Data memory of the E0C6235 Series has an address space of 608 words (656 words when display memory is laid out over two pages), of which 48 words are allocated to display memory and 32 words to I/O memory.
Figures 4.1.1(a)–(c) present the overall memory maps of the E0C6235 Series, and Tables 4.1.1(a)–(c) the peripheral circuits' (I/O space) memory maps.

Address Page	Low / High	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	0	M0	M1	M2	M3	M4	M5	M6	M7	M8	M9	MA	MB	MC	MD	ME	MF
	1	RAM (256 words x 4 bits) R/W															
	2																
	3																
	4																
	5																
	6																
	7																
	8																
	9																
	A																
	B																
	C																
	D																
	E																
	F																
1	0	RAM (256 words x 4 bits) R/W															
	1																
	2																
	3																
	4																
	5																
	6																
	7																
	8																
	9																
	A																
	B																
	C																
	D																
	E																
	F																

Fig. 4.1.1(a)
Memory map (page 0,1)

Address Page	Low / High	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
2	0	RAM (64 words x 4 bits) R/W															
	1																
	2																
	3																
	4	Unused area															
	5																
	6																
	7																
	8																
	9																
	A																
	B																
	C																
	D																
	E	I/O memory [See Tables 4.1.1(a)–(c)]															
	F																

Fig. 4.1.1(b)
Memory map (page2)

Address Page	Low / High	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0 or 2	4	Display memory (48 words x 4 bits) R/W (W)															
	5																
	6																

Fig. 4.1.1(c)
Memory map
(segment area)

Notes (1) See Tables 4.1.1(a)–(c) for details of I/O memory.

(2) The mask option can be used to select whether to assign the overall area of display memory to page 0 or page 2.

When page 0 (040H–06FH) is selected, read/write is enabled. When page 2 (240H–26FH) is selected, write only is enabled.

If page 0 is assigned, RAM (040H–06FH) is 48 words, and used as the segment area.

(3) Memory is not mounted in unused area within the memory map and in memory area not indicated in this chapter. For this reason, normal operation cannot be assured for programs that have been prepared with access to these areas.

Table 4.1.1(a) I/O memory map (2E0H–2EDH)

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
2E0H	TM3	TM2	TM1	TM0	TM3	0			Timer data (clock timer 2 Hz)
					TM2	0			Timer data (clock timer 4 Hz)
	R				TM1	0			Timer data (clock timer 8 Hz)
					TM0	0			Timer data (clock timer 16 Hz)
2E1H	SWL3	SWL2	SWL1	SWL0	SWL3	0			MSB
					SWL2	0			Stopwatch timer data 1/100 sec (BCD)
	R				SWL1	0			
					SWL0	0			LSB
2E2H	SWH3	SWH2	SWH1	SWH0	SWH3	0			MSB
					SWH2	0			Stopwatch timer data 1/10 sec (BCD)
					SWH1	0			
					SWH0	0			LSB
2E3H	K03	K02	K01	K00	K03	– *2	High	Low	Input port data (K00–K03)
					K02	– *2	High	Low	
	R				K01	– *2	High	Low	
					K00	– *2	High	Low	
2E4H	KCP03	KCP02	KCP01	KCP00	KCP03	0	↓	↑	Input comparison register (K00–K03)
					KCP02	0	↓	↑	
	R/W				KCP01	0	↓	↑	
					KCP00	0	↓	↑	
2E5H	EIK03	EIK02	EIK01	EIK00	EIK03	0	Enable	Mask	Interrupt mask register (K00–K03)
					EIK02	0	Enable	Mask	
	R/W				EIK01	0	Enable	Mask	
					EIK00	0	Enable	Mask	
2E6H	HLMOD	BLD0	EISWIT1	EISWIT0	HLMOD	0	Heavy load	Normal	Heavy load protection mode register
					BLD0	0	Low	Normal	Sub-BLD evaluation data
	R/W	R	R/W		EISWIT1	0	Enable	Mask	Interrupt mask register (stopwatch 1 Hz)
					EISWIT0	0	Enable	Mask	Interrupt mask register (stopwatch 10 Hz)
2E7H	SCTRG	EIK10	KCP10	K10	SCTRG*3	–	Trigger	–	Serial interface clock trigger
					EIK10	0	Enable	Mask	Interrupt mask register (K10)
	W	R/W		R	KCP10	0	↓	↑	Input comparison register (K10)
					K10	– *2	High	Low	Input port data (K10)
2E8H	CSDC	ETI2	ETI8	ETI32	CSDC	0	Static	Dynamic	LCD drive switch
					ETI2	0	Enable	Mask	Interrupt mask register (clock timer 2 Hz)
	R/W				ETI8	0	Enable	Mask	Interrupt mask register (clock timer 8 Hz)
					ETI32	0	Enable	Mask	Interrupt mask register (clock timer 32 Hz)
2E9H	0	TI2	TI8	TI32	0 *3	– *2	–	–	Unused
					TI2 *4	0	Yes	No	Interrupt factor flag (clock timer 2 Hz)
	R				TI8 *4	0	Yes	No	Interrupt factor flag (clock timer 8 Hz)
					TI32 *4	0	Yes	No	Interrupt factor flag (clock timer 32 Hz)
2EAH	IK1	IK0	SWIT1	SWIT0	IK1 *4	0	Yes	No	Interrupt factor flag (K10)
					IK0 *4	0	Yes	No	Interrupt factor flag (K00–K03)
	R				SWIT1 *4	0	Yes	No	Interrupt factor flag (stopwatch 1 Hz)
					SWIT0 *4	0	Yes	No	Interrupt factor flag (stopwatch 10 Hz)
2EBH	R03	R02	R01	R00	R03	0	High	Low	Output port (R03)
					R02	0	High	Low	Output port (R02)
	R/W				R01	0	High	Low	Output port (R01)
					R00	0	High	Low	Output port (R00)
2ECH	R13	R12	R11 / SIOF	R10	R13	0	High/On	Low/Off	Output port (R13)/$\overline{BZ}$ output control
					R12	0	High/On	Low/Off	Output port (R12)/FOUT output control
	R/W		R/W / R	R/W	R11	0	High	Low	Output port (R11, LAMP)
					SIOF	0	Run	Stop	Output port (SIOF)
					R10	0	High/On	Low/Off	Output port (R10)/BZ output control
2EDH	P03	P02	P01	P00	P03	– *2	High	Low	I/O port data (P00–P03)
					P02	– *2	High	Low	
	R/W				P01	– *2	High	Low	Output latch reset at time of SR
					P00	– *2	High	Low	

*1 Initial value at the time of initial reset
*2 Not set in the circuit
*3 Constantly "0" when being read
*4 Reset (0) immediately after being read
*5 Undefined

Table 4.1.1(b) I/O memory map (2EEH–2FBH)

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
2EEH	TMRST	SWRUN	SWRST	IOC0	TMRST*3	Reset	Reset	–	Clock timer reset
					SWRUN	0	Run	Stop	Stopwatch timer Run/Stop
	W	R/W	W	R/W	SWRST*3	Reset	Reset	–	Stopwatch timer reset
					IOC0	0	Output	Input	I/O control register 0 (P00–P03)
2EFH	WDRST	WD2	WD1	WD0	WDRST*3	Reset	Reset	–	Watchdog timer reset
					WD2	0			Timer data (watchdog timer) 1/4 Hz
	W	R			WD1	0			Timer data (watchdog timer) 1/2 Hz
					WD0	0			Timer data (watchdog timer) 1 Hz
2F0H	SD3	SD2	SD1	SD0	SD3	× *5			Serial interface data register (low-order 4 bits)
					SD2	× *5			
	R/W				SD1	× *5			
					SD0	× *5			
2F1H	SD7	SD6	SD5	SD4	SD7	× *5			Serial interface data register (high-order 4 bits)
					SD6	× *5			
	R/W				SD5	× *5			
					SD4	× *5			
2F2H	SCS1	SCS0	SE2	EISIO	SCS1	1			SIF clock mode selection register [SCS1, 0]: 0 Clock, 1 CLK, 2 CLK/2, 3 CLK/4, slave
					SCS0	1			
	R/W				SE2	0	↑	↓	SIF clock edge selection register
					EISIO	0	Enable	Mask	Interrupt mask register (serial interface)
2F3H	0	0	IK2	ISIO	0 *3	– *2	–	–	Unused
					0 *3	– *2	–	–	Unused
	R				IK2 *4	0	Yes	No	Interrupt factor flag (K20–K23)
					ISIO *4	0	Yes	No	Interrupt factor flag (serial interface)
2F4H	K23	K22	K21	K20	K23	– *2	High	Low	Input port data (K20–K23)
					K22	– *2	High	Low	
	R				K21	– *2	High	Low	
					K20	– *2	High	Low	
2F5H	EIK23	EIK22	EIK21	EIK20	EIK23	0	Enable	Mask	Interrupt mask register (K20–K23)
					EIK22	0	Enable	Mask	
	R/W				EIK21	0	Enable	Mask	
					EIK20	0	Enable	Mask	
2F6H	BZFQ2	BZFQ1	BZFQ0	ENVRST	BZFQ2	0			Buzzer frequency selection [BZFQ2–0]: 0 fOSC1/8, 1 fOSC1/10, 2 fOSC1/12, 3 fOSC1/14, 4 fOSC1/16, 5 fOSC1/20, 6 fOSC1/24, 7 fOSC1/28
					BZFQ1	0			
	R/W			W	BZFQ0	0			
					ENVRST*3	Reset	Reset	–	Envelope reset
2F7H	ENVON	ENVRT	AMPDT	AMPON	ENVON	0	On	Off	Envelope On/Off
					ENVRT	0	1.0 sec	0.5 sec	Envelope cycle selection register
	R/W		R	R/W	AMPDT	1	+ > -	+ < -	Analog comparator data
					AMPON	0	On	Off	Analog comparator On/Off
2F8H	EV03	EV02	EV01	EV00	EV03	0			Event counter 0 (low-order 4 bits)
					EV02	0			
	R				EV01	0			
					EV00	0			
2F9H	EV07	EV06	EV05	EV04	EV07	0			Event counter 0 (high-order 4 bits)
					EV06	0			
	R				EV05	0			
					EV04	0			
2FAH	EV13	EV12	EV11	EV10	EV13	0			Event counter 1 (low-order 4 bits)
					EV12	0			
	R				EV11	0			
					EV10	0			
2FBH	EV17	EV16	EV15	EV14	EV17	0			Event counter 1 (high-order 4 bits)
					EV16	0			
	R				EV15	0			
					EV14	0			

*1 Initial value at the time of initial reset
*2 Not set in the circuit
*3 Constantly "0" when being read
*4 Reset (0) immediately after being read
*5 Undefined

Table 4.1.1(c) I/O memory map (2FCH–2FFH)

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
2FCH	EVSEL	ENRUN	EV1RST	EV0RST	EVSEL	0	Separate	Phase	Event counter mode
					EVRUN	0	Run	Stop	Event counter Run/Stop
	R/W		W		EV1RST*3	Reset	Reset	–	Event counter 1 reset
					EV0RST*3	Reset	Reset	–	Event counter 0 reset
2FDH	P13	P12	P11	P10	P13	– *2	High	Low	I/O port data (P10–P13)
					P12	– *2	High	Low	
	R/W				P11	– *2	High	Low	Output latch reset at time of SR
					P10	– *2	High	Low	
2FEH	PRSM	CLKCHG	OSCC	IOC1	PRSM	0	38 kHz	32 kHz	OSC1 prescaler selection
					CLKCHG	0	OSC3	OSC1	CPU clock switch
	R/W				OSCC	0	On	Off	OSC3 oscillation On/Off
					IOC1	0	Output	Input	I/O control register 1 (P10–P13)
2FFH	BLS	BLC2	BLC1	BLC0	BLS	0	On	Off	BLD On/Off
	BLD1				BLD1	0	Low	Normal	BLD voltage evaluation data
	W	R/W			BLC2	× *5			Evaluation voltage setting register
	R				BLC1	× *5			[BLC2–0] 0 1 2 3 4 5 6 7
					BLC0	× *5			E0C6235/62A35 2.20 2.25 2.30 2.35 2.40 2.45 2.50 2.55 (V)
									E0C62L35 1.05 1.10 1.15 1.20 1.25 1.30 1.35 1.40 (V)

*1 Initial value at the time of initial reset
*2 Not set in the circuit
*3 Constantly "0" when being read
*4 Reset (0) immediately after being read
*5 Undefined

4.2 Resetting Watchdog Timer

Configuration of watchdog timer

The E0C6235 Series incorporates a watchdog timer as the source oscillator for OSC1 (clock timer 2 Hz signal). The watchdog timer must be reset cyclically by the software. If reset is not executed in at least 3 or 4 seconds, the initial reset signal is output automatically for the CPU.
Figure 4.2.1 is the block diagram of the watchdog timer.

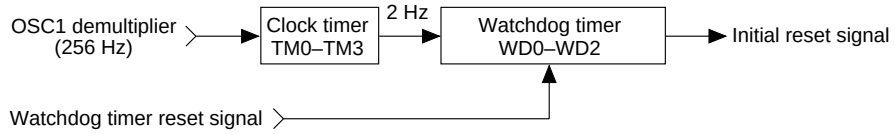


Fig. 4.2.1
Watchdog timer
block diagram

The watchdog timer, configured of a three-bit binary counter (WD0–WD2), generates the initial reset signal internally by overflow of the MSB.
Watchdog timer reset processing in the program's main routine enables detection of program overrun, such as when the main routine's watchdog timer processing is bypassed. Ordinarily this routine is incorporated where periodic processing takes place, just as for the timer interrupt routine.
The watchdog timer operates in the halt mode. If the halt status continues for 3 or 4 seconds, the initial reset signal restarts operation.

Mask option

You can select whether or not to use the watchdog timer with the mask option. When "Not use" is chosen, there is no need to reset the watchdog timer.

Control of watchdog timer

Table 4.2.1 lists the watchdog timer's control bits and their addresses.

Table 4.2.1 Control bits of watchdog timer

Address	Register								Comment
	D3	D2	D1	D0	Name	Init *1	1	0	
2EFH	WDRST	WD2	WD1	WD0	WDRST*3	Reset	Reset	–	Watchdog timer reset
					WD2	0			Timer data (watchdog timer) 1/4 Hz
	W	R			WD1	0			Timer data (watchdog timer) 1/2 Hz
					WD0	0			Timer data (watchdog timer) 1 Hz

*1 Initial value at the time of initial reset
*2 Not set in the circuit
*3 Constantly "0" when being read
*4 Reset (0) immediately after being read
*5 Undefined

WDRST: Watchdog timer reset (2EFH·D3)

This is the bit for resetting the watchdog timer.

When "1" is written : Watchdog timer is reset
When "0" is written : No operation
Read-out : Always "0"

When "1" is written to WDRST, the watchdog timer is reset, and the operation restarts immediately after this. When "0" is written to WDRST, no operation results.
This bit is dedicated for writing, and is always "0" for read-out.

Programming note

When the watchdog timer is being used, the software must reset it within 3-second cycles, and timer data (WD0–WD2) cannot be used for timer applications.

4.3 Oscillation Circuit and Prescaler

OSC1 oscillation circuit

The E0C6235 Series has a built-in crystal oscillation circuit (OSC1 oscillation circuit). As an external element, the OSC1 oscillation circuit generates the operating clock for the CPU and peripheral circuitry by connecting the crystal oscillator (Typ. 32.768 kHz) and trimmer capacitor (5–25 pF).
Figure 4.3.1 is the block diagram of the OSC1 oscillation circuit.

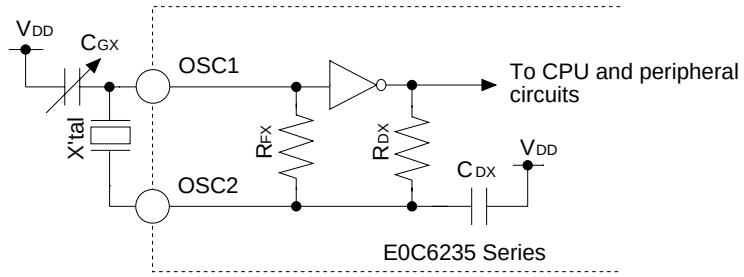


Fig. 4.3.1
OSC1 oscillation circuit

As Figure 4.3.1 indicates, the crystal oscillation circuit can be configured simply by connecting the crystal oscillator (X'tal) between terminals OSC1 and OSC2 to the trimmer capacitor (C_{GX}) between terminals OSC1 and V_{DD}.
Also, the crystal oscillator can be connected to the 38.4 kHz oscillator in addition to the 32.768 kHz oscillator (by mask option).

OSC3 oscillation circuit

In the E0C6235 Series, the E0C63A35 has twin clock specification. The mask option enables selection of either the CR or ceramic oscillation circuit (OSC3 oscillation circuit) as the CPU's subclock. Because the oscillation circuit itself is built-in, it provides the resistance as an external element when CR oscillation is selected, but when ceramic oscillation is selected both the ceramic oscillator and two capacitors (gate and drain capacitance) are required.
Figure 4.3.2 is the block diagram of the OSC3 oscillation circuit.

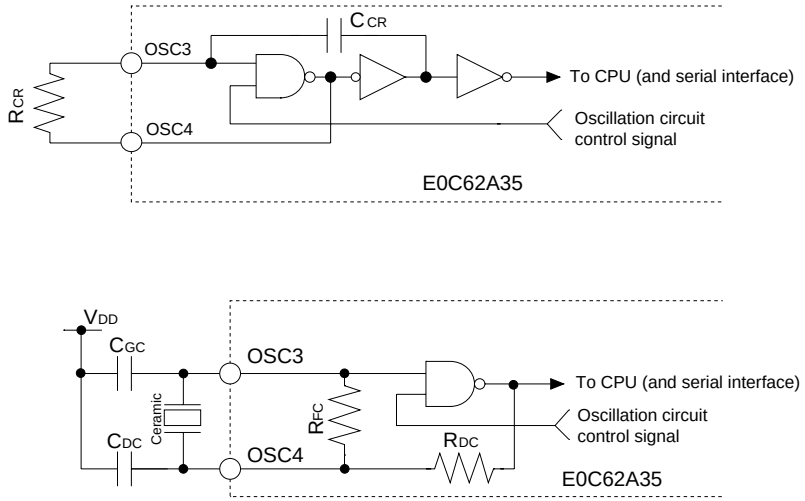


Fig. 4.3.2
OSC3 oscillation circuit

As indicated in Figure 4.3.2, the CR oscillation circuit can be configured simply by connecting the resistor (R_{CR}) between terminals OSC3 and OSC4 when CR oscillation is selected. When 82 kΩ is used for R_{CR}, the oscillation frequency is about 410 kHz. When ceramic oscillation is selected, the ceramic oscillation circuit can be configured by connecting the ceramic oscillator (Typ. 500 kHz) between terminals OSC3 and OSC4 to the two capacitors (C_{GC} and C_{DC}) located between terminals OSC3 and OSC4 and V_{DD}. For both C_{GC} and C_{DC}, connect capacitors that are about 100 pF. To lower current consumption of the OSC3 oscillation circuit, oscillation can be stopped through the software.

For the E0C6235 and E0C62L35 (single clock specification), do not connect anything to terminals OSC3 and OSC4.

Configuration of oscillation circuit and prescaler

The E0C6235 and E0C62L35 have one oscillation circuit (OSC1), and the E0C62A35 has two oscillation circuits (OSC1 and OSC3). OSC1 is a crystal oscillation circuit that supplies the operating clock the CPU and peripheral circuits. OSC3 is either a CR or ceramic oscillation circuit. When processing with the E0C62A35 requires high-speed operation, the CPU operating clock can be switched from OSC1 to OSC3.
Figure 4.3.3 is the block diagram of this oscillation system.

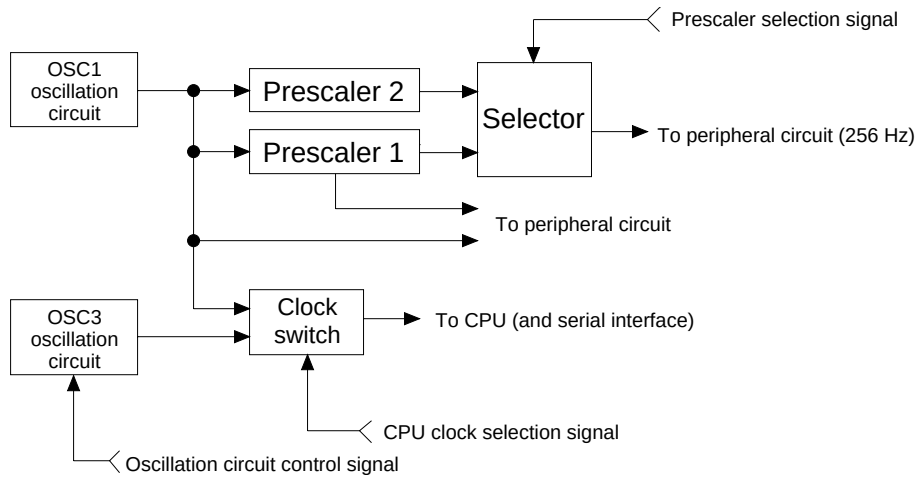


Fig. 4.3.3
Oscillation system

As Figure 4.3.3 indicates, two prescalers (demultiplier stage) are connected to the oscillation circuit.
Prescaler 1 is for 32.768 kHz and prescaler 2 is for 38.4 kHz. These can be selected through the software to suit the crystal oscillator. This selection invokes the basic signal (256 Hz) for running the clock timer, stopwatch timer, and so forth.
Also for E0C62A35, selection of either OSC1 or OSC3 for the CPU's operating clock can be made through the software.

Control of oscillation circuit and prescaler

Table 4.3.1 lists the control bits and their addresses for the oscillation circuit.

Table 4.3.1 Control bits of oscillation circuit and prescaler

Address	Register								Comment
	D3	D2	D1	D0	Name	Init *1	1	0	
2FEH	PRSM	CLKCHG	OSCC	IOC1	PRSM	0	38 kHz	32 kHz	OSC1 prescaler selection
					CLKCHG	0	OSC3	OSC1	CPU clock switch
					OSCC	0	On	Off	OSC3 oscillation On/Off
	R/W				IOC1	0	Output	Input	I/O control register 1 (P10–P13)

*1 Initial value at the time of initial reset
*2 Not set in the circuit
*3 Constantly "0" when being read
*4 Reset (0) immediately after being read
*5 Undefined

OSCC: OSC3 oscillation control (2FEH·D1)

Controls oscillation ON/OFF for the OSC3 oscillation circuit. (E0C62A35 only.)

When "1" is written : The OSC3 oscillation ON
When "0" is written : The OSC3 oscillation OFF
Read-out : Valid

When it is necessary to operate the CPU of the E0C62A35 at high speed, set OSCC to "1". At other times, set it to "0" to lessen the current consumption.
For E0C6235 and E0C62L35, keep OSCC set to "0".
At initial reset, OSCC is set to "0".

CLKCHG: The CPU's clock switch (2FEH·D2)

The CPU's operation clock is selected with this register. (E0C62A35 only.)

When "1" is written : OSC3 clock is selected
When "0" is written : OSC1 clock is selected
Read-out : Valid

When the E0C62A35's CPU clock is to be OSC3, set CLKCHG to "1"; for OSC1, set CLKCHG to "0". This register cannot be controlled for E0C6235 and E0C62L35, so that OSC1 is selected no matter what the set value.
At initial reset, CLKCHG is set to "0".

PRSM: OSC1 prescaler selection (2FEH·D3)

Selects the prescaler for the crystal oscillator of the OSC1 oscillation circuit.

When "1" is written : 38.4 kHz
When "0" is written : 32.768 kHz
Read-out : Valid

Operation of the clock timer and stopwatch timer can be mode accurate by selecting this register. When the set value for this register does not suit the crystal oscillator used, the operation cycles of the previously mentioned peripheral circuitry is multiplied as shown in Table 4.3.2.

Table 4.3.2 Operation cycle when the setting is wrong

32.768 kHz, PRSM = "1"	T'≈1.172T
38.4 kHz, PRSM = "0"	T'≈0.853T

At initial reset, PRSM is set to "0".

Programming notes

(1) It takes at least 5 msec from the time the OSC3 oscillation circuit goes ON until the oscillation stabilizes. Consequently, when switching the CPU operation clock from OSC1 to OSC3, do this after a minimum of 5 msec have elapsed since the OSC3 oscillation went ON.
Further, the oscillation stabilization time varies depending on the external oscillator characteristics and conditions of use, so allow ample margin when setting the wait time.

(2) When switching the clock form OSC3 to OSC1, use a separate instruction for switching the OSC3 oscillation OFF. An error in the CPU operation can result if this processing is performed at the same time by the one instruction.

(3) To operate the clock timer and stopwatch timer accurately, select the prescaler of the OSC1 to match the crystal oscillator used.

4.4 Input Ports (K00–K03, K10, K20–K23)

Configuration of input ports

The E0C6235 Series has nine bits (4 bits × 2 + 1 bit) general-purpose input ports. Each of the input port terminals (K00–K03, K10, K20–K23) provides internal pull-down resistor. Pull-down resistor can be selected for each bit with the mask option.
Figure 4.4.1 shows the configuration of input port.

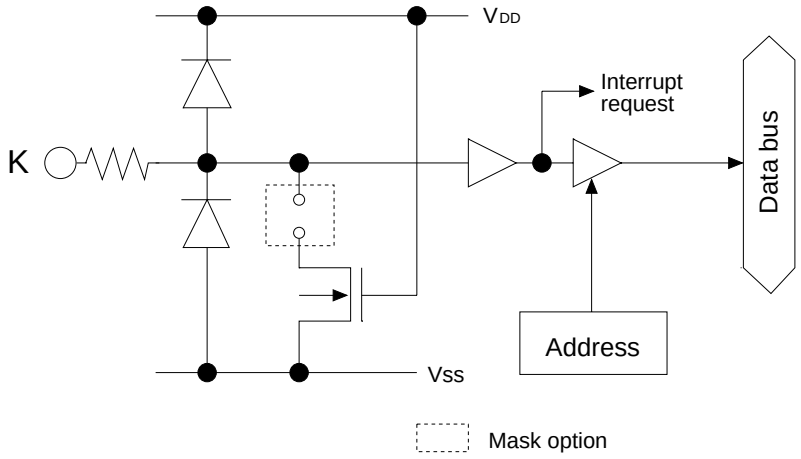


Fig. 4.4.1 Configuration of input port

Selection of "With pull-down resistor" with the mask option suits input from the push switch, key matrix, and so forth. When "Gate direct" is selected, the port can be used for slide switch input and interfacing with other LSIs.

Further, the input port terminal K02 and K03 are used as the input terminals for the event counter. (See "4.12 Event Counter" for details.)

Input comparison registers and interrupt function

All nine bits of the input ports (K00–K03, K10, K20–K23) provide the interrupt function for the five bits, K00–K03 and K10. The conditions for issuing an interrupt can be set by the software for the five bits, K00–K03 and K10. Further, whether to mask the interrupt function can be selected individually for all nine bits by the software.
Figure 4.4.2 shows the configuration of K00–K03 and K10.
Figure 4.4.4 shows the configuration of K20–K23.

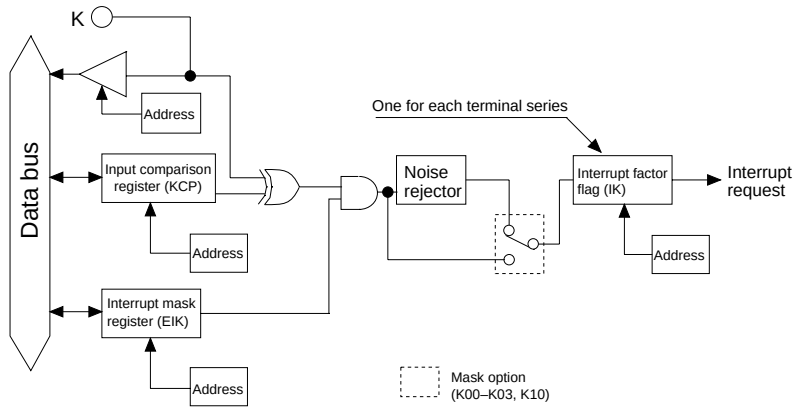


Fig. 4.4.2
Input interrupt circuit configuration (K00–K03, K10)

The input interrupt timing for K00–K03 and K10 depends on the value set for the input comparison registers (KCP00–KCP03 and KCP10). Interrupt can be selected to occur at the rising or falling edge of the input.
The interrupt mask registers (EIK00–EIK03, EIK10) enables the interrupt mask to be selected individually for K00–K03 and K10. However, whereas the interrupt function is enabled inside K00–K03, the interrupt occurs when the contents change from matching those of the input comparison register to non-matching contents. Interrupt for K10 can be generated by setting the same conditions individually.
When the interrupt is generated, the interrupt factor flag (IK0 and IK1) is set to "1".
Figure 4.4.3 shows an example of an interrupt for K00–K03.

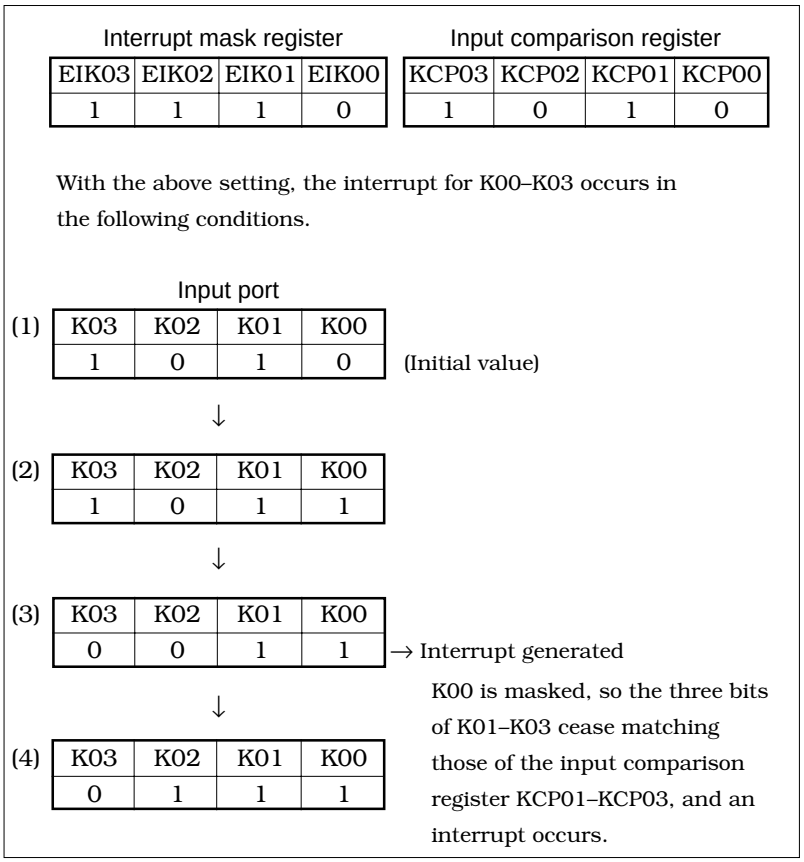


Fig. 4.4.3
Example of interrupt of K00–K03

K00 is masked by the interrupt mask register (EIK00), so that an interrupt does not occur at (2). At (3), K03 changes to "0"; the data of the terminal that is interrupt enabled no longer matches the data of the input comparison register, so that interrupt occurs. As already explained, the condition for the interrupt to occur is the change in the port data and contents of the input comparison register from matching to nonmatching. Hence, in (4), when the nonmatching status changes to another nonmatching status, an interrupt does not occur. Further, terminals that have been masked for interrupt do not affect the conditions for interrupt generation.

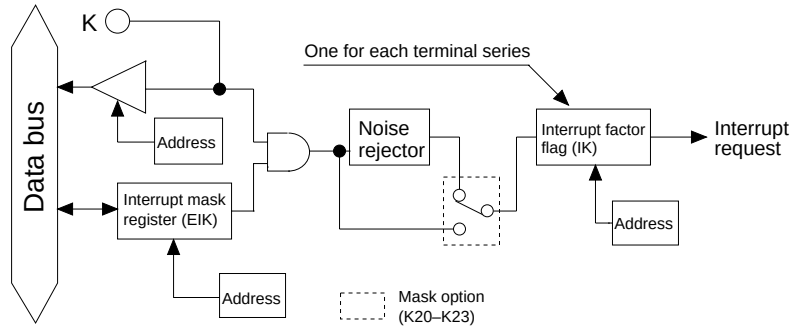


Fig. 4.4.4
Input interrupt circuit configuration (K20–K23)

There is no input comparison register for K20–K23, and interrupt is fixed to occur at th rising edge of input. The interrupt mask can be selected for each of the four terminals with the interrupt mask register (EIK20–EIK23). When all the enabled terminals are "0", interrupt occurs when one or more of the ports changed to "1".
When an interrupt occurs, the interrupt factor flag (IK2) is set to "1".
Figure 4.4.5 shows an example of an interrupt being generated for K20–K23.

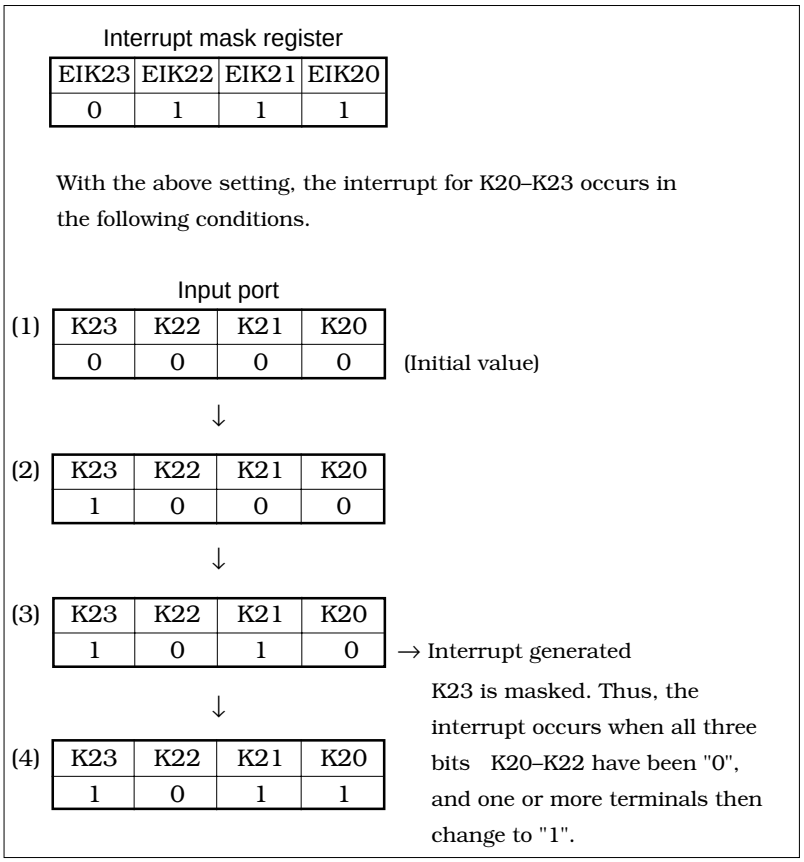


Fig. 4.4.5
Example of interrupt of K20–K23

The mask register (EIK23) masks the interrupt of K23, so an interrupt does not occur at (2). At (3), K21 becomes "1", so that an interrupt occurs if the interrupt enabled terminals were all "0" and at least one terminal then changes to "1". At (4), the conditions for interrupt are not established, so an interrupt does not occur.
Futher, terminals that have been masked for interrupt do not affect the conditions for interrupt generation.

Mask option

The contents that can be selected with the input port mask option are as follows:

(1) Internal pull-down resistor can be selected for each of the nine bits of the input ports (K00–K03, K10, K20–K23). When you have selected "Gate direct", take care that the floating status does not occur for the input. Select "With pull-down resistor" for input ports that are not being used.

(2) The input interrupt circuit contains a noise rejector for preventing interrupt occurring through noise. The mask option enables selection of whether to use the noise rejector for each separate terminal series.
When "Use" is selected, a maximum delay of 1 msec occurs from the time interrupt condition is established until the interrupt factor flag (IK) is set to "1".

Control of input ports

Table 4.4.1 lists the input ports control bits and their addresses.

Table 4.4.1 Input port control bits

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
2E3H	K03	K02	K01	K00	K03	– *2	High	Low	Input port data (K00–K03)
					K02	– *2	High	Low	
	R				K01	– *2	High	Low	
					K00	– *2	High	Low	
2E4H	KCP03	KCP02	KCP01	KCP00	KCP03	0	↓	↑	Input comparison register (K00–K03)
					KCP02	0	↓	↑	
	R/W				KCP01	0	↓	↑	
					KCP00	0	↓	↑	
2E5H	EIK03	EIK02	EIK01	EIK00	EIK03	0	Enable	Mask	Interrupt mask register (K00–K03)
					EIK02	0	Enable	Mask	
	R/W				EIK01	0	Enable	Mask	
					EIK00	0	Enable	Mask	
2E7H	SCTRG	EIK10	KCP10	K10	SCTRG*3	–	Trigger	–	Serial interface clock trigger
					EIK10	0	Enable	Mask	Interrupt mask register (K10)
	W	R/W		R	KCP10	0	↓	↑	Input comparison register (K10)
					K10	– *2	High	Low	Input port data (K10)
2EAH	IK1	IK0	SWIT1	SWIT0	IK1 *4	0	Yes	No	Interrupt factor flag (K10)
					IK0 *4	0	Yes	No	Interrupt factor flag (K00–K03)
	R				SWIT1 *4	0	Yes	No	Interrupt factor flag (stopwatch 1 Hz)
					SWIT0 *4	0	Yes	No	Interrupt factor flag (stopwatch 10 Hz)
2F3H	0	0	IK2	ISIO	0 *3	– *2	–	–	Unused
					0 *3	– *2	–	–	Unused
	R				IK2 *4	0	Yes	No	Interrupt factor flag (K20–K23)
					ISIO *4	0	Yes	No	Interrupt factor flag (serial interface)
2F4H	K23	K22	K21	K20	K23	– *2	High	Low	Input port data (K20–K23)
					K22	– *2	High	Low	
	R				K21	– *2	High	Low	
					K20	– *2	High	Low	
2F5H	EIK23	EIK22	EIK21	EIK20	EIK23	0	Enable	Mask	Interrupt mask register (K20–K23)
					EIK22	0	Enable	Mask	
	R/W				EIK21	0	Enable	Mask	
					EIK20	0	Enable	Mask	

*1 Initial value at the time of initial reset
*2 Not set in the circuit
*3 Constantly "0" when being read
*4 Reset (0) immediately after being read
*5 Undefined

K00–K03, K10, K20–K23: Input port data (2E3H, 2E7H·D0, 2F4H)

Input data of the input port terminals can be read out with these registers.

When "1" is read out : High level
When "0" is read out : Low level
Writing : Invalid

The read-out is "1" when the terminal voltage of the nine bits of the input ports (K00–K03, K10, K20–K23) goes high (V_{DD}), and "0" when the voltage goes low (V_{SS}).
These bits are dedicated for read-out, so writing cannot be done.

KCP00–KCP03, KCP10: Input comparison registers (2E4H, 2E7H·D1)

Interrupt conditions for terminals K00–K03 and K10 can be set with these registers.

When "1" is written :	Falling edge
When "0" is written :	Rising edge
Read-out:	Valid

Of the nine bits of the input ports, the interrupt conditions can be set for the rising or falling edge of input for each of the five bits (K00–K03 and K10), through the input comparison registers (KCP00–KCP03 and KCP10).
At initial reset, these registers are set to "0".

EIK00–EIK03, EIK10, EIK20–EIK23: Interrupt mask registers (2E5H, 2E7H·D2, 2F5H)

Masking the interrupt of the input port terminals can be selected with these registers.

When "1" is written :	Enable
When "0" is written :	Mask
Read-out :	Valid

With these registers, masking of the input port bits can be selected for each of the nine bits.
Writing to the interrupt mask registers can be done only in the DI status (interrupt flag = "0").
At initial reset, these registers are all set to "0".

IK0, IK1, IK2: Interrupt factor flags (2EAH·D2 and D3, 2F3H·D1)

These flags indicate the occurrence of input interrupt.

When "1" is read out :	Interrupt has occurred
When "0" is read out :	Interrupt has not occurred
Writing :	Invalid

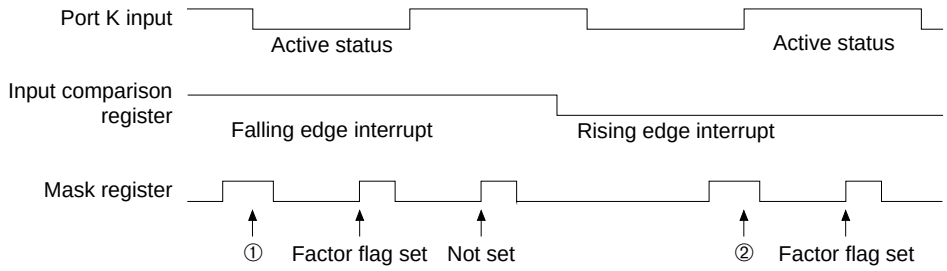
The interrupt factor flags IK0, IK1 and IK2 are associated with K00–K03, K10 and K20–K23, respectively. From the status of these flags, the software can decide whether an input interrupt has occurred.
These flags are reset when the software reads them. Read-out can be done only in the DI status (interrupt flag = "0").
At initial reset, these flags are set to "0".

Programming notes

(1) When input ports are changed from high to low by pull-down resistance, the fall of the waveform is delayed on account of the time constant of the pull-down resistance and input gate capacitance. Hence, when fetching input ports, set an appropriate wait time.
Particular care needs to be taken of the key scan during key matrix configuration. Aim for a wait time of about 1 msec.

(2) When "Use" is selected with the noise rejector mask option, a maximum delay of 1 msec occurs from time the interrupt conditions are established until the interrupt factor flag (IK) is set to "1" (until the interrupt is actually generated).
Hence, pay attention to the timing when reading out (resetting) the interrupt factor flag.
For example, when performing a key scan with the key matrix, the key scan changes the input status to set the interrupt factor flag, so it has to be read out to reset it. However, if the interrupt factor flag is read out immediately after key scanning, the delay will cause the flag to be set after read-out, so that it will not be reset.

(3) Input interrupt programing related precautions



When the content of the mask register is rewritten, while the port K input is in the active status. The input interrupt factor flags are set at ① and ②, ① being the interrupt due to the falling edge and ② the interrupt due to the rising edge.

Fig. 4.4.6
Input interrupt timing

When using an input interrupt, if you rewrite the content of the mask register, when the value of the input terminal which becomes the interrupt input is in the active status, the factor flag for input interrupt may be set.

Therefore, when using the input interrupt, the active status of the input terminal implies

input terminal = low status, when the falling edge interrupt is effected and

input terminal = high status, when the rising edge interrupt is effected.

When an interrupt is triggered at the falling edge of an input terminal, a factor flag is set with the timing of ① shown in Figure 4.4.6. However, when clearing the content of the mask register with the input terminal kept in the low status and then setting it, the factor flag of the input interrupt is again set at the timing that has been set.

Consequently, when the input terminal is in the active status (low status), do not rewrite the mask register (clearing, then setting the mask register), so that a factor flag will only set at the falling edge in this case. When clearing, then setting the mask register, set the mask register, when the input terminal is not in the active status (high status).

When an interrupt is triggered at the rising edge of the input terminal, a factor flag will be set at the timing of ② shown in Figure 4.4.6. In this case, when the mask registers cleared, then set, you should set the mask register, when the input terminal is in the low status.

In addition, when the mask register = "1" and the content of the input comparison register is rewritten in the input terminal active status, an input interrupt factor flag may be set. Thus, you should rewrite the content of the input comparison register in the mask register = "0" status.

(4) Read out the interrupt factor flag (IK) only in the DI status (interrupt flag = "0"). Read-out during EI status (interrupt flag = "1") will cause malfunction.

(5) Write the interrupt mask register (EIK) only in the DI status (interrupt flag = "0"). Writing during EI status (interrupt flag = "1") will cause malfunction.

4.5 Output Ports (R00–R03, R10–R13)

Configuration of output ports

The E0C6235 Series has eight bits (4 bits × 2) general output ports.
Output specifications of the output ports can be selected individually with the mask option. Two kinds of output specifications are available: complementary output and Pch open drain output.
Further, the mask option enables the output ports R10–R13 to be used as special output ports.
Figure 4.5.1 shows the configuration of the output ports.

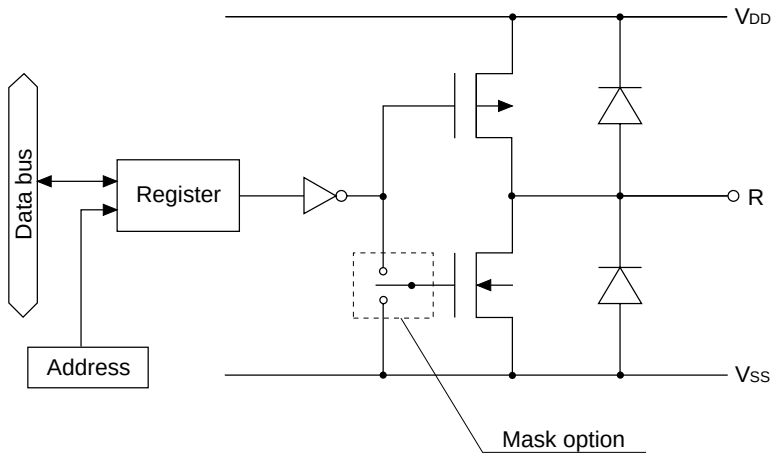


Fig. 4.5.1
Configuration of output ports

Mask option

The mask option enables the following output port selection.

(1) Output specifications of output ports

Output specifications for the output ports (R00–R03, R10–R13) enable selection of either complementary output or Pch open drain output for each of the eight bits.

However, even when Pch open drain output is selected, voltage exceeding source voltage must not be applied to the output port.

(2) Special output

In addition to the regular DC output, special output can be selected for the output ports R10–R13 as shown in Table 4.5.1. Figure 4.5.2 shows the structure of the output ports R10–R13.

Table 4.5.1 Special output

Pin name	When special output selected
R10	BZ
R13	$\overline{BZ}$ (Only when R10 = BZ output is selected)
R11	SIOF
R12	FOUT

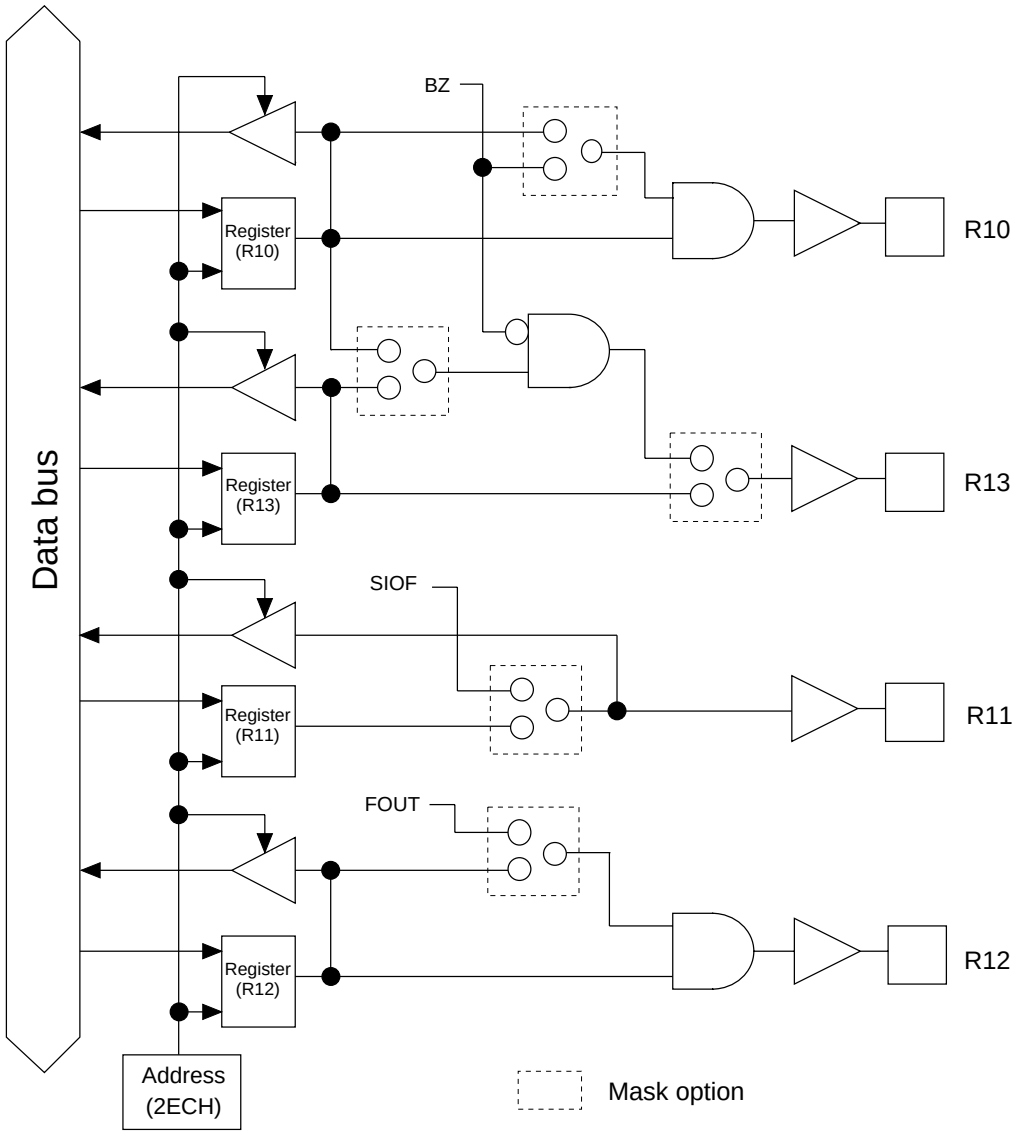


Fig. 4.5.2
Structure of output port R10–R13

BZ, $\overline{BZ}$: (R10, R13) BZ and $\overline{BZ}$ are the buzzer signal output for driving the piezoelectric buzzer. The buzzer signal is generated by demultiplicaion of f_{OSC1}. The buzzer signal frequency can be selected by software. Also, a digital envelope can be added to the buzzer signal. See "4.11 Sound Generator" for details.

Notes
- *When the BZ and $\overline{BZ}$ output signals are turned ON or OFF, a hazard can result.*
- *When DC output is set for the output port R10, the output port R13 cannot be set for $\overline{BZ}$ output.*

Figure 4.5.3 shows the output waveform for BZ and $\overline{BZ}$.

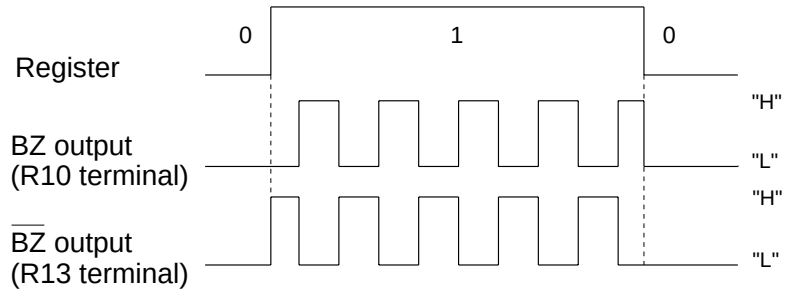


Fig. 4.5.3
Output waveform of BZ and $\overline{BZ}$

SIOF: (R11) When the output port R11 is set for SIOF output, it outputs the signal indicating the running status (RUN/STOP) of the serial interface.
See "4.7 Serial Interface" for details.

FOUT: (R12) When the output port R12 is set for FOUT output, it outputs the clock of fOSC1 or the demultiplied fOSC1. The clock frequency is selectable with the mask options, from the frequencies listed in Table 4.5.2.

Table 4.5.2
FOUT clock frequency

Setting value	Clock frequency (Hz)	
	fOSC1 = 32,768	fOSC1 = 38,400
fOSC1 / 1	32,768	38,400
fOSC1 / 2	16,384	19,200
fOSC1 / 4	8,192	9,600
fOSC1 / 8	4,096	4,800
fOSC1 / 16	2,048	2,400
fOSC1 / 32	1,024	1,200
fOSC1 / 64	512	600
fOSC1 / 128	256	300

Note A hazard may occur when the FOUT signal is turned ON or OFF.

Control of output ports

Table 4.5.3 lists the output ports' control bits and their addresses.

Table 4.5.3 Control bits of output ports

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
2EBH	R03	R02	R01	R00	R03	0	High	Low	Output port (R03)
					R02	0	High	Low	Output port (R02)
	R/W				R01	0	High	Low	Output port (R01)
					R00	0	High	Low	Output port (R00)
2ECH	R13	R12	R11 / SIOF	R10	R13	0	High/On	Low/Off	Output port (R13)/$\overline{BZ}$ output control
					R12	0	High/On	Low/Off	Output port (R12)/FOUT output control
	R/W		R/W	R/W	R11	0	High	Low	Output port (R11, LAMP)
			R		SIOF	0	Run	Stop	Output port (SIOF)
					R10	0	High/On	Low/Off	Output port (R10)/BZ output control

*1 Initial value at the time of initial reset
*2 Not set in the circuit
*3 Constantly "0" when being read
*4 Reset (0) immediately after being read
*5 Undefined

R00–R03, R10–R13 (when DC output): Output port data (2EBH, 2ECH)

Sets the output data for the output ports.

When "1" is written : High output
When "0" is written : Low output
Read-out : Valid

The output port terminals output the data written in the corresponding registers (R00–R03, R10–R13) without changing it. When "1" is written in the register, the output port terminal goes high (V_{DD}), and when "0" is written, the output port terminal goes low (V_{SS}).
At initial reset, all registers are set to "0".

R10, R13 (when BZ and $\overline{BZ}$ output is selected): Special output port data (2ECH·D0 and D3)

These bits control the output of the buzzer signals (BZ, $\overline{BZ}$).

When "1" is written :	Buzzer signal is output
When "0" is written :	Low level (DC) is output
Read-out :	Valid

$\overline{BZ}$ is output from terminal R13. With the mask option, selection can be made perform this output control by R13, or to perform output control simultaneously with BZ by R10.

- When R13 controls $\overline{BZ}$ output

  BZ output and $\overline{BZ}$ output can be controlled independently. BZ output is controlled by writing data to R10, and $\overline{BZ}$ output is controlled by writing data to R13.

- When R10 controls $\overline{BZ}$ output

  BZ output and $\overline{BZ}$ output can be controlled simultaneously by writing data to R10 only. For this case, R13 can be used as a one-bit general register having both read and write functions, and data of this register exerts no affect on $\overline{BZ}$ output (output from the R13 pin).

At initial reset, registers R10 and R13 are set to "0".

R11 (when SIOF output is selected): Special output port data (2ECH·D1)

Indicates the running status of the serial interface.

When "1" is read out :	RUN
When "0" is read out :	STOP
Writing :	Valid

See "4.7 Serial Interface" for details of SIOF.
This bit is exclusively for reading out, so data cannot be written to it.

R12 (when FOUT is selected): Special output port data (2ECH·D2)

Controls the FOUT (clock) output.

When "1" is written :	Clock output
When "0" is written :	Low level (DC) output
Read-out :	Valid

FOUT output can be controlled by writing data to R12.
At initial reset, this register is set to "0".

Programming note

When BZ, $\overline{BZ}$ and FOUT are selected with the mask option, a hazard may be observed in the output waveform when the data of the output register changes.

4.6 I/O Ports (P00–P03, P10–P13)

Configuration of I/O ports

The E0C6235 Series eight bits (4 bits × 2) has general-purpose I/O ports. Figure 4.6.1 shows the configuration of the I/O ports.
The four bits of each of the I/O ports P00–P03 and P10–P13 can be set to either input mode or output mode. Modes can be set by writing data to the I/O control register.

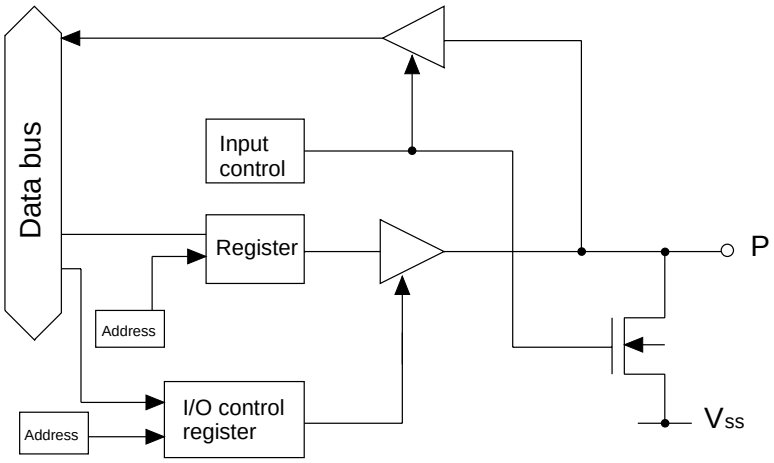


Fig. 4.6.1
Configuration of I/O ports

I/O control register and I/O mode

Input or output mode can be set for the four bits of I/O port P00–P03 and I/O port P10–P13 by writing data into the corresponding I/O control register IOC0 and IOC1.

To set the input mode, "0" is written to the I/O control register. When an I/O port is set to input mode, it becomes high impedance status and works as an input port. However, the input line is pulled down when input data is read.

The output mode is set when "1" is written to the I/O control register. When an I/O port set to output mode works as an output port, it outputs a high signal (V_{DD}) when the port output data is "1", and a low signal (V_{SS}) when the port output data is "0".

At initial reset, the I/O control registers are set to "0", and the I/O port enters the input mode.

Mask option

The output specification during output mode (IOC = "1") of these I/O ports can be set with the mask option for either complementary output or Pch open drain output. This setting can be performed for each bit of each port. However, when Pch open drain output has been selected, voltage in excess of the power voltage must not be applied to the port.

Control of I/O ports

Table 4.6.1 lists the I/O ports' control bits and their addresses.

Table 4.6.1 I/O port control bits

Address	Register								Comment
	D3	D2	D1	D0	Name	Init *1	1	0	
2EDH	P03	P02	P01	P00	P03	– *2	High	Low	I/O port data (P00–P03)
					P02	– *2	High	Low	
					P01	– *2	High	Low	Output latch reset at time of SR
	R/W				P00	– *2	High	Low	
2EEH	TMRST	SWRUN	SWRST	IOC0	TMRST*3	Reset	Reset	–	Clock timer reset
					SWRUN	0	Run	Stop	Stopwatch timer Run/Stop
	W	R/W	W	R/W	SWRST*3	Reset	Reset	–	Stopwatch timer reset
					IOC0	0	Output	Input	I/O control register 0 (P00–P03)
2FDH	P13	P12	P11	P10	P13	– *2	High	Low	I/O port data (P10–P13)
					P12	– *2	High	Low	
					P11	– *2	High	Low	Output latch reset at time of SR
	R/W				P10	– *2	High	Low	
2FEH	PRSM	CLKCHG	OSCC	IOC1	PRSM	0	38 kHz	32 kHz	OSC1 prescaler selection
					CLKCHG	0	OSC3	OSC1	CPU clock switch
					OSCC	0	On	Off	OSC3 oscillation On/Off
	R/W				IOC1	0	Output	Input	I/O control register 1 (P10–P13)

*1 Initial value at the time of initial reset
*2 Not set in the circuit
*3 Constantly "0" when being read
*4 Reset (0) immediately after being read
*5 Undefined

P00–P03, P10–P13: I/O port data (2EDH, 2FDH)

I/O port data can be read and output data can be set through these ports.

- When writing data

  When "1" is written : High level
  When "0" is written : Low level

  When an I/O port is set to the output mode, the written data is output unchanged from the I/O port terminal. When "1" is written as the port data, the port terminal goes high (V_{DD}), and when "0" is written, the level goes low (V_{SS}).
  Port data can be written also in the input mode.

- When reading data out

  When "1" is read out : High level
  When "0" is read out : Low level

  The terminal voltage level of the I/O port is read out. When the I/O port is in the input mode the voltage level being input to the port terminal can be read out; in the output mode the output voltage level can be read. When the terminal voltage is high (V_{DD}) the port data that can be read is "1", and when the terminal voltage is low (V_{SS}) the data is "0".
  Further, the built-in pull-down resistance goes ON during read-out, so that the I/O port terminal is pulled down.

Notes

- *When the I/O port is set to the output mode and a low-impedance load is connected to the port terminal, the data written to the register may differ from the data read out.*
- *When the I/O port is set to the input mode and a low-level voltage (V_{SS}) is input, erroneous input results if the time constant of the capacitive load of the input line and the built-in pull-down resistance load is greater than the read-out time. When the input data is being read out, the time that the input line is pulled down is equivalent to 1.5 cycles of the CPU system clock. However, the electric potential of the terminals must be settled within 0.5 cycles. If this condition cannot be fulfilled, some measure must be devised such as arranging pull-down resistance externally, or performing multiple read-outs.*

IOC0, IOC1: I/O control registers (2EEH·D0, 2FEH·D0)

The input and output modes of the I/O ports can be set with these registers.

When "1" is written :	Output mode
When "0" is written :	Input mode
Read-out :	Valid

The input and output modes of the I/O ports are set in units of four bits. IOC0 sets the mode for P00–P03, and IOC1 sets the mode for P10–P13.
Writing "1" to the I/O control register makes the corresponding I/O port enter the output mode, and writing "0" induces the input mode.
At initial reset, these two registers are set to "0", so the I/O ports are in the input mode.

Programming notes

(1) When input data are changed from high to low by built-in pull-down resistance, the fall of the waveform is delayed on account of the time constant of the pull-down resistance and input gate capacitance. Consequently, if data is read out while the CPU is running in the OSC3 oscillation circuit, data must be read out continuously for about 500 µsec.

(2) When the I/O port is set to the output mode and the data register has been read, the terminal data instead of the register data can be read out. Because of this, if a low-impedance load is connected and read-out performed, the value of the register and the read-out result may differ.

4.7 Serial Interface (SIN, SOUT, SCLK)

Configuration of serial interface

The E0C6235 has a synchronous clock type 8 bits serial interface built-in.
The configuration of the serial interface is shown in Figure 4.7.1.
The CPU, via the 8 bits shift register, can read the serial input data from the SIN terminal. Moreover, via the same 8 bits shift register, it can convert parallel data to serial data and output it to the SOUT terminal.
The synchronous clock for serial data input/output may be set by selecting by software any one of 3 types of master mode (internal clock mode: when the E0C6235 is to be the master for serial input/output) and a type of slave mode (external clock mode: when the E0C6235 is to be the slave for serial input/output).
Also, when the serial interface is used at slave mode, SIOF signal which indicates whether or not the serial interface is available to transmit or receive can be output to output port R11 by mask option.

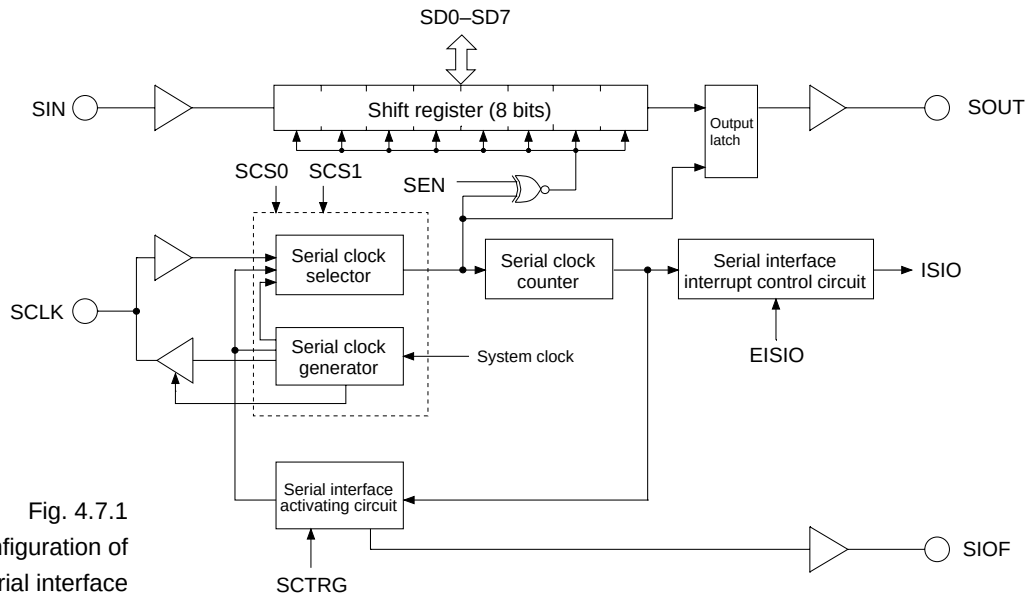


Fig. 4.7.1
Configuration of serial interface

Master mode and slave mode of serial interface

The serial interface of the E0C6235 has two types of operation mode: master mode and slave mode.
In the master mode, it uses an internal clock as synchronous clock of the built-in shift register, generates this internal clock at the SCLK terminal and controls the external (slave side) serial device.
In the slave mode, the synchronous clock output from the external (master side) serial device is input from the SCLK terminal and uses it as the synchronous clock to the built-in shift register.
The master mode and slave mode are selected by writing data to registers SCS1 and SCS0 (address 2F2H·D2, D3).
When the master mode is selected, a synchronous clock may be selected from among 3 types as shown in Table 4.7.1.

Table 4.7.1
Synchronous clock selection

SCS1	SCS0	Mode	Synchronous clock
0	0	Master mode	CLK
0	1		CLK/2
1	0		CLK/4
1	1	Slave mode	External clock

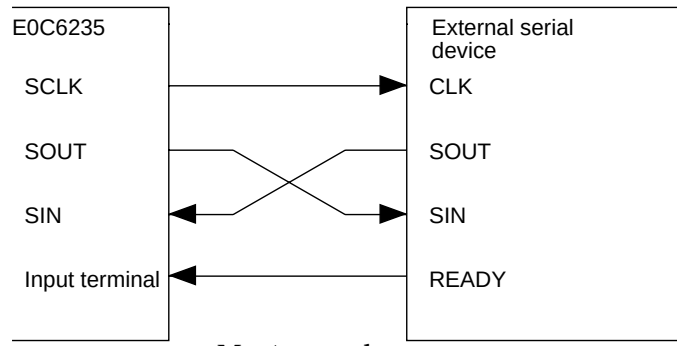
CLK : CPU system clock

At initial reset, the slave mode (external clock mode) is selected.
Moreover, the synchronous clock, along with the input /output of the 8 bits serial data, is controlled as follows:

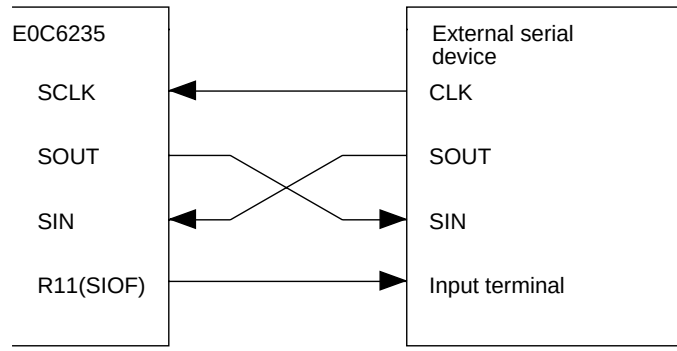
- At master mode, after output of 8 clocks from the SCLK terminal, clock output is automatically suspended and SCLK terminal is fixed at low level.
- At slave mode, after input of 8 clocks to the SCLK terminal, subsequent clock inputs are masked.

Note *When using the serial interface in the master mode, CPU system clock is used as the synchronous clock. Accordingly, when the serial interface is operating, system clock switching ($f_{OSC1} \leftrightarrow f_{OSC3}$) should not be performed.*

A sample basic serial input/output portion connection is shown in Figure 4.7.2.



a. Master mode



b. Slave mode

Fig. 4.7.2
Sample basic connection of serial input/output section

Data input/output and interrupt function

The serial interface of E0C6235 can input/output data via the internal 8 bits shift register. The shift register operates by synchronizing with either the synchronous clock output from SCLK terminal (master mode), or the synchronous clock input to SCLK (slave mode).
The serial interface generates interrupt on completion of the 8 bits serial data input/output. Detection of serial data input/output is done by the counting of the synchronous clock (SCLK); the clock completes input/output operation when 8 counts (equivalent to 8 cycles) have been made and then generates interrupt.
The serial data input/output procedure data is explained below:

(1) Serial data output procedure and interrupt

The E0C6235 serial interface is capable of outputting parallel data as serial data, in units of 8 bits.
By setting the parallel data to 4 bits registers SD0–SD3 (address 2F0H) and SD4–SD7 (address 2F1H) individually and writing "1" to SCTRG bit (address 2E7H·D3), it synchronizes with the synchronous clock and serial data is output at the SOUT terminal. The synchronous clock used here is as follows: in the master mode, internal clock which is output to the SCLK terminal while in the slave mode, external clock which is input from the SCLK terminal. The serial output of the SOUT termina changes with the rising edge of the clock that is input or output from the SCLK terminal.
The serial data to the built-in shift register is shifted with the rising edge of the SCLK signal when SE2 bit (address 2F2H·D1) is "1" and is shifted with the falling edge of the SCLK signal when SE2 bit (address 2F2H·D1) is "0".
When the output of the 8 bits data from SD0 to SD7 is completed, the interrupt factor flag ISIO (address 2F3H·D0) is set to "1" and interrupt is generated. Moreover, the interrupt can be masked by the interrupt mask register EISIO (address 2F2H·D0).

(2) Serial data input procedure and interrupt

The E0C6235 serial interface is capable of inputting serial data as parallel data, in units of 8 bits.
The serial data is input from the SIN terminal, synchronizes with the synchronous clock, and is sequentially read in the 8 bits shift register. As in the above item (1), the synchronous clock used here is as follows: in the master mode, internal clock which is output to the SCLK terminal while in the slave mode, external clock which is input from the SCLK terminal.
The serial data to the built-in shift register is read with the rising edge of the SCLK signal when SE2 bit is "1" and is read with the falling edge of the SCLK signal when SE2 bit is "0". Moreover, the shift register is sequentially shifted as the data is fetched.

When the input of the 8 bits data from SD0 to SD7 is completed, the interrupt factor flag ISIO is set to "1" and interrupt is generated. Moreover, the interrupt can be masked by the interrupt mask register EISIO. Note, however, that regardless of the setting of the interrupt mask register, the interrupt factor flag is set to "1" after input of the 8 bits data.

The data input in the shift register can be read from data registers SD0–SD7 by software.

(3) Serial data input/output permutation

E0C6235 allows the input/output permutation of serial data to be selected by mask option as to either LSB first or MSB first. The block diagram showing input/output permutation in case of LSB first and MSB first is provided in Figure 4.7.3.

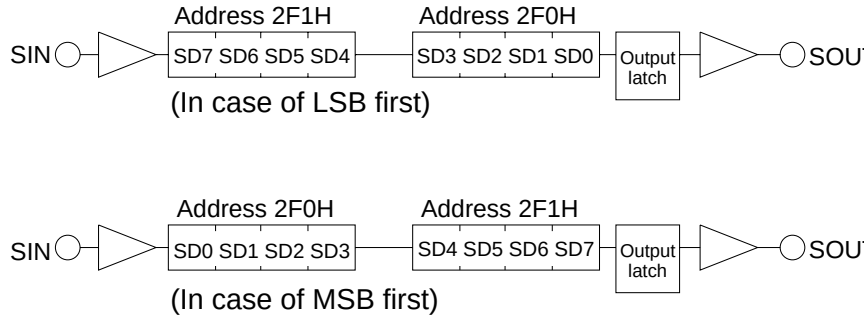


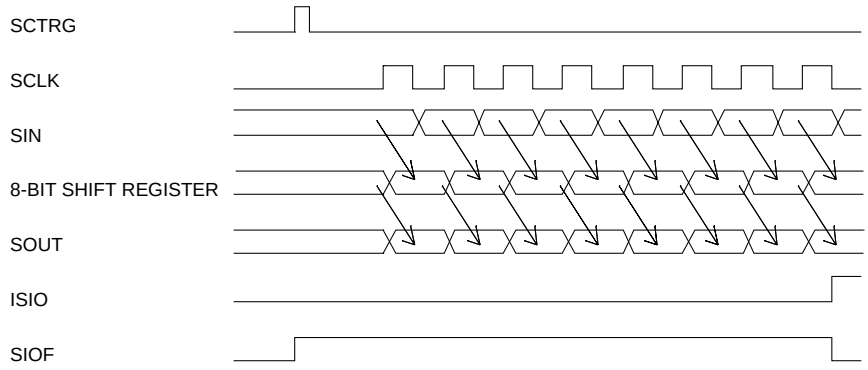
Fig. 4.7.3
Serial data input/output permutation

(4) SIOF signal

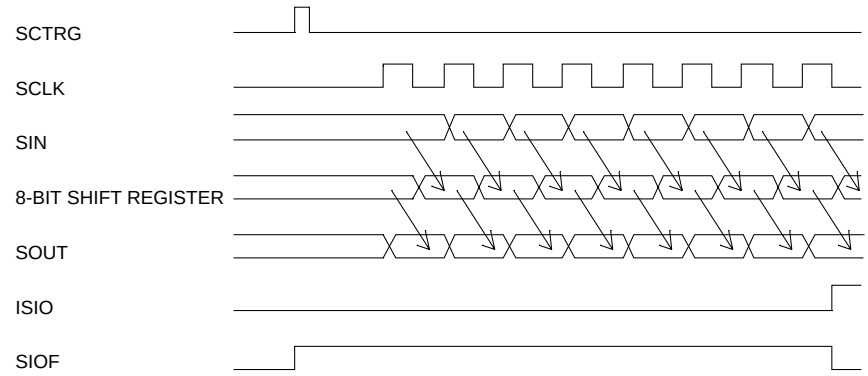
When the E0C6235 serial interface is used in the slave mode (external clock mode), SIOF is used to indicate whether the internal serial interface is available to transmit or receive data for the master side (external) serial device. SIOF signal is generated from output port R11 by mask option.
SIOF signal becomes "1" (high) when the E0C6235 serial interface becomes available to transmit or receive data; normally, it is at "0" (low).
SIOF signal changes from "0" to "1" immediately after "1" is written to SCTRG and returns from "1" to "0" when eight synchronous clock has been counted.

(5) Timing chart

The E0C6235 serial interface timing chart is shown in Figure 4.7.4.



a. Timing chart, SE2 = "1"



b. Timing chart, SE2 = "0"

Fig. 4.7.4
Serial interface timing chart

Mask option

The serial interface may be selected for the following by mask option.

(1) Whether or not the SIN terminal will use built-in pull down resistor may be selected.
If the use of no pull down resistor is selected, take care that floating state does not occur at the SIN terminal. When the SIN terminal is not used, the use of pull down resistor should be selected.

(2) Either complementary output or P channel (Pch) open drain as output specification for the SOUT terminal may be selected.
However, even if Pch open drain has been selected, application of voltage exceeding power source voltage to the SOUT terminal will be prohibited.

(3) Whether or not the SCLK terminal will use pull down resistor which is turned ON during input mode (external clock) may be selected.
If the use of no pull down resistor is selected, take care that floating state does not occur at the SCLK terminal during input mode.
Normally, the use of pull down resistor should be selected.

(4) As output specification during output mode, either complementary output or P channel (Pch) open drain output may be selected for the SCLK terminal.

(5) Positive or negative logic can be selected for the signal logic of the SCLK pin (SCLK or $\overline{\text{SCLK}}$).
However, keep in mind that only pull-down resistance can be set for the input mode (pull-up resistance is not built-in).

(6) LSB first or MSB first as input/output permutation of serial data may be selected.

(7) Output port R11 may be assigned as SIOF output terminal which will indicate whether the serial interface is available to transmit or receive signals.

Control of serial interface

The control registers for the serial interface are explained below.

Table 4.7.2 Control registers of serial interface

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
2F0H	SD3	SD2	SD1	SD0	SD3	× *5			Serial interface data register (low-order 4 bits)
					SD2	× *5			
	R/W				SD1	× *5			
					SD0	× *5			
2F1H	SD7	SD6	SD5	SD4	SD7	× *5			Serial interface data register (high-order 4 bits)
					SD6	× *5			
	R/W				SD5	× *5			
					SD4	× *5			
2F2H	SCS1	SCS0	SE2	EISIO	SCS1	1			SIF clock mode [SCS1, 0] 0 Clock; 1 CLK; 2 CLK/2; 3 CLK/4; slave
					SCS0	1			selection register
	R/W				SE2	0	↑	↓	SIF clock edge selection register
					EISIO	0	Enable	Mask	Interrupt mask register (serial interface)
2F3H	0	0	IK2	ISIO	0 *3	– *2	–	–	Unused
					0 *3	– *2	–	–	Unused
	R				IK2 *4	0	Yes	No	Interrupt factor flag (K20–K23)
					ISIO *4	0	Yes	No	Interrupt factor flag (serial interface)
2E7H	SCTRG	EIK10	KCP10	K10	SCTRG*3	–	Trigger	–	Serial interface clock trigger
					EIK10	0	Enable	Mask	Interrupt mask register (K10)
	W	R/W		R	KCP10	0	↓	↑	Input comparison register (K10)
					K10	– *2	High	Low	Input port data (K10)
2ECH	R13	R12	R11	R10	R13	0	High/On	Low/Off	Output port (R13)/$\overline{BZ}$ output control
			SIOF		R12	0	High/On	Low/Off	Output port (R12)/FOUT output control
					R11	0	High	Low	Output port (R11, LAMP)
	R/W		R/W	R/W	SIOF	0	Run	Stop	Output port (SIOF)
			R		R10	0	High/On	Low/Off	Output port (R10)/BZ output control

*1 Initial value at the time of initial reset
*2 Not set in the circuit
*3 Constantly "0" when being read
*4 Reset (0) immediately after being read
*5 Undefined

SD0–SD3, SD4–SD7: Serial interface data registers (2F0H, 2F1H)

These registers are used for writing and reading serial data.

- During writing operation

When "1" is written : High level
When "0" is written : Low level

Writes serial data will be output to SOUT terminal. From the SOUT terminal, the data converted to serial data as high (V_{DD}) level bit for bits set at "1" and as low (V_{SS}) level bit for bits set at "0".

- During reading operation

When "1" is read out : High level
When "0" is read out : Low level

The serial data input from the SIN terminal can be read by this register.
The data converted to parallel data, as high (V_{DD}) level bit "1" and as low (V_{SS}) level bit "0" input from SIN terminal.
Perform data reading only while the serial interface is halted (i.e., the synchronous clock is neither being input or output).

At initial reset, these registers will be undefined.

SCS1, SCS0: Clock mode selection register (2F2H·D3, D2)

Selects the synchronous clock for the serial interface (SCLK).

Table 4.7.3 Synchronous clock selection

SCS1	SCS0	Mode	Synchronous clock
0	0	Master mode	CLK
0	1		CLK/2
1	0		CLK/4
1	1	Slave mode	External clock

CLK : CPU system clock

Synchronous clock (SCLK) is selected from among the above 4 types: 3 types of internal clock and external clock.
At initial reset, external clock is selected.

SE2: Clock edge selection register (2F2H·D1)

Selects the timing for reading in the serial data input.

When "1" is written :	Rising edge of SCLK
When "0" is written :	Falling edge of SCLK
Read-out :	Valid

Selects whether the fetching for the serial input data to registers (SD0–SD7) at the rising edge (at "1" writing) or falling edge (at "0" writing) of the SCLK signal.
Pay attention if the synchtonous clock goes into reverse phase (SCLK → $\overline{\text{SCLK}}$) through the mask option.

SCLK rising = $\overline{\text{SCLK}}$ falling, SCLK falling = $\overline{\text{SCLK}}$ rising

When the internal clock is selected as the synchronous clock (SCLK), a hazard occurs in the synchronous clock (SCLK) when data is written to register SE2.
The input data fetching timing may be selected but output timing for output data is fixed at SCLK rising edge.
At initial reset, falling edge of SCLK (SE2 = "0") is selected.

EISIO: Interrupt mask register (2F2H·D0)

This is the interrupt mask register of the serial interface.

When "1" is written :	Enabled
When "0" is written :	Masked
Read-out :	Valid

At initial reset, this register is set to "0" (mask).

ISIO: Interrupt factor flag (2F3H·D0)

This is the interrupt factor flag of the serial interface.

When "1" is read out :	Interrupt has occurred
When "0" is read out :	Interrupt has not occurred
Writing :	Invalid

From the status of this flag, the software can decide whether the serial interface interrupt.
The interrupt factor flag is reset when it has been read out.
Note, however, that even if the interrupt is masked, this flag will be set to "1" after the 8 bits data input/output.

Be sure that the interrupt factor flag reading is done with the interrupt in the DI status (interrupt flag = "0").
At initial reset, this flag is set to "0".

SCTRG: Clock trigger (2E7H·D3)

This is a trigger to start input/output of synchronous clock.

When "1" is written :	Trigger
When "0" is written :	No operation
Read-out :	Always "0"

When this trigger is supplied to the serial interface activating circuit, the synchronous clock (SCLK) input/output is started.
As a trigger condition, it is required that data writing or reading on data registers SD0–SD7 be performed prior to writing "1" to SCTRG. (The internal circuit of the serial interface is initiated through data writing/reading on data registers SD0–SD7.)
Supply trigger only once every time the serial interface is placed in the RUN state. Refrain from perfoming trigger input multiple times, as leads to malfunctioning.
Moreover, when the synchronous clock SCLK is external clock, start to input the external clock after the trigger.

SIOF: Special output port data (2ECH·D1)

Indicates the running status of the serial interface.

When "1" is read out :	RUN status
When "0" is read out :	STOP status
Writing :	Invalid

The RUN status is indicated from immediatery after "1" is written to SCTRG bit through to the end of serial data input/output.

Programming notes

(1) If the bit data of SE2 changes while SCLK is in the master mode, a hazard will be output to the SCLK pin. If this poses a problem for the system, be sure to set the SCLK to the external clock if the bit data of SE2 is to be changed.

(2) Be sure that read-out of the interrupt factor flag (ISIO) is done only when the serial port is in the STOP status (SIOF = "0") and the DI status (interrupt flag = "0"). If read-out is performed while the serial data is in the RUN status (during input or output), the data input or output will be suspended and the initial status resumed. Read-out during the EI status (interrupt flag = "1") causes malfunctioning.

(3) When using the serial interface in the master mode, the synchronous clock uses the CPU system clock. Accordingly, do not change the system clock ($f_{OSC1} \leftrightarrow f_{OSC3}$) while the serial interface is operating.

(4) Perform data writing/reading to data registers SD0–SD7 only while the serial interface is halted (i.e., the synchronous clock is neither being input or output).

(5) As a trigger condition, it is required that data writing or reading on data registers SD0–SD7 be performed prior to writing "1" to SCTRG. (The internal circuit of the serial interface is initiated through data writing/reading on data registers SD0–SD7.) Supply trigger only once every time the serial interface is placed in the RUN state. Moreover, when the synchronous clock SCLK is external clock, start to input the external clock after the trigger.

(6) Be sure that writing to the interrupt mask register is done only in the DI status (interrupt flag = "0"). Writing to the interrupt mask register while in the EI status (interrupt flag = "1") may cause malfunction.

4.8 LCD Driver (COM0–COM3, SEG0–SEG47)

Configuration of LCD driver

The E0C6235 Series has four common terminals and 48 segment terminals, so that it can drive an LCD with a maximum of 192 (48 × 4) segments.
The power for driving the LCD is generated by the CPU internal circuit so that there is no need to apply power especially from outside.
The driving method is 1/4 duty (or 1/3 duty with the mask option) dynamic drive depending on the four types of potential, V_{DD}, V_{L1}, V_{L2} and V_{L3}. The frame frequency is f_{OSC1}/1,024 Hz for 1/4 duty, and f_{OSC1}/768 Hz for 1/3 duty.

Figure 4.8.1 shows the drive waveform for 1/4 duty, and Figure 4.8.2 shows the drive waveform for 1/3 duty.

Note *f_{OSC1} indicates the oscillation frequency of the OSC1 oscillation circuit.*

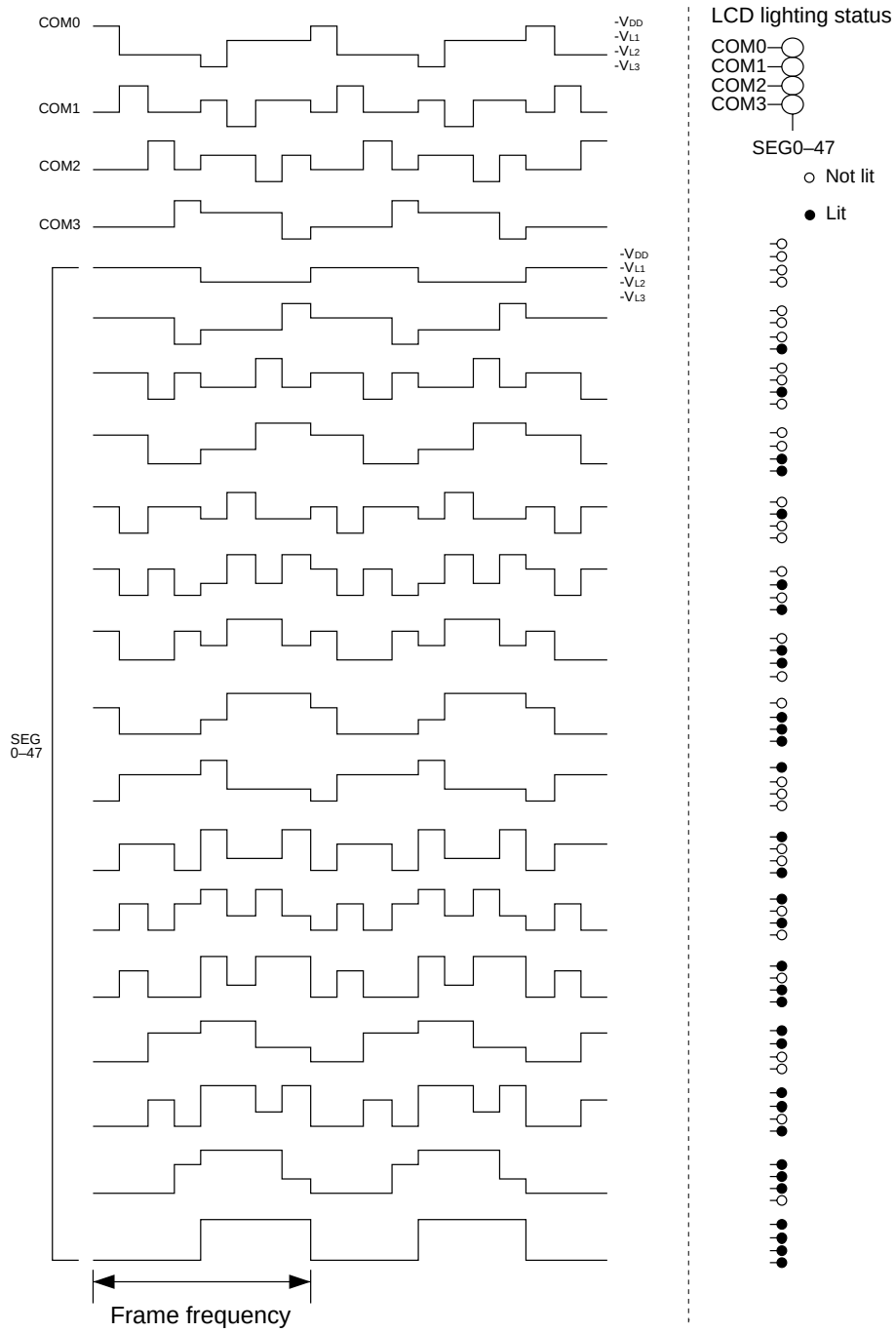


Fig. 4.8.1
Drive waveform for 1/4 duty

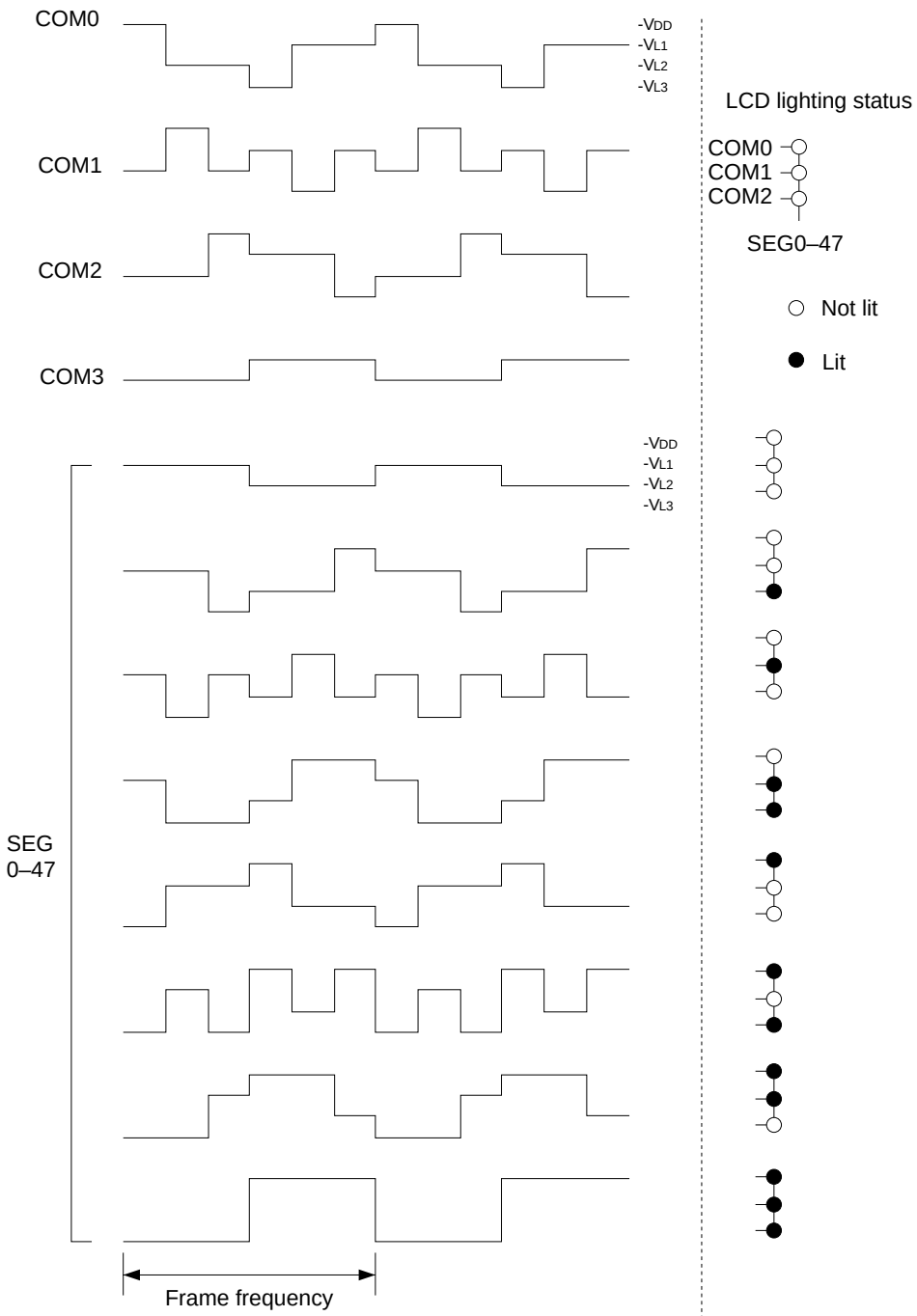


Fig. 4.8.2
Drive waveform for 1/3 duty

Switching between dynamic and static drive

The E0C6235 Series provides software setting of the LCD static drive. This function enables easy adjustment (cadence adjustment) of the oscillation frequency of the OSC1 oscillation circuit (crystal oscillation circuit).

The procedure for executing static drive of the LCD is as follows:

① Write "1" to register CSDC at address 2E8H·D3.

② Write the same value to all registers corresponding to COM0–COM3 of the display memory.

Notes
- *Even when 1/3 duty is selected, COM3 is valid for static drive. However, the output frequency is the same as for the frame frequency.*
- *For cadence adjustment, set the segment data so that all the LCDs light.*

Figure 4.8.3 shows the drive waveform for static drive.

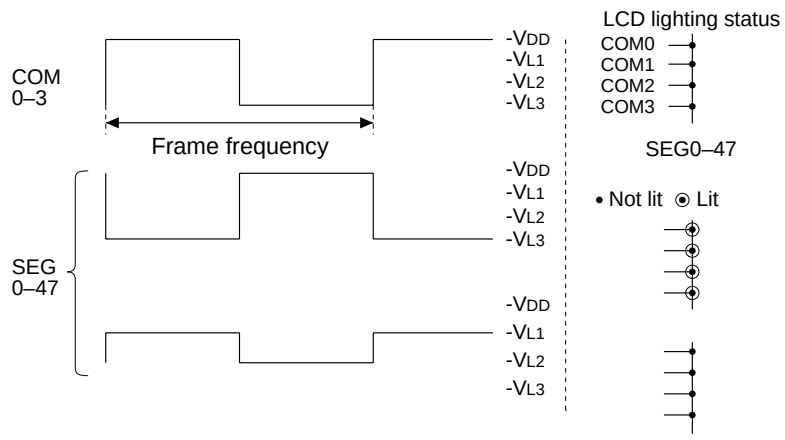


Fig. 4.8.3
LCD static drive waveform

Mask option (segment allocation)

(1) Segment allocation

As shown in Figure 4.1.1(c), segment data of the E0C6235 Series is decided depending on display data written to the display memory (write-only) at address 040H–06FH (page 0) or 240H–26FH (page 2).

① The mask option enables the display memory to be allocated entirely to either page 0 or page 2.

② The address and bits of the display memory can be made to correspond to the segment terminals (SEG0–SEG47) in any form through the mask option. This makes design easy by increasing the degree of freedom with which the liquid crystal panel can be designed.

Figure 4.8.4 shows an example of the relationship between the LCD segments (on the panel) and the display memory (when page 0 is selected) for the case of 1/3 duty.

Address	Data			
	D3	D2	D1	D0
06AH	d	c	b	a
06BH	p	g	f	e
06CH	d'	c'	b'	a'
06DH	p'	g'	f'	e'

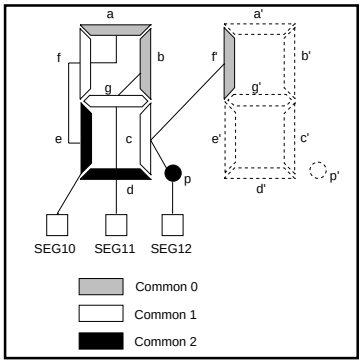
Segment data memory allocation

→

	Common 0	Common 1	Common 2
SEG10	6A, D0 (a)	6B, D1 (f)	6B, D0 (e)
SEG11	6A, D1 (b)	6B, D2 (g)	6A, D3 (d)
SEG12	6D, D1 (f')	6A, D2 (c)	6B, D3 (p)

Terminal address allocation

↑



Example of LCD panel

Fig. 4.8.4
Segment allocation

(2) Drive duty

With the mask option, either 1/4 or 1/3 duty can be selected for the LCD drive duty.
Table 4.8.1 shows the differences in the number of segments depending on the selected duty.

Table 4.8.1 Differences depending on selected duty

Duty	Terminals used in common	Maximum number of segments	Frame frequency (when f_{OSC1} = 32 kHz)
1/4	COM0–3	192 (48 × 4)	f_{OSC1}/1,024 (32 Hz)
1/3	COM0–2	144 (48 × 3)	f_{OSC1}/768 (42.7 Hz)

(3) Output specification

① The segment terminals (SEG0–SEG47) are selected with the mask option in pairs for either segment signal output or DC output (V_{DD} and V_{SS} binary output). When DC output is selected, the data corresponding to COM0 of each segment terminal is output.

② When DC output is selected, either complementary output or Pch open drain output can be selected for each terminal with the mask option.

*Note The terminal pairs are the combination of SEG2*n and SEG2*n + 1 (where n is an integer from 0 to 23).*

Control of LCD driver

Table 4.8.2 shows the LCD driver's control bits and their addresses. Figure 4.8.5 shows the display memory map.

Table 4.8.2 Control bits of LCD driver

Address	Register								Comment
	D3	D2	D1	D0	Name	Init *1	1	0	
2E8H	CSDC	ETI2	ETI8	ETI32	CSDC	0	Static	Dynamic	LCD drive switch
					ETI2	0	Enable	Mask	Interrupt mask register (clock timer 2 Hz)
					ETI8	0	Enable	Mask	Interrupt mask register (clock timer 8 Hz)
	R/W				ETI32	0	Enable	Mask	Interrupt mask register (clock timer 32 Hz)

*1 Initial value at the time of initial reset
*2 Not set in the circuit
*3 Constantly "0" when being read
*4 Reset (0) immediately after being read
*5 Undefined

Address / Page	Low / High	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0 or 2	4	Display memory (48 words x 4 bits) 0 page = R/W 2 page = W															
	5																
	6																

Fig. 4.8.5
Display memory map

CSDC: LCD drive switch (2E8H·D3)

The LCD drive format can be selected with this switch.

When "1" is written :	Static drive
When "0" is written :	Dynamic drive
Read-out :	Valid

At initial reset, dynamic drive (CSDC = "0") is selected.

Display memory: (040H–06FH or 240H–26FH)

The LCD segments are lit or turned off depending on this data.

When "1" is written :	Lit
When "0" is written :	Not lit
Read-out :	Valid for 0 page
	Undefined 2 page

By writing data into the display memory allocated to the LCD segment (on the panel), the segment can be lit or put out.
At initial reset, the contents of the display memory are undefined.

Programming notes

(1) When page 0 is selected for the display memory, the memory data and the display will not match until the area is initialized (through, for instance, memory clear processing by the CPU). Initialize the display memory by executing initial processing.

(2) When page 2 is selected for the display memory, that area becomes write-only. Consequently, data cannot be rewritten by arithmetic operations (such as AND, OR, ADD, SUB).

4.9 Clock Timer

Configuration of clock timer

The E0C6235 Series has a built-in clock timer as the source oscillator for prescaler. The clock timer is configured of a seven-bit binary counter that serves as the input clock, a 256 Hz signal output by the prescaler. Data of the four high-order bits (16 Hz–2 Hz) can be read out by the software. Figure 4.9.1 is the block diagram for the clock timer.

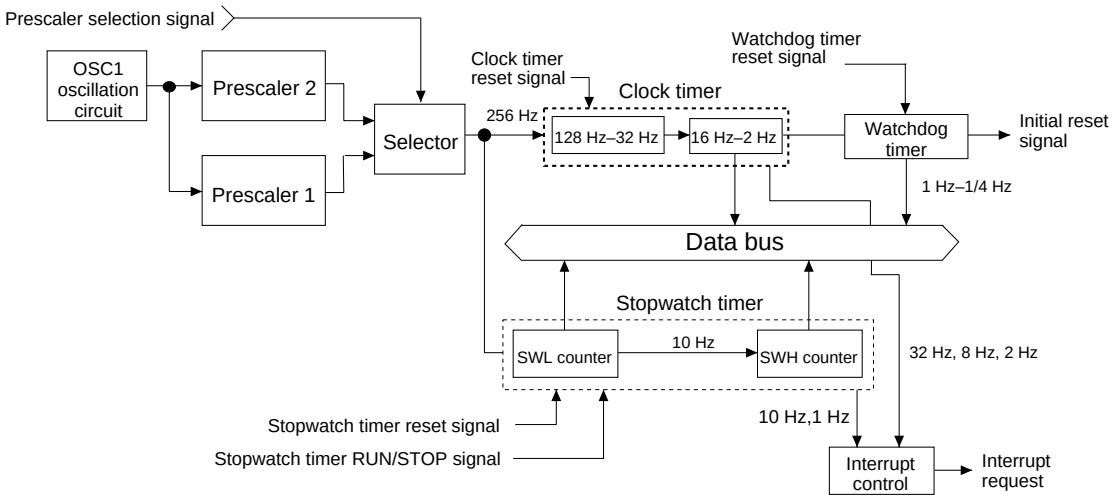


Fig. 4.9.1
Block diagram of clock timer

Ordinarily, this clock timer is used for all types of timing functions such as clocks.
The input clock of the clock timer is output through the prescaler, so the prescaler mode must be set correctly to suit the crystal oscillator to be used (32.768 kHz or 38.4 kHz). For how to set the prescaler, see "Control of oscillation circuit and prescaler".

Interrupt function

The clock timer can cause interrupts at the falling edge of 32 Hz, 8 Hz and 2 Hz signals. Software can set whether to mask any of these frequencies.
Figure 4.9.2 is the timing chart of the clock timer.

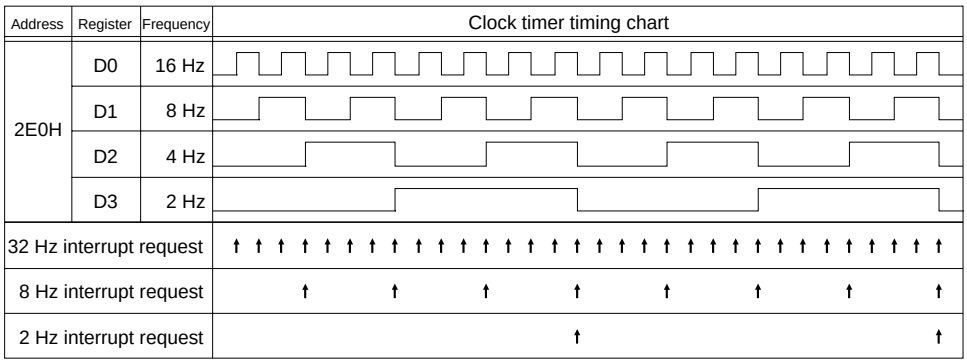


Fig. 4.9.2
Timing chart of
clock timer

As shown in Figure 4.9.2, interrupt is generated at the falling edge of the frequencies (32 Hz, 8 Hz , 2 Hz). At this time, the corresponding interrupt factor flag (TI32, TI8, TI2) is set to "1". Selection of whether to mask the separate interrupts can be made with the interrupt mask registers (ETI32, ETI8, ETI2). However, regardless of the interrupt mask register setting, the interrupt factor flag is set to "1" at the falling edge of the corresponding signal.

Control of clock timer

Table 4.9.1 shows the clock timer control bits and their addresses.

Table 4.9.1 Control bits of clock timer

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
2E0H	TM3	TM2	TM1	TM0	TM3	0			Timer data (clock timer 2 Hz)
					TM2	0			Timer data (clock timer 4 Hz)
					TM1	0			Timer data (clock timer 8 Hz)
	R				TM0	0			Timer data (clock timer 16 Hz)
2E8H	CSDC	ETI2	ETI8	ETI32	CSDC	0	Static	Dynamic	LCD drive switch
					ETI2	0	Enable	Mask	Interrupt mask register (clock timer 2 Hz)
					ETI8	0	Enable	Mask	Interrupt mask register (clock timer 8 Hz)
	R/W				ETI32	0	Enable	Mask	Interrupt mask register (clock timer 32 Hz)
2E9H	0	TI2	TI8	TI32	0 *3	– *2	–	–	Unused
					TI2 *4	0	Yes	No	Interrupt factor flag (clock timer 2 Hz)
					TI8 *4	0	Yes	No	Interrupt factor flag (clock timer 8 Hz)
	R				TI32 *4	0	Yes	No	Interrupt factor flag (clock timer 32 Hz)
2EEH	TMRST	SWRUN	SWRST	IOC0	TMRST*3	Reset	Reset	–	Clock timer reset
					SWRUN	0	Run	Stop	Stopwatch timer Run/Stop
					SWRST*3	Reset	Reset	–	Stopwatch timer reset
	W	R/W	W	R/W	IOC0	0	Output	Input	I/O control register 0 (P00–P03)

*1 Initial value at the time of initial reset
*2 Not set in the circuit
*3 Constantly "0" when being read
*4 Reset (0) immediately after being read
*5 Undefined

TM0–TM3: Timer data (2E0H)

The 16 Hz–2 Hz timer data of the clock timer can be read out with this register. These four bits are read-out only, and writing operations are invalid.
At initial reset, the timer data is initialized to "0H".

ETI32, ETI8, ETI2: Interrupt mask registers (2E8H·D0–D2)

These registers are used to select whether to mask the clock timer interrupt.

When "1" is written : Enabled
When "0" is written : Masked
Read-out : Valid

The interrupt mask registers (ETI32, ETI8, ETI2) are used to select whether to mask the interrupt to the separate frequencies (32 Hz, 8 Hz, 2 Hz).
Writing to the interrupt mask registers can be done only in the DI status (interrupt flag = "0").
At initial reset, these registers are all set to "0".

TI32, TI8, TI2: Interrupt factor flags (2E9H·D0–D2)

These flags indicate the status of the clock timer interrupt.

When "1" is read out :	Interrupt has occurred
When "0" is read out :	Interrupt has not occurred
Writing :	Invalid

The interrupt factor flags (TI32, TI8, TI2) correspond to the clock timer interrupts of the respective frequencies (32 Hz, 8 Hz, 2 Hz). The software can judge from these flags whether there is a clock timer interrupt. However, even if the interrupt is masked, the flags are set to "1" at the falling edge of the signal.
These flags can be reset through being read out by the software. Also, the flags can be read out only in the DI status (interrupt flag = "0").
At initial reset, these flags are set to "0".

TMRST: Clock timer reset (2EEH·D3)

This bit resets the clock timer.

When "1" is written :	Clock timer reset
When "0" is written :	No operation
Read-out :	Always "0"

The clock timer is reset by writing "1" to TMRST. The clock timer starts immediately after this. No operation results when "0" is written to TMRST.
This bit is write-only, and so is always "0" at read-out.

Programming notes

(1) The prescaler mode must be set correctly to suit the crystal oscillator to be used.

(2) When the clock timer has been reset, the interrupt factor flag (TI) may sometimes be set to "1". Consequently, perform flag read-out (reset the flag) as necessary at reset.

(3) The input clock of the watchdog timer is the 2 Hz signal of the clock timer, so that the watchdog timer may be counted up at timer reset.

(4) Read-out the interrupt factor flag (TI) only during the DI status (interrupt flag = "0"). Read-out during EI status (interrupt flag = "1") will cause malfunction.

4.10 Stopwatch Timer

Configuration of stopwatch timer

The E0C6235 Series incorporates a 1/100 sec and 1/10 sec stopwatch timer. The stopwatch timer is configured of a two-stage, four-bit BCD counter serving as the input clock of an approximately 100 Hz signal (signal obtained by approximately demultiplying the 256 Hz signal output by the prescaler). Data can be read out four bits at a time by the software.
Figure 4.10.1 is the block diagram of the stopwatch timer.

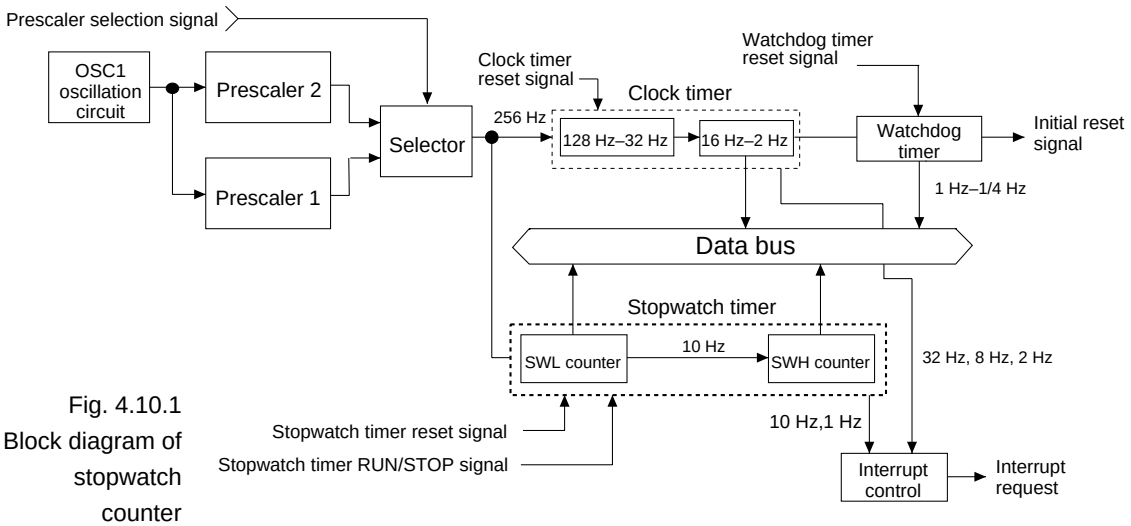


Fig. 4.10.1
Block diagram of stopwatch counter

The stopwatch timer can be used as a separate timer from the clock timer. In particular, digital watch stopwatch functions can be realized easily with software.
The input clock of the stopwatch timer is output through the prescaler, so the prescaler mode must be set correctly to suit the crystal oscillator to be used (32.768 kHz or 38.4 kHz). For how to set the prescaler, see "Control of oscillation circuit and prescaler".

Count-up pattern

The stopwatch timer is configured of four-bit BCD counters SWL and SWH.
The counter SWL, at the stage preceding the stopwatch timer, has an approximated 100 Hz signal for the input clock. It counts up every 1/100 sec, and generates an approximated 10 Hz signal. The counter SWH has an approximated 10 Hz signal generated by the counter SWL for the input clock. It count-up every 1/10 sec, and generated 1 Hz signal.
Figure 4.10.2 shows the count-up pattern of the stopwatch timer.

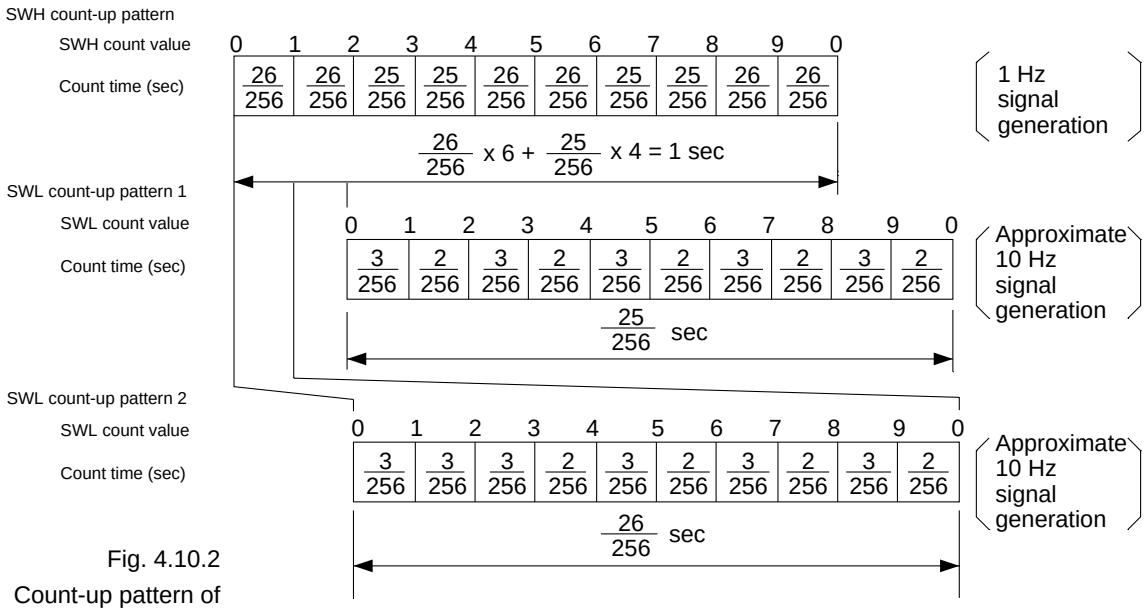


Fig. 4.10.2
Count-up pattern of stopwatch timer

SWL generates an approximated 10 Hz signal from the basic 256 Hz signal. The count-up intervals are 2/256 sec and 3/256 sec, so that finally two patterns are generated: 25/256 sec and 26/256 sec intervals. Consequently, these patterns do not amount to an accurate 1/100 sec.
SWH counts the approximated 10 Hz signals generated by the 25/256 sec and 26/256 sec intervals in the ratio of 4:6, to generate a 1 Hz signal. The count-up intervals are 25/256 sec and 26/256 sec, which do not amount to an accurate 1/10 sec.

Interrupt function

The 10 Hz (approximate 10 Hz) and 1 Hz interrupts can be generated through the overflow of stopwatch timers SWL and SWH respectively. Also, software can set whether to separately mask the frequencies described earlier.
Figure 4.10.3 is the timing chart for the stopwatch timer.

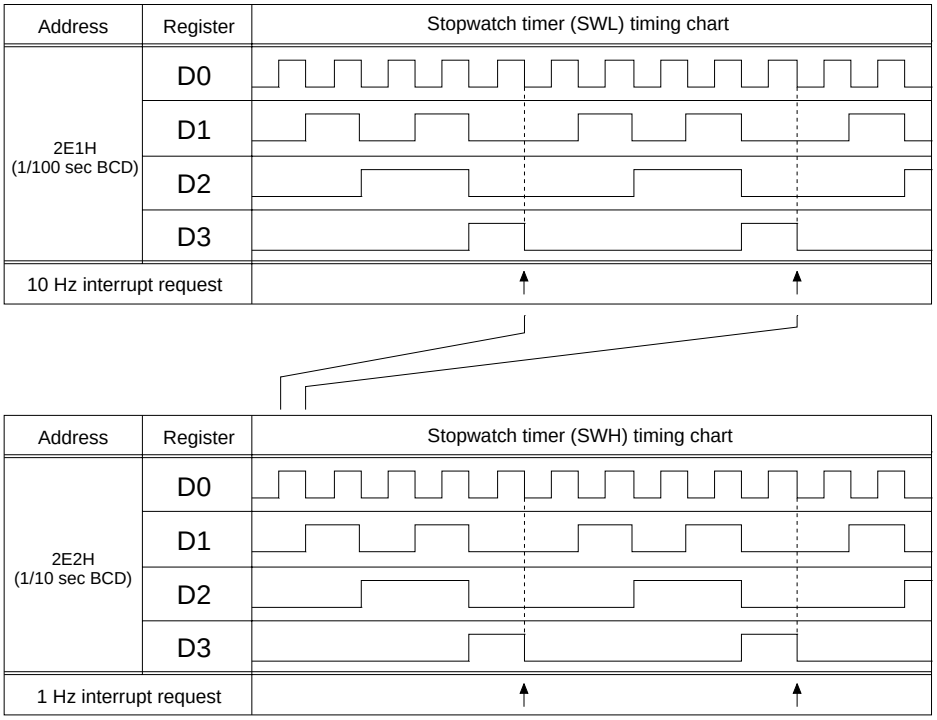


Fig. 4.10.3
Timing chart for stopwatch timer

As shown in Figure 4.10.3, the interrupts are generated by the overflow of their respective counters ("9" changing to "0"). Also, at this time the corresponding interrupt factor flags (SWIT0, SWIT1) are set to "1".
The respective interrupts can be masked separately through the interrupt mask registers (EISWIT0, EISWIT1). However, regardless of the setting of the interrupt mask registers, the interrupt factor flags are set to "1" by the overflow of their corresponding counters.

Control of stopwatch timer

Table 4.10.1 lists the stopwatch timer control bits and their addresses.

Table 4.10.1 Stopwatch timer control bits

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
2E1H	SWL3	SWL2	SWL1	SWL0	SWL3	0			MSB
					SWL2	0			Stopwatch timer data 1/100 sec (BCD)
	R				SWL1	0			
					SWL0	0			LSB
2E2H	SWH3	SWH2	SWH1	SWH0	SWH3	0			MSB
					SWH2	0			Stopwatch timer data 1/10 sec (BCD)
					SWH1	0			
					SWH0	0			LSB
2E6H	HLMOD	BLD0	EISWIT1	EISWIT0	HLMOD	0	Heavy load	Normal	Heavy load protection mode register
					BLD0	0	Low	Normal	Sub-BLD evaluation data
	R/W	R	R/W		EISWIT1	0	Enable	Mask	Interrupt mask register (stopwatch 1 Hz)
					EISWIT0	0	Enable	Mask	Interrupt mask register (stopwatch 10 Hz)
2EAH	IK1	IK0	SWIT1	SWIT0	IK1 *4	0	Yes	No	Interrupt factor flag (K10)
					IK0 *4	0	Yes	No	Interrupt factor flag (K00–K03)
	R				SWIT1 *4	0	Yes	No	Interrupt factor flag (stopwatch 1 Hz)
					SWIT0 *4	0	Yes	No	Interrupt factor flag (stopwatch 10 Hz)
2EEH	TMRST	SWRUN	SWRST	IOC0	TMRST*3	Reset	Reset	–	Clock timer reset
					SWRUN	0	Run	Stop	Stopwatch timer Run/Stop
	W	R/W	W	R/W	SWRST*3	Reset	Reset	–	Stopwatch timer reset
					IOC0	0	Output	Input	I/O control register 0 (P00–P03)

*1 Initial value at the time of initial reset
*2 Not set in the circuit
*3 Constantly "0" when being read
*4 Reset (0) immediately after being read
*5 Undefined

SWL0–SWL3: Stopwatch timer 1/100 sec (2E1H)

Data (BCD) of the 1/100 sec column of the stopwatch timer can be read out. These four bits are read-only, and cannot be used for writing operations.
At initial reset, the timer data is set to "0H".

SWH0–SWH3: Stopwatch timer 1/10 sec (2E2H)

Data (BCD) of the 1/10 sec column of the stopwatch timer can be read out. These four bits are read-only, and cannot be used for writing operations.
At initial reset, the timer data is set to "0H".

EISWIT0, EISWIT1: Interrupt mask register (2E6H·D0 and D1)

These registers are used to select whether to mask the stopwatch timer interrupt.

When "1" is written :	Enabled
When "0" is written :	Masked
Read-out :	Valid

The interrupt mask registers (EISWIT0, EISWIT1) are used to separately select whether to mask the 10 Hz and 1 Hz interrupts.
At initial reset, these registers are both set to "0".

SWIT0, SWIT1: Interrupt factor flag (2EAH·D0 and D1)

These flags indicate the status of the stopwatch timer interrupt.

When "1" is read out :	Interrupt has occurred
When "0" is read out :	Interrupt has not occurred
Writing :	Invalid

The interrupt factor flags (SWIT0, SWIT1) correspond to the 10 Hz and 1 Hz interrupts respectively. With these flags, the software can judge whether a stopwatch timer interrupt has occurred. However, regardless of the interrupt mask register setting, these flags are set to "1" by the counter overflow.
These flags are reset when read out by the software. Also, read-out is only possible in the DI status (interrupt flag = "0").
At initial reset, these flags are set to "0".

SWRST: Stopwatch timer reset (2EEH·D1)

This bit resets the stopwatch timer.

When "1" is written :	Stopwatch timer reset
When "0" is written :	No operation
Read-out :	Always "0"

The stopwatch timer is reset when "1" is written to SWRST. When the stopwatch timer is reset in the RUN status, operation restarts immediately. Also, in the STOP status the reset data is maintained.
This bit is write-only, and is always "0" at read-out.

SWRUN: Stopwatch timer RUN/STOP (2EEH·D2)

This bit controls RUN/STOP of the stopwatch timer.

When "1" is written :	RUN
When "0" is written :	STOP
Read-out :	Valid

The stopwatch timer enters the RUN status when "1" is written to SWRUN, and the STOP status when "0" is written. In the STOP status, the timer data is maintained until the next RUN status or resets timer. Also, when the STOP status changes to the RUN status, the data that was maintained can be used for resuming the count.
When the timer data is read out in the RUN status, correct read-out may be impossible because of the carry from the low-order bit (SWL) to the high-order bit (SWH). This occurs when read-out has extended over the SWL and SWH bits when the carry occurs. To prevent this, perform read out after entering the STOP status, and then return to the RUN status. Also, the duration of the STOP status must be within 976 µsec (256 Hz 1/4 cycle).
At initial reset, this register is set to "0".

Programming notes

(1) The prescaler mode must be set correctly so that the stopwatch timer suits the crystal oscillator to be used.

(2) If timer data is read out in the RUN status, the timer must be made into the STOP status, and after data is read out the RUN status can be restored. If data is read out when a carry occurs, the data cannot be read correctly.
Also, the processing above must be performed within the STOP interval of 976 µsec (256 Hz 1/4 cycle).

(3) Read-out of the interrupt factor flag (SWIT) must be done only in the DI status (interrupt flag = "0").
Read-out during EI status (interrupt flag = "1") will cause malfunction.

4.11 Sound Generator

Configuration of sound generator

The E0C6235 Series outputs buzzer signals (BZ, $\overline{BZ}$) to drive the piezoelectric buzzer.
The frequency of the buzzer signal is software-selectable from eight kinds of demultiplied f_{OSC1}. Further, a digital envelope can be added to the buzzer signal through duty ratio control.
Figure 4.11.1 shows the sound generator configuration.
Figure 4.11.2 shows the sound generator timing chart.

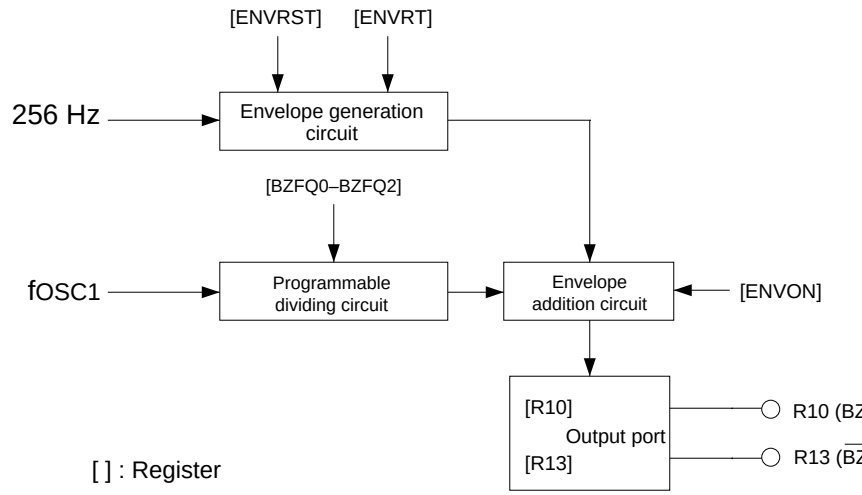


Fig. 4.11.1 Configuration of sound generator

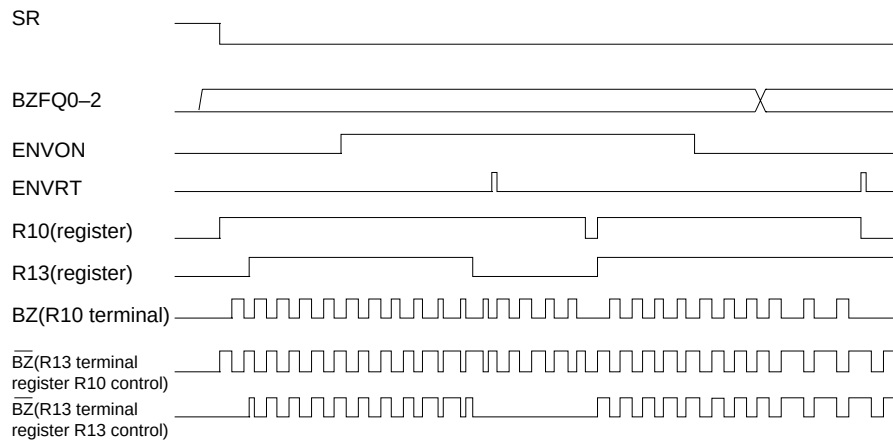


Fig. 4.11.2 Timing chart of sound generator

Frequency setting

The frequencies of the buzzer signals (BZ, $\overline{BZ}$) are set by writing data to registers BZFQ0–BZFQ2.
Table 4.11.1 lists the register setting values and the frequencies that can be set.

Table 4.11.1 Setting of frequencies of buzzer signals

BZFQ			Set frequecy (Hz)		
2	1	0	Demultiplier ratio	When f_{OSC1} = 32 kHz	When f_{OSC1} = 38.4 kHz
0	0	0	$f_{OSC1}/8$	4,096.0	4,800.0
0	0	1	$f_{OSC1}/10$	3,276.8	3,840.0
0	1	0	$f_{OSC1}/12$	2,730.7	3,200.0
0	1	1	$f_{OSC1}/14$	2,340.6	2,742.9
1	0	0	$f_{OSC1}/16$	2,048.0	2,400.0
1	0	1	$f_{OSC1}/20$	1,638.4	1,920.0
1	1	0	$f_{OSC1}/24$	1,365.3	1,600.0
1	1	1	$f_{OSC1}/28$	1,170.3	1,371.4

Note A hazard may be observed in the output waveform of the BZ and $\overline{BZ}$ signals when data of the buzzer frequency selection registers (BZFQ0–BZFQ2) changes.

Digital envelope

A duty ratio control data envelope (with duty ratio change in eight stages) can be added to the buzzer signal (BZ, $\overline{BZ}$). The duty ratio is the ratio of the pulse width compared with the pulse cycle. The BZ output is TH/ (TH+TL) when the high level output is TH and the low level output is TL. The $\overline{BZ}$ output (BZ inverted output) is TL/ (TH+TL). Also, care must be taken because the duty ratio differs depending on the buzzer frequency.

The envelope is added by writing "1" to register ENVON. If "0" is written the duty ratio is fixed to the maximum. Also, if the envelope is added, the duty ratio is reverted to the maximum by writing "1" in register ENVRST, and the duty ratio also becomes the maximum at the start of the buzzer signal output.

The decay time of the envelope (time for the duty ratio to change) can be selected with the register ENVRT. This time is 62.5 msec (16 Hz) when "0" is written, and 125 msec (8 Hz) when "1" is written. However, a maximum difference of 4 msec is taken from envelope-ON until the first change.

Table 4.11.2 lists the duty rates and buzzer frequencies.

Figure 4.11.3 shows the digital envelope timing chart.

Table 4.11.2
Duty rates and buzzer frequencies

BZFQ (register)	2	0	1	0	1	0	1	0	1
	1	0	0	0	0	1	1	1	1
Duty rate	0	0	0	1	1	0	0	1	1
Level 1 (max.)		8 / 16		8 / 20		12 / 24		12 / 28	
Level 2		7 / 16		7 / 20		11 / 24		11 / 28	
Level 3		6 / 16		6 / 20		10 / 24		10 / 28	
Level 4		5 / 16		5 / 20		9 / 24		9 / 28	
Level 5		4 / 16		4 / 20		8 / 24		8 / 28	
Level 6		3 / 16		3 / 20		7 / 24		7 / 28	
Level 7		2 / 16		2 / 20		6 / 24		6 / 28	
Level 8 (min.)		1 / 16		1 / 20		5 / 24		5 / 28	

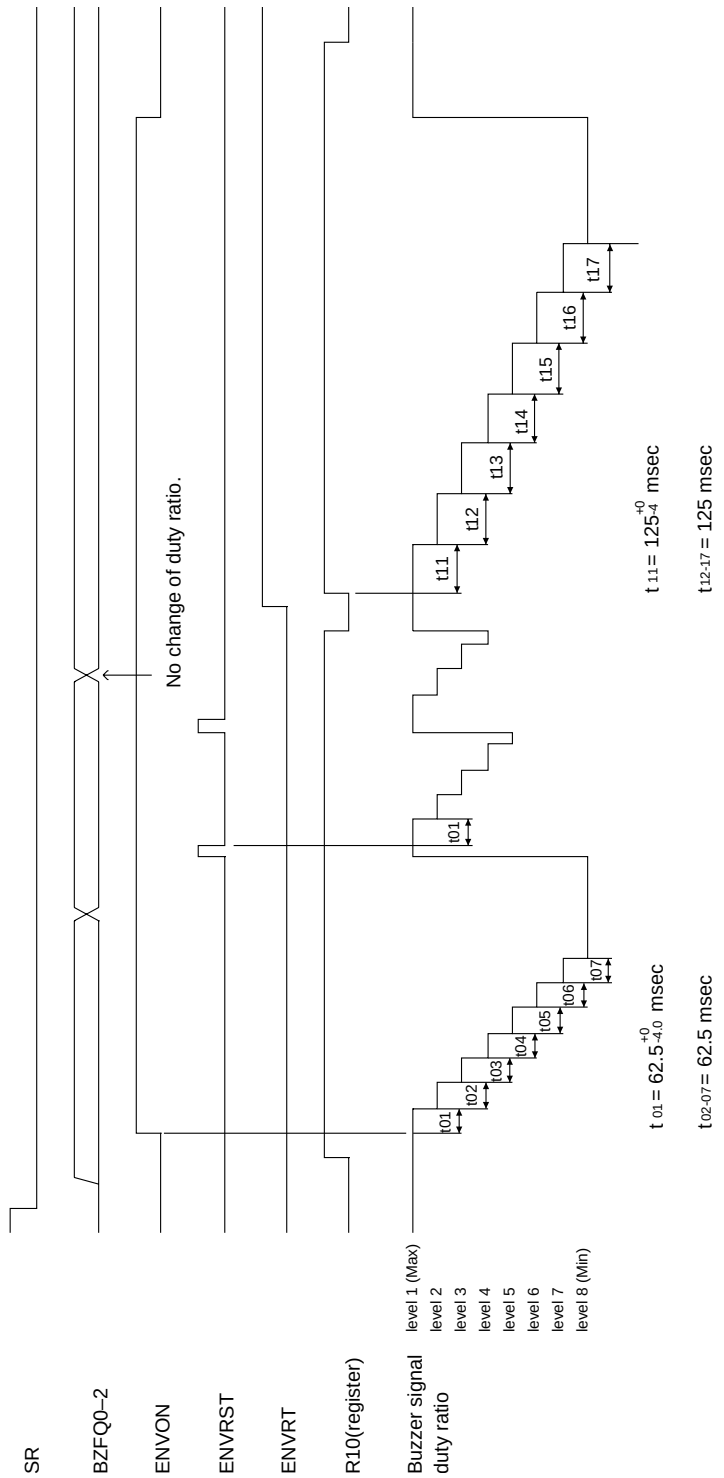


Fig. 4.11.3 Digital envelop timing chart

Mask option

(1) Selection can be made whether to output the BZ signal from the R10 pin.

(2) Selection can be made whether to output the $\overline{BZ}$ signal from the R13 pin. However, if the BZ signal is not output the $\overline{BZ}$ signal cannot be output.

(3) Selection can be made to perform the $\overline{BZ}$ signal output control through register R10 or register R13.

See "4.5 Output Ports" for details of the above mask option.

Control of sound generator

Table 4.11.3 lists the sound generator's control bits and their addresses.

Table 4.11.3 Control bits of sound generator

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
2ECH	R13	R12	R11 / SIOF	R10	R13	0	High/On	Low/Off	Output port (R13)/$\overline{BZ}$ output control
					R12	0	High/On	Low/Off	Output port (R12)/FOUT output control
					R11	0	High	Low	Output port (R11, LAMP)
	R/W		R/W / R	R/W	SIOF	0	Run	Stop	Output port (SIOF)
					R10	0	High/On	Low/Off	Output port (R10)/BZ output control
2F6H	BZFQ2	BZFQ1	BZFQ0	ENVRST	BZFQ2	0			Buzzer frequency selection [BZFQ2–0]: 0 Frequency $f_{OSC1}/8$; 1 $f_{OSC1}/10$; 2 $f_{OSC1}/12$; 3 $f_{OSC1}/14$; 4 $f_{OSC1}/16$; 5 $f_{OSC1}/20$; 6 $f_{OSC1}/24$; 7 $f_{OSC1}/28$
					BZFQ1	0			
	R/W			W	BZFQ0	0			
					ENVRST*3	Reset	Reset	–	Envelope reset
2F7H	ENVON	ENVRT	AMPDT	AMPON	ENVON	0	On	Off	Envelope On/Off
					ENVRT	0	1.0 sec	0.5 sec	Envelope cycle selection register
	R/W		R	R/W	AMPDT	1	+ > -	+ < -	Analog comparator data
					AMPON	0	On	Off	Analog comparator On/Off

*1 Initial value at the time of initial reset
*2 Not set in the circuit
*3 Constantly "0" when being read
*4 Reset (0) immediately after being read
*5 Undefined

BZFQ0–BZFQ2: Buzzer frequency selection register (2F6H·D1–D3)

This is used to select the frequency of the buzzer signal.

Table 4.11.4 Buzzer frequency

BZFQ2	BZFQ1	BZFQ0	Buzzer frequency (Hz)
0	0	0	f_{OSC1} / 8
0	0	1	f_{OSC1} / 10
0	1	0	f_{OSC1} / 12
0	1	1	f_{OSC1} / 14
1	0	0	f_{OSC1} / 16
1	0	1	f_{OSC1} / 20
1	1	0	f_{OSC1} / 24
1	1	1	f_{OSC1} / 28

Buzzer frequency is selected from the above eight types that have been divided by f_{OSC1} (oscillation frequency of the OSC1 oscillation circuit).
At initial reset, $f_{OSC1}/8$ (Hz) is selected.

ENVRST: Envelope reset (2F6H·D0)

This is the reset input to make the duty ratio of the buzzer signal the maximum.

When "1" is written :	Reset input
When "0" is written :	No operation
Read-out :	Always "0"

When the envelope is added to the buzzer signal, the duty ratio is made maximum through this reset input. When the envelope is not added or when the buzzer signal is not output, the reset input is invalid.

ENVON: Envelope ON/OFF (2F7H·D3)

This controls adding the envelope to the buzzer signal.

When "1" is written :	Envelope added (ON)
When "0" is written :	No envelope (OFF)
Read-out :	Valid

The envelope is the digital envelope based on duty ratio control. When there is no envelope, the duty ratio is fixed to the maximum.
At initial reset, no envelope (OFF) is selected.

ENVRT: Envelope decay time (2F7H·D2)

This input selects the decay time of the envelope added to the buzzer signal.

When "1" is written :	1.0 sec (125 msec × 7 = 875 msec)
When "0" is written :	0.5 sec (62.5 msec × 7 = 437.5 msec)
Read-out :	Valid

The decay time of the digital envelope is decided by the time taken for the duty ratio to change. When "1" is written to ENVRT the time is 125 msec (8 Hz) units, and when "0" is written it is 62.5 msec (16 Hz) units.
At initial reset, 0.5 sec (437.5 msec) is selected.

R10, R13 (at BZ, $\overline{BZ}$ output selection): Special output port data (2ECH·D0, D3)

These control output of the buzzer signals (BZ, $\overline{BZ}$).

When "1" is written :	Buzzer signal output
When "0" is written :	Low level (DC) output
Read-out :	Valid

- $\overline{BZ}$ output under R13 control
  BZ output and $\overline{BZ}$ output can be controlled independently. BZ output is controlled by writing data to register R10.
  $\overline{BZ}$ output is controlled by writing data to register R13.

- $\overline{BZ}$ output under R10 control
  By writing data to register R10 only, BZ output and $\overline{BZ}$ output can be controlled simultaneously. In this case, register R13 can be used as a read/write one-bit general register. This register does not affect $\overline{BZ}$ output (output to pin R13).

At initial reset, registers R10 and R13 are set to "0".

Programming note

A hazard may be observed in the output waveform of the BZ and $\overline{BZ}$ signals when data of the output registers (R10, R13) and the buzzer frequency selection registers (BZFQ0–BZFQ2) changes.

4.12 Event Counter

Configuration of event counter

The E0C6235 Series has an event counter that counts the clock signals input from outside.
The event counter is configured of a pair of eight-bit binary counters (UP counters). The clock pulses are input through terminals K02 and K03 of the input port.
The clock signals input from the terminals are input to the event counter via the noise rejector.
The event counter detects the phases of the two clock signals. Software selection provides for two modes, the phase detection mode in which one of the counters can be chosen to input the clock signal, and the separate mode in which each clock signal is input to different counters.
Figure 4.12.1 shows the configuration of the event counter.

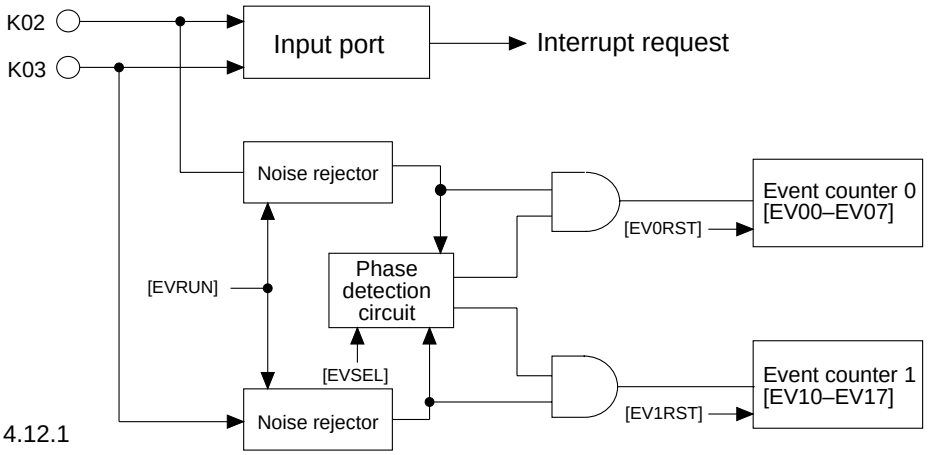


Fig. 4.12.1 Configuration of event counter

Switching count mode

The event counter detects the phases of the two clock signals. Software selection provides for two modes, the phase detection mode in which one of the counters can be chosen to input the clock signal, and the separate mode in which each clock signal is input to different counters.
Selection can be made by writing data to the EVSEL register. When "0" is written the phase detection mode is enabled, and when "1" is written the separate mode is enabled.
In the phase detection mode, the clock signals having different phases must be input simultaneously to terminals K02 and K03. When the input from terminal K02 is fast the clock signal is input to event counter 1, and when the input from terminal K03 is fast the clock signal is input to event counter 0.
In the separate mode, input from terminal K02 is made to event counter 0, and input from terminal K03 is made to event counter 1.
Figure 4.12.2 is the timing chart for the event counter.

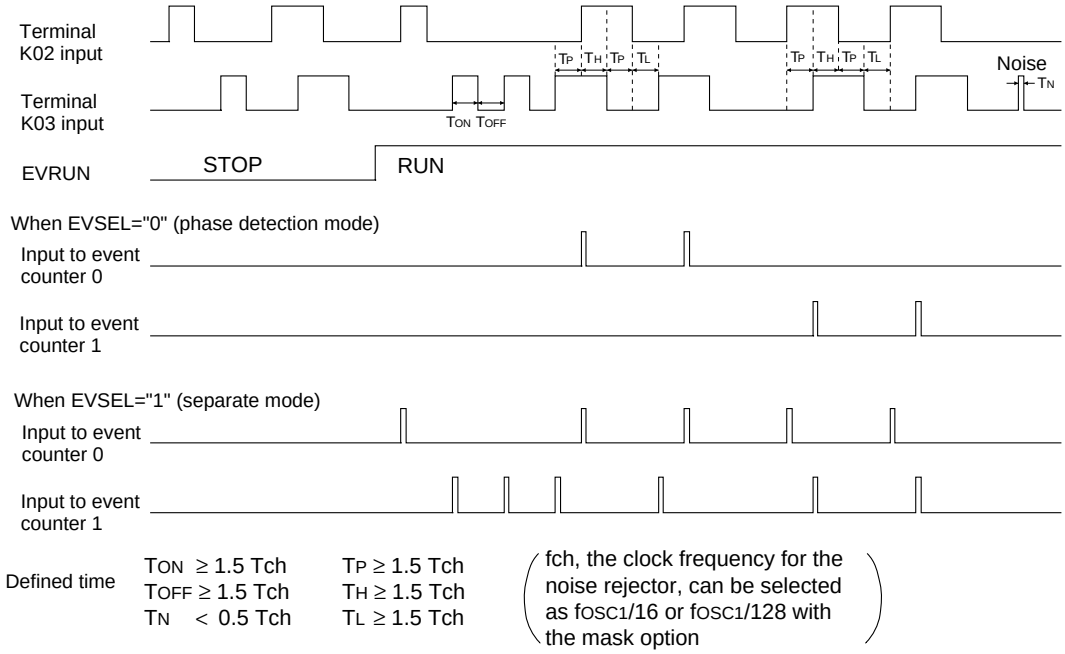


Fig. 4.12.2
Timing chart of event counter

Mask option

The clock frequency of the noise rejector can be selected as fOSC1/16 or fOSC1/128.
Table 4.12.1 lists the defined time depending on the frequency selected.

Table 4.12.1
Defined time depending on frequency selected

Selection	fOSC1 = 32,768 Hz		fOSC1 = 38,400 Hz	
	fOSC1/ 16	fOSC1/128	fOSC1/ 16	fOSC1/128
TN	0.24	1.95	0.20	1.66
TON	0.74	5.86	0.63	5.00
TOFF	0.74	5.86	0.63	5.00
TP	0.74	5.86	0.63	5.00
TH	0.74	5.86	0.63	5.00
TL	0.74	5.86	0.63	5.00

(Unit:msec)

TN : Max value
Others : Min value

Control of event counter

Table 4.12.2 shows the event counter control bits and their addresses.

Table 4.12.2 Event counter control bits

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
2F8H	EV03	EV02	EV01	EV00	EV03	0			Event counter 0 (low-order 4 bits)
					EV02	0			
					EV01	0			
	R				EV00	0			
2F9H	EV07	EV06	EV05	EV04	EV07	0			Event counter 0 (high-order 4 bits)
					EV06	0			
					EV05	0			
	R				EV04	0			
2FAH	EV13	EV12	EV11	EV10	EV13	0			Event counter 1 (low-order 4 bits)
					EV12	0			
					EV11	0			
	R				EV10	0			
2FBH	EV17	EV16	EV15	EV14	EV17	0			Event counter 1 (high-order 4 bits)
					EV16	0			
					EV15	0			
	R				EV14	0			
2FCH	EVSEL	ENRUN	EV1RST	EV0RST	EVSEL	0	Separate	Phase	Event counter mode
					EVRUN	0	Run	Stop	Event counter Run/Stop
	R/W		W		EV1RST*3	Reset	Reset	–	Event counter 1 reset
					EV0RST*3	Reset	Reset	–	Event counter 0 reset

*1 Initial value at the time of initial reset
*2 Not set in the circuit
*3 Constantly "0" when being read
*4 Reset (0) immediately after being read
*5 Undefined

EV00–EV03: Event counter 0 Low-order (2F8H)
The four low-order data bits of event counter 0 are read out. These four bits are read-only, and cannot be used for writing.
At initial reset, event counter 0 is set to "00H".

EV04–EV07: Event counter 0 High-order (2F9H)
The four high-order data bits of event counter 0 are read out. These four bits are read-only, and cannot be used for writing.
At initial reset, event counter 0 is set to "00H".

EV10–EV13: Event counter 1 Low-order (2FAH)
The four low-order data bits of event counter 1 are read out. These four bits are read-only, and cannot be used for writing.
At initial reset, event counter 1 is set to "00H".

EV14–EV17: Event counter 1 High-order (2FBH)
The four high-order data bits of event counter 1 are read out. These four bits are read-only, and cannot be used for writing.
At initial reset, event counter 1 is set to "00H".

EV0RST: Event counter 0 reset (2FCH·D0)
This is the register for resetting event counter 0.

When "1" is written :	Event counter 0 reset
When "0" is written :	No operation
Read-out :	Always "0"

When "1" is written, event counter 0 is reset and the data becomes "00H". When "0" is written, no operation is executed.
This is a write-only bit, and is always "0" at read-out.

EV1RST: Event counter 1 reset (2FCH·D1)

This is the register for resetting event counter 1.

When "1" is written :	Event counter 1 reset
When "0" is written :	No operation
Read-out :	Always "0"

When "1" is written, event counter 1 is reset and the data becomes "00H". When "0" is written, no operation is executed.
This is a write-only bit, and is always "0" at read-out.

EVRUN: Event counter RUN/STOP (2FCH·D2)

This register controls the event counter RUN/STOP status.

When "1" is written :	RUN
When "0" is written :	STOP
Read-out :	Valid

When "1" is written, the event counter enters the RUN status and starts receiving the clock signal input.
When "0" is written, the event counter enters the STOP status and the clock signal input is ignored. (However, input to the input port is valid.)
At initial reset, this register is set to "0".

EVSEL: Event counter mode (2FCH·D3)

This register control the count mode of the event counter.

When "1" is written :	Separate
When "0" is written :	Phase detection
Read-out :	Valid

When "0" is written, the phases of the two clock signals are detected, and the phase detection mode is selected, in which one of the counters is chosen to input the clock signal.
When "1" is written, the separate mode is selected, in which each clock signal is input to different counters.
At initial reset, this register is set to "0".

Programming notes

(1) After the event counter has written data to the EVRUN register, it operates or stops in synchronization with the falling edge of the noise rejector clock or stops. Hence, attention must be paid to the above timing when input signals (input to K02 and K03) are being received.

(2) To prevent erroneous reading of the event counter data, read out the counter data several times, compare it, and use the matching data as the result.

4.13 Analog Comparator

Configuration of analog comparator

The E0C6235 Series incorporates an MOS input analog comparator. This analog comparator, which has two differential input terminals (inverted input terminal AMPM, noninverted input terminal AMPP), can be used for general purposes.
Figure 4.13.1 shows the configuration of the analog comparator.

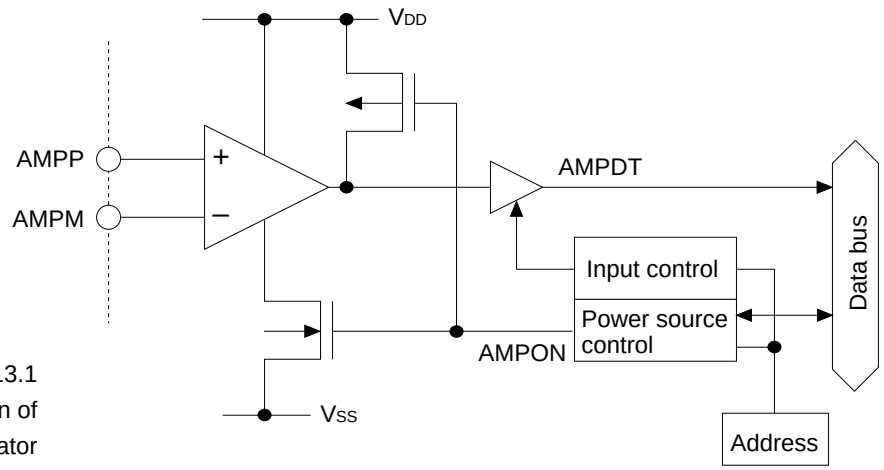


Fig. 4.13.1
Configuration of analog comparator

Operation of analog comparator

The analog comparator is ON when the AMPON register is "1", and compares the input levels of the AMPP and AMPM terminals. The result of the comparison is read from the AMPDT register. It is "1" when AMPP (+) > AMPM (-) and "0" when AMPP (+) < AMPM (-).

After the analog comparator goes ON it takes a maximum of 3 msec until the output stabilizes.

Control of analog comparator

Table 4.13.1 lists the analog comparator control bits and their addresses.

Table 4.13.1 Analog comparator control bits

Address	Register								Comment
	D3	D2	D1	D0	Name	Init *1	1	0	
2F7H	ENVON	ENVRT	AMPDT	AMPON	ENVON	0	On	Off	Envelope On/Off
					ENVRT	0	1.0 sec	0.5 sec	Envelope cycle selection register
	R/W		R	R/W	AMPDT	1	+ > -	+ < -	Analog comparator data
					AMPON	0	On	Off	Analog comparator On/Off

*1 Initial value at the time of initial reset
*2 Not set in the circuit
*3 Constantly "0" when being read
*4 Reset (0) immediately after being read
*5 Undefined

AMPON: Analog comparator ON/OFF (2F7H·D0)

Switches the analog comparator ON and OFF.

When "1" is written : The analog comparator goes ON
When "0" is written : The analog comparator goes OFF
Read-out : Valid

The analog comparator goes ON when "1" is written to AMPON, and OFF when "0" is written.
At initial reset, AMPON is set to "0".

AMPDT: Analog comparator data (2F7H·D1)

Reads out the output from the analog comparator.

When "1" is read out : AMPP (+) > AMPM (-)
When "0" is read out : AMPP (+) < AMPM (-)
Writing : Invalid

AMPDT is "0" when the input level of the inverted input terminal (AMPM) is greater than the input level of the noninverted input terminal (AMPP); and "1" when smaller.
At initial reset, AMPDT is set to "1".

Programming notes

(1) To reduce current consumption, set the analog comparator to OFF when it is not necessary.

(2) After setting AMPON to "1", wait at least 3 msec for the operation of the analog comparator to stabilize before reading the output data of the analog comparator from AMPDT.

4.14 Battery Life Detection (BLD) Circuit

Configuration of BLD circuit

The E0C6235 Series has a built-in battery life detection (BLD) circuit, so that the software can find when the source voltage lowers. The configuration of the BLD circuit is shown in Figure 4.14.1.
Also provides a heavy load protection function and an associated sub-BLD circuit. See 4.15 "Heavy Load Protection Function and Sub-BLD Circuit".
Turning the BLD operation ON/OFF is controlled through the software (HLMOD, BLS). Moreover, when a drop in source voltage (BLD0 = "1") is detected by the sub-BLD circuit, BLD operation is periodically performed by the hardware until the source voltage is recovered (BLD0 = "0"). Because the power current consumption of the IC becomes big when the BLD operation is turned ON, set the BLD operation to OFF unless otherwise necessary.

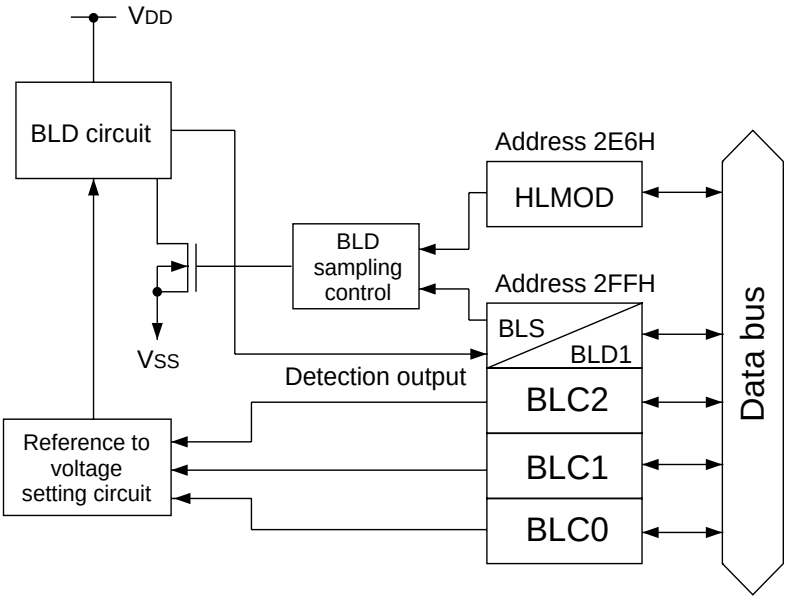


Fig. 4.14.1
Configuration of BLD circuit

Programmable selection of evaluation voltage

In the E0C6235 Series, the evaluation voltage for judging the battery life can be switched by programming. Consequently, the optimum evaluation voltage can be set for the battery used.
One of eight evaluation voltages can be selected with the software. Table 4.14.1 lists the evaluation voltages for the models in the E0C6235 Series.

Table 4.14.1
Evaluation voltages for BLD circuit

Evaluation voltage setting			Evaluation voltage		
BLC2	BLC1	BLC0	E0C62L35	E0C6235	E0C62A35
0	0	0	1.05 V	2.20 V	2.20 V
0	0	1	1.10 V	2.25 V	2.25 V
0	1	0	1.15 V	2.30 V	2.30 V
0	1	1	1.20 V	2.35 V	2.35 V
1	0	0	1.25 V	2.40 V	2.40 V
1	0	1	1.30 V	2.45 V	2.45 V
1	1	0	1.35 V	2.50 V	2.50 V
1	1	1	1.40 V	2.55 V	2.55 V

See the electrical characteristics for the evaluation voltage accuracy.

Detection timing of BLD circuit

This section explains the timing for when the BLD circuit writes the result of the source voltage detection to the BLD latch.
Turning the BLD operation ON/OFF is controlled through the software (HLMOD, BLS). Moreover, when a drop in source voltage (BLD0 = "1") is detected by the sub-BLD circuit, BLD operation is periodically performed by the hardware until the source voltage is recovered (BLD0 = "0").
The result of the source voltage detection is written to the BLD latch by the BLD circuit, and this data can be read out by the software to find the status of the source voltage.
There are three status, explained below, for the detection timing of the BLD circuit.

(1) Sampling with HLMOD set to "1"

When HLMOD is set to "1" and BLD sampling executed, the detection results can be written to the BLD latch in the following two timings.

① Immediately after the time for one instruction cycle has ended immediately after HLMOD = "1"
② Immediately after sampling in the 2 Hz cycle output by the clock timer while HLMOD = "1"

Consequently, the BLD latch data is loaded immediately after HLMOD has been set to "1", and at the same time the new detection result is written in 2 Hz cycles.
To obtain a stable BLD detection result, the BLD circuit must be set to ON with at least 100 µsec.
When the CPU system clock is f_{OSC3} in E0C62A35, the detection result at the timing in ① above may be invalid or incorrect. (When performing BLD detection using the timing in ①, be sure that the CPU system clock is f_{OSC1}.)

(2) Sampling with BLS set to "1"

When BLS is set to "1", BLD detection is executed. As soon as BLS is reset to "0" the detection result is loaded to the BLD latch. To obtain a stable BLD detection result, the BLD circuit must be set to ON with at least 100 µsec. Hence, to obtain the BLD detection result, follow the programming sequence below.

0. Set HLMOD to "1" (only when the CPU system clock is f_{OSC3} in E0C62A35)
1. Set BLS to "1"
2. Maintain at 100 µsec minimum
3. Set BLS to "0"
4. Read out BLD
5. Set HLMOD to "0" (only when the CPU system clock is f_{OSC3} in E0C62A35)

However, when a crystal oscillation clock (f_{OSC1}) is selected for the CPU system clock in E0C6235, E0C62L35, and E0C62A35, the instruction cycles are long enough, so that there is no need for concern about maintaining 100 µsec for the BLS = "1" with the software.

(3) Sampling by hardware when sub-BLD latch is set to "1"

When BLD0 (sub-BLD latch) is set to "1", the detection results can be written to the BLD0 (sub-BLD latch) and BLD1 (BLD latch) in the following two timings (same as that sampling with HLMOD set to "1").

① Immediately after the time for one instruction cycle has ended immediately after BLD0 = "1"

② Immediately after sampling in the 2 Hz cycle output by the clock timer while BLD0 = "1"

Consequently, the BLD0 (sub-BLD latch) and BLD1 (BLD latch) data are loaded immediately after BLD0 (sub-BLD latch) has been set to "1", and at the same time the new detection result is written in 2 Hz cycles.
To obtain a stable BLD detection result, the BLD circuit must be set to ON with at least 100 µsec.
When the CPU system clock is f_{OSC3} in E0C62A35, the detection result at the timing in ① above may be invalid or incorrect.

Control of BLD circuit

Table 4.14.2 shows the BLD circuit's control bits and their addresses.

Table 4.14.2 Control bits of BLD circuit

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
2E6H	HLMOD	BLD0	EISWIT1	EISWIT0	HLMOD	0	Heavy load	Normal	Heavy load protection mode register
					BLD0	0	Low	Normal	Sub-BLD evaluation data
	R/W	R	R/W		EISWIT1	0	Enable	Mask	Interrupt mask register (stopwatch 1 Hz)
					EISWIT0	0	Enable	Mask	Interrupt mask register (stopwatch 10 Hz)
2FFH	BLS	BLC2	BLC1	BLC0	BLS	0	On	Off	BLD On/Off
	BLD1				BLD1	0	Low	Normal	BLD voltage evaluation data
	W	R/W			BLC2	× *5			Evaluation voltage setting register
	R				BLC1	× *5			[BLC2–0] 0 1 2 3 4 5 6 7
					BLC0	× *5			E0C6235/62A35 2.20 2.25 2.30 2.35 2.40 2.45 2.50 2.55 (V)
									E0C62L35 1.05 1.10 1.15 1.20 1.25 1.30 1.35 1.40 (V)

*1 Initial value at the time of initial reset
*2 Not set in the circuit
*3 Constantly "0" when being read
*4 Reset (0) immediately after being read
*5 Undefined

HLMOD:	When "1" is written :	Heavy load protection mode is set
Heavy load protection mode	When "0" is written :	Heavy load protection mode is released
(2E6H·D3)	Read-out :	Valid

When HLMOD is set to "1", the IC operating status enters the heavy load protection mode and at the same time the battery life detection of the BLD circuit is controlled (ON/OFF).
For details about the heavy load protection mode, see "4.15 Heavy Load Protection Function and Sub-BLD Circuit".
When HLMOD is set to "1", sampling control is executed for the BLD circuit ON time. There are two types of sampling time, as follows:

(1) The time of one instruction cycle immediately after HLMOD = "1"
(2) Sampling at cycles of 2 Hz output by the clock timer while HLMOD = "1"

The BLD circuit must be made ON with at least 100 µsec for the BLD circuit to respond. Hence, when the CPU system clock is f_{OSC3} in E0C62A35, the detection result at the timing in (1) above may be invalid or incorrect. When performing BLD detection using the timing in (1), be sure that the CPU system clock is f_{OSC1}.
When BLD sampling is done with HLMOD set to "1", the results are written to the BLD latch in the timing as follows:

(1) As soon as the time has elapsed for one instruction cycle immediately following HLMOD = "1"
(2) Immediately on completion of sampling at cycles of 2 Hz output by the clock timer while HLMOD = "1"

Consequently, the BLD latch data is written immediately after HLMOD is set to "1", and at the same time the new detection result is written in 2 Hz cycles.

BLS/BLD1:	When "0" is written :	BLD detection OFF
BLD detection/BLD data	When "1" is written :	BLD detection ON
(2F3H·D3)	When "0" is read out :	Source voltage (V_{DD}–V_{SS}) is higher than BLD set value
	When "1" is read out :	Source voltage (V_{DD}–V_{SS}) is lower than BLD set value

Note that the function of this bit when written is different to when read out.
When this bit is written to, ON/OFF of the BLD detection operation is controlled; when this bit is read out, the result of the BLD detection (contents of BLD latch) is obtained.
Appreciable current is consumed during operation of BLD detection, so keep BLD detection OFF except when necessary.

When BLS is set to "1", BLD detection is executed. As soon as BLS is reset to "0" the detection result is loaded to the BLD latch. To obtain a stable BLD detection result, the BLD circuit must be set to ON with at least 100 µsec. Hence, to obtain the BLD detection result, follow the programming sequence below.

0. Set HLMOD to "1" (only when the CPU system clock is f_{OSC3} in E0C62A35)
1. Set BLS to "1"
2. Maintain at 100 µsec minimum
3. Set BLS to "0"
4. Read out BLD
5. Set HLMOD to "0" (only when the CPU system clock is f_{OSC3} in E0C62A35)

However, when a crystal oscillation clock (f_{OSC1}) is selected for the CPU system clock in E0C6235, E0C62L35, and E0C62A35, the instruction cycles are long enough, so that there is no need for concern about maintaining 100 µsec for the BLS = "1" with the software.

Programming notes

(1) It takes 100 µsec from the time the BLD circuit goes ON until a stable result is obtained. For this reason, keep the following software notes in mind:

① When the CPU system clock is fOSC1

1. When detection is done at HLMOD
   After writing "1" on HLMOD, read the BLD after 1 instruction has passed.

2. When detection is done at BLS
   After writing "1" on BLS, write "0" after at least 100 µsec has lapsed (possible with the next instruction) and then read the BLD.

② When the CPU system clock is fOSC3
(in case of E0C62A35 only)

1. When detection is done at HLMOD
   After writing "1" on HLMOD, read the BLD after 0.6 second has passed.
   (HLMOD holds "1" for at least 0.6 second)

2. When detection is done at BLS
   Before writing "1" on BLS, write "1" on HLMOD first; after at least 100 µsec has lapsed after writing "1" on BLS, write "0" on BLS and then read the BLD.

(2) BLS resides in the same bit at the same address as BLD1, and one or the other is selected by write or read operation. This means that arithmetic operations (AND, OR, ADD, SUB and so forth) cannot be used for BLS control.

4.15 Heavy Load Protection Function and Sub-BLD Circuit

This section explains the heavy load protection and sub-BLD circuit.

Configuration and operation of heavy load protection function

Note that the heavy load protection function on the E0C62L35 is different from the E0C6235/62A35.

(1) In case of E0C62L35

The E0C62L35 has the heavy load protection function for when the battery load becomes heavy and the source voltage drops, such as when an external buzzer sounds or an external lamp lights. The state where the heavy load protection function is in effect is called the heavy load protection mode. In this mode, operation with a lower voltage than normal is possible.
The normal mode changes to the heavy load protection mode in the following two cases:

① When the software changes the mode to the heavy load protection mode (HLMOD = "1")

② When source voltage drop (BLD0 = "1") in the sub-BLD circuit is detected, the mode will automatically shift to the heavy load protection mode until the source voltage is recovered (BLD0 = "0")

The sub-BLD circuit, a BLD circuit dedicated to 2.4 V/1.2 V detection, operates in synchronize with the BLD circuit. It is the E0C62L35's battery life detection circuit controlling the heavy load protection function so that operation is assured even when the source voltage drops. Based on the workings of the sub-BLD circuit and the heavy load protection function, the E0C62L35 realizes operation at 0.9 V source voltage. See the electrical characteristics for the precisions of voltage detection by this sub-BLD circuit.
Figure 4.15.1 shows the configuration of the heavy load protection function and the sub-BLD circuit.

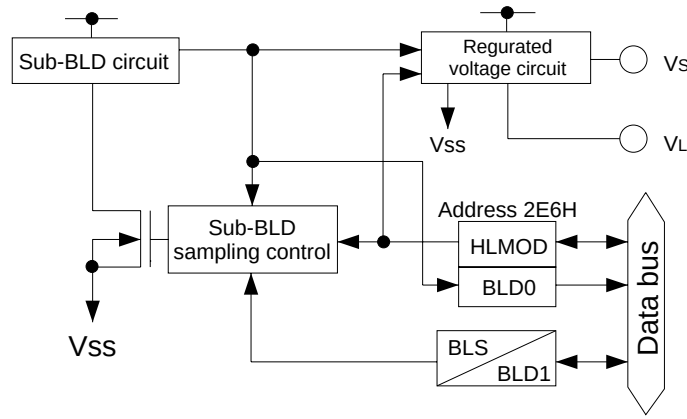


Fig. 4.15.1
Configuration of sub-BLD circuit

In the heavy load protection mode, the internally regulated voltage is generated by the liquid crystal driver source output V_{L2} so as to operate the internal circuit. Consequently, more current is consumed in the heavy load protection mode than in the normal mode. Unless it is necessary, be careful not to set the heavy load protection mode with the software.

(2) In case of E0C6235/62A35

The E0C6235/62A35 has the heavy load protection function for when the battery load becomes heavy and the source voltage changes, such as when an external buzzer sounds or an external lamp lights. The state where the heavy load protection function is in effect is called the heavy load protection mode. Compared with the normal operation mode, this mode can reduce the output voltage variation of the constant voltage/booster voltage circuit of the LCD system.
The normal mode changes to the heavy load protection mode in the following case:

① When the software changes the mode to the heavy load protection mode (HLMOD = "1")

The heavy load protection mode switches the constant voltage circuit of the LCD system to the high-stability mode from the low current consumption mode. Consequently, more current is consumed in the heavy load protection mode than in the normal mode. Unless it is necessary, be careful not to set the heavy load protection mode with the software.

Operation of sub-BLD circuit

Software control of the sub-BLD circuit is virtually the same as for the BLD circuit, except that the evaluation voltage cannot be set by programming.
Just as for the BLD circuit, HLMOD or BLS control the detection timing of the sub-BLD circuit and the timing for writing the detection data to the sub-BLD latch. However, for the E0C62L35, even if the sub-BLD circuit detects a drop in source voltage (1.2 V or below) and invokes the heavy load protection mode, this will be the same as when the software invokes the heavy load protection mode, in that the BLD circuit and sub-BLD circuit will be sampled in timing synchronized to the 2 Hz output from the prescaler. If the sub-BLD circuit detects a voltage drop and enters the heavy load protection mode, it will return to the normal mode once the source voltage recovers and the BLD circuit judges that the source voltage is 1.2 V or more.
For the E0C6235/62A35, when the sub-BLD circuit detects a drop in source voltage (2.4 V or below) and the detection data is written to the sub-BLD latch, the BLD circuit and sub-BLD circuit will be sampled in timing synchronized to the 2 Hz output from the prescaler. Once the source voltage recovers and the BLD circuit judges that the source voltage is 2.4 V or more, the BLD circuit and sub-BLD circuit won't be sampled in timing synchronized to the 2 Hz output from the prescaler.

Control of heavy load protection function and sub-BLD circuit

Table 4.15.1 shows the control bits and their addresses for the heavy load protection function and sub-BLD circuit.

Table 4.15.1 Control bits of BLD circuit

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
2E6H	HLMOD	BLD0	EISWIT1	EISWIT0	HLMOD	0	Heavy load	Normal	Heavy load protection mode register
					BLD0	0	Low	Normal	Sub-BLD evaluation data
	R/W	R	R/W		EISWIT1	0	Enable	Mask	Interrupt mask register (stopwatch 1 Hz)
					EISWIT0	0	Enable	Mask	Interrupt mask register (stopwatch 10 Hz)
2FFH	BLS	BLC2	BLC1	BLC0	BLS	0	On	Off	BLD On/Off
	BLD1				BLD1	0	Low	Normal	BLD voltage evaluation data
	W	R/W			BLC2	× *5			Evaluation voltage setting register
	R				BLC1	× *5			[BLC2–0] 0 1 2 3 4 5 6 7
					BLC0	× *5			E0C6235/62A35 2.20 2.25 2.30 2.35 2.40 2.45 2.50 2.55 (V)
									E0C62L35 1.05 1.10 1.15 1.20 1.25 1.30 1.35 1.40 (V)

*1 Initial value at the time of initial reset
*2 Not set in the circuit
*3 Constantly "0" when being read
*4 Reset (0) immediately after being read
*5 Undefined

HLMOD: Heavy load protection mode (2E6H·D3)	When "1" is written :	Heavy load protection mode is set
	When "0" is written :	Heavy load protection mode is released
	Read-out :	Valid

When HLMOD is set to "1", the IC operating status enters the heavy load protection mode and at the same time the battery life detection of the BLD circuit is controlled (ON/OFF).
When HLMOD is set to "1", sampling control is executed for the BLD circuit ON time. There are two types of sampling time, as follows:

(1) The time of one instruction cycle immediately after HLMOD = "1"
(2) Sampling at cycles of 2 Hz output by the clock timer while HLMOD = "1"

The BLD circuit must be made ON with at least 100 µsec for the BLD circuit to respond. Hence, when the CPU system clock is f_{OSC3} in E0C62A35, the detection result at the timing in (1) above may be invalid or incorrect. When performing BLD detection using the timing in (1), be sure that the CPU system clock is f_{OSC1}.
When BLD sampling is done with HLMOD set to "1", the results are written to the BLD latch in the timing as follows:

(1) As soon as the time has elapsed for one instruction cycle immediately following HLMOD = "1"
(2) Immediately on completion of sampling at cycles of 2 Hz output by the clock timer while HLMOD = "1"

Consequently, the BLD latch data is written immediately after HLMOD is set to "1", and at the same time the new detection result is written in 2 Hz cycles.

BLD0: Sub-BLD data (2E6H·D2)	When "0" is read out :	High source voltage upward from about 2.4 V (E0C6235/62A35) /1.2 V (E0C62L35)
	When "1" is read out :	Low source voltage from about 2.4 V (E0C6235/62A35) /1.2 V (E0C62L35) or under
	Writing :	Invalid

When BLD0 is "1" the CPU enters the heavy load protection mode. In the heavy load protection mode, the detection operation of the BLD circuit and sub-BLD circuit is sampled in 2 Hz cycles, and the respective detection results are written to the BLD latch and sub-BLD latch.

BLS/BLD1: BLD detection/BLD data (2F3H·D3)	When "0" is written :	BLD detection OFF
	When "1" is written :	BLD detection ON
	When "0" is read out :	Source voltage (V_{DD}–V_{SS}) is higher than BLD set value
	When "1" is read out :	Source voltage (V_{DD}–V_{SS}) is lower than BLD set value

Note that the function of this bit when written is different to when read out.
When this bit is written to, ON/OFF of the BLD detection operation is controlled; when this bit is read out, the result of the BLD detection (contents of BLD latch) is obtained.
Appreciable current is consumed during operation of BLD detection, so keep BLD detection OFF except when necessary.

When BLS is set to "1", BLD detection is executed. As soon as BLS is reset to "0" the detection result is loaded to the BLD latch. To obtain a stable BLD detection result, the BLD circuit must be set to ON with at least 100 µsec.

Hence, to obtain the BLD detection result, follow the programming sequence below.

0. Set HLMOD to "1" (only when the CPU system clock is fOSC3 in E0C62A35)
1. Set BLS to "1"
2. Maintain at 100 µsec minimum
3. Set BLS to "0"
4. Read out BLD
5. Set HLMOD to "0" (only when the CPU system clock is fOSC3 in E0C62A35)

However, when a crystal oscillation clock (fOSC1) is selected for the CPU system clock in E0C6235, E0C62L35, and E0C62A35, the instruction cycles are long enough, so that there is no need for concern about maintaining 100 µsec for the BLS = "1" with the software.

Programming notes

(1) It takes 100 µsec from the time the BLD circuit goes ON until a stable result is obtained. For this reason, keep the following software notes in mind:

① When the CPU system clock is f_{OSC1}

1. When detection is done at HLMOD
   After writing "1" on HLMOD, read the BLD after 1 instruction has passed.

2. When detection is done at BLS
   After writing "1" on BLS, write "0" after at least 100 µsec has lapsed (possible with the next instruction) and then read the BLD.

② When the CPU system clock is f_{OSC3}
(in case of E0C62A35 only)

1. When detection is done at HLMOD
   After writing "1" on HLMOD, read the BLD after 0.6 second has passed.
   (HLMOD holds "1" for at least 0.6 second)

2. When detection is done at BLS
   Before writing "1" on BLS, write "1" on HLMOD first; after at least 100 µsec has lapsed after writing "1" on BLS, write "0" on BLS and then read the BLD.

(2) BLS resides in the same bit at the same address as BLD1, and one or the other is selected by write or read operation. This means that arithmetic operations (AND, OR, ADD, SUB and so forth) cannot be used for BLS control.

(3) Select one of the following software processing to return to the normal mode after a heavy load has been driven in the heavy load protection mode in the E0C62L35.

① After heavy load drive is completed, return to the normal mode after at least one second has elapsed.

② After heavy load drive is completed, switch BLS ON and OFF (at least 100 µsec is necessary for the ON status) and then return to the normal mode.

The E0C6235/62A35 returns to the normal mode after driving a heavy load without special software processing.

(4) If the BLS is set to ON while the heavy load protection mode is in effect, keep the ON time within 10 msec.

4.16 Interrupt and HALT

The E0C6235 Series provides the following interrupt settings, each of which is maskable.

External interrupt:	Input interrupt (three)
Internal interrupt:	Timer interrupt (three)
	Stopwatch interrupt (two)
	Serial interface interrupt (one)

To authorize interrupt, the interrupt flag must be set to "1" (EI) and the necessary related interrupt mask registers must be set to "1" (enable).
When an interrupt occurs the interrupt flag is automatically reset to "0" (DI), and interrupts after that are inhibited.
When a HALT instruction is input the CPU operating clock stops, and the CPU enters the HALT status.
The CPU is reactivated from the HALT status when an interrupt request occurs.
If reactivation is not caused by an interrupt request, initial reset by the watchdog timer causes reactivates the CPU (when the watchdog timer is enabled).
Figure 4.16.1 shows the configuration of the interrupt circuit.

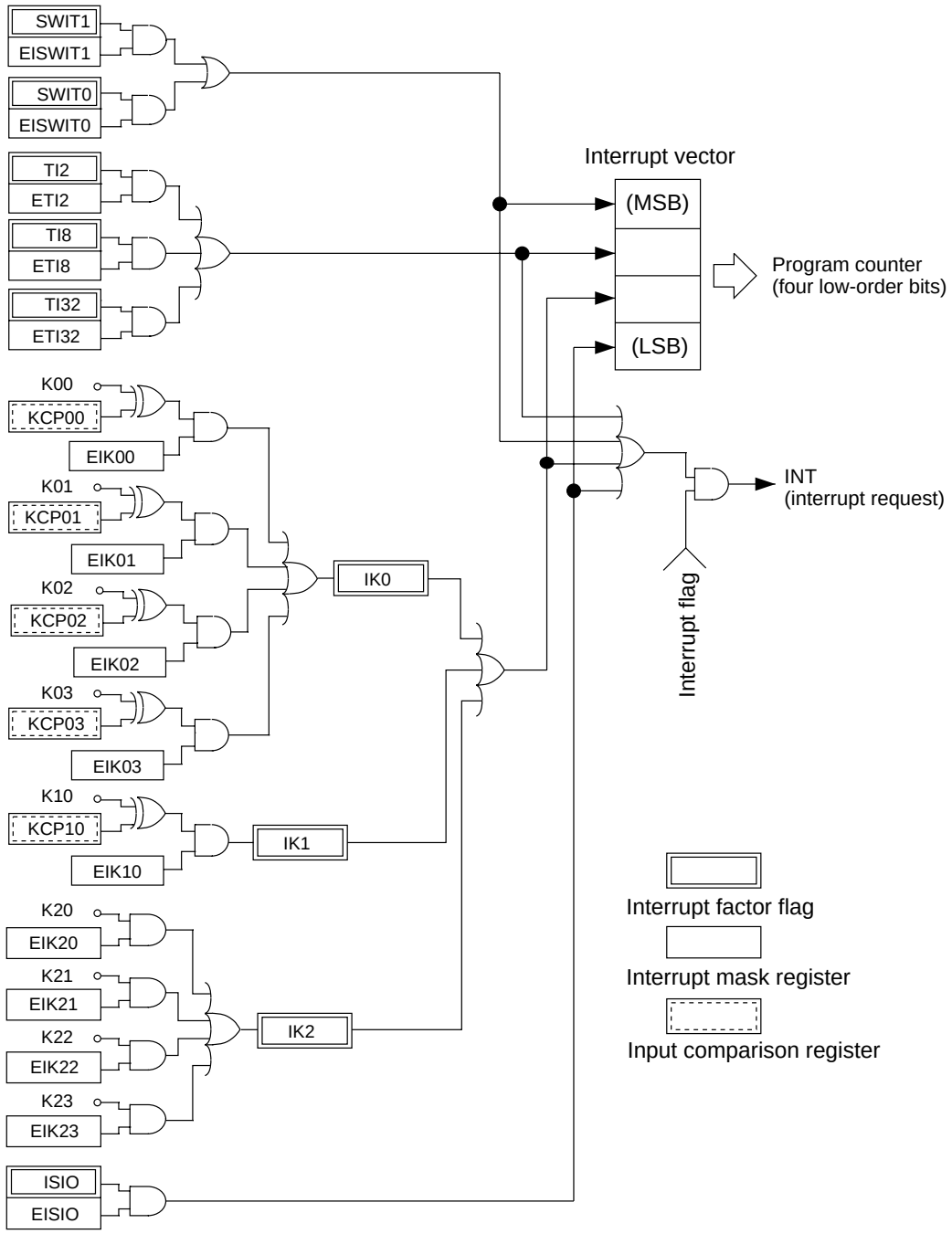


Fig. 4.16.1
Configuration of
interrupt circuit

Interrupt factors

Table 4.16.1 shows the factors for generating interrupt requests.

The interrupt flags are set to "1" depending on the corresponding interrupt factors.
The CPU operation is interrupted when any of the conditions below set an interrupt factor flag to "1".

- The corresponding mask register is "1" (enabled)
- The interrupt flag is "1" (EI)

The interrupt factor flag is a read-only register, but can be reset to "0" when the register data is read out.
At initial reset, the interrupt factor flags are reset to "0".

Note *Read the interrupt factor flags only in the DI status (interrupt flag = "0").*
A malfunction could result from read-out during the EI status (interrupt flag = "1").

Table 4.16.1
Interrupt factors

Interrupt factor	Interrupt factor flag	
Clock timer 2 Hz falling edge	TI2	(2E9H·D2)
Clock timer 8 Hz falling edge	TI8	(2E9H·D1)
Clock timer 32 Hz falling edge	TI32	(2E9H·D0)
Stopwatch timer 1 Hz falling edge	SWIT1	(2EAH·D1)
Stopwatch timer 10 Hz falling edge	SWIT0	(2EAH·D0)
Serial interface When 8-bit data input/output has completed	ISIO	(2F3H·D0)
Input data (K00–K03) Rising or falling edge	IK0	(2EAH·D2)
Input data (K10) Rising or falling edge	IK1	(2EAH·D3)
Input data (K00–K03) Rising or falling edge	IK2	(2F3H·D1)

Specific masks and factor flags for interrupt

The interrupt factor flags can be masked by the corresponding interrupt mask registers.
The interrupt mask registers are read/write registers. They are enabled (interrupt authorized) when "1" is written to them, and masked (interrupt inhibited) when "0" is written to them.
At initial reset, the interrupt mask register is set to "0".
Table 4.16.2 shows the correspondence between interrupt mask registers and interrupt factor flags.

Table 4.16.2
Interrupt mask registers and interrupt factor flags

Interrupt mask register		Interrupt factor flag	
ETI2	(2E8H·D2)	TI2	(2E9H·D2)
ETI8	(2E8H·D1)	TI8	(2E9H·D1)
ETI32	(2E8H·D0)	TI32	(2E9H·D0)
EISWIT1	(2E6H·D1)	SWIT1	(2EAH·D1)
EISWIT0	(2E6H·D0)	SWIT0	(2EAH·D0)
EISIO	(2F2H·D0)	ISIO	(2F3H·D0)
EIK03	(2E5H·D3)	IK0	(2EAH·D2)
EIK02	(2E5H·D2)		
EIK01	(2E5H·D1)		
EIK00	(2E5H·D0)		
EIK10	(2E7H·D2)	IK1	(2EAH·D3)
EIK23	(2F5H·D3)	IK2	(2F3H·D1)
EIK22	(2F5H·D2)		
EIK21	(2F5H·D1)		
EIK20	(2F5H·D0)		

* There is an interrupt mask register for each pin of the input ports.

Interrupt vectors

When an interrupt request is input to the CPU, the CPU begins interrupt processing. After the program being executed is terminated, the interrupt processing is executed in the following order.

① The address data (value of program counter) of the program to be executed next is saved in the stack area (RAM).

② The interrupt request causes the value of the interrupt vector (page 1, 01H–0FH) to be set in the program counter.

③ The program at the specified address is executed (execution of interrupt processing routine by software).

Table 4.16.3 shows the correspondence of interrupt requests and interrupt vectors.

Note *The processing in ① and ② above take 12 cycles of the CPU system clock.*

Table 4.16.3
Interrupt request and interrupt vectors

PC	Value	Interrupt request	
PCS3	1	Stopwatch interrupt	Enabled
	0		Masked
PCS2	1	Timer interrupt	Enabled
	0		Masked
PCS1	1	Input (K00–K03 or K10 or K20–K23) interrupt	Enabled
	0	Input (K00–K03 and K10 and K20–K23) interrupt	Masked
PCS0	1	Serial interface interrupt	Enabled
	0		Masked

The four low-order bits of the program counter are indirectly addressed through the interrupt request.

Control of interrupt and HALT

Table 4.16.4 shows the interrupt control bits and their addresses.

Table 4.16.4 Interrupt control bits

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
2E4H	KCP03	KCP02	KCP01	KCP00	KCP03	0	↓	↑	Input comparison register (K00–K03)
					KCP02	0	↓	↑	
					KCP01	0	↓	↑	
	R/W				KCP00	0	↓	↑	
2E5H	EIK03	EIK02	EIK01	EIK00	EIK03	0	Enable	Mask	Interrupt mask register (K00–K03)
					EIK02	0	Enable	Mask	
					EIK01	0	Enable	Mask	
	R/W				EIK00	0	Enable	Mask	
2E6H	HLMOD	BLD0	EISWIT1	EISWIT0	HLMOD	0	Heavy load	Normal	Heavy load protection mode register
					BLD0	0	Low	Normal	Sub-BLD evaluation data
	R/W	R	R/W		EISWIT1	0	Enable	Mask	Interrupt mask register (stopwatch 1 Hz)
					EISWIT0	0	Enable	Mask	Interrupt mask register (stopwatch 10 Hz)
2E7H	SCTRG	EIK10	KCP10	K10	SCTRG*3	–	Trigger	–	Serial interface clock trigger
					EIK10	0	Enable	Mask	Interrupt mask register (K10)
	W	R/W		R	KCP10	0	↓	↑	Input comparison register (K10)
					K10	– *2	High	Low	Input port data (K10)
2E8H	CSDC	ETI2	ETI8	ETI32	CSDC	0	Static	Dynamic	LCD drive switch
					ETI2	0	Enable	Mask	Interrupt mask register (clock timer 2 Hz)
					ETI8	0	Enable	Mask	Interrupt mask register (clock timer 8 Hz)
	R/W				ETI32	0	Enable	Mask	Interrupt mask register (clock timer 32 Hz)
2E9H	0	TI2	TI8	TI32	0 *3	– *2	–	–	Unused
					TI2 *4	0	Yes	No	Interrupt factor flag (clock timer 2 Hz)
					TI8 *4	0	Yes	No	Interrupt factor flag (clock timer 8 Hz)
	R				TI32 *4	0	Yes	No	Interrupt factor flag (clock timer 32 Hz)
2EAH	IK1	IK0	SWIT1	SWIT0	IK1 *4	0	Yes	No	Interrupt factor flag (K10)
					IK0 *4	0	Yes	No	Interrupt factor flag (K00–K03)
					SWIT1 *4	0	Yes	No	Interrupt factor flag (stopwatch 1 Hz)
	R				SWIT0 *4	0	Yes	No	Interrupt factor flag (stopwatch 10 Hz)
2F2H	SCS1	SCS0	SE2	EISIO	SCS1	1			SIF clock mode selection register [SCS1, 0]: 0 Clock, 1 CLK, 2 CLK/2, 3 CLK/4, slave
					SCS0	1			
					SE2	0	↑	↓	SIF clock edge selection register
	R/W				EISIO	0	Enable	Mask	Interrupt mask register (serial interface)
2F3H	0	0	IK2	ISIO	0 *3	– *2	–	–	Unused
					0 *3	– *2	–	–	Unused
	R				IK2 *4	0	Yes	No	Interrupt factor flag (K20–K23)
					ISIO *4	0	Yes	No	Interrupt factor flag (serial interface)
2F5H	EIK23	EIK22	EIK21	EIK20	EIK23	0	Enable	Mask	Interrupt mask register (K20–K23)
					EIK22	0	Enable	Mask	
					EIK21	0	Enable	Mask	
	R/W				EIK20	0	Enable	Mask	

*1 Initial value at the time of initial reset
*2 Not set in the circuit
*3 Constantly "0" when being read
*4 Reset (0) immediately after being read
*5 Undefined

– ETI32, ETI8, ETI2: Interrupt mask registers (2E8H·D0–D2)
– TI32, TI8, TI2: Interrupt factor flags (2E9H·D0–D2)

See "4.9 Clock Timer".

– EISWIT0, EISWIT1: Interrupt mask registers (2E6H·D0–D1)
– SWIT0, SWIT1: Interrupt factor flags (2EAH·D0–D1)

See "4.10 Stopwatch Timer".

– EISIO: Interrupt mask register (2F2H·D0)
– ISIO: Interrupt factor flag (2F3H·D0)

See "4.7 Serial Interface".

– KCP00–KCP03: Input comparison registers (2E4H)
– EIK00–EIK03: Interrupt mask registers (2E5H)
– IK0: Interrupt factor flag (2EAH·D2)

See "4.4 Input Ports".

– KCP10: Input comparison register (2E7H·D1)
– EIK10: Interrupt mask register (2E7H·D2)
– IK1: Interrupt factor flag (2EAH·D3)

See "4.4 Input Ports".

– EIK20–EIK23: Interrupt mask registers (2F5H)
– IK2: Interrupt factor flag (2F3H·D1)

See "4.4 Input Ports".

Programming notes

(1) When the interrupt mask register (EIK) is set to "0", the interrupt factor flag (IK) of the input port cannot be set even though the terminal status of the input port has changed.

(2) The interrupt factor flags of the clock timer, stopwatch timer and serial interface (TI, SWIT, ISIO) are set when the timing condition is established, even if the interrupt mask registers (ETI, EISWIT, EISIO) are set to "0".

(3) Read out the interrupt factor flags only in the DI status (interrupt flag = "0"). If read-out is performed in the EI status (interrupt flag = "1") a malfunction will result.

(4) Writing to the interrupt mask register only in the DI status (interrupt flag = "0"). Writing to the interrupt mask register while in the EI status (interrupt flag = "1") may cause mulfunction.

CHAPTER 5 SUMMARY OF NOTES

5.1 Notes for Low Current Consumption

The E0C6235 Series contains control registers for each of the circuits so that current consumption can be lowered. These control registers lower the current consumption through programs that operate the circuits at the minimum levels.
The following text explains the circuits that can control operation and their control registers. Refer to these when putting programs together.

Table 5.1.1 Circuits and control registers

Circuits (and Items)	Control registers	Order of consumed current
CPU	HALT instruction	See electrical characteristics (Chapter 7)
CPU operation frequency (E0C62A35)	CLKCHG, OSCC	See electrical characteristics (Chapter 7)
Heavy load protection mode	HLMOD	See electrical characteristics (Chapter 7)
BLD circuit	HLMOD, BLS	Several tens µA
Analog comparator	AMPON	Several tens µA

Below are the circuit statuses at initial reset.

CPU:	Operating status
CPU operating frequency:	Low speed side (CLKCHG = "0"), OSC3 oscillation circuit stop status (OSCC = "0")
Heavy load protection mode:	Normal operating mode (HLMOD = "0")
BLD circuit:	OFF status (HLMOD = "0", BLS = "0")
Analog comparator:	OFF status (AMPON = "0")

Also, be careful about panel selection because the current consumption can differ by the order of several µA on account of the LCD panel characteristics.

5.2 Summary of Notes by Function

Here, the cautionary notes are summed up by function category. Keep these notes well in mind when programming.

Memory

Memory is not mounted in unused area within the memory map and in memory area not indicated in this manual. For this reason, normal operation cannot be assured for programs that have been prepared with access to these areas.

Watchdog timer

When the watchdog timer is being used, the software must reset it within 3-second cycles, and timer data (WD0–WD2) cannot be used for timer applications.

Oscillation circuit and prescaler

(1) It takes at least 5 msec from the time the OSC3 oscillation circuit goes ON until the oscillation stabilizes. Consequently, when switching the CPU operation clock from OSC1 to OSC3, do this after a minimum of 5 msec have elapsed since the OSC3 oscillation went ON.
Further, the oscillation stabilization time varies depending on the external oscillator characteristics and conditions of use, so allow ample margin when setting the wait time.

(2) When switching the clock form OSC3 to OSC1, use a separate instruction for switching the OSC3 oscillation OFF. An error in the CPU operation can result if this processing is performed at the same time by the one instruction.

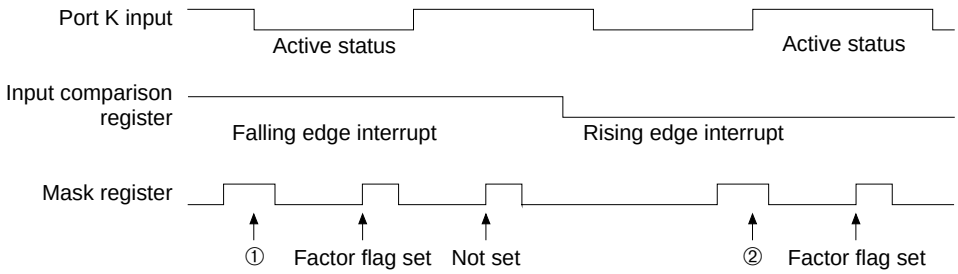
(3) To operate the clock timer and stopwatch timer accurately, select the prescaler of the OSC1 to match the crystal oscillator used.

Input port

(1) When input ports are changed from high to low by pull-down resistance, the fall of the waveform is delayed on account of the time constant of the pull-down resistance and input gate capacitance. Hence, when fetching input ports, set an appropriate wait time.
Particular care needs to be taken of the key scan during key matrix configuration. Aim for a wait time of about 1 msec.

(2) When "Use" is selected with the noise rejector mask option, a maximum delay of 1 msec occurs from time the interrupt conditions are established until the interrupt factor flag (IK) is set to "1" (until the interrupt is actually generated).
Hence, pay attention to the timing when reading out (resetting) the interrupt factor flag.
For example, when performing a key scan with the key matrix, the key scan changes the input status to set the interrupt factor flag, so it has to be read out to reset it. However, if the interrupt factor flag is read out immediately after key scanning, the delay will cause the flag to be set after read-out, so that it will not be reset.

(3) Input interrupt programing related precautions



When the content of the mask register is rewritten, while the port K input is in the active status. The input interrupt factor flags are set at ① and ②, ① being the interrupt due to the falling edge and ② the interrupt due to the rising edge.

Fig. 5.2.1
Input interrupt timing

When using an input interrupt, if you rewrite the content of the mask register, when the value of the input terminal which becomes the interrupt input is in the active status, the factor flag for input interrupt may be set. Therefore, when using the input interrupt, the active status of the input terminal implies

input terminal = low status, when the falling edge interrupt is effected and
input terminal = high status, when the rising edge interrupt is effected.

When an interrupt is triggered at the falling edge of an input terminal, a factor flag is set with the timing of ① shown in Figure 5.2.1.

However, when clearing the content of the mask register with the input terminal kept in the low status and then setting it, the factor flag of the input interrupt is again set at the timing that has been set.
Consequently, when the input terminal is in the active status (low status), do not rewrite the mask register (clearing, then setting the mask register), so that a factor flag will only set at the falling edge in this case. When clearing, then setting the mask register, set the mask register, when the input terminal is not in the active status (high status).
When an interrupt is triggered at the rising edge of the input terminal, a factor flag will be set at the timing of ② shown in Figure 5.2.1. In this case, when the mask registers cleared, then set, you should set the mask register, when the input terminal is in the low status.
In addition, when the mask register = "1" and the content of the input comparison register is rewritten in the input terminal active status, an input interrupt factor flag may be set. Thus, you should rewrite the content of the input comparison register in the mask register = "0" status.

(4) Read out the interrupt factor flag (IK) only in the DI status (interrupt flag = "0"). Read-out during EI status (interrupt flag = "1") will cause malfunction.

(5) Writing the interrupt mask register (EIK) only in the DI status (interrupt flag = "0"). Writing during EI status (interrupt flag = "1") will cause malfunction.

Output port

When BZ, $\overline{BZ}$ and FOUT are selected with the mask option, a hazard may be observed in the output waveform when the data of the output register changes.

I/O port

(1) When input data are changed from high to low by built-in pull-down resistance, the fall of the waveform is delayed on account of the time constant of the pull-down resistance and input gate capacitance. Consequently, if data is read out while the CPU is running in the OSC3 oscillation circuit, data must be read out continuously for about 500 µsec.

(2) When the I/O port is set to the output mode and the data register has been read, the terminal data instead of the register data can be read out. Because of this, if a low-impedance load is connected and read-out performed, the value of the register and the read-out result may differ.

Serial interface

(1) If the bit data of SE2 changes while SCLK is in the master mode, a hazard will be output to the SCLK pin. If this poses a problem for the system, be sure to set the SCLK to the external clock if the bit data of SE2 is to be changed.

(2) Be sure that read-out of the interrupt factor flag (ISIO) is done only when the serial port is in the STOP status (SIOF = "0") and the DI status (interrupt flag = "0"). If read-out is performed while the serial data is in the RUN status (during input or output), the data input or output will be suspended and the initial status resumed. Read-out during the EI status (interrupt flag = "1") causes malfunctioning.

(3) When using the serial interface in the master mode, the synchronous clock uses the CPU system clock. Accordingly, do not change the system clock ($f_{OSC1} \leftrightarrow f_{OSC3}$) while the serial interface is operating.

(4) Perform data writing/reading to data registers SD0–SD7 only while the serial interface is halted (i.e., the synchronous clock is neither being input or output).

(5) As a trigger condition, it is required that data writing or reading on data registers SD0–SD7 be performed prior to writing "1" to SCTRG. (The internal circuit of the serial interface is initiated through data writing/reading on data registers SD0–SD7.) Supply trigger only once every time the serial interface is placed in the RUN state. Moreover, when the synchronous clock SCLK is external clock, start to input the external clock after the trigger.

(6) Be sure that writing to the interrupt mask register is done only in the DI status (interrupt flag = "0"). Writing to the interrupt mask register while in the EI status (interrupt flag = "1") may cause malfunction.

LCD driver

(1) When page 0 is selected for the display memory, the memory data and the display will not match until the area is initialized (through, for instance, memory clear processing by the CPU). Initialize the display memory by executing initial processing.

(2) When page 2 is selected for the display memory, that area becomes write-only. Consequently, data cannot be rewritten by arithmetic operations (such as AND, OR, ADD, SUB).

Clock timer

(1) The prescaler mode must be set correctly to suit the rystl oscillator to be used.

(2) When the clock timer has been reset, the interrupt factor flag (TI) may sometimes be set to "1". Consequently, perform flag read-out (reset the flag) as necessary at reset.

(3) The input clock of the watchdog timer is the 2 Hz signal of the clock timer, so that the watchdog timer may be counted up at timer reset.

(4) Read-out the interrupt factor flag (TI) only during the DI status (interrupt flag = "0"). Read-out during EI status (interrupt flag = "1") will cause malfunction.

Stopwatch timer

(1) The prescaler mode must be set correctly so that the stopwatch timer suits the crystal oscillator to be used.

(2) If timer data is read out in the RUN status, the timer must be made into the STOP status, and after data is read out the RUN status can be restored. If data is read out when a carry occurs, the data cannot be read correctly.
Also, the processing above must be performed within the STOP interval of 976 µsec (256 Hz 1/4 cycle).

(3) Read-out of the interrupt factor flag (SWIT) must be done only in the DI status (interrupt flag = "0"). Read-out during EI status (interrupt flag = "1") will cause malfunction.

Sound generator

A hazard may be observed in the output waveform of the BZ and $\overline{BZ}$ signals when data of the output registers (R10, R13) and the buzzer frequency selection registers (BZFQ0–BZFQ2) changes.

Event counter

(1) After the event counter has written data to the EVRUN register, it operates or stops in synchronization with the falling edge of the noise rejector clock or stops. Hence, attention must be paid to the above timing when input signals (input to K02 and K03) are being received.

(2) To prevent erroneous reading of the event counter data, read out the counter data several times, compare it, and use the matching data as the result.

Analog comparator

(1) To reduce current consumption, set the analog comparator to OFF when it is not necessary.

(2) After setting AMPON to "1", wait at least 3 msec for the operation of the analog comparator to stabilize before reading the output data of the analog comparator from AMPDT.

Battery life detection (BLD) circuit

(1) It takes 100 µsec from the time the BLD circuit goes ON until a stable result is obtained. For this reason, keep the following software notes in mind:

① When the CPU system clock is f_{OSC1}

1. When detection is done at HLMOD
   After writing "1" on HLMOD, read the BLD after 1 instruction has passed.
2. When detection is done at BLS
   After writing "1" on BLS, write "0" after at least 100 µsec has lapsed (possible with the next instruction) and then read the BLD.

② When the CPU system clock is f_{OSC3}
(in case of E0C62A35 only)

1. When detection is done at HLMOD
   After writing "1" on HLMOD, read the BLD after 0.6 second has passed.
   (HLMOD holds "1" for at least 0.6 second)

2. When detection is done at BLS
   Before writing "1" on BLS, write "1" on HLMOD first; after at least 100 µsec has lapsed after writing "1" on BLS, write "0" on BLS and then read the BLD.

(2) BLS resides in the same bit at the same address as BLD1, and one or the other is selected by write or read operation. This means that arithmetic operations (AND, OR, ADD, SUB and so forth) cannot be used for BLS control.

Heavy load protection function and sub-BLD circuit

(1) It takes 100 µsec from the time the BLD circuit goes ON until a stable result is obtained. For this reason, keep the following software notes in mind:

① When the CPU system clock is f_{OSC1}

1. When detection is done at HLMOD
   After writing "1" on HLMOD, read the BLD after 1 instruction has passed.
2. When detection is done at BLS
   After writing "1" on BLS, write "0" after at least 100 µsec has lapsed (possible with the next instruction) and then read the BLD.

② When the CPU system clock is f_{OSC3}
(in case of E0C62A35 only)

1. When detection is done at HLMOD
   After writing "1" on HLMOD, read the BLD after 0.6 second has passed.
   (HLMOD holds "1" for at least 0.6 second)
2. When detection is done at BLS
   Before writing "1" on BLS, write "1" on HLMOD first; after at least 100 µsec has lapsed after writing "1" on BLS, write "0" on BLS and then read the BLD.

(2) BLS resides in the same bit at the same address as BLD1, and one or the other is selected by write or read operation. This means that arithmetic operations (AND, OR, ADD, SUB and so forth) cannot be used for BLS control.

(3) Select one of the following software processing to return to the normal mode after a heavy load has been driven in the heavy load protection mode in the E0C62L35.

① After heavy load drive is completed, return to the normal mode after at least one second has elapsed.

② After heavy load drive is completed, switch BLS ON and OFF (at least 100 µsec is necessary for the ON status) and then return to the normal mode.

The E0C6235/62A35 returns to the normal mode after driving a heavy load without special software processing.

(4) If the BLS is set to ON while the heavy load protection mode is in effect, keep the ON time within 10 msec.

Interrupt and HALT

(1) When the interrupt mask register (EIK) is set to "0", the interrupt factor flag (IK) of the input port cannot be set even though the terminal status of the input port has changed.

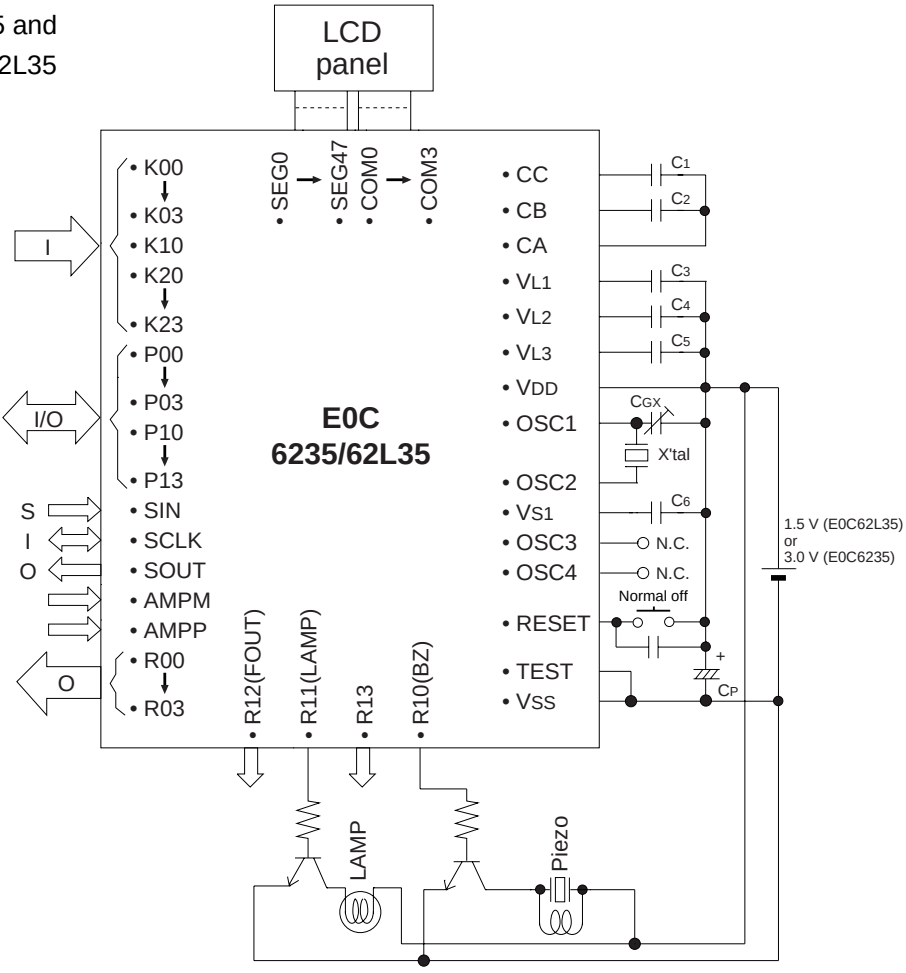
(2) The interrupt factor flags of the clock timer, stopwatch timer and serial interface (TI, SWIT, ISIO) are set when the timing condition is established, even if the interrupt mask registers (ETI, EISWIT, EISIO) are set to "0".

(3) Read out the interrupt factor flags only in the DI status (interrupt flag = "0"). If read-out is performed in the EI status (interrupt flag = "1") a malfunction will result.

(4) Writing to the interrupt mask register only in the DI status (interrupt flag = "0"). Writing to the interrupt mask register while in the EI status (interrupt flag = "1") may cause mulfunction.

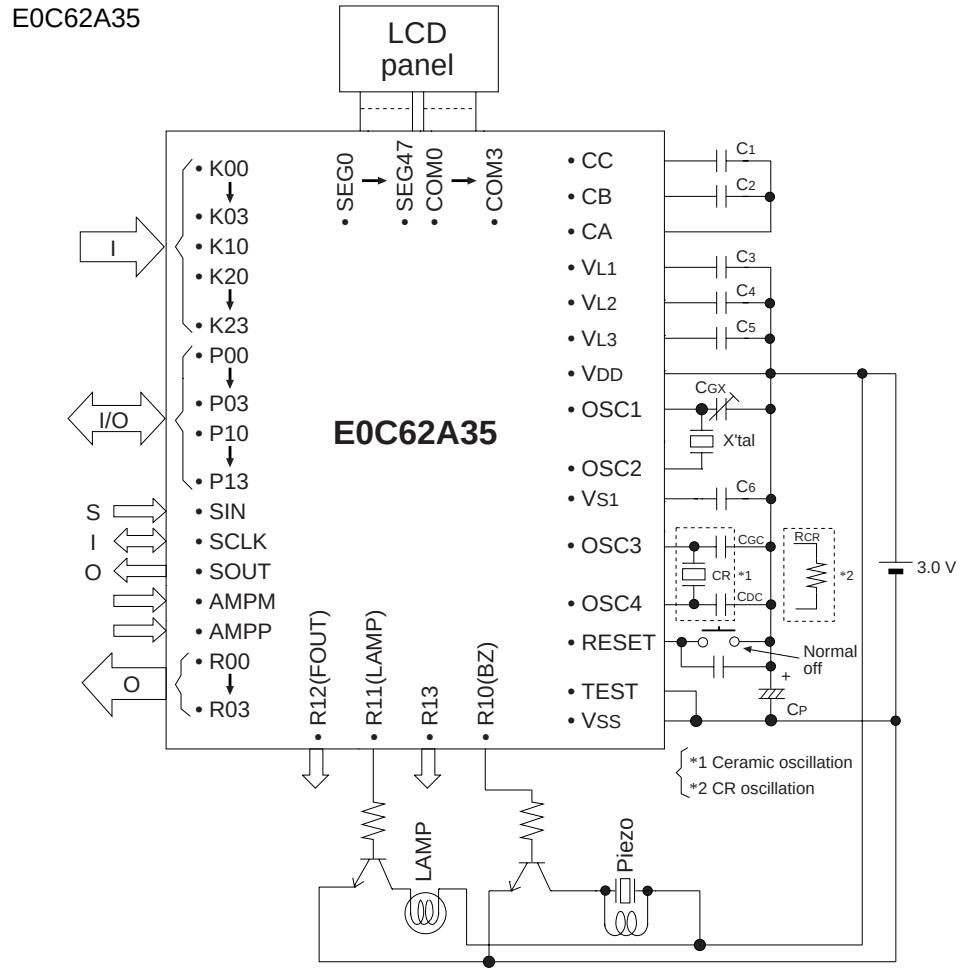
CHAPTER 6 DIAGRAM OF BASIC EXTERNAL CONNECTIONS

E0C6235 and
E0C62L35



X'tal	Crystal oscillator	32,768 Hz or 38,400 Hz CI (MAX)=35 kΩ
C_{GX}	Trimmer capacitor	5–25 pF
C_1		0.1 µF
C_2		0.1 µF
C_3		0.1 µF
C_4		0.1 µF
C_5		0.1 µF
C_6		0.1 µF
C_P		3.3 µF

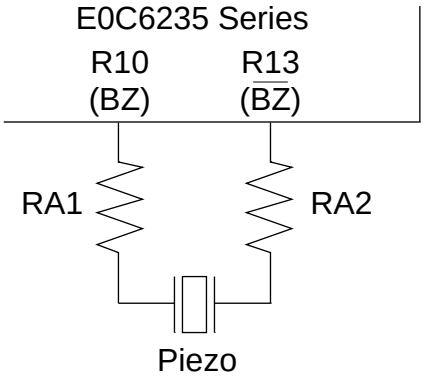
Note The above table is simply an example, and is not guaranteed to work.



X'tal	Crystal oscillator	32,768 Hz or 38,400 Hz CI (MAX)=35 kΩ
C_{GX}	Trimmer capacitor	5–25 pF
CR	Ceramic oscillator	500 kHz
C_{GC}	Gate capacitance	100 pF
C_{DC}	Drain capacitance	100 pF
R_{CR}	Resistance for CR oscillation	82 kΩ
C_1		0.1 µF
C_2		0.1 µF
C_3		0.1 µF
C_4		0.1 µF
C_5		0.1 µF
C_6		0.1 µF
C_P		3.3 µF

Note The above table is simply an example, and is not guaranteed to work.

When the piezoelectric buzzer is driven directly



RA1	Protection resistance	100 Ω
RA2	Protection resistance	100 Ω

CHAPTER 7 ELECTRICAL CHARACTERISTICS

7.1 Absolute Maximum Rating

E0C6235 and E0C62A35

(V_{DD} = 0 V)

Item	Code	Rated value	Unit
Supply voltage	V_{SS}	-5.0 to 0.5	V
Input voltage (1)	V_I	V_{SS}-0.3 to 0.5	V
Input voltage (2)	V_{IOSC}	V_{S1}-0.3 to 0.5	V
Permissible total output current *2	$\sum I_{VSS}$	10	mA
Operating temperature	T_{opr}	-20 to 70	°C
Storage temperature	T_{stg}	-65 to 150	°C
Soldered temperature, time	T_{sol}	260°C, 10 sec (lead section)	–
Permitted loss *1	P_D	250	mW

E0C62L35

(V_{DD} = 0 V)

Item	Code	Rated value	Unit
Supply voltage	V_{SS}	-2.0 to 0.5	V
Input voltage (1)	V_I	V_{SS}-0.3 to 0.5	V
Input voltage (2)	V_{IOSC}	V_{S1}-0.3 to 0.5	V
Permissible total output current *2	$\sum I_{VSS}$	10	mA
Operating temperature	T_{opr}	-20 to 70	°C
Storage temperature	T_{stg}	-65 to 150	°C
Soldered temperature, time	T_{sol}	260°C, 10 sec (lead section)	–
Permitted loss *1	P_D	250	mW

*1 For 100-pin plastic package

*2 The permissible total output current is the sum total of the current (average current) that simultaneously flows from the output pins (or is drawn in).

7.2 Recommended Operating Conditions

E0C6235

(Ta = -20 to 70°C)

Item	Code	Condition	Min.	Typ.	Max.	Unit
Supply voltage	VSS	VDD = 0V	-3.5	-3.0	-1.8	V
Oscillation frequency	fOSC1	Either one	–	32,768	–	Hz
		is selected	–	38,400	–	Hz

E0C62L35

(Ta = -20 to 70°C)

Item	Code	Condition	Min.	Typ.	Max.	Unit
Supply voltage	VSS	VDD = 0V	-1.7	-1.5	-1.1	V
		VDD = 0V Software controllable *1	-1.7	-1.5	-0.9 *2	V
		VDD = 0V When use the analog comparator	-1.7	-1.5	-1.2	V
Oscillation frequency	fOSC1	Either one	–	32,768	–	Hz
		is selected	–	38,400	–	Hz

*1 When switching to heavy load protection mode. (See Section 4.15 for details.)

*2 The possibility of LCD panel display differs depending on the characteristics of the LCD panel.

E0C62A35

(Ta = -20 to 70°C)

Item	Code	Condition	Min.	Typ.	Max.	Unit
Supply voltage	VSS	VDD = 0V	-3.5	-3.0	-2.2	V
Oscillation frequency (1)	fOSC1	Either one	–	32,768	–	Hz
		is selected	–	38,400	–	Hz
Oscillation frequency (2)	fOSC3	duty 50±5%	50	500	600	kHz

7.3 DC Characteristics

E0C6235 and E0C62A35

(V_{DD}=0V, V_{SS}=-3.0V, f_{OSC1}=32,768Hz, Ta=25°C, V_{S1}, V_{L1}, V_{L2}, V_{L3} are internal voltage, C_1=C_2=C_3=C_4=C_5=C_6=0.1µF)

Item	Code	Condition		Min.	Typ.	Max.	Unit
High-level input voltage (1)	V_{IH1}		K00–03·10·20–23 SIN, P00–03·10–13	0.2· V_{SS}		0	V
High-level input voltage (2)	V_{IH2}		SCLK RESET, TEST	0.1· V_{SS}		0	V
Low-level input voltage (1)	V_{IL1}		K00–03·10·20–23 SIN, P00–03·10–13	V_{SS}		0.8· V_{SS}	V
Low-level input voltage (2)	V_{IL2}		SCLK RESET, TEST	V_{SS}		0.9· V_{SS}	V
High-level input current (1)	I_{IH1}	V_{IH}=0V No pull-down resistance	K00–03·10·20–23 P00–03·10–13 SIN, SCLK AMPP, AMPM, RESET	0		0.5	µA
High-level input current (2)	I_{IH2}	V_{IH}=0V With pull-down resistance	K00–03·10·20–23 SIN, SCLK	4		16	µA
High-level input current (3)	I_{H3}	V_{IH}=0V With pull-down resistance	P00–03·10–13 RESET, TEST	25		100	µA
Low-level input current	I_{IL}	V_{IL}=V_{SS}	K00–03·10·20–23 P00–03·10–13 SIN, SCLK, AMPP AMPM, RESET, TEST	-0.5		0	µA
High-level output current (1)	I_{OH1}	V_{OH1}=0.1·V_{SS}	R10, R11, R13			-1.8	mA
High-level output current (2)	I_{OH2}	V_{OH2}=0.1·V_{SS}	R00–03·12 P00–03·10–13 SOUT, SCLK			-0.9	mA
Low-level output current (1)	I_{OL1}	V_{OL1}=0.9·V_{SS}	R10, R11, R13	6.0			mA
Low-level output current (2)	I_{OL2}	V_{OL2}=0.9·V_{SS}	R00–03·12 P00–03·10–13 SOUT, SCLK	3.0			mA
Common output current	I_{OH3}	V_{OH3}=-0.05V	COM0–3			-3	µA
	I_{OL3}	V_{OL3}=V_{L3}+0.05V		3			µA
Segment output current (at LCD output)	I_{OH4}	V_{OH4}=-0.05V	SEG0–47			-3	µA
	I_{OL4}	V_{OL4}=V_{L3}+0.05V		3			µA
Segment output current (at DC output)	I_{OH5}	V_{IH5}=0.1·V_{SS}	SEG0–47			-200	µA
	I_{OL5}	V_{IL5}=0.9·V_{SS}		200			µA

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(V_{DD}=0V, V_{SS}=-1.5V, f_{OSC1}=32,768Hz, Ta=25°C, V_{S1}, V_{L1}, V_{L2}, V_{L3} are internal voltage, C_1=C_2=C_3=C_4=C_5=C_6=0.1µF)

Item	Code	Condition		Min.	Typ.	Max.	Unit
High-level input voltage (1)	V_{IH1}		K00–03·10 P00–03·10–13	0.2·V_{SS}		0	V
High-level input voltage (2)	V_{IH2}		SCLK RESET, TEST	0.1·V_{SS}		0	V
Low-level input voltage (1)	V_{IL1}		K00–03·10 P00–03·10–13	V_{SS}		0.8·V_{SS}	V
Low-level input voltage (2)	V_{IL2}		SCLK RESET, TEST	V_{SS}		0.9·V_{SS}	V
High-level input current (1)	I_{IH1}	V_{IH}=0V No pull-down resistance	K00–03·10·20–23 P00–03·10–13 SIN, SCLK AMPP, AMPM, RESET	0		0.5	µA
High-level input current (2)	I_{IH2}	V_{IH}=0V With pull-down resistance	K00–03·10·20–23 SIN, SCLK	2		10	µA
High-level input current (3)	I_{H3}	V_{IH}=0 With pull-down resistance	P00–03·10–13 RESET, TEST	12		60	µA
Low-level input current	I_{IL}	V_{IL}=V_{SS}	K00–03·10·20–23 P00–03·10–13 SIN, SCLK, AMPP AMPM, RESET, TEST	-0.5		0	µA
High-level output current (1)	I_{OH1}	V_{OH1}=0.1·V_{SS}	R10, R11, R13			-300	µA
High-level output current (2)	I_{OH2}	V_{OH2}=0.1·V_{SS}	R00–03·12 P00–03·10–13 SOUT, SCLK			-150	µA
Low-level output current (1)	I_{OL1}	V_{OL1}=0.9·V_{SS}	R10, R11, R13	1400			µA
Low-level output current (2)	I_{OL2}	V_{OL2}=0.9·V_{SS}	R00–03·12 P00–03·10–13 SOUT, SCLK	700			µA
Common output current	I_{OH3}	V_{OH3}=-0.05V	COM0–3			-3	µA
	I_{OL3}	V_{OL3}=V_{L3}+0.05V		3			µA
Segment output current (at LCD output)	I_{OH4}	V_{OH4}=-0.05V	SEG0–47			-3	µA
	I_{OL4}	V_{OL4}=V_{L3}+0.05V		3			µA
Segment output current (at DC output)	I_{OH5}	V_{IH5}=0.1·V_{SS}	SEG0–47			-100	µA
	I_{OL5}	V_{IL5}=0.9·V_{SS}		100			µA

7.4 Analog Circuit Characteristics and Consumed Current

E0C6235 (Normal operation mode)

(V_{DD}=0V, V_{SS}=-3.0V, f_{OSC1}=32,768Hz, C_G=25pF, Ta=25°C, V_{S1}, V_{L1}, V_{L2}, V_{L3} are internal voltage, C_1=C_2=C_3=C_4=C_5=C_6=0.1µF)

Item	Code	Condition		Min.	Typ.	Max.	Unit
Internal voltage	V_{L1}	Connects a 1MΩ load resistance between V_{DD} and V_{L1} (No panel load)		-1.15	-1.05	-0.95	V
	V_{L2}	Connects a 1MΩ load resistance between V_{DD} and V_{L2} (No panel load)		2·V_{L1} -0.1		2·V_{L1} × 0.9	V
	V_{L3}	Connects a 1MΩ load resistance between V_{DD} and V_{L3} (No panel load)		3·V_{L1} -0.1		3·V_{L1} × 0.9	V
BLD voltage*1	V_{B0}	BLC = "0"		-2.35	-2.20	-2.05	V
	V_{B1}	BLC = "1"		-2.40	-2.25	-2.10	V
	V_{B2}	BLC = "2"		-2.45	-2.30	-2.15	V
	V_{B3}	BLC = "3"		-2.50	-2.35	-2.20	V
	V_{B4}	BLC = "4"		-2.55	-2.40	-2.25	V
	V_{B5}	BLC = "5"		-2.60	-2.45	-2.30	V
	V_{B6}	BLC = "6"		-2.65	-2.50	-2.35	V
	V_{B7}	BLC = "7"		-2.70	-2.55	-2.40	V
BLD circuit response time	t_B					100	µsec
Sub-BLD voltage	V_{BS}			-2.55	-2.40	-2.25	V
Sub-BLD circuit response time	t_{BS}					100	µsec
Analog comparator input voltage	V_{IP}	Noninverted input (AMPP)		V_{SS}+0.3		V_{DD}-0.9	V
	V_{IM}	Inverted input (AMPM)					
Analog comparator offset voltage	V_{OF}					10	mV
Analog comparator response time	t_{AMP}	V_{IP} = -1.5V V_{IM} = V_{IP}±15mV				3	msec
Consumed current	I_{OP}	During HALT	No panel load		1.8	4.0	µA
		During operation*2			6.0	10.0	µA

*1 The relationships among V_{B0}–V_{B7} are V_{B0}>V_{B1}>V_{B2}>...V_{B5}>V_{B6}>V_{B7}.

*2 The BLD circuit, sub-BLD circuit and analog comparator are in the OFF status.

E0C6235 (Heavy load protection mode)

(V_{DD}=0V, V_{SS}=-3.0V, f_{OSC1}=32,768Hz, C_G=25pF, Ta=25°C, V_{S1}, V_{L1}, V_{L2}, V_{L3} are internal voltage, C_1=C_2=C_3=C_4=C_5=C_6=0.1µF)

Item	Code	Condition		Min.	Typ.	Max.	Unit
Internal voltage	V_{L1}	Connects a 1MΩ load resistance between V_{DD} and V_{L1} (No panel load)		-1.15	-1.05	-0.95	V
	V_{L2}	Connects a 1MΩ load resistance between V_{DD} and V_{L2} (No panel load)		2·V_{L1} -0.1		2·V_{L1} × 0.9	V
	V_{L3}	Connects a 1MΩ load resistance between V_{DD} and V_{L3} (No panel load)		3·V_{L1} -0.1		3·V_{L1} × 0.9	V
BLD voltage*1	V_{B0}	BLC = "0"		-2.35	-2.20	-2.05	V
	V_{B1}	BLC = "1"		-2.40	-2.25	-2.10	V
	V_{B2}	BLC = "2"		-2.45	-2.30	-2.15	V
	V_{B3}	BLC = "3"		-2.50	-2.35	-2.20	V
	V_{B4}	BLC = "4"		-2.55	-2.40	-2.25	V
	V_{B5}	BLC = "5"		-2.60	-2.45	-2.30	V
	V_{B6}	BLC = "6"		-2.65	-2.50	-2.35	V
	V_{B7}	BLC = "7"		-2.70	-2.55	-2.40	V
BLD circuit response time	t_B					100	µsec
Sub-BLD voltage	V_{BS}			-2.55	-2.40	-2.25	V
Sub-BLD circuit response time	t_{BS}					100	µsec
Analog comparator input voltage	V_{IP}	Noninverted input (AMPP)		V_{SS}+0.3		V_{DD}-0.9	V
	V_{IM}	Inverted input (AMPM)					
Analog comparator offset voltage	V_{OF}					10	mV
Analog comparator response time	t_{AMP}	V_{IP} = -1.5V V_{IM} = V_{IP}±15mV				3	msec
Consumed current	I_{OP}	During HALT	No panel load		35	90	µA
		During operation*2			40	100	µA

*1 The relationships among V_{B0}–V_{B7} are V_{B0}>V_{B1}>V_{B2}>...V_{B5}>V_{B6}>V_{B7}.

*2 The BLD circuit and sub-BLD circuit are in the ON status (HLMOD = "1", BLS = "0"). The analog comparator is in the OFF status.

E0C62L35 (Normal operation mode)

(V_{DD}=0V, V_{SS}=-1.5V, f_{OSC1}=32,768Hz, C_G=25pF, Ta=25°C, V_{S1}, V_{L1}, V_{L2}, V_{L3} are internal voltage, C_1=C_2=C_3=C_4=C_5=C_6=0.1µF)

Item	Code	Condition		Min.	Typ.	Max.	Unit
Internal voltage	V_{L1}	Connects a 1MΩ load resistance between V_{DD} and V_{L1} (No panel load)		-1.15	-1.05	-0.95	V
	V_{L2}	Connects a 1MΩ load resistance between V_{DD} and V_{L2} (No panel load)		2·V_{L1} -0.1		2·V_{L1} × 0.9	V
	V_{L3}	Connects a 1MΩ load resistance between V_{DD} and V_{L3} (No panel load)		3·V_{L1} -0.1		3·V_{L1} × 0.9	V
BLD voltage*1	V_{B0}	BLC = "0"		-1.15	-1.05	-0.95	V
	V_{B1}	BLC = "1"		-1.20	-1.10	-1.00	V
	V_{B2}	BLC = "2"		-1.25	-1.15	-1.05	V
	V_{B3}	BLC = "3"		-1.30	-1.20	-1.10	V
	V_{B4}	BLC = "4"		-1.35	-1.25	-1.15	V
	V_{B5}	BLC = "5"		-1.40	-1.30	-1.20	V
	V_{B6}	BLC = "6"		-1.45	-1.35	-1.25	V
	V_{B7}	BLC = "7"		-1.50	-1.40	-1.30	V
BLD circuit response time	t_B					100	µsec
Sub-BLD voltage	V_{BS}			-1.30	-1.20	-1.10	V
Sub-BLD circuit response time	t_{BS}					100	µsec
Analog comparator input voltage	V_{IP}	Noninverted input (AMPP)		V_{SS}+0.3		V_{DD}-0.9	V
	V_{IM}	Inverted input (AMPM)					
Analog comparator offset voltage	V_{OF}					20	mV
Analog comparator response time	t_{AMP}	V_{IP} = -1.1V V_{IM} = V_{IP}±30mV				3	msec
Consumed current	I_{OP}	During HALT	No panel load		1.5	3.0	µA
		During operation*2			5.0	8.0	µA

*1 The relationships among V_{B0}–V_{B7} are V_{B0}>V_{B1}>V_{B2}>...V_{B5}>V_{B6}>V_{B7}.

*2 The BLD circuit, sub-BLD circuit and analog comparator are in the OFF status.

E0C62L35 (Heavy load protection mode)

(V_{DD}=0V, V_{SS}=-1.5V, f_{OSC1}=32,768Hz, C_G=25pF, Ta=25°C, V_{S1}, V_{L1}, V_{L2}, V_{L3} are internal voltage, C_1=C_2=C_3=C_4=C_5=C_6=0.1µF)

Item	Code	Condition		Min.	Typ.	Max.	Unit
Internal voltage	V_{L1}	Connects a 1MΩ load resistance between V_{DD} and V_{L1} (No panel load)		-1.15	-1.05	-0.95	V
	V_{L2}	Connects a 1MΩ load resistance between V_{DD} and V_{L2} (No panel load)		2·V_{L1} -0.1		2·V_{L1} × 0.85	V
	V_{L3}	Connects a 1MΩ load resistance between V_{DD} and V_{L3} (No panel load)		3·V_{L1} -0.1		3·V_{L1} × 0.85	V
BLD voltage*1	V_{B0}	BLC = "0"		-1.15	-1.05	-0.95	V
	V_{B1}	BLC = "1"		-1.20	-1.10	-1.00	V
	V_{B2}	BLC = "2"		-1.25	-1.15	-1.05	V
	V_{B3}	BLC = "3"		-1.30	-1.20	-1.10	V
	V_{B4}	BLC = "4"		-1.35	-1.25	-1.15	V
	V_{B5}	BLC = "5"		-1.40	-1.30	-1.20	V
	V_{B6}	BLC = "6"		-1.45	-1.35	-1.25	V
	V_{B7}	BLC = "7"		-1.50	-1.40	-1.30	V
BLD circuit response time	t_B					100	µsec
Sub-BLD voltage	V_{BS}			-1.30	-1.20	-1.10	V
Sub-BLD circuit response time	t_{BS}					100	µsec
Analog comparator input voltage	V_{IP}	Noninverted input (AMPP)		V_{SS}+0.3		V_{DD}-0.9	V
	V_{IM}	Inverted input (AMPM)					
Analog comparator offset voltage	V_{OF}					20	mV
Analog comparator response time	t_{AMP}	V_{IP} = -1.1V V_{IM} = V_{IP}±30mV				3	msec
Consumed current	I_{OP}	During HALT	No panel load		3.0	7.0	µA
		During operation*2			10.0	18.0	µA

*1 The relationships among V_{B0}–V_{B7} are V_{B0}>V_{B1}>V_{B2}>...V_{B5}>V_{B6}>V_{B7}.

*2 The BLD circuit and sub-BLD circuit are in the ON status (HLMOD = "1", BLS = "0"). The analog comparator is in the OFF status.

E0C62A35 (Normal operation mode)

(V_{DD}=0V, V_{SS}=-3.0V, f_{OSC1}=32,768Hz, C_G=25pF, Ta=25°C, V_{S1}, V_{L1}, V_{L2}, V_{L3} are internal voltage, C_1=C_2=C_3=C_4=C_5=C_6=0.1µF)

Item	Code	Condition		Min.	Typ.	Max.	Unit
Internal voltage	V_{L1}	Connects a 1MΩ load resistance between V_{DD} and V_{L1} (No panel load)		-1.15	-1.05	-0.95	V
	V_{L2}	Connects a 1MΩ load resistance between V_{DD} and V_{L2} (No panel load)		2·V_{L1} -0.1		2·V_{L1} × 0.9	V
	V_{L3}	Connects a 1MΩ load resistance between V_{DD} and V_{L3} (No panel load)		3·V_{L1} -0.1		3·V_{L1} × 0.9	V
BLD voltage*1	V_{B0}	BLC = "0"		-2.35	-2.20	-2.05	V
	V_{B1}	BLC = "1"		-2.40	-2.25	-2.10	V
	V_{B2}	BLC = "2"		-2.45	-2.30	-2.15	V
	V_{B3}	BLC = "3"		-2.50	-2.35	-2.20	V
	V_{B4}	BLC = "4"		-2.55	-2.40	-2.25	V
	V_{B5}	BLC = "5"		-2.60	-2.45	-2.30	V
	V_{B6}	BLC = "6"		-2.65	-2.50	-2.35	V
	V_{B7}	BLC = "7"		-2.70	-2.55	-2.40	V
BLD circuit response time	t_B					100	µsec
Sub-BLD voltage	V_{BS}			-2.55	-2.40	-2.25	V
Sub-BLD circuit response time	t_{BS}					100	µsec
Analog comparator input voltage	V_{IP}	Noninverted input (AMPP)		V_{SS}+0.3		V_{DD}-0.9	V
	V_{IM}	Inverted input (AMPM)					
Analog comparator offset voltage	V_{OF}					10	mV
Analog comparator response time	t_{AMP}	V_{IP} = -1.5V V_{IM} = V_{IP}±15mV				3	msec
Consumed current	I_{OP}	During HALT	No panel load		2.0	5.0	µA
		During operation*2			8.0	15	µA
		During operation at 500kHz*2			130	300	µA

*1 The relationships among V_{B0}–V_{B7} are V_{B0}>V_{B1}>V_{B2}>...V_{B5}>V_{B6}>V_{B7}.

*2 The BLD circuit, sub-BLD circuit and analog comparator are in the OFF status.

E0C62A35 (Hevy load protection mode)

(V_{DD}=0V, V_{SS}=-3.0V, f_{OSC1}=32,768Hz, C_G=25pF, Ta=25°C, V_{S1}, V_{L1}, V_{L2}, V_{L3} are internal voltage, C_1=C_2=C_3=C_4=C_5=C_6=0.1µF)

Item	Code	Condition		Min.	Typ.	Max.	Unit
Internal voltage	V_{L1}	Connects a 1MΩ load resistance between V_{DD} and V_{L1} (No panel load)		-1.15	-1.05	-0.95	V
	V_{L2}	Connects a 1MΩ load resistance between V_{DD} and V_{L2} (No panel load)		2·V_{L1} -0.1		2·V_{L1} × 0.9	V
	V_{L3}	Connects a 1MΩ load resistance between V_{DD} and V_{L3} (No panel load)		3·V_{L1} -0.1		3·V_{L1} × 0.9	V
BLD voltage*1	V_{B0}	BLC = "0"		-2.35	-2.20	-2.05	V
	V_{B1}	BLC = "1"		-2.40	-2.25	-2.10	V
	V_{B2}	BLC = "2"		-2.45	-2.30	-2.15	V
	V_{B3}	BLC = "3"		-2.50	-2.35	-2.20	V
	V_{B4}	BLC = "4"		-2.55	-2.40	-2.25	V
	V_{B5}	BLC = "5"		-2.60	-2.45	-2.30	V
	V_{B6}	BLC = "6"		-2.65	-2.50	-2.35	V
	V_{B7}	BLC = "7"		-2.70	-2.55	-2.40	V
BLD circuit response time	t_B					100	µsec
Sub-BLD voltage	V_{BS}			-2.55	-2.40	-2.25	V
Sub-BLD circuit response time	t_{BS}					100	µsec
Analog comparator input voltage	V_{IP}	Noninverted input (AMPP)		V_{SS}+0.3		V_{DD}-0.9	V
	V_{IM}	Inverted input (AMPM)					
Analog comparator offset voltage	V_{OF}					10	mV
Analog comparator response time	t_{AMP}	V_{IP} = -1.5V V_{IM} = V_{IP}±15mV				3	msec
Consumed current	I_{OP}	During HALT	No panel load		22	40	µA
		During operation*2			28	50	µA
		During operation at 500kHz*2			150	350	µA

*1 The relationships among V_{B0}–V_{B7} are V_{B0}>V_{B1}>V_{B2}>...V_{B5}>V_{B6}>V_{B7}.

*2 The BLD circuit and sub-BLD circuit are in the ON status (HLMOD = "1", BLS = "0"). The analog comparator is in the OFF status.

7.5 Oscillation Characteristics

The oscillation characteristics change depending on the conditions (components used, board pattern, etc.). Use the following characteristics as reference values.

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If no special requirement

V_{DD}=0V, V_{SS}=-3.0V, Crystal: C-002R (CI=35kΩ), C_G=25pF, C_D=built-in, Ta=25°C

Item	Code	Condition	Min.	Typ.	Max.	Unit
Oscillation start voltage	V_{sta} (V_{SS})	t_{sta}≤5sec	-1.8			V
Oscillation stop voltage	V_{stp} (V_{SS})	t_{stp}≤10sec	-1.8			V
Built-in capacitance (drain)	C_D	Including incidental capacitance inside IC		20		pF
Frequency/voltage deviation	f/V	V_{SS} = -1.8 to -3.5V			5	ppm
Frequency/IC deviation	f/I_C		-10		10	ppm
Frequency adjustment range	f/C_G	C_G = 5 to 25pF	35	45		ppm
Harmonic oscillation start voltage	V_{hho} (V_{SS})				-3.5	V
Permitted leak resistance	R_{leak}	Between OSC1 and V_{DD}, V_{SS}	200			MΩ

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If no special requirement

V_{DD}=0V, V_{SS}=-1.5V, Crystal: C-002R (CI=35kΩ), C_G=25pF, C_D=built-in, Ta=25°C

Item	Code	Condition	Min.	Typ.	Max.	Unit
Oscillation start voltage	V_{sta} (V_{SS})	t_{sta}≤5sec	-1.1			V
Oscillation stop voltage	V_{stp} (V_{SS})	t_{stp}≤10sec	-1.1 (-0.9)*1			V
Built-in capacitance (drain)	C_D	Including incidental capacitance inside IC		20		pF
Frequency/voltage deviation	f/V	V_{SS} = -1.1 to -1.7V (-0.9)*1			5	ppm
Frequency/IC deviation	f/I_C		-10		10	ppm
Frequency adjustment range	f/C_G	C_G = 5 to 25pF	35	45		ppm
Harmonic oscillation start voltage	V_{hho} (V_{SS})				-1.7	V
Permitted leak resistance	R_{leak}	Between OSC1 and V_{DD}, V_{SS}	200			MΩ

*1 Parentheses indicate value for operation in heavy load protection mode.

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OSC1, 2

If no special requirement

V_{DD}=0V, V_{SS}=-3.0V, Crystal: C-002R (CI=35kΩ), C_G=25pF, C_D=built-in, Ta=25°C

Item	Code	Condition	Min.	Typ.	Max.	Unit
Oscillation start voltage	V_{sta} (V_{SS})	t_{sta}≤5sec	-2.2			V
Oscillation stop voltage	V_{stp} (V_{SS})	t_{stp}≤10sec	-2.2			V
Built-in capacitance (drain)	C_D	Including incidental capacitance inside IC		20		pF
Frequency/voltage deviation	f/V	V_{SS} = -2.2 to -3.5V			5	ppm
Frequency/IC deviation	f/I$_C$		-10		10	ppm
Frequency adjustment range	f/C_G	C_G = 5 to 25pF	35	45		ppm
Harmonic oscillation start voltage	V_{hho} (V_{SS})				-3.5	V
Permitted leak resistance	R_{leak}	Between OSC1 and V_{DD}, V_{SS}	200			MΩ

OSC3, OSC4 (for CR oscillation circuit)

If no special requirement

V_{DD}=0V, V_{SS}=-3.0V, R_{CR}=82kΩ, Ta=25°C

Item	Code	Condition	Min.	Typ.	Max.	Unit
Oscillation frequency	f_{OSC3}		-30	480 kHz	30	%
Oscillation start voltage	V_{sta}		-2.2			V
Oscillation start time	t_{sta}	V_{SS} = -2.2 to -3.5V			3	msec
Oscillation stop voltage	V_{stp}		-2.2			V

OSC3, OSC4 (for ceramic oscillation circuit)

If no special requirement

V_{DD}=0V, V_{SS}=-3.0V, ceramic oscillation: 500kHz

C_{GC}=C_{DC}=100pF, Ta=25°C

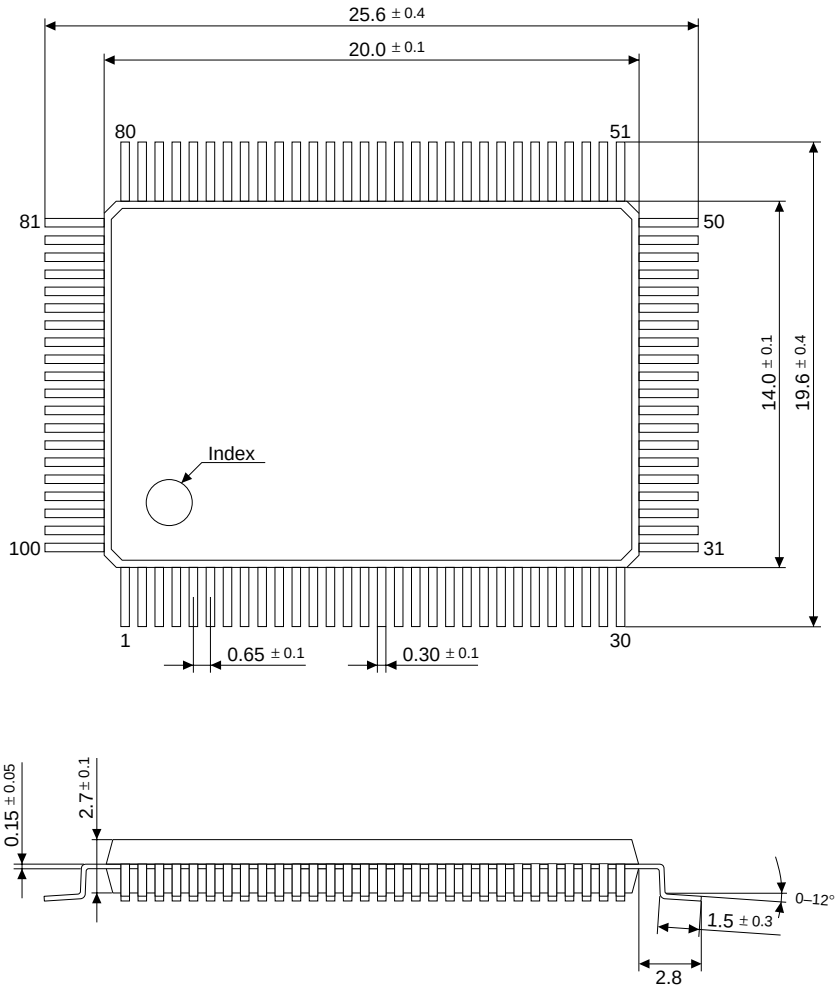
Item	Code	Condition	Min.	Typ.	Max.	Unit
Oscillation start voltage	V_{sta}		-2.2			V
Oscillation start time	t_{sta}	V_{SS} = -2.2 to -3.5V			5	msec
Oscillation stop voltage	V_{stp}		-2.2			V

CHAPTER 8 PACKAGE

8.1 Plastic Package

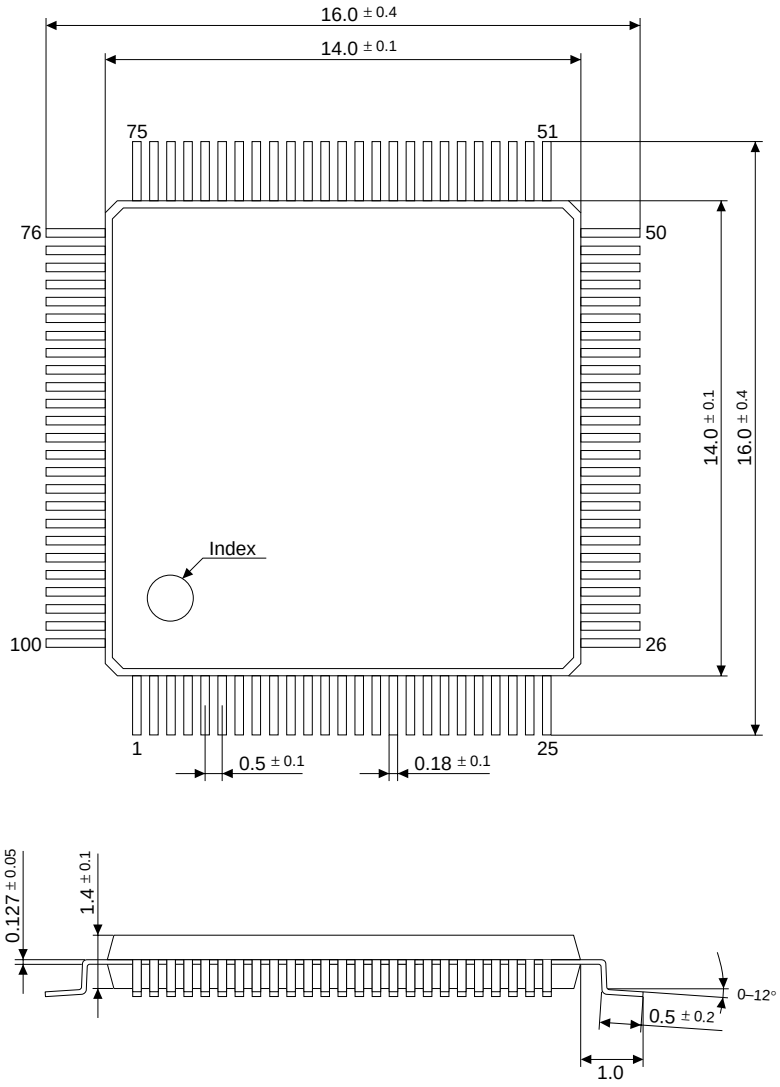
F100-5

100-pin Flat Package
(Unit: mm)



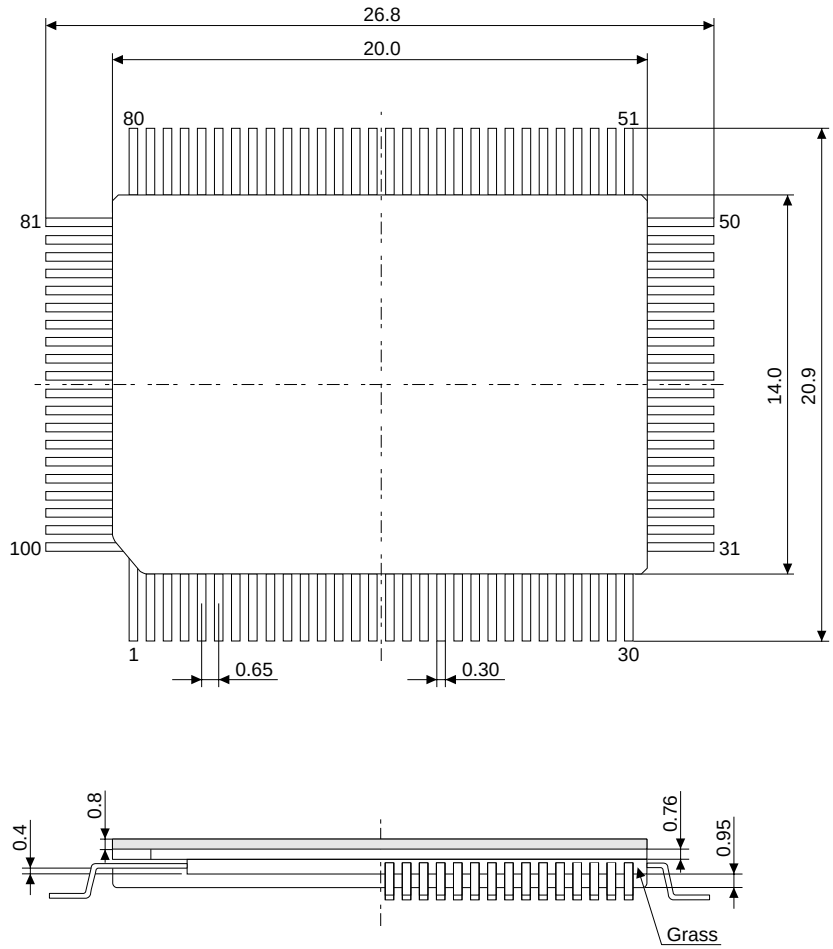
F100-15

100-pin Flat Package
(Unit: mm)



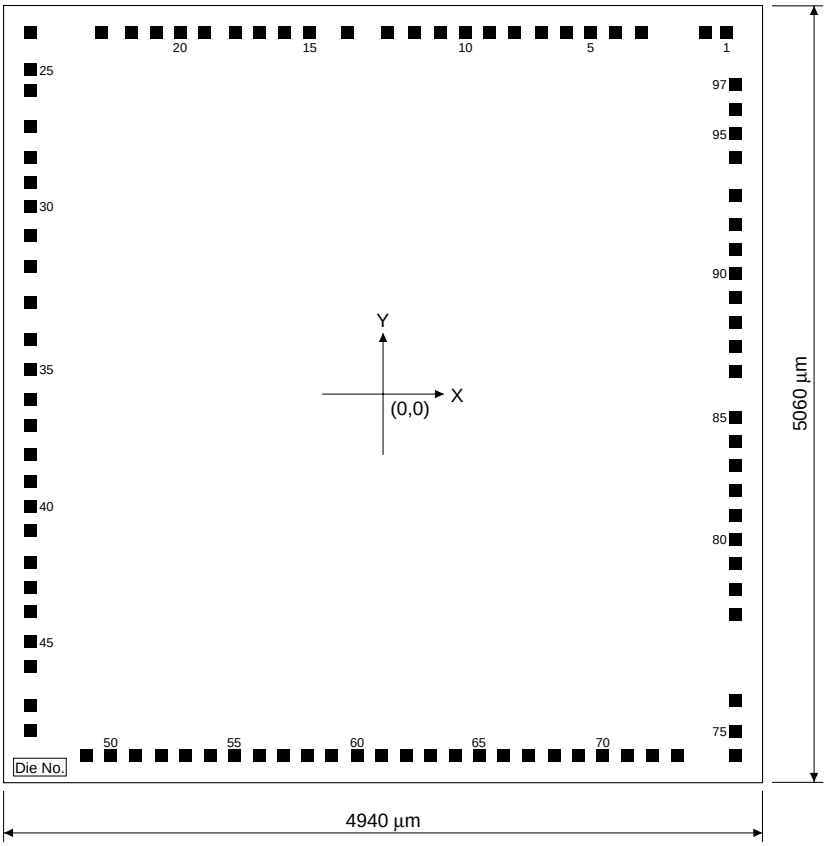
8.2 Ceramic Package for Test Samples

(Unit: mm)



CHAPTER 9 PAD LAYOUT

9.1 Diagram of Pad Layout



Chip thickness: 400 µm
Pad opening: 95 µm

9.2 Pad Coordinates

(Unit: μm)

PAD		COORDINATE		PAD		COORDINATE		PAD		COORDINATE	
No	NAME	X	Y	No	NAME	X	Y	No	NAME	X	Y
1	AMPP	2235	2355	34	OSC3	-2295	357	67	SEG29	951	-2355
2	AMPM	2010	2355	35	V_{S1}	-2295	161	68	SEG28	1111	-2355
3	K23	1680	2355	36	OSC2	-2295	-43	69	SEG27	1271	-2355
4	K22	1511	2355	37	OSC1	-2295	-203	70	SEG26	1431	-2355
5	K21	1351	2355	38	V_{DD}	-2295	-391	71	SEG25	1591	-2355
6	K20	1191	2355	39	V_{L3}	-2295	-571	72	SEG24	1751	-2355
7	K10	1031	2355	40	V_{L2}	-2295	-731	73	TEST	1921	-2355
8	K03	855	2355	41	V_{L1}	-2295	-891	74	SEG23	2295	-2355
9	K02	695	2355	42	CA	-2295	-1099	75	SEG22	2295	-2195
10	K01	535	2355	43	CB	-2295	-1259	76	SEG21	2295	-1992
11	K00	375	2355	44	CC	-2295	-1419	77	SEG20	2295	-1427
12	SIN	199	2355	45	COM3	-2295	-1611	78	SEG19	2295	-1267
13	SOUT	28	2355	46	COM2	-2295	-1771	79	SEG18	2295	-1107
14	SCLK	-232	2355	47	COM1	-2295	-2028	80	SEG17	2295	-947
15	P03	-481	2355	48	COM0	-2295	-2188	81	SEG16	2295	-787
16	P02	-641	2355	49	SEG47	-1929	-2355	82	SEG15	2295	-627
17	P01	-801	2355	50	SEG46	-1769	-2355	83	SEG14	2295	-467
18	P00	-961	2355	51	SEG45	-1609	-2355	84	SEG13	2295	-307
19	P13	-1160	2355	52	SEG44	-1449	-2355	85	SEG12	2295	-147
20	P12	-1320	2355	53	SEG43	-1289	-2355	86	SEG11	2295	149
21	P11	-1480	2355	54	SEG42	-1129	-2355	87	SEG10	2295	309
22	P10	-1640	2355	55	SEG41	-969	-2355	88	SEG9	2295	469
23	R03	-1832	2355	56	SEG40	-809	-2355	89	SEG8	2295	629
24	R02	-2295	2355	57	SEG39	-649	-2355	90	SEG7	2295	789
25	R01	-2295	2136	58	SEG38	-489	-2355	91	SEG6	2295	949
26	R00	-2295	1976	59	SEG37	-329	-2355	92	SEG5	2295	1109
27	R12	-2295	1741	60	SEG36	-169	-2355	93	SEG4	2295	1269
28	R11	-2295	1541	61	SEG35	-9	-2355	94	SEG3	2295	1538
29	R10	-2295	1381	62	SEG34	151	-2355	95	SEG2	2295	1698
30	R13	-2295	1221	63	SEG33	311	-2355	96	SEG1	2295	1858
31	V_{SS}	-2295	1033	64	SEG32	471	-2355	97	SEG0	2295	2018
32	RESET	-2295	834	65	SEG31	631	-2355				
33	OSC4	-2295	597	66	SEG30	791	-2355				

II. E0C6235 Technical Software

CONTENTS

CHAPTER 1 OVERVIEW

The E0C6235 Series is a single-chip microcomputer made up of the 4-bit core CPU E0C6200, ROM (4,096 words, 12 bits to a word), RAM 576 words, 4 bits to a word) LCD driver circuit, serial interface, event counter with dial input functions, watchdog timer, and two types of time base counter. Because of its low-voltage operation and low power consumption, this series is ideal for a wide range of applications, and is especially suitable for battery-driven systems.

• Configuration

The E0C6235 Series is configured as follows, depending on supply voltage and oscillation circuits.

Model	E0C6235	E0C62L35	E0C62A35
Supply voltage	3.0 V	1.5 V	3.0 V
Oscillation circuit	OSC1 only (Single clock)	OSC1 only (Single clock)	OSC1 and OSC3 (Twin clock)

CHAPTER 2 BLOCK DIAGRAM

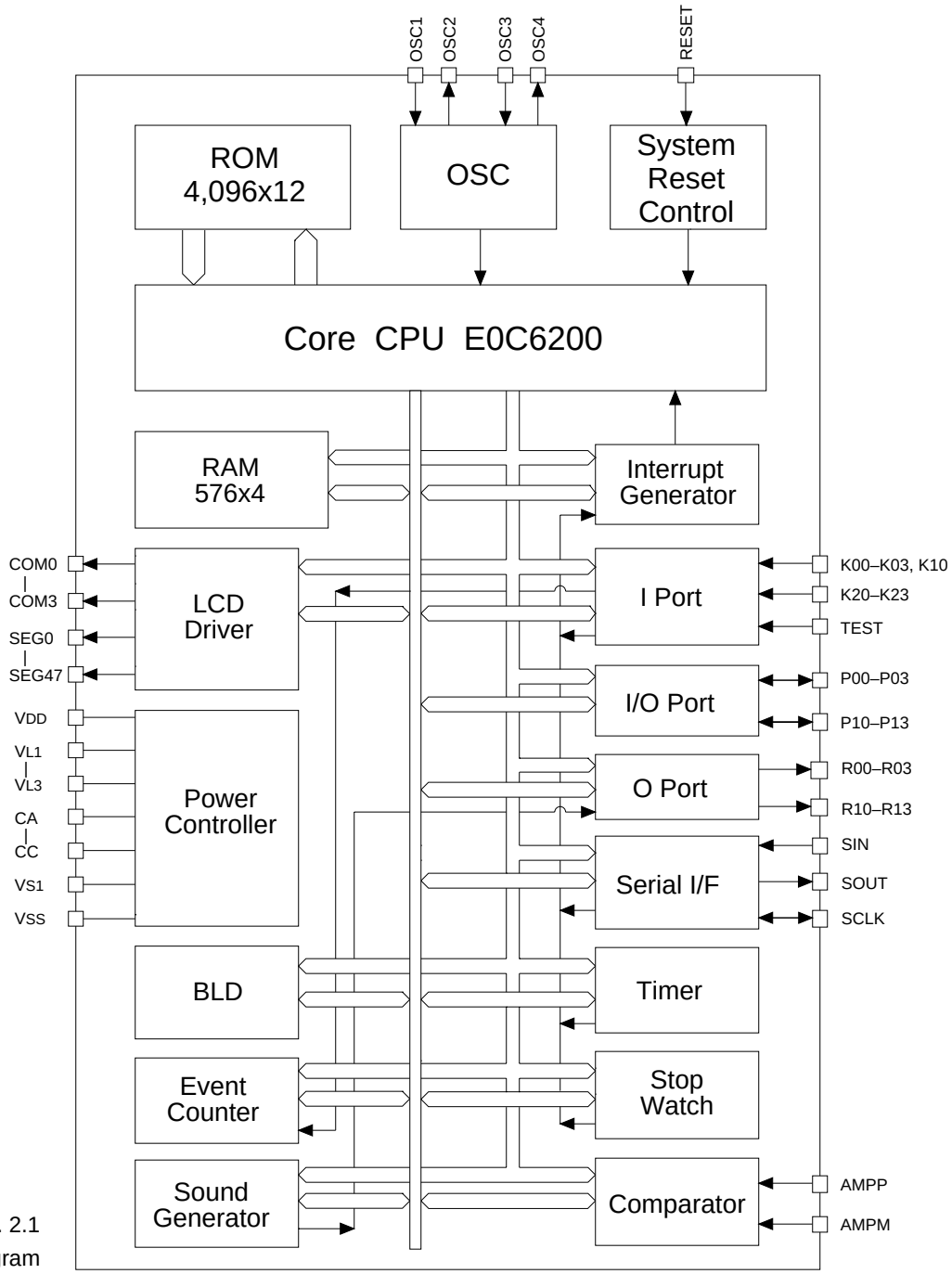


Fig. 2.1
Block diagram

CHAPTER 3 PROGRAM MEMORY (ROM)

3.1 Configuration of ROM

The built-in ROM, a mask ROM for loading the program, has a capacity of 4,096 steps, 12 bits each. The program area is 16 pages (0–15), each of 256 steps (00H–FFH). After initial reset, the program beginning address is page 1, step 00H. The interrupt vector is allocated to page 1, steps 01H–0FH.

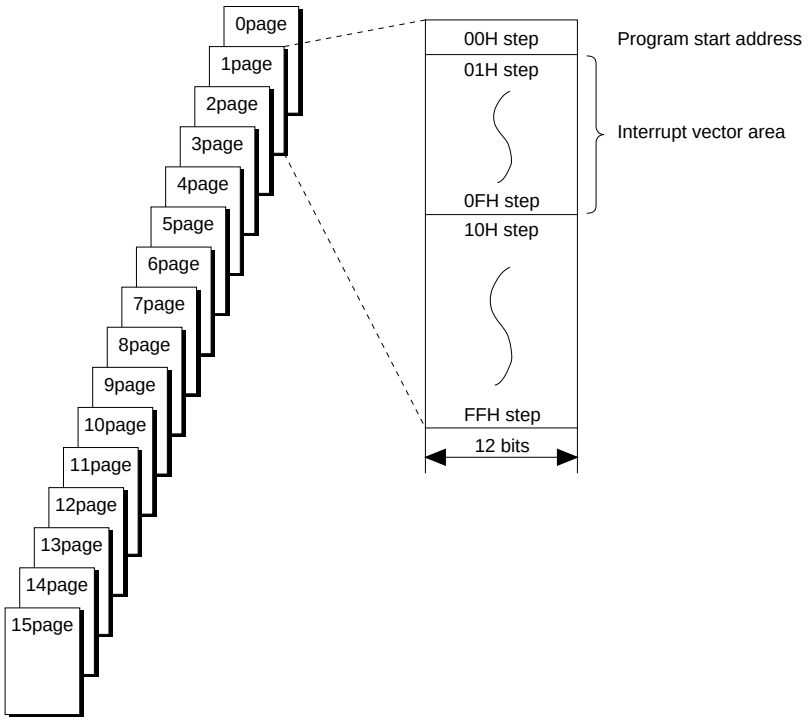


Fig. 3.1.1
Configuration of ROM

3.2 Interrupt Vector

When an interrupt request is input to the CPU, the CPU begins interrupt processing. After the program being executed is terminated, the interrupt processing is executed in the following order.

① The address data (value of program counter) of the program to be executed next is saved in the stack area (RAM).

② The interrupt request causes the value of the interrupt vector (page 1, 01H–0FH) to be set in the program counter.

③ The program at the specified address is executed (execution of interrupt processing routine by software).

Table 3.2.1 shows the correspondence of interrupt requests and interrupt vectors.

Note *The processing in ① and ② above take 12 cycles of the CPU system clock.*

Table 3.2.1
Interrupt request and interrupt vectors

PC	Value	Interrupt request	
PCS3	1	Stopwatch interrupt	Enabled
	0	Stopwatch interrupt	Masked
PCS2	1	Timer interrupt	Enabled
	0	Timer interrupt	Masked
PCS1	1	Input (K00–K03) interrupt or Input (K10) interrupt or Input (K20–K23) interrupt	Enabled
	0	Input (K00–K03) interrupt and Input (K10) interrupt and Input (K20–K23) interrupt	Masked
PCS0	1	Serial interface interrupt	Enabled
	0	Serial interface interrupt	Masked

* The four low-order bits of the program counter are indirectly addressed through the interrupt request.

CHAPTER 4 DATA MEMORY
(RAM, DISPLAY MEMORY, I/O MEMORY)

4.1 Configuration of Data Memory

Data memory of the E0C6235 Series has an address space of 608 words (656 words when segment data memory is laid out over two pages), of which 48 words are allocated to display memory and 32 words to I/O memory.
Figures 4.1.1(a)–(c) present the overall data memory maps of the E0C6235 Series, and Tables 4.2.1(a)–(c) the peripheral circuits' (I/O space) memory maps.

Address Page	Low / High	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	0	M0	M1	M2	M3	M4	M5	M6	M7	M8	M9	MA	MB	MC	MD	ME	MF
	1	RAM (256 words x 4 bits) R/W															
	2																
	3																
	4																
	5																
	6																
	7																
	8																
	9																
	A																
	B																
	C																
	D																
	E																
	F																
1	0	RAM (256 words x 4 bits) R/W															
	1																
	2																
	3																
	4																
	5																
	6																
	7																
	8																
	9																
	A																
	B																
	C																
	D																
	E																
	F																

Fig. 4.1.1(a)
Data memory map
(page 0, page 1)

Address Page	Low / High	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
2	0	RAM (64 words x 4 bits) R/W															
	1																
	2																
	3																
	4	Unused area															
	5																
	6																
	7																
	8																
	9																
	A																
	B																
	C																
	D																
	E	I/O memory [See Tables 4.2.1(a)–(c)]															
	F																

Fig. 4.1.1(b)
Data memory map
(page 2)

Address Page	Low / High	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0 or 2	4	Display memory (48 words x 4 bits) R/W (W)															
	5																
	6																

Fig. 4.1.1(c)
Data memory map
(segment area)

Notes (1) See Tables 4.2.1(a)–(c) for details of I/O memory.

(2) The mask option can be used to select whether to assign the overall area of display memory to page 0 or page 2.

When page 0 (040H–06FH) is selected, read/write is enabled. When page 2 (240H–26FH) is selected, write only is enabled.

If page 0 is assigned, RAM (040H–06FH) is 48 words, and is used as the segment area.

(3) Memory is not mounted in unused area within the memory map and in memory area not indicated in this chapter. For this reason, normal operation cannot be assured for programs that have been prepared with access to these areas.

4.2 I/O Memory Map

Table 4.2.1(a) I/O memory map (2E0H–2EDH)

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
2E0H	TM3	TM2	TM1	TM0	TM3	0			Timer data (clock timer 2 Hz)
					TM2	0			Timer data (clock timer 4 Hz)
	R				TM1	0			Timer data (clock timer 8 Hz)
					TM0	0			Timer data (clock timer 16 Hz)
2E1H	SWL3	SWL2	SWL1	SWL0	SWL3	0			MSB
					SWL2	0			Stopwatch timer data 1/100 sec (BCD)
	R				SWL1	0			
					SWL0	0			LSB
2E2H	SWH3	SWH2	SWH1	SWH0	SWH3	0			MSB
					SWH2	0			Stopwatch timer data 1/10 sec (BCD)
					SWH1	0			
					SWH0	0			LSB
2E3H	K03	K02	K01	K00	K03	– *2	High	Low	Input port data (K00–K03)
					K02	– *2	High	Low	
	R				K01	– *2	High	Low	
					K00	– *2	High	Low	
2E4H	KCP03	KCP02	KCP01	KCP00	KCP03	0	↓	↑	Input comparison register (K00–K03)
					KCP02	0	↓	↑	
	R/W				KCP01	0	↓	↑	
					KCP00	0	↓	↑	
2E5H	EIK03	EIK02	EIK01	EIK00	EIK03	0	Enable	Mask	Interrupt mask register (K00–K03)
					EIK02	0	Enable	Mask	
	R/W				EIK01	0	Enable	Mask	
					EIK00	0	Enable	Mask	
2E6H	HLMOD	BLD0	EISWIT1	EISWIT0	HLMOD	0	Heavy load	Normal	Heavy load protection mode register
					BLD0	0	Low	Normal	Sub-BLD evaluation data
	R/W	R	R/W		EISWIT1	0	Enable	Mask	Interrupt mask register (stopwatch 1 Hz)
					EISWIT0	0	Enable	Mask	Interrupt mask register (stopwatch 10 Hz)
2E7H	SCTRG	EIK10	KCP10	K10	SCTRG*3	–	Trigger	–	Serial interface clock trigger
					EIK10	0	Enable	Mask	Interrupt mask register (K10)
	W	R/W		R	KCP10	0	↓	↑	Input comparison register (K10)
					K10	– *2	High	Low	Input port data (K10)
2E8H	CSDC	ETI2	ETI8	ETI32	CSDC	0	Static	Dynamic	LCD drive switch
					ETI2	0	Enable	Mask	Interrupt mask register (clock timer 2 Hz)
	R/W				ETI8	0	Enable	Mask	Interrupt mask register (clock timer 8 Hz)
					ETI32	0	Enable	Mask	Interrupt mask register (clock timer 32 Hz)
2E9H	0	TI2	TI8	TI32	0 *3	– *2	–	–	Unused
					TI2 *4	0	Yes	No	Interrupt factor flag (clock timer 2 Hz)
	R				TI8 *4	0	Yes	No	Interrupt factor flag (clock timer 8 Hz)
					TI32 *4	0	Yes	No	Interrupt factor flag (clock timer 32 Hz)
2EAH	IK1	IK0	SWIT1	SWIT0	IK1 *4	0	Yes	No	Interrupt factor flag (K10)
					IK0 *4	0	Yes	No	Interrupt factor flag (K00–K03)
	R				SWIT1 *4	0	Yes	No	Interrupt factor flag (stopwatch 1 Hz)
					SWIT0 *4	0	Yes	No	Interrupt factor flag (stopwatch 10 Hz)
2EBH	R03	R02	R01	R00	R03	0	High	Low	Output port (R03)
					R02	0	High	Low	Output port (R02)
	R/W				R01	0	High	Low	Output port (R01)
					R00	0	High	Low	Output port (R00)
2ECH	R13	R12	R11 / SIOF	R10	R13	0	High/On	Low/Off	Output port (R13)/$\overline{BZ}$ output control
					R12	0	High/On	Low/Off	Output port (R12)/FOUT output control
	R/W		R/W / R	R/W	R11	0	High	Low	Output port (R11, LAMP)
					SIOF	0	Run	Stop	Output port (SIOF)
					R10	0	High/On	Low/Off	Output port (R10)/BZ output control
2EDH	P03	P02	P01	P00	P03	– *2	High	Low	I/O port data (P00–P03)
					P02	– *2	High	Low	Output latch reset at time of SR
	R/W				P01	– *2	High	Low	
					P00	– *2	High	Low	

*1 Initial value at the time of initial reset
*2 Not set in the circuit
*3 Constantly "0" when being read
*4 Reset (0) immediately after being read
*5 Undefined

Table 4.2.1(b) I/O memory map (2EEH–2FBH)

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
2EEH	TMRST	SWRUN	SWRST	IOC0	TMRST*3	Reset	Reset	–	Clock timer reset
					SWRUN	0	Run	Stop	Stopwatch timer Run/Stop
	W	R/W	W	R/W	SWRST*3	Reset	Reset	–	Stopwatch timer reset
					IOC0	0	Output	Input	I/O control register 0 (P00–P03)
2EFH	WDRST	WD2	WD1	WD0	WDRST*3	Reset	Reset	–	Watchdog timer reset
					WD2	0			Timer data (watchdog timer) 1/4 Hz
	W	R			WD1	0			Timer data (watchdog timer) 1/2 Hz
					WD0	0			Timer data (watchdog timer) 1 Hz
2F0H	SD3	SD2	SD1	SD0	SD3	× *5			Serial interface data register (low-order 4 bits)
					SD2	× *5			
	R/W				SD1	× *5			
					SD0	× *5			
2F1H	SD7	SD6	SD5	SD4	SD7	× *5			Serial interface data register (high-order 4 bits)
					SD6	× *5			
	R/W				SD5	× *5			
					SD4	× *5			
2F2H	SCS1	SCS0	SE2	EISIO	SCS1	1			SIF clock mode selection register [SCS1, 0]: 0 = Clock, 1 = CLK, 2 = CLK/2, 3 = CLK/4, slave
					SCS0	1			
	R/W				SE2	0	↑	↓	SIF clock edge selection register
					EISIO	0	Enable	Mask	Interrupt mask register (serial interface)
2F3H	0	0	IK2	ISIO	0 *3	– *2	–	–	Unused
					0 *3	– *2	–	–	Unused
	R				IK2 *4	0	Yes	No	Interrupt factor flag (K20–K23)
					ISIO *4	0	Yes	No	Interrupt factor flag (serial interface)
2F4H	K23	K22	K21	K20	K23	– *2	High	Low	Input port data (K20–K23)
					K22	– *2	High	Low	
	R				K21	– *2	High	Low	
					K20	– *2	High	Low	
2F5H	EIK23	EIK22	EIK21	EIK20	EIK23	0	Enable	Mask	Interrupt mask register (K20–K23)
					EIK22	0	Enable	Mask	
	R/W				EIK21	0	Enable	Mask	
					EIK20	0	Enable	Mask	
2F6H	BZFQ2	BZFQ1	BZFQ0	ENVRST	BZFQ2	0			Buzzer frequency selection [BZFQ2–0]: 0 = fOSC1/8, 1 = fOSC1/10, 2 = fOSC1/12, 3 = fOSC1/14, 4 = fOSC1/16, 5 = fOSC1/20, 6 = fOSC1/24, 7 = fOSC1/28
					BZFQ1	0			
	R/W			W	BZFQ0	0			
					ENVRST*3	Reset	Reset	–	Envelope reset
2F7H	ENVON	ENVRT	AMPDT	AMPON	ENVON	0	On	Off	Envelope On/Off
					ENVRT	0	1.0 sec	0.5 sec	Envelope cycle selection register
	R/W		R	R/W	AMPDT	1	+ > -	+ < -	Analog comparator data
					AMPON	0	On	Off	Analog comparator On/Off
2F8H	EV03	EV02	EV01	EV00	EV03	0			Event counter 0 (low-order 4 bits)
					EV02	0			
	R				EV01	0			
					EV00	0			
2F9H	EV07	EV06	EV05	EV04	EV07	0			Event counter 0 (high-order 4 bits)
					EV06	0			
	R				EV05	0			
					EV04	0			
2FAH	EV13	EV12	EV11	EV10	EV13	0			Event counter 1 (low-order 4 bits)
					EV12	0			
	R				EV11	0			
					EV10	0			
2FBH	EV17	EV16	EV15	EV14	EV17	0			Event counter 1 (high-order 4 bits)
					EV16	0			
	R				EV15	0			
					EV14	0			

*1 Initial value at the time of initial reset
*2 Not set in the circuit
*3 Constantly "0" when being read
*4 Reset (0) immediately after being read
*5 Undefined

Table 4.2.1(c) I/O memory map (2FCH–2FFH)

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
2FCH	EVSEL	ENRUN	EV1RST	EV0RST	EVSEL	0	Separate	Phase	Event counter mode
					EVRUN	0	Run	Stop	Event counter Run/Stop
	R/W		W		EV1RST*3	Reset	Reset	–	Event counter 1 reset
					EV0RST*3	Reset	Reset	–	Event counter 0 reset
2FDH	P13	P12	P11	P10	P13	– *2	High	Low	I/O port data (P10–P13) / Output latch reset at time of SR
					P12	– *2	High	Low	
	R/W				P11	– *2	High	Low	
					P10	– *2	High	Low	
2FEH	PRSM	CLKCHG	OSCC	IOC1	PRSM	0	38 kHz	32 kHz	OSC1 prescaler selection
					CLKCHG	0	OSC3	OSC1	CPU clock switch
	R/W				OSCC	0	On	Off	OSC3 oscillation On/Off
					IOC1	0	Output	Input	I/O control register 1 (P10–P13)
2FFH	BLS	BLC2	BLC1	BLC0	BLS	0	On	Off	BLD On/Off
	BLD1				BLD1	0	Low	Normal	BLD voltage evaluation data
	W	R/W			BLC2	× *5			Evaluation voltage setting register
					BLC1	× *5			
	R				BLC0	× *5			

Evaluation voltage setting register

[BLC2–0]	0	1	2	3	4	5	6	7	
E0C6235/62A35	2.20	2.25	2.30	2.35	2.40	2.45	2.50	2.55	(V)
E0C62L35	1.05	1.10	1.15	1.20	1.25	1.30	1.35	1.40	(V)

*1 Initial value at the time of initial reset
*2 Not set in the circuit
*3 Constantly "0" when being read
*4 Reset (0) immediately after being read
*5 Undefined

CHAPTER 5 INITIAL RESET

5.1 Internal Status at Initial Reset

Initial reset initializes the CPU as shown in the table below.

Table 5.1.1 Initial values

CPU core			
Name	Symbol	Bit length	Status
Program counter step	PCS	8	00H
Program counter page	PCP	4	1H
New page pointer	NPP	4	1H
Stack pointer	SP	8	Undefined
Index register X	X	10	Undefined
Index register Y	Y	10	Undefined
Register pointer	RP	4	Undefined
General register A	A	4	Undefined
General register B	B	4	Undefined
Interrupt flag	I	1	0
Decimal flag	D	1	Undefined
Zero flag	Z	1	Undefined
Carry flag	C	1	Undefined

Peripheral circuits		
Name	Bit length	Status
RAM	4	Undefined
Segment data	4	Undefined
Other peripheral circuits	4	*1

*1 See Tables 4.2.1(a)–(c).

5.2 Example of Initialize Program

```
ZTI     EQU  2E9H
ZSWC    EQU  2EEH
ZWDT    EQU  2EFH
XTMRST  EQU  1000B
XWDRST  EQU  1000B
STACK   EQU  000H
YRAM00  EQU  000H
YRAM08  EQU  080H
YRAM10  EQU  100H
ZLCD24  EQU  240H
;
        ORG  100H
;
        JP   INIT          ;JUMP INIT. ROUTINE
;
;
        ORG  110H
;
INIT    RST  F,0000B       ;CLEAR IDZC FLAG
;
        LD   A,STACK SHR 4
        LD   SPH,A
        LD   A,STACK SHR 8
        LD   SPL,A         ;SET STACK POINTER 000H
;
        LD   X,LOW YRAM00  ;SELECT RAM ADDR. ( 000H ) BY X REG.
;
RAMCL1  LD   XP,A          ;-----------------------------------
;
RAMCL2  LBPX MX,00H
        CP   XL,0
        JP   NZ,RAMCL2
;
        CP   A,2           ;ALL CLEAR RAM & LCD SEGMENT DATA
        JP   C,CONTCL
        CP   XH,7          ;ADDR. 000H TO 26FH
        JP   NC,QUITCL
;
CONTCL  CP   XH,0
        JP   NZ,RAMCL2
        ADD  A,1
        JP   RAMCL1        ;-----------------------------------
;
```

```
QUITCL  LD    X,LOW ZSWC    ;SELECT TMRST ADDR. BY X REG.
        OR    MX,XTMRST     ;RESET TM
;
        LD    X,LOW ZWDT    ;SELECT WDRST ADDR. BY X REG.
        LD    MX,XWDRST     ;RESET W.D.T.
;
        LD    X,LOW ZTI     ;SELECT TI ADDR. BY X REG.
        LD    A,MX          ;RESET INT. FLAG ( TI )
;
        LD    A,0
        RST   F,0000B       ;CLEAR IDZC FLAG
```

This program is the basic initialize program for the E0C6235 Series. When this program is executed the internal circuits shown in Table 5.2.1 are initialized. When using the program example, use it after adding the setting items necessary for the application.

Table 5.2.1
Results of initializing internal circuits

Internal circuit		Setting value
General register	A	0H
General register	B	0H
Stack pointer	SP	000H
Interrupt flag	IF	0
Decimal flag	DF	0
Zero flag	ZF	0
Carry flag	CF	0
RAM data	(000H–06FH) (080H–0EFH) (100H–1FFH)	0H
Segment data	(240H–26FH)	0H

CHAPTER 6 PERIPHERAL CIRCUITS

Peripheral circuits (timer, I/O, and so on) of the E0C6235 Series are memory mapped, and interfaced with the CPU. Thus, all the peripheral circuits can be controlled by using the memory operation command to access the I/O memory in the memory map.

6.1 Watchdog Timer

I/O memory map of watchdog timer

The control register of the watchdog timer is shown in Table 6.1.1.

Table 6.1.1 I/O memory map (watchdog timer)

Address	Register								Comment
	D3	D2	D1	D0	Name	Init *1	1	0	
2EFH	WDRST	WD2	WD1	WD0	WDRST*3	Reset	Reset	–	Watchdog timer reset
					WD2	0			Timer data (watchdog timer) 1/4 Hz
					WD1	0			Timer data (watchdog timer) 1/2 Hz
	W	R			WD0	0			Timer data (watchdog timer) 1 Hz

*1 Initial value at the time of initial reset
*2 Not set in the circuit
*3 Constantly "0" when being read
*4 Reset (0) immediately after being read
*5 Undefined

WDRST: Watchdog timer reset (2EFH·D3)

This is the bit for resetting the watchdog timer.

When "1" is written:	Watchdog timer is reset
When "0" is written:	No operation
Read-out:	Always "0"

When "1" is written to WDRST, the watchdog timer is reset, and the operation restarts immediately after this. When "0" is written to WDRST, no operation results.
This bit is dedicated for writing, and is always "0" for read-out.

Program example

• **Watchdog timer reset**

```
ZWDT    EQU  2EFH
XWDRST  EQU  1000B
;
        LD   A,ZWDT SHR 8
        LD   XP,A
        LD   X,LOW ZWDT  ;SELECT W.D.T. ADDR. BY X REG.
        LD   MX,XWDRST   ;RESET W.D.T.
```

The watchdog timer is reset when "1" is written to WDRST.

Programming note

When the watchdog timer is being used, the software must reset it within 3-second cycles, and timer data (WD0–WD2) cannot be used for timer applications.

6.2 Oscillation Circuit

I/O memory map of oscillation circuit

The control registers of the oscillation circuit are shown in Table 6.2.1.

Table 6.2.1 I/O memory map (oscillation circuit)

Address	Register								Comment
	D3	D2	D1	D0	Name	Init *1	1	0	
2FEH	PRSM	CLKCHG	OSCC	IOC1	PRSM	0	38 kHz	32 kHz	OSC1 prescaler selection
					CLKCHG	0	OSC3	OSC1	CPU clock switch
	R/W				OSCC	0	On	Off	OSC3 oscillation On/Off
					IOC1	0	Output	Input	I/O control register 1 (P10–P13)

*1 Initial value at the time of initial reset
*2 Not set in the circuit
*3 Constantly "0" when being read
*4 Reset (0) immediately after being read
*5 Undefined

OSCC: OSC3 oscillation control (2FEH·D1)

Controls oscillation ON/OFF for the OSC3 oscillation circuit. (E0C62A35 only)

When "1" is written: The OSC3 oscillation ON
When "0" is written: The OSC3 oscillation OFF
Read-out: Valid

When it is necessary to operate the CPU of the E0C62A35 at high speed, set OSCC to "1". At other times, set it to "0" to lessen the current consumption.
For E0C6235 and 62L35, keep OSCC set to "0".
At initial reset, OSCC is set to "0".

CLKCHG: The CPU's clock switch (2FEH·D2)

The CPU's operation clock is selected with this register. (E0C62A35 only)

When "1" is written: OSC3 clock is selected.
When "0" is written: OSC1 clock is selected.
Read-out: Valid

When the E0C62A35's CPU clock is to be OSC3, set CLKCHG to "1"; for OSC1, set CLKCHG to "0". This register cannot be controlled for E0C6235 and 62L35, so that OSC1 is selected no matter what the set value.
At initial reset, CLKCHG is set to "0".

PRSM: OSC1 prescaler selection (2FEH·D3)

Selects the prescaler for the crystal oscillator of the OSC1 oscillation circuit.

When "1" is written:	38.4 kHz
When "0" is written:	32.768 kHz
Read-out:	Valid

Operation of the clock timer and stopwatch timer can be made accurate by selecting this register. When the set value for this register does not suit the crystal oscillator used, the operation cycles of the previously mentioned peripheral circuitry is multiplied as shown in Table 6.2.2.

Table 6.2.2 Operation cycle when the setting is wrong

32.768 kHz, PRSM = "1"	T'≈1.172T
38.4 kHz, PRSM = "0"	T'≈0.853T

At initial reset, PRSM is set to "0".

Program examples

• Switching clock from OSC1 to OSC3

```
ZOSC    EQU  2FEH
XOSCC   EQU  0010B
XCLKCG  EQU  0100B
XLPCNT  EQU  0H
XDECRG  EQU  0FH
;
        LD   A,ZOSC SHR 8
        LD   XP,A
        LD   X,LOW ZOSC         ;SELECT OSC ADDR. BY X REG.
        OR   MX,XOSCC           ;OSCC ON
;
        LD   A,XLPCNT
WAITLP  ADD  A,XDECRG
        JP   NZ,WAITLP          ;WAIT 6 msec
        OR   MX,XCLKCG          ;CLK CHANGE OSC1 TO OSC3
```

It takes at least 5 msec from the time the OSC3 oscillation circuit goes ON until the oscillation stabilizes. In the program example, it takes about 6 msec (f_{OSC1} = 32.768 kHz) for OSC1 to switch to OSC3 after the OSC3 oscillation goes ON.

• Switching clock from OSC3 to OSC1

```
ZOSC    EQU  2FEH
XOSCC   EQU  0010B
XCLKCG  EQU  0100B
;
        LD   A,ZOSC SHR 8
        LD   XP,A
        LD   X,LOW ZOSC         ;SELECT OSC ADDR. BY X REG.
        AND  MX,XCLKCG XOR 0FH  ;CLK CHANGE OSC3 TO OSC1
        AND  MX,XOSCC XOR 0FH   ;OSCC OFF
```

In the program example, the CPU operation clock is switched from OSC3 to OSC1, and in the next step OSC3 oscillation goes OFF.

• OSC1 crystal selection (38.4 kHz)

```
ZOSC    EQU  2FEH
XPRSM   EQU  1000B
;
        LD   A,ZOSC SHR 8
        LD   XP,A
        LD   X,LOW ZOSC      ;SELECT PRSM ADDR. BY X REG.
        OR   MX,XPRSM        ;SET OSC1 38.4 kHz MODE
```

In the program example, "1" is written to PRSM, to select the 38.4 kHz prescaler.

Programming notes

(1) It takes at least 5 msec from the time the OSC3 oscillation circuit goes ON until the oscillation stabilizes. Consequently, when switching the CPU operation clock from OSC1 to OSC3, do this after a minimum of 5 msec have elapsed since the OSC3 oscillation went ON.
Further, the oscillation stabilization time varies depending on the external oscillator characteristics and conditions of use, so allow ample margin when setting the wait time.

(2) When switching the clock form OSC3 to OSC1, use a separate instruction for switching the OSC3 oscillation OFF. An error in the CPU operation can result if this processing is performed at the same time by the one instruction.

(3) To operate the clock timer and stopwatch timer accurately, select the prescaler of the OSC1 to match the crystal oscillator used.

6.3 Input Ports (K00–K03, K10, K20–K23)

I/O memory map of input ports

The control registers of the input ports are shown in Table 6.3.1.

Table 6.3.1 I/O memory map (input ports)

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
2E3H	K03	K02	K01	K00	K03	– *2	High	Low	Input port data (K00–K03)
					K02	– *2	High	Low	
	R				K01	– *2	High	Low	
					K00	– *2	High	Low	
2E4H	KCP03	KCP02	KCP01	KCP00	KCP03	0	↓	↑	Input comparison register (K00–K03)
					KCP02	0	↓	↑	
	R/W				KCP01	0	↓	↑	
					KCP00	0	↓	↑	
2E5H	EIK03	EIK02	EIK01	EIK00	EIK03	0	Enable	Mask	Interrupt mask register (K00–K03)
					EIK02	0	Enable	Mask	
	R/W				EIK01	0	Enable	Mask	
					EIK00	0	Enable	Mask	
2E7H	SCTRG	EIK10	KCP10	K10	SCTRG*3	–	Trigger	–	Serial interface clock trigger
					EIK10	0	Enable	Mask	Interrupt mask register (K10)
	W	R/W		R	KCP10	0	↓	↑	Input comparison register (K10)
					K10	– *2	High	Low	Input port data (K10)
2EAH	IK1	IK0	SWIT1	SWIT0	IK1 *4	0	Yes	No	Interrupt factor flag (K10)
					IK0 *4	0	Yes	No	Interrupt factor flag (K00–K03)
	R				SWIT1 *4	0	Yes	No	Interrupt factor flag (stopwatch 1 Hz)
					SWIT0 *4	0	Yes	No	Interrupt factor flag (stopwatch 10 Hz)
2F3H	0	0	IK2	ISIO	0 *3	– *2	–	–	Unused
					0 *3	– *2	–	–	Unused
	R				IK2 *4	0	Yes	No	Interrupt factor flag (K20–K23)
					ISIO *4	0	Yes	No	Interrupt factor flag (serial interface)
2F4H	K23	K22	K21	K20	K23	– *2	High	Low	Input port data (K20–K23)
					K22	– *2	High	Low	
	R				K21	– *2	High	Low	
					K20	– *2	High	Low	
2F5H	EIK23	EIK22	EIK21	EIK20	EIK23	0	Enable	Mask	Interrupt mask register (K20–K23)
					EIK22	0	Enable	Mask	
	R/W				EIK21	0	Enable	Mask	
					EIK20	0	Enable	Mask	

*1 Initial value at the time of initial reset
*2 Not set in the circuit
*3 Constantly "0" when being read
*4 Reset (0) immediately after being read
*5 Undefined

K00–K03, K10, K20–K23: Input port data (2E3H, 2E7H·D0, 2F4H)

Input data of the input port pins can be read out with these registers.

When "1" is read out:	High level
When "0" is read out:	Low level
Writing:	Invalid

The read-out is "1" when the pin voltage of the nine bits of the input ports (K00–K03, K10, K20–K23) goes high (V_{DD}), and "0" when the voltage goes low (V_{SS}).
These bits are dedicated for read-out, so writing cannot be done.

KCP00–KCP03, KCP10: Input comparison registers (2E4H, 2E7H·D1)

Interrupt conditions for pins K00–K03 and K10 can be set with this register.

When "1" is written:	Falling edge
When "0" is written:	Rising edge
Read-out:	Valid

Of the nine bits of the input ports, the interrupt conditions can be set for the rising or falling edge of input for each of the five bits (K00–K03 and K10), through the input comparison registers (KCP00–KCP03 and KCP10).
At initial reset, these registers are set to "0".

EIK00–EIK03, EIK10, EIK20–EIK23: Interrupt mask registers (2E5H, 2E7H·D2, 2F5H)

Masking the interrupt of the input port pins can be selected with these registers.

When "1" is written:	Enable
When "0" is written:	Mask
Read-out:	Valid

With these registers, masking of the input port bits can be selected for each of the nine bits.
At initial reset, these registers are all set to "0".

IK0, IK1, IK2: Interrupt factor flags (2EAH·D2 and D3, 2F3H·D1)

These flags indicate the occurrence of input interrupt.

When "1" is read out:	Interrupt has occurred
When "0" is read out:	Interrupt has not occurred
Writing:	Invalid

The interrupt factor flags IK0, IK1 and IK2 are associated with K00–K03, K10 and K20–K23, respectively. From the status of these flags, the software can decide whether an input interrupt has occurred.
These flags are reset when the software reads them. Read-out can be done only in the DI status (interrupt flag = "0"). At initial reset, these flags are set to "0".

Program examples

• Reading out from input ports (K00–K03, K20–K23)

```
ZK0     EQU   2E3H
ZK2     EQU   2F4H
;
        LD    A,ZK0 SHR 8
        LD    XP,A
        LD    X,LOW ZK0   ;SELECT K0 ADDR. BY X REG.
        LD    A,MX        ;READ K0 INPUT PORTS TO A REG.
;
        LD    X,LOW ZK2   ;SELECT K2 ADDR. BY X REG.
        LD    B,MX        ;READ K2 INPUT PORTS TO B REG.
```

In this program example, data from the input ports (K00–K03, K20–K23) is read to the general registers (A, B). Figure 6.3.1 shows the correspondence of the input ports and general registers.

Fig. 6.3.1 Correspondence between input ports and general registers

A register

D3	D2	D1	D0
K03	K02	K01	K00

B register

D3	D2	D1	D0
K23	K22	K21	K20

• Setting of input comparison register and interrupt mask register

```
ZKCP0   EQU  2E4H
ZK10    EQU  2E7H
ZEIK2   EQU  2F5H
XKCP0D  EQU  1100B      ;INT.  POS.-GOING EDGE K00,K01
                        ;INT.  NEG.-GOING EDGE K02,K03
;
XEIK0D  EQU  1111B      ;INT.  ENABLE K00-K03
XALK1D  EQU  0110B      ;INT.  NEG.-GOING EDGE K10
                        ;INT.  ENABLE K10
;
XEIK2D  EQU  0011B      ;INT.  ENABLE K20,K21
;
;
        LD   A,ZKCP0 SHR 8
        LD   XP,A
        LD   X,LOW ZKCP0 ;SELECT KCP0 ADDR. BY X REG.
        LDPX MX,XKCP0D   ;SET KCP00-KCP03 DATA
        LD   MX,XEIK0D   ;SET EIK00-EIK03 DATA
;
        LD   X,LOW ZK10  ;SELECT EIK1 & KCP1 ADDR. BY X REG.
        LD   MX,XALK1D   ;SET EIK10 & KCP10 DATA
;
        LD   X,LOW ZEIK2 ;SELECT EIK2 ADDR. BY X REG.
        LD   MX,XEIK2D   ;SET EIK20-EIK23 DATA
```

This program writes the data of the input comparison registers (KCP00–KCP03, KCP10) and interrupt mask registers (EIK00–EIK03, EIK10, EIK20–EIK23) to set the interrupt conditions as shown in Table 6.3.2.

Table 6.3.2
Example of setting interrupt conditions

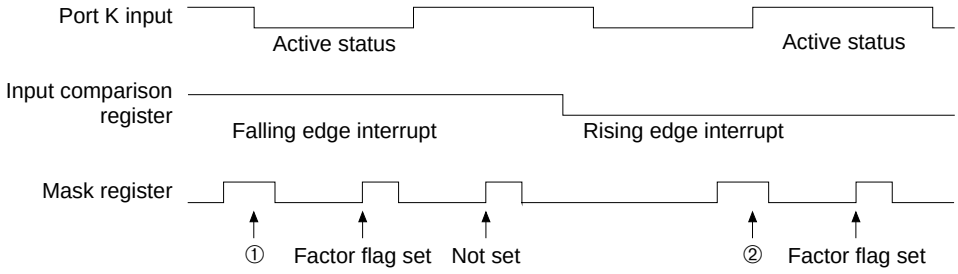
Terminal	Interrupt status	Edge
K00	Generated	Rising
K01	Generated	Rising
K02	Generated	Falling
K03	Generated	Falling
K10	Generated	Falling
K20	Generated	Rising
K21	Generated	Rising
K22	Not generated	– – –
K23	Not generated	– – –

Programming notes

(1) When input ports are changed from high to low by pull-down resistance, the fall of the waveform is delayed on account of the time constant of the pull-down resistance and input gate capacitance. Hence, when fetching input ports, set an appropriate wait time.
Particular care needs to be taken of the key scan during key matrix configuration. Aim for a wait time of about 1 msec.

(2) When "noise rejector circuit enable" is selected with the mask option, a maximum delay of 1 msec occurs from time the interrupt conditions are established until the interrupt factor flag (IK) is set to "1" (until the interrupt is actually generated).
Hence, pay attention to the timing when reading out (resetting) the interrupt factor flag.
For example, when performing a key scan with the key matrix, the key scan changes the input status to set the interrupt factor flag, so it has to be read out to reset it. However, if the interrupt factor flag is read out immediately after key scanning, the delay will cause the flag to be set after read-out, so that it will not be reset.

(3) Input interrupt programing related precautions



When the content of the mask register is rewritten, while the port K input is in the active status. The input interrupt factor flags are set at ① and ②, ① being the interrupt due to the falling edge and ② the interrupt due to the rising edge.

Fig. 6.3.2
Input interrupt timing

When using an input interrupt, if you rewrite the content of the mask register, when the value of the input terminal which becomes the interrupt input is in the active status, the factor flag for input interrupt may be set.

Therefore, when using the input interrupt, the active status of the input terminal implies

input terminal = low status, when the falling edge interrupt is effected and

input terminal = high status, when the rising edge interrupt is effected.

When an interrupt is triggered at the falling edge of an input terminal, a factor flag is set with the timing of ① shown in Figure 6.3.2. However, when clearing the content of the mask register with the input terminal kept in the low status and then setting it, the factor flag of the input interrupt is again set at the timing that has been set.

Consequently, when the input terminal is in the active status (low status), do not rewrite the mask register (clearing, then setting the mask register), so that a factor flag will only set at the falling edge in this case. When clearing, then setting the mask register, set the mask register, when the input terminal is not in the active status (high status).

When an interrupt is triggered at the rising edge of the input terminal, a factor flag will be set at the timing of ② shown in Figure 6.3.2. In this case, when the mask registers cleared, then set, you should set the mask register, when the input terminal is in the low status.

In addition, when the mask register = "1" and the content of the input comparison register is rewritten in the input terminal active status, an input interrupt factor flag may be set. Thus, you should rewrite the content of the input comparison register in the mask register = "0" status.

(4) Read-out of the interrupt factor flag (IK) can be done only in the DI status (interrupt flag = "0"). Read-out during EI status (interrupt flag = "1") will cause malfunction.

(5) Writing of the interrupt mask register (EIK) can be done only in the DI status (interrupt flag = "0"). Writing during EI status (interrupt flag = "1") will cause malfunction.

6.4 Output Ports (R00–R03, R10–R13)

I/O memory map of output ports

The control registers of the output ports are shown in Table 6.4.1.

Table 6.4.1 I/O memory map (output ports)

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
2EBH	R03	R02	R01	R00	R03	0	High	Low	Output port (R03)
					R02	0	High	Low	Output port (R02)
	R/W				R01	0	High	Low	Output port (R01)
					R00	0	High	Low	Output port (R00)
2ECH	R13	R12	R11 / SIOF	R10	R13	0	High/On	Low/Off	Output port (R13)/$\overline{BZ}$ output control
					R12	0	High/On	Low/Off	Output port (R12)/FOUT output control
	R/W		R/W	R/W	R11	0	High	Low	Output port (R11, LAMP)
					SIOF	0	Run	Stop	Output port (SIOF)
			R		R10	0	High/On	Low/Off	Output port (R10)/BZ output control

*1 Initial value at the time of initial reset
*2 Not set in the circuit
*3 Constantly "0" when being read
*4 Reset (0) immediately after being read
*5 Undefined

BZ, $\overline{BZ}$ (R10, R13): BZ and $\overline{BZ}$ are the buzzer signal output pins for driving the piezoelectric buzzer. The buzzer signal is generated by demultiplication of f_{OSC1}.
Also, a digital envelop can be added to the buzzer signal. See "6.14 Sound Generator" for details.

Notes
- *When the BZ and $\overline{BZ}$ output signals are turned ON or OFF, a hazard can result.*
- *When DC output is set for the output port R10, the output port R13 cannot be set for $\overline{BZ}$ output.*

Figure 6.4.1 shows the output waveform for BZ and $\overline{BZ}$.

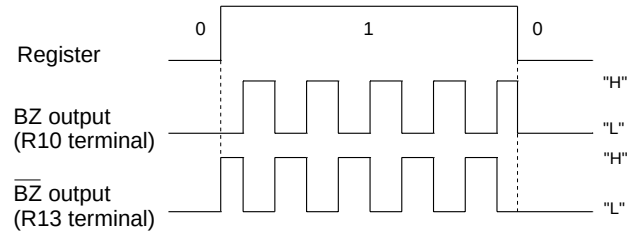


Fig. 6.4.1 Output waveform of BZ and $\overline{BZ}$

SIOF (R11): When the output port R11 is set for SIOF output, it outputs the signal indicating the running status (RUN/STOP) of the serial interface.
See "6.13 Serial Interface" for details.

FOUT (R12): When the output port R12 is set for FOUT output, it outputs the clock of fOSC1 or the demultiplied fOSC1. The clock frequency is selectable with the mask options, from the frequencies listed in Table 6.4.2.

Table 6.4.2
FOUT clock frequency

Setting value	Clock frequency (Hz)	
	fOSC1 = 32,768	fOSC1 = 38,400
fOSC1/1	32,768	38,400
fOSC1/2	16,384	19,200
fOSC1/4	8,192	9,600
fOSC1/8	4,096	4,800
fOSC1/16	2,048	2,400
fOSC1/32	1,024	1,200
fOSC1/64	512	600
fOSC1/128	256	300

Note *A hazard may occur when the FOUT signal is turned ON or OFF.*

R00–R03, R10–R13 (when DC output): Output port data (2EBH, 2ECH)

Sets the output data for the output ports.

When "1" is written: High output
When "0" is written: Low output
Read-out: Valid

The output port pins output the data written in the corresponding registers (R00–R03, R10–R13) without changing it. When "1" is written in the register, the output port pin goes high (VDD), and when "0" is written, the output port pin goes low (VSS).
At initial reset, all registers are set to "0".

R10, R13 (when BZ and $\overline{BZ}$ output is selected): Special output port data (2ECH·D0 and D3)

These bits control the output of the buzzer signals (BZ, $\overline{BZ}$).

When "1" is written:	Buzzer signal is output
When "0" is written:	Low level (DC) is output
Read-out:	Valid

$\overline{BZ}$ is output from pin R13. With the mask option, selection can be made perform this output control by R13, or to perform output control simultaneously with BZ by R10.

- When R13 controls $\overline{BZ}$ output

  BZ output and $\overline{BZ}$ output can be controlled independently. BZ output is controlled by writing data to R10, and $\overline{BZ}$ output is controlled by writing data to R13.

- When R10 controls $\overline{BZ}$ output

  BZ output and $\overline{BZ}$ output can be controlled simultaneously by writing data to R10 only. For this case, R13 can be used as a one-bit general register having both read and write functions, and data of this register exerts no affect on $\overline{BZ}$ output (output from the R13 pin).

At initial reset, registers R10 and R13 are set to "0".

R11 (when SIOF output is selected): Special output port data (2ECH·D1)

Indicates the running status of the serial interface.

When "1" is read out:	RUN
When "0" is read out:	STOP
Writing:	Invalid

See "6.13 Serial Interface" for details of SIOF. This bit is exclusively for reading out, so data cannot be written to it.

R12 (when FOUT is selected): Special output port data (2ECH·D2)

Controls the FOUT (clock) output.

When "1" is written:	Clock output
When "0" is written:	Low level (DC) output
Read-out:	Valid

FOUT output can be controlled by writing data to R12.
At initial reset, this register is set to "0".

Program examples

• Writing to output ports (R00–R03, R10–R13)

```
ZR0     EQU   2EBH
;
        LD    A,ZR0 SHR 8
        LD    XP,A
        LD    X,LOW ZR0 ;SELECT R0 ADDR. BY X REG.
        LDPX  MX,A      ;WRITE A REG. TO R0 OUTPUT PORTS
        LD    MX,B      ;WRITE B REG. TO R1 OUTPUT PORTS
```

In this program example, the contents of the general registers A and B are written to the output ports R00–R03 and R10–R13.
Figure 6.4.2 shows the correspondence of the output ports and the general registers.

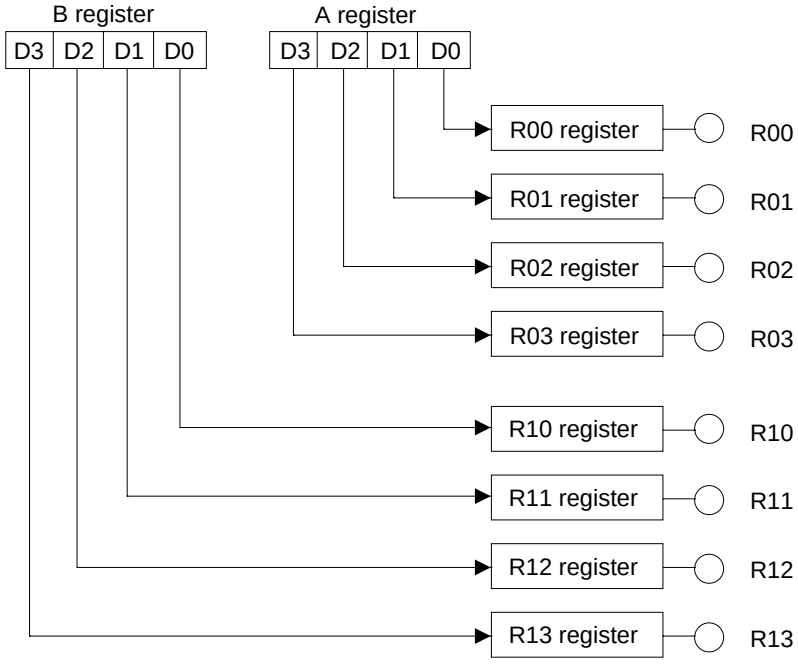


Fig. 6.4.2
Correspondence of output ports and general registers

• R12 clock output
(when R12 is made FOUT with the mask option)

```
ZR1     EQU   2ECH
XFOUT   EQU   0100B
;
        LD    A,ZR1 SHR 8
        LD    XP,A
        LD    X,LOW ZR1  ;SELECT FOUT(R12) ADDR. BY X REG.
        OR    MX,XFOUT   ;OUTPUT CLOCK
```

"1" is written to the output register R12, and the clock is output from the R12 pin.
Figure 6.4.3 shows the timing chart of the R12 clock output.

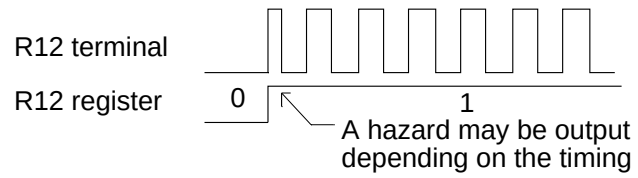


Fig. 6.4.3
Timing chart of the R12 clock output

Programming note

When BZ, $\overline{BZ}$ and FOUT are selected with the mask option, a hazard may be observed in the output waveform when the data of the output register changes.

6.5 I/O Ports (P00–P03, P10–P13)

I/O memory map of I/O ports

The control registers of the I/O ports are shown in Table 6.5.1.

Table 6.5.1 I/O memory map (I/O ports)

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
2EDH	P03	P02	P01	P00	P03	– *2	High	Low	I/O port data (P00–P03)
					P02	– *2	High	Low	
	R/W				P01	– *2	High	Low	Output latch reset at time of SR
					P00	– *2	High	Low	
2EEH	TMRST	SWRUN	SWRST	IOC0	TMRST*3	Reset	Reset	–	Clock timer reset
					SWRUN	0	Run	Stop	Stopwatch timer Run/Stop
	W	R/W	W	R/W	SWRST*3	Reset	Reset	–	Stopwatch timer reset
					IOC0	0	Output	Input	I/O control register 0 (P00–P03)
2FDH	P13	P12	P11	P10	P13	– *2	High	Low	I/O port data (P10–P13)
					P12	– *2	High	Low	
	R/W				P11	– *2	High	Low	Output latch reset at time of SR
					P10	– *2	High	Low	
2FEH	PRSM	CLKCHG	OSCC	IOC1	PRSM	0	38 kHz	32 kHz	OSC1 prescaler selection
					CLKCHG	0	OSC3	OSC1	CPU clock switch
	R/W				OSCC	0	On	Off	OSC3 oscillation On/Off
					IOC1	0	Output	Input	I/O control register 1 (P10–P13)

*1 Initial value at the time of initial reset
*2 Not set in the circuit
*3 Constantly "0" when being read
*4 Reset (0) immediately after being read
*5 Undefined

P00–P03, P10–P13: I/O port data (2EDH, 2FDH)

I/O port data can be read and output data can be set through these ports.

- **When writing data**

  When "1" is written: High level
  When "0" is written: Low level

  When an I/O port is set to the output mode, the written data is output unchanged from the I/O port pin. When "1" is written as the port data, the port pin goes high (V_{DD}), and when "0" is written, the level goes low (V_{SS}). Port data can be written also in the input mode.

- **When reading data out**

  When "1" is read out: High level
  When "0" is read out: Low level

  The pin voltage level of the I/O port is read out. When the I/O port is in the input mode the voltage level being input to the port pin can be read out; in the output mode the output voltage level can be read. When the pin voltage is high (V_{DD}) the port data that can be read is "1", and when the pin voltage is low (V_{SS}) the data is "0". Further, the built-in pull-down resistance goes ON during read-out, so that the I/O port pin is pulled down.

Notes

- *When the I/O port is set to the output mode and a low-impedance load is connected to the port pin, the data written to the register may differ from the data read out.*
- *When the I/O port is set to the input mode and a low-level voltage (V_{SS}) is input, erroneous input results if the time constant of the capacitive load of the input line and the built-in pull-down resistance load is greater than the read-out time. When the input data is being read out, the time that the input line is pulled down is equivalent to 1.5 cycles of the CPU system clock. However, the electric potential of the pins must be settled within 0.5 cycles. If this condition cannot be fulfilled, some measure must be devised such as arranging pull-down resistance externally, or performing multiple read-outs.*

IOC0, IOC1: I/O control registers (2EEH·D0, 2FEH·D0)

The input and output modes of the I/O ports can be set with these registers.

When "1" is written:	Output mode
When "0" is written:	Input mode
Read-out:	Valid

The input and output modes of the I/O ports are set in units of four bits. IOC0 sets the mode for P00–P03, and IOC1 sets the mode for P10–P13.
Writing "1" to the I/O control register makes the corresponding I/O port enter the output mode, and writing "0" induces the input mode.
At initial reset, these two registers are set to "0", so the I/O ports are in the input mode.

Program examples • Reading out the I/O ports (P00–P03, P10–P13)

```
ZP0     EQU  2EDH
ZP1     EQU  2FDH
ZSWC    EQU  2EEH
ZOSC    EQU  2FEH
XIOC0   EQU  0001B
XIOC1   EQU  0001B
;
        LD   A,ZP0 SHR 8
        LD   XP,A
        LD   X,LOW ZSWC        ;SELECT IOC0 ADDR. BY X REG.
        AND  MX,XIOC0 XOR 0FH  ;SET P0 I/O PORTS INPUT MODE
;
        LD   X,LOW ZOSC        ;SELECT IOC1 ADDR. BY X REG.
        AND  MX,XIOC1 XOR 0FH  ;SET P1 I/O PORTS INPUT MODE
;
        LD   X,LOW ZP0         ;SELECT P0 ADDR. BY X REG.
        LD   A,MX              ;READ P0 INPUT PORTS TO A REG.
;
        LD   X,LOW ZP1         ;SELECT P1 ADDR. BY X REG.
        LD   B,MX              ;READ P1 INPUT PORTS TO B REG.
```

In the example, data of the I/O ports (P00–P03, P10–P13) is read to the general registers (A, B).
Figure 6.5.1 shows the correspondence between the I/O ports (input) and the general registers.

Fig. 6.5.1
Correspondence between I/O ports (input) and general registers

A register

D3	D2	D1	D0
P03	P02	P01	P00

B register

D3	D2	D1	D0
P13	P12	P11	P10

- **Writing to I/O ports (P00–P03, P10–P13)**

```
ZP0     EQU   2EDH
ZP1     EQU   2FDH
ZSWC    EQU   2EEH
ZOSC    EQU   2FEH
XIOC0   EQU   0001B
XIOC1   EQU   0001B
;
        LD    A,ZP0 SHR 8
        LD    XP,A
        LD    X,LOW ZSWC   ;SELECT IOC0 ADDR. BY X REG.
        OR    MX,XIOC0     ;SET P0 I/O PORTS OUTPUT MODE
;
        LD    X,LOW ZOSC   ;SELECT IOC1 ADDR. BY X REG.
        OR    MX,XIOC1     ;SET P1 I/O PORTS OUTPUT MODE
;
        LD    X,LOW ZP0    ;SELECT P0 ADDR. BY X REG.
        LD    MX,A         ;WRITE A REG. TO P0 I/O PORTS
;
        LD    X,LOW ZP1    ;SELECT P1 ADDR. BY X REG.
        LD    MX,B         ;WRITE B REG. TO P1 I/O PORTS
```

In this example, the contents of the general registers (A, B) are written to the I/O ports (P00–P03, P10–P13).
Figure 6.5.2 shows the correspondence between the I/O ports (output) and the general registers.

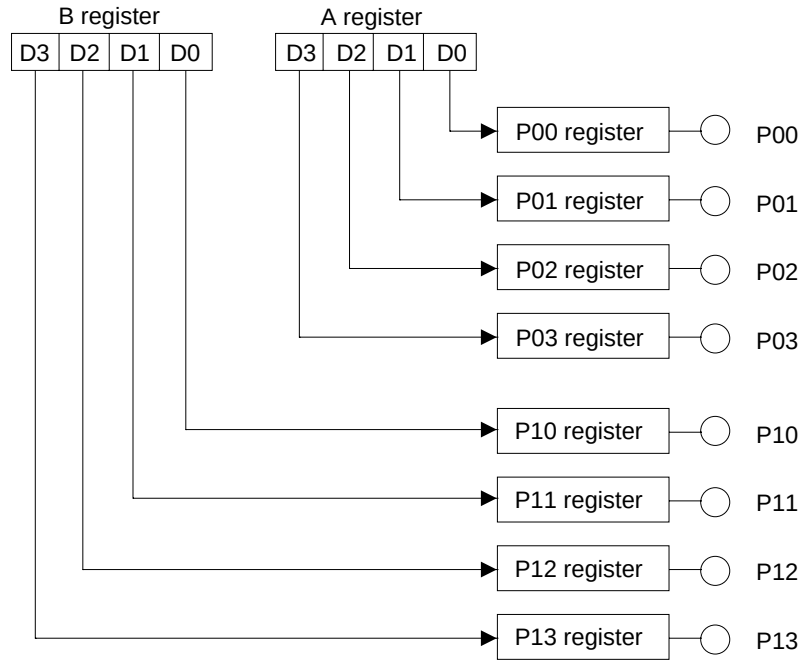


Fig. 6.5.2
Correspondence of I/O ports (output) and general registers

Programming notes

(1) When the I/O port is changed from high level to low level by the built-in pull down resistance, the falling-edge has the delay determined by the pull down resistance and the input gate capacitance. When the input data is being read out, the time that the input line is pulled down is equivalent to 1.5 cycles of the CPU system clock. However, the electric potential of the pins must be settled within 0.5 cycles. If this condition cannot be fulfilled, some measure must be devised such as arranging pull-down resistance externally, or performing multiple read-outs. Consequently, if data is read out while the CPU is running in the OSC3 oscillation circuit, data must be read out continuously for about 500 µsec.

(2) When the I/O port is set to the output mode and the data register has been read, the pin data instead of the register data can be read out. Because of this, if a low-impedance load is connected and read-out performed, the value of the register and the read-out result may differ.

6.6 LCD Driver (COM0–COM3, SEG0–SEG47)

I/O memory map of LCD driver

The control register of the LCD driver is shown in Table 6.6.1.

Table 6.6.1 I/O memory map (LCD driver)

Address	Register								Comment
	D3	D2	D1	D0	Name	Init *1	1	0	
2E8H	CSDC	ETI2	ETI8	ETI32	CSDC	0	Static	Dynamic	LCD drive switch
	R/W				ETI2	0	Enable	Mask	Interrupt mask register (clock timer 2 Hz)
					ETI8	0	Enable	Mask	Interrupt mask register (clock timer 8 Hz)
					ETI32	0	Enable	Mask	Interrupt mask register (clock timer 32 Hz)

*1 Initial value at the time of initial reset
*2 Not set in the circuit
*3 Constantly "0" when being read
*4 Reset (0) immediately after being read
*5 Undefined

CSDC: LCD drive switch (2E8H·D3)

The LCD drive format can be selected with this switch.

When "1" is written: Static drive
When "0" is written: Dynamic drive
Read-out: Valid

At initial reset, dynamic drive (CSDC = "0") is selected.

Fig. 6.6.1 Display memory map

Address / Page	Low / High	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0 or 2	4	Display memory (48 words x 4 bits) 0 page = R/W 2 page = W															
	5																
	6																

Display memory: (040H–06FH or 240H–26FH)

The LCD segments are lit or turned off depending on this data.

When "1" is written: Lit
When "0" is written: Not lit
Read-out: Valid for page 0
Undefined for page 2

By writing data into the display memory allocated to the LCD segment (on the panel), the segment can be lit or put out.
At initial reset, the contents of the display memory are undefined.

• **Segment allocation**

As shown in Figure 6.6.1, segment data of the E0C6235 Series is decided depending on display data written to the display memory (write-only) at address 040H–06FH (page 0) or 240H–26FH (page 2).

① The mask option enables the display memory to be allocated entirely to either page 0 or page 2.

② The address and bits of the display memory can be made to correspond to the segment pins (SEG0–SEG47) in any form through the mask option. This makes design easy by increasing the degree of freedom with which the liquid crystal panel can be designed.

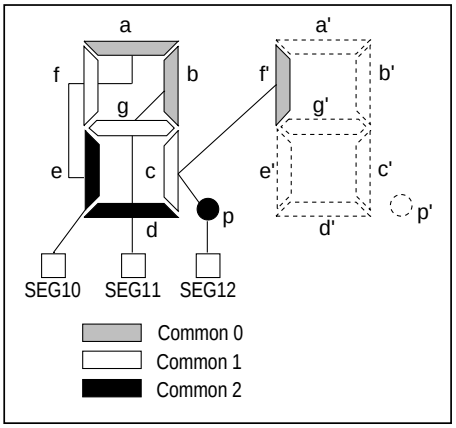
Figure 6.6.2 shows an example of the relationship between the LCD segments (on the panel) and the display memory (when page 0 is selected) for the case of 1/3 duty.

Address	Data			
	D3	D2	D1	D0
06AH	d	c	b	a
06BH	p	g	f	e
06CH	d'	c'	b'	a'
06DH	p'	g'	f'	e'

Display memory assignment table

	Common 0	Common 1	Common 2
SEG10	6A, D0 (a)	6B, D1 (f)	6B, D0 (e)
SEG11	6A, D1 (b)	6B, D2 (g)	6A, D3 (d)
SEG12	6D, D1 (f')	6A, D2 (c)	6B, D3 (p)

Pin assignment table



Example of LCD panel

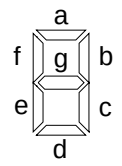
Fig. 6.6.2
Segment allocation

Program example

• Seven-segment display

```
LCHR0   EQU  3FH          ;CHR. DATA "0"
LCHR1   EQU  06H          ;CHR. DATA "1"
LCHR2   EQU  5BH          ;CHR. DATA "2"
LCHR3   EQU  4FH          ;CHR. DATA "3"
LCHR4   EQU  66H          ;CHR. DATA "4"
LCHR5   EQU  6DH          ;CHR. DATA "5"
LCHR6   EQU  7DH          ;CHR. DATA "6"
LCHR7   EQU  27H          ;CHR. DATA "7"
LCHR8   EQU  7FH          ;CHR. DATA "8"
LCHR9   EQU  6FH          ;CHR. DATA "9"
SECT    EQU  0H
;
        ORG  000H
;
        RETD LCHR0        ;LCD DISPLAY "0"
        RETD LCHR1        ;LCD DISPLAY "1"
        RETD LCHR2        ;LCD DISPLAY "2"
        RETD LCHR3        ;LCD DISPLAY "3"
        RETD LCHR4        ;LCD DISPLAY "4"
        RETD LCHR5        ;LCD DISPLAY "5"
        RETD LCHR6        ;LCD DISPLAY "6"
        RETD LCHR7        ;LCD DISPLAY "7"
        RETD LCHR8        ;LCD DISPLAY "8"
        RETD LCHR9        ;LCD DISPLAY "9"
;
DISP7S  LD   B,SECT       ;SET PROGRAM SECTION
        JPBA              ;JUMP DISPLAY TABLE
```

By setting the address of the segment to be lit in the X register and any value from 0 to 9 in the A register, and making CALL (CALZ) DISP7S, seven-segment display will be executed according to the contents of the A register. In the program example, correspondence of the segment and memory map is as shown in Figure 6.6.3.



A register	0	1	2	3	4
Display	0	1	2	3	4

Address "L"	d	c	b	a
Address "H"	—	g	f	e

A register	5	6	7	8	9
Display	5	6	7	8	9

Fig. 6.6.3
Correspondence with
A register

Programming notes

(1) When page 0 is selected for the display memory, the memory data and the display will not match until the area is initialized (through, for instance, memory clear processing by the CPU). Initialize the display memory by executing initial processing.

(2) When page 2 is selected for the display memory, that area becomes write-only. Consequently, data cannot be re-written by arithmetic operations (such as AND, OR, ADD, SUB).

6.7 Clock Timer

I/O memory map of clock timer

The control registers of the clock timer are shown in Table 6.7.1.

Table 6.7.1 I/O memory map (clock timer)

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
2E0H	TM3	TM2	TM1	TM0	TM3	0			Timer data (clock timer 2 Hz)
					TM2	0			Timer data (clock timer 4 Hz)
	R				TM1	0			Timer data (clock timer 8 Hz)
					TM0	0			Timer data (clock timer 16 Hz)
2E8H	CSDC	ETI2	ETI8	ETI32	CSDC	0	Static	Dynamic	LCD drive switch
					ETI2	0	Enable	Mask	Interrupt mask register (clock timer 2 Hz)
	R/W				ETI8	0	Enable	Mask	Interrupt mask register (clock timer 8 Hz)
					ETI32	0	Enable	Mask	Interrupt mask register (clock timer 32 Hz)
2E9H	0	TI2	TI8	TI32	0 *3	– *2	–	–	Unused
					TI2 *4	0	Yes	No	Interrupt factor flag (clock timer 2 Hz)
	R				TI8 *4	0	Yes	No	Interrupt factor flag (clock timer 8 Hz)
					TI32 *4	0	Yes	No	Interrupt factor flag (clock timer 32 Hz)
2EEH	TMRST	SWRUN	SWRST	IOC0	TMRST*3	Reset	Reset	–	Clock timer reset
					SWRUN	0	Run	Stop	Stopwatch timer Run/Stop
	W	R/W	W	R/W	SWRST*3	Reset	Reset	–	Stopwatch timer reset
					IOC0	0	Output	Input	I/O control register 0 (P00–P03)

*1 Initial value at the time of initial reset
*2 Not set in the circuit
*3 Constantly "0" when being read
*4 Reset (0) immediately after being read
*5 Undefined

TM0–TM3: Timer data (2E0H)

The 16 Hz–2 Hz timer data of the clock timer can be read out with this register. These four bits are read-out only, and writing operations are invalid.
At initial reset, the timer data is initialized to "0H".

TMRST: Clock timer reset (2EEH·D3)

This bit resets the clock timer.

When "1" is written: Clock timer reset
When "0" is written: No operation
Read-out: Always "0"

The clock timer is reset by writing "1" to TMRST. The clock timer starts immediately after this. No operation results when "0" is written to TMRST.
This bit is write-only, and so is always "0" at read-out.

ETI32, ETI8, ETI2: Interrupt mask registers (2E8H·D0–D2)

These registers are used to select whether to mask the clock timer interrupt.

When "1" is written:	Enabled
When "0" is written:	Masked
Read-out:	Valid

The interrupt mask registers (ETI32, ETI8, ETI2) are used to select whether to mask the interrupt to the separate frequencies (32 Hz, 8 Hz, 2 Hz).
At initial reset, these registers are all set to "0".

TI32, TI8, TI2: Interrupt factor flags (2E9H·D0–D2)

These flags indicate the status of the clock timer interrupt.

When "1" is read out:	Interrupt has occurred
When "0" is read out:	Interrupt has not occurred
Writing:	Invalid

The interrupt factor flags (TI32, TI8, TI2) correspond to the clock timer interrupts of the respective frequencies (32 Hz, 8 Hz, 2 Hz). The software can judge from these flags whether there is a clock timer interrupt. However, even if the interrupt is masked, the flags are set to "1" at the falling edge of the signal.
These flags can be reset through being read out by the software. Also, the flags can be read out only in the DI status (interrupt flag = "0").
At initial reset, these flags are set to "0".

- **Interrupt function**

  The clock timer can cause interrupts at the falling edge of 32 Hz, 8 Hz and 2 Hz signals. Software can set whether to mask any of these frequencies.
  Figure 6.7.1 is the timing chart of the clock timer.

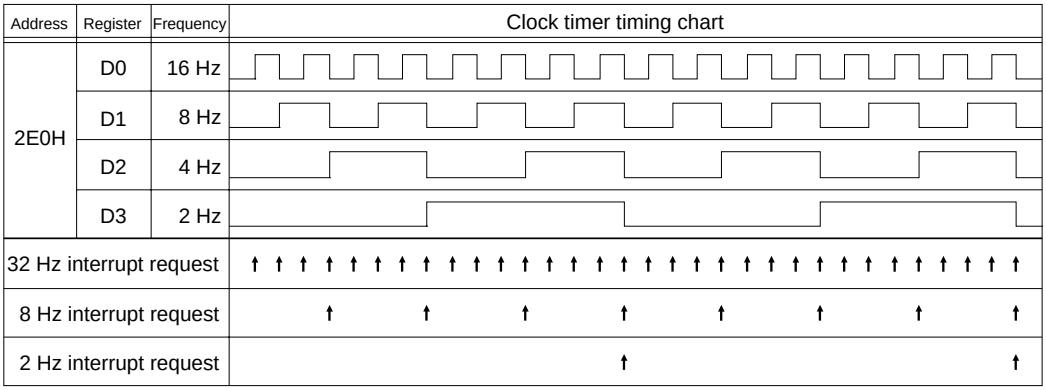


Fig. 6.7.1
Timing chart of the clock timer

As shown in Figure 6.7.1, interrupt is generated at the falling edge of the frequencies (32 Hz, 8 Hz, 2 Hz). At this time, the corresponding interrupt factor flag (TI32, TI8, TI2) is set to "1". Selection of whether to mask the separate interrupts can be made with the interrupt mask registers (ETI32, ETI8, ETI2). However, regardless of the interrupt mask register setting, the interrupt factor flag is set to "1" at the falling edge of the corresponding signal.

Program examples

• Initializing the clock timer and setting the interrupt mask register

```
ZETI    EQU  2E8H
ZSWC    EQU  2EEH
XETI2   EQU  0100B
XTMRST  EQU  1000B
;
        LD   A,ZETI SHR 8
        LD   XP,A
        LD   X,LOW ZETI   ;SELECT ETI ADDR. BY X REG.
        LDPX MX,XETI2     ;INT. ENABLE TM 2 Hz
;
        LD   YP,A
        LD   Y,LOW ZSWC   ;SELECT TMRST ADDR. BY Y REG.
        OR   MY,XTMRST    ;RESET TM
;
        LD   A,MX         ;RESET INT. FLAG (TI)
```

This program writes "1" to the interrupt mask register ETI2, to enable the 2 Hz interrupt. Also, the clock timer is initialized (reset) and the interrupt factor flag reset.

• Reading out clock timer

```
ZTM     EQU  2E0H
;
        LD   A,ZTM SHR 8
        LD   XP,A
        LD   X,LOW ZTM    ;SELECT TM ADDR. BY X REG.
        LD   A,MX         ;READ TM DATA TO A REG.
```

In this program example, the data of the clock timer (TM0–TM3) is read into the A register. Figure 6.7.2 shows the correspondence of the clock timer and the A register.

Fig. 6.7.2
Correspondence of clock timer and A register

A register

D3	D2	D1	D0
TM3	TM2	TM1	TM0

Programming notes

(1) The prescaler mode must be set correctly to suit the crystal oscillator to be used.

(2) When the clock timer has been reset, the interrupt factor flag (TI) may sometimes be set to "1". Consequently, perform flag read-out (reset the flag) as necessary at reset.

(3) The input clock of the watchdog timer is the 2 Hz signal of the clock timer, so that the watchdog timer may be counted up at timer reset.

(4) Read-out of the interrupt factor flag (TI) can be done only in the DI status (interrupt flag = "0"). Read-out during the EI status (interrupt flag = "1") will cause malfunctions.

(5) Writing of the interrupt mask register (ETI) can be done only in the DI status (interrupt flag = "0"). Writing during the EI status (interrupt flag = "1") will cause malfunctions.

6.8 Stopwatch Timer

I/O memory map of stopwatch timer

The control registers of the stopwatch timer are shown in Table 6.8.1.

Table 6.8.1 I/O memory map (stopwatch timer)

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
2E1H	SWL3	SWL2	SWL1	SWL0	SWL3	0			MSB
					SWL2	0			Stopwatch timer data 1/100 sec (BCD)
	R				SWL1	0			
					SWL0	0			LSB
2E2H	SWH3	SWH2	SWH1	SWH0	SWH3	0			MSB
					SWH2	0			Stopwatch timer data 1/10 sec (BCD)
					SWH1	0			
					SWH0	0			LSB
2E6H	HLMOD	BLD0	EISWIT1	EISWIT0	HLMOD	0	Heavy load	Normal	Heavy load protection mode register
					BLD0	0	Low	Normal	Sub-BLD evaluation data
	R/W	R	R/W		EISWIT1	0	Enable	Mask	Interrupt mask register (stopwatch 1 Hz)
					EISWIT0	0	Enable	Mask	Interrupt mask register (stopwatch 10 Hz)
2EAH	IK1	IK0	SWIT1	SWIT0	IK1 *4	0	Yes	No	Interrupt factor flag (K10)
					IK0 *4	0	Yes	No	Interrupt factor flag (K00–K03)
	R				SWIT1 *4	0	Yes	No	Interrupt factor flag (stopwatch 1 Hz)
					SWIT0 *4	0	Yes	No	Interrupt factor flag (stopwatch 10 Hz)
2EEH	TMRST	SWRUN	SWRST	IOC0	TMRST*3	Reset	Reset	–	Clock timer reset
					SWRUN	0	Run	Stop	Stopwatch timer Run/Stop
	W	R/W	W	R/W	SWRST*3	Reset	Reset	–	Stopwatch timer reset
					IOC0	0	Output	Input	I/O control register 0 (P00–P03)

*1 Initial value at the time of initial reset
*2 Not set in the circuit
*3 Constantly "0" when being read
*4 Reset (0) immediately after being read
*5 Undefined

SWL0–SWL3: Stopwatch timer 1/100 sec (2E1H)

Data (BCD) of the 1/100 sec column of the stopwatch timer can be read out. These four bits are read-only, and cannot be used for writing operations.
At initial reset, the timer data is set to "0H".

SWH0–SWH3: Stopwatch timer 1/10 sec (2E2H)

Data (BCD) of the 1/10 sec column of the stopwatch timer can be read out. These four bits are read-only, and cannot be used for writing operations.
At initial reset, the timer data is set to "0H".

SWRST: Stopwatch timer reset (2EEH·D1)

This bit resets the stopwatch timer.

When "1" is written:	Stopwatch timer reset
When "0" is written:	No operation
Read-out:	Always "0"

The stopwatch timer is reset when "1" is written to SWRST. When the stopwatch timer is reset in the RUN status, operation restarts immediately. Also, in the STOP status the reset data is maintained.
This bit is write-only, and is always "0" at read-out.

SWRUN: Stopwatch timer RUN/STOP (2EEH·D2)

This bit controls RUN/STOP of the stopwatch timer.

When "1" is written:	RUN
When "0" is written:	STOP
Read-out:	Valid

The stopwatch timer enters the RUN status when "1" is written to SWRUN, and the STOP status when "0" is written. In the STOP status, the timer data is maintained until the next RUN status or resets timer. Also, when the STOP status changes to the RUN status, the data that was maintained can be used for resuming the count.
When the timer data is read out in the RUN status, correct read-out may be impossible because of the carry from the low-order bit (SWL) to the high-order bit (SWH). This occurs when read-out has extended over the SWL and SWH bits when the carry occurs. To prevent this, perform read out after entering the STOP status, and then return to the RUN status. Also, the duration of the STOP status must be within 976 µsec (256 Hz 1/4 cycle).
At initial reset, this register is set to "0".

EISWIT0, EISWIT1: Interrupt mask register (2E6H·D0 and D1)

These registers are used to select whether to mask the stopwatch timer interrupt.

When "1" is written:	Enabled
When "0" is written:	Masked
Read-out:	Valid

The interrupt mask registers (EISWIT0, EISWIT1) are used to separately select whether to mask the 10 Hz and 1 Hz interrupts.
At initial reset, these registers are both set to "0".

SWIT0, SWIT1: Interrupt factor flag (2EAH·D0 and D1)

These flags indicate the status of the stopwatch timer interrupt.

When "1" is read out:	Interrupt has occurred
When "0" is read out:	Interrupt has not occurred
Writing:	Invalid

The interrupt factor flags (SWIT0, SWIT1) correspond to the 10 Hz and 1 Hz interrupts respectively. With these flags, the software can judge whether a stopwatch timer interrupt has occurred. However, regardless of the interrupt mask register setting, these flags are set to "1" by the timer overflow.
These flags are reset when read out by the software. Also, read-out is only possible in the DI status (interrupt flag = "0").
At initial reset, these flags are set to "0".

- **Interrupt function**

  The 10 Hz (approximate 10 Hz) and 1 Hz interrupts can be generated through the overflow of stopwatch timers SWL and SWH respectively. Also, software can set whether to separately mask the frequencies described earlier.
  Figure 6.8.1 is the timing chart for the stopwatch timer.

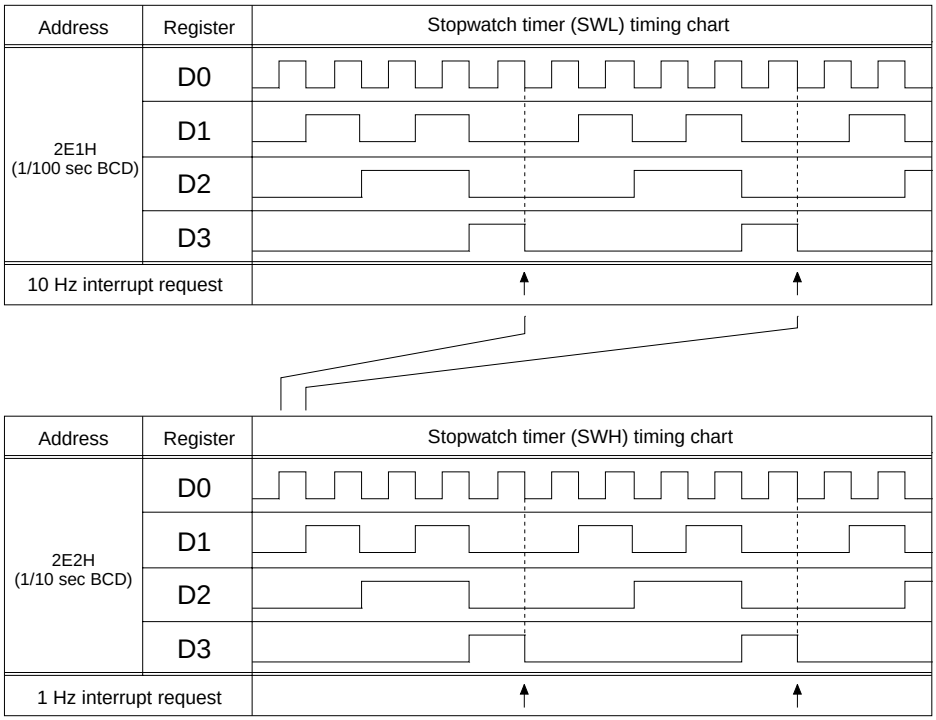


Fig. 6.8.1
Timing chart for stopwatch timer

As shown in Figure 6.8.1, the interrupts are generated by the overflow of their respective timers ("9" changing to "0"). Also, at this time the corresponding interrupt factor flags (SWIT0, SWIT1) are set to "1".
The respective interrupts can be masked separately through the interrupt mask registers (EISWIT0, EISWIT1). However, regardless of the setting of the interrupt mask registers, the interrupt factor flags are set to "1" by the overflow of their corresponding timers.

Program examples

• Setting start and interrupt mask register of stopwatch timer

```
ZBLDSI  EQU   2E6H
ZSWC    EQU   2EEH
XESWIT  EQU   0011B
XSWRUN  EQU   0100B
;
        LD    A,ZBLDSI SHR 8
        LD    XP,A
        LD    X,LOW ZBLDSI ;SELECT EISWIT ADDR. BY X REG.
        LD    MX,XESWIT    ;INT. ENABLE SW 10 & 1 Hz
;
        LD    X,LOW ZSWC   ;SELECT SWRUN ADDR. BY X REG.
        OR    MX,XSWRUN    ;START SW TIMER
```

"1" is written into the interrupt mask registers EISWIT0 and EISWIT1, enabling the 10 Hz and 1 Hz interrupts.
Also, "1" is written to SWRUN to start the stopwatch timer.

• Read-out of stopwatch timer

```
ZSWL    EQU  2E1H
ZSWC    EQU  2EEH
XSWRUN  EQU  0100B
;
        LD   A,ZSWC SHR 8
        LD   XP,A
        LD   X,LOW ZSWC         ;SELECT SWRUN ADDR.
                                ; BY X REG.
;
        LD   YP,A
        LD   Y,LOW ZSWL         ;SELECT SWL ADDR.
                                ; BY Y REG.
;
        AND  MX,XSWRUN XOR 0FH  ;STOP SW TIMER
        LDPY A,MY               ;READ SWL DATA TO A REG.
        LD   B,MY               ;READ SWH DATA TO B REG.
        OR   MX,XSWRUN          ;RUN SW TIMER
```

In the program example, the data of the stopwatch timer (SWL, SWH) is written into the general registers (A, B). To read out data, the count is made into the STOP status, and after read-out it is set to the RUN status again (to prevent incorrect read-out).
Figure 6.8.2 shows the correspondence between stopwatch timers and general registers.

Fig. 6.8.2 Correspondence between stopwatch timer and general registers

A register

D3	D2	D1	D0
SWL3	SWL2	SWL1	SWL0

B register

D3	D2	D1	D0
SWH3	SWH2	SWH1	SWH0

Programming notes

(1) The prescaler mode must be set correctly so that the stopwatch timer suits the crystal oscillator to be used.

(2) If timer data is read out in the RUN status, the timer must be made into the STOP status, and after data is read out the RUN status can be restored. If data is read out when a carry occurs, the data cannot be read correctly.
Also, the processing above must be performed within the STOP interval of 976 μsec (256 Hz 1/4 cycle).

(3) Read-out of the interrupt factor flag (SWIT) can be done only in the DI status (interrupt flag = "0"). Read-out during the EI status (interrupt flag = "1") will cause malfunctions.

(4) Writing of the interrupt mask register (EISWIT) can be done only in the DI status (interrupt flag = "0"). Writing during the EI status (interrupt flag = "1") will cause malfunctions.

6.9 Event Counter

I/O memory map of event counter

The control registers of the event counter are shown in Table 6.9.1.

Table 6.9.1 I/O memory map (event counter)

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
2F8H	EV03	EV02	EV01	EV00	EV03	0			Event counter 0 (low-order 4 bits)
	R				EV02	0			
					EV01	0			
					EV00	0			
2F9H	EV07	EV06	EV05	EV04	EV07	0			Event counter 0 (high-order 4 bits)
	R				EV06	0			
					EV05	0			
					EV04	0			
2FAH	EV13	EV12	EV11	EV10	EV13	0			Event counter 1 (low-order 4 bits)
	R				EV12	0			
					EV11	0			
					EV10	0			
2FBH	EV17	EV16	EV15	EV14	EV17	0			Event counter 1 (high-order 4 bits)
	R				EV16	0			
					EV15	0			
					EV14	0			
2FCH	EVSEL	ENRUN	EV1RST	EV0RST	EVSEL	0	Separate	Phase	Event counter mode
					EVRUN	0	Run	Stop	Event counter Run/Stop
	R/W		W		EV1RST*3	Reset	Reset	–	Event counter 1 reset
					EV0RST*3	Reset	Reset	–	Event counter 0 reset

*1 Initial value at the time of initial reset
*2 Not set in the circuit
*3 Constantly "0" when being read
*4 Reset (0) immediately after being read
*5 Undefined

EV00–EV03: Event counter 0 Low-order (2F8H)
The four low-order data bits of event counter 0 are read out. These four bits are read-only, and cannot be used for writing. At initial reset, event counter 0 is set to "00H".

EV04–EV07: Event counter 0 High-order (2F9H)
The four high-order data bits of event counter 0 are read out. These four bits are read-only, and cannot be used for writing. At initial reset, event counter 0 is set to "00H".

EV10–EV13: Event counter 1 Low-order (2FAH)
The four low-order data bits of event counter 1 are read out. These four bits are read-only, and cannot be used for writing. At initial reset, event counter 1 is set to "00H".

EV14–EV17: Event counter 1 High-order (2FBH)
The four high-order data bits of event counter 1 are read out. These four bits are read-only, and cannot be used for writing. At initial reset, event counter 1 is set to "00H".

EV0RST: Event counter 0 reset (2FCH·D0)
This is the register for resetting event counter 0.

When "1" is written:	Event counter 0 reset
When "0" is written:	No operation
Read-out:	Always "0"

When "1" is written, event counter 0 is reset and the data becomes "00H". When "0" is written, no operation is executed. This is a write-only bit, and is always "0" at read-out.

EV1RST: Event counter 1 reset (2FCH·D1)
This is the register for resetting event counter 1.

When "1" is written:	Event counter 1 reset
When "0" is written:	No operation
Read-out:	Always "0"

When "1" is written, event counter 1 is reset and the data becomes "00H". When "0" is written, no operation is executed. This is a write-only bit, and is always "0" at read-out.

EVRUN: Event counter RUN/STOP (2FCH·D2)

This register controls the event counter RUN/STOP status.

When "1" is written:	RUN
When "0" is written:	STOP
Read-out:	Valid

When "1" is written, the event counter enters the RUN status and starts receiving the clock input.
When "0" is written, the event counter enters the STOP status and the clock input is ignored. (However, input to the input port is valid.)
At initial reset, this register is set to "0".

EVSEL: Event counter mode (2FCH·D3)

This register control the count mode of the event counter.

When "1" is written:	Separate
When "0" is written:	Phase detection
Read-out:	Valid

When "0" is written, the phases of the two clock signals are detected, and the phase detection mode is selected, in which one of the counters is chosen to input the clock signal.
When "1" is written, the separate mode is selected, in which each clock signal is input to different counters.
At initial reset, this register is set to "0".

Program examples

• Initial restart of event counter

```
ZEVC    EQU  2FCH
XEVIND  EQU  0111B
;
        LD   A,ZEVC SHR 8
        LD   XP,A
        LD   X,LOW ZEVC    ;SELECT EVSEL, EVRUN,
                           ; EVRST ADDR. BY X REG.
        OR   MX,XEVIND     ;EV. COUNTER RESET & START
```

This program initialized event counters 0 and 1, and enables them to receive the external clock.

• Reading out event counter

```
STD03A  EQU  010H
STD47A  EQU  012H
STD03B  EQU  014H
STD47B  EQU  016H
STD03C  EQU  018H
STD47C  EQU  01AH
ZEV0L   EQU  2F8H
;
        LD   A,ZEV0L SHR 8
        LD   XP,A
        LD   YP,A
;
RETRY   LD   Y,LOW STD03A ;SELECT BUF0-A ADDR. BY Y REG.
        LD   B,3          ;INIT. READ TIMES COUNTER
;
RDLP2   LD   A,4          ;INIT. WORD LEN. COUNTER
        LD   X,LOW ZEV0L  ;SELECT EV03 ADDR. BY X REG.
;
RDLP1   LDPY MY,MX        ;READ EV-CNT DATA TO BUF
        INC  X            ;INC. EV-CNT ADDR.
        ADD  A,0FH        ;DEC. WORD LEN. COUNTER
        JP   NZ,RDLP1     ;IF W.L.C <> 0 THEN JUMP
;
```

```
        ADD   B,0FH         ;DEC. READ TIMES COUNTER
        JP    NZ,RDLP2      ;IF R.T.C <> 0 THEN JUMP
;
        LD    X,LOW STD03A  ;SELECT BUF0-A ADDR. BY X REG.
        LD    Y,LOW STD03B  ;SELECT BUF0-B ADDR. BY Y REG.
        CALL  CPDATA        ;CALL ( COMP. BUF0-A BUF0-B )
        JP    BADCP1
;
NEXTCP  LD    X,LOW STD47A  ;SELECT BUF1-A ADDR. BY X REG.
        LD    Y,LOW STD47B  ;SELECT BUF1-B ADDR. BY Y REG.
        CALL  CPDATA        ;CALL ( COMP. BUF1-A BUF1-B )
        JP    BADCP2
;
        JP    READOK
;
BADCP1  LD    X,LOW STD03B  ;SELECT BUF0-B ADDR. BY X REG.
        LD    Y,LOW STD03C  ;SELECT BUF0-C ADDR. BY Y REG.
        CALL  CPDATA        ;CALL ( COMP. BUF0-B BUF0-C )
        JP    RETRY
;
        LD    X,LOW STD03A  ;SELECT BUF0-A ADDR. BY X REG.
        LD    Y,LOW STD03B  ;SELECT BUF0-B ADDR. BY Y REG.
        LDPX  MX,MY
        INC   Y
        LD    MX,MY         ;MOVE BUF0-A <= BUF0-B
        JP    NEXTCP
;
BADCP2  LD    X,LOW STD47B  ;SELECT BUF1-B ADDR. BY X REG.
        LD    Y,LOW STD47C  ;SELECT BUF1-C ADDR. BY Y REG.
        CALL  CPDATA        ;CALL ( COMP. BUF1-B BUF1-C )
        JP    RETRY
;
        LD    X,LOW STD47A  ;SELECT BUF1-A ADDR. BY X REG.
        LD    Y,LOW STD47B  ;SELECT BUF1-B ADDR. BY Y REG.
        LDPX  MX,MY
        INC   Y
        LD    MX,MY         ;MOVE BUF1-A <= BUF1-B
;
READOK  LD    X,LOW STD03A  ;SELECT EV-CNT DATA BUF.
;
```

```
;
;**********  SUB ROUTINE  **********
;
;
CPDATA  CP    MX,MY       ;COMP. LOW WORD DATA
        JP    NZ,BADDT    ;IF L-DATA DIFFERENT THEN JUMP
;
        INC   X           ;INC. BUF?-A OR BUF?-B
        INC   Y           ;INC. BUF?-B OR BUF?-C
        CP    MX,MY       ;COMP. HIGH WORD DATA
        JP    NZ,BADDT    ;IF H-DATA DIFFERENT THEN JUMP
;
        RETS              ;DATA EQUAL
;
BADDT   RET               ;DATA NOT EQUAL
```

In this program example, event counters 0 and 1 are read out three times each, their data compared, and the result stored in RAM at address "010H–013H". This operation assures a correct result even if data is read out when the counter is changing (carry). The RAM address "014H–01BH" is used as a work area for temporarily saving counter data. Also, the maximum input frequency that can be responded to is $f_{OSC1}/256$ Hz, on account of the software processing speed.

Table 6.9.2 shows the correspondence of event counters 0 and 1 and the data stored in RAM.

Table 6.9.2 Correspondence of event counters 0 and 1 and data stored in RAM

Address	Data bit			
	D3	D2	D1	D0
010H	EV03	EV02	EV01	EV00
011H	EV07	EV06	EV05	EV04
012H	EV13	EV12	EV11	EV10
013H	EV17	EV16	EV15	EV14

Programming notes

(1) After the event counter has written data to the EVRUN register, it operates or stops in synchronization with the falling edge of the noise rejector clock or stops. Hence, attention must be paid to the above timing when input signals (input to K02 and K03) are being received.

(2) To prevent erroneous reading of the event counter data, read out the counter data several times, compare it, and use the matching data as the result.

6.10 Battery Life Detection (BLD) Circuit

I/O memory map of BLD circuit

The control registers of the BLD circuit are shown in Table 6.10.1.

Table 6.10.1 I/O memory map (BLD circuit)

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
2E6H	HLMOD	BLD0	EISWIT1	EISWIT0	HLMOD	0	Heavy load	Normal	Heavy load protection mode register
					BLD0	0	Low	Normal	Sub-BLD evaluation data
	R/W	R	R/W		EISWIT1	0	Enable	Mask	Interrupt mask register (stopwatch 1 Hz)
					EISWIT0	0	Enable	Mask	Interrupt mask register (stopwatch 10 Hz)
2FFH	BLS	BLC2	BLC1	BLC0	BLS	0	On	Off	BLD On/Off
	BLD1				BLD1	0	Low	Normal	BLD voltage evaluation data
	W	R/W			BLC2	× *5			Evaluation voltage setting register
	R				BLC1	× *5			[BLC2–0] 0 1 2 3 4 5 6 7
					BLC0	× *5			E0C6235/62A35 2.20 2.25 2.30 2.35 2.40 2.45 2.50 2.55 (V)
									E0C62L35 1.05 1.10 1.15 1.20 1.25 1.30 1.35 1.40 (V)

*1 Initial value at the time of initial reset
*2 Not set in the circuit
*3 Constantly "0" when being read
*4 Reset (0) immediately after being read
*5 Undefined

HLMOD: Heavy load protection mode (2E6H·D3)

When "1" is written: Heavy load protection mode is set
When "0" is written: Heavy load protection mode is released
Read-out: Valid

When HLMOD is set to "1", the IC operating status enters the heavy load protection mode and at the same time the battery life detection of the BLD circuit is controlled (ON/OFF). For details about the heavy load protection mode, see section 6.11.

When HLMOD is set to "1", sampling control is executed for the BLD circuit ON time. There are two types of sampling time, as follows:

(1) The time of one instruction cycle immediately after HLMOD = "1"
(2) Sampling at cycles of 2 Hz output by the prescaler while HLMOD = "1"

The BLD circuit must be made ON with at least 100 µsec for the BLD circuit to respond. When the CPU system clock is fOSC3 in E0C62A35, the detection result at the timing in (1) above may be invalid or incorrect. Hence, when using timing (1) to execute battery life detection, be sure that the CPU clock is the OSC1 clock (for E0C62A35).
When BLD sampling is done with HLMOD set to "1", the results are written to the BLD latch in the timing as follows:

(1) As soon as the time has elapsed for one instruction cycle immediately following HLMOD = "1"
(2) Immediately on completion of sampling at cycles of 2 Hz output by the prescaler while HLMOD = "1"

Consequently, the BLD latch data is written immediately after HLMOD is set to "1", and at the same time the new detection result is written in 2 Hz cycles.

BLC0, BLC1, BLC2: Evaluation voltage setting register (2FFH·D0–D2)

In the E0C6235 Series, the evaluation voltage for judging the battery life can be switched by programming. Consequently, the optimum evaluation voltage can be set for the battery used.
One of eight evaluation voltages can be selected with the software. Table 6.10.2 lists the evaluation voltages for the models in the E0C6235 Series.

Table 6.10.2
Evaluation voltages for BLD circuit

Evaluation voltage setting			Evaluation voltage		
BLC2	BLC1	BLC0	E0C62L35	E0C6235	E0C62A35
0	0	0	1.05 V	2.20 V	2.20 V
0	0	1	1.10 V	2.25 V	2.25 V
0	1	0	1.15 V	2.30 V	2.30 V
0	1	1	1.20 V	2.35 V	2.35 V
1	0	0	1.25 V	2.40 V	2.40 V
1	0	1	1.30 V	2.45 V	2.45 V
1	1	0	1.35 V	2.50 V	2.50 V
1	1	1	1.40 V	2.55 V	2.55 V

BLS/BLD1: BLD detection/BLD data (2FFH·D3)

When "0" is written: BLD detection OFF
When "1" is written: BLD detection ON
When "0" is read out: Source voltage (V_{DD}–V_{SS}) is higher than BLD set value
When "1" is read out: Source voltage (V_{DD}–V_{SS}) is lower than BLD set value

Note that the function of this bit when written is different to when read out.
When this bit is written to, ON/OFF of the BLD detection operation is controlled; when this bit is read out, the result of the BLD detection (contents of BLD latch) is obtained.
Appreciable current is consumed during operation of BLD detection, so keep BLD detection OFF except when necessary.
When BLS is set to "1", BLD detection is executed. As soon as BLS is reset to "0" the detection result is loaded to the BLD latch. To obtain a stable BLD detection result, the BLD circuit must be set to ON with at least 100 µsec. Hence, to obtain the BLD detection result, follow the programming sequence below.

0. Set HLMOD to "1" (only when the CPU system clock is f_{OSC3} in E0C62A35)
1. Set BLS to "1"
2. Maintain at 100 µsec minimum
3. Set BLS to "0"
4. Read out BLD
5. Set HLMOD to "0" (only when the CPU system clock is f_{OSC3} in E0C62A35)

However, when a crystal oscillation clock (f_{OSC1}) is selected for the CPU system clock in E0C6235, E0C62L35 and E0C62A35, the instruction cycles are long enough, so that there is no need for concern about maintaining 100 µsec for the BLS = "1" with the software.

Program example

• Evaluation of source voltage 2.3 V (1.15 V)

```
ZOSC    EQU  2FEH
ZBLC    EQU  2FFH
XCLKCG  EQU  0100B
XBLDON  EQU  1010B
XBLDOF  EQU  0010B
;
        LD   A,ZOSC SHR 8
        LD   XP,A
        LD   X,LOW ZOSC         ;SELECT CLKCHG ADDR.
                                ; BY X REG.
        AND  MX,XCLKCG XOR 0FH  ;CLK CHANGE OSC3 TO OSC1
;
        LD   X,LOW ZBLC         ;SELECT BLS & BLC ADDR.
                                ; BY X REG.
        LD   MX,XBLDON          ;BLD ON & BLC <= 2
        LD   MX,XBLDOF          ;BLD OFF
;
        LD   A,MX               ;READ BLD1 DATA TO A REG.
```

In the program example, the three bits BLC0–2 are set to "2" to select the evaluation voltage 2.3 V (1.15 V); the BLD circuit is operated and the result read into the A register. If the CPU's operating clock is OSC3, this is switched to OSC1. Figure 6.10.1 shows the result of BLD detection.

Fig. 6.10.1
Result of BLD detection

A register

D3	D2	D1	D0
BLD1	BLC2	BLC1	BLC0

Programming notes

(1) It takes 100 µsec from the time the BLD circuit goes ON until a stable result is obtained. For this reason, keep the following software notes in mind:

① When the CPU system clock is f_{OSC1}

1. When detection is done at HLMOD
   After writing "1" on HLMOD, read the BLD after 1 instruction has passed.

2. When detection is done at BLS
   After writing "1" on BLS, write "0" after at least 100 µsec has lapsed (possible with the next instruction) and then read the BLD.

② When the CPU system clock is f_{OSC3}
(in case of E0C62A35 only)

1. When detection is done at HLMOD
   After writing "1" on HLMOD, read the BLD after 0.6 second has passed.
   (HLMOD holds "1" for at least 0.6 second)

2. When detection is done at BLS
   Before writing "1" on BLS, write "1" on HLMOD first; after at least 100 µsec has lapsed after writing "1" on BLS, write "0" on BLS and then read the BLD.

(2) To reduce current consumption, set the BLD operation to OFF unless otherwise necessary.

(3) BLS resides in the same bit at the same address as BLD1, and one or the other is selected by write or read operation. This means that arithmetic operations (AND, OR, ADD, SUB and so forth) cannot be used for BLS control.

(4) Select one of the following software processing to return to the normal mode after a heavy load has been driven in the heavy load protection mode in the E0C62L35.

① After heavy load drive is completed, return to the normal mode after at least one second has elapsed.

② After heavy load drive is completed, switch BLS ON and OFF (at least 100 µsec is necessary for the ON status) and then return to the normal mode.

The E0C6235/62A35 returns to the normal mode after driving a heavy load without special software processing.

(5) If the BLS is set to ON while the heavy load protection mode is in effect, keep the ON time within 10 msec.

(6) To reduce current consumption, be careful not to set the heavy load protection mode with the software unless otherwise necessary.

6.11 Heavy Load Protection Function and Sub-BLD Circuit

I/O memory map of heavy load protection function and sub-BLD circuit

The control registers of the heavy load protection function and sub-BLD circuit are shown in Table 6.11.1.

Table 6.11.1 I/O memory map (HLMOD and sub-BLD circuit)

Address	Register								Comment
	D3	D2	D1	D0	Name	Init *1	1	0	
2E6H	HLMOD	BLD0	EISWIT1	EISWIT0	HLMOD	0	Heavy load	Normal	Heavy load protection mode register
					BLD0	0	Low	Normal	Sub-BLD evaluation data
	R/W	R	R/W		EISWIT1	0	Enable	Mask	Interrupt mask register (stopwatch 1 Hz)
					EISWIT0	0	Enable	Mask	Interrupt mask register (stopwatch 10 Hz)
2FFH	BLS	BLC2	BLC1	BLC0	BLS	0	On	Off	BLD On/Off
	BLD1				BLD1	0	Low	Normal	BLD voltage evaluation data
					BLC2	× *5			Evaluation voltage setting register
	W	R/W			BLC1	× *5			[BLC2–0] 0 1 2 3 4 5 6 7
	R				BLC0	× *5			E0C6235/62A35 2.20 2.25 2.30 2.35 2.40 2.45 2.50 2.55 (V)
									E0C62L35 1.05 1.10 1.15 1.20 1.25 1.30 1.35 1.40 (V)

*1 Initial value at the time of initial reset
*2 Not set in the circuit
*3 Constantly "0" when being read
*4 Reset (0) immediately after being read
*5 Undefined

BLD0: Sub-BLD data (2E6H·D2)

When "0" is read out: High source voltage upward from about 2.4 V (E0C6235/62A35) /1.2 V (E0C62L35)

When "1" is read out: Low source voltage from about 2.4 V (E0C6235/62A35) /1.2 V (E0C62L35) or under

Writing: Invalid

When BLD0 is "1" the CPU enters the heavy load protection mode. In the heavy load protection mode, the detection operation of the BLD circuit and sub-BLD circuit is sampled in 2 Hz cycles, and the respective detection results are written to the BLD latch and sub-BLD latch.

HLMOD: Heavy load protection mode (2E6H·D3)	When "1" is written:	Heavy load protection mode is set
	When "0" is written:	Heavy load protection mode is released
	Read-out:	Valid

When HLMOD is set to "1", the IC operating status enters the heavy load protection mode and at the same time the battery life detection of the BLD circuit is controlled (ON/OFF).
When HLMOD is set to "1", sampling control is executed for the BLD circuit ON time. There are two types of sampling time, as follows:

(1) The time of one instruction cycle immediately after HLMOD = "1"

(2) Sampling at cycles of 2 Hz output by the prescaler while HLMOD = "1"

When BLD sampling is done with HLMOD set to "1", the results are written to the BLD latch in the timing as follows:

(1) As soon as the time has elapsed for one instruction cycle immediately following HLMOD = "1"

(2) Immediately on completion of sampling at cycles of 2 Hz output by the prescaler while HLMOD = "1"

Consequently, the BLD latch data is written immediately after HLMOD is set to "1", and at the same time the new detection result is written in 2 Hz cycles.

BLS/BLD1:	When "0" is written:	BLD detection OFF
BLD detection/BLD data	When "1" is written:	BLD detection ON
(2FFH·D3)	When "0" is read out:	Source voltage (V_{DD}–V_{SS}) is higher than BLD set value
	When "1" is read out:	Source voltage (V_{DD}–V_{SS}) is lower than BLD set value

Note that the function of this bit when written is different to when read out.
When this bit is written to, ON/OFF of the BLD detection operation is controlled; when this bit is read out, the result of the BLD detection (contents of BLD latch) is obtained.
Appreciable current is consumed during operation of BLD detection, so keep BLD detection OFF except when necessary.
When BLS is set to "1", BLD detection is executed. As soon as BLS is reset to "0" the detection result is loaded to the BLD latch.

Program example

The E0C62L35 and E0C6235/62A35 each have software processing for the heavy load protection function.

• Heavy load protection when buzzer sounds (E0C62L35)

```
ZBLDSI  EQU  2E6H
ZR1     EQU  2ECH
ZOSC    EQU  2FEH
ZBLC    EQU  2FFH
XHLMOD  EQU  1000B
XR1013  EQU  1001B
XCLKCG  EQU  0100B
XBLDON  EQU  1000B
XBLDOFF EQU  0000B
;
        LD   A,ZOSC SHR 8
        LD   XP,A
        LD   X,LOW ZOSC         ;SELECT CLKCHG ADDR. BY X REG.
        AND  MX,XCLKCG XOR 0FH  ;CLK CHANGE OSC3 TO OSC1
;
        LD   X,LOW ZBLDSI       ;SELECT HLMOD ADDR. BY X REG.
        OR   MX,XHLMOD          ;HLMOD ON
;
        LD   X,LOW ZR1          ;SELECT R1 ADDR. BY X REG.
        OR   MX,XR1013          ;BZ, BZ  ON
;
        LD   B,5
W30MS2  LD   A,15
W30MS1  ADD  A,0FH
        JP   NZ,W30MS1
        ADD  A,0FH              ;ABOUT 30 msec WAIT
        JP   NZ,W30MS2          ;( OSC1 = 32768 Hz )
;
        AND  MX,XR1013 XOR 0FH  ;BZ, BZ  OFF
;
        LD   X,LOW ZBLC         ;SELECT BLS ADDR. BY X REG.
        LD   MX,XBLDON          ;BLD ON
        LD   MX,XBLDOFF         ;BLD OFF
                                ; ( FOR HLMOD STATE HOLD )
;
        LD   X,LOW ZBLDSI       ;SELECT HLMOD ADDR. BY X REG.
        AND  MX,XHLMOD XOR 0FH  ;HLMOD OFF
```

In this program example, HLMOD is "1" while the buzzer sounds, so the heavy load is protected against. Also, BLS is set ON and OFF immediately before the heavy load protection mode is released. In this way, when the source voltage is under 1.2 V after the heavy load protection mode is released, the hardware maintains the heavy load protection mode until 1.2 V is reached.
Figure 6.11.1 is the timing chart for the operation of the heavy load protection mode.

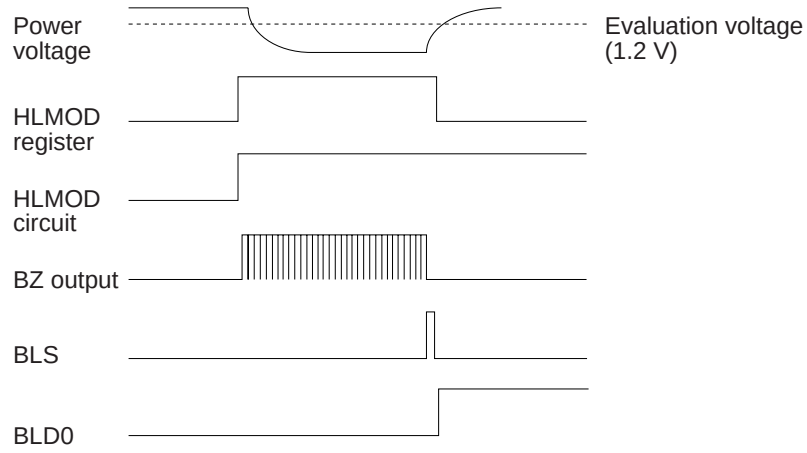


Fig. 6.11.1
Timing chart of operation of heavy load protection mode (E0C62L35)

• Heavy load protection when buzzer sounds (E0C6235/62A35)

```
ZBLDSI  EQU  2E6H
ZR1     EQU  2ECH
ZOSC    EQU  2FEH
XHLMOD  EQU  1000B
XR1013  EQU  1001B
XCLKCG  EQU  0100B
;
        LD   A,ZBLDSI SHR 8
        LD   XP,A
        LD   YP,A
        LD   X,LOW ZOSC        ;SELECT CLKCHG ADDR. BY X REG.
        AND  MX,XCLKCG XOR 0FH ;CLK CHANGE OSC3 TO OSC1
;
        LD   X,LOW ZBLDSI      ;SELECT HLMOD ADDR. BY X REG.
        OR   MX,XHLMOD         ;HLMOD ON
;
        LD   Y,LOW ZR1         ;SELECT R1 ADDR. BY Y REG.
        OR   MY,XR1013         ;BZ, BZ  ON
;
        CALL ST10MS            ;CALL (10 msec WAIT)
;
        AND  MY,XR1013 XOR 0FH ;BZ, BZ  OFF
        AND  MX,XHLMOD XOR 0FH ;HLMOD OFF
;
ST10MS  LD   A,0
        RDFz
ST10MS1 NOP7
        ADD  A,0FH
        JP   NZ,ST10MS1
        RET
```

The E0C6235 and E0C62A35 output a beep signal (BZ) for 10 msec in program examples of heavy load protection, then return to normal mode after driving the load (BZ output).

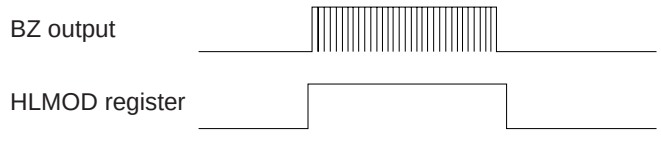


Fig. 6.11.2
Timing chart of operation of heavy load protection mode (E0C6235/62A35)

Programming notes

(1) It takes 100 µsec from the time the BLD circuit goes ON until a stable result is obtained. For this reason, keep the following software notes in mind:

① When the CPU system clock is f_{OSC1}

1. When detection is done at HLMOD
   After writing "1" on HLMOD, read the BLD after 1 instruction has passed.

2. When detection is done at BLS
   After writing "1" on BLS, write "0" after at least 100 µsec has lapsed (possible with the next instruction) and then read the BLD.

② When the CPU system clock is f_{OSC3}
(in case of E0C62A35 only)

1. When detection is done at HLMOD
   After writing "1" on HLMOD, read the BLD after 0.6 second has passed.
   (HLMOD holds "1" for at least 0.6 second)

2. When detection is done at BLS
   Before writing "1" on BLS, write "1" on HLMOD first; after at least 100 µsec has lapsed after writing "1" on BLS, write "0" on BLS and then read the BLD.

(2) BLS resides in the same bit at the same address as BLD1, and one or the other is selected by write or read operation. This means that arithmetic operations (AND, OR, ADD, SUB and so forth) cannot be used for BLS control.

(3) Select one of the following software processing to return to the normal mode after a heavy load has been driven in the heavy load protection mode in the E0C62L35.

① After heavy load drive is completed, return to the normal mode after at least one second has elapsed.

② After heavy load drive is completed, switch BLS ON and OFF (at least 100 µsec is necessary for the ON status) and then return to the normal mode.

The E0C6235/62A35 returns to the normal mode after driving a heavy load without special software processing.

(4) If the BLS is set to ON while the heavy load protection mode is in effect, keep the ON time within 10 msec.

(5) To reduce current consumption, be careful not to set the heavy load protection mode with the software unless otherwise necessary.

6.12 Analog Comparator

I/O memory map of analog comparator

The control registers of the analog comparator are shown in Table 6.12.1.

Table 6.12.1 I/O memory map (analog comparator)

Address	Register								Comment
	D3	D2	D1	D0	Name	Init *1	1	0	
2F7H	ENVON	ENVRT	AMPDT	AMPON	ENVON	0	On	Off	Envelope On/Off
					ENVRT	0	1.0 sec	0.5 sec	Envelope cycle selection register
	R/W		R	R/W	AMPDT	1	+ > -	+ < -	Analog comparator data
					AMPON	0	On	Off	Analog comparator On/Off

*1 Initial value at the time of initial reset
*2 Not set in the circuit
*3 Constantly "0" when being read
*4 Reset (0) immediately after being read
*5 Undefined

AMPON: Analog comparator ON/OFF (2F7H·D0)

Switches the analog comparator ON and OFF.

When "1" is written: The analog comparator goes ON
When "0" is written: The analog comparator goes OFF
Read-out: Valid

The analog comparator goes ON when "1" is written to AMPON, and OFF when "0" is written.
At initial reset, AMPON is set to "0".

AMPDT: Analog comparator data (2F7H·D1)

Reads out the output from the analog comparator.

When "1" is read out: AMPP (+) > AMPM (-)
When "0" is read out: AMPP (+) < AMPM (-)
Writing: Invalid

AMPDT is "0" when the input level of the inverted input terminal (AMPM) is greater than the input level of the noninverted input terminal (AMPP); and "1" when smaller.

Program example

• Setting the analog comparator ON and OFF, and reading data (when OSC1 is running)

```
ZOSC    EQU  2FEH
ZENAMP  EQU  2F7H
XCLKCHG EQU  1011B
XAMPON  EQU  0001B
XAMPOFF EQU  1110B
;
        LD   A,ZENAMP SHR 8;SET XP 2 PAGE
        LD   XP,A
        LD   X,LOW ZOSC    ;SELECT OSC ADDR. BY X REG.
        LD   B,MX          ;STORE OSC STATUS TO B REG.
        AND  MX,XCLKCHG    ;CLK CHANGE TO OSC1
;
        LD   X,LOW ZENAMP  ;SELECT ENAMP ADDR. BY X REG.
        LD   A,MX
        OR   MX,XAMPON     ;AMP CIRCUIT ON
        LD   A,8           ;3 msec DELAY
AMDLLP  ADD  A,0FH         ;DELAY LOOP
        JP   NZ,AMDLLP
;
        LD   A,MX          ;STORE THE RESULT TO A REG.
        AND  MX,XAMPOFF    ;AMP CIRCUIT OFF
        LD   X,LOW ZOSC    ;SELECT OSC ADDR. BY X REG.
        LD   MX,B          ;SET OSC STATUS TO
                           ; PREVIOUS CONDITION
```

In this program example, first sets the CPU clock to OSC1 (f_{OSC1} = 32.768 kHz), and then sets the AMP circuit to ON. Allows a delay, read the result into A register, sets the circuit to OFF, and switches the CPU clock to previous condition.

Programming notes

(1) To reduce current consumption, set the analog comparator to OFF when it is not necessary.

(2) After setting AMPON to "1", wait at least 3 msec for the operation of the analog comparator to stabilize before reading the output data of the analog comparator from AMPDT.

6.13 Serial Interface (SIN, SOUT, SCLK)

I/O memory map of serial interface

The control registers of the serial interface are shown in Table 6.13.1.

Table 6.13.1 I/O memory map (serial interface)

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
2F0H	SD3	SD2	SD1	SD0	SD3	× *5			Serial interface data register (low-order 4 bits)
					SD2	× *5			
					SD1	× *5			
	R/W				SD0	× *5			
2F1H	SD7	SD6	SD5	SD4	SD7	× *5			Serial interface data register (high-order 4 bits)
					SD6	× *5			
					SD5	× *5			
	R/W				SD4	× *5			
2F2H	SCS1	SCS0	SE2	EISIO	SCS1	1			SIF clock mode selection register [SCS1, 0]: 0 Clock, 1 CLK, 2 CLK/2, 3 CLK/4, slave
					SCS0	1			
					SE2	0	↑	↓	SIF clock edge selection register
	R/W				EISIO	0	Enable	Mask	Interrupt mask register (serial interface)
2F3H	0	0	IK2	ISIO	0 *3	– *2	–	–	Unused
					0 *3	– *2	–	–	Unused
	R				IK2 *4	0	Yes	No	Interrupt factor flag (K20–K23)
					ISIO *4	0	Yes	No	Interrupt factor flag (serial interface)
2E7H	SCTRG	EIK10	KCP10	K10	SCTRG*3	–	Trigger	–	Serial interface clock trigger
					EIK10	0	Enable	Mask	Interrupt mask register (K10)
	W	R/W		R	KCP10	0	↓	↑	Input comparison register (K10)
					K10	– *2	High	Low	Input port data (K10)
2ECH	R13	R12	R11	R10	R13	0	High/On	Low/Off	Output port (R13)/$\overline{BZ}$ output control
			SIOF		R12	0	High/On	Low/Off	Output port (R12)/FOUT output control
					R11	0	High	Low	Output port (R11, LAMP)
	R/W		R/W / R	R/W	SIOF	0	Run	Stop	Output port (SIOF)
					R10	0	High/On	Low/Off	Output port (R10)/BZ output control

*1 Initial value at the time of initial reset
*2 Not set in the circuit
*3 Constantly "0" when being read
*4 Reset (0) immediately after being read
*5 Undefined

SD0–SD3, SD4–SD7: Serial interface data registers (2F0H, 2F1H)

These registers are used for writing and reading serial data.

- **When writing data**

  When "1" is written: High level
  When "0" is written: Low level

  These registers write serial data to be output from the SOUT pin. The serially converted data is output from the SOUT pin as high (V_{DD}) when the bit is set to "1" and as low (V_{SS}) when the bit is set to "0".

- **When reading data**

  When "1" is read out: High level
  When "0" is read out: Low level

  Input serial data is read out from the SIN pin.
  These registers are loaded with data that has been parallel converted so that the high (V_{DD}) level bit input from the SIN pin is "1", and the low (V_{SS}) bit is "0".
  Perform data reading only while serial interface is halted (i.e., the synchronous clock is neither being input or output).

Data is undefined in this register at initial reset.

SCS1, SCS0: Clock mode selection register (2F2H·D3 and D2)

The synchronous clock (SCLK) of the serial interface can be selected with these registers.

Table 6.13.2
Synchronous clock selection

SCS1	SCS0	Mode	Synchronous clock
0	0	Master mode	CLK
0	1		CLK/2
1	0		CLK/4
1	1	Slave mode	External clock

CLK: CPU system clock

The synchronous clock (SCLK) can be selected from among the four types listed above, namely from three types of internal clock and one external clock.
At initial reset, the external clock is selected.

SE2: Clock edge selection register (2F2H·D1)

Timing for reading in the serial data input from the SIN pin can be selected with these registers.

When "1" is written:	SCLK rising edge
When "0" is written:	SCLK falling edge
Read-out:	Valid

These registers enable selection of whether to perform reading to the serial input data register (SD0–SD7) at the SCLK signal's rising edge (when "1" is written) or falling edge (when "0" is written).
Pay attention if the synchronous clock goes into reverse phase (SCLK→$\overline{\text{SCLK}}$) through the mask option.

SCLK rising = $\overline{\text{SCLK}}$ falling, SCLK falling = $\overline{\text{SCLK}}$ rising

When the internal clock is selected as the synchronous clock (SCLK), a hazard occurs in the synchronous clock (SCLK) when data is written to register SE2.
The timing for reading in the input data can be selected, but the output timing for the output data is fixed to the SCLK rising edge.
At initial reset, SCLK falling (SE2 = "0") is selected.

EISIO: Interrupt mask register (2F2H·D0)

The interrupt mask from the serial interface can be set with this register.

When "1" is written:	Enabled
When "0" is written:	Masked
Read-out:	Valid

At initial reset, the mask (EISIO = "0") is selected.

ISIO: Interrupt factor flag (2F3H·D0)

This flag indicates the status of the interrupt from the serial interface.

When "1" is read out:	Interrupt has occurred
When "0" is read out:	Interrupt has not occurred
Writing:	Invalid

By reading out this interrupt factor flag, the software can judge whether an interrupt from the serial interface has occurred. The interrupt factor flag is reset when it has been read out. Note, however, that even if the interrupt is masked, this flag will be set to "1" after the 8 bits data input/output.
The flag can be read out only when in the DI status (interrupt flag = "0").
At initial reset, this flag is set to "0".

SCTRG: Clock trigger (2E7H·D3)

This is the trigger for starting input or output of the synchronous clock (SCLK).

When "1" is written:	Trigger input
When "0" is written:	No operation
Read-out:	Always "0"

When this trigger is supplied to the serial interface activating circuit, the synchronous clock (SCLK) input/output is started.
As a trigger condition, it is required that data writing or reading on data registers SD0–SD7 be performed prior to writing "1" to SCTRG. (The internal circuit of the serial interface is initiated through data writing/reading on data registers SD0–SD7.)
Whenever the serial interface is in the RUN status, apply this trigger input once only. Refrain from performing trigger input multiple times, as this leads to malfunctioning.
Further, if the synchronous clock (SCLK) is the external clock, start the external clock input after the trigger input.

SIOF: Indicates the running status of the serial interface.

Special output port data (2ECH·D1)

When "1" is read out:	RUN status
When "0" is read out:	STOP status
Writing:	Invalid

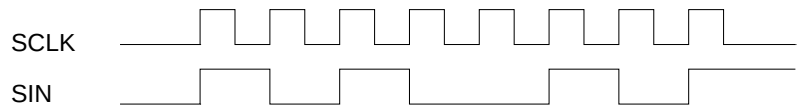
The RUN status is indicated from the end of writing "1" to SCTRG through to the end of serial data input/output.

Program examples

• Fetching data used by the internal clock

```
ZK10    EQU  2E7H
ZR1     EQU  2ECH
ZSDL    EQU  2F0H
ZSDH    EQU  2F1H
ZSC     EQU  2F2H
XSCTRG  EQU  1000B
XSIOF   EQU  0010B
XSCS    EQU  1100B
;
        LD   A,ZSC SHR 8
        LD   XP,A
        LD   X,LOW ZSC       ;SELECT SCS ADDR. BY X REG.
        AND  MX,XSCS XOR 0FH ;SET INTERNAL CLOCK MODE
                             ; ( CLK/1 )
;
        LD   X,LOW ZSDH      ;SELECT SD47 ADDR. BY X REG.
        LD   A,MX            ;INIT. CIRCUIT
;
        LD   X,LOW ZK10      ;SELECT SCTRG ADDR. BY X REG.
        OR   MX,XSCTRG       ;SHOT SCTRG
;
        LD   X,LOW ZR1       ;SELECT SIOF ADDR. BY X REG.
WAIT    FAN  MX,XSIOF        ;CHECK SIO STATUS
        JP   NZ,WAIT         ;IF SIO RUNNING THEN LOOP
;
        LD   X,LOW ZSDL      ;SELECT SD03 ADDR. BY X REG.
        LDPX A,MX            ;READ SD0-SD3 DATA TO A REG.
        LD   B,MX            ;READ SD4-SD7 DATA TO B REG.
```

The above program outputs to the outside a clock having the same frequency as the CPU system clock, and takes serial data into the general registers (A, B). Figure 6.13.1 shows an example of data being taken in when the mask option has been used to select SCLK = positive logic, permutation = MSB first, and R11 = SIOF.



B register

D3	D2	D1	D0
1	0	1	0

A register

D3	D2	D1	D0
0	1	0	1

Fig. 6.13.1 Example of fetching serial interface data

- **Output of data used by the external clock**

```
ZK10    EQU  2E7H
ZSDL    EQU  2F0H
ZSC     EQU  2F2H
XSCTRG  EQU  1000B
XSCS    EQU  1100B
;
        LD   A,ZSC SHR 8
        LD   XP,A
        LD   X,LOW ZSC    ;SELECT SCS ADDR. BY X REG.
        OR   MX,XSCS      ;SET EXTERNAL CLOCK MODE
;
        LD   X,LOW ZSDL   ;SELECT SD03 ADDR. BY X REG.
        LDPX MX,A         ;WRITE A REG. TO SD0-SD3
        LD   MX,B         ;WRITE B REG. TO SD4-SD7
;
        LD   X,LOW ZK10   ;SELECT SCTRG ADDR. BY X REG.
        OR   MX,XSCTRG    ;SHOT SCTRG
```

This program synchronizes SCLK with the external clock it is assigned to, and sends the contents of the general registers (A, B) to the outside. Figure 6.13.2 shows an output example when the mask option has been used to select SCLK = positive logic, permutation = MSB first, R11 = SIOF.

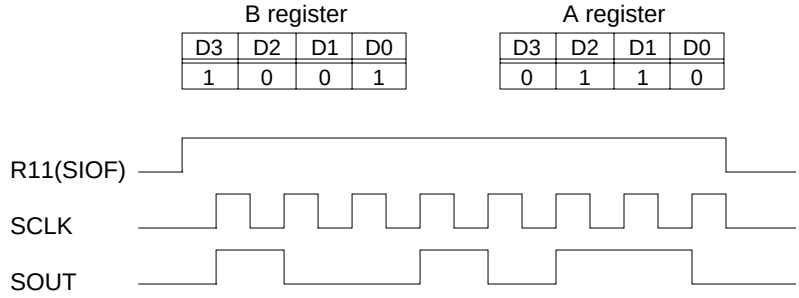


Fig. 6.13.2
Example of output of serial interface data

Programming notes

(1) When using the serial interface in the master mode, the synchronous clock uses the CPU system clock. Accordingly, do not change the system clock ($f_{OSC1} \leftrightarrow f_{OSC3}$) while the serial interface is operating.

(2) Perform data writing/reading to data registers SD0–SD7 only while the serial interface is halted (i.e., the synchronous clock is neither being input or output).

(3) As a trigger condition, it is required that data writing or reading on data registers SD0–SD7 be performed prior to writing "1" to SCTRG. (The internal circuit of the serial interface is initiated through data writing/reading on data registers SD0–SD7.) Supply trigger only once every time the serial interface is placed in the RUN state. Moreover, when the synchronous clock SCLK is external clock, start to input the external clock after the trigger.

(4) If the bit data of SE2 changes while SCLK is in the master mode, a hazard will be output to the SCLK pin. If this poses a problem for the system, be sure to set the SCLK to the external clock mode if the bit data of SE2 is to be changed.

(5) Reading the interrupt factor flag (ISIO) can be done only in the DI status (interrupt flag = "0"). Reading during EI status (interrupt flag = "1") will cause malfunction.

(6) Writing the interrupt mask register (EISIO) can be done only in the DI status (interrupt flag = "0"). Writing during EI status (interrupt flag = "1") will cause malfunction.

6.14 Sound Generator

I/O memory map of sound generator

The control registers of the sound generator are shown in Table 6.14.1.

Table 6.14.1 I/O memory map (sound generator)

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
2ECH	R13	R12	R11 / SIOF	R10	R13	0	High/On	Low/Off	Output port (R13)/$\overline{BZ}$ output control
					R12	0	High/On	Low/Off	Output port (R12)/FOUT output control
					R11	0	High	Low	Output port (R11, LAMP)
	R/W		R/W / R	R/W	SIOF	0	Run	Stop	Output port (SIOF)
					R10	0	High/On	Low/Off	Output port (R10)/BZ output control
2F6H	BZFQ2	BZFQ1	BZFQ0	ENVRST	BZFQ2	0			Buzzer frequency selection: [BZFQ2–0] 0 1 2 3 / Frequency f_{OSC1}/8 f_{OSC1}/10 f_{OSC1}/12 f_{OSC1}/14; [BZFQ2–0] 4 5 6 7 / Frequency f_{OSC1}/16 f_{OSC1}/20 f_{OSC1}/24 f_{OSC1}/28
					BZFQ1	0			
	R/W			W	BZFQ0	0			
					ENVRST*3	Reset	Reset	–	Envelope reset
2F7H	ENVON	ENVRT	AMPDT	AMPON	ENVON	0	On	Off	Envelope On/Off
					ENVRT	0	1.0 sec	0.5 sec	Envelope cycle selection register
	R/W		R	R/W	AMPDT	1	+ > -	+ < -	Analog comparator data
					AMPON	0	On	Off	Analog comparator On/Off

*1 Initial value at the time of initial reset
*2 Not set in the circuit
*3 Constantly "0" when being read
*4 Reset (0) immediately after being read
*5 Undefined

BZFQ0–BZFQ2: Buzzer frequency selection register (2F6H·D1–D3)

This is used to select the frequency of the buzzer signal. The frequencies of the buzzer signals (BZ, $\overline{BZ}$) are set by writing data to registers BZFQ0–BZFQ2.

Table 6.14.2 Buzzer frequency

BZFQ			Set frequency (Hz)		
2	1	0	Demultiplier ratio	When f_{OSC1} = 32 kHz	When f_{OSC1} = 38.4 kHz
0	0	0	$f_{OSC1}/8$	4,096.0	4,800.0
0	0	1	$f_{OSC1}/10$	3,276.8	3,840.0
0	1	0	$f_{OSC1}/12$	2,730.7	3,200.0
0	1	1	$f_{OSC1}/14$	2,340.6	2,742.9
1	0	0	$f_{OSC1}/16$	2,048.0	2,400.0
1	0	1	$f_{OSC1}/20$	1,638.4	1,920.0
1	1	0	$f_{OSC1}/24$	1,365.3	1,600.0
1	1	1	$f_{OSC1}/28$	1,170.3	1,371.4

Buzzer frequency is selected from the above eight types that have been divided by f_{OSC1} (oscillation frequency of the OSC1 oscillation circuit).
At initial reset, $f_{OSC1}/8$ (Hz) is selected.

Note *A hazard may be observed in the output waveform of the BZ and $\overline{BZ}$ signals when data of the buzzer frequency selection registers (BZFQ0–2) changes.*

ENVRST: Envelope reset (2F6H·D0)

This is the reset input to make the duty ratio of the buzzer signal the maximum.

When "1" is written: Reset input
When "0" is written: No operation
Read-out: Always "0"

When the envelope is added to the buzzer signal, the duty ratio is made maximum through this reset input. When the envelope is not added or when the buzzer signal is not output, the reset input is invalid.

ENVON: Envelope ON/OFF (2F7H·D3)

This controls adding the envelope to the buzzer signal.

When "1" is written:	Envelope added (ON)
When "0" is written:	No envelope (OFF)
Read-out:	Valid

The envelope is the digital envelope based on duty ratio control. When there is no envelope, the duty ratio is fixed to the maximum.
At initial reset, no envelope (OFF) is selected.

ENVRT: Envelope decay time (2F7H·D2)

This input selects the decay time of the envelope added to the buzzer signal.

When "1" is written:	1.0 sec (125 msec × 7 = 875 msec)
When "0" is written:	0.5 sec (62.5 msec × 7 = 437.5 msec)
Read-out:	Valid

The decay time of the digital envelope is decided by the time taken for the duty ratio to change. When "1" is written to ENVRT the time is 125 msec (8 Hz) units, and when "0" is written it is 62.5 msec (16 Hz) units.
At initial reset, 0.5 sec (437.5 msec) is selected.

R10, R13 (at BZ, $\overline{BZ}$ output selection): Special output port data (2ECH·D0 and D3)

These control output of the buzzer signals (BZ, $\overline{BZ}$).

When "1" is written:	Buzzer signal output
When "0" is written:	Low level (DC) output
Read-out:	Valid

- **$\overline{BZ}$ output under R13 control**
  BZ output and $\overline{BZ}$ output can be controlled independently. BZ output is controlled by writing data to register R10. $\overline{BZ}$ output is controlled by writing data to register R13.

- **$\overline{BZ}$ output under R10 control**
  By writing data to register R10 only, BZ output and $\overline{BZ}$ output can be controlled simultaneously. In this case, register R13 can be used as a read/write one-bit general register. This register does not affect $\overline{BZ}$ output (output to pin R13).

At initial reset, registers R10 and R13 are set to "0".

Program example

• Alarm sound

```
TCNT    EQU  210H
ZTM     EQU  2E0H
ZR1     EQU  2ECH
ZBZFQ   EQU  2F6H
;
        LD   A,TCNT SHR 8
        LD   XP,A
        LD   X,LOW TCNT     ;SELECT T-CNT ADDR. BY X REG.
        LD   MX,0           ;INIT. TIMING COUNTER ( RAM )
;
        LD   A,ZTM SHR 8
        LD   YP,A
        LD   Y,LOW ZTM      ;SELECT TM ADDR. BY Y REG.
        LD   A,MY           ;READ TM DATA TO A REG.
CKEDGE  LD   B,MY           ;READ TM DATA TO B REG.
        XOR  A,B
        FAN  A,0100B        ;CHECK EDGE OF 4 Hz SIGNAL
        LD   A,B            ;STORE NEW TM DATA
        JP   Z,CKEDGE       ;IF EDGE NO CHANGE THEN JUMP
;
        CP   MX,1           ;CHECK TIMING COUNTER
        JP   Z,INCPT        ;IF T-CNT = 1 THEN JUMP
        JP   NC,NEXT1       ;IF T-CNT > 1 THEN JUMP
;
        LD   X,LOW ZBZFQ    ;SELECT BZFQ ADDR. BY X REG.
        LBPX MX,10000001B   ;BZ 4 kHz, ENV. ON & RESET,
                            ; RT 0.5 sec
;
        LD   X,LOW ZR1      ;SELECT R1 ADDR. BY X REG.
        OR   MX,1001B       ;BZ, BZ ON
;
INCPT   LD   X,LOW TCNT     ;SELECT T-CNT ADDR. BY X REG.
        ADD  MX,1           ;INC. TIMING COUNTER
        JP   CKEDGE
;
NEXT1   CP   MX,2           ;CHECK TIMING COUNTER
        JP   NZ,NEXT2       ;IF T-CNT <> 2 THEN JUMP
;
```

```
        LD   X,LOW ZBZFQ   ;SELECT BZFQ ADDR. BY X REG.
        LBPX MX,10000011B  ;BZ 3.3 kHz, ENV. ON & RESET,
                           ; RT 0.5 sec
        JP   INCPT
;
NEXT2   CP   MX,8          ;CHECK TIMING COUNTER
        JP   C,INCPT       ;IF T-CNT < 8 THEN JUMP
;
        LD   X,LOW ZR1     ;SELECT R1 ADDR. BY X REG.
        AND  MX,0110B      ;BZ, BZ OFF
```

In the program example, the 1-second alarm is sounded. Figure 6.14.1 is the timing chart for the effective value of the output waveform.

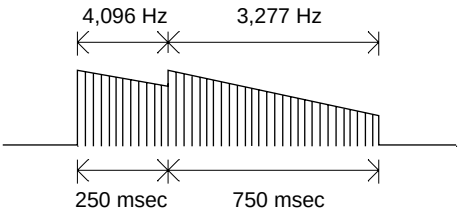


Fig. 6.14.1
Timing chart of effective value of output waveform

Programming note

A hazard may be observed in the output waveform of the BZ and $\overline{BZ}$ signals when data of the output registers (R10, R13) and the buzzer frequency selection registers (BZFQ0–2) changes.

6.15 Interrupt

I/O memory map of interrupt

The control registers of the interrupt are shown in Table 6.15.1.

Table 6.15.1 I/O memory map (interrupt)

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
2E4H	KCP03	KCP02	KCP01	KCP00	KCP03	0	↓	↑	Input comparison register (K00–K03)
					KCP02	0	↓	↑	
					KCP01	0	↓	↑	
	R/W				KCP00	0	↓	↑	
2E5H	EIK03	EIK02	EIK01	EIK00	EIK03	0	Enable	Mask	Interrupt mask register (K00–K03)
					EIK02	0	Enable	Mask	
					EIK01	0	Enable	Mask	
	R/W				EIK00	0	Enable	Mask	
2E6H	HLMOD	BLD0	EISWIT1	EISWIT0	HLMOD	0	Heavy load	Normal	Heavy load protection mode register
					BLD0	0	Low	Normal	Sub-BLD evaluation data
	R/W	R	R/W		EISWIT1	0	Enable	Mask	Interrupt mask register (stopwatch 1 Hz)
					EISWIT0	0	Enable	Mask	Interrupt mask register (stopwatch 10 Hz)
2E7H	SCTRG	EIK10	KCP10	K10	SCTRG*3	–	Trigger	–	Serial interface clock trigger
					EIK10	0	Enable	Mask	Interrupt mask register (K10)
	W	R/W		R	KCP10	0	↓	↑	Input comparison register (K10)
					K10	– *2	High	Low	Input port data (K10)
2E8H	CSDC	ETI2	ETI8	ETI32	CSDC	0	Static	Dynamic	LCD drive switch
					ETI2	0	Enable	Mask	Interrupt mask register (clock timer 2 Hz)
	R/W				ETI8	0	Enable	Mask	Interrupt mask register (clock timer 8 Hz)
					ETI32	0	Enable	Mask	Interrupt mask register (clock timer 32 Hz)
2E9H	0	TI2	TI8	TI32	0 *3	– *2	–	–	Unused
					TI2 *4	0	Yes	No	Interrupt factor flag (clock timer 2 Hz)
	R				TI8 *4	0	Yes	No	Interrupt factor flag (clock timer 8 Hz)
					TI32 *4	0	Yes	No	Interrupt factor flag (clock timer 32 Hz)
2EAH	IK1	IK0	SWIT1	SWIT0	IK1 *4	0	Yes	No	Interrupt factor flag (K10)
					IK0 *4	0	Yes	No	Interrupt factor flag (K00–K03)
	R				SWIT1 *4	0	Yes	No	Interrupt factor flag (stopwatch 1 Hz)
					SWIT0 *4	0	Yes	No	Interrupt factor flag (stopwatch 10 Hz)
2F2H	SCS1	SCS0	SE2	EISIO	SCS1	1			SIF clock mode selection register [SCS1, 0]: 0 = Clock, 1 = CLK, 2 = CLK/2, 3 = CLK/4, slave
					SCS0	1			
	R/W				SE2	0	↑	↓	SIF clock edge selection register
					EISIO	0	Enable	Mask	Interrupt mask register (serial interface)
2F3H	0	0	IK2	ISIO	0 *3	– *2	–	–	Unused
					0 *3	– *2	–	–	Unused
	R				IK2 *4	0	Yes	No	Interrupt factor flag (K20–K23)
					ISIO *4	0	Yes	No	Interrupt factor flag (serial interface)
2F5H	EIK23	EIK22	EIK21	EIK20	EIK23	0	Enable	Mask	Interrupt mask register (K20–K23)
					EIK22	0	Enable	Mask	
	R/W				EIK21	0	Enable	Mask	
					EIK20	0	Enable	Mask	

*1 Initial value at the time of initial reset
*2 Not set in the circuit
*3 Constantly "0" when being read
*4 Reset (0) immediately after being read
*5 Undefined

- **Interrupt factors**

  Table 6.15.2 shows the factors for generating interrupt requests.

  The interrupt flags are set to "1" depending on the corresponding interrupt factors.
  The CPU operation is interrupted when any of the conditions below set an interrupt factor flag to "1".

  - The corresponding mask register is "1" (enabled)
  - The interrupt flag is "1" (EI)

  The interrupt factor flag is a read-only register, but can be reset to "0" when the register data is read out.
  At initial reset, the interrupt factor flags are reset to "0".

Note *Read the interrupt factor flags only in the DI status (interrupt flag = "0"). A malfunction could result from read-out during the EI status (interrupt flag = "1").*

Table 6.15.2
Interrupt factors

Interrupt factor		Interrupt factor flag	
Clock timer	2 Hz falling edge	TI2	(2E9H·D2)
Clock timer	8 Hz falling edge	TI8	(2E9H·D1)
Clock timer	32 Hz falling edge	TI32	(2E9H·D0)
Stopwatch timer	1 Hz falling edge	SWIT1	(2EAH·D1)
Stopwatch timer	10 Hz falling edge	SWIT0	(2EAH·D0)
Serial interface	When 8-bit data input/output has completed	ISIO	(2F3H·D0)
Input data (K00–K03)	Rising or falling edge	IK0	(2EAH·D2)
Input data (K10)	Rising or falling edge	IK1	(2EAH·D3)
Input data (K20–K23)	Rising edge	IK2	(2F3H·D1)

- **Specific masks and factor flags for interrupt**

  The interrupt factor flags can be masked by the corresponding interrupt mask registers.
  The interrupt mask registers are read/write registers. They are enabled (interrupt authorized) when "1" is written to them, and masked (interrupt inhibited) when "0" is written to them.
  At initial reset, the interrupt mask register is set to "0".
  Table 6.15.3 shows the correspondence between interrupt mask registers and interrupt factor flags.

Table 6.15.3
Interrupt mask registers and interrupt factor flags

Interrupt mask register		Interrupt factor flag	
ETI2	(2E8H·D2)	TI2	(2E9H·D2)
ETI8	(2E8H·D1)	TI8	(2E9H·D1)
ETI32	(2E8H·D0)	TI32	(2E9H·D0)
EISWIT1	(2E6H·D1)	SWIT1	(2EAH·D1)
EISWIT0	(2E6H·D0)	SWIT0	(2EAH·D0)
EISIO	(2F2H·D0)	ISIO	(2F3H·D0)
EIK03	(2E5H·D3)	IK0	(2EAH·D2)
EIK02	(2E5H·D2)		
EIK01	(2E5H·D1)		
EIK00	(2E5H·D0)		
EIK10	(2E7H·D2)	IK1	(2EAH·D3)
EIK23	(2F5H·D3)	IK2	(2F3H·D1)
EIK22	(2F5H·D2)		
EIK21	(2F5H·D1)		
EIK20	(2F5H·D0)		

* There is an interrupt mask register for each pin of the input ports.

– ETI32, ETI8, ETI2: Interrupt mask registers (2E8H·D0–D2)
– TI32, TI8, TI2: Interrupt factor flags (2E9H·D0–D2)

See "6.7 Clock Timer".

– EISWIT0, EISWIT1: Interrupt mask registers (2E6H·D0–D1)
– SWIT0, SWIT1: Interrupt factor flags (2EAH·D0–D1)

See "6.8 Stopwatch Timer".

– EISI0: Interrupt mask register (2F2H·D0)
– ISI0: Interrupt factor flag (2F3H·D0)

See "6.13 Serial Interface".

– KCP00–KCP03: Input comparison registers (2E4H)
– EIK00–EIK03: Interrupt mask registers (2E5H)
– IK0: Interrupt factor flag (2EAH·D2)

See "6.3 Input Ports".

– KCP10: Input comparison register (2E7H·D1)
– EIK10: Interrupt mask register (2E7H·D2)
– IK1: Interrupt factor flag (2EAH·D3)

See "6.3 Input Ports".

– EIK20–EIK23: Interrupt mask registers (2F5H)
– IK2: Interrupt factor flag (2F3H·D1)

See "6.3 Input Ports".

Program example

• Interrupt vector processing

```
ZTI     EQU  2E9H
ZIKSW   EQU  2EAH
ZIK2SI  EQU  2F3H
ZR1     EQU  2ECH
ZOSC    EQU  2FEH
XTI2    EQU  0100B
XTI8    EQU  0010B
XTI32   EQU  0001B
XIK0    EQU  0100B
XIK1    EQU  1000B
XSWIT0  EQU  0001B
XSWIT1  EQU  0010B
XIK2    EQU  0010B
XISIO   EQU  0001B
XSIOF   EQU  0010B
XCLKCG  EQU  0100B
;
;
        ORG  101H
;
        JP   INTRPT       ;SIO
        JP   INTRPT       ;K0,K1,K2
        JP   INTRPT       ;K0,K1,K2,SIO
        JP   INTRPT       ;TM
        JP   INTRPT       ;TM,SIO
        JP   INTRPT       ;TM,K0,K1,K2
        JP   INTRPT       ;TM,K0,K1,K2,SIO
        JP   INTRPT       ;SW
        JP   INTRPT       ;SW,SIO
        JP   INTRPT       ;SW,K0,K1,K2
        JP   INTRPT       ;SW,K0,K1,K2,SIO
        JP   INTRPT       ;SW,TM
        JP   INTRPT       ;SW,TM,SIO
        JP   INTRPT       ;SW,TM,K0,K1,K2
        JP   INTRPT       ;SW,TM,K0,K1,K2,SIO
;
;
INTRPT  PUSH XP
        PUSH XH
        PUSH XL           ;STORE X REG. ( 12 Bits )
```

```
;
        PUSH  YP
        PUSH  YH            ;STORE Y REG. ( 12 Bits )
        PUSH  YL
;
        PUSH  B             ;STORE B REG.
        PUSH  A             ;STORE A REG.
        PUSH  F             ;STORE FLAG ( IDZC )
;
;
        LD    A,ZIKSW SHR 8
        LD    XP,A
        LD    X,LOW ZIKSW   ;SELECT IK0 IK1 SWIT ADDR. X REG.
        LD    A,MX
        LD    M0,A          ;STORE IK0 IK1 SWIT0 SWIT1
;
        FAN   A,XIK0        ;CHECK IK0
        JP    Z,CHKK1       ;IF IK0 = 0 THEN JUMP
        CALL  INTK0         ;CALL K0 INT. ROUTINE
;
CHKK1   LD    A,M0
        FAN   A,XIK1        ;CHECK IK1
        JP    Z,CHKSW0      ;IF IK1 = 0 THEN JUMP
        CALL  INTK1         ;CALL K1 INT. ROUTINE
;
CHKSW0  LD    A,M0
        FAN   A,XSWIT0      ;CHECK SWIT0
        JP    Z,CHKSW1      ;IF SWIT0 = 0 THEN JUMP
        CALL  INTSW0        ;CALL SW 10 Hz INT. ROUTINE
;
CHKSW1  LD    A,M0
        FAN   A,XSWIT1      ;CHECK SWIT1
        JP    Z,CHKT32      ;IF SWIT1 = 0 THEN JUMP
        CALL  INTSW1        ;CALL SW 1 Hz INT. ROUTINE
;
;
CHKT32  LD    A,ZTI SHR 8
        LD    XP,A
        LD    X,LOW ZTI     ;SELECT TI2 TI8 TI32 ADDR. X REG.
        LD    A,MX
        LD    M0,A          ;STORE TI2 TI8 TI32
```

```
;
        FAN   A,XTI32       ;CHECK TI32
        JP    Z,CHKT8       ;IF TI32 = 0 THEN JUMP
        CALL  INTT32        ;CALL TM 32 Hz INT. ROUTINE
;
CHKT8   LD    A,M0
        FAN   A,XTI8        ;CHECK TI8
        JP    Z,CHKT2       ;IF TI8 = 0 THEN JUMP
        CALL  INTT8         ;CALL TM 8 Hz INT. ROUTINE
;
CHKT2   LD    A,M0
        FAN   A,XTI2        ;CHECK TI2
        JP    Z,CKSIOF      ;IF TI2 = 0 THEN JUMP
        CALL  INTT2         ;CALL TM 2 Hz INT. ROUTINE
;
;
CKSIOF  LD    A,ZOSC SHR 8
        LD    XP,A
        LD    X,LOW ZOSC    ;SELECT CLKCHG ADDR. BY X REG.
        LD    A,MX          ;STORE CLKCHG
;
        AND   MX,XCLKCG XOR 0FH  ;CLK CHANGE OSC3 TO OSC1
;
        LD    B,11          ;SET 8 msec LOOP COUNTER
        LD    X,LOW ZR1     ;SELECT R1 ADDR. BY X REG.
;
LPSIOF  FAN   MX,XSIOF      ;CHECK SIOF
        JP    Z,CHKK2       ;IF SIOF = 0 THEN JUMP
        ADD   B,0FH         ;DEC. LOOP COUNTER
        JP    NZ,LPSIOF     ;IF LOOP COUNTER <> 0 THEN JUMP
;
;
CHKK2   LD    X,LOW ZOSC    ;SELECT CLKCHG ADDR. BY X REG.
        LD    MX,A          ;LOAD CLKCHG
;
        LD    X,LOW ZIK2SI  ;SELECT IK2 ISIO ADDR. BY X REG.
        LD    A,MX
        LD    M0,A          ;STORE IK2 ISIO
;
        FAN   A,XIK2        ;CHECK IK2
        JP    Z,CHKSIO      ;IF IK2 = 0 THEN JUMP
```

```
        CALL  INTK2
;
CHKSIO  LD    A,M0
        FAN   A,XISIO       ;CHECK ISIO
        JP    Z,INTEND      ;IF ISIO = 0 THEN JUMP
        CALL  INTSIO

;
;
INTEND  POP   F             ;LOAD FLAG ( IDZC )
        POP   A             ;LOAD A REG.
        POP   B             ;LOAD B REG.
;
        POP   YL
        POP   YH
        POP   YP            ;LOAD Y REG. ( 12 Bits )
;
        POP   XL
        POP   XH
        POP   XP            ;LOAD X REG. ( 12 Bits )
;
        EI                  ;ENABLE INTERRUPT
        RET
```

In the above interrupt vector program, the register data at the time of interrupt is saved, to be recovered when the interrupt processing ends; then the main routine is resumed.

Interrupt priority can be set by the software, interrupt nesting inhibited, and the processing executed in order of highest priority. The interrupt processing routine can be invoked by the CALL instruction for processing.

When the serial I/O ports are in operation, the interrupt factor flags IK2 and ISI0 (address 2F3H) cannot be read out. Their operating status can be monitored by the software, and if they are currently operating the read-out can be executed after waiting a maximum of 8 msec (32.768 kHz).

Table 6.15.4 shows the order of priority of interrupts in the program example.

Table 6.15.4
Order of interrupt priority in program example

Priority	Interrupt factor
1	K00–K03 input port
2	K10 input port
3	Stopwatch timer 10 Hz
4	Stopwatch timer 1 Hz
5	Clock timer 32 Hz
6	Clock timer 8 Hz
7	Clock timer 2 Hz
8	K20–K23 input port
9	Serial interface

Programming notes

(1) When the interrupt mask register (EIK) is set to "0", the interrupt factor flag (IK) of the input port cannot be set even though the pin status of the input port has changed.

(2) The interrupt factor flags of the clock timer, stopwatch timer and serial interface (TI, SWIT, ISIO) are set when the timing condition is established, even if the interrupt mask registers (ETI, EISWIT, EISIO) are set to "0".

(3) Read-out of the interrupt factor flags can be done only in the DI status (interrupt flag = "0"). Read-out during the EI status (interrupt flag = "1") will cause malfunction.

(4) Writing of the interrupt mask registers can be done only in the DI status (interrupt flag = "0"). Writing during the EI status (interrupt flag = "1") will cause malfunction.

CHAPTER 7 SUMMARY OF NOTES

Data Memory

The RAM, a data memory storing a variety of data, has a capacity of 480 words, each of four bits. When programming, keep the following points in mind.

(1) Part of the data memory can be used as stack area when saving subroutine calls and registers, so be careful not to overlap the data area and stack area.

(2) Subroutine calls and interrupts take up three words of the stack area.

(3) The data memory 000H–00FH is for the register pointers (RP), and is the addressable memory register area.

(4) The mask option can be used to select whether to assign the overall area of display memory to page 0 or page 2.
When page 0 (040H–06FH) is selected, read/write is enabled.
When page 2 (240H–26FH) is selected, write only is enabled.
If page 0 is assigned, RAM (040H–06FH) is 48 words, and is used as the segment area.

(5) Memory is not mounted in unused area within the memory map and in memory area not indicated in this manual. For this reason, normal operation cannot be assured for programs that have been prepared with access to these areas.

Watchdog Timer

When the watchdog timer is being used, the software must reset it within 3-second cycles, and timer data (WD0–WD2) cannot be used for timer applications.

Oscillation Circuit

(1) It takes at least 5 msec from the time the OSC3 oscillation circuit goes ON until the oscillation stabilizes. Consequently, when switching the CPU operation clock from OSC1 to OSC3, do this after a minimum of 5 msec have elapsed since the OSC3 oscillation went ON.

Further, the oscillation stabilization time varies depending on the external oscillator characteristics and conditions of use, so allow ample margin when setting the wait time.

(2) When switching the clock form OSC3 to OSC1, use a separate instruction for switching the OSC3 oscillation OFF. An error in the CPU operation can result if this processing is performed at the same time by the one instruction.

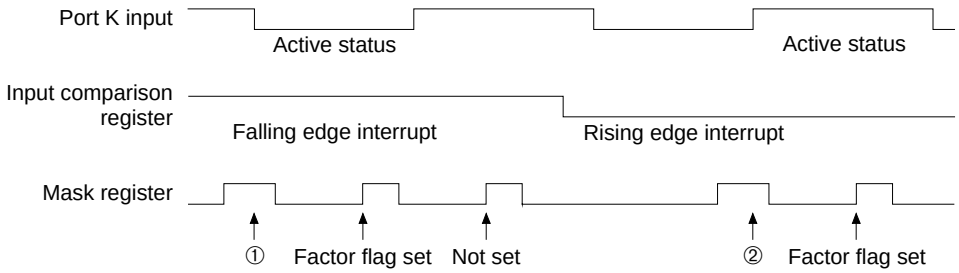
(3) To operate the clock timer and stopwatch timer accurately, select the prescaler of the OSC1 to match the crystal oscillator used.

Input Ports

(1) When input ports are changed from high to low by pull-down resistance, the fall of the waveform is delayed on account of the time constant of the pull-down resistance and input gate capacitance. Hence, when fetching input ports, set an appropriate wait time.
Particular care needs to be taken of the key scan during key matrix configuration. Aim for a wait time of about 1 msec.

(2) When "noise rejector circuit enable" is selected with the mask option, a maximum delay of 1 msec occurs from time the interrupt conditions are established until the interrupt factor flag (IK) is set to "1" (until the interrupt is actually generated).
Hence, pay attention to the timing when reading out (resetting) the interrupt factor flag.
For example, when performing a key scan with the key matrix, the key scan changes the input status to set the interrupt factor flag, so it has to be read out to reset it. However, if the interrupt factor flag is read out immediately after key scanning, the delay will cause the flag to be set after read-out, so that it will not be reset.

(3) Input interrupt programing related precautions



When the content of the mask register is rewritten, while the port K input is in the active status. The input interrupt factor flags are set at ① and ②, ① being the interrupt due to the falling edge and ② the interrupt due to the rising edge.

Fig. 7.1
Input interrupt timing

When using an input interrupt, if you rewrite the content of the mask register, when the value of the input terminal which becomes the interrupt input is in the active status, the factor flag for input interrupt may be set.
Therefore, when using the input interrupt, the active status of the input terminal implies

input terminal = low status, when the falling edge interrupt is effected and

input terminal = high status, when the rising edge interrupt is effected.

When an interrupt is triggered at the falling edge of an input terminal, a factor flag is set with the timing of ① shown in Figure 7.1. However, when clearing the content of the mask register with the input terminal kept in the low status and then setting it, the factor flag of the input interrupt is again set at the timing that has been set. Consequently, when the input terminal is in the active status (low status), do not rewrite the mask register (clearing, then setting the mask register), so that a factor flag will only set at the falling edge in this case. When clearing, then setting the mask register, set the mask register, when the input terminal is not in the active status (high status).
When an interrupt is triggered at the rising edge of the input terminal, a factor flag will be set at the timing of ② shown in Figure 7.1.

In this case, when the mask registers cleared, then set, you should set the mask register, when the input terminal is in the low status.
In addition, when the mask register = "1" and the content of the input comparison register is rewritten in the input terminal active status, an input interrupt factor flag may be set. Thus, you should rewrite the content of the input comparison register in the mask register = "0" status.

(4) Read-out of the interrupt factor flag (IK) can be done only in the DI status (interrupt flag = "0"). Read-out during EI status (interrupt flag = "1") will cause malfunction.

(5) Writing of the interrupt mask register (EIK) can be done only in the DI status (interrupt flag = "0"). Writing during EI status (interrupt flag = "1") will cause malfunction.

Output Ports When BZ, $\overline{BZ}$ and FOUT are selected with the mask option, a hazard may be observed in the output waveform when the data of the output register changes.

I/O Ports (1) When the I/O port is changed from high level to low level by the built-in pull down resistance, the falling-edge has the delay determined by the pull down resistance and the input gate capacitance. When the input data is being read out, the time that the input line is pulled down is equivalent to 1.5 cycles of the CPU system clock. However, the electric potential of the pins must be settled within 0.5 cycles. If this condition cannot be fulfilled, some measure must be devised such as arranging pull-down resistance externally, or performing multiple read-outs. Consequently, if data is read out while the CPU is running in the OSC3 oscillation circuit, data must be read out continuously for about 500 µsec.

(2) When the I/O port is set to the output mode and the data register has been read, the pin data instead of the register data can be read out. Because of this, if a low-impedance load is connected and read-out performed, the value of the register and the read-out result may differ.

LCD Driver

(1) When page 0 is selected for the display memory, the memory data and the display will not match until the area is initialized (through, for instance, memory clear processing by the CPU). Initialize the display memory by executing initial processing.

(2) When page 2 is selected for the display memory, that area becomes write-only. Consequently, data cannot be re-written by arithmetic operations (such as AND, OR, ADD, SUB).

Clock Timer

(1) The prescaler mode must be set correctly to suit the crystal oscillator to be used.

(2) When the clock timer has been reset, the interrupt factor flag (TI) may sometimes be set to "1". Consequently, perform flag read-out (reset the flag) as necessary at reset.

(3) The input clock of the watchdog timer is the 2 Hz signal of the clock timer, so that the watchdog timer may be counted up at timer reset.

(4) Read-out of the interrupt factor flag (IT) can be done only in the DI status (interrupt flag = "0"). Read-out during the EI status (interrupt flag = "1") will cause malfunctions.

(5) Writing of the interrupt mask register (EIT) can be done only in the DI status (interrupt flag = "0"). Writing during the EI status (interrupt flag = "1") will cause malfunctions.

Stopwatch Timer

(1) The prescaler mode must be set correctly so that the stopwatch timer suits the crystal oscillator to be used.

(2) If timer data is read out in the RUN status, the timer must be made into the STOP status, and after data is read out the RUN status can be restored. If data is read out when a carry occurs, the data cannot be read correctly.
Also, the processing above must be performed within the STOP interval of 976 µsec (256 Hz 1/4 cycle).

(3) Read-out of the interrupt factor flag (SWIT) can be done only in the DI status (interrupt flag = "0"). Read-out during the EI status (interrupt flag = "1") will cause malfunctions.

(4) Writing of the interrupt mask register (EISWIT) can be done only in the DI status (interrupt flag = "0"). Writing during the EI status (interrupt flag = "1") will cause malfunctions.

Event Counter

(1) After the event counter has written data to the EVRUN register, it operates or stops in synchronization with the falling edge of the noise rejector clock or stops. Hence, attention must be paid to the above timing when input signals (input to K02 and K03) are being received.

(2) To prevent erroneous reading of the event counter data, read out the counter data several times, compare it, and use the matching data as the result.

Battery Life Detection (BLD) Circuit

(1) It takes 100 µsec from the time the BLD circuit goes ON until a stable result is obtained. For this reason, keep the following software notes in mind:

① When the CPU system clock is f_{OSC1}

1. When detection is done at HLMOD
   After writing "1" on HLMOD, read the BLD after 1 instruction has passed.
2. When detection is done at BLS
   After writing "1" on BLS, write "0" after at least 100 µsec has lapsed (possible with the next instruction) and then read the BLD.

② When the CPU system clock is f_{OSC3}
(in case of E0C62A35 only)

1. When detection is done at HLMOD
   After writing "1" on HLMOD, read the BLD after 0.6 second has passed.
   (HLMOD holds "1" for at least 0.6 second)

2. When detection is done at BLS
   Before writing "1" on BLS, write "1" on HLMOD first; after at least 100 µsec has lapsed after writing "1" on BLS, write "0" on BLS and then read the BLD.

(2) To reduce current consumption, set the BLD operation to OFF unless otherwise necessary.

(3) BLS resides in the same bit at the same address as BLD1, and one or the other is selected by write or read operation. This means that arithmetic operations (AND, OR, ADD, SUB and so forth) cannot be used for BLS control.

(4) Select one of the following software processing to return to the normal mode after a heavy load has been driven in the heavy load protection mode in the E0C62L35.

① After heavy load drive is completed, return to the normal mode after at least one second has elapsed.

② After heavy load drive is completed, switch BLS ON and OFF (at least 100 µsec is necessary for the ON status) and then return to the normal mode.

The E0C6235/62A35 returns to the normal mode after driving a heavy load without special software processing.

(5) If the BLS is set to ON while the heavy load protection mode is in effect, keep the ON time within 10 msec.

(6) To reduce current consumption, be careful not to set the heavy load protection mode with the software unless otherwise necessary.

Heavy Load Protection Function and Sub-BLD Circuit

(1) It takes 100 µsec from the time the BLD circuit goes ON until a stable result is obtained. For this reason, keep the following software notes in mind:

① When the CPU system clock is f_{OSC1}

1. When detection is done at HLMOD
   After writing "1" on HLMOD, read the BLD after 1 instruction has passed.

2. When detection is done at BLS
   After writing "1" on BLS, write "0" after at least 100 µsec has lapsed (possible with the next instruction) and then read the BLD.

② When the CPU system clock is fOSC3
(in case of E0C62A35 only)

1. When detection is done at HLMOD
   After writing "1" on HLMOD, read the BLD after 0.6 second has passed.
   (HLMOD holds "1" for at least 0.6 second)

2. When detection is done at BLS
   Before writing "1" on BLS, write "1" on HLMOD first; after at least 100 µsec has lapsed after writing "1" on BLS, write "0" on BLS and then read the BLD.

(2) BLS resides in the same bit at the same address as BLD1, and one or the other is selected by write or read operation. This means that arithmetic operations (AND, OR, ADD, SUB and so forth) cannot be used for BLS control.

(3) Select one of the following software processing to return to the normal mode after a heavy load has been driven in the heavy load protection mode in the E0C62L35.

① After heavy load drive is completed, return to the normal mode after at least one second has elapsed.

② After heavy load drive is completed, switch BLS ON and OFF (at least 100 µsec is necessary for the ON status) and then return to the normal mode.

The E0C6235/62A35 returns to the normal mode after driving a heavy load without special software processing.

(4) If the BLS is set to ON while the heavy load protection mode is in effect, keep the ON time within 10 msec.

(5) To reduce current consumption, be careful not to set the heavy load protection mode with the software unless otherwise necessary.

Analog Comparator

(1) To reduce current consumption, set the analog comparator to OFF when it is not necessary.

(2) After setting AMPON to "1", wait at least 3 msec for the operation of the analog comparator to stabilize before reading the output data of the analog comparator from AMPDT.

Serial Interface

(1) When using the serial interface in the master mode, the synchronous clock uses the CPU system clock. Accordingly, do not change the system clock ($f_{OSC1} \leftrightarrow f_{OSC3}$) while the serial interface is operating.

(2) Perform data writing/reading to data registers SD0–SD7 only while the serial interface is halted (i.e., the synchronous clock is neither being input or output).

(3) As a trigger condition, it is required that data writing or reading on data registers SD0–SD7 be performed prior to writing "1" to SCTRG. (The internal circuit of the serial interface is initiated through data writing/reading on data registers SD0–SD7.) Supply trigger only once every time the serial interface is placed in the RUN state. Moreover, when the synchronous clock SCLK is external clock, start to input the external clock after the trigger.

(4) If the bit data of SE2 changes while SCLK is in the master mode, a hazard will be output to the SCLK pin. If this poses a problem for the system, be sure to set the SCLK to the external clock mode if the bit data of SE2 is to be changed.

(5) Reading the interrupt factor flag (ISIO) can be done only when the serial interface is in the STOP status (SIOF = "0") and the DI status (interrupt flag = "0"). If reading is performed while the serial interface is in the RUN mode (during input or output), the data input or output will be suspended and the initial status resumed. Reading during EI status (interrupt flag = "1") will cause malfunction.

(6) Writing the interrupt mask register (EISIO) can be done only in the DI status (interrupt flag = "0"). Writing during EI status (interrupt flag = "1") will cause malfunction.

Sound Generator A hazard may be observed in the output waveform of the BZ and $\overline{BZ}$ signals when data of the output registers (R10, R13) and the buzzer frequency selection registers (BZFQ0–2) changes.

Interrupt

(1) When the interrupt mask register (EIK) is set to "0", the interrupt factor flag (IK) of the input port cannot be set even though the pin status of the input port has changed.

(2) The interrupt factor flags of the clock timer, stopwatch timer and serial interface (TI, SWIT, ISIO) are set when the timing condition is established, even if the interrupt mask registers (ETI, EISWIT, EISIO) are set to "0".

(3) Read-out of the interrupt factor flags can be done only in the DI status (interrupt flag = "0"). Read-out during the EI status (interrupt flag = "1") will cause malfunction.

(4) Writing of the interrupt mask registers can be done only in the DI status (interrupt flag = "0"). Writing during the EI status (interrupt flag = "1") will cause malfunction.

APPENDIX A E0C6235 DATA MEMORY (RAM) MAP

PROGRAM NAME : C235

P	H	L	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	0	NAME																
		MSB																
		LSB																
	1	NAME																
		MSB																
		LSB																
	2	NAME																
		MSB																
		LSB																
	3	NAME																
		MSB																
		LSB																
	4	NAME																
		MSB																
		LSB																
	5	NAME																
		MSB																
		LSB																
	6	NAME																
		MSB																
		LSB																
	7	NAME																
		MSB																
		LSB																

PROGRAM NAME : C235																		
P	H	L	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	8	NAME																
		MSB																
		LSB																
	9	NAME																
		MSB																
		LSB																
	A	NAME																
		MSB																
		LSB																
	B	NAME																
		MSB																
		LSB																
	C	NAME																
		MSB																
		LSB																
	D	NAME																
		MSB																
		LSB																
	E	NAME																
		MSB																
		LSB																
	F	NAME																
		MSB																
		LSB																

PROGRAM NAME : C235																	
P	H	L	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
1	0	NAME																
		MSB																
		LSB																
	1	NAME																
		MSB																
		LSB																
	2	NAME																
		MSB																
		LSB																
	3	NAME																
		MSB																
		LSB																
	4	NAME																
		MSB																
		LSB																
	5	NAME																
		MSB																
		LSB																
	6	NAME																
		MSB																
		LSB																
	7	NAME																
		MSB																
		LSB																

PROGRAM NAME : C235																		
P	H	L	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
1	8	NAME																
		MSB																
		LSB																
	9	NAME																
		MSB																
		LSB																
	A	NAME																
		MSB																
		LSB																
	B	NAME																
		MSB																
		LSB																
	C	NAME																
		MSB																
		LSB																
	D	NAME																
		MSB																
		LSB																
	E	NAME																
		MSB																
		LSB																
	F	NAME																
		MSB																
		LSB																

PROGRAM NAME : C235

P	H	L	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
2	0	NAME																
		MSB																
		LSB																
	1	NAME																
		MSB																
		LSB																
	2	NAME																
		MSB																
		LSB																
	3	NAME																
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	4	NAME																
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		LSB																
	5	NAME																
		MSB																
		LSB																
	6	NAME																
		MSB																
		LSB																
	7	NAME																
		MSB																
		LSB																

PROGRAM NAME : C235

P	H	L	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
2	8	NAME																
		MSB																
		LSB																
	9	NAME																
		MSB																
		LSB																
	A	NAME																
		MSB																
		LSB																
	B	NAME																
		MSB																
		LSB																
	C	NAME																
		MSB																
		LSB																
	D	NAME																
		MSB																
		LSB																
	E	NAME	ZTM	ZSWL	ZSWH	ZK0	ZKCP0	ZEIK0	ZBLDSI	ZK10	ZETI	ZTI	ZIKSW	ZR0	ZR1	ZP0	ZSWC	ZWDT
		MSB	TM3	SWL3	SWH3	K03	KCP03	EIK03	HLMOD	SCTRG	CSDC	------	IK1	R03	R13	P03	TMRST	WDRST
			TM2	SWL2	SWH2	K02	KCP02	EIK02	BLD0	EIK10	ETI2	TI2	IK0	R02	R12	P02	SWRUN	WD2
			TM1	SWL1	SWH1	K01	KCP01	EIK01	EISWI1	KCP10	ETI8	TI8	SWIT1	R01	R11/SF	P01	SWRST	WD1
		LSB	TM0	SWL0	SWH0	K00	KCP00	EIK00	EISWI0	K10	ETI32	TI32	SWIT0	R00	R10	P00	IOC0	WD0
	F	NAME	ZSDL	ZSDH	ZSC	ZIK2SI	ZK2	ZEIK2	ZBZFQ	ZENAMP	ZEV0L	ZEV0H	ZEV1L	ZEV1H	ZEVC	ZP1	ZOSC	ZBLC
		MSB	SD3	SD7	SCS1	------	K23	EIK23	BZFQ2	ENVON	EV03	EV07	EV13	EV17	EVSEL	P13	PRSM	BLS/D1
			SD2	SD6	SCS0	------	K22	EIK22	BZFQ1	ENVRT	EV02	EV06	EV12	EV16	EVRUN	P12	CLKCHG	BLC2
			SD1	SD5	SE2	IK2	K21	EIK21	BZFQ0	AMPDT	EV01	EV05	EV11	EV15	EV1RST	P11	OSCC	BLC1
		LSB	SD0	SD4	EISIO	ISIO	K20	EIK20	ENVRST	AMPON	EV00	EV04	EV10	EV14	EV0RST	P10	IOC1	BLC0

APPENDIX B E0C6235 INSTRUCTION SET

Instruction Set (1)

Classification	Mnemonic	Operand	Operation Code												Flag				Clock	Operation
			B	A	9	8	7	6	5	4	3	2	1	0	I	D	Z	C		
Branch instructions	PSET	p	1	1	1	0	0	1	0	p4	p3	p2	p1	p0					5	NBP ← p4, NPP ← p3~p0
	JP	s	0	0	0	0	s7	s6	s5	s4	s3	s2	s1	s0					5	PCB ← NBP, PCP ← NPP, PCS ← s7~s0
		C, s	0	0	1	0	s7	s6	s5	s4	s3	s2	s1	s0					5	PCB ← NBP, PCP ← NPP, PCS ← s7~s0 if C=1
		NC, s	0	0	1	1	s7	s6	s5	s4	s3	s2	s1	s0					5	PCB ← NBP, PCP ← NPP, PCS ← s7~s0 if C=0
		Z, s	0	1	1	0	s7	s6	s5	s4	s3	s2	s1	s0					5	PCB ← NBP, PCP ← NPP, PCS ← s7~s0 if Z=1
		NZ, s	0	1	1	1	s7	s6	s5	s4	s3	s2	s1	s0					5	PCB ← NBP, PCP ← NPP, PCS ← s7~s0 if Z=0
	JPBA		1	1	1	1	1	1	1	0	1	0	0	0					5	PCB ← NBP, PCP ← NPP, PCSH ← B, PCSL ← A
	CALL	s	0	1	0	0	s7	s6	s5	s4	s3	s2	s1	s0					7	M(SP-1) ← PCP, M(SP-2) ← PCSH, M(SP-3) ← PCSL+1 SP ← SP-3, PCP ← NPP, PCS ← s7~s0
	CALZ	s	0	1	0	1	s7	s6	s5	s4	s3	s2	s1	s0					7	M(SP-1) ← PCP, M(SP-2) ← PCSH, M(SP-3) ← PCSL+1 SP ← SP-3, PCP ← 0, PCS ← s7~s0
	RET		1	1	1	1	1	1	0	1	1	1	1	1					7	PCSL ← M(SP), PCSH ← M(SP+1), PCP ← M(SP+2) SP ← SP+3
	RETS		1	1	1	1	1	1	0	1	1	1	1	0					12	PCSL ← M(SP), PCSH ← M(SP+1), PCP ← M(SP+2) SP ← SP+3, PC ← PC+1
	RETD	*l*	0	0	0	1	*l*7	*l*6	*l*5	*l*4	*l*3	*l*2	*l*1	*l*0					12	PCSL ← M(SP), PCSH ← M(SP+1), PCP ← M(SP+2) SP ← SP+3, M(X) ← *l*3~*l*0, M(X+1) ← *l*7~*l*4, X ← X+2
System control instructions	NOP5		1	1	1	1	1	1	1	1	1	0	1	1					5	No operation (5 clock cycles)
	NOP7		1	1	1	1	1	1	1	1	1	1	1	1					7	No operation (7 clock cycles)
	HALT		1	1	1	1	1	1	1	1	1	0	0	0					5	Halt (stop clock)
Index operation instructions	INC	X	1	1	1	0	1	1	1	0	0	0	0	0					5	X ← X+1
		Y	1	1	1	0	1	1	1	1	0	0	0	0					5	Y ← Y+1
	LD	X, x	1	0	1	1	x7	x6	x5	x4	x3	x2	x1	x0					5	XH ← x7~x4, XL ← x3~x0
		Y, y	1	0	0	0	y7	y6	y5	y4	y3	y2	y1	y0					5	YH ← y7~y4, YL ← y3~y0
		XP, r	1	1	1	0	1	0	0	0	0	0	r1	r0					5	XP ← r
		XH, r	1	1	1	0	1	0	0	0	0	1	r1	r0					5	XH ← r
		XL, r	1	1	1	0	1	0	0	0	1	0	r1	r0					5	XL ← r
		YP, r	1	1	1	0	1	0	0	1	0	0	r1	r0					5	YP ← r
		YH, r	1	1	1	0	1	0	0	1	0	1	r1	r0					5	YH ← r
		YL, r	1	1	1	0	1	0	0	1	1	0	r1	r0					5	YL ← r
		r, XP	1	1	1	0	1	0	1	0	0	0	r1	r0					5	r ← XP
		r, XH	1	1	1	0	1	0	1	0	0	1	r1	r0					5	r ← XH
		r, XL	1	1	1	0	1	0	1	0	1	0	r1	r0					5	r ← XL
		r, YP	1	1	1	0	1	0	1	1	0	0	r1	r0					5	r ← YP
		r, YH	1	1	1	0	1	0	1	1	0	1	r1	r0					5	r ← YH
		r, YL	1	1	1	0	1	0	1	1	1	0	r1	r0					5	r ← YL
	ADC	XH, i	1	0	1	0	0	0	0	0	i3	i2	i1	i0			↕	↕	7	XH ← XH+i3~i0+C
		XL, i	1	0	1	0	0	0	0	1	i3	i2	i1	i0			↕	↕	7	XL ← XL+i3~i0+C
		YH, i	1	0	1	0	0	0	1	0	i3	i2	i1	i0			↕	↕	7	YH ← YH+i3~i0+C
		YL, i	1	0	1	0	0	0	1	1	i3	i2	i1	i0			↕	↕	7	YL ← YL+i3~i0+C

Instruction Set (2)

Classification	Mnemonic	Operand	Operation Code												Flag				Clock	Operation
			B	A	9	8	7	6	5	4	3	2	1	0	I	D	Z	C		
Index operation instructions	CP	XH, i	1	0	1	0	0	1	0	0	i3	i2	i1	i0			↕	↕	7	XH-i3~i0
		XL, i	1	0	1	0	0	1	0	1	i3	i2	i1	i0			↕	↕	7	XL-i3~i0
		YH, i	1	0	1	0	0	1	1	0	i3	i2	i1	i0			↕	↕	7	YH-i3~i0
		YL, i	1	0	1	0	0	1	1	1	i3	i2	i1	i0			↕	↕	7	YL-i3~i0
Data transfer instructions	LD	r, i	1	1	1	0	0	0	r1	r0	i3	i2	i1	i0					5	r←i3~i0
		r, q	1	1	1	0	1	1	0	0	r1	r0	q1	q0					5	r←q
		A, Mn	1	1	1	1	1	0	1	0	n3	n2	n1	n0					5	A←M(n3~n0)
		B, Mn	1	1	1	1	1	0	1	1	n3	n2	n1	n0					5	B←M(n3~n0)
		Mn, A	1	1	1	1	1	0	0	0	n3	n2	n1	n0					5	M(n3~n0)←A
		Mn, B	1	1	1	1	1	0	0	1	n3	n2	n1	n0					5	M(n3~n0)←B
	LDPX	MX, i	1	1	1	0	0	1	1	0	i3	i2	i1	i0					5	M(X)←i3~i0, X←X+1
		r, q	1	1	1	0	1	1	1	0	r1	r0	q1	q0					5	r←q, X←X+1
	LDPY	MY, i	1	1	1	0	0	1	1	1	i3	i2	i1	i0					5	M(Y)←i3~i0, Y←Y+1
		r, q	1	1	1	0	1	1	1	1	r1	r0	q1	q0					5	r←q, Y←Y+1
	LBPX	MX, *l*	1	0	0	1	*l*7	*l*6	*l*5	*l*4	*l*3	*l*2	*l*1	*l*0					5	M(X)←*l*3~*l*0, M(X+1)←*l*7~*l*4, X←X+2
Flag operation instructions	SET	F, i	1	1	1	1	0	1	0	0	i3	i2	i1	i0	↑	↑	↑	↑	7	F←F∨i3~i0
	RST	F, i	1	1	1	1	0	1	0	1	i3	i2	i1	i0	↓	↓	↓	↓	7	F←F∧i3~i0
	SCF		1	1	1	1	0	1	0	0	0	0	0	1				↑	7	C←1
	RCF		1	1	1	1	0	1	0	1	1	1	1	0				↓	7	C←0
	SZF		1	1	1	1	0	1	0	0	0	0	1	0			↑		7	Z←1
	RZF		1	1	1	1	0	1	0	1	1	1	0	1			↓		7	Z←0
	SDF		1	1	1	1	0	1	0	0	0	1	0	0		↑			7	D←1 (Decimal Adjuster ON)
	RDF		1	1	1	1	0	1	0	1	1	0	1	1		↓			7	D←0 (Decimal Adjuster OFF)
	EI		1	1	1	1	0	1	0	0	1	0	0	0	↑				7	I ←1 (Enables Interrupt)
	DI		1	1	1	1	0	1	0	1	0	1	1	1	↓				7	I ←0 (Disables Interrupt)
Stack operation instructions	INC	SP	1	1	1	1	1	1	0	1	1	0	1	1					5	SP←SP+1
	DEC	SP	1	1	1	1	1	1	0	0	1	0	1	1					5	SP←SP-1
	PUSH	r	1	1	1	1	1	1	0	0	0	0	r1	r0					5	SP←SP-1, M(SP)←r
		XP	1	1	1	1	1	1	0	0	0	1	0	0					5	SP←SP-1, M(SP)←XP
		XH	1	1	1	1	1	1	0	0	0	1	0	1					5	SP←SP-1, M(SP)←XH
		XL	1	1	1	1	1	1	0	0	0	1	1	0					5	SP←SP-1, M(SP)←XL
		YP	1	1	1	1	1	1	0	0	0	1	1	1					5	SP←SP-1, M(SP)←YP
		YH	1	1	1	1	1	1	0	0	1	0	0	0					5	SP←SP-1, M(SP)←YH
		YL	1	1	1	1	1	1	0	0	1	0	0	1					5	SP←SP-1, M(SP)←YL
		F	1	1	1	1	1	1	0	0	1	0	1	0					5	SP←SP-1, M(SP)←F
	POP	r	1	1	1	1	1	1	0	1	0	0	r1	r0					5	r←M(SP), SP←SP+1
		XP	1	1	1	1	1	1	0	1	0	1	0	0					5	XP←M(SP), SP←SP+1
		XH	1	1	1	1	1	1	0	1	0	1	0	1					5	XH←M(SP), SP←SP+1
		XL	1	1	1	1	1	1	0	1	0	1	1	0					5	XL←M(SP), SP←SP+1
		YP	1	1	1	1	1	1	0	1	0	1	1	1					5	YP←M(SP), SP←SP+1

Instruction Set (3)

Classification	Mnemonic	Operand	Operation Code												Flag				Clock	Operation
			B	A	9	8	7	6	5	4	3	2	1	0	I	D	Z	C		
Stack operation instructions	POP	YH	1	1	1	1	1	1	0	1	1	0	0	0					5	YH← M(SP), SP← SP+1
		YL	1	1	1	1	1	1	0	1	1	0	0	1					5	YL← M(SP), SP← SP+1
		F	1	1	1	1	1	1	0	1	1	0	1	0	↕	↕	↕	↕	5	F← M(SP), SP← SP+1
	LD	SPH, r	1	1	1	1	1	1	1	0	0	0	r1	r0					5	SPH← r
		SPL, r	1	1	1	1	1	1	1	1	0	0	r1	r0					5	SPL ← r
		r, SPH	1	1	1	1	1	1	1	0	0	1	r1	r0					5	r← SPH
		r, SPL	1	1	1	1	1	1	1	1	0	1	r1	r0					5	r← SPL
Arithmetic instructions	ADD	r, i	1	1	0	0	0	0	r1	r0	i3	i2	i1	i0	★	↕	↕		7	r← r+i3~i0
		r, q	1	0	1	0	1	0	0	0	r1	r0	q1	q0	★	↕	↕		7	r← r+q
	ADC	r, i	1	1	0	0	0	1	r1	r0	i3	i2	i1	i0	★	↕	↕		7	r← r+i3~i0+C
		r, q	1	0	1	0	1	0	0	1	r1	r0	q1	q0	★	↕	↕		7	r← r+q+C
	SUB	r, q	1	0	1	0	1	0	1	0	r1	r0	q1	q0	★	↕	↕		7	r← r-q
	SBC	r, i	1	1	0	1	0	1	r1	r0	i3	i2	i1	i0	★	↕	↕		7	r← r-i3~i0-C
		r, q	1	0	1	0	1	0	1	1	r1	r0	q1	q0	★	↕	↕		7	r← r-q-C
	AND	r, i	1	1	0	0	1	0	r1	r0	i3	i2	i1	i0		↕			7	r← r∧i3~i0
		r, q	1	0	1	0	1	1	0	0	r1	r0	q1	q0		↕			7	r← r∧q
	OR	r, i	1	1	0	0	1	1	r1	r0	i3	i2	i1	i0		↕			7	r← r∨i3~i0
		r, q	1	0	1	0	1	1	0	1	r1	r0	q1	q0		↕			7	r← r∨q
	XOR	r, i	1	1	0	1	0	0	r1	r0	i3	i2	i1	i0		↕			7	r← r∀i3~i0
		r, q	1	0	1	0	1	1	1	0	r1	r0	q1	q0		↕			7	r← r∀q
	CP	r, i	1	1	0	1	1	1	r1	r0	i3	i2	i1	i0		↕	↕		7	r-i3~i0
		r, q	1	1	1	1	0	0	0	0	r1	r0	q1	q0		↕	↕		7	r-q
	FAN	r, i	1	1	0	1	1	0	r1	r0	i3	i2	i1	i0		↕			7	r∧i3~i0
		r, q	1	1	1	1	0	0	0	1	r1	r0	q1	q0		↕			7	r∧q
	RLC	r	1	0	1	0	1	1	1	1	r1	r0	r1	r0		↕	↕		7	d3← d2, d2← d1, d1← d0, d0 ←C, C← d3
	RRC	r	1	1	1	0	1	0	0	0	1	1	r1	r0		↕	↕		5	d3← C, d2← d3, d1← d2, d0← d1, C← d0
	INC	Mn	1	1	1	1	0	1	1	0	n3	n2	n1	n0		↕	↕		7	M(n3~n0) ←M(n3~n0)+1
	DEC	Mn	1	1	1	1	0	1	1	1	n3	n2	n1	n0		↕	↕		7	M(n3~n0) ←M(n3~n0)-1
	ACPX	MX, r	1	1	1	1	0	0	1	0	1	0	r1	r0	★	↕	↕		7	M(X) ←M(X)+r+C, X ←X+1
	ACPY	MY, r	1	1	1	1	0	0	1	0	1	1	r1	r0	★	↕	↕		7	M(Y) ←M(Y)+r+C, Y ←Y+1
	SCPX	MX, r	1	1	1	1	0	0	1	1	1	0	r1	r0	★	↕	↕		7	M(X) ←M(X)-r-C, X← X+1
	SCPY	MY, r	1	1	1	1	0	0	1	1	1	1	r1	r0	★	↕	↕		7	M(Y) ←M(Y)-r-C, Y← Y+1
	NOT	r	1	1	0	1	0	0	r1	r0	1	1	1	1		↕			7	r← $\overline{r}$

Abbreviations used in the explanations have the following meanings.

Symbols associated with registers and memory

A ..... A register
B ..... B register
X ..... XHL register (low order eight bits of index register IX)
Y ..... YHL register (low order eight bits of index register IY)
XH ..... XH register (high order four bits of XHL register)
XL ..... XL register (low order four bits of XHL register)
YH ..... YH register (high order four bits of YHL register)
YL ..... YL register (low order four bits of YHL register)
XP ..... XP register (high order four bits of index register IX)
YP ..... YP register (high order four bits of index register IY)
SP ..... Stack pointer SP
SPH ..... High-order four bits of stack pointer SP
SPL ..... Low-order four bits of stack pointer SP
MX, M(X) .. Data memory whose address is specified with index register IX
MY, M(Y) ... Data memory whose address is specified with index register IY
Mn, M(n) .. Data memory address 000H–00FH (address specified with immediate data n of 00H–0FH)
M(SP) ..... Data memory whose address is specified with stack pointer SP
r, q ..... Two-bit register code
r, q is two-bit immediate data; according to the contents of these bits, they indicate registers A, B, and MX and MY (data memory whose addresses are specified with index registers IX and IY)

r		q		Registers specified
r1	r0	q1	q0	
0	0	0	0	A
0	1	0	1	B
1	0	1	0	MX
1	1	1	1	MY

Symbols associated with program counter

NBP	New bank pointer
NPP	New page pointer
PCB	Program counter bank
PCP	Program counter page
PCS	Program counter step
PCSH	Four high order bits of PCS
PCSL	Four low order bits of PCS

Symbols associated with flags

F	Flag register (I, D, Z, C)
C	Carry flag
Z	Zero flag
D	Decimal flag
I	Interrupt flag
↓	Flag reset
↑	Flag set
↕	Flag set or reset

Associated with immediate data

p	Five-bit immediate data or label 00H–1FH
s	Eight-bit immediate data or label 00H–0FFH
l	Eight-bit immediate data 00H–0FFH
i	Four-bit immediate data 00H–0FH

Associated with arithmetic and other operations

+	Add
-	Subtract
∧	Logical AND
∨	Logical OR
∀	Exclusive-OR
★	Add-subtract instruction for decimal operation when the D flag is set

APPENDIX C PSEUDO-INSTRUCTION TABLE OF THE CROSS ASSEMBLER

Item No.	Pseudo-instruction	Meaning	Example of Use
1	EQU (Equation)	To allocate data to label	ABC EQU 9 BCD EQU ABC+1
2	ORG (Origin)	To define location counter	ORG 100H ORG 256
3	SET (Set)	To allocate data to label (data can be changed)	ABC SET 0001H ABC SET 0002H
4	DW (Define Word)	To define ROM data	ABC DW 'AB' BCD DW 0FFBH
5	PAGE (Page)	To define boundary of page	PAGE 1H PAGE 15
6	SECTION (Section)	To define boundary of section	SECTION
7	END (End)	To terminate assembly	END
8	MACRO (Macro)	To define macro	CHECK 1
9	LOCAL (Local)	To make local specification of label during macro definition	CHECK MACRO DATA LOCAL LOOP LOOP CP MX,DATA JP NZ,LOOP
10	ENDM (End Macro)	To end macro definition	ENDM

APPENDIX D COMMAND TABLE OF ICE6200

Item No.	Function	Command Format	Outline of Operation
1	Assemble	#A,a ↵	Assemble command mnemonic code and store at address "a"
2	Disassemble	#L,a1,a2 ↵	Contents of addresses a1 to a2 are disassembled and displayed
3	Dump	#DP,a1,a2 ↵	Contents of program area a1 to a2 are displayed
		#DD,a1,a2 ↵	Content of data area a1 to a2 are displayed
4	Fill	#FP,a1,a2,d ↵	Data d is set in addresses a1 to a2 (program area)
		#FD,a1,a2,d ↵	Data d is set in addresses a1 to a2 (data area)
5	Set Run Mode	#G,a ↵	Program is executed from the "a" address
		#TIM ↵	Execution time and step counter selection
		#OTF ↵	On-the-fly display selection
6	Trace	#T,a,n ↵	Executes program while displaying results of step instruction from "a" address
		#U,a,n ↵	Displays only the final step of #T,a,n
7	Break	#BA,a ↵	Sets Break at program address "a"
		#BAR,a ↵	Breakpoint is canceled
		#BD ↵	Break condition is set for data RAM
		#BDR ↵	Breakpoint is canceled
		#BR ↵	Break condition is set for EVA62XXCPU internal registers
		#BRR ↵	Breakpoint is canceled
		#BM ↵	Combined break conditions set for program data RAM address and registers
		#BMR ↵	Cancel combined break conditions for program data ROM address and registers
		#BRES ↵	All break conditions canceled
		#BC ↵	Break condition displayed
		#BE ↵	Enter break enable mode
		#BSYN ↵	Enter break disable mode
		#BT ↵	Set break stop/trace modes
		#BRKSEL,REM ↵	Set BA condition clear/remain modes
8	Move	#MP,a1,a2,a3 ↵	Contents of program area addresses a1 to a2 are moved to addresses a3 and after
		#MD,a1,a2,a3 ↵	Contents of data area addresses a1 to a2 are moved to addresses a3 and after
9	Data Set	#SP,a ↵	Data from program area address "a" are written to memory
		#SD,a ↵	Data from data area address "a" are written to memory
10	Change CPU Internal Registers	#DR ↵	Display EVA62XXCPU internal registers
		#SR ↵	Set EVA62XXCPU internal registers
		#I ↵	Reset EVA62XXCPU
		#DXY ↵	Display X, Y, MX and MY
		#SXY ↵	Set data for X and Y display and MX, MY

Item No.	Function	Command Format	Outline of Operation
11	History	#H,p1,p2 ↵	Display history data for pointer 1 and pointer 2
		#HB ↵	Display upstream history data
		#HG ↵	Display 21 line history data
		#HP ↵	Display history pointer
		#HPS,a ↵	Set history pointer
		#HC,S/C/E ↵	Sets up the history information acquisition before (S), before/after (C) and after (E)
		#HA,a1,a2 ↵	Sets up the history information acquisition from program area a1 to a2
		#HAR,a1,a2 ↵	Sets up the prohibition of the history information acquisition from program area a1 to a2
		#HAD ↵	Indicates history acquisition program area
		#HS,a ↵	Retrieves and indicates the history information which executed a program address "a"
		#HSW,a ↵ #HSR,a ↵	Retrieves and indicates the history information which wrote or read the data area address "a"
12	File	#RF,file ↵	Move program file to memory
		#RFD,file ↵	Move data file to memory
		#VF,file ↵	Compare program file and contents of memory
		#VFD,file ↵	Compare data file and contents of memory
		#WF,file ↵	Save contents of memory to program file
		#WFD,file ↵	Save contents of memory to data file
		#CL,file ↵	Load ICE6200 set condition from file
		#CS,file ↵	Save ICE6200 set condition to file
13	Coverage	#CVD ↵ #CVR ↵	Indicates coverage information Clears coverage information
14	ROM Access	#RP ↵ #VP ↵	Move contents of ROM to program memory Compare contents of ROM with contents of program memory
		#ROM ↵	Set ROM type
15	Terminate ICE	#Q ↵	Terminate ICE and return to operating system control
16	Command Display	#HELP ↵	Display ICE6200 instruction
17	Self Diagnosis	#CHK ↵	Report results of ICE6200 self diagnostic test

↵ means press the RETURN key.

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