MF740-03

EPSON

CMOS 4-BIT SINGLE CHIP MICROCOMPUTER

E0C6247 TECHNICAL MANUAL

E0C6247 Technical Hardware

E0C6247 Technical Software

ENERGY SAVING EPSON

SEIKO EPSON CORPORATION

PREFACE

This manual is individualy described about the hardware and the software of the E0C6247.

I. E0C6247 Technical Hardware

This part explains the function of the E0C6247, the circuit configurations, and details the controlling method.

II. E0C6247 Technical Software

This part explains the programming method of the E0C6247.

I. E0C6247 Technical Hardware

CONTENTS

CHAPTER 1 OVERVIEW

The E0C6247 is a single-chip microcomputer made up of the 4-bit core CPU E0C6200A, ROM (8,192 words, 12 bits to a word), RAM (1,792 words, 4 bits to a word), dot matrix LCD driver, serial interface, watchdog timer, programmable timer, time base counter and SVD circuit. Moreover, in the E0C6247 external memory device control is possible, and are most suitable for applications with equipment requiring large memory and dot matrix display functions such as a highly functional electronic pocketbook.

1.1 Features

OSC1 oscillation circuit	32.768 kHz/38.4 kHz/50 kHz/76.8 kHz (Typ.) crystal oscillation circuit
OSC3 oscillation circuit	200 kHz/1 MHz (Typ.) CR or ceramic oscillation circuit (*1)
Instruction set	108 types
Instruction execution time (differ depending on instruction)	During operation at 32 kHz: 153 µsec, 214 µsec, 366 µsec During operation at 38.4 kHz: 130 µsec, 182 µsec, 313 µsec During operation at 50 kHz: 100 µsec, 140 µsec, 240 µsec During operation at 76.8 kHz: 65 µsec, 91 µsec, 156 µsec During operation at 200 kHz: 25 µsec, 35 µsec, 60 µsec During operation at 1 MHz: 5 µsec, 7 µsec, 12 µsec
ROM capacity	8,192 words × 12 bits
RAM capacity	Data memory: 1,792 words × 4 bits Display memory: 256 words × 4 bits
External memory capacity	Read/write (RAM): max. 512K-bit × 4 Read only (ROM): max. 1M-bit × 4
Input port	8 bits (Pull up resistors may be supplemented *1)
Output port	20 bits (Switching to external memory bus and buzzer output are possible *2)
I/O port	20 bits (Switching to external memory bus, special outputs and serial inputs/outputs are possible *2)
Serial interface	1 port (Clock synchronous system, Asynchronous system 8-bit/7-bit *2)
LCD driver	64 segments × 8 or 16 commons (*2)
Time base counter	Clock timer: 1 system
Programmable timer	Built-in, 1 input × 8 bits with event counter function
Watchdog timer	Built-in
SVD (supply voltage detection)	16 values programmable (1.05–2.60 V)
External interrupt	Input port interrupt: 2 systems
Internal interrupt	Clock timer interrupt: 1 system Programmable timer interrupt: 1 system Serial interface interrupt: 3 systems
Supply voltage	0.9–3.6 V (during operation at 1 MHz: 2.2–3.6 V)
Current consumption	Single clock: During HALT: 1.5 V (normal, LCD power OFF) 2 µA 1.5 V (normal, LCD power ON) 6.5 µA 3.0 V (halver ON, LCD power ON) 5 µA During operation at 32 kHz: 1.5 V (normal, LCD power ON) 10 µA 3.0 V (halver ON, LCD power ON) 7 µA Twin clock: During operation at 200 kHz: 3.0 V (normal, LCD power ON) 40 µA During operation at 1 MHz: 3.0 V (normal, LCD power ON) 300 µA
Package	QFP8-160pin (plastic) or chip

*1 May be selected with mask option.
*2 May be selected with software.

1.2 Block Diagram

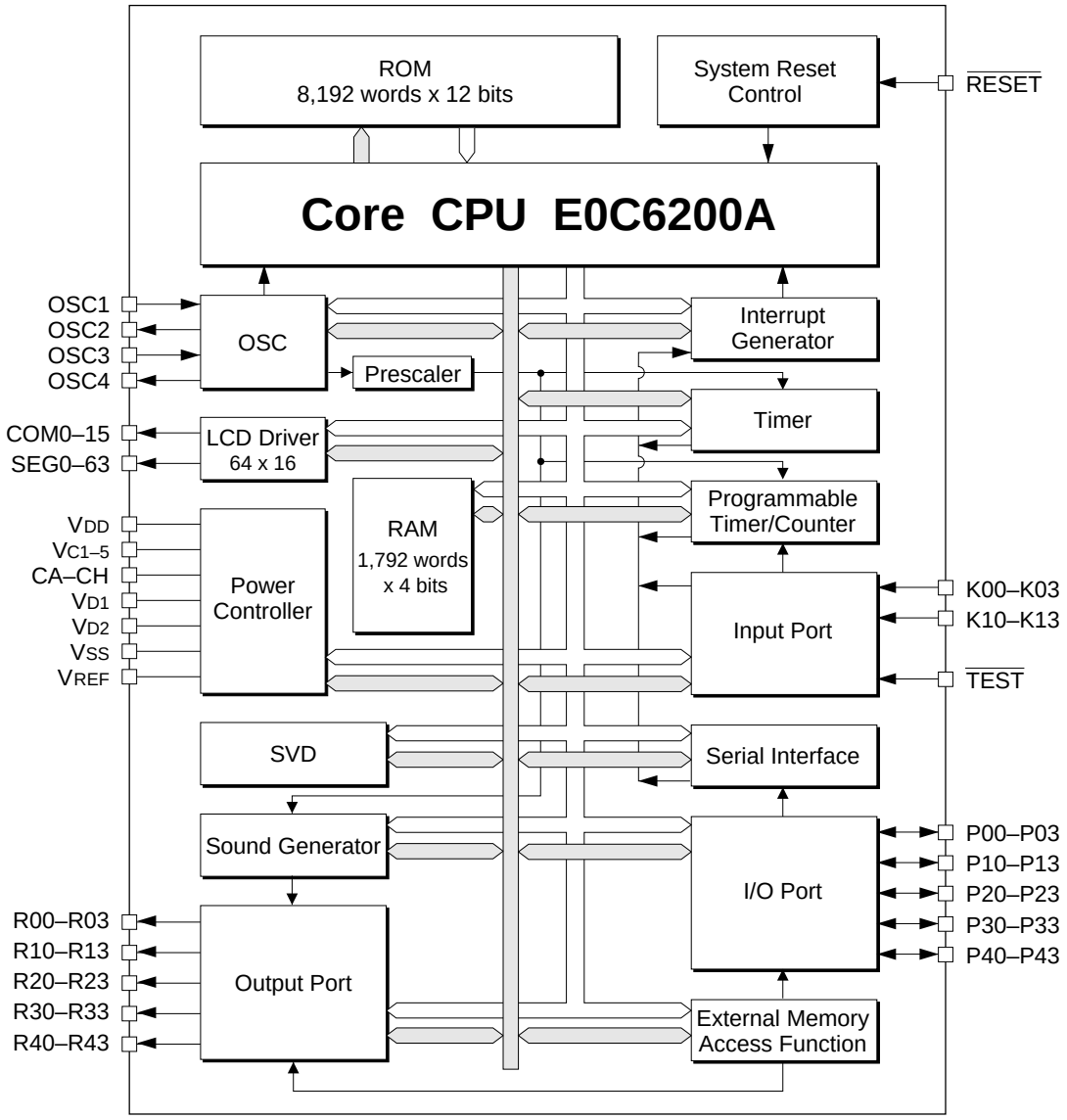
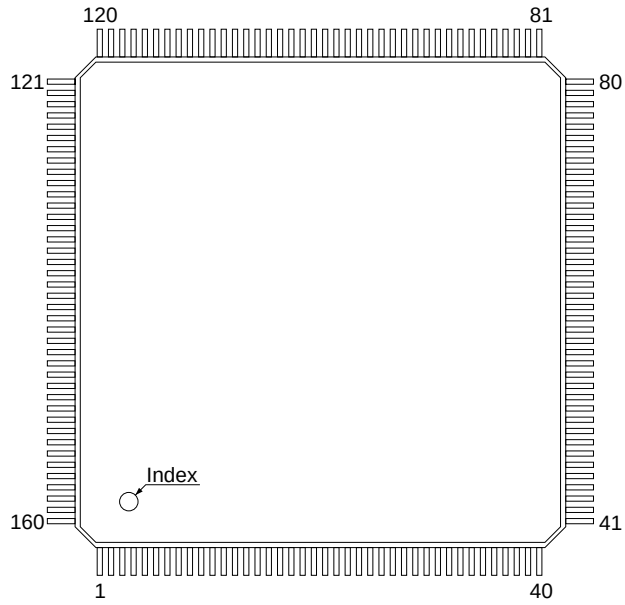


Fig. 1.2.1 Block diagram

1.3 Pin Layout Diagram

QFP8-160pin



Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name
1	SEG52	33	SEG20	65	K03	97	R01	129	V_{C1}
2	SEG51	34	SEG19	66	K10	98	R02	130	V_{C2}
3	SEG50	35	SEG18	67	K11	99	R03	131	V_{C3}
4	SEG49	36	SEG17	68	K12	100	R10	132	V_{C4}
5	SEG48	37	SEG16	69	K13	101	R11	133	V_{C5}
6	SEG47	38	SEG15	70	P00	102	R12	134	CH
7	SEG46	39	SEG14	71	P01	103	R13	135	CG
8	SEG45	40	SEG13	72	P02	104	R20	136	CF
9	SEG44	41	SEG12	73	P03	105	R21	137	CE
10	SEG43	42	SEG11	74	P10	106	R22	138	CD
11	SEG42	43	SEG10	75	P11	107	R23	139	CC
12	SEG41	44	SEG9	76	P12	108	R30	140	CB
13	SEG40	45	SEG8	77	P13	109	R31	141	CA
14	SEG39	46	SEG7	78	N.C.	110	R32	142	COM0
15	SEG38	47	SEG6	79	N.C.	111	R33	143	COM1
16	SEG37	48	SEG5	80	N.C.	112	R40	144	COM2
17	SEG36	49	SEG4	81	N.C.	113	R41	145	COM3
18	SEG35	50	SEG3	82	N.C.	114	R42	146	COM4
19	SEG34	51	SEG2	83	N.C.	115	R43	147	COM5
20	SEG33	52	SEG1	84	P20	116	N.C.	148	COM6
21	SEG32	53	SEG0	85	P21	117	N.C.	149	COM7
22	SEG31	54	COM15	86	P22	118	$\overline{TEST}$	150	SEG63
23	SEG30	55	COM14	87	P23	119	$\overline{RESET}$	151	SEG62
24	SEG29	56	COM13	88	P30	120	V_{REF}	152	SEG61
25	SEG28	57	COM12	89	P31	121	V_{DD}	153	SEG60
26	SEG27	58	COM11	90	P32	122	OSC4	154	SEG59
27	SEG26	59	COM10	91	P33	123	OSC3	155	SEG58
28	SEG25	60	COM9	92	P40	124	V_{D1}	156	SEG57
29	SEG24	61	COM8	93	P41	125	OSC2	157	SEG56
30	SEG23	62	K00	94	P42	126	OSC1	158	SEG55
31	SEG22	63	K01	95	P43	127	V_{SS}	159	SEG54
32	SEG21	64	K02	96	R00	128	V_{D2}	160	SEG53

Fig. 1.3.1 Pin layout diagram

1.4 Pin Description

Table 1.4.1 Pin description

Pin name	Pin No.	In/Out	Function
V_{DD}	121	–	Power (+) supply pin
V_{SS}	127	–	Power (-) supply pin
V_{D1}	124	–	Oscillation/internal logic system regulated voltage output pin
V_{D2}	128	–	Power voltage doubling/halving output pin
V_{C1}– V_{C5}	129–133	–	LCD system power supply pin 1/4 bias generated internally, 1/5 bias impressed externally (selected by mask option)
V_{REF}	120	O	LCD system power test pin
CA–CF	141–136	–	LCD system boosting/reducing condenser connecting pins
CG, CH	135, 134	–	Power voltage boosting/reducing condenser connecting pins
OSC1	126	I	Crystal osciration input pin
OSC2	125	O	Crystal oscillation output pin
OSC3	123	I	Ceramic or CR oscillation input pin (selected by mask option)
OSC4	122	O	Ceramic or CR oscillation output pin (selected by mask option)
K00–K03	62–65	I	Input pins
K10–K13	66–69	I	Input pins
P00–P03	70–73	I/O	I/O pins (Switching to external data bus D00–D03 is possible by software)
P10–P13	74–77	I/O	I/O pins (Switching to external data bus D04–D07 is possible by software)
P20–P23	84–87	I/O	I/O pins (Switching to chip select $\overline{CS0}$–$\overline{CS3}$ outputs is possible by software)
P30	88	I/O	I/O pins (Switching to CL output is possible by software)
P31	89	I/O	I/O pins (Switching to FR output is possible by software)
P32	90	I/O	I/O pins (Switching to PTOVF output is possible by software)
P33	91	I/O	I/O pins (Switching to FOUT output is possible by software)
P40–P43	92–95	I/O	I/O pins (Switching to serial I/F input/output is possible by software)
R00–R03	96–99	O	Output pins (Switching to external address bus A00–A03 is posible by software)
R10–R13	100–103	O	Output pins (Switching to external address bus A04–A07 is posible by software)
R20–R23	104–107	O	Output pins (Switching to external address bus A08–A12 is posible by software)
R30–R33	108–111	O	Output pins (Switching to external address bus A13–A15 is posible by software)
R40	112	O	Output pin (Switching to A16 or $\overline{WR}$ output is posible by software)
R41	113	O	Output pin (Switching to $\overline{RD}$ output is possible by software)
R42	114	O	Output pin (Switching to $\overline{BZ}$ output is possible by software)
R43	115	O	Output pin (Switching to BZ output is possible by software)
COM0–COM15	142–149, 61–54	O	LCD common output pins (1/8 or 1/16 duty can be selected by software)
SEG0–SEG63	53–1, 160–150	O	LCD segment output pins
$\overline{RESET}$	119	I	Initial reset input pin
$\overline{TEST}$	118	I	Testing input pin (connect to V_{DD} pin in normal operation)

CHAPTER 2 POWER SUPPLY AND INITIAL RESET

2.1 Power Supply

The E0C6247 operating power voltage is as follows:

0.9 V to 3.6 V

Note: • *When the range of 0.9 V to 1.25 V is used as the operating power voltage, software control is necessary (see Section 4.2).*

• *Power voltage must be within 2.2 V to 3.6 V when the OSC3 oscillation circuit with a 1 MHz clock is used.*

The E0C6247 operates when a single power supply within the above range is applied between V_{DD} and V_{SS}. Even if the voltage is not within the above range necessary for the internal circuits, the IC itself can generate the following built-in power circuits.

Table 2.1.1 Power supply circuits

Circuit	Power supply circuit	Output voltage
Oscillation circuit and internal circuits	Oscillation system regulated voltage circuit	V_{D1}
LCD driver	LCD system voltage circuit	V_{C1}–V_{C5}
Oscillation system regulated voltage circuit and LCD system voltage circuit	Voltage doubler/halver	V_{D2}

Note: • *External loads cannot be driven by the output voltages from the internal power supply circuits.*

• *V_{C3} is used only when the driving voltage of the LCD system will be supplied externally (1/5 bias); when using the internal LCD system voltage circuit (1/4 bias), it is shorted with V_{C2}.*

• *See Chapter 7, "ELECTRICAL CHARACTERISTICS", for voltage values and drive capacity.*

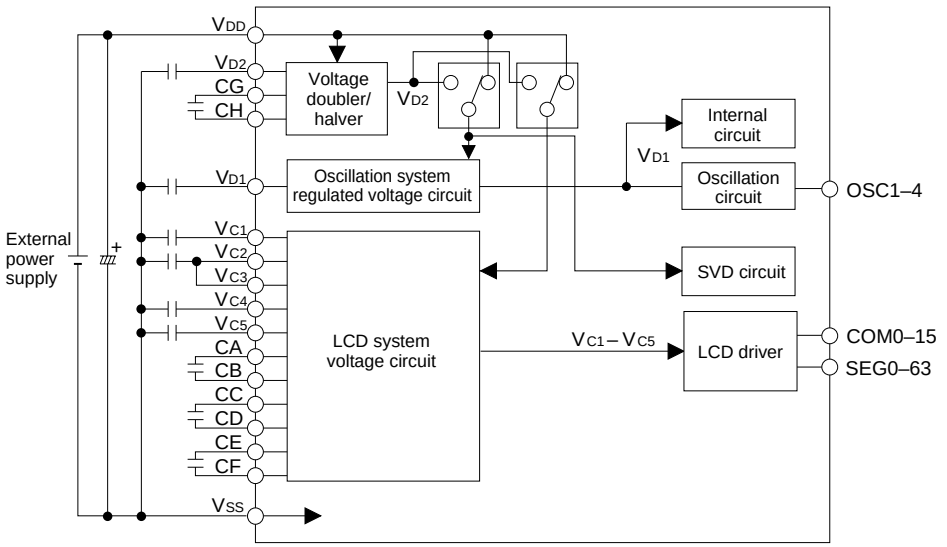


Fig. 2.1.1 Configuration of power supply

2.1.1 Voltage <V_{D1}> for oscillation circuit and internal circuits

V_{D1} is a voltage for the oscillation circuit and the internal logic circuits, and is generated by the oscillation system regulated voltage circuit for stabilizing the oscillation.
The E0C6247 is designed with twin clock specification; it has two types of oscillation circuits OSC1 and OSC3 built-in. Use OSC1 clock for normal operation, and switch it to OSC3 by the software when high-speed operation is necessary. When switching the clock, the operating voltage V_{D1} must be switched by the software to stabilize the operation of the oscillation circuit and internal circuits of the clock to be switched.
The oscillation system regulated voltage circuit can output the following three types of V_{D1} voltage, it should be set at the value according to the oscillation circuit and oscillation frequency by the software.

1. Single clock operation (OSC1): V_{D1} = 1.2 V
2. Twin clock operation (OSC3, 200 kHz): V_{D1} = approx. 1.4 V
3. Twin clock operation (OSC3, 1 MHz): V_{D1} = 2.1 V

See Section 4.4, "Oscillation Circuit", for the V_{D1} switching procedure.
To generate the voltage above, a larger voltage is needed for the oscillation system regulated voltage circuit. Thus the oscillation system regulated voltage circuit can be driven by the voltage V_{D2} that is boosted to double the supply voltage (details are explained later). Either the V_{DD} or V_{D2} can be set by the software to drive the oscillation system regulated voltage circuit.
However, when a 1 MHz clock (item 3 of above) is used, 2.2 V or more supply voltage is necessary and it cannot be operated with the boosted voltage.

2.1.2 Voltage <V_{C1}–V_{C5}> for LCD driving

V_{C1}–V_{C5} are driving voltages for the LCD, and for which either the voltages generated by the LCD system regulated voltage circuit or voltages to be supplied from outside can be used. The built-in LCD system regulated voltage circuit generates four electric potentials (1/4 bias) for V_{C1}, V_{C2}, V_{C4} and V_{C5} except for V_{C3}. These four output voltages can be supplied to the outside only for the externally expanded LCD driver.
When external voltages are supplied, 1/5 bias driving can be made by inputting five electric potentials to the V_{C1}–V_{C5} terminals (including V_{C3}).
Either the internal generated voltages or external voltages used for the LCD drive voltage can be selected by the mask option.
The LCD system voltage circuit generates V_{C1} or V_{C2} with the regulated voltage circuit incorporated in itself, and generates three other electric potentials by boosting or reducing the voltage of V_{C1} or V_{C2}. Table 2.1.2.1 shows the V_{C1}, V_{C2}, V_{C4} and V_{C5} voltage values and boost/reduce status.

Table 2.1.2.1 LCD drive voltage when generated internally

LCD drive voltage	V_{DD} = 0.9–3.6 V	V_{DD} = 2.6–3.6 V
V_{C1} (0.975–1.2 V)	V_{C1} (standard)	1/2 × V_{C2}
V_{C2} (1.950–2.4 V)	2 × V_{C1}	V_{C2} (standard)
V_{C4} (2.925–3.6 V)	3 × V_{C1}	3/2 × V_{C2}
V_{C5} (3.900–4.8 V)	4 × V_{C1}	2 × V_{C2}

Note: The LCD drive voltage can be adjusted by the software (see Section 4.8.6). Values in the above table are typical values.

Either the V_{C1} or V_{C2} used for the standard is selected according to the supply voltage by the software. The V_{C2} standard improves the display quality and reduces current consumption, however, the supply voltage V_{DD} must be 2.6 V or more. 1.25 V or more voltage is needed even in the V_{C1} standard, the LCD system voltage circuit can also be driven with the V_{D2} voltage boosted from the supply voltage, if the supply voltage is less than 1.25 V, same as the oscillation system regulated voltage circuit. This selection can be done separately from the oscillation system regulated voltage circuit.
See Section 4.2, "Setting of Power Supply and Operating Mode", for control of the LCD drive voltage.

2.1.3 Voltage doubler/halver and operating mode

The power supply circuit has the voltage doubler/halver built-in to generate the above mentioned voltages for the oscillation circuit/internal circuits and LCD driving even if the supply voltage is less than those setting voltages, or to reduce current consumption when the supply voltage has some redundancy. The voltage doubler/halver doubles or halves the voltage supplied from outside, and generates the V_{D2} voltage for the internal power supply circuits (oscillation system regulated voltage circuit and LCD system voltage circuit).
There are the following three operation modes depending on the status of the voltage doubler/halver, and switching between them is done by the software. Further the mode setting can be done for the oscillation system regulated circuit and the LCD system voltage circuit, independently.

(1) Boost mode

The E0C6247 operates with 0.9–3.6 V supply voltage. However, a minimum 1.25 V supply voltage during single clock operation (OSC1) or a minimum 2.2 V during twin clock operation (OSC3, 200 kHz) is needed for the oscillation system regulated voltage circuit. Therefore, when operating with the following supply voltage (V_{DD}), perform a doubling using the voltage doubler/halver and drive the oscillation system regulated voltage circuit with the V_{D2}.

- During single clock operation (OSC1): V_{DD} = 0.9–1.25 V (V_{D2} = 1.8–2.5 V, with doubling)
- During twin clock operation (OSC3, 200 kHz): V_{DD} = 0.9–2.2 V (V_{D2} = 1.8–4.4 V, with doubling)

Operating mode at this time is the boost mode.
When the LCD system power circuit is used (the LCD drive voltage is generated internally), a minimum 1.25 V supply voltage is necessary same as above. Therefore, when operating with 0.9–1.25 V supply voltage V_{DD}, perform a doubling using the voltage doubler/halver and drive the oscillation system regulated voltage circuit with V_{D2}. Since this control can independently be done from the oscillation system regulated voltage circuit, when the supply voltage V_{DD} is more than 1.25 V, it is not necessary to operate the LCD system power circuit with the boost mode even if the oscillation system regulated voltage circuit is operated with the boost mode for OSC3 (200 kHz).

When the supply voltage is more than needed for operation, do not set in this mode because boosting voltage increases current consumption.

Note: 1. Set the boost mode when supply voltage drop is detected by the SVD circuit, such as during heavy load operation (buzzer sounds or a lamp lights) or by the battery life. (*)

2. 1 MHz OSC3 oscillation circuit cannot be used in this mode even when 2.2 V or more voltage is generated by boosting. Turning the OSC3 oscillation circuit (1 MHz) ON in this mode may cause malfunction.

(2) Normal mode

In this mode, the internal power circuit directly operates by the supply voltage V_{DD} within the range of 1.25–3.6 V (2.2–3.6 V when the OSC3 clock is used) without the voltage doubler/halver. The OSC3 oscillation circuit can be used when supplying a 2.2 V or more supply voltage. At initial reset, this mode is set.

(3) Reduce mode

The reduce mode can be set when a 2.6–3.6 V supply voltage is used to operate. This mode halves the supply voltage using the halver, and operates the internal power circuit using its output voltage. Therefore, current consumption can be reduced to about half of the normal mode.

Note: The OSC3 oscillation circuit cannot be used in the reduce mode. Turning the OSC3 oscillation circuit ON in this mode may cause malfunction.

Table 2.1.3.1 Correspondence between supply voltage and operating mode

Power circuit	Operating condition	Supply voltage V_{DD} (V)			
		0.9–1.25	1.25–2.2	2.2–2.6	2.6–3.6
Oscillation system regulated voltage circuit	OSC1	Boost mode	Normal mode*		Reduce or normal mode
	OSC3, 200kHz	Boost mode		Normal mode*	
	OSC3, 1MHz	Cannot be used		Normal mode	
LCD system voltage circuit	V_{C1} standard	Boost mode	Normal mode		Reduce or normal mode
	V_{C2} standard	Cannot be used			Normal mode

* See above Note 1.

See Section 4.2, "Setting of Power Supply and Operating Mode", for setting method of the operating mode.

2.2 Initial Reset

To initialize the E0C6247 circuits, initial reset must be executed. There are four ways of doing this.

(1) External initial reset by the $\overline{\text{RESET}}$ terminal
(2) External initial reset by simultaneous low input to terminals K00–K03 (mask option setting)
(3) Initial reset by the oscillation detection circuit
(4) Initial reset by watchdog timer (mask option setting)

Be sure to use reset functions (1) or (2) at power-on and be sure to initialize securely. In normal operation, the circuit may be initialized by any of the above four types.

Figure 2.2.1 shows the configuration of the initial reset circuit.

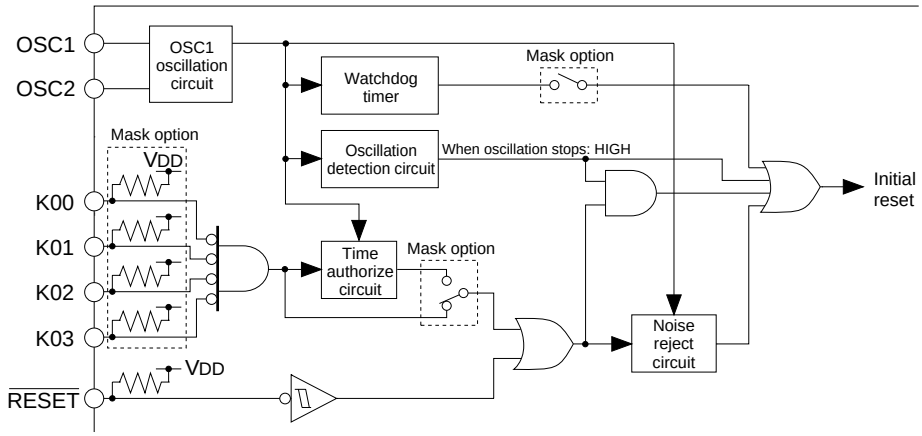


Fig. 2.2.1 Configuration of initial reset circuit

2.2.1 Reset terminal ($\overline{\text{RESET}}$)

The initial resetting can be done by externally setting the reset terminal to a low level. However, be sure to observe the following precautions, because the $\overline{\text{RESET}}$ signal passes through the noise reject circuit.
When the reset terminal is used for initial resetting during operation, a pulse (low level) of 0.3 msec (0.2 msec when the oscillation frequency f_{OSC1} = 76.8 kHz) or less is considered to be noise by the noise reject circuit. Maintain a low level of 1.5 msec (3 msec when f_{OSC1} = 76.8 kHz) to securely perform the initial reset. When the reset terminal goes high, the CPU begins to operate.
Since the noise reject circuit does not operate when oscillation is stopped, the noise reject circuit is bypassed until it starts oscillation. For this reason, be sure to maintain a low level the reset input in the oscillation stopped status at power-on, until starting oscillation.

2.2.2 Simultaneous low input to terminals K00–K03

Another way of executing initial reset externally is to input a low signal simultaneously to the input ports (K00–K03) selected with the mask option.
Since this initial reset also passes through the same noise reject circuit as the reset terminal, you should maintain the specified input port terminal at low level for 1.5 msec (3 msec when f_{OSC1} = 76.8 kHz) or more during operation and until it begins oscillation at times such as when making power.
Table 2.2.2.1 shows the combinations of input ports (K00–K03) that can be selected with the mask option.

Table 2.2.2.1 Combinations of input ports

1	Not use
2	K00*K01*K02*K03
3	K00*K01*K02
4	K00*K01

When, for instance, mask option 2 (K00*K01*K02*K03) is selected, initial reset is executed when the signals input to the four ports K00–K03 are all low at the same time. The initial reset is done, even when a key entry including a combination of selected input ports is made.
Further, the time authorize circuit can be selected with the mask option. The time authorize circuit performs initial reset, when the input time of the simultaneous low input is authorized and found to be the same or more than the defined time (1 to 2 sec).
If you use this function, make sure that the specified ports do not go low at the same time during ordinary operation.

2.2.3 Oscillation detection circuit

The oscillation detection circuit outputs the initial reset signal at power-on until the OSC1 oscillation circuit begins oscillating, or when the OSC1 oscillation circuit halts oscillating for some reason.
In addition, it uses a simultaneous low input of the input ports (K00–K03) or reset terminal for the initial reset at power-on and you should not execute it by this function alone.

2.2.4 Watchdog timer

If the CPU runs away for some reason, the watchdog timer will detect this situation and output an initial reset signal. See Section 4.3, "Resetting Watchdog Timer" for details.
As with the oscillation detection circuit, you should not do an initial reset at power-on using this function.

2.2.5 Internal register at initial resetting

Initial reset initializes the CPU as shown in the table below.

Table 2.2.5.1 Initial values

CPU core			
Name	Symbol	Number of bits	Setting value
Program counter step	PCS	8	00H
Program counter page	PCP	4	1H
Program counter bank	PCB	1	0
New page pointer	NPP	4	1H
New bank pointer	NBP	1	0
Stack pointer	SP	8	Undefined
Index register IX	IX	12	Undefined
Index register IY	IY	12	Undefined
Register pointer	RP	4	Undefined
General-purpose register A	A	4	Undefined
General-purpose register B	B	4	Undefined
Interrupt flag	I	1	0
Decimal flag	D	1	0
Zero flag	Z	1	Undefined
Carry flag	C	1	Undefined

Peripheral circuits		
Name	Number of bits	Setting value
RAM	4	Undefined
Display memory	4	Undefined
Other peripheral circuits	—	*

* See Section 4.1, "Memory Map".

2.2.6 Terminal settings at initial resetting

The output port (R) terminals and I/O port (P) terminals are combined with the bus terminals for external memory accessing or the special output terminals, and these functions are selected by the software. At initial reset, these terminals are set to the general purpose output port terminals and I/O port terminals. Settings according to the system should be set with the initial routine in the application. In addition, take care of the initial status of output terminals when designing a system.
Table 2.2.6.1 shows the list of the combined terminal settings.

Table 2.2.6.1 List of combined terminal settings

Terminal name	Terminal status at initial reset	When external memory is used				When special output is used						When serial I/F is used		
		1M-bit	512K-bit	256K-bit	64K-bit	$\overline{BZ}$	BZ	CL	FR	PTOVF	FOUT	Master	Slave	Async.
R00–R03	R00–R03(High output)	A00–A03	A00–A03	A00–A03	A00–A03									
R10–R13	R10–R13(High output)	A04–A07	A04–A07	A04–A07	A04–A07									
R20–R23	R20–R23(High output)	A08–A11	A08–A11	A08–A11	A08–A11									
R30	R30(High output)	A12	A12	A12	A12									
R31	R31(High output)	A13	A13	A13	R31									
R32	R32(High output)	A14	A14	A14	R32									
R33	R33(High output)	A15	A15	R33	R33									
R40	R40(High output)	A16	$\overline{WR}$	$\overline{WR}$	$\overline{WR}$									
R41	R41(High output)	$\overline{RD}$	$\overline{RD}$	$\overline{RD}$	$\overline{RD}$									
R42	R42(Low output)					$\overline{BZ}$								
R43	R43(Low output)						BZ							
P00–P03	P00–P03(Input & PullUp)	D00–D03	D00–D03	D00–D03	D00–D03									
P10–P13	P10–P13(Input & PullUp)	D04–D07	D04–D07	D04–D07	D04–D07									
P20–P23	P20–P23(Input & PullUp)	$\overline{CS0}$–$\overline{CS3}$	$\overline{CS0}$–$\overline{CS3}$	$\overline{CS0}$–$\overline{CS3}$	$\overline{CS0}$–$\overline{CS3}$									
P30	P30(Input & PullUp)							CL						
P31	P31(Input & PullUp)								FR					
P32	P32(Input & PullUp)									PTOVF				
P33	P33(Input & PullUp)										FOUT			
P40	P40(Input & PullUp)											SIN(I)	SIN(I)	SIN(I)
P41	P41(Input & PullUp)											SOUT(O)	SOUT(O)	SOUT(O)
P42	P42(Input & PullUp)											$\overline{SCLK}$(O)	$\overline{SCLK}$(I)	P42
P43	P43(Input & PullUp)											P43	$\overline{SRDY}$(O)	P43

Master: Clock synchronous master mode
Slave: Clock synchronous slave mode
Async.: Asynchronous mode

For setting procedure of the functions, see explanations for each of the peripheral circuits.

2.3 Test Terminal ($\overline{TEST}$)

This is the terminal that is used at the time of the factory inspection of the IC. During normal operation, connect the $\overline{TEST}$ to V_{DD}.

CHAPTER 3 CPU, ROM, RAM

3.1 CPU

The E0C6247 employs the 4-bit core CPU E0C6200A for the CPU, so that register configuration, instructions and so forth are virtually identical to those in other family processors using the E0C6200A.
Refer to "E0C6200/6200A Core CPU Manual" for details about the E0C6200A.
However, The SLEEP operation is not assumed in the E0C6247, so the SLP instruction cannot be used.

3.2 ROM

The built-in ROM, a mask ROM for loading the program, has a capacity of 8,192 steps × 12 bits. The program area is two banks, each of 16 (0–15) pages × 256 (00H–FFH) steps. After initial reset, the program beginning address is set to bank 0, page 1, step 00H. The interrupt vector is allocated to page 1 of each bank, steps 02H–0EH.

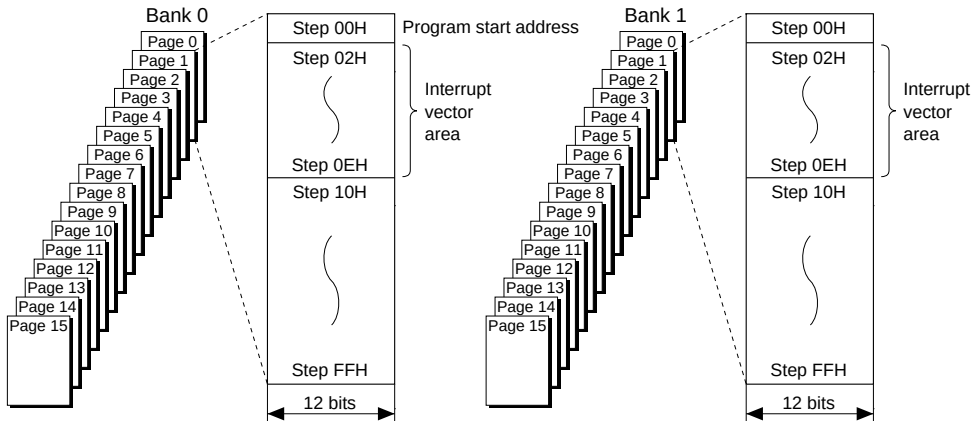


Fig. 3.2.1 ROM configuration

3.3 RAM

The RAM, a data memory storing a variety of data, has a capacity of 1,792 words × 4 bits. When programming, keep the following points in mind.

(1) Part of the data memory can be used as stack area when subroutine calls and saving registers, so be careful not to overlap the data area and stack area.

(2) Subroutine calls and interrupts take up three words of the stack area.

(3) The data memory 000H–00FH is for the register pointers (RP), and is the addressable memory register area.

3.4 External Memory

When external memory access function is selected by the software, maximum four 64K-byte (512K-bit) RAM or maximum four 128K-byte (1M-bit) ROM may be expanded externally.
See Section 4.13, "External Memory Access", for details of external memory.

CHAPTER 4 PERIPHERAL CIRCUITS AND OPERATION

Peripheral circuits (timer, I/O, and so on) of the E0C6247 are memory mapped, and interfaced with the CPU. Thus, all the peripheral circuits can be controlled by using the memory operation command to access the I/O memory in the memory map.
The following sections describe how the peripheral circuits operation.

4.1 Memory Map

Data memory of the E0C6247 is composed of 1,792-word RAM, 256-word display memory, 80-word I/O memory and 256-word external memory access area
Figures 4.1.1(a) and (b) present the overall memory maps of the E0C6247, and Tables 4.1.1(a)–(h) the peripheral circuits' (I/O space) memory maps.
In the E0C6247 the same I/O memory has been laid out for 80H–FCH from page 0 to 3. As a result, the I/O memory can be accessed without changing over the data memory page if it is in page 0 to 3. The same result is obtained for I/O memory changes and for readable/writable address references, no matter on what page within 0 to 3 it is done.

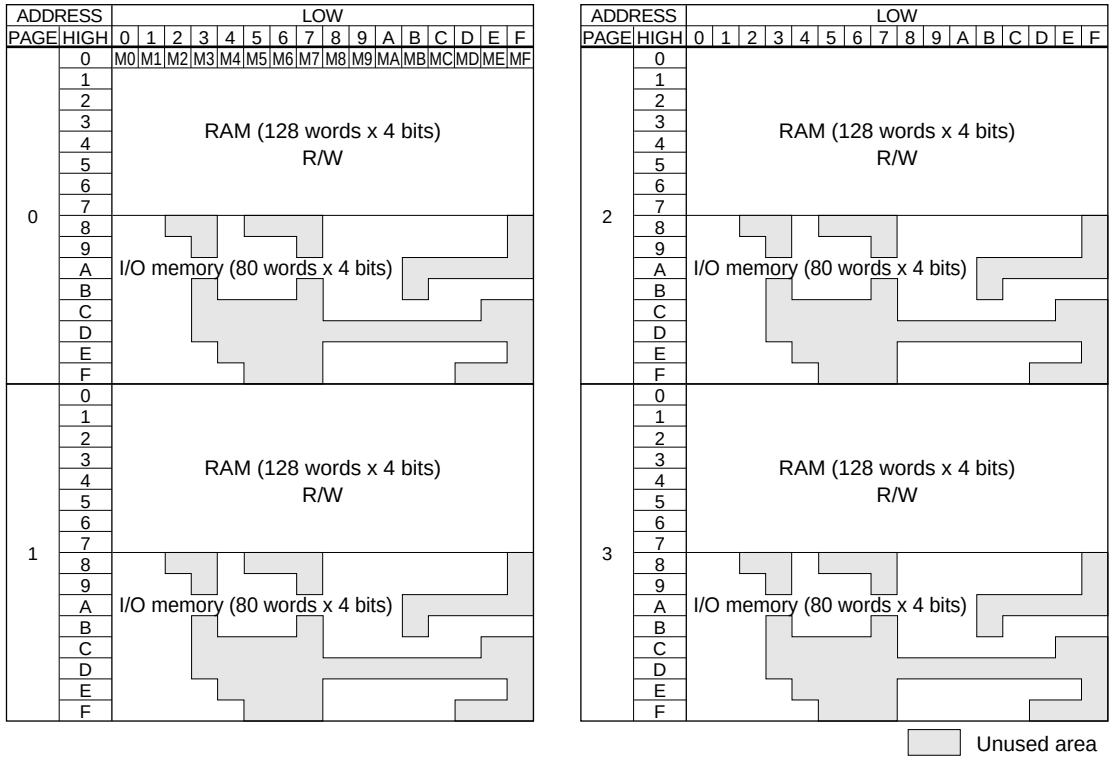


Fig. 4.1.1(a) Memory map

Note: Memory is not mounted in unused area within the memory map and in memory area not indicated in this chapter. For this reason, normal operation cannot be assured for programs that have been prepared with access to these areas.

ADDRESS		LOW													
PAGE	HIGH	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
4	0	RAM (256 words x 4 bits) R/W															
	1																
	2																
	3																
	4																
	5																
	6																
	7																
	8																
	9																
	A																
	B																
	C																
	D																
	E																
	F																
5	0	RAM (256 words x 4 bits) R/W															
	1																
	2																
	3																
	4																
	5																
	6																
	7																
	8																
	9																
	A																
	B																
	C																
	D																
	E																
	F																
6	0	RAM (256 words x 4 bits) R/W															
	1																
	2																
	3																
	4																
	5																
	6																
	7																
	8																
	9																
	A																
	B																
	C																
	D																
	E																
	F																
7	0	RAM (256 words x 4 bits) R/W															
	1																
	2																
	3																
	4																
	5																
	6																
	7																
	8																
	9																
	A																
	B																
	C																
	D																
	E																
	F																

ADDRESS		LOW													
PAGE	HIGH	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
8	0	RAM (256 words x 4 bits) R/W															
	1																
	2																
	3																
	4																
	5																
	6																
	7																
	8																
	9																
	A																
	B																
	C																
	D																
	E																
	F																
9	0	For external memory accessing (256 words x 4 bits) R/W															
	1																
	2																
	3																
	4																
	5																
	6																
	7																
	8																
	9																
	A																
	B																
	C																
	D																
	E																
	F																
A	0	Display memory (256 words x 4 bits) R/W															
	1																
	2																
	3																
	4																
	5																
	6																
	7																
	8																
	9																
	A																
	B																
	C																
	D																
	E																
	F																

Fig. 4.1.1(b) Memory map

Table 4.1.1(a) I/O memory map (80H–8EH)

Address *7	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
80H	SVDS3	SVDS2	SVDS1	SVDS0	SVDS3	0			SVD criteria voltage setting SVDS [3][2][1][0] Voltage (V) / SVDS [3][2][1][0] Voltage (V) 0 1 1 1 1.60 / 1 1 1 1 2.60 0 1 1 0 1.40 / 1 1 1 0 2.50 0 1 0 1 1.30 / 1 1 0 1 2.30 0 1 0 0 1.25 / 1 1 0 0 2.20 0 0 1 1 1.20 / 1 0 1 1 2.10 0 0 1 0 1.15 / 1 0 1 0 2.05 0 0 0 1 1.10 / 1 0 0 1 2.00 0 0 0 0 1.05 / 1 0 0 0 1.95
					SVDS2	0			
					SVDS1	0			
	R/W				SVDS0	0			
81H	0	0	SVDDT	SVDON	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R			R/W	SVDDT	0	Low	Normal	SVD evaluation data
					SVDON	0	On	Off	SVD circuit On/Off
84H	VCSEL	VDSEL	HLON	DBON	VCSEL	0	V_{D2}	V_{DD}	Power selection for LCD system voltage circuit
					VDSEL	0	V_{D2}	V_{DD}	Power selection for oscillation system regulated voltage circuit
	R/W				HLON	0	On	Off	Halver On/Off
					DBON	0	On	Off	Doubler On/Off
88H	0	0	PRSM1	PRSM0	0 *5	– *2			Unused PRSM[1][0] f_{OSC1} (kHz) 1 1 76.8 1 0 50.0 0 1 38.4 0 0 32.768
					0 *5	– *2			Unused
	R		R/W		PRSM1	0			OSC1 prescaler selection
					PRSM0	0			
89H	CLKCHG	OSCC	VDC1	VDC0	CLKCHG	0	OSC3	OSC1	CPU system clock switch
					OSCC	0	On	Off	OSC3 oscillation On/Off
	R/W				VDC1	0			CPU operating voltage switch VDC[1][0] V_{D1} Oscillation circuit 1 * 2.1 V OSC3 (1 MHz) 0 1 1.4 V OSC3 (200 kHz) 0 0 1.2 V OSC1
					VDC0	0			
8AH	FOUTE	0	FOFQ1	FOFQ0	FOUTE	0	Enable	Disable	FOUT output enable
					0 *5	– *2			Unused
					FOFQ1	0			FOUT frequency selection FOFQ[1][0] FOUT frequency 1 1 f_{OSC3} 1 0 f_{OSC1} 0 1 f_{OSC1}/8 (f_{OSC1}/16) 0 0 f_{OSC1}/64 (f_{OSC1}/128) (In case of f_{OSC1} = 76.8 kHz)
	R/W	R	R/W		FOFQ0	0			
8BH	0	0	0	WDRST	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R			W	0 *5	– *2			Unused
					WDRST *5	Reset	Reset	–	Watchdog timer reset
8CH	0	0	TMRUN	TMRST	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R		R/W	W	TMRUN	0	Run	Stop	Clock timer Run/Stop
					TMRST *5	Reset	Reset	–	Clock timer reset
8DH	TM3	TM2	TM1	TM0	TM3	0			Clock timer data (16 Hz) (f_{OSC1} = 50 kHz: (12.5 Hz) → (50 Hz))
					TM2	0			Clock timer data (32 Hz)
	R				TM1	0			Clock timer data (64 Hz)
					TM0	0			Clock timer data (128 Hz) (100 Hz)
8EH	TM7	TM6	TM5	TM4	TM7	0			Clock timer data (1 Hz)
					TM6	0			Clock timer data (2 Hz)
	R				TM5	0			Clock timer data (4 Hz)
					TM4	0			Clock timer data (8 Hz)

Remarks

*1 Initial value at the time of initial reset
*2 Not set in the circuit
*3 Undefined
*4 Reset (0) immediately after being read
*5 Constantly "0" when being read
*6 Refer to main manual
*7 I/O memory is allocated from page 0 to 3

Table 4.1.1(b) I/O memory map (90H–9EH)

Address *7	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
90H	SIK03	SIK02	SIK01	SIK00	SIK03	0	Enable	Disable	K00–K03 interrupt selection register
					SIK02	0	Enable	Disable	
	R/W				SIK01	0	Enable	Disable	
					SIK00	0	Enable	Disable	
91H	K03	K02	K01	K00	K03	– *2	High	Low	K00–K03 input port data
					K02	– *2	High	Low	
	R				K01	– *2	High	Low	
					K00	– *2	High	Low	
92H	KCP03	KCP02	KCP01	KCP00	KCP03	1	↓	↑	K00–K03 input comparison register
					KCP02	1	↓	↑	
	R/W				KCP01	1	↓	↑	
					KCP00	1	↓	↑	
94H	SIK13	SIK12	SIK11	SIK10	SIK13	0	Enable	Disable	K10–K13 interrupt selection register
					SIK12	0	Enable	Disable	
	R/W				SIK11	0	Enable	Disable	
					SIK10	0	Enable	Disable	
95H	K13	K12	K11	K10	K13	– *2	High	Low	K10–K13 input port data
					K12	– *2	High	Low	
	R				K11	– *2	High	Low	
					K10	– *2	High	Low	
96H	KCP13	KCP12	KCP11	KCP10	KCP13	1	↓	↑	K10–K13 input comparison register
					KCP12	1	↓	↑	
	R/W				KCP11	1	↓	↑	
					KCP10	1	↓	↑	
98H	EXTMF	0	MEMS1	MEMS0	EXTMF	0	On	Off	External memory access function control
	0 *5		– *2						Unused
					MEMS1	0			External memory size selection
					MEMS0	0			
	R/W	R	R/W						

MEMS [1][0] Size (bit)

[1]	[0]	Size (bit)
1	1	1M (R only) (A00–A16)
1	0	512K (R/W) (A00–A15)
0	1	256K (R/W) (A00–A14)
0	0	64K (R/W) (A00–A12)

99H	HZCS	HZBUS	ADINC	PICON	HZCS	0	High-Z	Output	$\overline{CS0}$–$\overline{CS3}$ output high-impedance control
					HZBUS	0	High-Z	Output	Address bus, $\overline{RD}$/$\overline{WR}$ high-impedance control
	R/W		W	R/W	ADINC	0	Increment	–	External memory address increment
					PICON	0	Auto inc.	Normal	External memory address auto increment mode
9AH	A03	A02	A01	A00	A03	– *2	1	0	External memory address A00–A03 (EXTMF = 1) Functions as a general-purpose register when EXTMF = 0.
					A02	– *2	1	0	
	R/W				A01	– *2	1	0	
					A00	– *2	1	0	
9BH	A07	A06	A05	A04	A07	– *2	1	0	External memory address A04–A07 (EXTMF = 1) Functions as a general-purpose register when EXTMF = 0.
					A06	– *2	1	0	
	R/W				A05	– *2	1	0	
					A04	– *2	1	0	
9CH	A11	A10	A09	A08	A11	– *2	1	0	External memory address A08–A11 (EXTMF = 1) Functions as a general-purpose register when EXTMF = 0.
					A10	– *2	1	0	
	R/W				A09	– *2	1	0	
					A08	– *2	1	0	
9DH	A15	A14	A13	A12	A15	– *2	1	0	External memory address A12–A15 (EXTMF = 1) Bits that are not used as an address for external memory access can also be used as a general-purpose register.
					A14	– *2	1	0	
	R/W				A13	– *2	1	0	
					A12	– *2	1	0	
9EH	0	0	0	A16	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R			R/W	0 *5	– *2			Unused
					A16	– *2	1	0	External memory address A16 *8

*8 When other than EXTMF = 1 and a memory less than 1M bits are used, it functions as a general-purpose register.

Table 4.1.1(c) I/O memory map (A0H–AAH)

Address *7	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
A0H	0	0	0	R0HIZ	0 *5	– *2			Unused
					0 *5	– *2			Unused * R0HIZ functions as a general-purpose
	R			R/W	0 *5	– *2			Unused register when EXTMF = 1.
					R0HIZ	0	High-Z	Output	R0 output high-impedance control (EXTMF = 0)
A1H	R03	R02	R01	R00	R03	1	High	Low	R00–R03 output port data (EXTMF = 0)
					R02	1	High	Low	Functions as a general-purpose register
	R/W				R01	1	High	Low	when EXTMF = 1.
					R00	1	High	Low	
A2H	0	0	0	R1HIZ	0 *5	– *2			Unused
					0 *5	– *2			Unused * R1HIZ functions as a general-purpose
	R			R/W	0 *5	– *2			Unused register when EXTMF = 1.
					R1HIZ	0	High-Z	Output	R1 output high-impedance control (EXTMF = 0)
A3H	R13	R12	R11	R10	R13	1	High	Low	R10–R13 output port data (EXTMF = 0)
					R12	1	High	Low	Functions as a general-purpose register
	R/W				R11	1	High	Low	when EXTMF = 1.
					R10	1	High	Low	
A4H	0	0	0	R2HIZ	0 *5	– *2			Unused
					0 *5	– *2			Unused * R2HIZ functions as a general-purpose
	R			R/W	0 *5	– *2			Unused register when EXTMF = 1.
					R2HIZ	0	High-Z	Output	R2 output high-impedance control (EXTMF = 0)
A5H	R23	R22	R21	R20	R23	1	High	Low	R20–R23 output port data (EXTMF = 0)
					R22	1	High	Low	Functions as a general-purpose register
	R/W				R21	1	High	Low	when EXTMF = 1.
					R20	1	High	Low	
A6H	R33HIZ	R32HIZ	R31HIZ	R30HIZ	R33HIZ	0	High-Z	Output	R30–R33 output high-impedance control
					R32HIZ	0	High-Z	Output	Bit corresponding to the address bus for external
	R/W				R31HIZ	0	High-Z	Output	memory can be used as a general-purpose register
					R30HIZ	0	High-Z	Output	when EXTMF = 1.
A7H	R33	R32	R31	R30	R33	1	High	Low	R30–R33 output port data
					R32	1	High	Low	Bit corresponding to the address bus for external
	R/W				R31	1	High	Low	memory can be used as a general-purpose register
					R30	1	High	Low	when EXTMF = 1.
A8H	R43HIZ	R42HIZ	R41HIZ	R40HIZ	R43HIZ	0	High-Z	Output	R43 output high-impedance control
					R42HIZ	0	High-Z	Output	R42 output high-impedance control
					R41HIZ	0	High-Z	Output	R41 output high-impedance control (EXTMF = 0)
	R/W								(General-purpose register when EXTMF = 1)
					R40HIZ	0	High-Z	Output	R40 output high-impedance control (EXTMF = 0)
									(General-purpose register when EXTMF = 1)
A9H	R43	R42	R41	R40	R43	0	High	Low	R43 output port data (SELR43 = 0)
									(General-purpose register when BZ output is selected)
					R42	0	High	Low	R42 output port data (SELR42 = 0)
									(General-purpose register when $\overline{BZ}$ output is selected)
	R/W				R41	1	High	Low	R41 output port data (EXTMF = 0)
									(General-purpose register when EXTMF = 1)
					R40	1	High	Low	R40 output port data (EXTMF = 0)
									(General-purpose register when EXTMF = 1)
AAH	SELR43	SELR42	0	0	SELR43	0	BZ	Normal	R43 function selection register (BZ or general-purpose output)
					SELR42	0	$\overline{BZ}$	Normal	R42 function selection register ($\overline{BZ}$ or general-purpose output)
	R/W		R		0 *5	– *2			Unused
					0 *5	– *2			Unused

Table 4.1.1(d) I/O memory map (B0H–BAH)

Address *7	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
B0H	IOC03	IOC02	IOC01	IOC00	IOC03	0	Output	Input	P00–P03 I/O control register (EXTMF = 0) Functions as a general-purpose register when EXTMF = 1.
					IOC02	0	Output	Input	
	R/W				IOC01	0	Output	Input	
					IOC00	0	Output	Input	
B1H	PUL03	PUL02	PUL01	PUL00	PUL03	1	On	Off	P00–P03 pull up control register (EXTMF = 0) Functions as a general-purpose register when EXTMF = 1.
					PUL02	1	On	Off	
	R/W				PUL01	1	On	Off	
					PUL00	1	On	Off	
B2H	P03	P02	P01	P00	P03	– *2	High	Low	P00–P03 I/O port data (EXTMF = 0)
					P02	– *2	High	Low	
	D03	D02	D01	D00	P01	– *2	High	Low	
					P00	– *2	High	Low	
	R/W				D03	– *2	1	0	External memory data D00–D03 (EXTMF = 1)
					D02	– *2	1	0	
					D01	– *2	1	0	
					D00	– *2	1	0	
B4H	IOC13	IOC12	IOC11	IOC10	IOC13	0	Output	Input	P10–P13 I/O control register (EXTMF = 0) Functions as a general-purpose register when EXTMF = 1.
					IOC12	0	Output	Input	
	R/W				IOC11	0	Output	Input	
					IOC10	0	Output	Input	
B5H	PUL13	PUL12	PUL11	PUL10	PUL13	1	On	Off	P10–P13 pull up control register (EXTMF = 0) Functions as a general-purpose register when EXTMF = 1.
					PUL12	1	On	Off	
	R/W				PUL11	1	On	Off	
					PUL10	1	On	Off	
B6H	P13	P12	P11	P10	P13	– *2	High	Low	P10–P13 I/O port data (EXTMF = 0)
					P12	– *2	High	Low	
	D07	D06	D05	D04	P11	– *2	High	Low	
					P10	– *2	High	Low	
	R/W				D07	– *2	1	0	External memory data D04–D07 (EXTMF = 1)
					D06	– *2	1	0	
					D05	– *2	1	0	
					D04	– *2	1	0	
B8H	IOC23	IOC22	IOC21	IOC20	IOC23	0	Output	Input	P20–P23 I/O control register (EXTMF = 0) Functions as a general-purpose register when EXTMF = 1.
					IOC22	0	Output	Input	
	R/W				IOC21	0	Output	Input	
					IOC20	0	Output	Input	
B9H	PUL23	PUL22	PUL21	PUL20	PUL23	1	On	Off	P20–P23 pull up control register (EXTMF = 0) Functions as a general-purpose register when EXTMF = 1.
					PUL22	1	On	Off	
	R/W				PUL21	1	On	Off	
					PUL20	1	On	Off	
BAH	P23	P22	P21	P20	P23	– *2	High	Low	P20–P23 I/O port data (EXTMF = 0)
					P22	– *2	High	Low	
	CS3	CS2	CS1	CS0	P21	– *2	High	Low	
					P20	– *2	High	Low	
	R/W				CS3	– *2	Disable	Active	Chip select $\overline{CS0}$–$\overline{CS3}$ active standby (EXTMF = 1)
					CS2	– *2	Disable	Active	
					CS1	– *2	Disable	Active	
					CS0	– *2	Disable	Active	

Table 4.1.1(e) I/O memory map (BCH–C2H)

Address *7	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
BCH	IOC33	IOC32	IOC31	IOC30	IOC33	0	Output	Input	P33 I/O control register (SELP33 = 0) (General-purpose register when FOUT output is selected)
					IOC32	0	Output	Input	P32 I/O control register (SELP32 = 0) (General-purpose register when PTOVF output is selected)
	R/W				IOC31	0	Output	Input	P31 I/O control register (SELP31 = 0) (General-purpose register when FR output is selected)
					IOC30	0	Output	Input	P30 I/O control register (SELP30 = 0) (General-purpose register when CL output is selected)
BDH	PUL33	PUL32	PUL31	PUL30	PUL33	1	On	Off	P33 pull up control register (SELP33 = 0) (General-purpose register when FOUT output is selected)
					PUL32	1	On	Off	P32 pull up control register (SELP32 = 0) (General-purpose register when PTOVF output is selected)
	R/W				PUL31	1	On	Off	P31 pull up control register (SELP31 = 0) (General-purpose register when FR output is selected)
					PUL30	1	On	Off	P30 pull up control register (SELP30 = 0) (General-purpose register when CL output is selected)
BEH	P33	P32	P31	P30	P33	– *2	High	Low	P33 I/O port data (SELP33 = 0) (General-purpose register when FOUT output is selected)
					P32	– *2	High	Low	P32 I/O port data (SELP32 = 0) (General-purpose register when PTOVF output is selected)
	R/W				P31	– *2	High	Low	P31 I/O port data (SELP31 = 0) (General-purpose register when FR output is selected)
					P30	– *2	High	Low	P30 I/O port data (SELP30 = 0) (General-purpose register when CL output is selected)
BFH	SELP33	SELP32	SELP31	SELP30	SELP33	0	FOUT	I/O	P33 function selection register (FOUT output or I/O)
					SELP32	0	PTOVF	I/O	P32 function selection register (PTOVF output or I/O)
	R/W				SELP31	0	FR	I/O	P31 function selection register (FR output or I/O)
					SELP30	0	CL	I/O	P30 function selection register (CL output or I/O)
C0H	IOC43	IOC42	IOC41	IOC40	IOC43	0	Output	Input	P43 I/O control register (General-purpose register when SI/F (sync. slave) is selected)
					IOC42	0	Output	Input	P42 I/O control register (General-purpose register when SI/F (sync.) is selected)
	R/W				IOC41	0	Output	Input	P41 I/O control register (ESIF = 0) (General-purpose register when SI/F is selected)
					IOC40	0	Output	Input	P40 I/O control register (ESIF = 0) (General-purpose register when SI/F is selected)
C1H	PUL43	PUL42	PUL41	PUL40	PUL43	1	On	Off	P43 pull up control register (General-purpose register when SI/F (sync. slave) is selected)
					PUL42	1	On	Off	P42 pull up control register (General-purpose register when SI/F (sync. master) is selected)
	R/W				PUL41	1	On	Off	P41 pull up control register (ESIF = 0) (General-purpose register when SI/F is selected)
					PUL40	1	On	Off	P40 pull up control register (ESIF = 0) SIN pull up control register (ESIF = 1)
C2H	P43	P42	P41	P40	P43	– *2	High	Low	P43 I/O port data (General-purpose register when SI/F (sync. slave) is selected)
					P42	– *2	High	Low	P42 I/O port data (General-purpose register when SI/F (sync.) is selected)
	R/W				P41	– *2	High	Low	P41 I/O port data (ESIF = 0) (General-purpose register when SI/F is selected)
					P40	– *2	High	Low	P40 I/O port data (ESIF = 0) (General-purpose register when SI/F is selected)

Table 4.1.1(f) I/O memory map (C8H–D2H)

Address *7	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
C8H	0	SMD1	SMD0	ESIF	0 *5	– *2			Unused
					SMD1	0			Serial I/F mode selection SMD[1][0] Mode 1 1 Asynchronous 8-bit 1 0 Asynchronous 7-bit 0 1 Clock synchronous slave 0 0 Clock synchronous master
	R	R/W			SMD0	0			
					ESIF	0	SI/F	I/O	Serial I/F enable (P4 port function selection)
C9H	EPR	PMD	SCS1	SCS0	EPR	0	WithParity	NonParity	Parity enable (only for asynchronous mode)
					PMD	0	Odd	Even	Parity mode selection
	R/W				SCS1	0			Clock source selection SCS[1][0] Clock source 1 1 PT × 1/2 1 0 CPU clock × 1/4 0 1 CPU clock × 1/8 0 0 CPU clock × 1/16
					SCS0	0			
CAH	RXTRG	RXEN	TXTRG	TXEN	RXTRG(R)	0	Run	Stop	Receive status (when reading)
					RXTRG(W)		Trigger	–	Receive trigger (when writing)
					RXEN	0	Enable	Disable	Receive enable
	R/W				TXTRG(R)	0	Run	Stop	Transmit status (when reading)
					TXTRG(W)		Trigger	–	Transmit trigger (when writing)
					TXEN	0	Enable	Disable	Transmit enable
CBH	0	FER	PER	OER	0 *5	– *2			Unused
					FER(R)	0	Error	NoError	Framing error flag (when reading)
					FER(W)		Reset	–	flag reset (when writing)
					PER(R)	0	Error	NoError	Parity error flag (when reading)
	R	R/W			PER(W)		Reset	–	flag reset (when writing)
					OER(R)	0	Error	NoError	Overrun error flag (when reading)
					OER(W)		Reset	–	flag reset (when writing)
CCH	TRXD3	TRXD2	TRXD1	TRXD0	TRXD3	– *2	High	Low	Transmit/Receive data (low-order 4 bits)
					TRXD2	– *2	High	Low	
					TRXD1	– *2	High	Low	
	R/W				TRXD0	– *2	High	Low	LSB
CDH	TRXD7	TRXD6	TRXD5	TRXD4	TRXD7	– *2	High	Low	MSB
					TRXD6	– *2	High	Low	Transmit/Receive data (high-order 4 bits)
					TRXD5	– *2	High	Low	
	R/W				TRXD4	– *2	High	Low	
D0H	LDUTY	VCCHG	0	LPWR	LDUTY	0	1/8	1/16	LCD drive duty switch
					VCCHG	0	V_{C2}	V_{C1}	LCD regulated voltage switch
	R/W				0 *5	– *2			Unused
					LPWR	0	On	Off	LCD power On/Off
D1H	0	ALOFF	ALON	0	0 *5	– *2			Unused
					ALOFF	1	AllOff	Normal	All LCD dots fade out control
	R	R/W		R	ALON	0	AllOn	Normal	All LCD dots displayed control
					0 *5	– *2			Unused
D2H	LC3	LC2	LC1	LC0	LC3	– *2			LCD contrast adjustment LC3–LC0 = 0 Light : LC3–LC0 = 15 Dark
					LC2	– *2			
	R/W				LC1	– *2			
					LC0	– *2			

Table 4.1.1(g) I/O memory map (E0H–EEH)

Address *7	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
E0H	ENRTM	ENRST	ENON	BZE	ENRTM	0	1 sec	0.5 sec	Envelope attenuation time selection
					ENRST *5	– *2	Reset	–	Envelope reset
	R/W	W	R/W		ENON	0	On	Off	Envelope On/Off
					BZE	0	Enable	Disable	BZ output enable
E1H	0	BZSTP	BZSHT	SHTPW	0 *5	– *2			Unused
					BZSTP *5	– *2	Stop	–	One-shot buzzer stop
					BZSHT(W)	– *2	Trigger	–	One-shot buzzer trigger (when writing)
					BZSHT(R)	0	Busy	Ready	One-shot buzzer status (when reading)
	R	W	R/W		SHTPW	0	125 msec	31.25 msec	One-shot buzzer pulse width selection (160/40 msec is in case of f_{OSC1} = 50 kHz)
E2H	0	BZFQ2	BZFQ1	BZFQ0	0 *5	– *2			Unused
					BZFQ2	0			Buzzer frequency selection
					BZFQ1	0			
	R	R/W			BZFQ0	0			

Buzzer frequency selection:

BZFQ [2][1][0]	Buzzer frequency	f_{OSC1} = 32 kHz (Hz)
1 1 1	f_{OSC1}/28	1170.3
1 1 0	f_{OSC1}/24	1365.3
1 0 1	f_{OSC1}/20	1638.4
1 0 0	f_{OSC1}/16	2048.0
0 1 1	f_{OSC1}/14	2340.6
0 1 0	f_{OSC1}/12	2730.7
0 0 1	f_{OSC1}/10	3276.8
0 0 0	f_{OSC1}/8	4096.0

E3H	0	BDTY2	BDTY1	BDTY0	0 *5	– *2			Unused
					BDTY2	0			Buzzer signal duty ratio selection *6
	R	R/W			BDTY1	0			
					BDTY0	0			
E8H	0	0	PTPS1	PTPS0	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R		R/W		PTPS1	0			Programmable timer clock dividing ratio selection
					PTPS0	0			
E9H	0	0	PTPC1	PTPC0	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R		R/W		PTPC1	0			PT prescaler clock source selection
					PTPC0	0			

Programmable timer clock dividing ratio selection:

PTPS [1][0]	Dividing ratio
1 1	1/256
1 0	1/32
0 1	1/4
0 0	1/1

PT prescaler clock source selection:

PTPC [1][0]	CLK
1 1	OSC3
1 0	OSC1
0 1	K02
0 0	K02 (NR)

EAH	PNRFS	PTOE	PTRUN	PTRST	PNRFS	0	1024 Hz	256 Hz	Noise rejector clock frequency selection
					PTOE	0	Enable	Disable	PTOVF output enable
	R/W			W	PTRUN	0	Run	Stop	Programmable timer Run/Stop
					PTRST *5	– *2	Rst (reload)	–	Programmable timer reset (reload)
EBH	RD3	RD2	RD1	RD0	RD3	0			MSB Programmable timer reload data (low-order 4 bits) LSB
					RD2	0			
	R/W				RD1	0			
					RD0	0			
ECH	RD7	RD6	RD5	RD4	RD7	0			MSB Programmable timer reload data (high-order 4 bits) LSB
					RD6	0			
	R/W				RD5	0			
					RD4	0			
EDH	PT3	PT2	PT1	PT0	PT3	0			MSB Programmable timer data (low-order 4 bits) LSB
					PT2	0			
	R				PT1	0			
					PT0	0			
EEH	PT7	PT6	PT5	PT4	PT7	0			MSB Programmable timer data (high-order 4 bits) LSB
					PT6	0			
	R				PT5	0			
					PT4	0			

Table 4.1.1(h) I/O memory map (F0H–FCH)

Address *7	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
F0H	0	0	0	EIPT	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R			R/W	0 *5	– *2			Unused
					EIPT	0	Enable	Mask	Interrupt mask register (programmable timer)
F1H	0	EISIFE	EISIFT	EISIFR	0 *5	– *2			Unused
					EISIFE	0	Enable	Mask	Interrupt mask register (serial I/F error)
	R	R/W			EISIFT	0	Enable	Mask	Interrupt mask register (serial I/F transmitting)
					EISIFR	0	Enable	Mask	Interrupt mask register (serial I/F receiving)
F2H	0	0	0	EIK1	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R			R/W	0 *5	– *2			Unused
					EIK1	0	Enable	Mask	Interrupt mask register (K10–K13)
F3H	0	0	0	EIK0	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R			R/W	0 *5	– *2			Unused
					EIK0	0	Enable	Mask	Interrupt mask register (K00–K03)
F4H	EIT3	EIT2	EIT1	EIT0	EIT3	0	Enable	Mask	Interrupt mask register (clock timer 1 Hz)
					EIT2	0	Enable	Mask	Interrupt mask register (clock timer 2 Hz)
	R/W				EIT1	0	Enable	Mask	Interrupt mask register (clock timer 8 Hz)
					EIT0	0	Enable	Mask	Interrupt mask register (clock timer 16 Hz)
									* When f_{OSC1} = 50 kHz: 16 Hz → 12.5 Hz
F8H	0	0	0	IPT	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R				0 *5	– *2			Unused
					IPT *4	0	Yes	No	Interrupt factor flag (programmable timer)
F9H	0	ISIFE	ISIFT	ISIFR	0 *5	– *2			Unused
					ISIFE*4	0	Yes	No	Interrupt factor flag (serial I/F error)
	R				ISIFT*4	0	Yes	No	Interrupt factor flag (serial I/F transmitting)
					ISIFR*4	0	Yes	No	Interrupt factor flag (serial I/F receiving)
FAH	0	0	0	IK1	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R				0 *5	– *2			Unused
					IK1 *4	0	Yes	No	Interrupt factor flag (K10–K13)
FBH	0	0	0	IK0	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R				0 *5	– *2			Unused
					IK0 *4	0	Yes	No	Interrupt factor flag (K00–K03)
FCH	IT3	IT2	IT1	IT0	IT3 *4	0	Yes	No	Interrupt factor flag (clock timer 1 Hz)
					IT2 *4	0	Yes	No	Interrupt factor flag (clock timer 2 Hz)
	R				IT1 *4	0	Yes	No	Interrupt factor flag (clock timer 8 Hz)
					IT0 *4	0	Yes	No	Interrupt factor flag (clock timer 16 Hz)
									* When f_{OSC1} = 50 kHz: 16 Hz → 12.5 Hz

4.2 Setting of Power Supply and Operating Mode

This section explains the control of the operating mode and the LCD drive voltage. See Section 2.1, "Power Supply" for the configuration of the power supply circuit.

4.2.1 Control of supply voltage doubler/halver

When the voltage more than a value that can drive the oscillation system regulated voltage circuit or the LCD system voltage circuit is not obtained, drive each power supply circuit using the voltage that is doubled with the supply voltage by the voltage doubler/halver. On the other hand, when the supply voltage has some redundancy, drive the power supply circuit using the voltage that is halved to reduce current consumption.
Control of the voltage doubler/halver is done using the registers DBON and HLON.

- When not performing doubling/halves: Set to DBON = "0" and HLON = "0"
- When performing doubling: Set to DBON = "1" and HLON = "0"
- When performing halves: Set to DBON = "0" and HLON = "1"

Since the voltage doubler/halver is used in common with the oscillation system regulated voltage circuit, when the doubling or halves voltage is used for either of these circuits, set it accordingly. The doubled/halved voltage is output as V_{D2} from the voltage doubler/halver.

Note: The DBON has priority over the HLON.

Either V_{DD} or V_{D2} can be selected as the drive voltage for the oscillation system regulated voltage circuit and the LCD system voltage circuit, independently. This operation mode control is done using the register VDSEL for the oscillation system regulated voltage circuit and the register VCSEL for the LCD system voltage circuit. By writing "1" in the registers, V_{D2} is selected as the drive voltage and writing "0", V_{DD} is selected.
After turning the voltage doubler/halver on by the HLON or DBON, about 100 msec is necessary until the V_{D2} voltage stabilizes. Therefore, switching the operating mode should be done as the following sequences.

Normal mode → reduce/boost mode

1. Turn the voltage doubler/halver on (set HLON = "1" or DBON = "1").
2. Maintain 100 msec or more.
3. Set "1" into the VDSEL (for the oscillation system regulated voltage circuit) or VCSEL (for the LCD system voltage circuit).

Reduce/boost mode → normal mode

1. Set "0" into the VDSEL or VCSEL.
2. Turn the voltage doubler/halver off (set HLON = "0" and DBON = "0").

Note:
- *When the supply voltage is out of the specified voltage range of an operating mode, do not switch into the operating mode. It may cause malfunction or increase current consumption.*
- *When operating with 0.9–1.25 V supply voltage, the boost mode must be set for both the oscillation system regulated voltage circuit and the LCD system voltage circuit in the initial routine that is executed immediately after an initial reset before controlling the peripheral circuits. At initial reset, the normal mode is set.*
- *When switching from the boost/reduce mode to the normal mode, use separate instructions to switch the mode (VDSEL = "0" or VCSEL = "0") and turn the voltage doubler/halver off (HLON = "0" or DBON = "0"). Simultaneous processing with a single instruction may cause malfunction.*

4.2.2 Operating mode for oscillation system regulated voltage circuit and internal operating voltage

The oscillation system regulated voltage circuit generates the operating voltage V_{D1} for the oscillation circuit and internal logic circuit. This V_{D1} voltage must be switched according to the oscillation circuit and the oscillation frequency to be used. The operating mode for the oscillation system regulated voltage circuit must be also switched depending on the supply voltage.
Control of V_{D1} and oscillation circuit will be explained in Section 4.4, "Oscillation Circuit", this section explains the operating mode for the oscillation system regulated voltage circuit that must be set before controlling the oscillation circuit.
The following shows the setting contents according to the supply voltage and the oscillation circuit.

Table 4.2.2.1 Supply voltage and operating mode

Power circuit	CPU clock	Operating voltage V_{D1}	Supply voltage V_{DD} (V)			
			0.9–1.25	1.25–2.2	2.2–2.6	2.6–3.6
Oscillation system regulated voltage circuit	OSC1	1.2 V	Boost mode	Normal mode*		Reduce or normal mode
	OSC3, 200kHz	1.4 V	Boost mode		Normal mode*	
	OSC3, 1MHz	2.1 V	Cannot be used		Normal mode	

* Set the boost mode when supply voltage drop is detected by the SVD circuit, such as during heavy load operation (buzzer sounds or a lamp lights) or by the battery life.

(1) Supply voltage V_{DD} = 0.9–1.25 V

When the supply voltage is in this range, the oscillation system regulated voltage circuit can be operated only in the boost mode.
Set the boost mode in the initial routine, and after that do not change to the other mode during operating. Moreover, the 1 MHz clock in the OSC3 oscillation circuit cannot be generated in this voltage range.

(2) Supply voltage V_{DD} = 1.25–2.2 V

When the CPU is operated with the OSC1 clock only (OSC3 oscillation circuit is off), the oscillation system regulated voltage circuit can be operated in the normal mode. Be sure not to set in the reduce mode. The boost mode can be set, but do not use it in normal operation because it increases current consumption.
When switching the CPU clock from OSC1 to OSC3 (200 kHz), set the boost mode before switching V_{D1} to 1.4 V (V_{D1} switching is necessary before turning the OSC3 oscillation circuit on). Switching the OSC3 clock leaving in the normal mode may cause malfunction. On the other hand, when switched from OSC3 (200 kHz) to OSC1, after turning the OSC3 oscillation circuit off, return V_{D1} to 1.2 V then return to the normal mode.
1 MHz clock in the OSC3 oscillation circuit cannot be generated in this voltage range.

As described above, OSC3 (200 kHz) clock can be used by setting the boost mode, but 3.6 V or more is generated by doubling if the supply voltage is 1.8 V or more. It does not cause any problems in operation, but, it is not advisable to reduce current consumption. When OSC3 (200 kHz) is used, do not use 1.8–2.2 V supply voltage, if possible.

(3) Supply voltage V_{DD} = 2.2–2.6 V

When the supply voltage is in this range, the oscillation system regulated voltage circuit can always be operated in the normal mode regardless of the oscillation circuit setting. Be sure not to set to the reduce mode.
In this voltage range, 1 MHz clock can be generated by the OSC3 oscillation circuit and V_{D1} can be switched without changing the operating mode.

(4) Supply voltage V_{DD} = 2.6–3.6 V

When the supply voltage is in this range, the oscillation system regulated voltage circuit can be operated in the normal mode regardless of the oscillation circuit setting. Be sure not to set to the boost mode. In addition, when the CPU is operated by the OSC1 clock (OSC3 oscillation circuit is off), the reduce mode can be set to reduce current consumption.
In this voltage range, OSC3 oscillation circuit can be used only in the normal mode. When switching to the OSC3 clock during operating in the reduce mode, it should be done after switching the operating mode into the normal mode.

4.2.3 Operating mode for LCD system voltage circuit and reference voltage for LCD driving

The LCD system voltage circuit generates the voltages V_{C1}, V_{C2}, V_{C4} and V_{C5} to drive the LCD.
First the LCD system voltage circuit generates V_{C1} or V_{C2} by the built-in regulated voltage circuit, then generates three other voltages by boosting or reducing those voltages.
Output on or off of the LCD power supply can be controlled using the register LPWR, the LCD drive voltage is output to the LCD driver and SVD circuit only when it is on (LPWR = "1"). This control is necessary when external impression of the LCD drive voltage has been selected by the mask option. The controls explained below are unnecessary when external impression of the LCD drive voltage has been selected.

Table 4.2.3.1 shows the voltage values of V_{C1}, V_{C2}, V_{C4} and V_{C5} generated by the LCD system voltage circuit and the status of boosting/reducing.

Table 4.2.3.1 LCD drive voltage generated internally

LCD drive voltage	V_{DD} = 0.9–3.6 V	V_{DD} = 2.6–3.6 V
V_{C1} (0.975–1.2 V)	V_{C1} (standard)	$1/2 \times V_{C2}$
V_{C2} (1.950–2.4 V)	$2 \times V_{C1}$	V_{C2} (standard)
V_{C4} (2.925–3.6 V)	$3 \times V_{C1}$	$3/2 \times V_{C2}$
V_{C5} (3.900–4.8 V)	$4 \times V_{C1}$	$2 \times V_{C2}$

Select either V_{C1} standard or V_{C2} standard using the register VCCHG.
When "1" is written to the VCCHG, V_{C2} standard is selected and when "0" is written, V_{C1} standard is selected. At initial reset, V_{C1} standard (VCCHG = "0") is set.

The operating mode should be set according to the supply voltage and the V_{C1}/V_{C2} selection for the LCD system voltage circuit set the same as the oscillation system regulated voltage circuit.
The following shows the setting contents according to supply voltage.

Table 4.2.3.2 Supply voltage and operating mode

Power circuit	Operating condition	Supply voltage V_{DD} (V)			
		0.9–1.25	1.25–2.2	2.2–2.6	2.6–3.6
LCD system voltage circuit	V_{C1} standard	Boost mode	Normal mode*		Reduce or normal mode
	V_{C2} standard	Cannot be used			Normal mode

* Set the boost mode when supply voltage drop is detected by the SVD circuit, such as during heavy load operation (buzzer sounds or a lamp lights) or by the battery life.

(1) Supply voltage V_{DD} = 0.9 –1.25 V

When the supply voltage is in this range, the LCD system voltage circuit can be operated only in the boost mode.
Set the boost mode in the initial routine, and after that do not change to an other mode during operating. Moreover, V_{C2} standard cannot be selected in this voltage range.

(2) Supply voltage V_{DD} = 1.25–2.6 V

When the supply voltage is in this range, the LCD system voltage circuit can be operated only in the normal mode. Be sure not to switch the power for the LCD system voltage circuit into the output of the voltage doubler/halver (writing "1" to the VCSEL). Moreover, V_{C2} standard cannot be selected in this voltage range.

(3) Supply voltage V_{DD} = 2.6–3.6 V

When the supply voltage is in this range, the LCD system voltage circuit can be operated in the normal mode. Be sure not to set to the boost mode. V_{C2} standard can be selected in this voltage range. Also it is possible to select V_{C1} standard and to operate in the normal mode or reduce mode. However, select V_{C2} standard for normal use because V_{C2} standard improves display quality and reduces current consumption more than V_{C1} standard.

4.2.4 Control of power supply and operating mode

Table 4.2.4.1 lists the control bits and their addresses for the power supply and the operating mode.

Table 4.2.4.1 Control bits of power supply and operating mode

Address *7	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
84H	VCSEL	VDSEL	HLON	DBON	VCSEL	0	V_{D2}	V_{DD}	Power selection for LCD system voltage circuit
					VDSEL	0	V_{D2}	V_{DD}	Power selection for oscillation system regulated voltage circuit
	R/W				HLON	0	On	Off	Halver On/Off
					DBON	0	On	Off	Doubler On/Off
D0H	LDUTY	VCCHG	0	LPWR	LDUTY	0	1/8	1/16	LCD drive duty switch
					VCCHG	0	V_{C2}	V_{C1}	LCD regulated voltage switch
	R/W				0 *5	– *2			Unused
					LPWR	0	On	Off	LCD power On/Off

*1 Initial value at the time of initial reset
*2 Not set in the circuit
*3 Undefined
*4 Reset (0) immediately after being read
*5 Constantly "0" when being read
*6 Refer to main manual
*7 I/O memory is allocated from page 0 to 3

DBON: Doubler ON/OFF (84H•D0)

Controls doubling ON/OFF for the voltage doubler/halver.

When "1" is written: Doubler ON
When "0" is written: Doubler OFF
Reading: Valid

When supply voltage is in a range of 0.9 to 1.25 V (0.9 to 2.2 V when 200 kHz OSC3 clock is used), generate V_{D2} by doubling the supply voltage to drive the internal power supply circuit. When "1" is written to DBON, the voltage doubler/halver generates V_{D2} doubling with supply voltage. When "0" is written, doubling is not performed.
When supply voltage is 1.25 V or more (2.2 V or more when 200 kHz OSC3 clock is used), do not double the supply voltage.
At initial reset, this register is set to "0".
The DBON has priority over the HLON.

HLON: Halver ON/OFF (84H•D1)

Controls halves ON/OFF for the voltage doubler/halver.

When "1" is written: Halver ON
When "0" is written: Halver OFF
Reading: Valid

When supply voltage is in a range of 2.6 to 3.6 V, the internal power supply circuit can be driven by the halved voltage to reduce current consumption. When "1" is written to HLON, the voltage doubler/halver generates V_{D2} halving with supply voltage. When "0" is written, halving is not performed.
When supply voltage is 2.6 V or less, do not halve the supply voltage.
At initial reset, this register is set to "0".

VDSEL: Power selection for oscillation system regulated voltage circuit (84H•D2)

Selects the power for the oscillation system regulated voltage circuit.

When "1" is written: V_{D2}
When "0" is written: V_{DD}
Reading: Valid

When "1" is written to VDSEL, the oscillation system regulated voltage circuit operates with V_{D2} output from the voltage doubler/halver. It becomes the boost mode or the reduce mode according to the DBON and HLON settings. When "0" is written to VDSEL, the oscillation system regulated voltage circuit operates with V_{DD} and it becomes the normal mode.
When switching from the normal mode to the boost/reduce mode, VDSEL should be set to "1" wait 100 msec or more for the V_{D2} to stabilize after setting DBON or HLON to "1".
At initial reset, this register is set to "0".

VCSEL: Power selection for LCD system voltage circuit (84H•D3)
Selects the power for the LCD system voltage circuit.

When "1" is written: V_{D2}
When "0" is written: V_{DD}
Reading: Valid

When "1" is written to VCSEL, the LCD system voltage circuit operates with V_{D2} output from the voltage doubler/halver. It becomes the boost mode or the reduce mode according to the DBON and HLON settings. When "0" is written to VCSEL, the LCD system voltage circuit operates with V_{DD} and it becomes the normal mode.
When switching from the normal mode to the boost/reduce mode, VDSEL should be set to "1" taking 100 msec or more stabilizing time for V_{D2} after setting DBON or HLON to "1".
At initial reset, this register is set to "0".

LPWR: LCD power ON/OFF (D0H•D0)
Controls the LCD system voltage circuit ON/OFF.

When "1" is written: ON
When "0" is written: OFF
Reading: Valid

When "1" is written to LPWR, the LCD system voltage circuit goes ON and generates the LCD drive voltage. When "0" is written, the LCD drive voltage is not output.
At initial reset, this register is set to "0".

VCCHG: LCD regulated voltage switching (D0H•D2)
Selects the reference voltage for the LCD drive voltage.

When "1" is written: V_{C2}
When "0" is written: V_{C1}
Reading: Valid

When "1" is written to VCCHG, the LCD system voltage circuit generates the LCD drive voltage as V_{D2} standard. When "0" is written into the VCCHG, it becomes V_{C1} standard. Select V_{C2} when supply voltage is 2.6 V or more, otherwise, select V_{C1}.
At initial reset, this register is set to "0".

4.2.5 Programming notes

(1) When operating with 0.9–1.25 V supply voltage, the boost mode must be set in the initial routine before controlling the peripheral circuits.

(2) When the supply voltage is out of the specified voltage range of an operating mode, do not switch into the operating mode. It may cause a malfunction or increase current consumption.

(3) Do not set HLON (halves) and DBON (doubling) to "1" at the same time.

(4) When switching from the normal mode to the boost/reduce mode, VDSEL should be set to "1" wait 100 msec or more for V_{D2} to stabilize after setting DBON or HLON to "1".

(5) When switching from the boost/reduce mode to the normal mode, use separate instructions to switch the mode (VDSEL = "0" or VCSEL = "0") and turn the voltage doubler/halver off (HLON = "0" or DBON = "0"). Simultaneous processing with a single instruction may cause malfunction.

4.3 Resetting Watchdog Timer

4.3.1 Configuration of watchdog timer

The E0C6247 has a built-in watchdog timer that operates with a 256 Hz (200 Hz when f_{OSC1} = 50 kHz) clock divided from the OSC1. The watchdog timer must be reset cyclically by the software. If reset is not executed in at least 3–4 seconds (3.84–5.12 seconds when f_{OSC1} = 50 kHz), the initial reset signal is output automatically for the CPU.
Figure 4.3.1.1 is the block diagram of the watchdog timer.

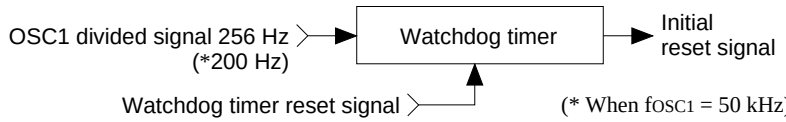


Fig. 4.3.1.1 Watchdog timer block diagram

The watchdog timer contains a 10-bit binary counter, and generates the initial reset signal internally by an overflow of 0.25 Hz counted in the last stage (0.2 Hz when f_{OSC1} = 50 kHz).
Watchdog timer reset processing in the program's main routine enables detection of program overrun, such as when the main routine's watchdog timer processing is bypassed. Ordinarily this routine is incorporated where periodic processing takes place, just as for the timer interrupt routine.
The watchdog timer operates in the HALT mode. If the HALT status continues for 3–4 seconds (3.84–5.12 seconds when f_{OSC1} = 50 kHz), the initial reset signal restarts operation.

4.3.2 Mask option

Whether the watchdog timer will be used or not can be selected by the mask option. When "Not used" is selected, it is unnecessary to reset the watchdog timer.

4.3.3 Control of watchdog timer

Table 4.3.3.1 lists the watchdog timer's control bits and their addresses.

Table 4.3.3.1 Control bits of watchdog timer

Address *7	Register								Comment
	D3	D2	D1	D0	Name	Init *1	1	0	
8BH	0	0	0	WDRST	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R			W	0 *5	– *2			Unused
					WDRST	Reset	Reset	–	Watchdog timer reset

*1 Initial value at the time of initial reset
*2 Not set in the circuit
*3 Undefined
*4 Reset (0) immediately after being read
*5 Constantly "0" when being read
*6 Refer to main manual
*7 I/O memory is allocated from page 0 to 3

WDRST: Watchdog timer reset (8BH•D0)
This is the bit for resetting the watchdog timer.

When "1" is written: Watchdog timer is reset
When "0" is written: No operation
Reading: Always "0"

When "1" is written to WDRST, the watchdog timer is reset, and the operation restarts immediately after this. When "0" is written, no operation results.
This bit is dedicated for writing, and is always "0" for reading.

4.3.4 Programming note

When the watchdog timer is being used, the software must reset it within 3-second cycles.

4.4 Oscillation Circuit

4.4.1 Configuration of oscillation circuit

The E0C6247 has two oscillation circuits (OSC1 and OSC3). OSC1 is a crystal oscillation circuit that supplies the operating clock to the CPU and peripheral circuits. OSC3 is either a CR or ceramic oscillation circuit. When processing with the E0C6247 requires high-speed operation, the CPU operating clock can be switched from OSC1 to OSC3. To stabilize operation of the internal circuit, the operating voltage V_{D1} must be switched according to the oscillation circuit to be used and the oscillation frequency.
Figure 4.4.1.1 is the block diagram of this oscillation system.

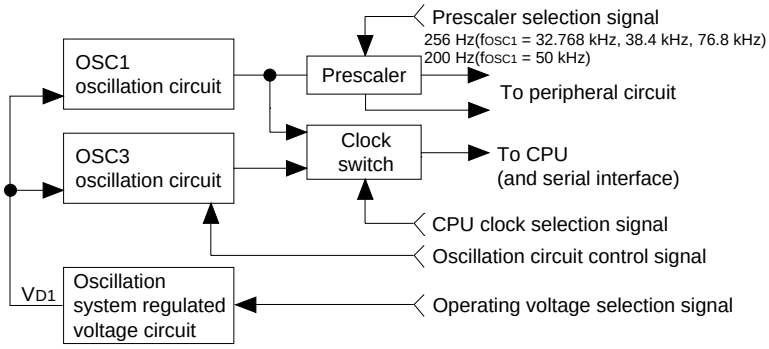


Fig. 4.4.1.1 Oscillation system

The OSC1 oscillation circuit can deal with four types of oscillation frequencies (32.768 kHz, 38.4 kHz, 50.0 kHz or 76.8 kHz). For this purpose, the prescalers (dividing stages) for the frequencies are connected to the OSC1 oscillation circuit, and one of them should be selected by the software according to the frequency to be used.

4.4.2 OSC1 oscillation circuit

The E0C6247 has a built-in crystal oscillation circuit (OSC1 oscillation circuit). As an external element, the OSC1 oscillation circuit generates the operating clock for the CPU and peripheral circuitry by connecting the crystal oscillator (Typ. 32.768 kHz, 38.4 kHz, 50 kHz or 76.8 kHz) and trimmer capacitor (5–25 pF).
Figure 4.4.2.1 is the block diagram of the OSC1 oscillation circuit.

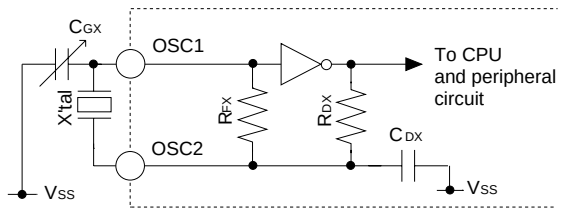


Fig. 4.4.2.1 OSC1 oscillation circuit

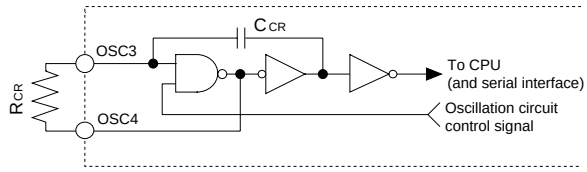
As Figure 4.4.2.1 indicates, the crystal oscillation circuit can be configured simply by connecting the crystal oscillator (X'tal) between terminals OSC1 and OSC2 to the trimmer capacitor (C_{GX}) between terminals OSC1 and V_{SS}.

Note: The OSC1 oscillation circuit deal with four types of crystal oscillators (32.768 kHz, 38.4 kHz, 50 kHz or 76.8 kHz). To operate the timer and other circuits properly, the prescaler should be selected according to the frequency of the connected oscillator.

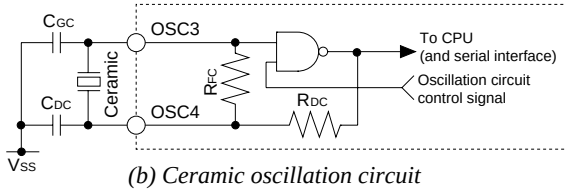
4.4.3 OSC3 oscillation circuit

The E0C6247 has twin clock specification. The mask option enables selection of either the CR or ceramic oscillation circuit (OSC3 oscillation circuit) as the CPU's sub-clock for high-speed operation (Typ. 200 kHz or 1 MHz). Because the oscillation circuit itself is built-in, it provides the resistance as an external element when CR oscillation is selected, but when ceramic oscillation is selected both the ceramic oscillator and two capacitors (gate and drain capacitance) are required.

Figure 4.4.3.1 is the block diagram of the OSC3 oscillation circuit.



(a) CR oscillation circuit



(b) Ceramic oscillation circuit

Fig. 4.4.3.1 OSC3 oscillation circuit

As indicated in Figure 4.4.3.1, the CR oscillation circuit can be configured simply by connecting the resistor (R_{CR}) between terminals OSC3 and OSC4 when CR oscillation is selected. See Chapter 7, "ELECTRICAL CHARACTERISTICS" for resistance value of R_{CR}.
When ceramic oscillation is selected, the ceramic oscillation circuit can be configured by connecting the ceramic oscillator (Typ. 1 MHz) between terminals OSC3 and OSC4 to the two capacitors (C_{GC} and C_{DC}) located between terminals OSC3 and OSC4 and V_{SS}. For both C_{GC} and C_{DC}, connect capacitors that are about 100 pF. To lower current consumption of the OSC3 oscillation circuit, oscillation can be stopped by the software (OSCC register).
When performing 1 MHz oscillation, a 2.2 V or more voltage is necessary.

4.4.4 Switching of operating voltage

The CPU system clock is switched to OSC1 or OSC3 by the software (CLKCHG register). In this case, to obtain stable operation, the operating voltage V_{D1} for the internal circuit must be switched by the software (VDC1 and VDC0 registers). As described in Section 4.2, "Setting of Power Supply and Operation Mode", the oscillation system regulated voltage circuit that generates V_{D1} must be set in an appropriate operating mode according to supply voltage.
Table 4.4.4.1 shows the correspondence of the system clock, operating voltage V_{D1} and operating mode for the oscillation system regulated voltage circuit.

Table 4.4.4.1 System clock and operating voltage

System clock	Operating voltage V_{D1} (V)	Operating mode according to V_{DD} (V)			
		0.9–1.25	1.25–2.2	2.2–2.6	2.6–3.6
OSC1	1.2	Boost mode	Normal mode*		Reduce or normal mode
OSC3, 200 kHz	approx. 1.4	Boost mode		Normal mode*	
OSC3, 1 MHz	2.1	Cannot be used		Normal mode	

* Set the boost mode when supply voltage drop is detected by the SVD circuit, such as during heavy load operation (buzzer sounds or a lamp lights) or by the battery life.

When switching the operating voltage and the system clock, properly set the operating mode for the oscillation system regulated voltage circuit before and after. (See Section 4.2, "Setting of Power Supply and Operation Mode".)

When OSC3 is to be used as the CPU system clock, it should be done as the following procedure using the software: first switch the operating mode (if necessary) and the operating voltage V_{D1}, turn the OSC3 oscillation ON after waiting 2.5 msec or more for the above operation to stabilize, switch the clock after waiting 5 msec or more for oscillation stabilization.
When switching from OSC3 to OSC1, turn the OSC3 oscillation circuit OFF after switching the clock then set the operating voltage V_{D1} to 1.2 V. After that, switch the operating mode if necessary.
Furthermore, when switching V_{D1} from 1.2V (for OSC1) to 2.1 V (for OSC3, 1 MHz) or from 2.1 V to 1.2 V, be sure to hold the 1.4 V setting for more than 2.5 msec first for voltage stabilization.

OSC1 → OSC3 (200 kHz)

1. Set operation mode for OSC3 (200 kHz). *1
2. Set VDC1 and VDC0 to "01" (1.2 V → 1.4 V).
3. Maintain 2.5 msec or more.
4. Set OSCC to "1" (OSC3 oscillation ON).
5. Maintain 5 msec or more.
6. Set CLKCHG to "1" (OSC1 → OSC3).

OSC3 (200 kHz) → OSC1

1. Set CLKCHG to "0" (OSC3 → OSC1).
2. Set OSCC to "0" (OSC3 oscillation OFF).
3. Set VDC1 and VDC0 to "00" (1.4 V → 1.2 V).
4. Set operation mode for OSC1. *1

(*1: It should be done if necessary.)

OSC1 → OSC3 (1 MHz)

1. Set operating mode to the normal mode. *2
2. Set VDC1 and VDC0 to "01" (1.2 V → 1.4 V).
3. Maintain 2.5 msec or more.
4. Set VDC1 and VDC0 to "11" (1.4 V → 2.1 V).
5. Maintain 2.5 msec or more.
6. Set OSCC to "1" (OSC3 oscillation ON).
7. Maintain 5 msec or more.
8. Set CLKCHG to "1" (OSC1 → OSC3).

OSC3 (1 MHz) → OSC1

1. Set CLKCHG to "0" (OSC3 → OSC1).
2. Set OSCC to "0" (OSC3 oscillation OFF).
3. Set VDC1 and VDC0 to "01" (2.1 V → 1.4 V).
4. Maintain 2.5 msec or more.
5. Set VDC1 and VDC0 to "00" (1.4 V → 1.2 V).
6. Set operation mode for OSC1. *2

(*2: It should be done only when operating in the reduce mode with OSC1.)

The following shows the operating mode settings for the oscillation system regulated voltage circuit depending on supply voltage.

(1) Supply voltage V_{DD} = 0.9–1.25 V

When the supply voltage is in this range, the oscillation system regulated voltage circuit can be operated only in the boost mode. Therefore, it is unnecessary to switch the operating mode before and after switching the system clock. Moreover, the 1 MHz clock in the OSC3 oscillation circuit cannot be generated in this voltage range.

(2) Supply voltage V_{DD} = 1.25–2.2 V

When the system clock is OSC1, operate in the normal mode. Before switching to the OSC3 clock (200 kHz), set the boost mode. Do not switch to the OSC3 clock in the normal mode because it may cause a malfunction. 1 MHz clock in the OSC3 oscillation circuit cannot be generated in this voltage range.

(3) Supply voltage V_{DD} = 2.2–2.6 V

When the supply voltage is in this range, the oscillation system regulated voltage circuit can always be operated in the normal mode regardless of the system clock selection. Therefore, it is unnecessary to switch the operating mode before and after switching the system clock. In this voltage range, 1 MHz clock can be generated by the OSC3 oscillation circuit.

(4) Supply voltage V_{DD} = 2.6–3.6 V

When the system clock is OSC1, the reduce mode can be set to reduce current consumption. In this case, return to the normal mode before switching the system clock to OSC3. After switching from OSC3 to OSC1, return to the reduce mode. It is unnecessary to switch the operating mode before and after switching the system clock when operating in the normal mode.
Be sure not to switch to the OSC3 clock in the reduce mode because it may cause a malfunction.

Note: Switching the operating voltage when the supply voltage is lower than the set voltage (that can generate V_{D1}) may cause a malfunction. Switch the operating voltage only after making sure that supply voltage is more than the set voltage using the SVD circuit.

4.4.5 Clock frequency and instruction execution time

Table 4.4.5.1 shows the instruction execution time according to each frequency of the system clock.

Table 4.4.5.1 Clock frequency and instruction execution time

Clock frequency	Instruction execution time (μsec)		
	5-clock instruction	7-clock instruction	12-clock instruction
OSC1: 32.768 kHz	152.6	213.6	366.2
OSC1: 38.4 kHz	130.2	182.3	312.5
OSC1: 50.0 kHz	100.0	140.0	240.0
OSC1: 76.8 kHz	65.1	91.1	156.3
OSC3: 200 kHz	25.0	35.0	60.0
OSC3: 1 MHz	5.0	7.0	12.0

4.4.6 Control of oscillation circuit

Table 4.4.6.1 lists the control bits and their addresses for the oscillation circuit.

Table 4.4.6.1 Control bits of oscillation circuit

Address *7	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
88H	0	0	PRSM1	PRSM0	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R		R/W		PRSM1	0			OSC1 prescaler selection
					PRSM0	0			
89H	CLKCHG	OSCC	VDC1	VDC0	CLKCHG	0	OSC3	OSC1	CPU system clock switch
					OSCC	0	On	Off	OSC3 oscillation On/Off
	R/W				VDC1	0			CPU operating voltage switch
					VDC0	0			

PRSM[1][0] / fOSC1 (kHz): 1 1 — 76.8; 1 0 — 50.0; 0 1 — 38.4; 0 0 — 32.768

VDC[1][0] / VD1 / Oscillation circuit: 1 * — 2.1 V — OSC3 (1 MHz); 0 1 — 1.4 V — OSC3 (200 kHz); 0 0 — 1.2 V — OSC1

*1 Initial value at the time of initial reset
*2 Not set in the circuit
*3 Undefined
*4 Reset (0) immediately after being read
*5 Constantly "0" when being read
*6 Refer to main manual
*7 I/O memory is allocated from page 0 to 3

PRSM1, PRSM0: OSC1 prescaler selection (88H•D1, D0)

Selects the prescaler for the OSC1 oscillation circuit.

Table 4.4.6.2 Prescaler selection

PRSM1	PRSM0	Oscillation frequency
1	1	76.8 kHz
1	0	50.0 kHz
0	1	38.4 kHz
0	0	32.768 kHz

Select one according to the connected oscillator.

VDC1, VDC0: CPU operating voltage switch (89H•D1, D0)

Switches the operating voltage V_{D1}.

Table 4.4.6.3 Setting of operating voltage V_{D1}

VDC1	VDC0	Operating voltage V_{D1}	Oscillation circuit
1	1 or 0	2.1 V	OSC3 (1 MHz)
0	1	approx. 1.4 V	OSC3 (200 kHz)
0	0	1.2 V	OSC1

When switching the CPU system clock, the operating voltage V_{D1} should also be switched according to the clock.
When switching from OSC1 to OSC3, set V_{D1} before turning the OSC3 oscillation ON. After that maintain 2.5 msec or more, and then turn the OSC3 oscillation ON.
When switching from OSC3 to OSC1, set V_{D1} to 1.2 V after switching to OSC1 and turning the OSC3 oscillation OFF.
When switching V_{D1} from 1.2 V to 2.1 V, or vice versa, be sure to hold the 1.4 V setting for more than 2.5 msec or more first for voltage stabilization.
It is necessary to switch the operating mode for the oscillation system regulated voltage circuit depending on the supply voltage.
At initial reset, this register is set to "0".

OSCC: OSC3 oscillation control (89H•D2)

Controls oscillation ON/OFF for the OSC3 oscillation circuit.

When "1" is written: OSC3 oscillation ON
When "0" is written: OSC3 oscillation OFF
Reading: Valid

When it is necessary to operate the CPU at high speed, set OSCC to "1". At other times, set it to "0" to reduce current consumption. Furthermore, when performing this setting, it is necessary to switch the operating voltage V_{D1}.
At initial reset, this register is set to "0".

CLKCHG: The CPU's clock switch (89H•D3)

The CPU's operation clock is selected with this register.

When "1" is written: OSC3 clock is selected
When "0" is written: OSC1 clock is selected
Reading: Valid

When the CPU clock is to be OSC3, set CLKCHG to "1"; for OSC1, set CLKCHG to "0".
After turning the OSC3 oscillation ON (OSCC = "1"), switching of the clock should be done after waiting 5 msec or more.
When V_{D1} is 1.2 V (VDC1 = VDC0 = "0"), setting of CLKCHG = "1" becomes invalid and switching to OSC3 is not performed.
At initial reset, this register is set to "0".

4.4.7 Programming notes

(1) When switching the CPU system clock from OSC1 to OSC3, set V_{D1} and the operating mode before turning the OSC3 oscillation ON. After that maintain 2.5 msec or more, and then turn the OSC3 oscillation ON.
When switching from OSC3 to OSC1, set V_{D1} and the operating mode after switching to OSC1 and turning the OSC3 oscillation OFF.

(2) When switching V_{D1} from 1.2 V to 2.1 V, or vice versa, be sure to hold the 1.4 V setting for more than 2.5 msec or more first for voltage stabilization.

(3) It takes at least 5 msec from the time the OSC3 oscillation circuit goes ON until the oscillation stabilizes. Consequently, when switching the CPU operation clock from OSC1 to OSC3, do this after a minimum of 5 msec have elapsed since the OSC3 oscillation went ON.
Further, the oscillation stabilization time varies depending on the external oscillator characteristics and conditions of use, so allow ample margin when setting the wait time.

(4) When switching the clock form OSC3 to OSC1, use a separate instruction for switching the OSC3 oscillation OFF. An error in the CPU operation can result if this processing is performed at the same time by the one instruction.

(5) Switching the operating voltage when the supply voltage is lower than the set voltage (that can generate V_{D1}) may cause a malfunction. Switch the operating voltage only after making sure that supply voltage is more than the set voltage using the SVD circuit.

(6) The OSC1 oscillation circuit deal with four types of crystal oscillators (32.768 kHz, 38.4 kHz, 50 kHz or 76.8 kHz). To operate the timer and other circuits properly, the prescaler should be selected according to the frequency of the connected oscillator.

4.5 Input Ports (K00–K03 and K10–K13)

4.5.1 Configuration of input ports

The E0C6247 has eight bits general-purpose input ports. Each of the input port terminals (K00–K03, K10–K13) provides internal pull up resistor. Pull up resistor can be selected for each bit with the mask option. Figure 4.5.1.1 shows the configuration of input port.

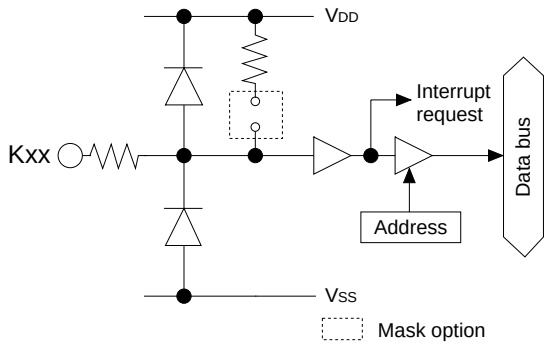


Fig. 4.5.1.1 Configuration of input port

Selection of "With pull up resistor" with the mask option suits input from the push switch, key matrix, and so forth. When "Gate direct" is selected, the port can be used for slide switch input and interfacing with other LSIs.

4.5.2 Interrupt function

All eight bits of the input ports (K00–K03, K10–K13) provide the interrupt function. The conditions for issuing an interrupt can be set by the software. Further, whether to mask the interrupt function can be selected by the software.
Figure 4.5.2.1 shows the configuration of K00–K03 (K10–K13) interrupt circuit.

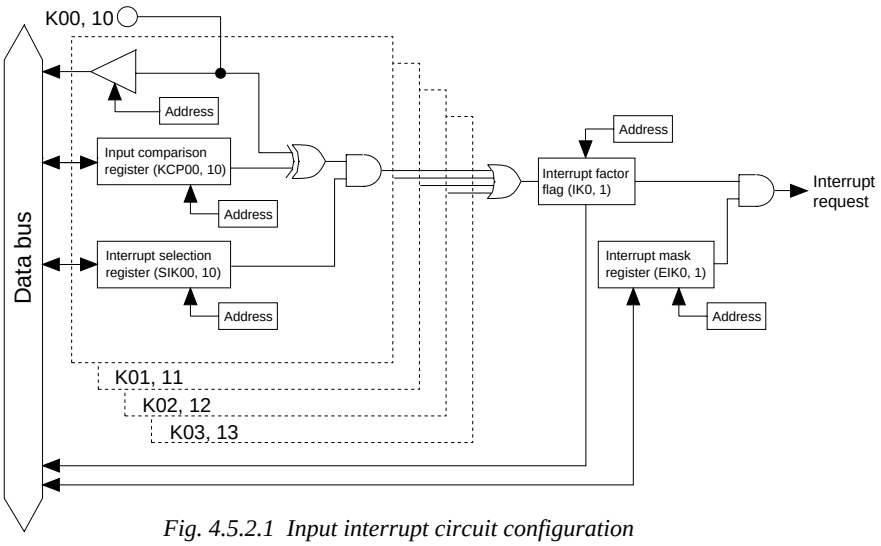


Fig. 4.5.2.1 Input interrupt circuit configuration

The interrupt selection register (SIK) and input comparison register (KCP) are individually set for the input ports K00–K03 and K10–K13, and can specify the terminal for generating interrupt and interrupt timing.
The interrupt selection registers (SIK00–SIK03, SIK10–SIK13) select what input of K00–K03 and K10–K13 to use for the interrupt. Writing "1" into an interrupt selection register incorporates that input port into the interrupt generation conditions. The changing the input port where the interrupt selection register has been set to "0" does not affect the generation of the interrupt.
The input interrupt timing can select that the interrupt be generated at the rising edge of the input or that it be generated at the falling edge according to the set value of the input comparison registers (KCP00–KCP03, KCP10–KCP13).

By setting these two conditions, the interrupt for K00–K03 or K10–K13 is generated when an input port in which an interrupt has been enabled by the input selection register and the content of the input comparison register have been changed from matching to no matching.
The interrupt mask registers (EIK0, EIK1) enable the interrupt mask to be selected for K00–K03 and K10–K13.
When the interrupt is generated, the interrupt factor flag (IK0, IK1) is set to "1".
Figure 4.5.2.2 shows an example of an interrupt for K00–K03.

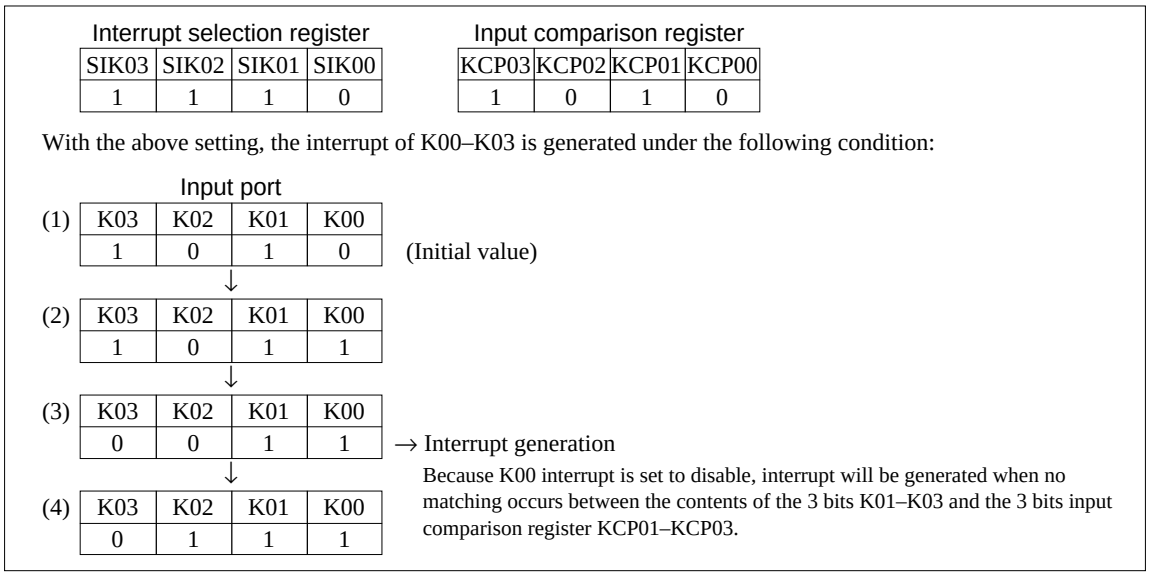


Fig. 4.5.2.2 Example of interrupt of K00–K03

K00 interrupt is disabled by the interrupt selection register (SIK00), so that an interrupt does not occur at (2). At (3), K03 changes to "0"; the data of the terminal that is interrupt enabled no longer matches the data of the input comparison register, so that interrupt occurs. As already explained, the condition for the interrupt to occur is the change in the port data and contents of the input comparison register from matching to no matching. Hence, in (4), when the no matching status changes to another no matching status, an interrupt does not occur. Further, terminals that have been masked for interrupt do not affect the conditions for interrupt generation.

4.5.3 Mask option

Internal pull up resistor can be selected for each of the eight bits of the input ports (K00–K03, K10–K13) with the input port mask option.
When you have selected "Gate direct", take care that the floating status does not occur for the input. Select "With pull up resistor" for input ports that are not being used.

4.5.4 Control of input ports

Table 4.5.4.1 lists the input ports control bits and their addresses.

Table 4.5.4.1 Input port control bits

Address *7	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
90H	SIK03	SIK02	SIK01	SIK00	SIK03	0	Enable	Disable	K00–K03 interrupt selection register
					SIK02	0	Enable	Disable	
	R/W				SIK01	0	Enable	Disable	
					SIK00	0	Enable	Disable	
91H	K03	K02	K01	K00	K03	– *2	High	Low	K00–K03 input port data
					K02	– *2	High	Low	
	R				K01	– *2	High	Low	
					K00	– *2	High	Low	
92H	KCP03	KCP02	KCP01	KCP00	KCP03	1	↓	↑	K00–K03 input comparison register
					KCP02	1	↓	↑	
	R/W				KCP01	1	↓	↑	
					KCP00	1	↓	↑	
94H	SIK13	SIK12	SIK11	SIK10	SIK13	0	Enable	Disable	K10–K13 interrupt selection register
					SIK12	0	Enable	Disable	
	R/W				SIK11	0	Enable	Disable	
					SIK10	0	Enable	Disable	
95H	K13	K12	K11	K10	K13	– *2	High	Low	K10–K13 input port data
					K12	– *2	High	Low	
	R				K11	– *2	High	Low	
					K10	– *2	High	Low	
96H	KCP13	KCP12	KCP11	KCP10	KCP13	1	↓	↑	K10–K13 input comparison register
					KCP12	1	↓	↑	
	R/W				KCP11	1	↓	↑	
					KCP10	1	↓	↑	
F2H	0	0	0	EIK1	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R			R/W	0 *5	– *2			Unused
					EIK1	0	Enable	Mask	Interrupt mask register (K10–K13)
F3H	0	0	0	EIK0	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R			R/W	0 *5	– *2			Unused
					EIK0	0	Enable	Mask	Interrupt mask register (K00–K03)
FAH	0	0	0	IK1	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R				0 *5	– *2			Unused
					IK1 *4	0	Yes	No	Interrupt factor flag (K10–K13)
FBH	0	0	0	IK0	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R				0 *5	– *2			Unused
					IK0 *4	0	Yes	No	Interrupt factor flag (K00–K03)

*1 Initial value at the time of initial reset
*2 Not set in the circuit
*3 Undefined
*4 Reset (0) immediately after being read
*5 Constantly "0" when being read
*6 Refer to main manual
*7 I/O memory is allocated from page 0 to 3

K00–K03, K10–K13: Input port data (91H, 95H)

Input data of the input port terminals can be read with these registers.

When "1" is read:	High level
When "0" is read:	Low level
Writing:	Invalid

The reading is "1" when the terminal voltage of the eight bits of the input ports (K00–K03, K10–K13) goes high (V_{DD}), and "0" when the voltage goes low (V_{SS}).
These bits are dedicated for reading, so writing cannot be done.

KCP00–KCP03, KCP10–KCP13: Input comparison registers (92H, 96H)

Interrupt conditions for terminals K00–K03 and K10–K13 can be set with these registers.

When "1" is written:	Falling edge
When "0" is written:	Rising edge
Reading:	Valid

The interrupt conditions can be set for the rising or falling edge of input for each of the eight bits (K00–K03 and K10–K13), through the input comparison registers (KCP00–KCP03 and KCP10–KCP13).
For KCP00–KCP03, a comparison is done only with the ports that are enabled by the interrupt among K00–K03 by means of the SIK00–SIK03 registers. For KCP10–KCP13, a comparison is done only with the ports that are enabled by the interrupt among K10–K13 by means of the SIK10–SIK13 registers.
At initial reset, these registers are set to "0".

SIK00–SIK03, SIK10–SIK13: Interrupt selection registers (90H, 94H)

Selects the port to be used for the K00–K03 and K10–K13 input interrupts.

When "1" is written:	Enable
When "0" is written:	Disable
Reading:	Valid

Enables the interrupt for the input ports (K00–K03, K10–K13) for which "1" has been written into the interrupt selection registers (SIK00–SIK03, SIK10–SIK13). The input port set for "0" does not affect the interrupt generation condition.
At initial reset, these registers are set to "0".

EIK0, EIK1: Interrupt mask registers (F3H•D0, F2H•D0)

Masking the interrupt of the input port can be selected with these registers.

When "1" is written:	Enable
When "0" is written:	Mask
Reading:	Valid

With these registers, masking of the input port can be selected for each of the two systems (K00–K03, K10–K13).
Writing to the interrupt mask registers can be done only in the DI status (interrupt flag = "0").
At initial reset, these registers are all set to "0".

IK0, IK1: Interrupt factor flags (FBH•D0, FAH•D0)

These flags indicate the occurrence of input interrupt.

When "1" is read:	Interrupt has occurred
When "0" is read:	Interrupt has not occurred
Writing:	Invalid

The interrupt factor flags IK0 and IK1 are associated with K00–K03 and K10–K13, respectively. From the status of these flags, the software can decide whether an input interrupt has occurred.
Reading of interrupt factor flags is available at EI, but be careful in the following cases.
If the interrupt mask register value corresponding to the interrupt factor flags to be read is set to "1", an interrupt request will be generated by the interrupt factor flags set timing, or an interrupt request will not be generated.
These flags are reset when the software reads them.
At initial reset, these flags are set to "0".

4.5.5 Programming notes

(1) When input ports are changed from low to high by pull up resistor, the rise of the waveform is delayed on account of the time constant of the pull up resistor and input gate capacitance. Hence, when fetching input ports, set an appropriate wait time.
Particular care needs to be taken of the key scan during key matrix configuration.
Make this waiting time the amount of time or more calculated by the following expression.
$10 \times C \times R$
C: terminal capacitance 5 pF + parasitic capacitance ? pF
R: pull up resistance 300 kΩ

(2) The K02 terminal functions as the clock input terminal for the programmable timer, and the input signal is combined with the input port and the programmable timer. Consequently, when the K02 terminal is set to the clock input terminal for the programmable timer, take care of the interrupt setting.

(3) Reading of interrupt factor flags is available at EI, but be careful in the following cases.
If the interrupt mask register value corresponding to the interrupt factor flags to be read is set to "1", an interrupt request will be generated by the interrupt factor flags set timing, or an interrupt request will not be generated.

(4) Write the interrupt mask register (EIK) only in the DI status (interrupt flag = "0"). Writing during EI status (interrupt flag = "1") will cause malfunction.

4.6 Output Ports *(R00–R03, R10–R13, R20–R23, R30–R33 and R40–R43)*

4.6.1 Configuration of output ports

The E0C6247 has 20 bits general output ports.
Output specifications of the output ports can be selected individually with the mask option. Two kinds of output specifications are available: complementary output and Nch open drain output.
Further, each of the output port to be used as special output ports by the software setting.
Figure 4.6.1.1 shows the configuration of the output port.

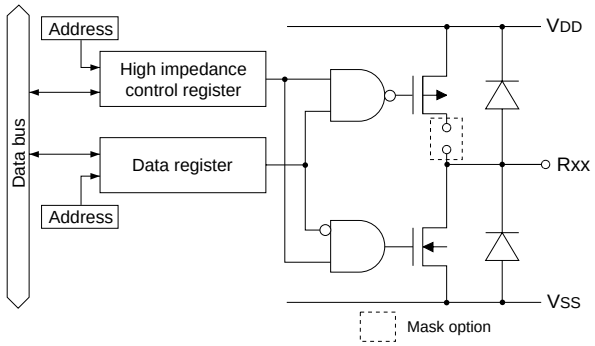


Fig. 4.6.1.1 Configuration of output port

20-bit output terminals are shared with bus signal output terminals for external memory accessing and buzzer signal output terminals and these functions are selected by the software. At initial reset, these are all set to the general purpose output port.
Table 4.6.1.1 shows the setting of the output terminals by function selection.

Table 4.6.1.1 Function setting of output terminals

Terminal name	Terminal status at initial reset	When external memory is used *1				Buzzer *2	
		1M-bit	512K-bit	256K-bit	64K-bit	$\overline{BZ}$	BZ
R00–R03	R00–R03 (HIGH output)	A00–A03	A00–A03	A00–A03	A00–A03		
R10–R13	R10–R13 (HIGH output)	A04–A07	A04–A07	A04–A07	A04–A07		
R20–R23	R20–R23 (HIGH output)	A08–A11	A08–A11	A08–A11	A08–A11		
R30	R30 (HIGH output)	A12	A12	A12	A12		
R31	R31 (HIGH output)	A13	A13	A13	R31		
R32	R32 (HIGH output)	A14	A14	A14	R32		
R33	R33 (HIGH output)	A15	A15	R33	R33		
R40	R40 (HIGH output)	A16	$\overline{WR}$	$\overline{WR}$	$\overline{WR}$		
R41	R41 (HIGH output)	$\overline{RD}$	$\overline{RD}$	$\overline{RD}$	$\overline{RD}$		
R42	R42 (LOW output)					$\overline{BZ}$	
R43	R43 (LOW output)						BZ

*1: EXTMF = "1" (external memory access function is ON), memory size is selected by MEMS1 and MEMS0.
*2: SELR42 = "1" ($\overline{BZ}$ output is selected), SELR43 = "1" (BZ output is selected)

The data registers and high impedance control registers of output ports set for bus signal output and the data registers of output port set for buzzer signal output can be used as general purpose registers that do not affect the outputs.
See Section 4.13, "External Memory Access", for control of external bus signals and see Section 4.12, "Sound Generator", for control of buzzer signals.

4.6.2 Mask option

Output specifications of the output ports can be selected with the mask option.
Output specifications for the output ports R00–R03, R10–R13 and R20–R23 enable selection of either complementary output or Nch open drain output for each of the four bits, and for the output ports R30–R33 and R40–R43, it can be done in a bit unit.
However, even when Nch open drain output is selected, voltage exceeding source voltage must not be applied to the output port.
This mask option is effective even when the output ports are used for outputs of external bus signals or for buzzer signal outputs.

4.6.3 High impedance control

The terminal output status of output ports may be set in high impedance status. This control is done using the high impedance control registers.
The following high impedance control registers are provided corresponding to the output ports.

High impedance control register	Corresponding output port
R0HIZ	R00–R03 (4-bit)
R1HIZ	R10–R13 (4-bit)
R2HIZ	R20–R23 (4-bit)
R30HIZ	R30 (1-bit)
R31HIZ	R31 (1-bit)
R32HIZ	R32 (1-bit)
R33HIZ	R33 (1-bit)
R40HIZ	R40 (1-bit)
R41HIZ	R41 (1-bit)
R42HIZ	R42 (1-bit)
R43HIZ	R43 (1-bit)

When "1" is written into the high impedance control register, the corresponding output port terminal goes into high impedance status. When "0" is written, output is performed according to the data register.

Since the exclusive registers are provided for high impedance control for external bus, the high impedance control registers of the outputs that are set for external bus signal output can be used as general purpose registers that do not affect the outputs.

4.6.4 Control of output ports

Table 4.6.4.1 lists the output ports' control bits and their addresses.

Table 4.6.4.1 Control bits of output ports

Address *7	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
98H	EXTMF	0	MEMS1	MEMS0	EXTMF	0	On	Off	External memory access function control
					0 *5	– *2			Unused
					MEMS1	0			External memory size selection (MEMS [1][0]: 1 1 1M (R only) (A00–A16); 1 0 512K (R/W) (A00–A15); 0 1 256K (R/W) (A00–A14); 0 0 64K (R/W) (A00–A12)
	R/W	R	R/W		MEMS0	0			
A0H	0	0	0	R0HIZ	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R			R/W	0 *5	– *2			Unused
					R0HIZ	0	High-Z	Output	R0 output high-impedance control (EXTMF = 0)
A1H	R03	R02	R01	R00	R03	1	High	Low	R00–R03 output port data (EXTMF = 0)
					R02	1	High	Low	
	R/W				R01	1	High	Low	
					R00	1	High	Low	
A2H	0	0	0	R1HIZ	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R			R/W	0 *5	– *2			Unused
					R1HIZ	0	High-Z	Output	R1 output high-impedance control (EXTMF = 0)
A3H	R13	R12	R11	R10	R13	1	High	Low	R10–R13 output port data (EXTMF = 0)
					R12	1	High	Low	
	R/W				R11	1	High	Low	
					R10	1	High	Low	
A4H	0	0	0	R2HIZ	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R			R/W	0 *5	– *2			Unused
					R2HIZ	0	High-Z	Output	R2 output high-impedance control (EXTMF = 0)
A5H	R23	R22	R21	R20	R23	1	High	Low	R20–R23 output port data (EXTMF = 0)
					R22	1	High	Low	
	R/W				R21	1	High	Low	
					R20	1	High	Low	
A6H	R33HIZ	R32HIZ	R31HIZ	R30HIZ	R33HIZ	0	High-Z	Output	R30–R33 output high-impedance control
					R32HIZ	0	High-Z	Output	
	R/W				R31HIZ	0	High-Z	Output	
					R30HIZ	0	High-Z	Output	
A7H	R33	R32	R31	R30	R33	1	High	Low	R30–R33 output port data
					R32	1	High	Low	
	R/W				R31	1	High	Low	
					R30	1	High	Low	
A8H	R43HIZ	R42HIZ	R41HIZ	R40HIZ	R43HIZ	0	High-Z	Output	R43 output high-impedance control
					R42HIZ	0	High-Z	Output	R42 output high-impedance control
					R41HIZ	0	High-Z	Output	R41 output high-impedance control (EXTMF = 0)
	R/W								(General-purpose register when EXTMF = 1)
					R40HIZ	0	High-Z	Output	R40 output high-impedance control (EXTMF = 0)
									(General-purpose register when EXTMF = 1)
A9H	R43	R42	R41	R40	R43	0	High	Low	R43 output port data (SELR43 = 0)
									(General-purpose register when BZ output is selected)
					R42	0	High	Low	R42 output port data (SELR42 = 0)
									(General-purpose register when $\overline{BZ}$ output is selected)
	R/W				R41	1	High	Low	R41 output port data (EXTMF = 0)
									(General-purpose register when EXTMF = 1)
					R40	1	High	Low	R40 output port data (EXTMF = 0)
									(General-purpose register when EXTMF = 1)
AAH	SELR43	SELR42	0	0	SELR43	0	BZ	Normal	R43 function selection register (BZ or general-purpose output)
					SELR42	0	$\overline{BZ}$	Normal	R42 function selection register ($\overline{BZ}$ or general-purpose output)
	R/W		R		0 *5	– *2			Unused
					0 *5	– *2			Unused

*1 Initial value at the time of initial reset
*2 Not set in the circuit
*3 Undefined
*4 Reset (0) immediately after being read
*5 Constantly "0" when being read
*6 Refer to main manual
*7 I/O memory is allocated from page 0 to 3

EXTMF: External memory access function control (98H•D3)

Controls the external memory access function ON or OFF.

When "1" is written: ON
When "0" is written: OFF
Reading: Valid

By writing "1" to EXTMF, the external memory access function goes ON, and the output ports R00–R03, R10–R13, R20–R23, R30–R33, R40 and R41 are set as external signal outputs according to the contents of the registers MEMS1 and MEMS0. When EXTMF is "0", the external memory access function is OFF and all the ports above can be used as general purpose output ports.
At initial reset, this register is set to "0".

MEMS1, MEMS0: External memory size selection (98H•D1, D0)

Selects size of the external address bus.
The configuration of the output ports R00–R03, R10–R13, R20–R23, R30–R33, R40 and R41 is decided by this setting.

Table 4.6.4.2 External memory size and usable output port

MEMS1	MEMS0	Memory size (bit)	Usable output port
1	1	1M (R only)	None
1	0	512K (R/W)	None
0	1	256K (R/W)	R33
0	0	64K (R/W)	R31, R32, R33

(R42 and R43 are not included in above setting.)
This setting is valid when EXTMF is "1".
At initial reset, this register is set to "0".

SELR42: R42 function selection register (AAH•D2)

Selects the output function for R42.

When "1" is written: $\overline{BZ}$ output
When "0" is written: General purpose output
Reading: Valid

When setting R42 to $\overline{BZ}$ (buzzer inverted signal) output, write "1" to this register and when R42 is used as general purpose output port, write "0".
See Section 4.12, "Sound Generator", for control of $\overline{BZ}$ output.
At initial reset, this register is set to "0".

SELR43: R43 function selection register (AAH•D3)

Selects the output function for R43.

When "1" is written: BZ output
When "0" is written: General purpose output
Reading: Valid

When setting R43 to BZ (buzzer signal) output, write "1" to this register and when R43 is used as general purpose output port, write "0".
See Section 4.12, "Sound Generator", for control of BZ output.
At initial reset, this register is set to "0".

R0HIZ, R1HIZ, R2HIZ, R30HIZ–R33HIZ, R40HIZ–R43HIZ: High impedance control registers (A0H•D0, A2H•D0, A4H•D0, A6H, A8H)

Controls high impedance output of the output port.

When "1" is written: High impedance
When "0" is written: Data output
Reading: Valid

By writing "0" into the high impedance control register, the corresponding output terminal outputs according to the data register. When "1" is written, it shifts to high impedance status.
The high impedance control registers of output ports set for bus signal output when the external memory access function is used (EXTMF = "1") can be used as general purpose registers that do not affect to the outputs.
At initial reset, these registers are set to "0".

R00–R03, R10–R13, R20–R23, R30–R33, R40–R43: Output port data (A1H, A3H, A5H, A7H, A9H)

Sets the output data for the output ports.

When "1" is written:	High output
When "0" is written:	Low output
Reading:	Valid

The output port terminals output the data written in the corresponding data registers without changing it. When "1" is written in the register, the output port terminal goes high (V_{DD}), and when "0" is written, the output port terminal goes low (V_{SS}).
The data registers of output ports set for bus signal output when the external memory access function is used (EXTMF = "1") and the data registers of output ports set for buzzer signal output can be used as general purpose registers that do not affect the outputs.
At initial reset, these registers are set to "0".

4.7 I/O Ports *(P00–P03, P10–P13, P20–P23, P30–P33 and P40–P43)*

4.7.1 Configuration of I/O ports

The E0C6247 has 20 bits general-purpose I/O ports. Figure 4.7.1.1 shows the configuration of the I/O port.

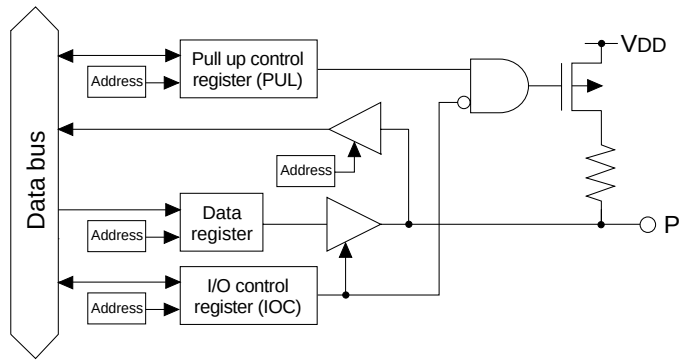


Fig. 4.7.1.1 Configuration of I/O port

20-bit I/O port terminals are shared with bus signal input/output terminals for external memory accessing, special output (CL, FR, PTOVF and FOUT) terminals and serial interface input/output terminals and these functions are selected by the software. At initial reset, these are all set to the I/O port.
Table 4.7.1.1 shows the setting of the input/output terminals by function selection.

Table 4.7.1.1 Function setting of input/output terminals

Terminal name	Terminal status at initial reset	When external memory is used *1				Special output *2				Serial interface *3		
		1M-bit	512K-bit	256K-bit	64K-bit	CL	FR	PTOVF	FOUT	Master	Slave	Async.
P00–P03	P00–P03 (Input & pull up)	D00–D03	D00–D03	D00–D03	D00–D03							
P10–P13	P10–P13 (Input & pull up)	D04–D07	D04–D07	D04–D07	D04–D07							
P20–P23	P20–P23 (Input & pull up)	$\overline{CS0}$–$\overline{CS3}$	$\overline{CS0}$–$\overline{CS3}$	$\overline{CS0}$–$\overline{CS3}$	$\overline{CS0}$–$\overline{CS3}$							
P30	P30 (Input & pull up)					CL						
P31	P31 (Input & pull up)						FR					
P32	P32 (Input & pull up)							PTOVF				
P33	P33 (Input & pull up)								FOUT			
P40	P40 (Input & pull up)									SIN(I)	SIN(I)	SIN(I)
P41	P41 (Input & pull up)									SOUT(O)	SOUT(O)	SOUT(O)
P42	P42 (Input & pull up)									$\overline{SCLK}$(O)	$\overline{SCLK}$(I)	P42
P43	P43 (Input & pull up)									P43	$\overline{SRDY}$(O)	P43

*1: EXTMF = "1" (external memory access function is ON)
*2: SELP30 = "1" (CL Output), SELP31 = "1" (FR output), SELP32 = "1" (PTOVF output), SELP33 = "1" (FOUT output)
*3: EISF = "1", Master: Clock synchronous master mode, Slave: Clock synchronous slave mode, Async.: Asynchronous mode

When these ports are used as I/O ports, each ports can be set to either input mode or output mode in a bit unit. Modes can be set by writing data to the I/O control register. Moreover, pull up resistor which is turned ON during input mode can be controlled by the software (pull up control register).

When the external memory access function is used, the data registers of P00–P03 and P10–P13 are used as the registers for the external data bus, and the data registers of P20–P23 are used to control the chip select signal outputs. The I/O control registers and pull up control registers of these ports can be used as general purpose registers.
The data registers, I/O control registers and pull up control registers of the I/O ports that are set in special outputs or input/output for the serial interface can be used as general purpose registers.
However, the pull up control registers of the port set as input for the serial interface (SIN, $\overline{SCLK}$ in the slave mode) functions as is.
See Section 4.13, "External Memory Access", for control of the input/output signals for the external bus, and see Section 4.11, "Serial Interface", for control of the serial interface.

4.7.2 I/O control registers and input/output mode

Input or output mode can be set for the I/O ports by writing data into the corresponding I/O control registers IOCxx.

To set the input mode, "0" is written to the I/O control register. When an I/O port is set to input mode, it becomes high impedance status and works as an input port.
However, when the pull up explained in the following section has been set by software, the input line is pulled up only during this input mode.

The output mode is set when "1" is written to the I/O control register. When an I/O port set to output mode works as an output port, it outputs a high level (V_{DD}) when the port output data is "1", and a low level (V_{SS}) when the port output data is "0".

If perform the read out in each mode; when output mode, the register value is read out, and when input mode, the port value is read out.

At initial reset, the I/O control registers are set to "0", and the I/O port enters the input mode.

The I/O control registers of the ports that are set as input/output for external bus signals, special output or input/output for the serial interface can be used as general purpose registers that do not affect to the I/O control. (See Table 4.7.1.1.)

4.7.3 Pull up during input mode

A pull up resistor that operates during the input mode is built into the I/O ports of the E0C6247. Software can set the use or non-use of this pull up. The pull up resistor becomes effective by writing "1" into the pull up control registers PULxx that correspond to each port, and the input line is pulled up during the input mode. When "0" has been written, no pull up is done.
At initial reset, the pull up control registers are set to "0".
The pull up control registers of the ports that are set as input/output for external bus signals, special output or output for the serial interface can be used as general purpose registers that do not affect to the pull up control. (See Table 4.7.1.1.)
The pull up control registers of the port set as input for the serial interface functions as is.

4.7.4 Mask option

For output specifications during the output mode (IOC = "1"), either complementary output or Nch open drain output can be selected with the mask option. Setting for P00–P03, P10–P13, P20–P23 and P40–P43 can be done in each terminal group (4-bit unit). Setting for P30–P33 can be done in 1-bit unit.
However, even when Nch open drain output is selected, voltage exceeding source voltage must not be applied to the I/O port.
This option is effective even when I/O ports are used for input/output of external bus signal, special output or input/output of the serial interface.

4.7.5 Special outputs (CL, FR, PTOVF, FOUT)

The I/O ports P30–P33 can be used as special output ports by switching the function with software. Since P30–P33 are set to I/O port (input mode with pull up) at initial reset, when special outputs are used, select the required special output function using the function selection registers shown in Table 4.7.5.1.
The data registers, I/O control registers and pull up control registers of the ports set in special output can be used as general purpose registers that do not affect the output.

Table 4.7.5.1 Special output selection

Terminal name	Function selection register	Setting of function selection register	
		"1"	"0"
P30	SELP30	CL output port	I/O port
P31	SELP31	FR output port	I/O port
P32	SELP32	PTOVF output port	I/O port
P33	SELP33	FOUT output port	I/O port

• CL, FR output (P30, P31)

When "1" is written to SELP30, P30 is set as the CL output port and when "1" is written to SELP31, P31 is set as the FR output port.
The CL and FR signals are LCD synchronous signal (CL) and LCD flame signal (FR) for externally expanded LCD driver, and are output from the P30 terminal and P31 terminal when the functions are switched by SELP30 and SELP31, respectively.
The frequency of the CL signal is 1,024 Hz (when f_{OSC1} = 32.768 kHz. 1,200 Hz when f_{OSC1} = 38.4 kHz or 76.8 kHz. 1,000 Hz when f_{OSC1} = 50 kHz) when 1/16 duty is selected, or 512 Hz (when f_{OSC1} = 32.768 kHz. 600 Hz when f_{OSC1} = 38.4 kHz or 76.8 kHz. 500 Hz when f_{OSC1} = 50 kHz) when 1/8 duty is selected. The frequency of the FR signal is 32 Hz (when f_{OSC1} = 32.768 kHz. 37.5 Hz when f_{OSC1} = 38.4 kHz or 76.8 kHz. 31.25 Hz when f_{OSC1} = 50 kHz).
See Section 4.8, "LCD Driver", for control of the LCD drive duty.

Note: A hazard may occur when the CL signal or FR signal is turned ON or OFF (when the port function is switched).

Figure 4.7.5.1 shows the output waveforms of CL and FR signals.

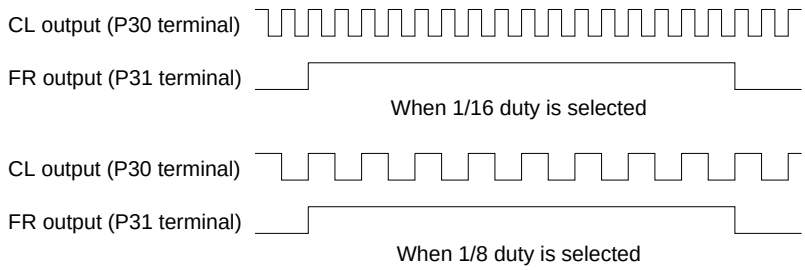


Fig. 4.7.5.1 Output waveforms of CL and FR signals

• PTOVF (P32)

When "1" is written to SELP32, R32 is set to the PTOVF output port.
The PTOVF signal is clock that is output from the programmable timer, and can be used to provide a clock signal to an external device.
The PTOVF signal is controlled using the PTOE register. When "1" is written to PTOE, the PTOVF signal is output from the P32 terminal and when "0" is written, a high (V_{DD}) level is output.
See Section 4.10, "Programmable Timer" for details of the programmable timer.

Note: A hazard may occur when the PTOVF signal is turned ON or OFF.

Figure 4.7.5.2 shows the output waveform of the PTOVF signal.

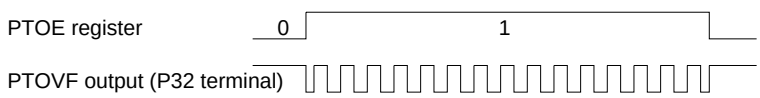


Fig. 4.7.5.2 Output waveform of PTOVF signal

• FOUT (P33)

When "1" is written to SELP33, R33 is set to the FOUT output port.
FOUT is the signal divided from the internal oscillation clock, and can be used to provide a clock signal to an external device.
The FOUT signal is controlled using the FOUTE register. When "1" is written to FOUTE, the FOUT signal is output from the P33 terminal and when "0" is written, a high (V_{DD}) level is output.
The frequency of the clock output signal may be selected from among 4 types shown in Table 4.7.5.2 by setting of the FOFQ1 and FOFQ0 registers.

Table 4.7.5.2 FOUT clock frequency

FOFQ1	FOFQ0	Clock frequency
1	1	f_{OSC3}
1	0	f_{OSC1}
0	1	f_{OSC1} / 8 (f_{OSC1} / 16 *)
0	0	f_{OSC1} / 16 (f_{OSC1} / 128 *)

* When f_{OSC1} = 76.8 kHz

When f_{OSC3} is selected, it is necessary to turn the OSC3 oscillation ON before output.

Note: A hazard may occur when the FOUT signal is turned ON or OFF.

Figure 4.7.5.3 shows the output waveform of FOUT signal.

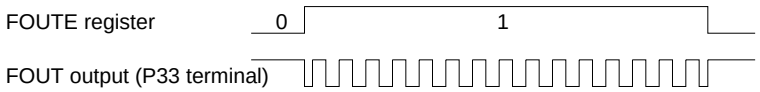


Fig. 4.7.5.3 Output waveform of FOUT signal

4.7.6 Control of I/O ports

Tables 4.7.6.1(a)–(c) list the I/O ports' control bits and their addresses.

Table 4.7.6.1(a) Control bits of I/O ports

Address *7	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
B0H	IOC03	IOC02	IOC01	IOC00	IOC03	0	Output	Input	P00–P03 I/O control register (EXTMF = 0) Functions as a general-purpose register when EXTMF = 1.
					IOC02	0	Output	Input	
	R/W				IOC01	0	Output	Input	
					IOC00	0	Output	Input	
B1H	PUL03	PUL02	PUL01	PUL00	PUL03	1	On	Off	P00–P03 pull up control register (EXTMF = 0) Functions as a general-purpose register when EXTMF = 1.
					PUL02	1	On	Off	
	R/W				PUL01	1	On	Off	
					PUL00	1	On	Off	
B2H	P03	P02	P01	P00	P03	– *2	High	Low	P00–P03 I/O port data (EXTMF = 0)
					P02	– *2	High	Low	
	D03	D02	D01	D00	P01	– *2	High	Low	
					P00	– *2	High	Low	
	R/W				D03	– *2	1	0	External memory data D00–D03 (EXTMF = 1)
					D02	– *2	1	0	
					D01	– *2	1	0	
					D00	– *2	1	0	
B4H	IOC13	IOC12	IOC11	IOC10	IOC13	0	Output	Input	P10–P13 I/O control register (EXTMF = 0) Functions as a general-purpose register when EXTMF = 1.
					IOC12	0	Output	Input	
	R/W				IOC11	0	Output	Input	
					IOC10	0	Output	Input	
B5H	PUL13	PUL12	PUL11	PUL10	PUL13	1	On	Off	P10–P13 pull up control register (EXTMF = 0) Functions as a general-purpose register when EXTMF = 1.
					PUL12	1	On	Off	
	R/W				PUL11	1	On	Off	
					PUL10	1	On	Off	
B6H	P13	P12	P11	P10	P13	– *2	High	Low	P10–P13 I/O port data (EXTMF = 0)
					P12	– *2	High	Low	
	D07	D06	D05	D04	P11	– *2	High	Low	
					P10	– *2	High	Low	
	R/W				D07	– *2	1	0	External memory data D04–D07 (EXTMF = 1)
					D06	– *2	1	0	
					D05	– *2	1	0	
					D04	– *2	1	0	
B8H	IOC23	IOC22	IOC21	IOC20	IOC23	0	Output	Input	P20–P23 I/O control register (EXTMF = 0) Functions as a general-purpose register when EXTMF = 1.
					IOC22	0	Output	Input	
	R/W				IOC21	0	Output	Input	
					IOC20	0	Output	Input	
B9H	PUL23	PUL22	PUL21	PUL20	PUL23	1	On	Off	P20–P23 pull up control register (EXTMF = 0) Functions as a general-purpose register when EXTMF = 1.
					PUL22	1	On	Off	
	R/W				PUL21	1	On	Off	
					PUL20	1	On	Off	
BAH	P23	P22	P21	P20	P23	– *2	High	Low	P20–P23 I/O port data (EXTMF = 0)
					P22	– *2	High	Low	
	CS3	CS2	CS1	CS0	P21	– *2	High	Low	
					P20	– *2	High	Low	
	R/W				CS3	– *2	Disable	Active	Chip select $\overline{CS0}$–$\overline{CS3}$ active standby (EXTMF = 1)
					CS2	– *2	Disable	Active	
					CS1	– *2	Disable	Active	
					CS0	– *2	Disable	Active	

*1 Initial value at the time of initial reset
*2 Not set in the circuit
*3 Undefined
*4 Reset (0) immediately after being read
*5 Constantly "0" when being read
*6 Refer to main manual
*7 I/O memory is allocated from page 0 to 3

Table 4.7.6.1(b) Control bits of I/O ports

Address *7	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
BCH	IOC33	IOC32	IOC31	IOC30	IOC33	0	Output	Input	P33 I/O control register (SELP33 = 0) (General-purpose register when FOUT output is selected)
					IOC32	0	Output	Input	P32 I/O control register (SELP32 = 0) (General-purpose register when PTOVF output is selected)
	R/W				IOC31	0	Output	Input	P31 I/O control register (SELP31 = 0) (General-purpose register when FR output is selected)
					IOC30	0	Output	Input	P30 I/O control register (SELP30 = 0) (General-purpose register when CL output is selected)
BDH	PUL33	PUL32	PUL31	PUL30	PUL33	1	On	Off	P33 pull up control register (SELP33 = 0) (General-purpose register when FOUT output is selected)
					PUL32	1	On	Off	P32 pull up control register (SELP32 = 0) (General-purpose register when PTOVF output is selected)
	R/W				PUL31	1	On	Off	P31 pull up control register (SELP31 = 0) (General-purpose register when FR output is selected)
					PUL30	1	On	Off	P30 pull up control register (SELP30 = 0) (General-purpose register when CL output is selected)
BEH	P33	P32	P31	P30	P33	– *2	High	Low	P33 I/O port data (SELP33 = 0) (General-purpose register when FOUT output is selected)
					P32	– *2	High	Low	P32 I/O port data (SELP32 = 0) (General-purpose register when PTOVF output is selected)
	R/W				P31	– *2	High	Low	P31 I/O port data (SELP31 = 0) (General-purpose register when FR output is selected)
					P30	– *2	High	Low	P30 I/O port data (SELP30 = 0) (General-purpose register when CL output is selected)
BFH	SELP33	SELP32	SELP31	SELP30	SELP33	0	FOUT	I/O	P33 function selection register (FOUT output or I/O)
					SELP32	0	PTOVF	I/O	P32 function selection register (PTOVF output or I/O)
	R/W				SELP31	0	FR	I/O	P31 function selection register (FR output or I/O)
					SELP30	0	CL	I/O	P30 function selection register (CL output or I/O)
C0H	IOC43	IOC42	IOC41	IOC40	IOC43	0	Output	Input	P43 I/O control register (General-purpose register when SI/F (sync. slave) is selected)
					IOC42	0	Output	Input	P42 I/O control register (General-purpose register when SI/F (sync.) is selected)
	R/W				IOC41	0	Output	Input	P41 I/O control register (ESIF = 0) (General-purpose register when SI/F is selected)
					IOC40	0	Output	Input	P40 I/O control register (ESIF = 0) (General-purpose register when SI/F is selected)
C1H	PUL43	PUL42	PUL41	PUL40	PUL43	1	On	Off	P43 pull up control register (General-purpose register when SI/F (sync. slave) is selected)
					PUL42	1	On	Off	P42 pull up control register (General-purpose register when SI/F (sync. master) is selected)
	R/W				PUL41	1	On	Off	P41 pull up control register (ESIF = 0) (General-purpose register when SI/F is selected)
					PUL40	1	On	Off	P40 pull up control register (ESIF = 0) SIN pull up control register (ESIF = 1)
C2H	P43	P42	P41	P40	P43	– *2	High	Low	P43 I/O port data (General-purpose register when SI/F (sync. slave) is selected)
					P42	– *2	High	Low	P42 I/O port data (General-purpose register when SI/F (sync.) is selected)
	R/W				P41	– *2	High	Low	P41 I/O port data (ESIF = 0) (General-purpose register when SI/F is selected)
					P40	– *2	High	Low	P40 I/O port data (ESIF = 0) (General-purpose register when SI/F is selected)

*1 Initial value at the time of initial reset
*2 Not set in the circuit
*3 Undefined
*4 Reset (0) immediately after being read
*5 Constantly "0" when being read
*6 Refer to main manual
*7 I/O memory is allocated from page 0 to 3

Table 4.7.6.1(c) Control bits of I/O ports

Address *7	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
8AH	FOUTE	0	FOFQ1	FOFQ0	FOUTE	0	Enable	Disable	FOUT output enable
					0 *5	– *2			Unused
					FOFQ1	0			FOUT frequency selection
					FOFQ0	0			FOUT frequency selection
	R/W	R	R/W						FOFQ[1][0] FOUT frequency: 1 1 fOSC3; 1 0 fOSC1; 0 1 fOSC1/8 (fOSC1/16); 0 0 fOSC1/64 (fOSC1/128) (In case of fOSC1 = 76.8 kHz)
98H	EXTMF	0	MEMS1	MEMS0	EXTMF	0	On	Off	External memory access function control
					0 *5	– *2			Unused
					MEMS1	0			External memory size selection
					MEMS0	0			External memory size selection
	R/W	R	R/W						MEMS[1][0] Size (bit): 1 1 1M (R only) (A00–A16); 1 0 512K (R/W) (A00–A15); 0 1 256K (R/W) (A00–A14); 0 0 64K (R/W) (A00–A12)
C8H	0	SMD1	SMD0	ESIF	0 *5	– *2			Unused
					SMD1	0			Serial I/F mode selection
					SMD0	0			Serial I/F mode selection
	R	R/W							SMD[1][0] Mode: 1 1 Asynchronous 8-bit; 1 0 Asynchronous 7-bit; 0 1 Clock synchronous slave; 0 0 Clock synchronous master
					ESIF	0	SI/F	I/O	Serial I/F enable (P4 port function selection)
EAH	PNRFS	PTOE	PTRUN	PTRST	PNRFS	0	1024 Hz	256 Hz	Noise rejector clock frequency selection
					PTOE	0	Enable	Disable	PTOVF output enable
					PTRUN	0	Run	Stop	Programmable timer Run/Stop
	R/W			W	PTRST *5	– *2	Rst (reload)	–	Programmable timer reset (reload)

*1 Initial value at the time of initial reset
*2 Not set in the circuit
*3 Undefined
*4 Reset (0) immediately after being read
*5 Constantly "0" when being read
*6 Refer to main manual
*7 I/O memory is allocated from page 0 to 3

(1) Function selection for ports

EXTMF: External memory access function control (98H•D3)

Controls the external memory access function ON or OFF.

When "1" is written: ON
When "0" is written: OFF
Reading: Valid

By writing "1" to EXTMF, the external memory access function goes ON, and the I/O ports P00–P03 and P10–P13 are set as external data bus, and P20–P23 are set as chip select ($\overline{CS0}$–$\overline{CS3}$) signal outputs. When EXTMF is "0", the external memory access function is OFF and all the ports above can be used as I/O ports.
At initial reset, this register is set to "0".

SELP30: P30 function selection register (BFH•D0)

Selects function for P30.

When "1" is written: CL output
When "0" is written: I/O port
Reading: Valid

When setting P30 to CL (LCD synchronous signal) output, write "1" to this register and when P30 is used as I/O port, write "0".
At initial reset, this register is set to "0".

SELP31: P31 function selection register (BFH•D1)

Selects function for P31.

When "1" is written: FR output
When "0" is written: I/O port
Reading: Valid

When setting P31 to FR (LCD frame signal) output, write "1" to this register and when P31 is used as I/O port, write "0".
At initial reset, this register is set to "0".

SELP32: P32 function selection register (BFH•D2)

Selects function for P32.

When "1" is written: PTOVF output
When "0" is written: I/O port
Reading: Valid

When setting P32 to PTOVF (clock output from the programmable timer) output, write "1" to this register and when P32 is used as I/O port, write "0".
At initial reset, this register is set to "0".

SELP33: P33 function selection register (BFH•D3)

Selects function for P33.

When "1" is written: FOUT output
When "0" is written: I/O port
Reading: Valid

When setting P33 to FOUT (clock) output, write "1" to this register and when P33 is used as I/O port, write "0".
At initial reset, this register is set to "0".

ESIF: Serial interface enable (C8H•D0)

Selects function for P40–P43.

When "1" is written: Serial interface input/output port
When "0" is written: I/O port
Reading: Valid

When the serial interface is used, write "1" to this register and when P40–P43 are used as I/O port, write "0". The configuration of the terminals within P40–P43 that are used for the serial interface is decided by the mode selected with the SMD1 and SMD0 registers.
At initial reset, this register is set to "0".

SMD1, SMD0: Serial interface mode selection (C8H•D2, D1)

Selects the transfer mode.
The configuration of the I/O ports P40–P43 is decided with this setting.

Table 4.7.6.2 Serial I/F mode and usable I/O port

SMD1	SMD0	Serial interface mode	Usable I/O port (P40–P43)
1	1	Asynchronous 8-bit	P42, P43
1	0	Asynchronous 7-bit	P42, P43
0	1	Clock synchronous slave	None
0	0	Clock synchronous master	P43

This setting is valid when ESIF is "1".
At initial reset, this register is set to "0".

(2) I/O port control

P00–P03, P10–P13, P20–P23, P30–P33, P40–P43: I/O port data (B2H, B6H, BAH, BEH, C2H)

I/O port data can be read and output data can be set through these registers.

- ***When writing data***

When "1" is written: High level
When "0" is written: Low level

When an I/O port is set to the output mode, the written data is output unchanged from the I/O port terminal. When "1" is written as the port data, the port terminal goes high (V_{DD}), and when "0" is written, the level goes low (V_{SS}).
Port data can be written also in the input mode.

• ***When reading data***

When "1" is read: High level
When "0" is read: Low level

The terminal voltage level of the I/O port is read out. When the I/O port is in the input mode the voltage level being input to the port terminal can be read out; in the output mode the register value can be read. When the terminal voltage is high (V_{DD}) the port data that can be read is "1", and when the terminal voltage is low (V_{SS}) the data is "0".
When PUL register is set to "1", the built-in pull up resister goes ON during input mode, so that the I/O port terminal is pulled up. Internal pull up registers are only ON during input mode, but the gate floating has not occur even during output mode.

When the special output or the serial input/output function is selected for P30–P33 or P40–P43 ports, the data registers can be used as general purpose register, and data of this register exerts no affect on input/output signal.

Note: When in the input mode, I/O ports are changed from low to high by pull up resistor, the rise of the waveform is delayed on account of the time constant of the pull up resistor and input gate capacitance. Hence, when fetching input ports, set an appropriate wait time.
Particular care needs to be taken of the key scan during key matrix configuration.
Make this waiting time the amount of time or more calculated by the following expression.
10 x C x R
C: terminal capacitance 5 pF + parasitic capacitance ? pF
R: pull up resistance 300 kΩ

IOC00–IOC03, IOC10–IOC13, IOC20–IOC23, IOC30–IOC33, IOC40–IOC43:
I/O control registers (B0H, B4H, B8H, BCH, C0H)

The input and output modes of the I/O ports can be set with these registers.

When "1" is written: Output mode
When "0" is written: Input mode
Reading: Valid

The input and output modes of the I/O ports are set in 1-bit unit.
Writing "1" to the I/O control register makes the corresponding I/O port enter the output mode, and writing "0" induces the input mode.
At initial reset, these registers are set to "0", so the I/O ports are in the input mode.
The I/O control registers of the ports that are set as input/output for external bus signals, special output or input/output for the serial interface can be used as general purpose registers that do not affect to the input/output.

PUL00–PUL03, PUL10–PUL13, PUL20–PUL23, PUL30–PUL33, PUL40–PUL43:
Pull up control registers (B1H, B5H, B9H, BDH, C1H)

The pull up during the input mode can be set with these registers.

When "1" is written: Pull up ON
When "0" is written: Pull up OFF
Reading: Valid

The built-in pull up resistor which is turned ON during input mode is set to enable in 1-bit unit.
By writing "1" to the pull up control register, the corresponding I/O ports are pulled up (during input mode), while writing "0" turns the pull up function OFF.
At initial reset, these registers are set to "0", so the pull up function is set to OFF.

The pull up control registers of the ports that are set as input/output for external bus signals, special output or output for the serial interface can be used as general purpose registers that do not affect to the pull up control.
The pull up control registers of the port set as input for the serial interface functions as is. (See Section 4.11, "Serial Interface".)

(3) Special output ontrol

PTOE: PTOVF output enable register (EAH•D2)
Controls the PTOVF output.

When "1" is written: PTOVF output enable
When "0" is written: PTOVF output disable
Reading: Valid

By writing "1" to PTOE when SELP32 is set to "1", PTOVF signal is output from the P32 terminal. When "0" is written, the P32 terminal goes to high (V_{DD}).
At initial reset, this register is set to "0".
See Section 4.10, "Programmable Timer", for details of the PTOVF signal.

FOUTE: FOUT output enable register (8AH•D3)
Controls the FOUT output.

When "1" is written: FOUT output enable
When "0" is written: FOUT output disable
Reading: Valid

By writing "1" to FOUTE when SELP33 is set to "1", FOUT signal is output from the P33 terminal. When "0" is written, the P33 terminal goes to high (V_{DD}).
At initial reset, this register is set to "0".

FOFQ1, FOFQ0: FOUT frequency selection registers (8AH•D1, D0)
Selects frequency of the FOUT signal.

Table 4.7.6.3 FOUT frequency setting

FOFQ1	FOFQ0	Clock frequency
1	1	f_{OSC3}
1	0	f_{OSC1}
0	1	f_{OSC1} / 8 (f_{OSC1} / 16 *)
0	0	f_{OSC1} / 16 (f_{OSC1} / 128 *)

* When f_{OSC1} = 76.8 kHz

At initial reset, these registers are set to "0"

4.7.7 Programming notes

(1) When in the input mode, I/O ports are changed from low to high by pull up resistor, the rise of the waveform is delayed on account of the time constant of the pull up resistor and input gate capacitance. Hence, when fetching input ports, set an appropriate wait time.
Particular care needs to be taken of the key scan during key matrix configuration.
Make this waiting time the amount of time or more calculated by the following expression.
$10 \times C \times R$
C: terminal capacitance 5 pF + parasitic capacitance ? pF
R: pull up resistance 300 kΩ

(2) When special output has been selected, a hazard may occur when the signal is turned ON or OFF.

(3) When f_{OSC3} is selected for the FOUT output clock, it is necessary to turn the OSC3 oscillation ON before output.

(4) When Nch open drain has been selected for the P10–P13 output specifications by the mask option and during output mode, read data from the P10–P13 registers (address B6H•D0–D3) may differ from the data written to them.

4.8 LCD Driver (COM0–COM15, SEG0–SEG63)

4.8.1 Configuration of LCD driver

The E0C6247 has 16 common terminals (COM0–COM15) and 64 segment terminals (SEG0–SEG63), so that it can drive a dot matrix type LCD with a maximum of 1024 (64 × 16) dots (12 characters × 2 lines when an 8 × 5 matrix LCD is used).
The driving method is 1/16 duty or 1/8 duty dynamic drive depending on the four types of potential (1/4 bias), V_{C1}, V_{C2}, V_{C4} and V_{C5} (1/5 bias driving may be set by impressing five potentials from outside). The frame frequency is 32 Hz when f_{OSC1} = 32.768 kHz (37.5 Hz when f_{OSC1} = 34.8 kHz or 76.8 kHz, 31.25 Hz when f_{OSC1} = 50 kHz).
LCD display ON/OFF may be controlled by the software.

4.8.2 Power supply for LCD driving

V_{C1}–V_{C5} are driving voltages for the LCD, and for which either the voltages generated by the LCD system voltage circuit or voltages to be supplied from outside can be used. The built-in LCD system voltage circuit generates four electric potentials (1/4 bias) for V_{C1}, V_{C2}, V_{C4} and V_{C5} except for V_{C3}. These four output voltages can be supplied to the outside only for the externally expanded LCD driver.
When external voltages are supplied, 1/5 bias driving can be made by inputting five electric potentials to the V_{C1}–V_{C5} terminals (including V_{C3}).
Either the internal generated voltages or external voltages used for the LCD drive voltage can be selected by the mask option.

Turning the LCD system voltage circuit ON or OFF is controlled with the LPWR register. This control is also necessary when supplying from outside. When LPWR is set to "1", the LCD system voltage circuit outputs the LCD drive voltages V_{C1}–V_{C5} to the LCD driver.

The LCD system voltage circuit generates V_{C1} or V_{C2} with the regulated voltage circuit incorporated in itself, and generates three other electric potentials by boosting or reducing the voltage of V_{C1} or V_{C2}. Table 4.8.2.1 shows the V_{C1}, V_{C2}, V_{C4} and V_{C5} voltage values and boost/reduce status.

Table 4.8.2.1 LCD drive voltage when generated internally

LCD drive voltage	V_{DD} = 0.9–3.6 V	V_{DD} = 2.6–3.6 V
V_{C1} (0.975–1.2 V)	V_{C1} (standard)	1/2 × V_{C2}
V_{C2} (1.950–2.4 V)	2 × V_{C1}	V_{C2} (standard)
V_{C4} (2.925–3.6 V)	3 × V_{C1}	3/2 × V_{C2}
V_{C5} (3.900–4.8 V)	4 × V_{C1}	2 × V_{C2}

Note: The LCD drive voltage can be adjusted by the software. Values in the above table are typical values.

Select either V_{C1} standard or V_{C2} standard using the register VCCHG.
When "1" is written to the VCCHG, V_{C2} standard is selected and when "0" is written, V_{C1} standard is selected. At initial reset, V_{C1} standard (VCCHG = "0") is set.

The operating mode setting according to the supply voltage and the V_{C1}/V_{C2} selection is necessary for the LCD system voltage circuit. See Section 4.2, "Setting of Power Supply and Operating Mode", for setting of the operating mode.

4.8.3 Mask option

Disconnecting the internal power supply for LCD driving will enable electric potentials to be supplied externally. In such case, the five electric potentials are entered in V_{C1}, V_{C2}, V_{C3}, V_{C4} and V_{C5} terminals and 1/5 bias driving may then be set. Since 1/5 bias driving provides better display quality, when low power current consumption is not required (i.e., when power is supplied from AC outlet), select external power mode. However, note that in order to maintain a stable display, power source must be one which will remain stable even when heavy load such as buzzer, etc. is driven.
Moreover, in the external power mode, the contrast adjustment function cannot be used. Accommodate this limitation by utilizing the external circuit as necessary.

A sample circuit of external power for LCD driving when power is supplied externally is shown in Figure 4.8.3.1.

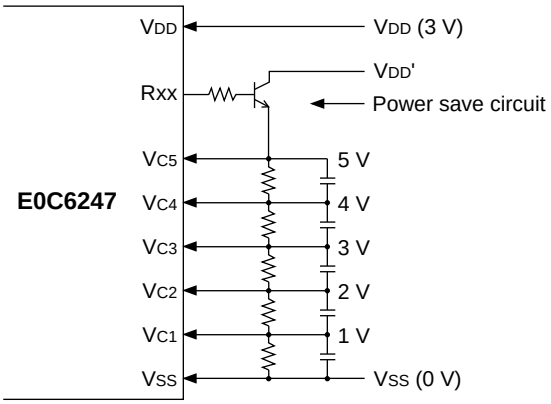


Fig. 4.8.3.1 Sample circuit of external power for LCD driving when power is supplied externally

4.8.4 LCD display control (ON/OFF) and switching of duty

(1) Display ON/OFF control

The E0C6247 incorporates the ALON and ALOFF registers to blink display. When "1" is written to ALON, all the dots go ON, and when "1" is written to ALOFF, all the dots go OFF. At such a time, an ON waveform or an OFF waveform is output from SEG terminals. When "0" is written to these registers, normal display is performed. Furthermore, when "1" is written to both of the ALON and ALOFF, ALON (all ON) has priority over the ALOFF (all OFF).

(2) Switching of drive duty

In the E0C6247, the drive duty can be set to 1/6 or 1/8 by the software. This setting is done using the register LDUTY as shown in Table 4.8.4.1.

Table 4.8.4.1 LCD drive duty setting

LDUTY	Duty	Common terminal used	Maximum segment number
1	1/8	COM0–COM7	512 (64 × 8)
0	1/16	COM0–COM15	1024 (64 × 16)

Figures 4.8.4.1 and 4.8.4.2 show the drive waveform for 1/4 bias and 1/5 bias.

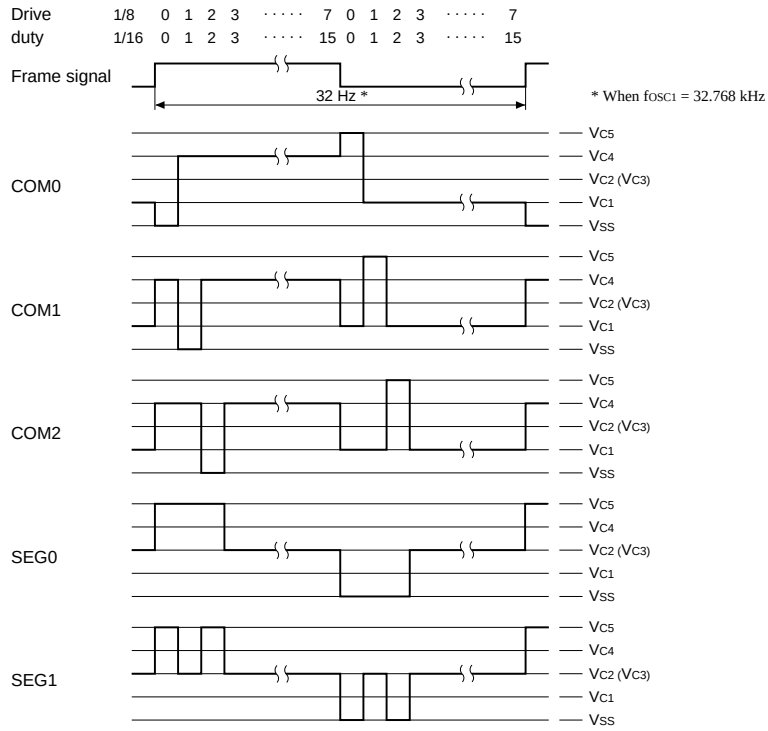


Fig. 4.8.4.1 Drive waveform for 1/4 bias

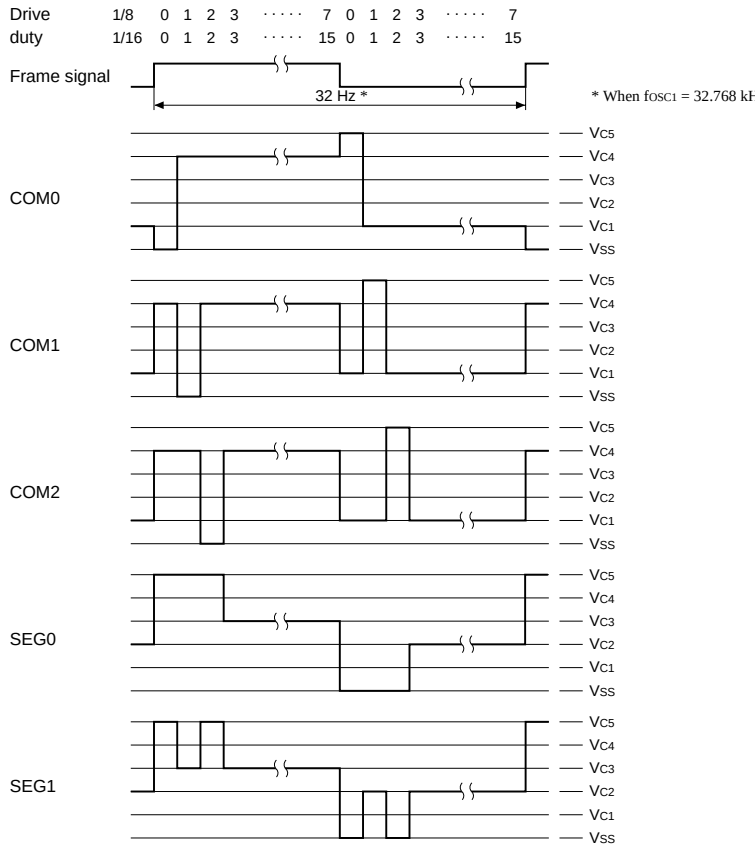


Fig. 4.8.4.2 Drive waveform for 1/5 bias

4.8.5 Display memory

The display memory is allocated to page 0AH (10) in the data memory area and the addresses and the data bits correspond to COM and SEG outputs as shown in Figure 4.8.5.1.

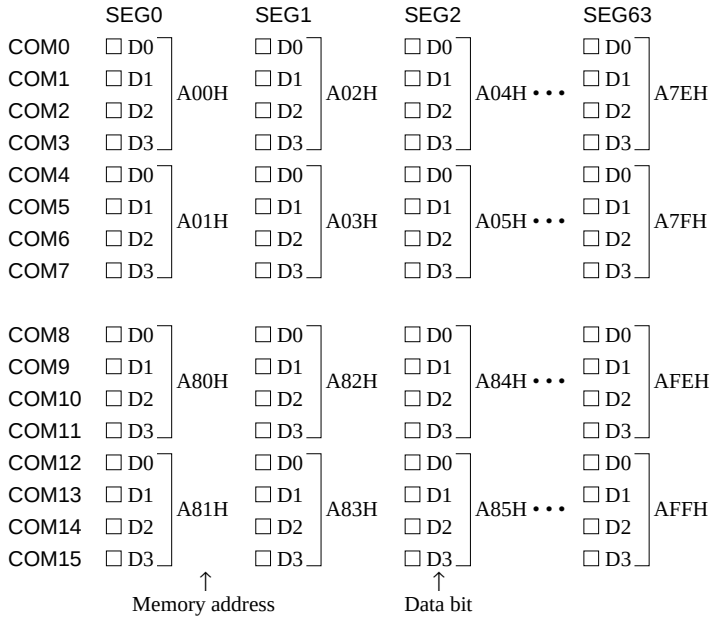


Fig. 4.8.5.1 Correspondence between display memory and LCD dot matrix

When the display memory bit is assigned as "1", the corresponding LCD dot goes ON, and when assigned as "0", the dot goes OFF.
At 1/16 duty drive, all data of COM0–COM15 is output.
At 1/8 duty drive, data only corresponding to COM0–COM7 is output.
At initial reset, the data memory content becomes undefined hence, there is need to initialize using the software.
The display memory has read/write capability, and the addresses that have not been used for LCD display can be used as general purpose registers.

4.8.6 LCD contrast adjustment

In the E0C6247, the LCD contrast can be adjusted by the software.
It is realized by controlling the voltages V_{C1}, V_{C2}, V_{C4} and V_{C5} output from the LCD system voltage circuit.When these voltages are supplied to the externally expanded LCD driver, the expanded LCD contrast is adjusted at the same time. However, when the LCD drive voltage is supplied from outside by the mask option selection, this adjustment becomes invalid.
The contrast can be adjusted to 16 levels as shown in Table 4.8.6.1. When VCCHG = "0", V_{C1} is changed within the range from 0.975 V to 1.2 V, and other voltages change according to V_{C1}. When VCCHG = "1", V_{C2} is changed within the range from 1.95 V to 2.4 V, and other voltages change according to V_{C2}.

At room temperature, use setting number 7 or 8 as standard.
Since the contents of LC0–LC3 are undefined at initial reset, initialize it by the software.

Table 4.8.6.1 LCD contrast

	LC3	LC2	LC1	LC0	Contrast
0	0	0	0	0	light
1	0	0	0	1	↑
2	0	0	1	0	
3	0	0	1	1	
4	0	1	0	0	
5	0	1	0	1	
6	0	1	1	0	
7	0	1	1	1	
8	1	0	0	0	
9	1	0	0	1	
A	1	0	1	0	
B	1	0	1	1	
C	1	1	0	0	
D	1	1	0	1	
E	1	1	1	0	↓
F	1	1	1	1	dark

4.8.7 Control of LCD driver

Table 4.8.7.1 shows the LCD driver's control bits and their addresses.

Table 4.8.7.1 LCD driver control bits

Address *7	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
D0H	LDUTY	VCCHG	0	LPWR	LDUTY	0	1/8	1/16	LCD drive duty switch
					VCCHG	0	V_{C2}	V_{C1}	LCD regulated voltage switch
	R/W				0 *5	– *2			Unused
					LPWR	0	On	Off	LCD power On/Off
D1H	0	ALOFF	ALON	0	0 *5	– *2			Unused
					ALOFF	1	AllOff	Normal	All LCD dots fade out control
	R	R/W		R	ALON	0	AllOn	Normal	All LCD dots displayed control
					0 *5	– *2			Unused
D2H	LC3	LC2	LC1	LC0	LC3	– *2			LCD contrast adjustment
					LC2	– *2			LC3–LC0 = 0 Light
	R/W				LC1	– *2			:
					LC0	– *2			LC3–LC0 = 15 Dark

*1 Initial value at the time of initial reset
*2 Not set in the circuit
*3 Undefined
*4 Reset (0) immediately after being read
*5 Constantly "0" when being read
*6 Refer to main manual
*7 I/O memory is allocated from page 0 to 3

LPWR: LCD power ON/OFF (D0H•D0)

Controls the LCD system voltage circuit ON/OFF.

When "1" is written: ON
When "0" is written: OFF
Reading: Valid

When "1" is written to LPWR, the LCD system voltage circuit goes ON and generates the LCD drive voltage. When "0" is written, all the LCD drive voltages go to V_{SS} level.
It takes about 100 msec for the LCD drive voltage to stabilize after starting up the LCD system voltage circuit by writing "1" to LPWR.
At initial reset, this register is set to "0".

VCCHG: LCD regulated voltage switching (D0H•D2)

Selects the reference voltage for the LCD drive voltage.

When "1" is written: V_{C2}
When "0" is written: V_{C1}
Reading: Valid

When "1" is written to VCCHG, the LCD system voltage circuit generates the LCD drive voltage as V_{D2} standard. When "0" is written into the VCCHG, it becomes V_{C1} standard. Select V_{C2} when supply voltage is 2.6 V or more, otherwise, select V_{C1}. Furthermore, it is necessary to switch the operating mode for the LCD system voltage circuit according to supply voltage. (See Section 4.2, "Setting of Power Supply and Operating Mode", for the operating mode. When external power mode is selected by the mask option, this control is unnecessary.
At initial reset, this register is set to "0".

LDUTY: LCD drive duty switch (D0H•D3)

Selects the LCD drive duty.

When "1" is written: 1/8 duty
When "0" is written: 1/16 duty
Reading: Valid

By writing "1" to LDUTY, 1/8 duty is set, and when "0" is written, 1/16 duty is set.
At initial reset, this register is set to "0".

ALON: LCD all ON control (D1H•D1)
Displays the all LCD dots ON.

When "1" is written: All LCD dots displayed
When "0" is written: Normal display
Reading: Valid

By writing "1" to ALON, all the LCD dots goes ON, and when "0" is written, it returns to normal display. All LCD displaying outputs an ON waveform to SEG, and does not affect the content of the display memory.
ALON has priority over ALOFF.
At initial reset, this register is set to "0".

ALOFF: LCD all OFF control (D1H•D2)
Fade outs the all LCD dots.

When "1" is written: All LCD dots fade out
When "0" is written: Normal display
Reading: Valid

By writing "1" to ALOFF, all the LCD dots goes OFF, and when "0" is written, it returns to normal display. All fading out of LCD outputs an OFF waveform to SEG, and does not affect the content of the display memory.
At initial reset, this register is set to "0".

LC3–LC0: LCD contrast adjustment (D2H)
Adjusts the LCD contrast.

LC3–LC0 = 0000B light
: :
LC3–LC0 = 1111B dark

At room temperature, use setting number 7 or 8 as standard.
When the LCD drive voltage is supplied from outside by the mask option selection, this adjustment becomes invalid.
At initial reset, LC0–LC3 are undefined.

4.8.8 Programming note

Because at initial reset, the contents of display memory and LC3–LC0 (LCD contrast) are undefined, there is need to initialize by the software. Furthermore, take care of the registers LPWR and ALOFF because these are set so that the display goes OFF.

4.9 Clock Timer

4.9.1 Configuration of clock timer

The E0C6247 has a built-in clock timer as the source oscillator for OSC1 (crystal oscillator). The clock timer is configured of an 8-bit binary counter that serves as the input clock, fOSC1 divided clock output from the prescaler. Timer data (128–16 Hz and 8–1 Hz) can be read out by the software.
Figure 4.9.1.1 is the block diagram for the clock timer.

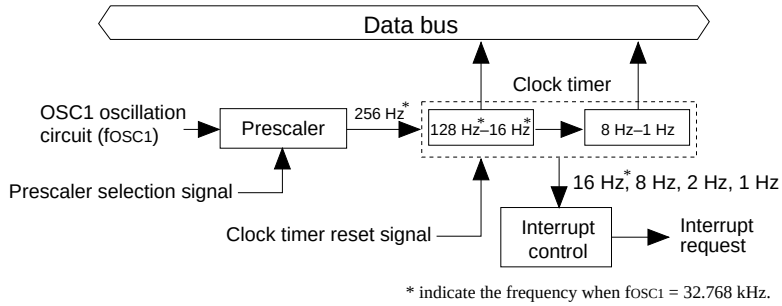


Fig. 4.9.1.1 Block diagram for the clock timer

Ordinarily, this clock timer is used for all types of timing functions such as clocks.
The clock timer uses the clock output from the prescaler. For this reason, the prescaler must be set correctly according to the frequency of the crystal oscillator to be used for OSC1 oscillation. (See Section 4.4, "Oscillation Circuit".)
When the OSC1 clock is 32.768 kHz, 38.4 kHz or 76.8 kHz, the clock timer counts using a 256 Hz clock output from the prescaler, and the 8-bit (4 bits × 2) timer data becomes 128–16 Hz and 8–1Hz. When the OSC1 clock is 50 kHz, counting is performed by a 200 Hz clock, and the timer data becomes 100–12.5 Hz and 8–1 Hz.
The following explains for fOSC1 = 32.768 kHz unless otherwise stated. Take care when using a 50 kHz oscillator.

4.9.2 Data reading and hold function

The 8 bits timer data are allocated to the address 8DH and 8EH.

<8DH>	D0: TM0 = 128 Hz (100 Hz)	D1: TM1 = 64 Hz (50 Hz)	D2: TM2 = 32 Hz (25 Hz)	D3: TM3 = 16 Hz (12.5 Hz)
<8EH>	D0: TM4 = 8 Hz	D1: TM5 = 4 Hz	D2: TM6 = 2 Hz	D3: TM7 = 1 Hz

( ) indicate value when fOSC1 = 50 kHz.

Since the clock timer data has been allocated to two addresses, a carry is generated from the low-order data within the count (TM0–TM3: 128–16 Hz) to the high-order data (TM4–TM7: 8–1 Hz). When this carry is generated between the reading of the low-order data and the high-order data, a content combining the two does not become the correct value (the low-order data is read as FFH and the high-order data becomes the value that is counted up 1 from that point).
The high-order data hold function in the E0C6247 is designed to operate to avoid this. This function temporarily stops the counting up of the high-order data (by carry from the low-order data) at the point where the low-order data has been read and consequently the time during which the high-order data is held is the shorter of the two indicated here following.

1. Period until it reads the high-order data.
2. 0.48–1.5 msec* (fOSC1 = 32.768 kHz)
   0.41–1.25 msec* (fOSC1 = 38.4 kHz or 76.8 kHz)
   0.3–1 msec* (fOSC1 = 50 kHz)
   * Varies due to the timing of the reading

Note: When the high-order data has previously been read, since the low-order data is not held, you should be sure to first read from the low-order data.

4.9.3 Interrupt function

The clock timer can cause interrupts at the falling edge of 16 Hz (12.5 Hz when f_{OSC1} = 50 kHz), 8 Hz, 2 Hz and 1 Hz signals. Software can set whether to mask any of these frequencies.
Figure 4.9.3.1 is the timing chart of the clock timer.

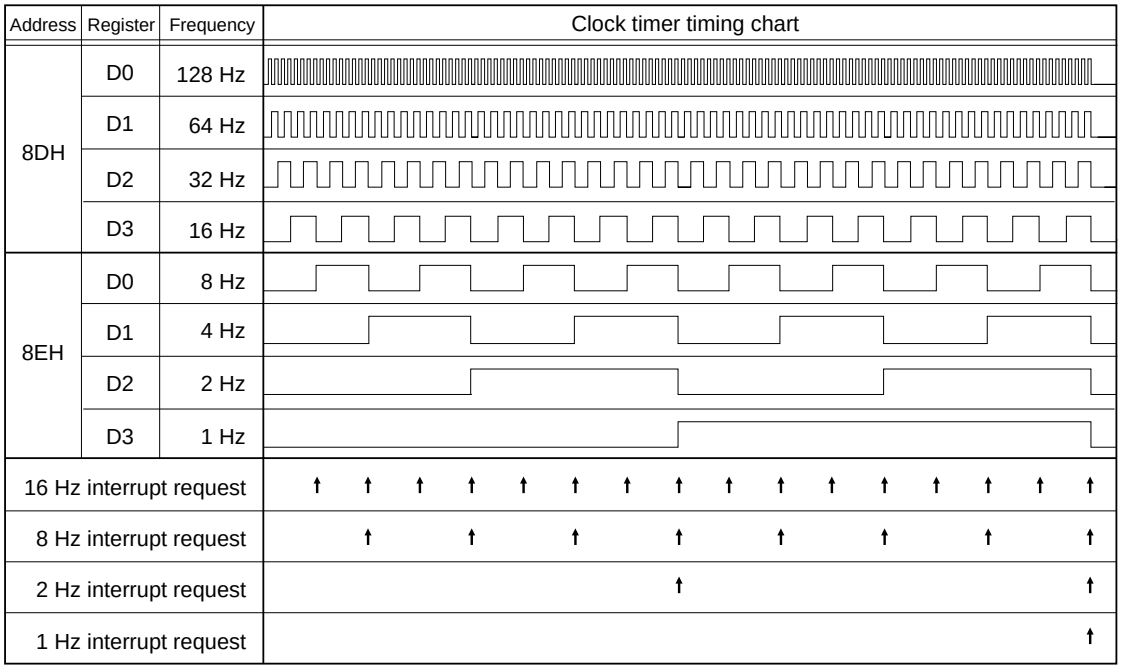


Fig. 4.9.3.1 Timing chart of clock timer

As shown in Figure 4.9.3.1, interrupt is generated at the falling edge of the frequencies (16 Hz, 8 Hz, 2 Hz, 1 Hz). At this time, the corresponding interrupt factor flag (IT0, IT1, IT2, IT3) is set to "1". Selection of whether to mask the separate interrupts can be made with the interrupt mask registers (EIT0, EIT1, EIT2, EIT3). However, regardless of the interrupt mask register setting, the interrupt factor flag is set to "1" at the falling edge of the corresponding signal.

Note:
- *Reading of interrupt factor flags is available at EI, but be careful in the following cases. If the interrupt mask register value corresponding to the interrupt factor flags to be read is set to "1", an interrupt request will be generated by the interrupt factor flags set timing, or an interrupt request will not be generated. Be very careful when interrupt factor flags are in the same address.*
- *Write the interrupt mask register only in the DI status (interrupt flag = "0"). Writing during EI status (interrupt flag = "1") will cause malfunction.*

4.9.4 Control of clock timer

Table 4.9.4.1 shows the clock timer control bits and their addresses.

Table 4.9.4.1 Control bits of clock timer

Address *7	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
8CH	0	0	TMRUN	TMRST	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R		R/W	W	TMRUN	0	Run	Stop	Clock timer Run/Stop
					TMRST *5	Reset	Reset	–	Clock timer reset
8DH	TM3	TM2	TM1	TM0	TM3	0			Clock timer data (16 Hz) [fOSC1 (12.5 Hz)
					TM2	0			Clock timer data (32 Hz) = 50 kHz (25 Hz)
	R				TM1	0			Clock timer data (64 Hz) → (50 Hz)
					TM0	0			Clock timer data (128 Hz) (100 Hz)]
8EH	TM7	TM6	TM5	TM4	TM7	0			Clock timer data (1 Hz)
					TM6	0			Clock timer data (2 Hz)
	R				TM5	0			Clock timer data (4 Hz)
					TM4	0			Clock timer data (8 Hz)
F4H	EIT3	EIT2	EIT1	EIT0	EIT3	0	Enable	Mask	Interrupt mask register (clock timer 1 Hz)
					EIT2	0	Enable	Mask	Interrupt mask register (clock timer 2 Hz)
	R/W				EIT1	0	Enable	Mask	Interrupt mask register (clock timer 8 Hz)
					EIT0	0	Enable	Mask	Interrupt mask register (clock timer 16 Hz)
									* When fOSC1 = 50 kHz: 16 Hz → 12.5 Hz
FCH	IT3	IT2	IT1	IT0	IT3 *4	0	Yes	No	Interrupt factor flag (clock timer 1 Hz)
					IT2 *4	0	Yes	No	Interrupt factor flag (clock timer 2 Hz)
	R				IT1 *4	0	Yes	No	Interrupt factor flag (clock timer 8 Hz)
					IT0 *4	0	Yes	No	Interrupt factor flag (clock timer 16 Hz)
									* When fOSC1 = 50 kHz: 16 Hz → 12.5 Hz

*1 Initial value at the time of initial reset
*2 Not set in the circuit
*3 Undefined
*4 Reset (0) immediately after being read
*5 Constantly "0" when being read
*6 Refer to main manual
*7 I/O memory is allocated from page 0 to 3

TM0–TM7: Timer data (8DH, 8EH)

The 128–1 Hz (100–12.5 Hz when fOSC1 = 50 kHz) timer data of the clock timer can be read out with these registers. These eight bits are read only, and writing operations are invalid.
By reading the low-order data (8DH), the high-order data (8EH) is held until reading or during the following time (one of shorter of them).

0.48–1.5 msec (fOSC1 = 32.768 kHz)
0.41–1.25 msec (fOSC1 = 38.4 kHz or 76.8 kHz)
0.3–1 msec (fOSC1 = 50 kHz)

At initial reset, the timer data is initialized to "00H".

TMRST: Clock timer reset (8CH•D0)

This bit resets the clock timer.

When "1" is written: Clock timer reset
When "0" is written: No operation
Reading: Always "0"

The clock timer is reset by writing "1" to TMRST. When the clock timer is reset in the RUN status, operation restarts immediately. Also, in the STOP status the reset data is maintained. No operation results when "0" is written to TMRST.
This bit is write-only, and so is always "0" at reading.

TMRUN: Clock timer RUN/STOP (8CH•D1)
This bit controls RUN/STOP of the clock timer.

When "1" is written:	RUN
When "0" is written:	STOP
Reading:	Valid

The clock timer enters the RUN status when "1" is written to TMRUN, and the STOP status when "0" is written.
In the STOP status, the timer data is maintained until the next RUN status or resets timer. Also, when the STOP status changes to the RUN status, the data that was maintained can be used for resuming the count.
At initial reset, this register is set to "0".

EIT0, EIT1, EIT2, EIT3: Interrupt mask registers (F4H)
These registers are used to select whether to mask the clock timer interrupt.

When "1" is written:	Enabled
When "0" is written:	Masked
Reading:	Valid

The interrupt mask registers (EIT0, EIT1, EIT2, EIT3) are used to select whether to mask the interrupt to the separate frequencies (16 Hz, 8 Hz, 2 Hz, 1 Hz).
Writing to the interrupt mask registers can be done only in the DI status (interrupt flag = "0").
When f_{OSC1} = 50 kHz, 16 Hz interrupt is changed to 12.5 Hz.
At initial reset, these registers are all set to "0".

IT0, IT1, IT2, IT3: Interrupt factor flags (FCH)
These flags indicate the status of the clock timer interrupt.

When "1" is read:	Interrupt has occurred
When "0" is read:	Interrupt has not occurred
Writing:	Invalid

The interrupt factor flags (IT0, IT1, IT2, IT3) correspond to the clock timer interrupts of the respective frequencies (16 Hz, 8 Hz, 2 Hz, 1 Hz). When f_{OSC1} = 50 kHz, 16 Hz interrupt is changed to 12.5 Hz. The software can judge from these flags whether there is a clock timer interrupt. However, even if the interrupt is masked, the flags are set to "1" at the falling edge of the signal.
These flags can be reset through being read out by the software.
Reading of interrupt factor flags is available at EI, but be careful in the following cases.
If the interrupt mask register value corresponding to the interrupt factor flags to be read is set to "1", an interrupt request will be generated by the interrupt factor flags set timing, or an interrupt request will not be generated. Be very careful when interrupt factor flags are in the same address.
At initial reset, these flags are set to "0".

4.9.5 Programming notes

(1) The prescaler must be set correctly to suit the crystal oscillator to be used for the OSC1 oscillation circuit.

(2) Be sure to data reading in the order of low-order data (TM0–TM3) then high-order data (TM4–TM7).

(3) When the clock timer has been reset, the interrupt factor flag (IT) may sometimes be set to "1". Consequently, perform flag reading (reset the flag) as necessary at reset.

(4) Reading of interrupt factor flags is available at EI, but be careful in the following cases.
If the interrupt mask register value corresponding to the interrupt factor flags to be read is set to "1", an interrupt request will be generated by the interrupt factor flags set timing, or an interrupt request will not be generated. Be very careful when interrupt factor flags are in the same address.

(5) Write the interrupt mask register (EIT) only in the DI status (interrupt flag = "0"). Writing during EI status (interrupt flag = "1") will cause malfunction.

4.10 Programmable Timer

4.10.1 Configuration of programmable timer

E0C6247 has a programmable timer which is configured with an 8 bits pre-settable down counter.
Aside from the count by the built-in clock (f_{OSC1}/f_{OSC3}), this programmable timer also possesses an event counter function that performs counting by making the signal input from the input port K02 the clock.
The initial value of count data can be set by software to the reload register; at the point where the down-counter value is "0", the programmable timer reloads the initial value and continues to down-count.
In addition, the clock created by the underflow of the down counter can be output to the serial interface and to the I/O port P32 (when the special output is selected).
Figure 4.10.1.1 shows the configuration of the programmable timer.

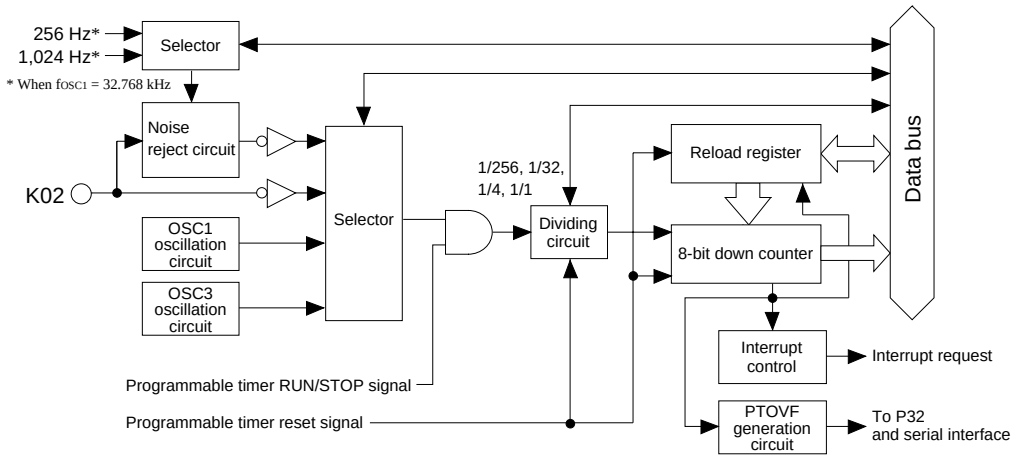


Fig. 4.10.1.1 Configuration of programmable timer

4.10.2 Input clock and pre-divider

(1) Clock source selection

The counter clock source can be selected among four types shown in Table 4.10.2.1 by registers PTPC0 and PTPC1.

Table 4.10.2.1 Clock source selection

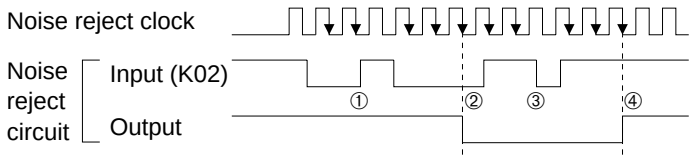
PTPC1	PTPC0	Clock source
1	1	OSC3
1	0	OSC1
0	1	K01 input (direct)
0	0	K02 input (with noise reject circuit)

When using the OSC3 clock, you must turn ON the OSC3 oscillation circuit in advance. If the OSC3 oscillation circuit is ON, counting can be done by the OSC3 clock, even when the CPU clock is OSC1.
The K02 input is an external input when used as an event counter. When K02 input (with noise reject circuit) has been selected, it passes through the noise reject circuit. In case such as when counting by a key input, this causes it to eliminate noise such as chattering.
The noise reject circuit performs an input clock sampling with 256 Hz or 1,024 Hz (when f_{OSC1} = 32.768 kHz). The sampling frequency can be selected using the register PNRFS. Signals less than 3 clocks in selected frequency are considered as noise and are not input as counting clocks.

Table 4.10.2.2 Noise reject clock selection

PNRFS	Frequency *	Sampling time
0	256 Hz	12 msec
1	1,024 Hz	3 msec

* 200 Hz and 1,562.5 Hz when fOSC1 = 50 kHz
256 Hz and 1,200 Hz when fOSC1 = 38.4 kHz or 76.8 kHz



① Low level is less than 3 clocks: the falling edge is not accepted
② Low level is 3 clocks or more: the falling edge is accepted
③ High level is less than 3 clocks: the rising edge is not accepted
④ High level is 3 clocks or more: the rising edge is accepted

Fig. 4.10.2.1 Sampling for noise rejection

The K02 input (direct) is bypassed by this noise reject circuit. When it inputs a clock of 3 msec or less (when fOSC1 = 32.768 kHz), you should select direct.

(2) Clock dividing ratio selection

For the programmable timer, the predivider is established after the selector for the above mentioned clock source and the input clock dividing ratio can be selected from four types. As shown in Table 4.10.2.3, this selection can be done by the registers PTPS0 and PTPS1.

Table 4.10.2.3 Clock dividing ratio selection

PTPS1	PTPS0	Dividing ratio
1	1	1/256
1	0	1/32
0	1	1/4
0	0	1/1

4.10.3 Operation of programmable timer

(1) Down-count

The 8-bit down counter counts down the divided input clock explained in the foregoing clause as the clock.
In case of K02 input, the down count timing becomes the falling edge of the clock and in OSC1 and OSC3 it becomes the rising edge.

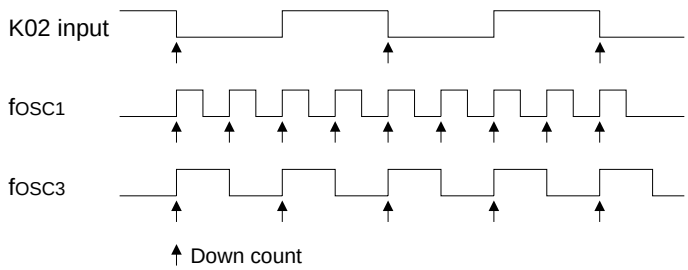


Fig. 4.10.3.1 Timing of down-counts

Run/Stop of the programmable timer can be controlled by register PTRUN.
When initiating programmable timer count, perform programming by the following steps:

1. Set the initial data to RD0–RD7.
2. Reset the programmable timer by writing "1" to PTRST.
3. Start the down-count by writing "1" to PTRUN.

(2) Data reload

The reload register (8 bits) for the initial value setting of the down counter is built into the programmable timer. The data set into the reload register is loaded into the down counter in the following instances and the count down is done from that value.

1. When the programmable timer has been reset by software
2. When the count down advances and the down counter becomes 00H

(3) Data reading

The low-order 4 bits of the down counter data is allocated to the address EDH and the high-order 4 bits are allocated to EEH and they can respectively be read.
At the time of this reading as well, the high-order data hold function operates the same as the clock timer. See to Section 4.9, "Clock Timer", for details of the hold function.

(4) PTOVF signal

The programmable timer generates a PTOVF signal by inverting the level each time the down counter becomes 00H.

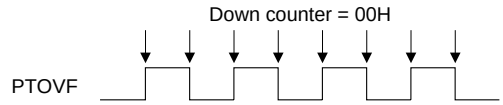


Fig. 4.10.3.2 PTOVF signal

The cycles (frequency) for this signal can be set according to the input clock, the dividing ratio and initial value that has been set for the reload register. The frequency of the output clock is indicated by the following expression.

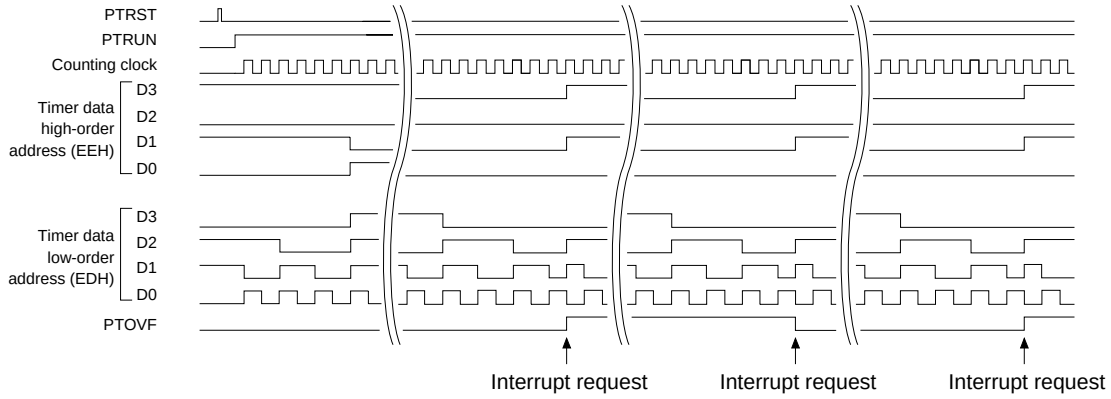
$fout = 1/2 \times fin \times dv / RD$

fout: PTOVF frequency
fin: Input clock frequency
dv: Dividing ratio (1/256, 1/32, 1/4, 1/1)
RD: Reload data

This PTOVF signal is input into the serial interface and can be used as the transfer clock. In addition, it can also be output externally through the I/O port P32.

4.10.4 Interrupt function

The programmable timer generates interrupt after the down-count from the initial setting is completed and the content of the down-counter indicates 00H.
After interrupt generation, the programmable timer reloads the initial count value into the down-counter and resumes counting.
Figure 4.10.4.1 shows the timing chart of the programmable timer.



Note: When "A6H" is set into reload register

Fig. 4.10.4.1 Timing chart of the programmable timer

When the down-counter values PT0–PT7 have become 00H the interrupt factor flag IPT is set to "1" and an interrupt is generated. The interrupt can be masked through the interrupt mask register EIPT. However, regardless of the setting of the interrupt mask register, the interrupt factor flag is set to "1" when the down-counter equals 00H.

4.10.5 Control of programmable timer

Table 4.10.5.1 list the programmable timer control bits and their addresses.

Table 4.10.5.1 Control bits of programmable timer

Address *7	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
E8H	0	0	PTPS1	PTPS0	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R		R/W		PTPS1	0			Programmable timer clock dividing ratio selection
					PTPS0	0			
E9H	0	0	PTPC1	PTPC0	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R		R/W		PTPC1	0			PT prescaler clock source selection
					PTPC0	0			
EAH	PNRFS	PTOE	PTRUN	PTRST	PNRFS	0	1024 Hz	256 Hz	Noise rejector clock frequency selection
					PTOE	0	Enable	Disable	PTOVF output enable
	R/W			W	PTRUN	0	Run	Stop	Programmable timer Run/Stop
					PTRST *5	– *2	Rst (reload)	–	Programmable timer reset (reload)
EBH	RD3	RD2	RD1	RD0	RD3	0			MSB Programmable timer reload data (low-order 4 bits) LSB
					RD2	0			
	R/W				RD1	0			
					RD0	0			
ECH	RD7	RD6	RD5	RD4	RD7	0			MSB Programmable timer reload data (high-order 4 bits) LSB
					RD6	0			
	R/W				RD5	0			
					RD4	0			
EDH	PT3	PT2	PT1	PT0	PT3	0			MSB Programmable timer data (low-order 4 bits) LSB
					PT2	0			
	R				PT1	0			
					PT0	0			
EEH	PT7	PT6	PT5	PT4	PT7	0			MSB Programmable timer data (high-order 4 bits) LSB
					PT6	0			
	R				PT5	0			
					PT4	0			
BFH	SELP33	SELP32	SELP31	SELP30	SELP33	0	FOUT	I/O	P33 function selection register (FOUT output or I/O)
					SELP32	0	PTOVF	I/O	P32 function selection register (PTOVF output or I/O)
	R/W				SELP31	0	FR	I/O	P31 function selection register (FR output or I/O)
					SELP30	0	CL	I/O	P30 function selection register (CL output or I/O)
F0H	0	0	0	EIPT	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R			R/W	0 *5	– *2			Unused
					EIPT	0	Enable	Mask	Interrupt mask register (programmable timer)
F8H	0	0	0	IPT	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R				0 *5	– *2			Unused
					IPT *4	0	Yes	No	Interrupt factor flag (programmable timer)

*1 Initial value at the time of initial reset
*2 Not set in the circuit
*3 Undefined
*4 Reset (0) immediately after being read
*5 Constantly "0" when being read
*6 Refer to main manual
*7 I/O memory is allocated from page 0 to 3

PTPC0, PTPC1: Prescaler clock source selection (E9H•D0, D1)

Selects the input clock for the prescaler.

Table 4.10.5.2 Clock source selection

PTPC1	PTPC0	Clock source
1	1	OSC3
1	0	OSC1
0	1	K01 input (direct)
0	0	K02 input (with noise reject circuit)

At initial reset, these registers are set to "0".

PNRFS: Noise reject clock frequency selection (EAH•D3)
Selects the frequency for noise reject clock.

When "1" is written: 1,024 Hz (*1)
When "0" is written: 256 Hz (*2)
Reading: Always "0"

Select either 1,024 Hz (*1) or 256 Hz (*2) for the noise reject clock frequency when K02 (with noise reject circuit) is selected for the clock source. When "1" is written to PNRFS, 1,024 Hz (*1) is selected and it accepts 3 msec or more K02 input signals. When "0" is written, 256 Hz (*2) is selected and it accepts 12 msec or more K02 input.
*1: 1,200 kHz when f_{OSC1} = 38.4 kHz or 76.8 kHz
1,562.5 Hz when f_{OSC1} = 50 kHz
*2: 200 Hz when f_{OSC1} = 50 kHz
At initial reset, this register is set to "0".

PTPS0, PTPS1: Dividing ratio selection (E8H•D0, D1)
Selects the dividing ratio for input clock.

Table 4.10.5.3 Clock dividing ratio selection

PTPS1	PTPS0	Dividing ratio
1	1	1/256
1	0	1/32
0	1	1/4
0	0	1/1

At initial reset, these registers are set to "0".

RD0–RD3, RD4–RD7: Reload register (EBH, ECH)
These are reload registers for setting the initial value of the timer.
Sets the low-order 4 bits of the 8 bits timer data to RD0–RD3, and the high-order 4 bits to RD4–RD7.
The set timer data is loaded to the down-counter when the programmable timer is reset or when the content of the down-counter is "00H".
When data of reload registers is set at "00H", the down-counter becomes a 256-value counter.
At initial reset, these registers are set to "0".

PTRST: Programmable timer reset (EAH•D0)
This bit resets the programmable timer.

When "1" is written: Programmable timer reset
When "0" is written: No operation
Reading: Always "0"

By writing "1" on PTRST, the programmable timer is reset.
The contents set in RD0–RD7 are loaded into the down-counter.
When the programmable timer is reset in the RUN mode, it will re-start counting immediately after loading and at STOP mode, the load data is maintained.
Because this bit is only for writing, it is always "0" during reading.

PTRUN: Programmable timer RUN/STOP (EAH•D1)
This register controls RUN/STOP of the programmable timer.

When "1" is written: RUN
When "0" is written: STOP
Reading: Valid

By writing "1" on PTRUN, the programmable timer performs counting operation. Writing "0" will make the programmable timer stop counting.
Even if the programmable timer is stopped, the timer data at that point is kept.
At initial reset, this register is set to "0".

PT0–PT3, PT4–PT7: Programmable timer data (EDH, EEH)

Will read the data from the down-counter of the programmable timer.
Will read the low-order 4 bits of the 8 bits counter data PT0–PT3, and the high-order 4 bits PT4–PT7.
Because these 8 bits are only for reading, writing operation is rendered invalid.
By reading the low-order 4 bits, the high-order data hold function operates. Reading should be done low-order 4 bits first.
At initial reset, timer data is set to "00H".

SELP32: P32 function selection register (BFH•D2)

Selects function for P32.

When "1" is written:	PTOVF output
When "0" is written:	I/O port
Reading:	Valid

When setting P32 to PTOVF (clock output from the programmable timer) output, write "1" to this register and when P32 is used as I/O port, write "0".
At initial reset, this register is set to "0".
When P32 is set to PTOVF output, the data register P32, I/O control register IOC32 and pull up control register PUL32 for the I/O port P32 can be used as general purpose registers that do not affect to the PTOVF output.

PTOE: PTOVF output enable register (EAH•D2)

Sets the PTOVF output.

When "1" is written:	PTOVF output enable
When "0" is written:	PTOVF output disable (high level output)
Reading:	Valid

By writing "1" to PTOE when SELP32 is set to "1", PTOVF signal is output from the P32 terminal. When "0" is written, the P32 terminal goes to high (V_{DD}).
At initial reset, this register is set to "0".

EIPT: Interrupt mask register (F0H•D0)

This register is used to select whether to mask the programmable timer interrupt.

When "1" is written:	Enabled
When "0" is written:	Masked
Reading:	Valid

With this register, masking of the programmable timer can be selected.
Writing to the interrupt mask registers can be done only in the DI status (interrupt flag = "0").
At initial reset, this register is set to "0".

IPT: Interrupt factor flag (F8H•D0)

This is the interrupt factor flag of the programmable timer.

When "1" is read:	Interrupt has occurred
When "0" is read:	Interrupt has not occurred
Writing:	Invalid

From the status of this flag, the software can decide whether the programmable timer interrupt. Note, however, that even if the interrupt is masked, this flag will be set to "1" by the counter value will become "00H".
This flag is reset when read out by the software.
Reading of interrupt factor flags is available at EI, but be careful in the following cases.
If the interrupt mask register value corresponding to the interrupt factor flags to be read is set to "1", an interrupt request will be generated by the interrupt factor flags set timing, or an interrupt request will not be generated.
At initial reset, this flag is set to "0".

4.10.6 Programming notes

(1) Be sure to data reading in the order of low-order data (PT0–PT3) then high-order data (PT4–PT7).

(2) When data of reload registers is set at "00H", the down-counter becomes a 256-value counter.

(3) Reading of interrupt factor flags is available at EI, but be careful in the following cases.
If the interrupt mask register value corresponding to the interrupt factor flags to be read is set to "1", an interrupt request will be generated by the interrupt factor flags set timing, or an interrupt request will not be generated.

(4) Write the interrupt mask register (EIPT) only in the DI status (interrupt flag = "0"). Writing during EI status (interrupt flag = "1") will cause malfunction.

4.11 Serial Interface

4.11.1 Configuration of serial interface

The E0C6247 incorporates a full duplex serial interface (when asynchronous system is selected) that allows the user to select either clock synchronous system or asynchronous system.
The data transfer method can be selected in software.
When the clock synchronous system is selected, 8-bit data transfer is possible.
When the asynchronous system is selected, either 7-bit or 8-bit data transfer is possible, and a parity check of received data and the addition of a parity bit for transmitting data can be done by selecting in software.
Figure 4.11.1.1 shows the configuration of the serial interface.

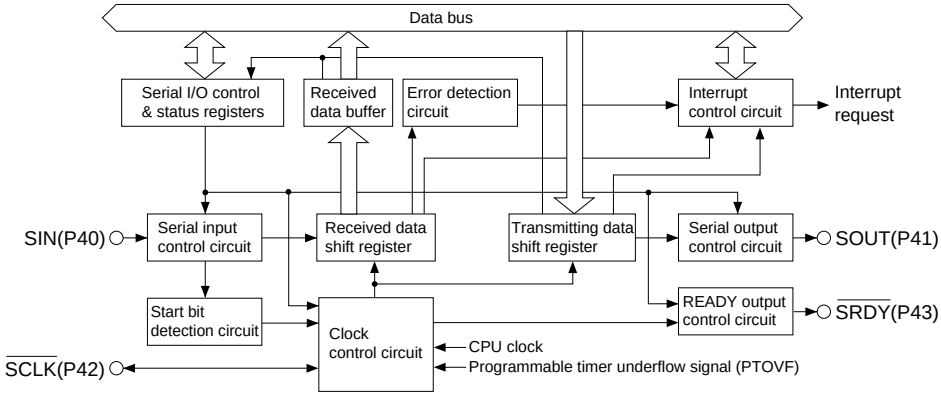


Fig. 4.11.1.1 Configuration of serial interface

Serial interface input/output terminals, SIN, SOUT, $\overline{SCLK}$ and $\overline{SRDY}$ are shared with I/O ports P40–P43. In order to utilize these terminals for the serial interface input/output terminals, proper settings have to be made with registers ESIF, SMD0 and SMD1.
At initial reset, these terminals are set as I/O port terminals. When the serial interface is used, switch the function (ESIF = "1") in the initial routine.
The direction of I/O port terminals set for serial interface input/output terminals are determined by the signal and transfer mode for each terminal. Furthermore, the settings for the corresponding I/O control registers for the I/O ports become invalid.

Table 4.11.1.1 Configuration of input/output terminals

Terminal	When serial interface is selected
P40	SIN
P41	SOUT
P42	$\overline{SCLK}$
P43	$\overline{SRDY}$

SIN and SOUT are serial data input and output terminals which function identically in clock synchronous system and asynchronous system. $\overline{SCLK}$ is exclusively for use with clock synchronous system and functions as a synchronous clock input/output terminal. $\overline{SRDY}$ is exclusively for use in clock synchronous slave mode and functions as a send-receive ready signal output terminal.
When asynchronous system is selected, since $\overline{SCLK}$ and $\overline{SRDY}$ are superfluous, the I/O port terminals P42 and P43 can be used as I/O ports.
In the same way, when clock synchronous master mode is selected, since $\overline{SRDY}$ is superfluous, the I/O port terminal P43 can be used as I/O port.

4.11.2 Mask option

Since the input/output terminal of the serial interface is dual used with the I/O ports (P40–P43), the mask option that selects the output specification for the I/O port is also applied to the serial interface.
The output specification of the terminals SOUT, $\overline{\text{SCLK}}$ (during the clock synchronous master mode) and $\overline{\text{SRDY}}$ (during the clock synchronous slave mode) that are used as output in the input/output port of the serial interface is respectively selected by the mask options of P41, P42 and P43.
Either complementary output or Nch open drain as output specification may be selected. However, even if Nch open drain has been selected, application on the terminal of voltage exceeding power source voltage is not permitted.

4.11.3 Transfer modes

There are four transfer modes for the serial interface and mode selection is made by setting the two bits of the mode selection registers SMD0 and SMD1 as shown in the table below.

Table 4.11.3.1 Transfer modes

SMD1	SMD0	Mode
1	1	Asynchronous 8-bit
1	0	Asynchronous 7-bit
0	1	Clock synchronous slave
0	0	Clock synchronous master

Table 4.11.3.2 Terminal settings corresponding to each transfer mode

Mode	SIN	SOUT	$\overline{\text{SCLK}}$	$\overline{\text{SRDY}}$
Asynchronous 8-bit	Input	Output	P42	P43
Asynchronous 7-bit	Input	Output	P42	P43
Clock synchronous slave	Input	Output	Input	Output
Clock synchronous master	Input	Output	Output	P43

At initial reset, transfer mode is set to clock synchronous master mode.

(1) Clock synchronous master mode

In this mode, the internal clock is utilized as a synchronous clock for the built-in shift registers, and clock synchronous 8-bit serial transfers can be performed with this serial interface as the master.
The synchronous clock is also output from the $\overline{\text{SCLK}}$ (P42) terminal which enables control of the external (slave side) serial I/O device. Since the $\overline{\text{SRDY}}$ (P43) terminal is not utilized in this mode, it can be used as an I/O port (P43).
Figure 4.11.3.1(a) shows the connection example of input/output terminals in the clock synchronous master mode.

(2) Clock synchronous slave mode

In this mode, a synchronous clock from the external (master side) serial input/output device is utilized and clock synchronous 8-bit serial transfers can be performed with this serial interface as the slave.
The synchronous clock is input to the $\overline{\text{SCLK}}$ (P42) terminal and is utilized by this interface as the synchronous clock.
Furthermore, the $\overline{\text{SRDY}}$ signal indicating the transmit-receive ready status is output from the $\overline{\text{SRDY}}$ (P43) terminal in accordance with the serial interface operating status.
In the slave mode, the settings for registers SCS0 and SCS1 used to select the clock source are invalid.
Figure 4.11.3.1(b) shows the connection example of input/output terminals in the clock synchronous slave mode.

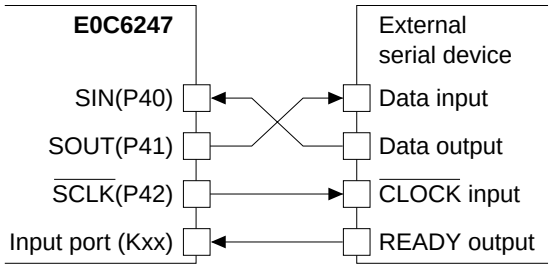
(3) Asynchronous 7-bit mode

In this mode, asynchronous 7-bit transfer can be performed. Parity check during data reception and addition of parity bit (odd/even/none) during transmitting can be specified and data processed in 7 bits with or without parity. Since this mode employs the internal clock, the $\overline{\text{SCLK}}$ (P42) terminal is not used. Furthermore, since the $\overline{\text{SRDY}}$ (P43) terminal is not utilized either, both of these terminals can be used as I/O ports (P42, P43).
Figure 4.11.3.1(c) shows the connection example of input/output terminals in the asynchronous mode.

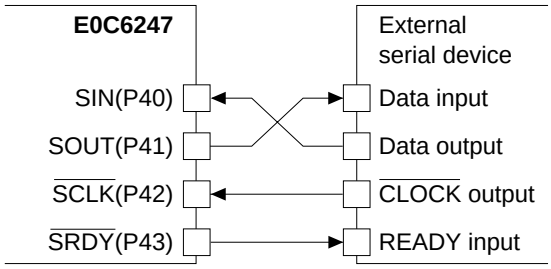
(4) Asynchronous 8-bit mode

In this mode, asynchronous 8-bit transfer can be performed. Parity check during data reception and addition of parity bit (odd/even/none) during transmitting can be specified and data processed in 8 bits with or without parity. Since this mode employs the internal clock, the $\overline{\text{SCLK}}$ (P42) terminal is not used. Furthermore, since the $\overline{\text{SRDY}}$ (P43) terminal is not utilized either, both of these terminals can be used as I/O ports (P42, P43).

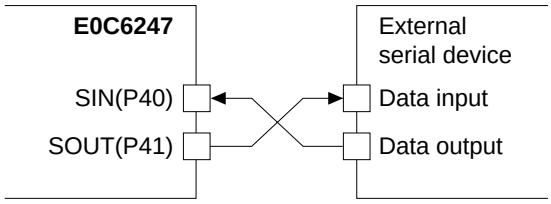
Figure 4.11.3.1(c) shows the connection example of input/output terminals in the asynchronous mode.



(a) Clock synchronous master mode



(b) Clock synchronous slave mode



(c) Asynchronous 7-bit/8-bit mode

Fig. 4.11.3.1 Connection examples of serial interface I/O terminals

4.11.4 Clock source

There are four clock sources and selection is made by setting the two bits of the clock source selection register SCS0 and SCS1 as shown in table below.

Table 4.11.4.1 Clock source

SCS1	SCS0	Clock source
1	1	Programmable timer × 1/2
1	0	CPU clock × 1/4
0	1	CPU clock × 1/8
0	0	CPU clock × 1/16

This register setting is invalid in clock synchronous slave mode and the external clock input from the $\overline{SCLK}$ (P42) terminal is used.
When the "programmable timer" is selected, the programmable timer underflow signal is divided by 1/2 and this signal (PTOVF signal) used as the clock source.
See Section 4.10, "Programmable Timer", for details of PTOVF signal.
At initial reset, the synchronous clock is set to "OSC1 × 1/16".
Whichever clock is selected, the signal is further divided by 1/16 and then used as the synchronous clock.
Furthermore, external clock input is used as is for $\overline{SCLK}$ in clock synchronous slave mode.

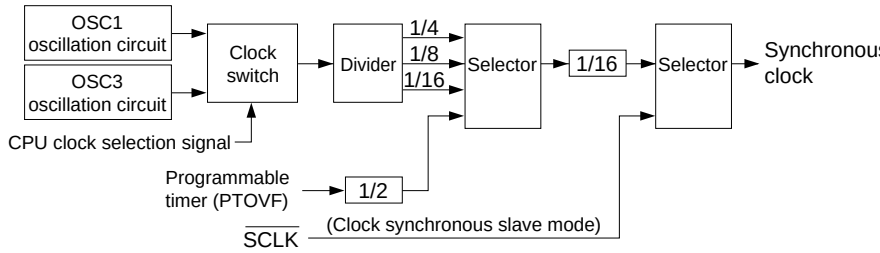


Fig. 4.11.4.1 Division of the synchronous clock

Table 4.11.4.2 shows an examples of transfer rates and OSC3 oscillation frequencies when the clock source is set to programmable timer.

Table 4.11.4.2 OSC3 oscillation frequencies and transfer rates

Transfer rate (bps)	OSC3 oscillation frequency/Programmable timer settings			
	f_{OSC3} = 0.9216 MHz		f_{OSC3} = 192 kHz	
	PTPSx	RDx	PTPSx	RDx
9,600	0 (1/1)	03H	0 (1/1)	0EH
4,800	0 (1/1)	06H	0 (1/1)	1DH
2,400	0 (1/1)	0CH	0 (1/1)	3BH
1,200	0 (1/1)	18H	0 (1/1)	05H
600	0 (1/1)	31H	0 (1/1)	0AH
300	0 (1/1)	61H	0 (1/1)	14H
150	0 (1/1)	C1H	0 (1/1)	28H

When the demultiplied signal of the OSC3 oscillation circuit is made the clock source, it is necessary to turn the OSC3 oscillation ON, prior to using the serial interface.
A time interval of several msec to several 10 msec, from the turning ON of the OSC3 oscillation circuit to until the oscillation stabilizes, is necessary, due to the oscillation element that is used. Consequently, you should allow an adequate waiting time after turning ON of the OSC3 oscillation, before starting transmitting/receiving of serial interface. (The oscillation start time will vary somewhat depending on the oscillator and on the externally attached parts. Refer to the oscillation start time example indicated in Chapter 7, "ELECTRICAL CHARACTERISTICS".)
At initial reset, the OSC3 oscillation circuit is set to OFF status.

4.11.5 Transmit-receive control

Below is a description of the registers which handle transmit-receive control. With respect to transmit-receive control procedures and operations, please refer to the following sections in which these are discussed on a mode by mode basis.

• Shift register and received data buffer

Exclusive shift registers for transmitting and receiving are installed in this serial interface. Consequently, duplex communication simultaneous transmit and receive is possible when the asynchronous system is selected.
Data being transmitted are written to TRXD0–TRXD7 and converted to serial through the shift register and is output from the SOUT (P41) terminal.
In the reception section, a received data buffer is installed separate from the shift register.
Data being received are input to the SIN (P40) terminal and is converted to parallel through the shift register and written to the received data buffer.
Since the received data buffer can be read even during serial input operation, the continuous data is received efficiently.
However, since buffer functions are not used in clock synchronous mode, be sure to read out data before the next data reception begins.

• Transmit enable register and transmit control bit

For transmitting control, use the transmit enable register TXEN and transmit control bit TXTRG.
The transmit enable register TXEN is used to set the transmitting enable/disable status. When "1" is written to this register to set the transmitting enable status, clock input to the shift register is enabled and the system is ready to transmit data. In the clock synchronous mode, synchronous clock input/output from the $\overline{\text{SCLK}}$ (P42) terminal is also enabled.
The transmit control bit TXTRG is used as the trigger to start transmitting data.
Data to be transmitted is written to the transmit data shift register, and when transmitting preparations a recomplete, "1" is written to TXTRG whereupon data transmitting begins.
When interrupt has been enabled, an interrupt is generated when the transmission is completed. If there is subsequent data to be transmitted it can be sent using this interrupt.
In addition, TXTRG can be read as the status. When set to "1", it indicates transmitting operation, and "0" indicates transmitting stop.
For details on timing, see the timing chart which gives the timing for each mode.
When not transmitting, set TXEN to "0" to disable transmitting status.

• Receive enable register, receive control bit

For receiving control, use the receive enable register RXEN and receive control bit RXTRG.
Receive enable register RXEN is used to set receiving enable/disable status. When "1" is written into this register to set the receiving enable status, clock input to the shift register is enabled and the system is ready to receive data. In the clock synchronous mode, synchronous clock input/output from the $\overline{\text{SCLK}}$ (P42) terminal is also enabled.
With the above setting, receiving begins and serial data input from the SIN (P40) terminal goes to the shift register.
The operation of the receive control bit RXTRG is slightly different depending on whether a clock synchronous system or an asynchronous system is being used.
In the clock synchronous system, the receive control bit RXTRG is used as the trigger to start receiving data.
When received data has been read and the preparation for next data receiving is completed, write "1" into RXTRG to start receiving. (When "1" is written to RXTRG in slave mode, $\overline{\text{SRDY}}$ switches to "0".)
In an asynchronous system, RXTRG is used to prepare for next data receiving. After reading the received data from the received data buffer, write "1" into RXTRG to signify that the received data buffer is empty. If "1" is not written into RXTRG, the overrun error flag OER will be set to "1" when the next receiving operation is completed. (An overrun error will be generated when receiving is completed between reading the received data and the writing of "1" to RXTRG.)
In addition, RXTRG can be read as the status. In either clock synchronous mode or asynchronous mode, when RXTRG is set to "1", it indicates receiving operation and when set to "0", it indicates that receiving has stopped.
For details on timing, see the timing chart which gives the timing for each mode.
When you do not receive, set RXEN to "0" to disable receiving status.

4.11.6 Operation of clock synchronous transfer

Clock synchronous transfer involves the transfer of 8-bit data by synchronizing it to eight clocks. The same synchronous clock is used by both the transmitting and receiving sides.
When the serial interface is used in the master mode, the clock signal selected using SCS0 and SCS1 is further divided by 1/16 and employed as the synchronous clock. This signal is then sent via the $\overline{\text{SCLK}}$ (P42) terminal to the slave side (external serial input/output device).
When used in the slave mode, the clock input to the $\overline{\text{SCLK}}$ (P42) terminal from the master side (external serial input/output device) is used as the synchronous clock.

In the clock synchronous mode, since one clock line ($\overline{\text{SCLK}}$) is shared for both transmitting and receiving, transmitting and receiving cannot be performed simultaneously. (Half duplex only is possible in clock synchronous mode.)

Transfer data is fixed at 8 bits and both transmitting and receiving are conducted with the LSB (bit 0) coming first.

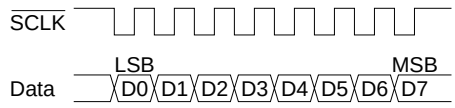


Fig. 4.11.6.1 Transfer data configuration using clock synchronous mode

Below is a description of initialization when performing clock synchronous transfer, transmit-receive control procedures and operations.
With respect to serial interface interrupt, see "Interrupt function".

• Initialization of serial interface

When performing clock synchronous transfer, the following initial settings must be made.

(1) Setting of transmitting/receiving disable

To set the serial interface into a status in which both transmitting and receiving are disabled, "0" must be written to both the transmit enable register TXEN and the receive enable register RXEN. Fix these two registers to a disable status until data transfer actually begins.

(2) Port selection

Because serial interface input/output ports SIN, SOUT, $\overline{\text{SCLK}}$ and $\overline{\text{SRDY}}$ are set as I/O port terminals P40–P43 at initial reset, "1" must be written to the serial interface enable register ESIF in order to set these terminals for serial interface use.

(3) Setting of transfer mode

Select the clock synchronous mode by writing the data as indicated below to the two bits of the mode selection registers SMD0 and SMD1 .

Master mode: SMD0 = "0", SMD1 = "0"
Slave mode: SMD0 = "1", SMD1 = "0"

(4) Clock source selection

In the master mode, select the synchronous clock source by writing data to the two bits of the clock source selection registers SCS0 and SCS1. (See Table 4.11.4.1.)
This selection is not necessary in the slave mode.

Since parity is not necessary in the clock synchronous mode, parity check will not take place regardless of EPR and PMD settings.

(5) Clock source control

When the master mode is selected and programmable timer for the clock source is selected, set transfer rate on the programmable timer side. (See Section 4.10, "Programmable Timer".)
When the divided signal of OSC3 oscillation circuit is selected for the clock source, be sure that the OSC3 oscillation circuit is turned ON prior to commencing data transfer. (See Section 4.4, "Oscillation Circuit".)

• Data transmit procedure

The control procedure and operation during transmitting is as follows.

(1) Write "0" in the transmit enable register TXEN and the receive enable register RXEN to reset the serial interface.

(2) Write "1" in the transmit enable register TXEN to set into the transmitting enable status.

(3) Write the transmitting data into TRXD0–TRXD7.

(4) In case of the master mode, confirm the receive ready status on the slave side (external serial input/output device), if necessary. Wait until it reaches the receive ready status.

(5) Write "1" in the transmit control bit TXTRG and start transmitting.

In the master mode, this control causes the synchronous clock to change to enable and to be provided to the shift register for transmitting and output from the $\overline{SCLK}$ (P42) terminal.
In the slave mode, it waits for the synchronous clock to be input from the $\overline{SCLK}$ (P42) terminal.
The transmitting data of the shift register shifts one bit at a time at each falling edge of the synchronous clock and is output from the SOUT (P41) terminal. When the final bit (MSB) is output, the SOUT (P41) terminal is maintained at that level, until the next transmitting begins.

The transmitting complete interrupt factor flag ISIFT is set to "1" at the point where the data transmitting of the shift register is completed. When interrupt has been enabled, a transmitting complete interrupt is generated at this point.
Set the following transmitting data using this interrupt.

(6) Repeat steps (3) to (5) for the number of bytes of transmitting data, and then set the transmit disable status by writing "0" to the transmit enable register TXEN, when the transmitting is completed.

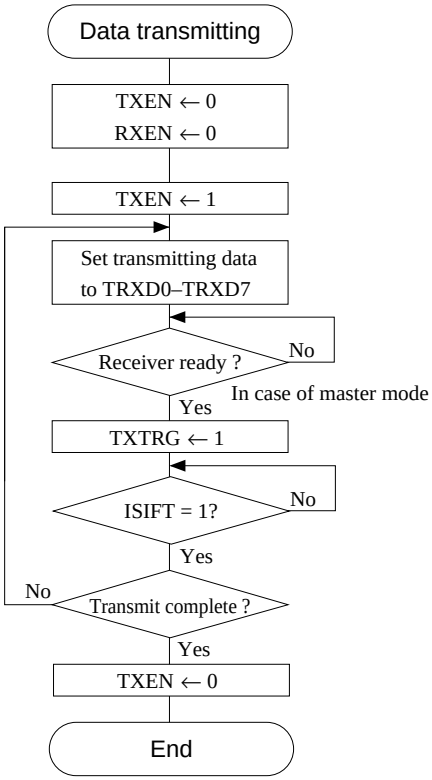


Fig. 4.11.6.2 Transmit procedure in clock synchronous mode

• Data receive procedure

The control procedure and operation during receiving is as follows.

(1) Write "0" in the receive enable register RXEN and transmit enable register TXEN to reset the serial interface.

(2) Write "1" in the receive enable register RXEN to set into the receiving enable status.

(3) In case of the master mode, confirm the transmit ready status on the slave side (external serial input/output device), if necessary. Wait until it reaches the transmit ready status.

(4) Write "1" in the receive control bit RXTRG and start receiving.

In the master mode, this control causes the synchronous clock to change to enable and is provided to the shift register for receiving and output from the $\overline{\text{SCLK}}$ (P42) terminal.
In the slave mode, it waits for the synchronous clock to be input from the $\overline{\text{SCLK}}$ (P42) terminal. The received data input from the SIN (P40) terminal is successively incorporated into the shift register in synchronization with the rising edge of the synchronous clock.
At the point where the data of the 8th bit has been incorporated at the final (8th) rising edge of the synchronous clock, the content of the shift register is sent to the received data buffer and the receiving complete interrupt factor flag ISIFR is set to "1". When interrupt has been enabled, a receiving complete interrupt is generated at this point.

(5) Read the received data from TRXD0–TRXD7 using receiving complete interrupt.

(6) Repeat steps (3) to (5) for the number of bytes of receiving data, and then set the receive disable status by writing "0" to the receive enable register RXEN, when the receiving is completed.

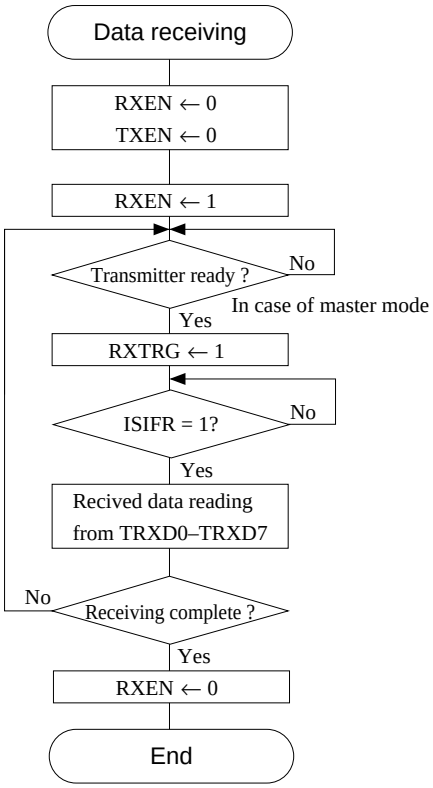


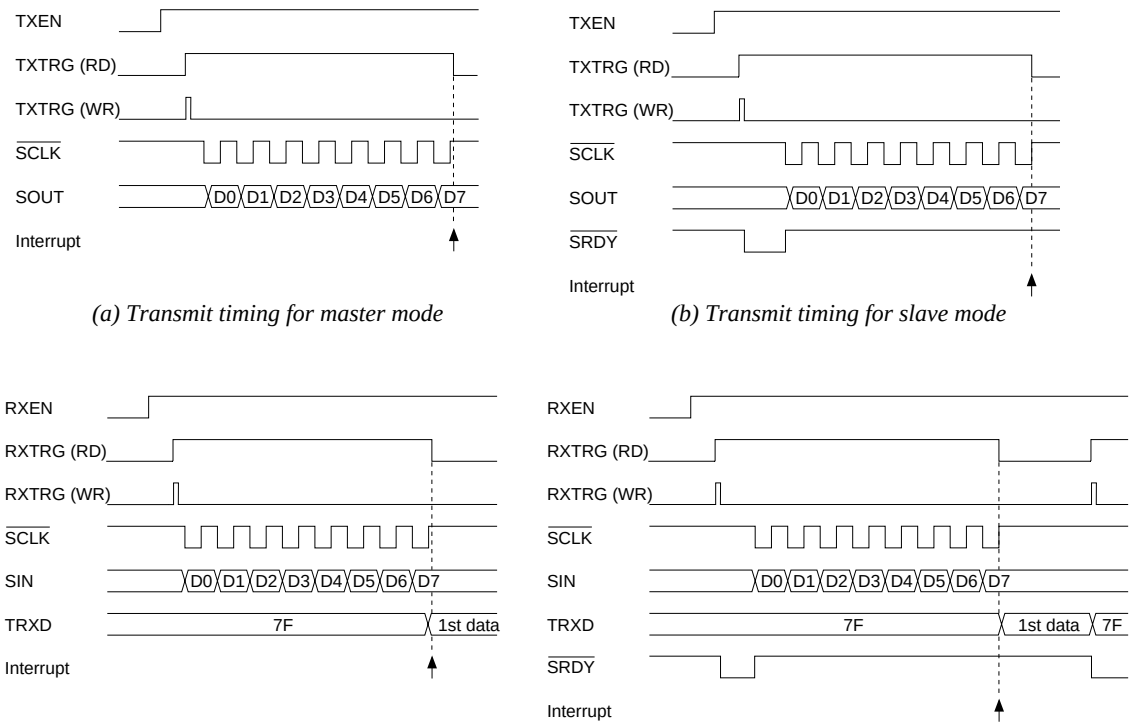
Fig. 4.11.6.3 Receiving procedure in clock synchronous mode

• Transmit/receive ready ($\overline{\text{SRDY}}$) signal

When this serial interface is used in the clock synchronous slave mode (external clock input), an $\overline{\text{SRDY}}$ signal is output to indicate whether or not this serial interface can transmit/receive to the master side (external serial input/output device). This signal is output from the $\overline{\text{SRDY}}$ (P43) terminal and when this interface enters the transmit or receive enable (READY) status, it becomes "0" (LOW level) and becomes "1" (HIGH level) when there is a BUSY status, such as during transmit/receive operation.
The $\overline{\text{SRDY}}$ signal changes the "1" to "0," immediately after writing "1" into the transmit control bit TXTRG or the receive control bit RXTRG and returns from "0" to "1", at the point where the first synchronous clock has been input (falling edge).
When you have set in the master mode, control the transfer by inputting the same signal from the slave side using the input port or I/O port. At this time, since the $\overline{\text{SRDY}}$ (P43) terminal is not set and instead P43 functions as the I/O port, you can apply this port for said control.

• Timing chart

The timing chart for the clock synchronous system transmission is shown in Figure 4.11.6.4.



(a) Transmit timing for master mode

(b) Transmit timing for slave mode

(c) Receive timing for master mode

(d) Receive timing for slave mode

Fig. 4.11.6.4 Timing chart (clock synchronous system transmission)

4.11.7 Operation of asynchronous transfer

Asynchronous transfer is a mode that transfers by adding a start bit and a stop bit to the front and the back of each piece of serial converted data. In this mode, there is no need to use a clock that is fully synchronized clock on the transmit side and the receive side, but rather transmission is done while adopting the synchronization at the start/stop bits that have attached before and after each piece of data. The RS-232C interface functions can be easily realized by selecting this transfer mode.
This interface has separate transmit and receive shift registers and is designed to permit full duplex transmission to be done simultaneously for transmitting and receiving.

For transfer data in the asynchronous 7-bit mode, either 7 bits data (no parity) or 7 bits data + parity bit can be selected. In the asynchronous 8-bit mode, either 8 bits data (no parity) or 8 bits data + parity bit can be selected.
Parity can be even or odd, and parity checking of received data and adding a party bit to transmitting data will be done automatically. Thereafter, it is not necessary to be conscious of parity itself in the program.
The start bit and stop bit are respectively fixed at one bit and data is transmitted and received by placing the LSB (bit 0) at the front.

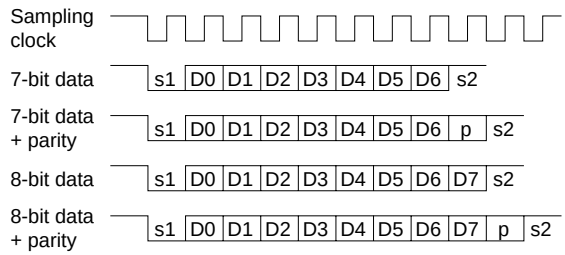


Fig. 4.11.7.1 Transfer data configuration for asynchronous system

Here following, we will explain the control sequence and operation for initialization and transmitting / receiving in case of asynchronous data transfer. See "Interrupt function" for the serial interface interrupts.

• Initialization of serial interface

The below initialization must be done in cases of asynchronous system transfer.

(1) Setting of transmitting/receiving disable

To set the serial interface into a status in which both transmitting and receiving are disabled, "0" must be written to both the transmit enable register TXEN and the receive enable register RXEN. Fix these two registers to a disable status until data transfer actually begins.

(2) Port selection

Because serial interface input/output terminals SIN and SOUT are set as I/O port terminals P40 and P41 at initial reset, "1" must be written to the serial interface enable register ESIF in order to set these terminals for serial interface use.
$\overline{\text{SCLK}}$ and $\overline{\text{SRDY}}$ terminals set in the clock synchronous mode are not used in the asynchronous mode. These terminals function as I/O port terminals P42 and P43.

(3) Setting of transfer mode

Select the asynchronous mode by writing the data as indicated below to the two bits of the mode selection registers SMD0 and SMD1.

7-bit mode: SMD0 = "0", SMD1 = "1"
8-bit mode: SMD0 = "1", SMD1 = "1"

(4) Parity bit selection

When checking and adding parity bits, write "1" into the parity enable register EPR to set to "with parity check". As a result of this setting, in the asynchronous 7-bit mode, it has a 7 bits data + parity bit configuration and in the asynchronous 8-bit mode it has an 8 bits data + parity bit configuration. In this case, parity checking for receiving and adding a party bit for transmitting is done automatically in hardware. Moreover, when "with parity check" has been selected, "odd" or "even" parity must be further selected in the parity mode selection register PMD.

When "0" is written to the EPR register to select "without parity check" in the asynchronous 7-bit mode, data configuration is set to 7 bits data (no parity) and in the asynchronous 8-bit mode (no parity) it is set to 8 bits data (no parity) and parity checking and parity bit adding will not be done.

(5) Clock source selection

Select the clock source by writing data to the two bits of the clock source selection registers SCS0 and SCS1. (See Table 4.11.4.1.)

(6) Clock source control

When the programmable timer is selected for the clock source, set transfer rate on the programmable timer side. (See Section 4.10, "Programmable Timer".)
When the divided signal of OSC3 oscillation circuit is selected for the clock source, be sure that the OSC3 oscillation circuit is turned ON prior to commencing data transfer. (See Section 4.4, "Oscillation Circuit.)

• Data transmit procedure

The control procedure and operation during transmitting is as follows.

(1) Write "0" in the transmit enable register TXEN to reset the serial interface.

(2) Write "1" in the transmit enable register TXEN to set into the transmitting enable status.

(3) Write the transmitting data into TRXD0–TRXD7.
Also, when 7-bit data is selected, the TRXD7 data becomes invalid.

(4) Write "1" in the transmit control bit TXTRG and start transmitting.
This control causes the shift clock to change to enable and a start bit (LOW) is output to the SOUT (P41) terminal in synchronize to its falling edge. The transmitting data set to the shift register is shifted one bit at a time at each falling edge of the clock thereafter and is output from the SOUT (P41) terminal. After the data output, it outputs a stop bit (HIGH) and HIGH level is maintained until the next start bit is output.

The transmitting complete interrupt factor flag ISIFT is set to "1" at the point where the data transmitting is completed. When interrupt has been enabled, a transmitting complete interrupt is generated at this point.
Set the following transmitting data using this interrupt.

(5) Repeat steps (3) to (4) for the number of bytes of transmitting data, and then set the transmit disable status by writing "0" to the transmit enable register TXEN, when the transmitting is completed.

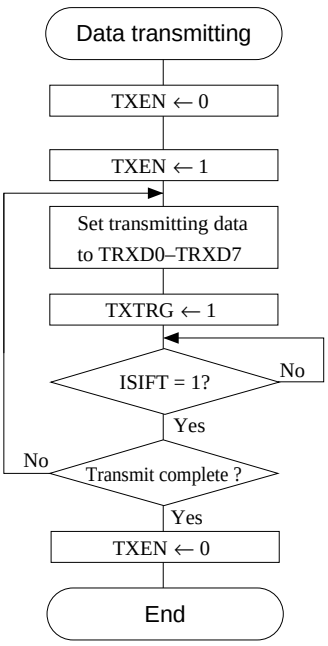


Fig. 4.11.7.2 Transmit procedure in asynchronous mode

• Data receive procedure

The control procedure and operation during receiving is as follows.

(1) Write "0" in the receive enable register RXEN to set the receiving disable status and to reset the respective PER, OER, FER flags that indicate parity, overrun and framing errors.

(2) Write "1" in the receive enable register RXEN to set into the receiving enable status.

(3) The shift clock will change to enable from the point where the start bit (LOW) has been input from the SIN (P40) terminal and the receive data will be synchronized to the rising edge following the second clock, and will thus be successively incorporated into the shift register.
After data bits have been incorporated, the stop bit is checked and, if it is not HIGH, it becomes a framing error and the error interrupt factor flag ISIFE is set to "1". When interrupt has been enabled, an error interrupt is generated at this point.
When receiving is completed, data in the shift register is transferred to the received data buffer and the receiving complete interrupt flag ISIFR is set to "1". When interrupt has been enabled, a receiving complete interrupt is generated at this point. (When an overrun error is generated, the interrupt factor flag ISIFR is not set to "1" and a receiving complete interrupt is not generated.)
If "with parity check" has been selected, a parity check is executed when data is transferred into the received data buffer from the shift register and if a parity error is detected, the error interrupt factor flag is set to "1". When the interrupt has been enabled, an error interrupt is generated at this point just as in the framing error mentioned above.

(4) Read the received data from TRXD0–TRXD7 using receiving complete interrupt.

(5) Write "1" to the receive control bit RXTRG to inform that the receive data has been read out.
When the following data is received prior to writing "1" to RXTRG, it is recognized as an overrun error and the error interrupt factor flag ISIFE is set to "1". When the interrupt has been enabled, an error interrupt is generated at this point just as in the framing error and parity error mentioned above.

(6) Repeat steps (3) to (5) for the number of bytes of receiving data, and then set the receive disable status by writing "0" to the receive enable register RXEN, when the receiving is completed.

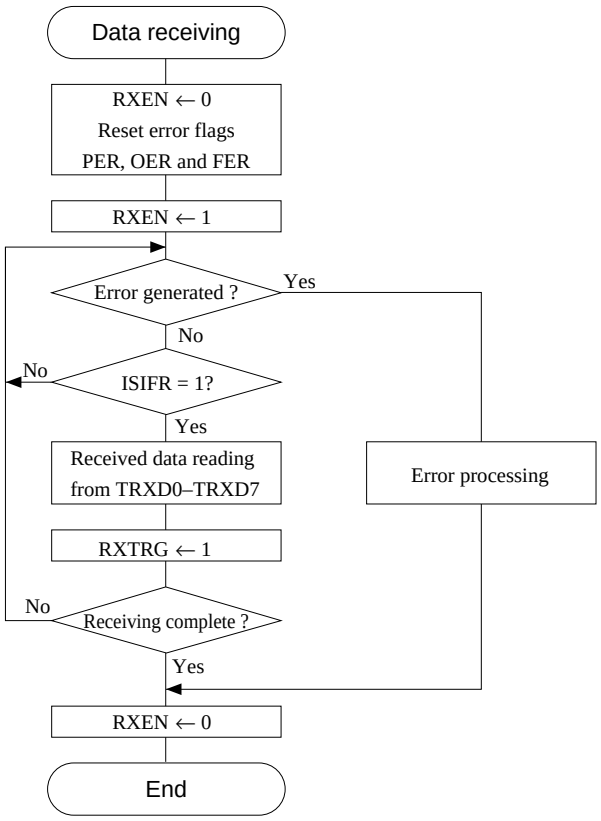


Fig. 4.11.7.3 Receiving procedure in asynchronous mode

• Receive error

During receiving the following three types of errors can be detected by an interrupt.

(1) Parity error

When writing "1" to the EPR register to select "with parity check", a parity check (vertical parity check) is executed during receiving. After each data bit is sent a parity check bit is sent. The parity check bit is a "0" or a "1". Even parity checking will cause the sum of the parity bit and the other bits to be even. Odd parity causes the sum to be odd. This is checked on the receiving side.

The parity check is performed when data received in the shift register is transferred to the received data buffer. It checks whether the parity check bit is a "1" or a "0" (the sum of the bits including the parity bit) and the parity set in the PMD register match. When it does not match, it is recognized as an parity error and the parity error flag PER and the error interrupt factor flag ISIFE is set to "1".

When interrupt has been enabled, an error interrupt is generated at this point.

The PER flag is reset to "0" by writing "1".

Even when this error has been generated, the received data corresponding to the error is transferred in the received data buffer and the receive operation also continues.

The received data at this point cannot assured because of the parity error.

(2) Framing error

In asynchronous transfer, synchronization is adopted for each character at the start bit ("0") and the stop bit ("1"). When receiving has been done with the stop bit set at "0", the serial interface judges the synchronization to be off and a framing error is generated. When this error is generated, the framing error flag FER and the error interrupt factor flag ISIFE are set to "1". When interrupt has been enabled, an error interrupt is generated at this point.

The FER flag is reset to "0" by writing "1".

Even when this error has been generated, the received data corresponding to the error is transferred in the received data buffer and the receive operation also continues. However, even when it does not become a framing error with the following data receiving, such data cannot be assured.

(3) Overrun error

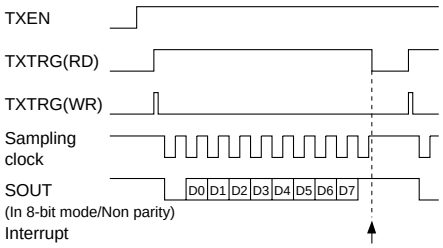
When the next data is received before "1" is written to RXTRG, an overrun error will be generated, because the previous receive data will be overwritten. When this error is generated, the overrun error flag OER and the error interrupt factor flag ISIFE are set to "1". When interrupt has been enabled, an error interrupt is generated at this point. The OER flag is reset to "0" by writing "1" into it.

Even when this error has been generated, the received data corresponding to the error is transferred in the received data buffer and the receive operation also continues.

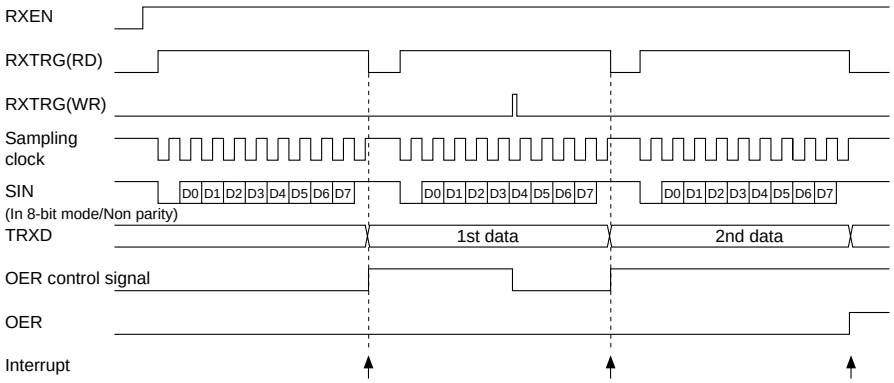
Furthermore, when the timing for writing "1" to RXTRG and the timing for the received data transfer to the received data buffer overlap, it will be recognized as an overrun error.

• Timing chart

Figure 4.11.7.4 show the asynchronous transfer timing chart.



(a) Transmit timing



(b) Receive timing

Fig. 4.11.7.4 Timing chart (asynchronous transfer)

4.11.8 Interrupt function

This serial interface includes a function that generates the below indicated three types of interrupts.

- Transmitting complete interrupt
- Receiving complete interrupt
- Error interrupt

The interrupt factor flag ISIFx and the interrupt mask register EISIFx for the respective interrupt factors are provided and then the interrupt enable/mask can be selected by the software.

• Transmitting complete interrupt

This interrupt factor is generated at the point where the sending of the data written into the shift register has been completed and sets the interrupt factor flag ISIFT to "1". When set in this manner, if the corresponding interrupt mask register EISIFT is set to "1", an interrupt will be generated to the CPU.
When "0" has been written into the interrupt mask register EISIFT and interrupt has been disabled, an interrupt is not generated to the CPU. Even in this case, the interrupt factor flag ISIFT is set to "1".
The interrupt factor flag ISIFT is reset to "0" by reading.
The following transmitting data can be set and the transmitting start (writing "1" to TXTRG) can be controlled by generation of this interrupt factor.
The interrupt vector address for this interrupt factor is set at 108H.

• Receiving complete interrupt

This interrupt factor is generated at the point where receiving has been completed and the receive data incorporated into the shift register has been transferred into the received data buffer and it sets the interrupt factor flag ISIFR to "1". When set in this manner, if the corresponding interrupt mask register EISIFR is set to "1", an interrupt will be generated to the CPU.
When "0" has been written into the interrupt mask register EISIFR and interrupt has been disabled, an interrupt is not generated to the CPU. Even in this case, the interrupt factor flag ISIFR is set to "1".
The interrupt factor flag ISIFR is reset to "0" by reading.

The generation of this interrupt factor permits the received data to be read.

Also, the interrupt factor flag ISIFR is set to "1" when a parity error or framing error is generated.

The interrupt vector address for this interrupt factor is set at 106H.

• Error interrupt

This interrupt factor is generated at the point where a parity error, framing error or overrun error is detected during receiving and it sets the interrupt factor flag ISIFE to "1". When set in this manner, if the corresponding interrupt mask register EISIFE is set to "1", an interrupt will be generated to the CPU.
When "0" has been written in the interrupt mask register EISIFE and interrupt has been disabled, an interrupt is not generated to the CPU. Even in this case, the interrupt factor flag ISIFE is set to "1".
The interrupt factor flag ISIFE is reset to "0" by reading.

Since all three types of errors result in the same interrupt factor, you should identify the error that has been generated by the error flags PER (parity error), OER (overrun error) and FER (framing error).

The interrupt vector address for this interrupt factor is set at 104H.

4.11.9 Control of serial interface

Table 4.11.9.1 list the serial interface control bits and their addresses.

Table 4.11.9.1 Control bits of serial interface

Address *7	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
C8H	0	SMD1	SMD0	ESIF	0 *5	– *2			Unused
					SMD1	0			Serial I/F mode selection (SMD[1][0]: 1 1 Asynchronous 8-bit; 1 0 Asynchronous 7-bit; 0 1 Clock synchronous slave; 0 0 Clock synchronous master)
	R	R/W			SMD0	0			
					ESIF	0	SI/F	I/O	Serial I/F enable (P4 port function selection)
C9H	EPR	PMD	SCS1	SCS0	EPR	0	WithParity	NonParity	Parity enable (only for asynchronous mode)
					PMD	0	Odd	Even	Parity mode selection
	R/W				SCS1	0			Clock source selection (SCS[1][0]: 1 1 PT × 1/2; 1 0 CPU clock × 1/4; 0 1 CPU clock × 1/8; 0 0 CPU clock × 1/16)
					SCS0	0			
CAH	RXTRG	RXEN	TXTRG	TXEN	RXTRG(R)	0	Run	Stop	Receive status (when reading)
					RXTRG(W)		Trigger	–	Receive trigger (when writing)
					RXEN	0	Enable	Disable	Receive enable
	R/W				TXTRG(R)	0	Run	Stop	Transmit status (when reading)
					TXTRG(W)		Trigger	–	Transmit trigger (when writing)
					TXEN	0	Enable	Disable	Transmit enable
CBH	0	FER	PER	OER	0 *5	– *2			Unused
					FER(R)	0	Error	NoError	Framing error flag (when reading)
					FER(W)		Reset	–	flag reset (when writing)
					PER(R)	0	Error	NoError	Parity error flag (when reading)
	R	R/W			PER(W)		Reset	–	flag reset (when writing)
					OER(R)	0	Error	NoError	Overrun error flag (when reading)
					OER(W)		Reset	–	flag reset (when writing)
CCH	TRXD3	TRXD2	TRXD1	TRXD0	TRXD3	– *2	High	Low	Transmit/Receive data (low-order 4 bits)
					TRXD2	– *2	High	Low	
	R/W				TRXD1	– *2	High	Low	
					TRXD0	– *2	High	Low	LSB
CDH	TRXD7	TRXD6	TRXD5	TRXD4	TRXD7	– *2	High	Low	MSB
					TRXD6	– *2	High	Low	Transmit/Receive data (high-order 4 bits)
	R/W				TRXD5	– *2	High	Low	
					TRXD4	– *2	High	Low	
C1H	PUL43	PUL42	PUL41	PUL40	PUL43	1	On	Off	P43 pull up control register (General-purpose register when SI/F (sync. slave) is selected)
					PUL42	1	On	Off	P42 pull up control register (General-purpose register when SI/F (sync. master) is selected)
	R/W				PUL41	1	On	Off	P41 pull up control register (ESIF = 0) (General-purpose register when SI/F is selected)
					PUL40	1	On	Off	P40 pull up control register (ESIF = 0) SIN pull up control register (ESIF = 1)
F1H	0	EISIFE	EISIFT	EISIFR	0 *5	– *2			Unused
					EISIFE	0	Enable	Mask	Interrupt mask register (serial I/F error)
	R	R/W			EISIFT	0	Enable	Mask	Interrupt mask register (serial I/F transmitting)
					EISIFR	0	Enable	Mask	Interrupt mask register (serial I/F receiving)
F9H	0	ISIFE	ISIFT	ISIFR	0 *5	– *2			Unused
					ISIFE*4	0	Yes	No	Interrupt factor flag (serial I/F error)
	R				ISIFT*4	0	Yes	No	Interrupt factor flag (serial I/F transmitting)
					ISIFR*4	0	Yes	No	Interrupt factor flag (serial I/F receiving)

*1 Initial value at the time of initial reset
*2 Not set in the circuit
*3 Undefined
*4 Reset (0) immediately after being read
*5 Constantly "0" when being read
*6 Refer to main manual
*7 I/O memory is allocated from page 0 to 3

ESIF: Serial interface enable (C8H•D0)

Sets P40–P43 as input/output port for the serial interface.

When "1" is written: Serial interface
When "0" is written: I/O port
Reading: Valid

The ESIF is the serial interface enable register and P40–P43 terminals become serial input/output terminals (SIN, SOUT, $\overline{\text{SCLK}}$, $\overline{\text{SRDY}}$) when "1" is written, and they become I/O port terminals when "0" is written. Also, see Table 4.11.3.2 for the terminal settings according to the transfer modes.
At initial reset, this register is set to "0".

SMD1, SMD0: Serial interface mode selection (C8H•D2, D1)

Set the transfer modes according to Table 4.11.9.2.

Table 4.11.9.2 Transfer mode settings

SMD1	SMD0	Mode
1	1	Asynchronous 8-bit
1	0	Asynchronous 7-bit
0	1	Clock synchronous slave
0	0	Clock synchronous master

SMD0 and SMD1 can also read out.
At initial reset, these registers are set to "0".

SCS1, SCS0: Clock source selection (C9H•D1, D0)

Select the clock source according to Table 4.11.9.3.

Table 4.11.9.3 Clock source selection

SCS1	SCS0	Clock source
1	1	Programmable timer × 1/2
1	0	CPU clock × 1/4
0	1	CPU clock × 1/8
0	0	CPU clock × 1/16

SCS0 and SCS1 can also be read out.
In the clock synchronous slave mode, setting of this register is invalid. At initial reset, these registers are set to "0".

EPR: Parity enable (C9H•D3)

Selects the parity function.

When "1" is written: With parity
When "0" is written: Non parity
Reading: Valid

Selects whether or not to check parity of the received data and to add a parity bit to the transmitting data. When "1" is written to EPR, the most significant bit of the received data is considered to be the parity bit and a parity check is executed. A parity bit is added to the transmitting data. When "0" is written, neither checking is done nor is a parity bit added.
Parity is valid only in asynchronous mode and the EPR setting becomes invalid in the clock synchronous mode.
At initial reset, this register is set to "0".

PMD: Parity mode selection (C9H•D2)

Selects odd parity/even parity.

When "1" is written: Odd parity
When "0" is written: Even parity
Reading: Valid

When "1" is written to PMD, odd parity is selected and even parity is selected when "0" is written. The parity check and addition of a parity bit is only valid when "1" has been written to EPR. When "0" has been written to EPR, the parity setting by PMD becomes invalid.
At initial reset, this register is set to "0".

PUL40, PUL42: Pull up control registers (C1H•D0, D2)

The pull up for the SIN (P40) terminal and the $\overline{SCLK}$ (P42) terminal (during clock synchronous slave mode) can be set with these registers.

When "1" is written:	Pull up ON
When "0" is written:	Pull up OFF
Reading:	Valid

The pull up resistors built into the SIN (P40) and $\overline{SCLK}$ (P42) terminals are set to ON or OFF.
Pull up for the $\overline{SCLK}$ (P42) terminal is valid only in the clock synchronous slave mode.
At initial reset, these registers are set to "1", so the pull up resistors are set to ON.

TXEN: Transmit enable (CAH•D0)

Sets the serial interface to the transmitting enable status.

When "1" is written:	Transmitting enable
When "0" is written:	Transmitting disable
Reading:	Valid

When "1" is written to TXEN, the serial interface shifts to the transmitting enable status and shifts to the transmitting disable status when "0" is written.
Set TXEN to "0" when making the initial settings of the serial interface and similar operations.
At initial reset, this register is set to "0".

TXTRG: Transmit control bit (CAH•D1)

Functions as the transmitting start trigger and the operation status indicator (transmitting/stop status).

When "1" is read:	During transmitting
When "0" is read:	During stop
When "1" is written:	Transmitting start
When "0" is written:	Invalid

Starts the transmitting when "1" is written to TXTRG after writing the transmitting data.
TXTRG can be read as the status. When set to "1", it indicates transmitting operation, and "0" indicates transmitting stop.
At initial reset, this bit is set to "0".

RXEN: Receive enable (CAH•D2)

Sets the serial interface to the receiving enable status.

When "1" is written:	Receiving enable
When "0" is written:	Receiving disable
Reading:	Valid

When "1" is written to RXEN, the serial interface shifts to the receiving enable status and shifts to the receiving disable status when "0" is written.
Set RXEN to "0" when making the initial settings of the serial interface and similar operations.
At initial reset, this register is set to "0".

RXTRG: Receive control trigger (CAH•D3)

Functions as the receiving start trigger or preparation for the following data receiving and the operation status indicator (during receiving/during stop).

When "1" is read:	During receiving
When "0" is read:	During stop
When "1" is written:	Receiving start/following data receiving preparation
When "0" is written:	Invalid

RXTRG has a slightly different operation in the clock synchronous system and the asynchronous system.

The RXTRG in the clock synchronous system, is used as the trigger for the receiving start.
Writes "1" into RXTRG to start receiving at the point where the receive data has been read and the following receive preparation has been done. (In the slave mode, $\overline{SRDY}$ becomes "0" at the point where "1" has been written into into the RXTRG.)

RSTRG is used in the asynchronous system for preparation of the following data receiving. Reads the received data located in the received data buffer and writes "1" into RXTRG to inform that the received data buffer has shifted to empty. When "1" has not been written to RXTRG, the overrun error flag OER is set to "1" at the point where the following receiving has been completed. (When the receiving has been completed between the operation to read the received data and the operation to write "1" into RXTRG, an overrun error occurs.)

In addition, RXTRG can be read as the status. In either clock synchronous mode or asynchronous mode, when RXTRG is set to "1", it indicates receiving operation and when set to "0", it indicates that receiving has stopped.
At initial reset, this bit is set to "0".

TRXD7–TRXD0: Transmit/receive data (CDH, CCH)

During transmitting
Write the transmitting data into the transmit shift register.

When "1" is written: HIGH level
When "0" is written: LOW level

Write the transmitting data prior to starting transmitting.
In the case of continuous transmitting, wait for the transmitting complete interrupt, then write the data.
The TRXD7 becomes invalid for the asynchronous 7-bit mode.
Converted serial data for which the bits set at "1" as HIGH (V_{DD}) level and for which the bits set at "0" as LOW (V_{SS}) level are output from the SOUT (P41) terminal.

During receiving
Read the received data.

When "1" is read: HIGH level
When "0" is read: LOW level

The data from the received data buffer can be read out.
Since the sift register is provided separately from this buffer, reading can be done during the receive operation in the asynchronous mode. (The buffer function is not used in the clock synchronous mode.)
Read the data after waiting for the receiving complete interrupt.
When performing parity check in the asynchronous 7-bit mode, "0" is loaded into the 8th bit (TRXD7) that corresponds to the parity bit.
The serial data input from the SIN (P40) terminal is level converted, making the HIGH (V_{DD}) level bit "1" and the LOW (V_{SS}) level bit "0" and is then loaded into this buffer.
At initial reset, the buffer content is undefined.

OER: Overrun error flag (CBH•D0)

Indicates the generation of an overrun error.

When "1" is read: Error
When "0" is read: No error

When "1" is written: Reset to "0"
When "0" is written: Invalid

OER is an error flag that indicates the generation of an overrun error and becomes "1" when an error has been generated.
An overrun error is generated when the receiving of data has been completed prior to the writing of "1" to RXTRG in the asynchronous mode.
OER is reset to "0" by writing "1".
At initial reset and when RXEN is "0", this flag is set to "0".

PER: Parity error flag (CBH•D1)

Indicates the generation of a parity error.

When "1" is read:	Error
When "0" is read:	No error
When "1" is written:	Reset to "0"
When "0" is written:	Invalid

PER is an error flag that indicates the generation of a parity error and becomes "1" when an error has been generated.
When a parity check is performed in the asynchronous mode, if data that does not match the parity is received, a parity error is generated.
PER is reset to "0" by writing "1".
At initial reset and when RXEN is "0", this flag is set to "0".

FER: Framing error flag (CBH•D2)

Indicates the generation of a framing error.

When "1" is read:	Error
When "0" is read:	No error
When "1" is written:	Reset to "0"
When "0" is written:	Invalid

FER is an error flag that indicates the generation of a framing error and becomes "1" when an error has been generated.
When the stop bit for the receiving of the asynchronous mode has become "0", a framing error is generated.
FER is reset to "0" by writing "1".
At initial reset and when RXEN is "0", this flag is set to "0" (no error).

EISIFE, ESIFT, ESIFR: Interrupt mask registers (F1H•D2, D1, D0)

These are the interrupt mask registers of the serial interface.

When "1" is written:	Enabled
When "0" is written:	Masked
Reading:	Valid

EISIFE, EISIFT and EISIFR are interrupt mask registers that respectively correspond to the interrupt factors for receiving error, transmitting complete and receiving complete. Interrupts set to "1" are enabled and interrupts set to "0" are masked.
Writing to the interrupt mask registers can be done only in the DI status (interrupt flag = "0").
At initial reset, these registers are set to "0".

ISIFE, ISIFT, ISIFR: Interrupt factor flags (F9H•D2, D1, D0)

Indicates the serial interface interrupt generation status.

When "1" is read:	Interrupt has occurred
When "0" is read:	Interrupt has not occurred
Writing:	Invalid

ISIFE, ISIFT and ISIFR are interrupt factor flags that respectively correspond to the interrupts for receiving error, transmitting complete and receiving complete and are set to "1" by generation of each factor.
Receiving error interrupt factor is generated when a parity error, framing error or overrun error has been detected during data receiving.
Transmitting complete interrupt factor is generated at the point where the data transmitting of the shift register has been completed.
Receiving complete interrupt factor is generated at the point where the received data has been transferred into the received data buffer.
The interrupt factor flag is reset when it has been read out.
At initial reset, these flags are reset to "0".

4.11.10 Programming notes

(1) Be sure to initialize the serial interface mode in the transmitting/receiving disable status (TXEN = RXEN = "0").

(2) Do not perform double trigger (writing "1") to TXTRG (RXTRG) when the serial interface is in the transmitting (receiving) operation.

(3) In the clock synchronous mode, since one clock line ($\overline{SCLK}$) is shared for both transmitting and receiving, transmitting and receiving cannot be performed simultaneously.
Consequently, be sure not to write "1" to RXTRG (TXTRG) when TXTRG (RXTRG) is "1".

(4) When a parity error or flaming error is generated during receiving in the asynchronous mode, the receiving error interrupt factor flag ISIFE is set to "1" prior to the receiving complete interrupt factor flag ISIFR for the time indicated in Table 4.11.10.1. Consequently, you should reset the receiving complete interrupt factor flag ISIFR to "0" by providing a wait time in error processing routines and similar routines.
When an overrun error is generated, the receiving complete interrupt factor flag ISIFR is not set to "1" and a receiving complete interrupt is not generated.

Table 4.11.10.1 Time difference between ISIFE and ISIFR on error generation

Clock source	Time difference
CPU clock / n	1/2 cycles of CPU clock / n
Programmable timer × 1/2	1 cycle of programmable timer underflow

(5) When the demultiplied signal of the OSC3 oscillation circuit is made the clock source, it is necessary to turn the OSC3 oscillation ON, prior to using the serial interface.
A time interval of 5 msec, from the turning ON of the OSC3 oscillation circuit to until the oscillation stabilizes, is necessary, due to the oscillation element that is used. Consequently, you should allow an adequate waiting time after turning ON of the OSC3 oscillation, before starting transmitting/receiving of serial interface. (The oscillation start time will vary somewhat depending on the oscillator and on the externally attached parts. Refer to the oscillation start time example indicated in Chapter 7, "ELECTRICAL CHARACTERISTICS".)
At initial reset, the OSC3 oscillation circuit is set to OFF status.

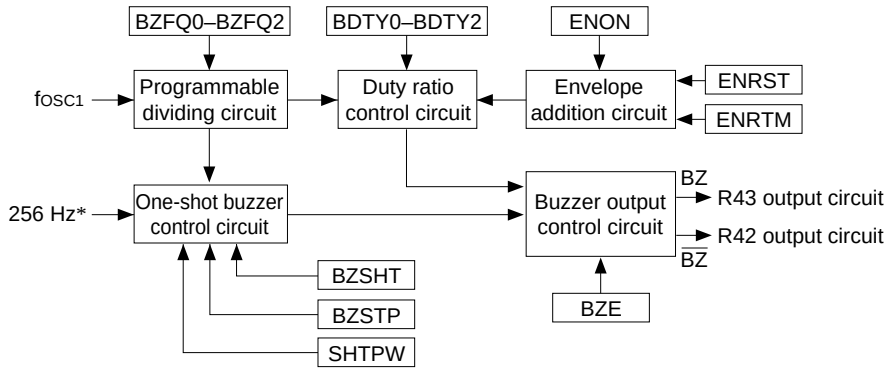
(6) Write the interrupt mask register only in the DI status (interrupt flag = "0"). Writing during EI status (interrupt flag = "1") will cause malfunction.

(7) Reading of interrupt factor flags is available at EI, but be careful in the following cases.
If the interrupt mask register value corresponding to the interrupt factor flags to be read is set to "1", an interrupt request will be generated by the interrupt factor flags set timing, or an interrupt request will not be generated. Be very careful when interrupt factor flags are in the same address.

4.12 Sound Generator

4.12.1 Configuration of sound generator

The E0C6247 has a built-in sound generator for generating buzzer signal.
The buzzer signal generated from the sound generator can be output from the R43 (BZ) and R42 ($\overline{BZ}$) output port terminals.
Aside permitting the respective setting of the buzzer signal frequency and sound level (duty adjustment) to 8 stages, it permits the adding of a digital envelope by means of duty ratio control. It also has a one-shot output function for outputting key operated sounds.
Figure 4.12.1.1 shows the configuration of the sound generator.



* When fOSC1 = 32.768 kHz, 38.4 kHz and 76.8 kHz

Fig. 4.12.1.1 Configuration of sound generator

4.12.2 Control of buzzer output

Buzzer signal (BZ) can be output from the R43 output port terminal. The buzzer inverted signal ($\overline{BZ}$) that is generated by inverting the phase of the buzzer signal can be output from the R42 output port terminal.
The output terminals are shared with the R43 and R42. When outputting the buzzer signals, R43 and R42 should be set to the buzzer output independently using the SELR43 register and the SELR42 register.
The data register of the output port set to the buzzer output can be used as a general purpose register that does not affect the output.
The high impedance control registers R43HIZ and R42HIZ are effective even when the buzzer output has been set. When "1" is written to the register, the output shifts to high impedance status and "0" is written, the buzzer signal is output.
The BZ signal generated by the sound generator can be output from the R43 terminal by writing "1" to the BZ output enable register (BZE) when the output port R43 is set to the buzzer output (SELR43 = "1"). The $\overline{BZ}$ signal can be controlled by the BZE register at the same time with the BZ signal, it is output from the R42 terminal when the output port R42 is set to the buzzer inverted output (SELR42 = "1"). When BZE is set to "0", the output terminals go to low (VSS) level.

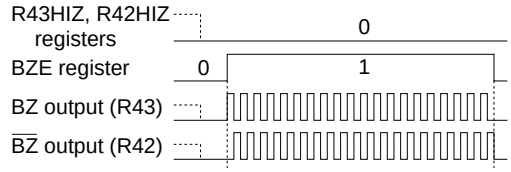


Fig. 4.12.2.1 Timing chart of buzzer signal output

Note: Since the buzzer signal is generated asynchronously from the register BZE, when the signal is turned ON or OFF by the register setting, a hazard is generated.

4.12.3 Setting of buzzer frequency and sound level

The buzzer signal is a divided signal using the OSC1 oscillation circuit as the clock source and 8 frequencies can be selected. This selection is done by the buzzer frequency selection register BZFQ0–BZFQ2. The setting value and buzzer frequency correspondence is shown in Table 4.12.3.1.

Table 4.12.3.1 Buzzer signal frequency settings

BZFQ2	BZFQ1	BZFQ0	Dividing ratio	Buzzer frequency (Hz)			
				f_{OSC1} = 32.768 kHz	f_{OSC1} = 38.4 kHz	f_{OSC1} = 50.0 kHz	f_{OSC1} = 76.8 kHz
0	0	0	f_{OSC1} /8	4096.0	4800.0	6250.0	9600.0
0	0	1	f_{OSC1} /10	3276.8	3840.0	5000.0	7680.0
0	1	0	f_{OSC1} /12	2730.7	3200.0	4166.7	6400.0
0	1	1	f_{OSC1} /14	2340.6	2742.9	3571.4	5485.7
1	0	0	f_{OSC1} /16	2048.0	2400.0	3125.0	4800.0
1	0	1	f_{OSC1} /20	1638.4	1920.0	2500.0	3840.0
1	1	0	f_{OSC1} /24	1365.3	1600.0	2083.3	3200.0
1	1	1	f_{OSC1} /28	1170.3	1371.4	1785.7	2742.9

By selecting the duty ratio of the buzzer signal from among 8 types, the buzzer sound level can be adjusted. This selection is made in the duty ratio selection register BDTY0–BDTY2. The setting value and duty ratio correspondence is shown in Table 4.12.3.2.

Table 4.12.3.2 Duty ratio settings

Level	BDTY2	BDTY1	BDTY0	Duty ratio by buzzer frequency			
				f_{OSC1} /8 f_{OSC1} /16	f_{OSC1} /10 f_{OSC1} /20	f_{OSC1} /12 f_{OSC1} /24	f_{OSC1} /14 f_{OSC1} /28
Level 1 (maximum)	0	0	0	8/16	8/20	12/24	12/28
Level 2	0	0	1	7/16	7/20	11/24	11/28
Level 3	0	1	0	6/16	6/20	10/24	10/28
Level 4	0	1	1	5/16	5/20	9/24	9/28
Level 5	1	0	0	4/16	4/20	8/24	8/28
Level 6	1	0	1	3/16	3/20	7/24	7/28
Level 7	1	1	0	2/16	2/20	6/24	6/28
Level 8 (minimum)	1	1	1	1/16	1/20	5/24	5/28

Duty ratio refers to the ratio of pulse width to the pulse cycle; given that HIGH level output time is TH, and low level output time is TL the buzzer signal becomes TH/(TH+TL).
When BDTY0–BDTY2 have all been set to "0", the duty ratio becomes maximum and the sound level also becomes maximum. Conversely, when BDTY0–BDTY2 have all been set to "1", the duty ratio becomes minimum and the sound level also becomes minimum.
Note that the duty ratio setting differ depending on frequency.

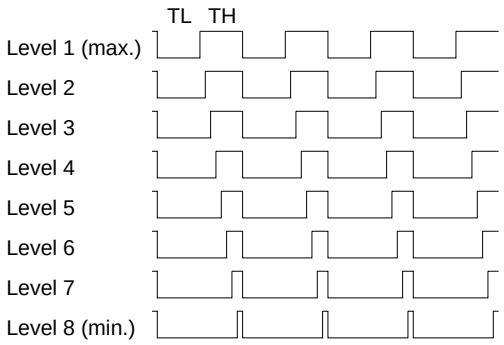


Fig. 4.12.3.1 Duty ratio of buzzer signal waveform

Note: When using the digital envelope, the BDTY0–BDTY2 setting becomes invalid.

4.12.4 Digital envelope

A digital envelope with duty control can be added to the buzzer signal.
The envelope can be realized by staged changing of the same duty ratio as detailed in Table 4.12.3.2 in the preceding section from level 1 (maximum) to level 8 (minimum).
The addition of an envelope to the buzzer signal can be done by writing "1" to the envelope control register ENON. When "0" is written, the duty ratio is set at the level selected in BDTY0–BDTY2.
By writing "1" to ENON to turn the buzzer output ON (writing "1" to BZE), a buzzer signal with a level 1 duty ratio is output, and then the duty ratio can be attenuated in stages to level 8. The attenuated envelope can be returned to level 1 by writing "1" to the envelope reset bit ENRST. When attenuated to level 8, the duty level remains at level 8 until the buzzer output is turned OFF (writing "0" to BZON) or writing "1" to ENRST.
The stage changing time for the envelope level can be selected with the ENRTM register. This time is 62.5 msec (80 msec when f_{OSC1} = 50 kHz) when "0" is written, and 125 msec (160 msec when f_{OSC1} = 50 kHz) when "1" is written. However, a maximum difference of 4 msec (5 msec when f_{OSC1} = 50 kHz) is taken from envelope-ON until the first change.
Figure 4.12.4.1 shows the timing chart of the digital envelope.

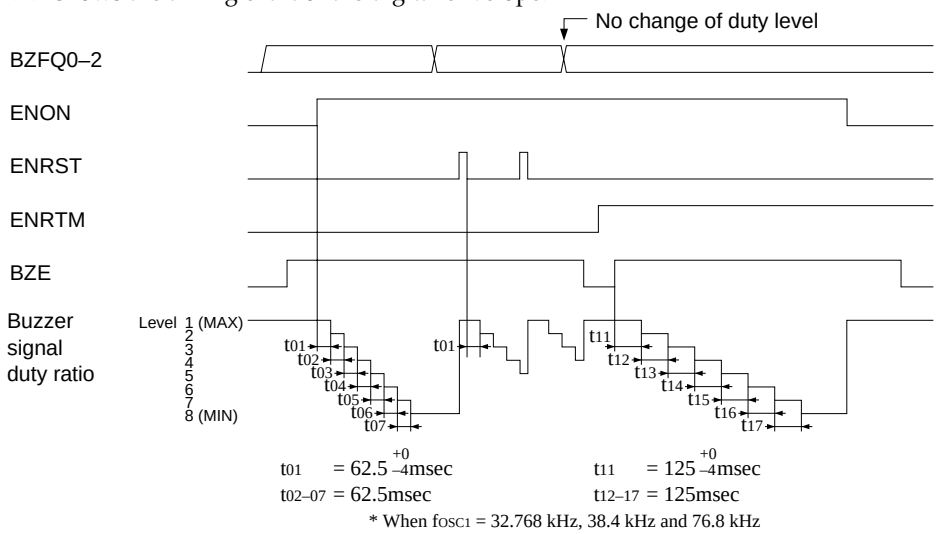


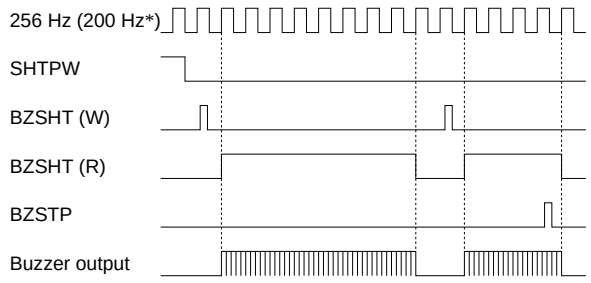
Fig. 4.12.4.1 Timing chart of digital envelope

4.12.5 One-shot output

The sound generator has a built-in one-shot output function for outputting a short duration buzzer signal for key operation sounds and similar effects. Either 125 msec or 31.25 msec can be selected by the one-shot buzzer duration selection register SHTPW for buzzer signal output time. (160 msec or 40 msec when f_{OSC1} = 50 kHz)
The output control of the one-shot buzzer is done by writing "1" to the one-shot buzzer trigger BZSHT (there is no need to control BZE), then the BZ signal is output from the R43 terminal and the $\overline{BZ}$ signal from R42 terminal in synchronization with the internal 256 Hz (200 Hz when f_{OSC1} = 50 kHz) signal. (When R43 and R42 are set to buzzer output.) Thereafter, when the set time has elapsed, the buzzer signal in synchronization with the 256 Hz (200 Hz) signal automatically goes OFF in the same manner.
The BZSHT can be read to determine status. When BZSHT is "1", it indicates a BUSY status (during one-shot output) and when BZSHT is "0", it indicates a READY status (during stop).
When you want to turn the buzzer signal OFF prior to the elapse of the set time, the buzzer signal can be immediately stopped (goes OFF in asynchonization with 256 Hz (200 Hz) signal) by writing "1" to the one-shot forced stop bit BZSTP.

Since the one-shot output has a short duration, an envelope cannot be added. (When "1" is written to BZSHT, ENON is automatically reset to "0".) Consequently, only the frequency and sound level can be set for one-shot output.

The control for the one-shot output is invalid during normal buzzer output.
Figure 4.12.5.1 shows the timing chart of the one-shot output.



* 200 Hz: when f_{OSC1} = 50 kHz

Fig. 4.12.5.1 Timing chart of one-shot output

4.12.6 Control of sound generator

Table 4.12.6.1 list the sound generator control bits and their addresses.

Table 4.12.6.1 Control bits of sound generator

Address *7	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
E0H	ENRTM	ENRST	ENON	BZE	ENRTM	0	1 sec	0.5 sec	Envelope attenuation time selection
					ENRST *5	– *2	Reset	–	Envelope reset
	R/W	W	R/W		ENON	0	On	Off	Envelope On/Off
					BZE	0	Enable	Disable	BZ output enable
E1H	0	BZSTP	BZSHT	SHTPW	0 *5	– *2			Unused
					BZSTP *5	– *2	Stop	–	One-shot buzzer stop
					BZSHT(W)	– *2	Trigger	–	One-shot buzzer trigger (when writing)
					BZSHT(R)	0	Busy	Ready	One-shot buzzer status (when reading)
	R	W	R/W		SHTPW	0	125 msec	31.25 msec	One-shot buzzer pulse width selection (160/40 msec is in case of f_{OSC1} = 50 kHz)
E2H	0	BZFQ2	BZFQ1	BZFQ0	0 *5	– *2			Unused
					BZFQ2	0			Buzzer frequency selection
					BZFQ1	0			
	R	R/W			BZFQ0	0			
E3H	0	BDTY2	BDTY1	BDTY0	0 *5	– *2			Unused
					BDTY2	0			Buzzer signal duty ratio selection *6
	R	R/W			BDTY1	0			
					BDTY0	0			
A8H	R43HIZ	R42HIZ	R41HIZ	R40HIZ	R43HIZ	0	High-Z	Output	R43 output high-impedance control
					R42HIZ	0	High-Z	Output	R42 output high-impedance control
					R41HIZ	0	High-Z	Output	R41 output high-impedance control (EXTMF = 0) (General-purpose register when EXTMF = 1)
	R/W				R40HIZ	0	High-Z	Output	R40 output high-impedance control (EXTMF = 0) (General-purpose register when EXTMF = 1)
AAH	SELR43	SELR42	0	0	SELR43	0	BZ	Normal	R43 function selection register (BZ or general-purpose output)
					SELR42	0	$\overline{BZ}$	Normal	R42 function selection register ($\overline{BZ}$ or general-purpose output)
	R/W		R		0 *5	– *2			Unused
					0 *5	– *2			Unused

Buzzer frequency selection	BZFQ [2][1][0]	Buzzer frequency	f_{OSC1} = 32 kHz (Hz)
	1 1 1	f_{OSC1}/28	1170.3
	1 1 0	f_{OSC1}/24	1365.3
	1 0 1	f_{OSC1}/20	1638.4
	1 0 0	f_{OSC1}/16	2048.0
	0 1 1	f_{OSC1}/14	2340.6
	0 1 0	f_{OSC1}/12	2730.7
	0 0 1	f_{OSC1}/10	3276.8
	0 0 0	f_{OSC1}/8	4096.0

*1 Initial value at the time of initial reset
*2 Not set in the circuit
*3 Undefined
*4 Reset (0) immediately after being read
*5 Constantly "0" when being read
*6 Refer to main manual
*7 I/O memory is allocated from page 0 to 3

SELR42: R42 function selection register (AAH•D2)

Selects the output function for R42.

When "1" is written: $\overline{BZ}$ output
When "0" is written: General purpose output port
Reading: Valid

When setting R42 to $\overline{BZ}$ (buzzer inverted signal) output, write "1" to this register and when R42 is used as general purpose output port, write "0".
At initial reset, this register is set to "0".
When the $\overline{BZ}$ output has been set, the data register of the output port 42 can be used as a general purpose register that does not affect the output.

SELR43: R43 function selection register (AAH•D3)

Selects the output function for R43.

When "1" is written: BZ output
When "0" is written: General purpose output port
Reading: Valid

When setting R43 to BZ (buzzer signal) output, write "1" to this register and when R43 is used as general purpose output port, write "0".
At initial reset, this register is set to "0".
When the BZ output has been set, the data register of the output port 43 can be used as a general purpose register that does not affect the output.

R42HIZ, R43HIZ: High impedance control registers (A8H•D2, D3)

Controls high impedance output of the output port.

When "1" is written: High impedance
When "0" is written: Buzzer output
Reading: Valid

By writing "0" into the high impedance control register, the corresponding output terminal shifts to the status that can output the buzzer signal. When "1" is written, it shifts to high impedance status.
At initial reset, these registers are set to "0".

BZE: Buzzer output enable (E0H•D0)

Controls the buzzer signal output.

When "1" is written: Buzzer signal output enabled
When "0" is written: Buzzer signal output disabled
Reading: Valid

When "1" is written to BZE, the buzzer signal output is enabled. It outputs the buzzer signal from the R42 or R43 terminals that is set to the buzzer output by the SELR42 or SELR43 register settings. When "0" is written, LOW (V_{SS}) level is output.
At initial reset, this register is set to "0".

BZFQ0–BZFQ2: Buzzer frequency selection registers (E2H•D0–D2)

Selects the buzzer signal frequency.

Table 4.12.6.2 Buzzer frequency settings

BZFQ2	BZFQ1	BZFQ0	Dividing ratio	Buzzer frequency (Hz)			
				f_{OSC1} = 32.768 kHz	f_{OSC1} = 38.4 kHz	f_{OSC1} = 50.0 kHz	f_{OSC1} = 76.8 kHz
0	0	0	f_{OSC1} /8	4096.0	4800.0	6250.0	9600.0
0	0	1	f_{OSC1} /10	3276.8	3840.0	5000.0	7680.0
0	1	0	f_{OSC1} /12	2730.7	3200.0	4166.7	6400.0
0	1	1	f_{OSC1} /14	2340.6	2742.9	3571.4	5485.7
1	0	0	f_{OSC1} /16	2048.0	2400.0	3125.0	4800.0
1	0	1	f_{OSC1} /20	1638.4	1920.0	2500.0	3840.0
1	1	0	f_{OSC1} /24	1365.3	1600.0	2083.3	3200.0
1	1	1	f_{OSC1} /28	1170.3	1371.4	1785.7	2742.9

The buzzer frequency can be selected from among the above 8 types that have divided the OSC1 clock.
At initial reset, these registers are set at "0".

BDTY0–BDTY2: Duty ratio selection registers (E3H•D0–D2)

Selects the duty ratio of the buzzer signal.

Table 4.12.6.3 Duty ratio settings

Level	BDTY2	BDTY1	BDTY0	Duty ratio by buzzer frequency			
				fosc1 /8 fosc1 /16	fosc1 /10 fosc1 /20	fosc1 /12 fosc1 /24	fosc1 /14 fosc1 /28
Level 1 (maximum)	0	0	0	8/16	8/20	12/24	12/28
Level 2	0	0	1	7/16	7/20	11/24	11/28
Level 3	0	1	0	6/16	6/20	10/24	10/28
Level 4	0	1	1	5/16	5/20	9/24	9/28
Level 5	1	0	0	4/16	4/20	8/24	8/28
Level 6	1	0	1	3/16	3/20	7/24	7/28
Level 7	1	1	0	2/16	2/20	6/24	6/28
Level 8 (minimum)	1	1	1	1/16	1/20	5/24	5/28

The buzzer sound level can be adjusted by selecting the duty ratio from among the above 8 types. However, when the envelope has been set to ON (ENON = "1"), this setting becomes invalid.
At initial reset, these registers are set to "0".

ENRST: Envelope reset (E0H•D2)

Resets the envelope.

When "1" is written: Reset
When "0" is written: No operation
Reading: Always "0"

The envelope is reset by writing "1" to ENRST and the duty ratio returns to level 1 (maximum).
Resetting becomes invalid when an envelope has not been added or the buzzer signal has not been output.
Since ENRST is exclusively for writing, it always becomes "0" during reading.

ENON: Envelope ON/OFF (E0H•D1)

Controls the addition of an envelope to the buzzer signal.

When "1" is written: ON
When "0" is written: OFF
Reading: Valid

By writing "1" to ENON, an envelope can be added to buzzer signal output. When "0" is written, an envelope is not added and the buzzer signal is fixed at the duty ratio selected in BDTY0–BDTY2.
At initial reset and when "1" is written to BZSHT, ENON is set to "0".

ENRTM: Envelope attenuation time selection register (E0H•D3)

Selects the envelope attenuation time that is added to the buzzer signal.

When "1" is written: 1.0 sec (125 msec × 7 = 875 msec)
When "0" is written: 0.5 sec (62.5 msec × 7 = 437.5 msec)
Reading: Valid

The attenuation time of the digital envelope is determined by the time for changing the duty ratio.
The duty ratio is changed in 125 msec (160 msec when f_{OSC1} = 50 kHz) units when "1" is written to ENRTM and in 62.5 msec (80 msec when f_{OSC1} = 50 kHz) units, when "0" is written.
This setting becomes invalid when an envelope has been set to OFF (ENON = "0").
At initial reset, this register is set to "0".

SHTPW: One-shot buzzer pulse width selection register (E1H•D0)

Selects the output duration width of the one-shot buzzer.

When "1" is written: 125 msec
When "0" is written: 31.25 msec
Reading: Valid

The one-shot buzzer output duration width is set to 125 msec (160 msec when f_{OSC1} = 50 kHz) when "1" is written to SHTPW and 31.25 msec (40 msec when f_{OSC1} = 50 kHz), when "0" is written.
This setting does not affect the normal buzzer output.
At initial reset, this register is set to "0".

BZSHT: One-shot buzzer trigger/status (E1H•D1)
Controls the one-shot buzzer output.

• ***When writing data***

When "1" is written: Trigger
When "0" is written: No operation

Writing "1" into BZSHT causes the one-shot output circuit to operate and the buzzer signal to be output. The buzzer output is automatically turned OFF after the time set by SHTPW has elapsed.
The one-shot output is only valid when the normal buzzer output is OFF (BZE = "0") status. The trigger is invalid during ON (BZE = "1") status including the one-shot output.

• ***When reading data***

When "1" is read: Busy
When "0" is read: Ready

The operation status of the one-shot output circuit can be confirmed by reading BZSHT, when the one-shot output is ON (busy), BZSHT is set to "1" and when the output is OFF (ready), it is set to "0".
At initial reset, this bit is set to "0".

BZSTP: One-shot buzzer STOP (E1H•D2)
Forcibly stops the one-shot buzzer output.

When "1" is written: Stop
When "0" is written: No operation
Reading: Constantly "0"

By writing "1" into BZSTP, the one-shot buzzer output can be stopped prior to the elapsing of the time set with SHTPW.
Writing "0" is invalid and writing "1" except during one-shot output is also invalid.
When "1" is written to BZSHT and BZSTP simultaneously, BZSTP takes precedence and one-shot output becomes stop status.
Since BZSTP is for writing only, during readout it is constantly set to "0".

4.12.7 Programming note

A hazard may occur when data of the BZE register or the buzzer frequency selection registers (BZFQ0–BZFQ2) are changed.

4.13 External Memory Access

To control external devices such as expansion of the LCD driver and static RAM, the E0C6247 can set the output port terminals and the I/O port terminals as bus signal input/output terminals for external memory access.
External bus is configured with a maximum 16-bit address bus (maximum 17 bits when read only devices only are connected), an 8-bit data bus, 4-bit chip select signal and read/write signals (read signal only when read only devices only are connected), and can be expanded externally up to a maximum of four 64K-byte (512K-bit) RAM (read/write device) or up to a maximum of four 128K-byte (1M-bit) ROM (read only device).
Figure 4.13.1 shows the external bus block diagram.

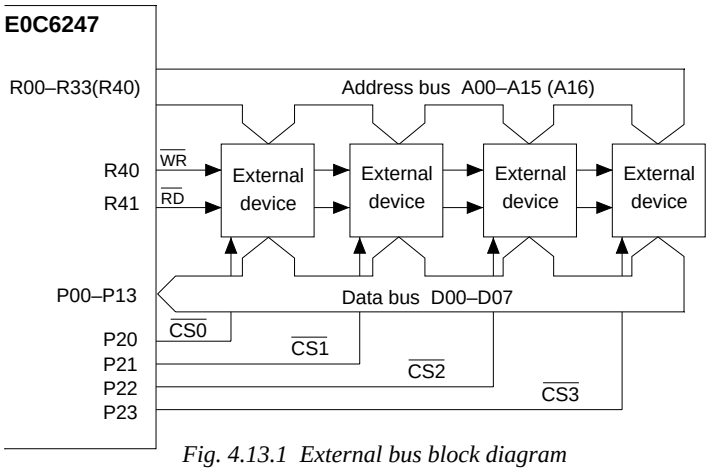


Fig. 4.13.1 External bus block diagram

Note: At initial reset, terminals that are used as input/output external bus signals are all set as general purpose output port or I/O port terminals. When the external memory access function is used, switch the function in the initial routine (set EXTMF register to "1").

4.13.1 Address bus

(1) Address bus setting

When the external memory access function is selected (EXTMF = "1"), the address bus output is assigned on the output port terminals.
Any one of four types of memory size shown in Table 4.13.1.1 can be selected by the software (MEMS1 and MEMS0 register settings). This selection decides the address bus size and the configuration of the output terminals that are used as the address bus.

Table 4.13.1.1 Setting of memory size and address bus

MEMS1	MEMS0	Memory size	Address bus
1	1	1M-bit (R only)	A00–A16
1	0	512K-bit (R/W)	A00–A15
0	1	256K-bit (R/W)	A00–A14
0	0	64K-bit (R/W)	A00–A12

Table 4.13.1.2 Configuration of output terminal depending on memory size

Terminal name	Function of terminals			
	1M-bit	512K-bit	256K-bit	64K-bit
R00–R03	A00–A03	A00–A03	A00–A03	A00–A03
R10–R13	A04–A07	A04–A07	A04–A07	A04–A07
R20–R23	A08–A11	A08–A11	A08–A11	A08–A11
R30	A12	A12	A12	A12
R31	A13	A13	A13	R31
R32	A14	A14	A14	R32
R33	A15	A15	R33	R33
R40	A16	$\overline{WR}$	$\overline{WR}$	$\overline{WR}$
R41	$\overline{RD}$	$\overline{RD}$	$\overline{RD}$	$\overline{RD}$

Output port terminals that are not used as address outputs depending on the selected memory size are not changed.
The data registers and high impedance control registers of the output port set for the address bus can be used as general purpose registers that do not affect output.
At initial reset, all the terminals above are set to the output port terminals, and they output a high level.

(2) Specifying external address

The registers A00 to A16 are set to specify external addresses. Data set in these registers are output from address bus terminals as external address data.
Registers corresponding to the address that is not used depending on the selected memory size can be used as general purpose registers. Also when the external memory access function is not used, the registers A00 to A16 can be used as general purpose registers.
At initial reset, the contents of the registers A00 to A16 are undefined, address data must be set before accessing the external memory.
The external memory access function contains the address increment function to access the external memory addresses consecutively. For this reason, when performing a consecutive access, it is only necessary to write the top address to the register A00 to A16, and writing the following addresses are not necessary.
There are two procedures to increment.

1. ***Specifying every increments using the software***
   The content of the address registers A00 to A16 is incremented (+1) by writing "1" to the ADINC register.

2. ***To perform increment automatically***
   By writing "1" to the PICON register, the address auto increment mode is set. When this mode has been set, the content of the address registers A00 to A16 is automatically incremented (+1) when the external memory is read or written.

4.13.2 Data bus

Data bus is configured with an 8-bit (D00–D07), and is assigned to the I/O ports shown in Table 4.13.2.1 when the external memory access function is selected (EXTMF = "1").

Table 4.13.2.1 Relation of I/O port and data bus

I/O port	Data bus
P00–P03	D00–A03
P10–P13	D04–D07

The data registers of the I/O ports (P00–P03, P10–P13), that are assigned as the data bus, function as the data registers for external memory access. The I/O control registers and the pull up control registers can be used as general purpose registers that do not affect output.
At initial reset, all the terminals above are set to the I/O port terminals, and the input mode (terminals are pulled up) is set.

Data is written or read in the order of low-order bits D00 to D03 (P00 to P03) then high-order bits D04 to D07 (P10 to P13). Through writing/reading operations to these registers, the chip select signal ($\overline{CS0}$–$\overline{CS3}$), write signal ($\overline{WR}$) and read signal ($\overline{RD}$) to the external memory are automatically output.
See "4.13.6 External memory read/write sequence" for the timing for data reading/writing.

• Consecutive access of data and virtual data register

Output or input of external memory data to the external data bus is done by accessing registers P00–P03 and P10–P13. It requires access of low-order data and high-order data, and is related to the increase of program steps.
Hence, the E0C6247 allows even and odd number addresses in the RAM addresses (900H–9FFH) to be logically allocated to P00–P03 and P10–P13, respectively, as virtual data; E0C6247 also makes consecutive access by LBPX and RETD instructions possible.
The memory map of this logical space is shown on Figure 4.13.2.1.

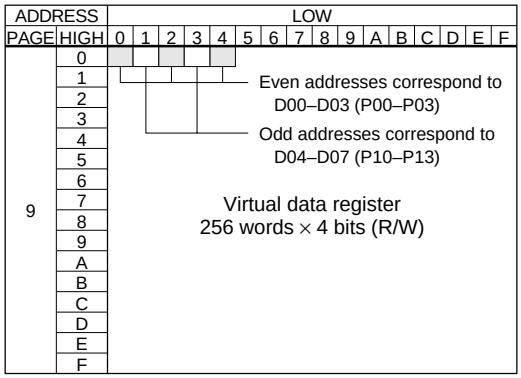


Fig. 4.13.2.1 Memory map (virtual data registers)

Note: The virtual data register is a logical space and no memory is physically allocated. The actual writing/reading through access of this space is done for registers P00–P03 and P10–P13.

4.13.3 Write signal ($\overline{WR}$) and read signal ($\overline{RD}$)

Write signal ($\overline{WR}$) and read signal ($\overline{RD}$) are assigned to the output ports shown in Table 4.13.3.1 when the external memory access function is selected (EXTMF = "1").

Table 4.13.3.1 Relation of output port and $\overline{WR}$/$\overline{RD}$ signal

Output port	$\overline{WR}$/$\overline{RD}$ signal
R40	$\overline{WR}$
R41	$\overline{RD}$

When 1M-bit (read only) is selected for the memory size, R40 is set to address A16 and the $\overline{WR}$ signal output is not set.
The data registers and high impedance registers of the output ports (R40, R41) that are assigned as the $\overline{WR}$/$\overline{RD}$ signal outputs can be used as general purpose registers that do not affect output.
At initial reset, the terminals above are set to the output port terminals, and output a high level.

The write signal ($\overline{WR}$) and the read signal ($\overline{RD}$) for the external memory are automatically output according to data writing/reading from R40 terminal and R41 terminal, respectively.

See "4.13.6 External memory read/write sequence" for the timing for data reading/writing.

4.13.4 Chip select signals ($\overline{CS0}$–$\overline{CS3}$)

The E0C6247 can output maximum four chip select signals ($\overline{CS0}$–$\overline{CS3}$). Therefore, there is no need to connect an address decoder externally.
The chip select signals are assigned to the I/O ports shown in Table 4.13.4.1 when the external memory access function is selected (EXTMF = "1").

Table 4.13.4.1 Relation of I/O port and chip select signal

I/O port	Chip select signal
P20	$\overline{CS0}$
P21	$\overline{CS1}$
P22	$\overline{CS2}$
P23	$\overline{CS3}$

The data registers of the I/O port (P20–P23) that are set to the chip select signal output are used to select the chip select signal to be output. The I/O control registers and the pull up control registers can be used as general purpose registers that do not affect output.
The assignment of chip select signals take four bits all together, it cannot be selected with one bit. The data register of the I/O port that is assigned to an unused chip select signal can be used as a general purpose register.
At initial reset, all the terminals above are set to the I/O port terminals, and the input mode (terminals are pulled up) is set.

By writing "0" to the chip select register CSx (P2x), the $\overline{CSx}$ signal goes into active standby status ($\overline{CSx}$ output enable status); writing "1" will make it output disabled. It does not mean that writing of this register directly changes a $\overline{CSx}$ signal.
Set only one $\overline{CSx}$ signal corresponding to the device to be accessed to active standby. Writing "0" to two or more CSx registers causes a bus conflict.

By writing "0" to the chip select register CSx (P2x) to correspond with the device to be accessed and then performing data reading/writing, the $\overline{CSx}$ terminal that is set to active standby will be automatically set to low level, in the same manner as $\overline{RD}$ and $\overline{WR}$ signals. Moreover, after the access, it automatically returns to high level.

4.13.5 High impedance control for external bus

High impedance control can be done for the external bus signal lines using the HZBUS register and the HZCS registers.
When "1" is written to the HZBUS register, the address bus and $\overline{RD}$/$\overline{WR}$ signal output terminals shift into high impedance status. When reading/writing of the external data bus is done in high impedance status, the address and $\overline{RD}$/$\overline{WR}$ signals are not output.
When "0" is written to the HZBUS register, the external data set in the address register is output on the address bus, and the $\overline{RD}$/$\overline{WR}$ signal output terminals go to high level. The $\overline{RD}$/$\overline{WR}$ signal becomes active (low level) during reading/writing.
When "1" is written to the HZCS register, the chip select signal ($\overline{CS0}$–$\overline{CS3}$) output terminals shift into high impedance status. However, the built-in pull up resistors go ON to avoid malfunction of external devices.
When "0" is written to the HZCS register, the chip select signal ($\overline{CS0}$–$\overline{CS3}$) output terminals go to high level. The specified chip select signal becomes active (low level) during external memory accessing.

The data bus lines shift to high impedance status except during reading/writing of external device data. There is no need to control using the software.

4.13.6 External memory read/write sequence

Reading and writing of external memory data is done by the following steps:

(1) Write the address data to the address register A00 to A15 (A16).
(It is unnecessary to write data to the address register that is unused depending on the selected memory size.)

(2) Write "0" to the chip select register CS0–CS3 (P20–P23) corresponding to the external device which will be read or written.

Note: Do not set at one time multiple $\overline{CS}$ signals to active standby.

(3) Perform data reading/writing.
When the address auto increment function is set to valid, the address is incremented (+1) after completion of reading/writing operation.

• Data reading
Data register is read in the order of: low-order 4 bits first, then high-order 4 bits.
$\overline{RD}$ signal and $\overline{CS}$ signal are automatically output at the point where the low-order 4 bits are read.
The low-order 4-bit data can be read from D00–D03 (P00–P03) and the high-order 4-bit data from D04–D07 (P10–P13), or from the even address (low order) and odd address (high order) of the 900H–9FFH addresses.

• Data writing
Data register is written in the order of: low-order 4 bits first, then high-order 4 bits.
$\overline{WR}$ signal and $\overline{CS}$ signal are automatically output at the point where the high-order 4 bits are written.
The low-order 4-bit data can be written to D00–D03 (P00–P03) and the high-order 4-bit data to D04–D07 (P10–P13), or to the even address (low order) and odd address (high order) of the 900H–9FFH addresses.
When the address auto increment function is set to be valid, consecutive writing is possible from 900H–9FFH addresses using the LBPX and RETD instructions.

(4) Write "1" to the chip select register set in step (2) above.

For high impedance control, follow the requirements of the external circuit.
Figure 4.13.6.1 shows the timing chart of external memory access.

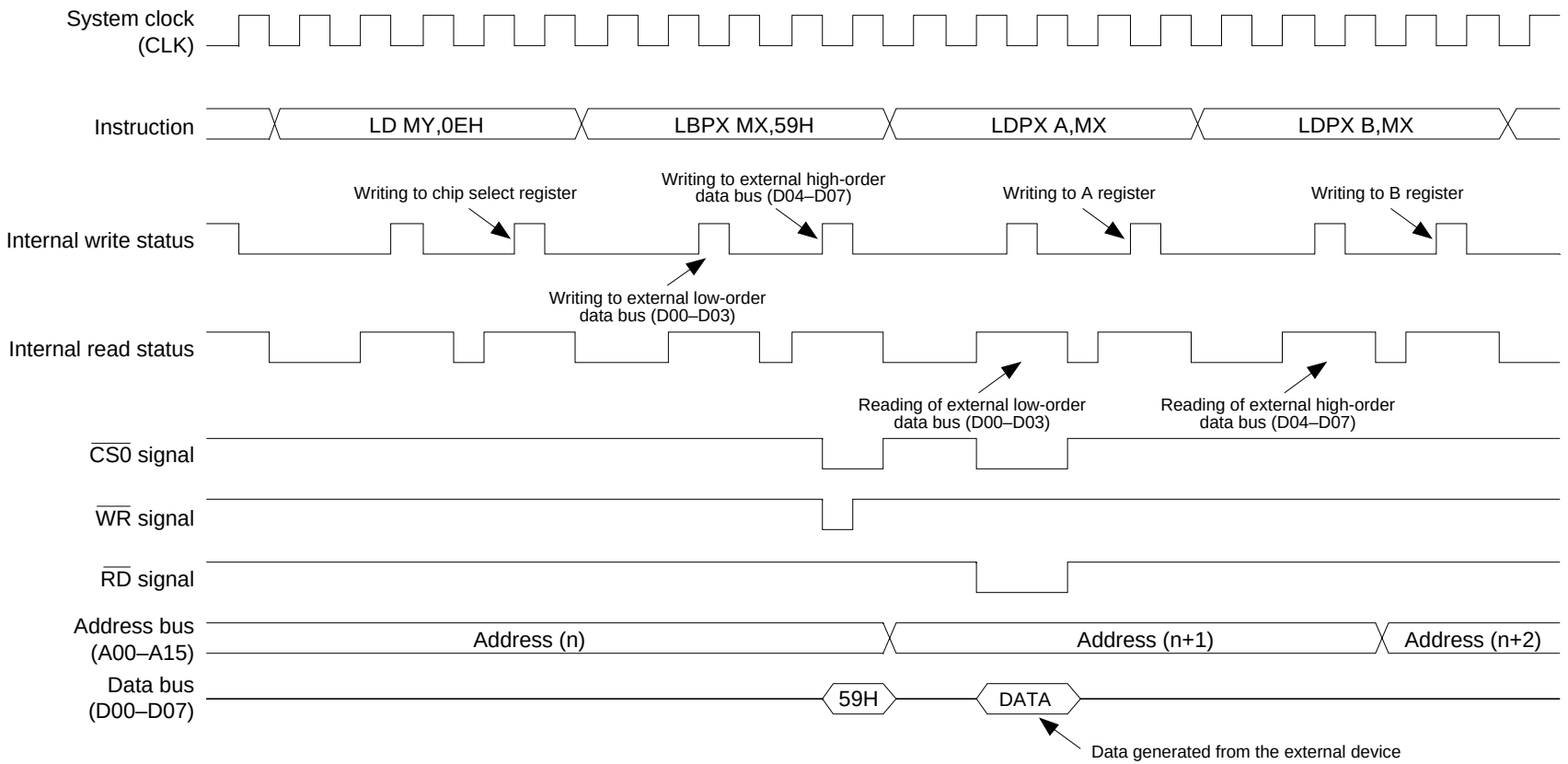


Fig. 4.13.6.1 Timing chart of external memory access

4.13.7 Control of external memory access function

Table 4.13.7.1 lists the control bits and their addresses for the external memory access function.

Table 4.13.7.1 Control bits of external memory access function

Address *7	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
98H	EXTMF	0	MEMS1	MEMS0	EXTMF	0	On	Off	External memory access function control
					0 *5	– *2			Unused
					MEMS1	0			External memory size selection: MEMS [1][0] 1 1 1M (R only) (A00–A16); 1 0 512K (R/W) (A00–A15); 0 1 256K (R/W) (A00–A14); 0 0 64K (R/W) (A00–A12)
					MEMS0	0			
	R/W	R	R/W						
99H	HZCS	HZBUS	ADINC	PICON	HZCS	0	High-Z	Output	$\overline{CS0}$–$\overline{CS3}$ output high-impedance control
					HZBUS	0	High-Z	Output	Address bus, $\overline{RD}$/$\overline{WR}$ high-impedance control
					ADINC	0	Increment	–	External memory address increment
	R/W		W	R/W	PICON	0	Auto inc.	Normal	External memory address auto increment mode
9AH	A03	A02	A01	A00	A03	– *2	1	0	External memory address A00–A03 (EXTMF = 1) Functions as a general-purpose register when EXTMF = 0.
					A02	– *2	1	0	
					A01	– *2	1	0	
	R/W				A00	– *2	1	0	
9BH	A07	A06	A05	A04	A07	– *2	1	0	External memory address A04–A07 (EXTMF = 1) Functions as a general-purpose register when EXTMF = 0.
					A06	– *2	1	0	
					A05	– *2	1	0	
	R/W				A04	– *2	1	0	
9CH	A11	A10	A09	A08	A11	– *2	1	0	External memory address A08–A11 (EXTMF = 1) Functions as a general-purpose register when EXTMF = 0.
					A10	– *2	1	0	
					A09	– *2	1	0	
	R/W				A08	– *2	1	0	
9DH	A15	A14	A13	A12	A15	– *2	1	0	External memory address A12–A15 (EXTMF = 1) Bits that are not used as an address for external memory access can also be used as a general-purpose register.
					A14	– *2	1	0	
					A13	– *2	1	0	
	R/W				A12	– *2	1	0	
9EH	0	0	0	A16	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R			R/W	0 *5	– *2			Unused
					A16	– *2	1	0	External memory address A16 *8
B2H	P03	P02	P01	P00	P03	– *2	High	Low	P00–P03 I/O port data (EXTMF = 0)
					P02	– *2	High	Low	
	D03	D02	D01	D00	P01	– *2	High	Low	
					P00	– *2	High	Low	
	R/W				D03	– *2	1	0	External memory data D00–D03 (EXTMF = 1)
					D02	– *2	1	0	
					D01	– *2	1	0	
					D00	– *2	1	0	
B6H	P13	P12	P11	P10	P13	– *2	High	Low	P10–P13 I/O port data (EXTMF = 0)
					P12	– *2	High	Low	
	D07	D06	D05	D04	P11	– *2	High	Low	
					P10	– *2	High	Low	
	R/W				D07	– *2	1	0	External memory data D04–D07 (EXTMF = 1)
					D06	– *2	1	0	
					D05	– *2	1	0	
					D04	– *2	1	0	
BAH	P23	P22	P21	P20	P23	– *2	High	Low	P20–P23 I/O port data (EXTMF = 0)
					P22	– *2	High	Low	
	CS3	CS2	CS1	CS0	P21	– *2	High	Low	
					P20	– *2	High	Low	
	R/W				CS3	– *2	Disable	Active	Chip select $\overline{CS0}$–$\overline{CS3}$ active standby (EXTMF = 1)
					CS2	– *2	Disable	Active	
					CS1	– *2	Disable	Active	
					CS0	– *2	Disable	Active	

*1 Initial value at the time of initial reset
*2 Not set in the circuit
*3 Undefined
*4 Reset (0) immediately after being read
*5 Constantly "0" when being read
*6 Refer to main manual
*7 I/O memory is allocated from page 0 to 3
*8 When other than EXTMF = 1 and a memory less than 1M bits are used, it functions as a general purpose register.

EXTMF: External memory access function control (98H•D3)

Controls the external memory access function ON or OFF.

When "1" is written: ON
When "0" is written: OFF
Reading: Valid

By writing "1" to EXTMF, the external memory access function goes ON, and the specific terminals of output ports and I/O ports are set as external signal input/output terminals. When EXTMF is "0", the external memory access function cannot be used.
At initial reset, this register is set to "0".

MEMS1, MEMS0: External memory size selection (98H•D1, D0)

Selects size of the external address bus.

Table 4.13.7.2 External memory size and address bus

MEMS1	MEMS0	Memory size	Address bus
1	1	1M-bit (R only)	A00–A16
1	0	512K-bit (R/W)	A00–A15
0	1	256K-bit (R/W)	A00–A14
0	0	64K-bit (R/W)	A00–A12

This setting is valid when EXTMF is "1".
At initial reset, this register is set to "0".

HZBUS: Bus output high impedance control (99H•D2)

Controls the high impedance of the address bus and $\overline{RD}/\overline{WR}$ signal outputs.

When "1" is written: High impedance
When "0" is written: Signal output
Reading: Valid

When "1" is written to the HZBUS register, the address bus and $\overline{RD}/\overline{WR}$ signal output terminals shift into high impedance status. When "0" is written, the external data set in the address register is output on the address bus, and the $\overline{RD}/\overline{WR}$ signal output terminals go to high level. The $\overline{RD}/\overline{WR}$ signal becomes active (low level) during reading/writing.
At initial reset, this register is set to "0".

HZCS: $\overline{CS}$ output high impedance control (99H•D3)

Controls the high impedance of the $\overline{CS0}$–$\overline{CS3}$ signal outputs.

When "1" is written: High impedance
When "0" is written: Signal output
Reading: Valid

When "1" is written to the HZCS register, the chip select signal ($\overline{CS0}$–$\overline{CS3}$) output terminals shift into high impedance status. However, the built-in pull up resistors go ON to avoid malfunction of external devices. When "0" is written to the HZCS register, the chip select signal ($\overline{CS0}$–$\overline{CS3}$) output terminals go to high level. The specified chip select signal becomes active (low level) during external memory accessing. At initial reset, this register is set to "0".

A00–A16: External memory address (9AH, 9BH, 9CH, 9DH, 9EH•D0)

Set the external memory address.

When "1" is written: Address bit high level
When "0" is written: Address bit low level
Reading: Valid

By writing "1" to Axx register, the corresponding address bit is generated as high level on the address bus; by writing "0", it is generated as low level on the address bus.
Registers corresponding to the address that is not used depending on the selected memory size can be used as general purpose registers.
At initial reset, the contents of these registers are undefined.

CS0–CS3 (P20–P23): Chip select active standby (BAH)
Sets the chip select signal to active standby status.

When "0" is written: Active standby
When "1" is written: Output disabled
Reading: Valid

By writing "0" to CSx, the $\overline{CSx}$ signal goes into active standby status; during reading/writing operation of the external memory device, it goes low.
The $\overline{CSx}$ signal is fixed at high level by writing "1".
At initial reset, the contents of these registers are undefined.

D00–D03 (P00–P03), D04–D07 (P10–P13): External memory data (B2H, B6H, or even address, odd address of 900H–9FFH)
These registers perform reading/writing for external memory data.

• ***When writing data***

When "1" is written: Data bit high level
When "0" is written: Data bit low level

By writing "1" to the Dxx register, the corresponding data bit is generated as high level on the data bus; by writing "0", it is generated as low level on the data bus.
$\overline{WR}$ signal and $\overline{CS}$ signal (that is set into active standby) are automatically output at the point where the high-order 4 bits (D04–D07) are written.

• ***When reading data***

When "1" is read: Data bit high level
When "0" is read: Data bit low level

The data on the data bus is read from the corresponding register Dxx with the high level as "1" and the low level as "0".
$\overline{RD}$ signal and $\overline{CS}$ signal (that is set into active standby) are automatically output at the point where the low-order 4 bits (D00–D03) are read.

Note: The data should be written and read in the order of low-order bits (D00–D03) then high-order bits (D04–D07).

At initial reset, the contents of these registers are undefined.

ADINC: External memory address increment (99H•D1)
Increments the external memory address.

When "1" is written: Address incremented (+1)
When "0" is written: No operation
Reading: Always "0"

When "1" is written to ADINC, the external memory address A00–A15 (A16) is incremented (+1).

PICON: External memory address auto increment mode (99H•D0)
Sets the address auto increment function.

When "1" is written: Auto increment mode
When "0" is written: Normal mode
Reading: Valid

When "1" is written to PICON, the auto increment function for the external memory address A00–A15 (A16) becomes effective. In the auto increment mode, the address is automatically incremented (+1) after high-order data (D04–D07) is written or read. When "0" is written to PICON, auto increment is not possible.
At initial reset, this register is set to "0".

4.13.8 Programming note

Be sure to data writing/reading for external memory in the order of low-order bits (D00–D03) then high-order bits (D04–D07).

4.14 SVD (Supply Voltage Detection) Circuit

4.14.1 Configuration of SVD circuit

The E0C6247 has a built-in SVD (supply voltage detection) circuit, so that the software can find when the source voltage lowers. Turning the SVD circuit ON/OFF and the SVD criteria voltage setting can be controlled through the software.
Figure 4.14.1.1 shows the configuration of the SVD circuit.

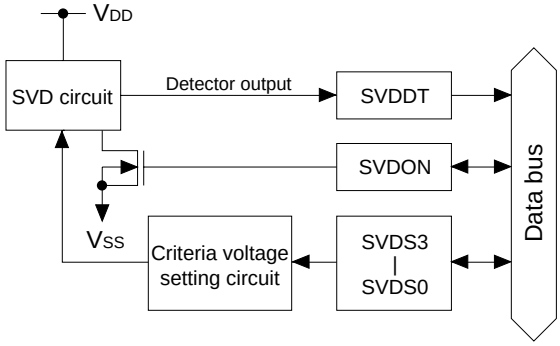


Fig. 4.14.1.1 Configuration of the SVD circuit

4.14.2 SVD operation

The SVD circuit compares the criteria voltage set by the software and the supply voltage (V_{DD}–V_{SS}) and sets its results into the SVDDT latch. By reading the data of this SVDDT latch, it can be determined by means of software whether the supply voltage is normal or has dropped.
The criteria voltage can be set for the 16 types shown in Table 4.14.2.1 by SVDS3–SVDS0.

Table 4.14.2.1 Criteria voltage setting

SVDS3	SVDS2	SVDS1	SVDS0	Criteria voltage	SVDS3	SVDS2	SVDS1	SVDS0	Criteria voltage
0	1	1	1	1.60 V	1	1	1	1	2.60 V
0	1	1	0	1.40 V	1	1	1	0	2.50 V
0	1	0	1	1.30 V	1	1	0	1	2.30 V
0	1	0	0	1.25 V	1	1	0	0	2.20 V
0	0	1	1	1.20 V	1	0	1	1	2.10 V
0	0	1	0	1.15 V	1	0	1	0	2.05 V
0	0	0	1	1.10 V	1	0	0	1	2.00 V
0	0	0	0	1.05 V	1	0	0	0	1.95 V

When SVDON is set to "1", source voltage detection by the SVD circuit is executed. As soon as SVDON is reset to "0", the result is loaded to in the SVDDT register and SVD circuit goes OFF.
To obtain a stable SVD detection result, the SVD circuit must be on for at least l00 µsec. So, to obtain the SVD detection result, follow the programming sequence below.

① Set SVDON to "1"
② Maintain for 100 µsec minimum
③ Set SVDON to "0"
④ Read SVDDT

However, when f_{OSC1} (32.768 kHz, 38.4 kHz or 50 kHz) is selected for CPU system clock, the instruction cycles are long enough, so there is no need to worry about maintaining 100 µsec or more for SVDON = "1" in the software.
When SVD is on, the IC draws a large current, so keep SVD off unless it is.

4.14.3 Control of SVD circuit

Table 4.14.3.1 shows the control bits and their addresses for the SVD circuit.

Table 4.14.3.1 Control bits for SVD circuit

Address *7	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
80H	SVDS3	SVDS2	SVDS1	SVDS0	SVDS3	0			SVD criteria voltage setting
					SVDS2	0			SVDS [3][2][1][0] Voltage (V) / SVDS [3][2][1][0] Voltage (V)
					SVDS1	0			0 1 1 1 1.60 / 1 1 1 1 2.60
	R/W				SVDS0	0			0 1 1 0 1.40 / 1 1 1 0 2.50
									0 1 0 1 1.30 / 1 1 0 1 2.30
									0 1 0 0 1.25 / 1 1 0 0 2.20
									0 0 1 1 1.20 / 1 0 1 1 2.10
									0 0 1 0 1.15 / 1 0 1 0 2.05
									0 0 0 1 1.10 / 1 0 0 1 2.00
									0 0 0 0 1.05 / 1 0 0 0 1.95
81H	0	0	SVDDT	SVDON	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R			R/W	SVDDT	0	Low	Normal	SVD evaluation data
					SVDON	0	On	Off	SVD circuit On/Off

*1 Initial value at the time of initial reset
*2 Not set in the circuit
*3 Undefined
*4 Reset (0) immediately after being read
*5 Constantly "0" when being read
*6 Refer to main manual
*7 I/O memory is allocated in page 0 to 3

SVDS3–SVDS0: SVD criteria voltage setting (80H)
Criteria voltage for SVD is set as shown in Table 4.14.2.1.
At initial reset, these registers are set to "0".

SVDON: SVD ON/OFF (81H•D0)
Turns the SVD circuit ON and OFF.

When "1" is written: SVD circuit ON
When "0" is written: SVD circuit OFF
Reading: Valid

When SVDON is set to "1", source voltage detection by the SVD circuit is executed. As soon as SVDON is reset to "0", the result is loaded to in the SVDDT register. To obtain a stable SVD detection result, the SVD circuit must be on for at least l00 µsec.
At initial reset, this register is set to "0".

SVDDT: SVD data (81H•D1)
This is the result of supply voltage detection.

When "0" is read: Supply voltage (V_{DD}–V_{SS}) ≥ Criteria voltage
When "1" is read: Supply voltage (V_{DD}–V_{SS}) < Criteria voltage
Writing: Invalid

The result of supply voltage detection at time of SVDON is set to "0" can be read from this register.
At initial reset, SVDDT is set to "0".

4.14.4 Programming notes

(1) To obtain a stable SVD detection result, the SVD circuit must be on for at least l00 µsec. So, to obtain the SVD detection result, follow the programming sequence below.

① Set SVDON to "1"
② Maintain for 100 µsec minimum
③ Set SVDON to "0"
④ Read SVDDT

However, when f_{OSC1} (32.768 kHz, 38.4 kHz or 50 kHz) is selected for CPU system clock, the instruction cycles are long enough, so there is no need to worry about maintaining 100 µsec or more for SVDON = "1" in the software.

(2) The SVD circuit should normally be turned OFF as the consumption current of the IC becomes large when it is ON.

4.15 Interrupt and HALT

<Interrupt types>

The E0C6247 provides the following interrupt settings, each of which is maskable.

External interrupt:
- Input interrupt (2 systems)

Internal interrupt:
- Timer interrupt (4 systems)
- Programmable timer interrupt (1 system)
- Serial interface interrupt (3 systems)

To authorize interrupt, the interrupt flag must be set to "1" (EI) and the necessary related interrupt mask registers must be set to "1" (enable).
When an interrupt occurs the interrupt flag is automatically reset to "0" (DI), and interrupts after that are inhibited.
Figure 4.15.1 shows the configuration of the interrupt circuit.

<HALT>

The E0C6247 has HALT functions that considerably reduce the current consumption when it is not necessary.
The CPU enters the HALT status when the HALT instruction is executed.
In the HALT status, the operation of the CPU is stopped. However, the oscillation circuit operates. Reactivating the CPU from the HALT status is done by generating an interrupt request. When it does not reactivate upon an interrupt request, the watchdog timer will cause it to restart from the initial reset status.

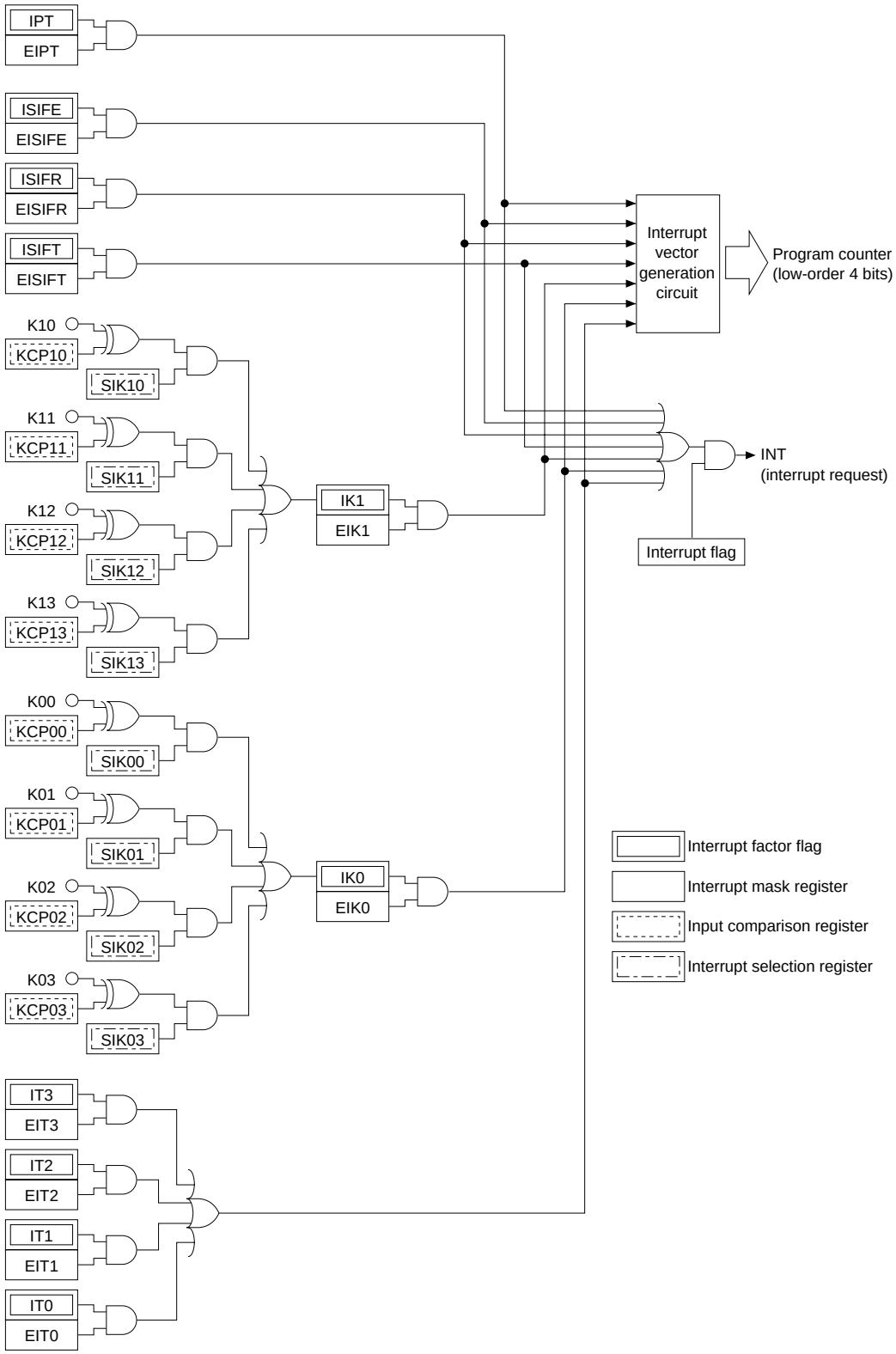


Fig. 4.15.1 Configuration of the interrupt circuit

4.15.1 Interrupt factor

Table 4.15.1.1 shows the factors for generating interrupt requests.

The interrupt flags are set to "1" depending on the corresponding interrupt factors.
The CPU operation is interrupted when any of the conditions below set an interrupt factor flag to "1".

- The corresponding mask register is "1" (enabled)
- The interrupt flag is "1" (EI)

The interrupt factor flag is a read-only register, but can be reset to "0" when the register data is read out.
At initial reset, the interrupt factor flags are reset to "0".

Table 4.15.1.1 Interrupt factors

Interrupt factor	Interrupt factor flag	
Programmable timer (counter = 0)	IPT	(F8H•D0)
Serial interface (error generation)	ISIFE	(F9H•D2)
Serial interface (data receiving completion)	ISIFR	(F9H•D0)
Serial interface (data transmitting completion)	ISIFT	(F9H•D1)
K10–K13 input (falling or rising edge)	IK1	(FAH•D0)
K00–K03 input (falling or rising edge)	IK0	(FBH•D0)
Clock timer 1 Hz (falling edge)	IT3	(FCH•D3)
Clock timer 2 Hz (falling edge)	IT2	(FCH•D2)
Clock timer 8 Hz (falling edge)	IT1	(FCH•D1)
Clock timer 16 Hz (falling edge)	IT0	(FCH•D0)

Note: Reading of interrupt factor flags is available at EI, but be careful in the following cases.
If the interrupt mask register value corresponding to the interrupt factor flags to be read is set to "1", an interrupt request will be generated by the interrupt factor flags set timing, or an interrupt request will not be generated. Be very careful when interrupt factor flags are in the same address.

4.15.2 Interrupt mask

The interrupt factor flags can be masked by the corresponding interrupt mask registers.
The interrupt mask registers are read/write registers. They are enabled (interrupt authorized) when "1" is written to them, and masked (interrupt inhibited) when "0" is written to them.
At initial reset, the interrupt mask register is set to "0".
Table 4.15.2.1 shows the correspondence between interrupt mask registers and interrupt factor flags.

Table 4.15.2.1 Interrupt mask registers and interrupt factor flags

Interrupt mask register		Interrupt factor flag	
EIPT	(F0H•D0)	IPT	(F8H•D0)
EISIFE	(F1H•D2)	ISIFE	(F9H•D2)
EISIFR	(F1H•D0)	ISIFR	(F9H•D0)
EISIFT	(F1H•D1)	ISIFT	(F9H•D1)
EIK1	(F2H•D0)	IK1	(FAH•D0)
EIK0	(F3H•D0)	IK0	(FBH•D0)
EIT3	(F4H•D3)	IT3	(FCH•D3)
EIT2	(F4H•D2)	IT2	(FCH•D2)
EIT1	(F4H•D1)	IT1	(FCH•D1)
EIT0	(F4H•D0)	IT0	(FCH•D0)

Note: Write the interrupt mask register only in the DI status (interrupt flag = "0"). Writing during EI status (interrupt flag = "1") will cause malfunction.

4.15.3 Interrupt vector

When an interrupt request is input to the CPU, the CPU begins interrupt processing. After the program being executed is terminated, the interrupt processing is executed in the following order.

① The address data (value of program counter) of the program to be executed next is saved in the stack area (RAM).

② The interrupt request causes the value of the interrupt vector (page 1, 02H–0EH) to be set in the program counter.

③ The program at the specified address is executed (execution of interrupt processing routine by software).

Table 4.15.3.1 shows the correspondence of interrupt requests and interrupt vectors.

Note: The processing in ① and ② above take 12 cycles of the CPU system clock.

Table 4.15.3.1 Interrupt request and interrupt vectors

Interrupt vector (every Bank)	Interrupt factor	Priority
102H	Programmable timer	High
104H	Serial I/F (error generation)	↑
106H	Serial I/F (receiving completion)	
108H	Serial I/F (transmitting completion)	
10AH	K10–K13 input	
10CH	K00–K03 input	↓
10EH	Clock timer	Low

The four low-order bits of the program counter are indirectly addressed through the interrupt request.

4.15.4 Control of interrupt

Tables 4.15.4.1(a) and (b) show the interrupt control bits and their addresses.

Table 4.15.4.1(a) Control bits of interrupt (1)

Address *7	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
90H	SIK03	SIK02	SIK01	SIK00	SIK03	0	Enable	Disable	K00–K03 interrupt selection register
					SIK02	0	Enable	Disable	
					SIK01	0	Enable	Disable	
	R/W				SIK00	0	Enable	Disable	
92H	KCP03	KCP02	KCP01	KCP00	KCP03	1	↓	↑	K00–K03 input comparison register
					KCP02	1	↓	↑	
					KCP01	1	↓	↑	
	R/W				KCP00	1	↓	↑	
94H	SIK13	SIK12	SIK11	SIK10	SIK13	0	Enable	Disable	K10–K13 interrupt selection register
					SIK12	0	Enable	Disable	
					SIK11	0	Enable	Disable	
	R/W				SIK10	0	Enable	Disable	
96H	KCP13	KCP12	KCP11	KCP10	KCP13	1	↓	↑	K10–K13 input comparison register
					KCP12	1	↓	↑	
					KCP11	1	↓	↑	
	R/W				KCP10	1	↓	↑	

*1 Initial value at the time of initial reset
*2 Not set in the circuit
*3 Undefined
*4 Reset (0) immediately after being read
*5 Constantly "0" when being read
*6 Refer to main manual
*7 I/O memory is allocated from page 0 to 3

Table 4.15.4.1(b) Control bits of interrupt (2)

Address *7	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
F0H	0	0	0	EIPT	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R			R/W	0 *5	– *2			Unused
					EIPT	0	Enable	Mask	Interrupt mask register (programmable timer)
F1H	0	EISIFE	EISIFT	EISIFR	0 *5	– *2			Unused
					EISIFE	0	Enable	Mask	Interrupt mask register (serial I/F error)
	R	R/W			EISIFT	0	Enable	Mask	Interrupt mask register (serial I/F transmitting)
					EISIFR	0	Enable	Mask	Interrupt mask register (serial I/F receiving)
F2H	0	0	0	EIK1	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R			R/W	0 *5	– *2			Unused
					EIK1	0	Enable	Mask	Interrupt mask register (K10–K13)
F3H	0	0	0	EIK0	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R			R/W	0 *5	– *2			Unused
					EIK0	0	Enable	Mask	Interrupt mask register (K00–K03)
F4H	EIT3	EIT2	EIT1	EIT0	EIT3	0	Enable	Mask	Interrupt mask register (clock timer 1 Hz)
					EIT2	0	Enable	Mask	Interrupt mask register (clock timer 2 Hz)
	R/W				EIT1	0	Enable	Mask	Interrupt mask register (clock timer 8 Hz)
					EIT0	0	Enable	Mask	Interrupt mask register (clock timer 16 Hz)
									* When f_{OSC1} = 50 kHz: 16 Hz → 12.5 Hz
F8H	0	0	0	IPT	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R				0 *5	– *2			Unused
					IPT *4	0	Yes	No	Interrupt factor flag (programmable timer)
F9H	0	ISIFE	ISIFT	ISIFR	0 *5	– *2			Unused
					ISIFE*4	0	Yes	No	Interrupt factor flag (serial I/F error)
	R				ISIFT*4	0	Yes	No	Interrupt factor flag (serial I/F transmitting)
					ISIFR*4	0	Yes	No	Interrupt factor flag (serial I/F receiving)
FAH	0	0	0	IK1	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R				0 *5	– *2			Unused
					IK1 *4	0	Yes	No	Interrupt factor flag (K10–K13)
FBH	0	0	0	IK0	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R				0 *5	– *2			Unused
					IK0 *4	0	Yes	No	Interrupt factor flag (K00–K03)
FCH	IT3	IT2	IT1	IT0	IT3 *4	0	Yes	No	Interrupt factor flag (clock timer 1 Hz)
					IT2 *4	0	Yes	No	Interrupt factor flag (clock timer 2 Hz)
	R				IT1 *4	0	Yes	No	Interrupt factor flag (clock timer 8 Hz)
					IT0 *4	0	Yes	No	Interrupt factor flag (clock timer 16 Hz)
									* When f_{OSC1} = 50 kHz: 16 Hz → 12.5 Hz

*1 Initial value at the time of initial reset
*2 Not set in the circuit
*3 Undefined
*4 Reset (0) immediately after being read
*5 Constantly "0" when being read
*6 Refer to main manual
*7 I/O memory is allocated from page 0 to 3

EIPT: **Interrupt mask register (F0H•D0)**
IPT: **Interrupt factor flag (F8H•D0)**
..... See Section 4.10, "Programmable Timer".

EISIFE: **Interrupt mask register (F1H•D2)**
EISIFR: **Interrupt mask register (F1H•D0)**
EISIFT: **Interrupt mask register (F1H•D1)**
ISIFE: **Interrupt factor flag (F9H•D2)**
ISIFR: **Interrupt factor flag (F9H•D0)**
ISIFT: **Interrupt factor flag (F9H•D1)**
..... See Section 4.11, "Serial Interface".

KCP13–KCP10: **Input comparison registers (96H)**
KCP03–KCP00: **Input comparison registers (92H)**
SIK13–SIK10: **Interrupt selection registers (94H)**
SIK03–SIK00: **Interrupt selection registers (90H)**
EIK1: **Interrupt mask register (F2H•D0)**
EIK0: **Interrupt mask register (F3H•D0)**
IK1: **Interrupt factor flag (FAH•D0)**
IK0: **Interrupt factor flag (FBH•D0)**
..... See Section 4.5, "Input Ports".

EIT3, EIT2, EIT1, EIT0: **Interrupt mask registers (F4H)**
IT3, IT2, IT1, IT0: **Interrupt factor flags (FCH)**
..... See Section 4.9, "Clock Timer".

4.15.5 Programming notes

(1) The interrupt factor flags are set when the timing condition is established, even if the interrupt mask registers are set to "0".

(2) Write the interrupt mask register only in the DI status (interrupt flag = "0"). Writing during EI status (interrupt flag = "1") will cause malfunction.

(3) Reading of interrupt factor flags is available at EI, but be careful in the following cases.
If the interrupt mask register value corresponding to the interrupt factor flags to be read is set to "1", an interrupt request will be generated by the interrupt factor flags set timing, or an interrupt request will not be generated. Be very careful when interrupt factor flags are in the same address.

(4) The interrupt vector address will be an interrupt vector within the bank that is specified by the program counter when an interrupt occurs.

CHAPTER 5 SUMMARY OF NOTES

5.1 Notes for Low Current Consumption

The E0C6247 contains control registers for each of the circuits so that current consumption can be lowered. These control registers lower the current consumption through programs that operate the circuits at the minimum levels.
The following text explains the circuits that can control operation and their control registers. Refer to these when putting programs together.

Table 5.1.1 Circuits and control registers

Circuit (and Item)	Control register	Order of current consumption
CPU	HALT instruction	See electrical characteristics (Chapter 7)
CPU operating frequency	CLKCHG, OSCC	
Oscillation system regulated voltage circuit	VDC1, VDC0	
LCD system voltage circuit	LPWR	
Voltage doubler/halver	DBON, HLON, VDSEL, VCSEL	
SVD circuit	SVDON	Several tens µA

Below are the circuit statuses at initial reset.

CPU:
Operating status

CPU operating frequency:
Low speed side (CLKCHG = "0"),
OSC3 oscillation circuit OFF status (OSCC = "0")

Oscillation system regulated voltage circuit:
Low speed side 1.2 V (VDC1, VDC0 = "0")

LCD system voltage circuit:
OFF status (LPWR = "0")

Voltage doubler/halver:
Regulated voltage circuit is driven with V_{DD},
Normal mode (DBON = "0", HLON = "0", VDSEL = "0", VCSEL = "0")

SVD circuit:
OFF status (SVDON = "0")

Also, be careful about panel selection because the current consumption can differ by the order of several µA on account of the LCD panel characteristics.

5.2 Summary of Notes by Function

Here, the cautionary notes are summed up by function category. Keep these notes well in mind when programming.

Memory

Memory is not mounted in unused area within the memory map and in memory area not indicated in this manual. For this reason, normal operation cannot be assured for programs that have been prepared with access to these areas.

Power supply and operating mode

(1) When operating with 0.9–1.25 V supply voltage, the boost mode must be set in the initial routine before controlling the peripheral circuits.

(2) When the supply voltage is out of the specified voltage range of an operating mode, do not switch into the operating mode. It may cause a malfunction or increase current consumption.

(3) Do not set HLON (halves) and DBON (doubling) to "1" at the same time.

(4) When switching from the normal mode to the boost/reduce mode, VDSEL should be set to "1" wait 100 msec or more for V_{D2} to stabilize after setting DBON or HLON to "1".

(5) When switching from the boost/reduce mode to the normal mode, use separate instructions to switch the mode (VDSEL = "0" or VCSEL = "0") and turn the voltage doubler/halver off (HLON = "0" or DBON = "0"). Simultaneous processing with a single instruction may cause malfunction.

Watchdog timer

When the watchdog timer is being used, the software must reset it within 3-second cycles.

Oscillation circuit

(1) When switching the CPU system clock from OSC1 to OSC3, set V_{D1} and the operating mode before turning the OSC3 oscillation ON. After that maintain 2.5 msec or more, and then turn the OSC3 oscillation ON.
When switching from OSC3 to OSC1, set V_{D1} and the operating mode after switching to OSC1 and turning the OSC3 oscillation OFF.

(2) When switching V_{D1} from 1.2 V to 2.1 V, or vice versa, be sure to hold the 1.4 V setting for more than 2.5 msec or more first for voltage stabilization.

(3) It takes at least 5 msec from the time the OSC3 oscillation circuit goes ON until the oscillation stabilizes. Consequently, when switching the CPU operation clock from OSC1 to OSC3, do this after a minimum of 5 msec have elapsed since the OSC3 oscillation went ON.
Further, the oscillation stabilization time varies depending on the external oscillator characteristics and conditions of use, so allow ample margin when setting the wait time.

(4) When switching the clock form OSC3 to OSC1, use a separate instruction for switching the OSC3 oscillation OFF. An error in the CPU operation can result if this processing is performed at the same time by the one instruction.

(5) Switching the operating voltage when the supply voltage is lower than the set voltage (that can generate V_{D1}) may cause a malfunction. Switch the operating voltage only after making sure that supply voltage is more than the set voltage using the SVD circuit.

(6) The OSC1 oscillation circuit deal with four types of crystal oscillators (32.768 kHz, 38.4 kHz, 50 kHz or 76.8 kHz). To operate the timer and other circuits properly, the prescaler should be selected according to the frequency of the connected oscillator.

Input ports

(1) When input ports are changed from low to high by pull up resistor, the rise of the waveform is delayed on account of the time constant of the pull up resistor and input gate capacitance. Hence, when fetching input ports, set an appropriate wait time.
Particular care needs to be taken of the key scan during key matrix configuration.
Make this waiting time the amount of time or more calculated by the following expression.
$10 \times C \times R$
C: terminal capacitance 5 pF + parasitic capacitance ? pF
R: pull up resistance 300 kΩ

(2) The K02 terminal functions as the clock input terminal for the programmable timer, and the input signal is combined with the input port and the programmable timer. Consequently, when the K02 terminal is set to the clock input terminal for the programmable timer, take care of the interrupt setting.

I/O ports

(1) When in the input mode, I/O ports are changed from low to high by pull up resistor, the rise of the waveform is delayed on account of the time constant of the pull up resistor and input gate capacitance. Hence, when fetching input ports, set an appropriate wait time.
Particular care needs to be taken of the key scan during key matrix configuration.
Make this waiting time the amount of time or more calculated by the following expression.
$10 \times C \times R$
C: terminal capacitance 5 pF + parasitic capacitance ? pF
R: pull up resistance 300 kΩ

(2) When special output has been selected, a hazard may occur when the signal is turned ON or OFF.

(3) When f_{OSC3} is selected for the FOUT output clock, it is necessary to turn the OSC3 oscillation ON before output.

(4) When Nch open drain has been selected for the P10–P13 output specifications by the mask option and during output mode, read data from the P10–P13 registers (address B6H•D0–D3) may differ from the data written to them.

LCD driver

Because at initial reset, the contents of display memory and LC3–LC0 (LCD contrast) are undefined, there is need to initialize by the software. Furthermore, take care of the registers LPWR and ALOFF because these are set so that the display goes OFF.

Clock timer

(1) The prescaler must be set correctly to suit the crystal oscillator to be used for the OSC1 oscillation circuit.

(2) Be sure to data reading in the order of low-order data (TM0–TM3) then high-order data (TM4–TM7).

(3) When the clock timer has been reset, the interrupt factor flag (IT) may sometimes be set to "1". Consequently, perform flag reading (reset the flag) as necessary at reset.

Programmable timer

(1) Be sure to data reading in the order of low-order data (PT0–PT3) then high-order data (PT4–PT7).

(2) When data of reload registers is set at "00H", the down-counter becomes a 256-value counter.

Serial interface

(1) Be sure to initialize the serial interface mode in the transmitting/receiving disable status (TXEN = RXEN = "0").

(2) Do not perform double trigger (writing "1") to TXTRG (RXTRG) when the serial interface is in the transmitting (receiving) operation.

(3) In the clock synchronous mode, since one clock line ($\overline{SCLK}$) is shared for both transmitting and receiving, transmitting and receiving cannot be performed simultaneously.
Consequently, be sure not to write "1" to RXTRG (TXTRG) when TXTRG (RXTRG) is "1".

(4) When a parity error or flaming error is generated during receiving in the asynchronous mode, the receiving error interrupt factor flag ISIFE is set to "1" prior to the receiving complete interrupt factor flag ISIFR for the time indicated in Table 5.2.1. Consequently, you should reset the receiving complete interrupt factor flag ISIFR to "0" by providing a wait time in error processing routines and similar routines.
When an overrun error is generated, the receiving complete interrupt factor flag ISIFR is not set to "1" and a receiving complete interrupt is not generated.

Table 5.2.1 Time difference between ISIFE and ISIFR on error generation

Clock source	Time difference
CPU clock / n	1/2 cycles of CPU clock / n
Programmable timer × 1/2	1 cycle of programmable timer underflow

(5) When the demultiplied signal of the OSC3 oscillation circuit is made the clock source, it is necessary to turn the OSC3 oscillation ON, prior to using the serial interface.
A time interval of 5 msec, from the turning ON of the OSC3 oscillation circuit to until the oscillation stabilizes, is necessary, due to the oscillation element that is used. Consequently, you should allow an adequate waiting time after turning ON of the OSC3 oscillation, before starting transmitting/receiving of serial interface. (The oscillation start time will vary somewhat depending on the oscillator and on the externally attached parts. Refer to the oscillation start time example indicated in Chapter 7, "ELECTRICAL CHARACTERISTICS".)
At initial reset, the OSC3 oscillation circuit is set to OFF status.

Sound generator

A hazard may occur when data of the BZE register or the buzzer frequency selection registers (BZFQ0–BZFQ2) are changed.

External memory access

Be sure to data writing/reading for external memory in the order of low-order bits (D00–D03) then high-order bits (D04–D07).

SVD circuit

(1) To obtain a stable SVD detection result, the SVD circuit must be on for at least l00 μsec. So, to obtain the SVD detection result, follow the programming sequence below.

① Set SVDON to "1"
② Maintain for 100 μsec minimum
③ Set SVDON to "0"
④ Read SVDDT

However, when f_{OSC1} (32.768 kHz, 38.4 kHz or 50 kHz) is selected for CPU system clock, the instruction cycles are long enough, so there is no need to worry about maintaining 100 μsec or more for SVDON = "1" in the software.

(2) The SVD circuit should normally be turned OFF as the consumption current of the IC becomes large when it is ON.

Interrupt

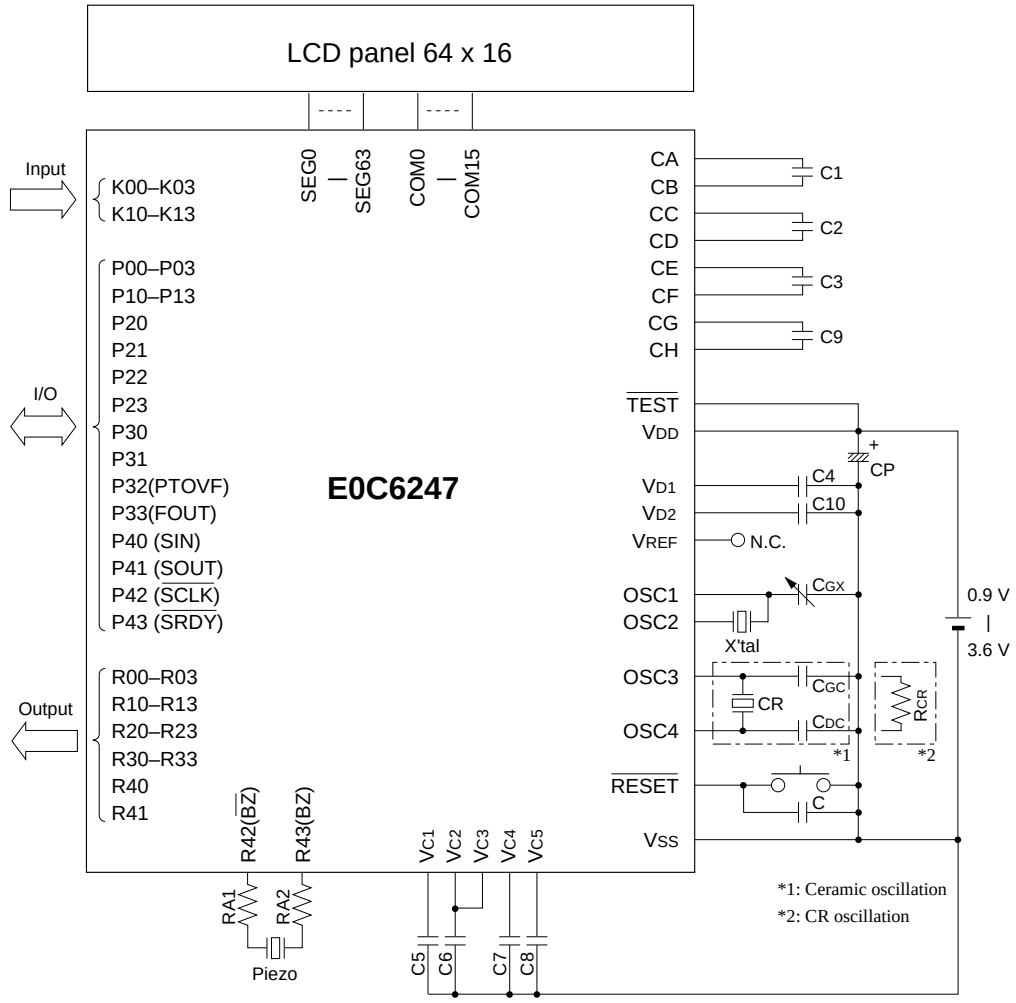
(1) The interrupt factor flags are set when the timing condition is established, even if the interrupt mask registers are set to "0".

(2) Write the interrupt mask register only in the DI status (interrupt flag = "0"). Writing during EI status (interrupt flag = "1") will cause malfunction.

(3) Reading of interrupt factor flags is available at EI, but be careful in the following cases.
If the interrupt mask register value corresponding to the interrupt factor flags to be read is set to "1", an interrupt request will be generated by the interrupt factor flags set timing, or an interrupt request will not be generated. Be very careful when interrupt factor flags are in the same address.

(4) The interrupt vector address will be an interrupt vector within the bank that is specified by the program counter when an interrupt occurs.

CHAPTER 6 BASIC EXTERNAL WIRING DIAGRAM



X'tal	Crystal oscillator	32.768 kHz / 38.4 kHz / 50 kHz / 76.8 kHz, CI (MAX) = 35 kΩ
CGX	Trimmer capacitor	5–25 pF
CR	Ceramic oscillator	1 MHz (3.0 V)
CGC	Gate capacitor	100 pF
CDC	Drain capacitor	100 pF
RCR	Resistor for CR oscillation	160 kΩ (200 kHz), 33 kΩ (1 MHz)
RA1, RA2	Protection resistors	100 Ω
C1–C8	Capacitors	0.2 µF
C9, C10	Capacitors	0.4 µF
CP	Capacitor	3.3 µF

Note: The above table is simply an example, and is not guaranteed to work.

CHAPTER 7 ELECTRICAL CHARACTERISTICS

7.1 Absolute Maximum Rating

(V_{DD} = 0 V)

Item	Symbol	Rated value	Unit
Power voltage	V_{DD}	-0.5 to 7.0	V
Input voltage (1)	V_I	-0.5 to V_{DD} + 0.3	V
Input voltage (2)	V_{IOSC}	-0.5 to V_{D1} + 0.3	V
Permissible total output current *1	ΣI_{VDD}	10	mA
Operating temperature	Topr	-20 to 70	°C
Storage temperature	Tstg	-65 to 150	°C
Soldering temperature / Time	Tsol	260°C, 10sec (lead section)	–
Allowable dissipation *2	P_D	250	mW

*1 The permissible total output current is the sum total of the current (average current) that simultaneously flows from the output pins (or is drawn in).

*2 In case of plastic package (QFP8-160pin).

7.2 Recommended Operating Conditions

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Power voltage	V_{DD}	V_{SS} = 0 V	Boost mode (OSC3: OFF)	0.9	1.1	1.25	V
			Boost mode (OSC3: ON *1)	0.9	1.5	2.2	V
			Normal mode (OSC3: OFF)	1.25	3.0	3.6	V
			Normal mode (OSC3: ON *2)	2.2	3.0	3.6	V
			Reduce mode (OSC3: OFF)	2.6	3.0	3.6	V
Oscillation frequency (1)	f_{OSC1}	Any one is selected		–	32.768	–	kHz
				–	38.4	–	kHz
				–	50.0	–	kHz
				–	76.8	–	kHz
Oscillation frequency (2)	f_{OSC3}	Either one is selected	VDC0, 1 = "1"	50	200	260	kHz
		Duty 50±5%	VDC0, 1 = "2" or "3"	50	1,000	1,200	kHz

*1 1 MHz oscillation cannot be performed.

*2 200 kHz or 1 MHz oscillation can be performed.

7.3 DC Characteristics

Unless otherwise specified:

V_{DD} = 1.5 V, V_{SS} = 0 V, f_{OSC1} = 32.768 kHz, Ta = 25°C, V_{D1}/V_{C1}/V_{C2}/V_{C4}/V_{C5} are internal voltage, C1–C8 = 0.2 µF, C9–C10 = 0.4 µF

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
High level input voltage (1)	V_{IH1}		K00–03, K10–13 P00–03, P10–13 P20–23, P30–33 P40–43	0.8·V_{DD}		V_{DD}	V
High level input voltage (2)	V_{IH2}		$\overline{RESET}$, $\overline{TEST}$	0.9·V_{DD}		V_{DD}	V
Low level input voltage (1)	V_{IL1}		K00–03, K10–13 P00–03, P10–13 P20–23, P30–33 P40–43	0		0.2·V_{DD}	V
Low level input voltage (2)	V_{IL2}		$\overline{RESET}$, $\overline{TEST}$	0		0.1·V_{DD}	V
High level input current	I_{IH}	V_{IH} = 1.5 V	K00–03, K10–13 P00–03, P10–13 P20–23, P30–33 P40–43, $\overline{RESET}$, $\overline{TEST}$	0		0.5	µA
Low level input current (1)	I_{IL1}	V_{IL1} = V_{SS} Without pull up resistor	K00–03, K10–13 P00–03, P10–13 P20–23, P30–33 P40–43, $\overline{RESET}$, $\overline{TEST}$	-0.5		0	µA
Low level input current (2)	I_{IL2}	V_{IL2} = V_{SS} With pull up resistor	K00–03, K10–13 P00–03, P10–13 P20–23, P30–33 P40–43, $\overline{RESET}$, $\overline{TEST}$	-8	-5	-3	µA
High level output current	I_{OH1}	V_{OH1} = 0.9·V_{DD}	R00–03, R10–13 R20–23, R30–33 R40–43 P00–03, P10–13 P20–23, P30–33 P40–43			-0.3	mA
Low level output current	I_{OL1}	V_{OL1} = 0.1·V_{DD}	R00–03, R10–13 R20–23, R30–33 R40–43 P00–03, P10–13 P20–23, P30–33 P40–43	0.7			mA
Common output current	I_{OH2}	V_{OH2} = V_{C5} - 0.05 V	COM0–15			-30	µA
	I_{OL2}	V_{OL2} = V_{SS} + 0.05 V		30			µA
Segment output current	I_{OH3}	V_{OH3} = V_{C5} - 0.05 V	SEG0–63			-10	µA
	I_{OL3}	V_{OL3} = V_{SS} + 0.05 V		10			µA

Unless otherwise specified:

V_{DD} = 3.0 V, V_{SS} = 0 V, f_{OSC1} = 32.768 kHz, Ta = 25°C, V_{D1}/V_{C1}/V_{C2}/V_{C4}/V_{C5} are internal voltage, C1–C8 = 0.2 µF, C9–C10 = 0.4 µF

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
High level input voltage (1)	V_{IH1}		K00–03, K10–13 P00–03, P10–13 P20–23, P30–33 P40–43	0.8·V_{DD}		V_{DD}	V
High level input voltage (2)	V_{IH2}		$\overline{RESET}$, $\overline{TEST}$	0.9·V_{DD}		V_{DD}	V
Low level input voltage (1)	V_{IL1}		K00–03, K10–13 P00–03, P10–13 P20–23, P30–33 P40–43	0		0.2·V_{DD}	V
Low level input voltage (2)	V_{IL2}		$\overline{RESET}$, $\overline{TEST}$	0		0.1·V_{DD}	V
High level input current	I_{IH}	V_{IH} = 3.0 V	K00–03, K10–13 P00–03, P10–13 P20–23, P30–33 P40–43, $\overline{RESET}$, $\overline{TEST}$	0		0.5	µA
Low level input current (1)	I_{IL1}	V_{IL1} = V_{SS} Without pull up resistor	K00–03, K10–13 P00–03, P10–13 P20–23, P30–33 P40–43, $\overline{RESET}$, $\overline{TEST}$	-0.5		0	µA
Low level input current (2)	I_{IL2}	V_{IL2} = V_{SS} With pull up resistor	K00–03, K10–13 P00–03, P10–13 P20–23, P30–33 P40–43, $\overline{RESET}$, $\overline{TEST}$	-16	-10	-6	µA
High level output current	I_{OH1}	V_{OH1} = 0.9·V_{DD}	R00–03, R10–13 R20–23, R30–33 R40–43 P00–03, P10–13 P20–23, P30–33 P40–43			-1.5	mA
Low level output current	I_{OL1}	V_{OL1} = 0.1·V_{DD}	R00–03, R10–13 R20–23, R30–33 R40–43 P00–03, P10–13 P20–23, P30–33 P40–43	6			mA
Common output current	I_{OH2}	V_{OH2} = V_{C5} - 0.05 V	COM0–15			-30	µA
	I_{OL2}	V_{OL2} = V_{SS} + 0.05 V		30			µA
Segment output current	I_{OH3}	V_{OH3} = V_{C5} - 0.05 V	SEG0–63			-10	µA
	I_{OL3}	V_{OL3} = V_{SS} + 0.05 V		10			µA

7.4 Analog Circuit Characteristics and Power Current Consumption

Unless otherwise specified: V_{DD} = 1.5 V (when V_{C1} standard is selected), V_{DD} = 3.0 V (when V_{C2} standard is selected)
V_{SS} = 0 V, f_{OSC1} = 32.768 kHz, C_G = 25 pF, Ta = 25°C, V_{D1}/V_{C1}/V_{C2}/V_{C4}/V_{C5} are internal voltage, C1–C8 = 0.2 µF, C9–C10 = 0.4 µF

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
LCD drive voltage (when V_{C1} standard is selected)	V_{C1}	Connect 1MΩ load resistor between V_{SS} and V_{C1} (without panel load) V_{DD} = 1.5 V	LC0–3 = "0"		0.975		V
			LC0–3 = "1"		0.990		
			LC0–3 = "2"		1.005		
			LC0–3 = "3"		1.020		
			LC0–3 = "4"		1.035		
			LC0–3 = "5"		1.050		
			LC0–3 = "6"		1.065		
			LC0–3 = "7"	Typ.	1.080	Typ.	
			LC0–3 = "8"	x 0.88	1.095	x 1.12	
			LC0–3 = "9"		1.110		
			LC0–3 = "10"		1.125		
			LC0–3 = "11"		1.140		
			LC0–3 = "12"		1.155		
			LC0–3 = "13"		1.170		
			LC0–3 = "14"		1.185		
			LC0–3 = "15"		1.200		
	V_{C2}	Connect 1MΩ load resistor between V_{SS} and V_{C2} (without panel load)		$2 \cdot V_{C1}$		$2 \cdot V_{C1}$ x 0.9	V
	V_{C4}	Connect 1MΩ load resistor between V_{SS} and V_{C4} (without panel load)		$3 \cdot V_{C1}$		$3 \cdot V_{C1}$ x 0.9	V
	V_{C5}	Connect 1MΩ load resistor between V_{SS} and V_{C5} (without panel load)		$4 \cdot V_{C1}$		$4 \cdot V_{C1}$ x 0.9	V
LCD drive voltage (when V_{C2} standard is selected)	V_{C1}	Connect 1MΩ load resistor between V_{SS} and V_{C1} (without panel load)		$1/2 \cdot V_{C2}$ -0.1		$1/2 \cdot V_{C2}$ x 0.95	V
	V_{C2}	Connect 1MΩ load resistor between V_{SS} and V_{C2} (without panel load) V_{DD} = 3.0 V	LC0–3 = "0"		1.95		V
			LC0–3 = "1"		1.98		
			LC0–3 = "2"		2.01		
			LC0–3 = "3"		2.04		
			LC0–3 = "4"		2.07		
			LC0–3 = "5"		2.10		
			LC0–3 = "6"		2.13		
			LC0–3 = "7"	Typ.	2.16	Typ.	
			LC0–3 = "8"	x 0.88	2.19	x 1.12	
			LC0–3 = "9"		2.22		
			LC0–3 = "10"		2.25		
			LC0–3 = "11"		2.28		
			LC0–3 = "12"		2.31		
			LC0–3 = "13"		2.34		
			LC0–3 = "14"		2.37		
			LC0–3 = "15"		2.40		
	V_{C4}	Connect 1MΩ load resistor between V_{SS} and V_{C4} (without panel load)		$3/2 \cdot V_{C2}$		$3/2 \cdot V_{C2}$ x 0.95	V
	V_{C5}	Connect 1MΩ load resistor between V_{SS} and V_{C5} (without panel load)		$2 \cdot V_{C2}$		$2 \cdot V_{C2}$ x 0.95	V

Unless otherwise specified: V_{DD} = 3.0 V, V_{SS} = 0 V, f_{OSC1} = 32.768 kHz,
C_G = 25 pF, Ta = 25°C, V_{D1}/V_{C1}/V_{C2}/V_{C4}/V_{C5} are internal voltage, C1–C8 = 0.2 µF, C9–C10 = 0.4 µF, VCCHG = "1"

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
SVD voltage	V_{SVD}	SVDS0–3 = "0"		0.95	1.05	1.15	V
		SVDS0–3 = "1"		1.05	1.10	1.15	
		SVDS0–3 = "2"		1.10	1.15	1.20	
		SVDS0–3 = "3"		1.15	1.20	1.25	
		SVDS0–3 = "4"		1.20	1.25	1.30	
		SVDS0–3 = "5"		1.25	1.30	1.35	
		SVDS0–3 = "6"		1.35	1.40	1.45	
		SVDS0–3 = "7"		1.55	1.60	1.65	
		SVDS0–3 = "8"		1.90	1.95	2.00	
		SVDS0–3 = "9"		1.95	2.00	2.05	
		SVDS0–3 = "10"		2.00	2.05	2.10	
		SVDS0–3 = "11"		2.05	2.10	2.15	
		SVDS0–3 = "12"		2.15	2.20	2.25	
		SVDS0–3 = "13"		2.25	2.30	2.35	
		SVDS0–3 = "14"		2.45	2.50	2.55	
		SVDS0–3 = "15"		2.55	2.60	2.65	
SVD circuit response time	t_{SVD}					100	µS
Power current consumption	I_{OP}	During HALT	32.768 kHz		2.0	4.0	µA
		Normal mode	50.0 kHz		2.3	5.0	µA
		LCD power OFF	76.8 kHz		3.0	5.6	µA
		During HALT	32.768 kHz		6.5	10.0	µA
		Normal mode *1	50.0 kHz		8.0	14.0	µA
		LCD power ON	76.8 kHz		11.0	18.0	µA
		During HALT	32.768 kHz		13.5	25.0	µA
		Boost mode *1	50.0 kHz		16.0	30.0	µA
		V_{DD} = 1.2 V, LCD power ON	76.8 kHz		22.0	38.0	µA
		During HALT	32.768 kHz		5.0	8.0	µA
		Reduce mode *1	50.0 kHz		6.5	11.0	µA
		V_{DD} = 3.0 V, LCD power ON	76.8 kHz		9.0	14.0	µA
		During execution	32.768 kHz		10.0	18.0	µA
		Normal mode *1	50.0 kHz		13.0	24.0	µA
		LCD power ON	76.8 kHz		19.0	32.0	µA
			200 kHz (CR)		40	100	µA
			870 kHz (CR)		330	600	µA
			1 MHz (Ceramic)		300	500	µA
		During execution	32.768 kHz		20.0	36.0	µA
		Boost mode *1	50.0 kHz		26.0	48.0	µA
		V_{DD} = 1.2 V, LCD power ON	76.8 kHz		37.0	64.0	µA
			200 kHz (CR)		80	200	µA
		During execution	32.768 kHz		7.0	14.0	µA
		Reduce mode *1	50.0 kHz		10.0	18.0	µA
		V_{DD} = 3.0 V, LCD power ON	76.8 kHz		14.0	25.0	µA

*1 Without panel load. The SVD circuit is turned OFF.

7.5 Oscillation Characteristics

Oscillation characteristics will vary according to different conditions. Use the following characteristics are as reference values.

OSC1 Crystal Oscillation Circuit

Unless otherwise specified:

V_{DD} = 3.0 V, V_{SS} = 0 V, f_{OSC1} = 32.768 kHz, C_G = 25 pF, C_D = built-in, Ta = 25°C

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Oscillation start voltage	Vsta	tsta ≤ 3 sec	(V_{DD})	1.1			V
Oscillation stop voltage	Vstp	tstp ≤ 10 sec	Normal mode	1.1			V
		(V_{DD})	Boost mode	0.9			V
Built-in capacitance (drain)	C_D	Including the parasitic capacitance inside the IC (in chip)			14		pF
Frequency/voltage deviation	∂f/∂V	V_{DD} = 0.9 to 3.6 V	with VDC switching			5	ppm
			without VDC switching			10	ppm
Frequency/IC deviation	∂f/∂IC			-10		10	ppm
Frequency adjustment range	∂f/∂C_G	C_G = 5 to 25 pF	32.768, 38.4, 50 kHz	35	45		ppm
			76.8 kHz	25	35		ppm
Harmonic oscillation start voltage	V_{hho}	C_G = 5 pF	(V_{DD})	3.6			V
Permitted leak resistance	R_{leak}	Between OSC1 and V_{DD}, V_{SS}		200			MΩ

OSC3 CR Oscillation Circuit 1 (200 kHz)

Unless otherwise specified:

V_{DD} = 3.0 V, V_{SS} = 0 V, R_{CR} = 160 kΩ, Ta = 25°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation frequency dispersion	f_{OSC3}		-30	200 kHz	30	%
Oscillation start voltage	Vsta	Normal mode (V_{DD})	2.2 (0.9)*1			V
Oscillation start time	tsta	V_{DD} = 2.2 to 3.6 V			3	mS
Oscillation stop voltage	Vstp	Normal mode (V_{DD})	2.2 (0.9)*1			V

*1 Items enclosed in parentheses ( ) is those used in the boost mode.

OSC3 CR Oscillation Circuit 2 (1 MHz)

Unless otherwise specified:

V_{DD} = 3.0 V, V_{SS} = 0 V, R_{CR} = 33 kΩ, Ta = 25°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation frequency dispersion	f_{OSC3}		-30	870 kHz	30	%
Oscillation start voltage	Vsta	Normal mode (V_{DD})	2.2			V
Oscillation start time	tsta	V_{DD} = 2.2 to 3.6 V			3	mS
Oscillation stop voltage	Vstp	Normal mode (V_{DD})	2.2			V

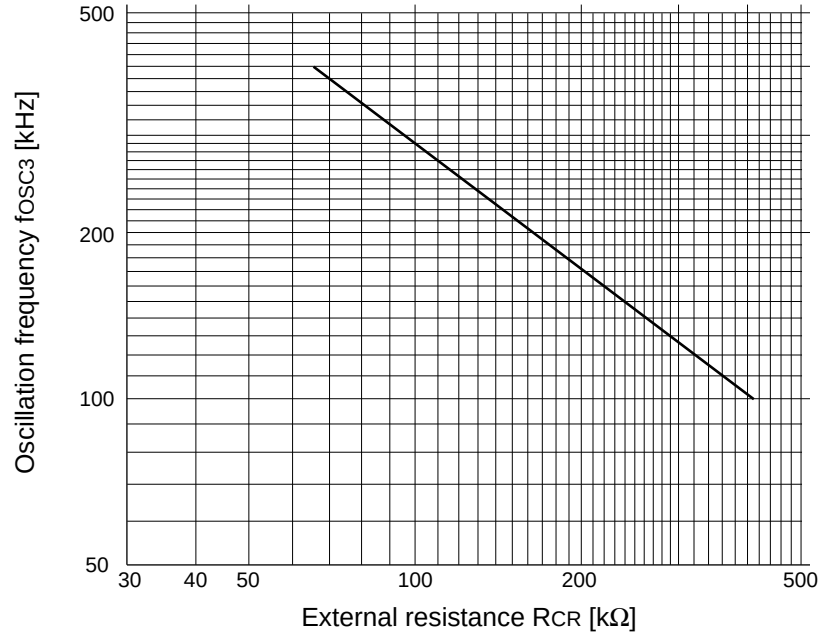
OSC3 Ceramic Oscillation Circuit (1 MHz)

Unless otherwise specified:

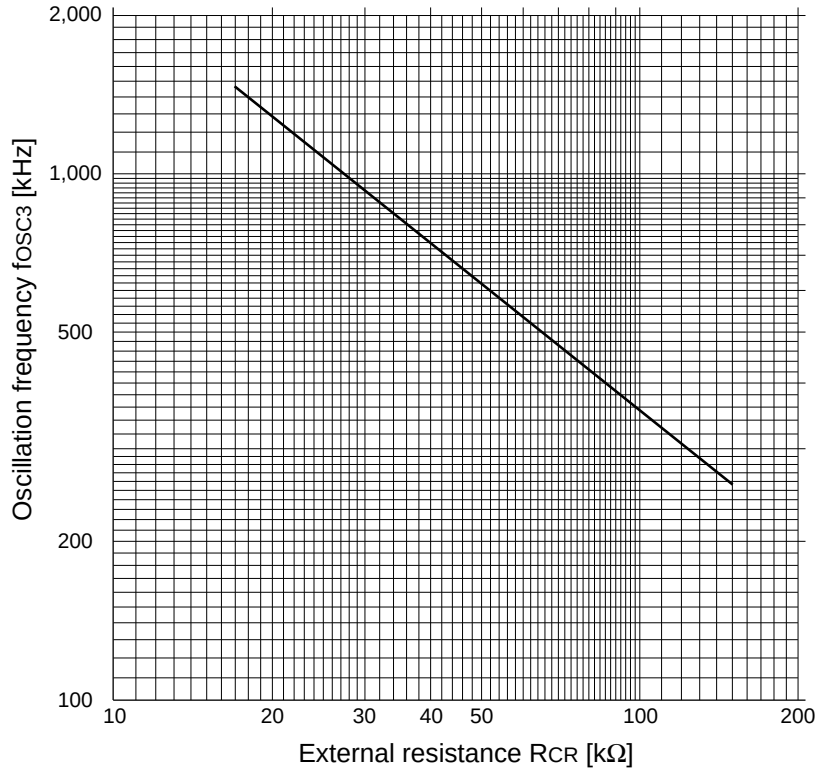
V_{DD} = 3.0 V, V_{SS} = 0 V, Ceramic oscillator: 1 MHz, C_{GC} = C_{DC} = 100 pF, Ta = 25°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start voltage	Vsta	Normal mode (V_{DD})	2.2			V
Oscillation start time	tsta	V_{DD} = 2.2 to 3.6 V			5	mS
Oscillation stop voltage	Vstp	Normal mode (V_{DD})	2.2			V

CR Oscillation Frequency-Resistance Characteristics (200 kHz)



CR Oscillation Frequency-Resistance Characteristics (1 MHz)



7.6 External Memory Access AC Characteristics

Read Cycle

• During 32 kHz (OSC1) operation

Condition: V_{DD} = 1.5 V, V_{SS} = 0 V, Ta = 25°C, V_{IH} = 0.8V_{DD}, V_{IL} = 0.2V_{DD}, V_{OH} = 0.8V_{DD}, V_{OL} = 0.2V_{DD}, CL = 100 pF (load capacitance)

Item	Symbol	Min.	Typ.	Max.	Unit
$\overline{CSx}$ set-up time in read cycle	tras	0.15 × tc			µS
$\overline{CSx}$ hold time in read cycle	trah	0			µS
$\overline{RD}$ set-up time in read cycle	trds	0.15 × tc			µS
$\overline{RD}$ hold time in read cycle	trdh	0			µS

• During 1 MHz (OSC3) operation

Condition: V_{DD} = 3.0 V, V_{SS} = 0 V, Ta = 25°C, V_{IH} = 0.8V_{DD}, V_{IL} = 0.2V_{DD}, V_{OH} = 0.8V_{DD}, V_{OL} = 0.2V_{DD}, CL = 100 pF (load capacitance)

Item	Symbol	Min.	Typ.	Max.	Unit
$\overline{CSx}$ set-up time in read cycle	tras	0.15 × tc			nS
$\overline{CSx}$ hold time in read cycle	trah	0			nS
$\overline{RD}$ set-up time in read cycle	trds	0.15 × tc			nS
$\overline{RD}$ hold time in read cycle	trdh	0			nS

Write Cycle

• During 32 kHz (OSC1) operation

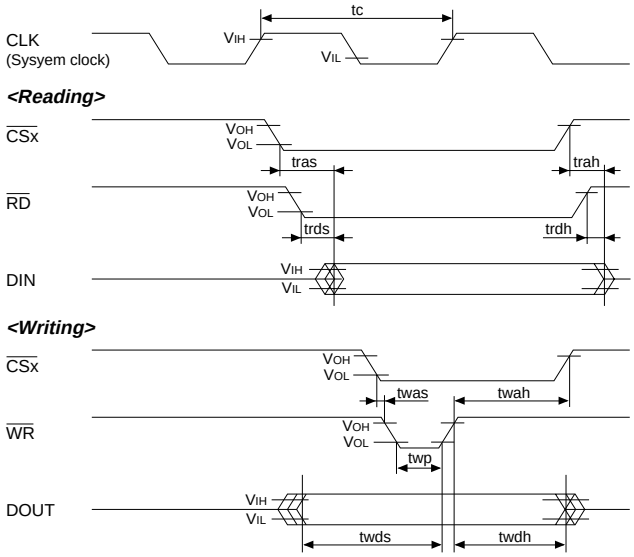
Condition: V_{DD} = 1.5 V, V_{SS} = 0 V, Ta = 25°C, V_{IH} = 0.8V_{DD}, V_{IL} = 0.2V_{DD}, V_{OH} = 0.8V_{DD}, V_{OL} = 0.2V_{DD}, CL = 100 pF (load capacitance)

Item	Symbol	Min.	Typ.	Max.	Unit
Address set-up time in write cycle	twas	0			µS
Address hold time in write cycle	twah	5			µS
Write signal pulse width	twp	5			µS
Data output set-up time in write cycle	twds	5			µS
Data output hold time in write cycle	twdh	5		30	µS

• During 1 MHz (OSC3) operation

Condition: V_{DD} = 3.0 V, V_{SS} = 0 V, Ta = 25°C, V_{IH} = 0.8V_{DD}, V_{IL} = 0.2V_{DD}, V_{OH} = 0.8V_{DD}, V_{OL} = 0.2V_{DD}, CL = 100 pF (load capacitance)

Item	Symbol	Min.	Typ.	Max.	Unit
Address set-up time in write cycle	twas	0			nS
Address hold time in write cycle	twah	200			nS
Write signal pulse width	twp	200			nS
Data output set-up time in write cycle	twds	200			nS
Data output hold time in write cycle	twdh	200		1500	nS



* 1/tc: oscillation frequency

7.7 Serial Interface AC Characteristics

Clock Synchronous Master Mode

• During 32 kHz (OSC1) operation

Condition: V_{DD} = 1.5 V, V_{SS} = 0 V, Ta = 25°C, V_{IH1} = 0.8V_{DD}, V_{IL1} = 0.2V_{DD}, V_{OH} = 0.8V_{DD}, V_{OL} = 0.2V_{DD}

Item	Symbol	Min.	Typ.	Max.	Unit
Transmitting data output delay time	tsmd			5	µS
Receiving data input set-up time	tsms	10			µS
Receiving data input hold time	tsmh	5			µS

• During 1 MHz (OSC3) operation

Condition: V_{DD} = 3.0 V, V_{SS} = 0 V, Ta = 25°C, V_{IH1} = 0.8V_{DD}, V_{IL1} = 0.2V_{DD}, V_{OH} = 0.8V_{DD}, V_{OL} = 0.2V_{DD}

Item	Symbol	Min.	Typ.	Max.	Unit
Transmitting data output delay time	tsmd			200	nS
Receiving data input set-up time	tsms	400			nS
Receiving data input hold time	tsmh	200			nS

Clock Synchronous Slave Mode

• During 32 kHz (OSC1) operation

Condition: V_{DD} = 1.5 V, V_{SS} = 0 V, Ta = 25°C, V_{IH1} = 0.8V_{DD}, V_{IL1} = 0.2V_{DD}, V_{OH} = 0.8V_{DD}, V_{OL} = 0.2V_{DD}

Item	Symbol	Min.	Typ.	Max.	Unit
Transmitting data output delay time	tssd			10	µS
Receiving data input set-up time	tsss	10			µS
Receiving data input hold time	tssh	5			µS

• During 1 MHz (OSC3) operation

Condition: V_{DD} = 3.0 V, V_{SS} = 0 V, Ta = 25°C, V_{IH1} = 0.8V_{DD}, V_{IL1} = 0.2V_{DD}, V_{OH} = 0.8V_{DD}, V_{OL} = 0.2V_{DD}

Item	Symbol	Min.	Typ.	Max.	Unit
Transmitting data output delay time	tssd			500	nS
Receiving data input set-up time	tsss	400			nS
Receiving data input hold time	tssh	200			nS

Asynchronous Mode

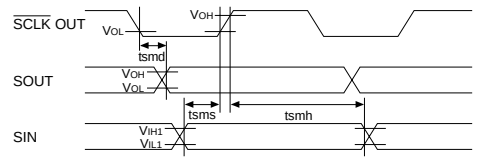
Condition: V_{DD} = 1.5 V, V_{SS} = 0 V, Ta = 25°C

Item	Symbol	Min.	Typ.	Max.	Unit
Start bit detection error time *1	t_{sa1}	0		t/16	S
Erroneous start bit detection range time *2	t_{sa2}	9t/16		10t/16	S

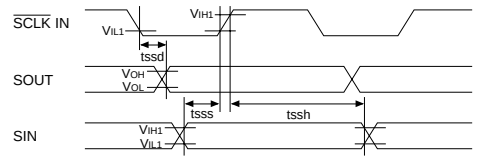
*1 Start bit detection error time is a logical delay time from inputting the start bit until internal sampling begins operating. (Time as far as AC is excluded.)

*2 Erroneous start bit detection range time is a logical range to detect whether a LOW level (start bit) has been input again after a start bit has been detected and the internal sampling clock has started.
When a HIGH level is detected, the start bit detection circuit is reset and goes into a wait status until the next start bit. (Time as far as AC is excluded.)

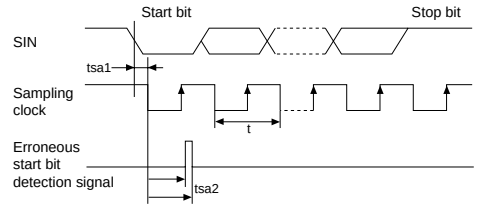
<Clock synchronous master mode>



<Clock synchronous slave mode>

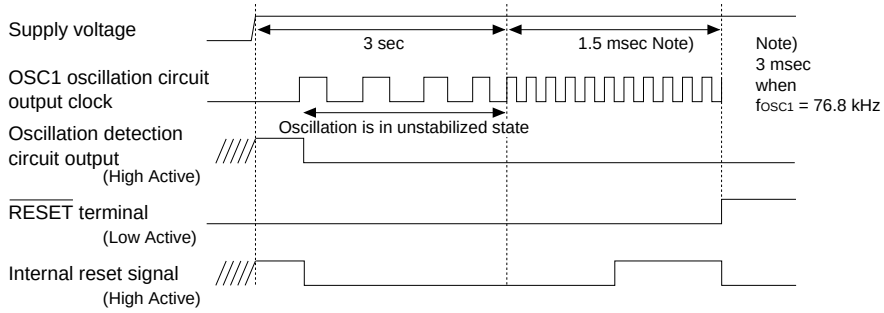


<Asynchronous mode>

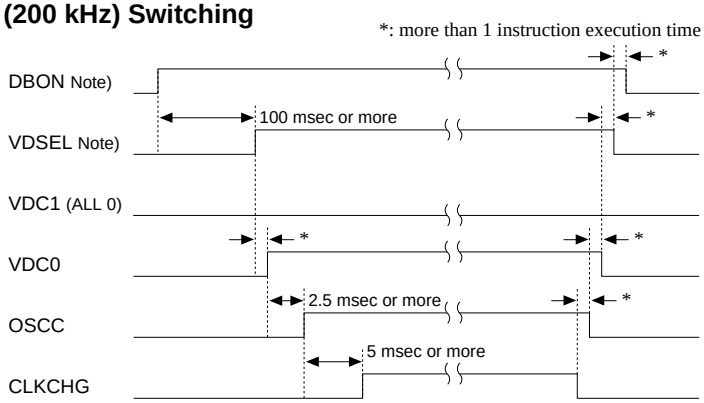


7.8 Timing Chart

Initial Reset

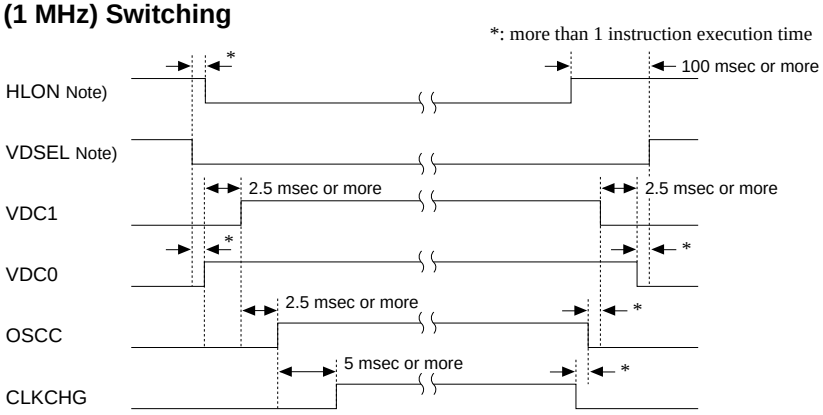


OSC1 ↔ OSC3 (200 kHz) Switching



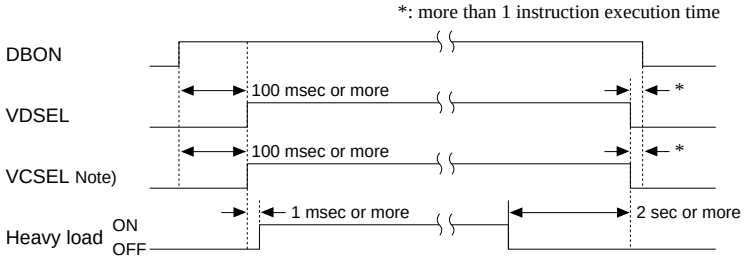
Note) Use DBON and VDSEL only when changes are required.

OSC1 ↔ OSC3 (1 MHz) Switching



Note) When the reduce mode is used. However, when using the reduce mode in the LCD system voltage circuit (VCSEL = "1"), HLON should be set to "1".

Boost Mode Setting when Driving Heavy Load



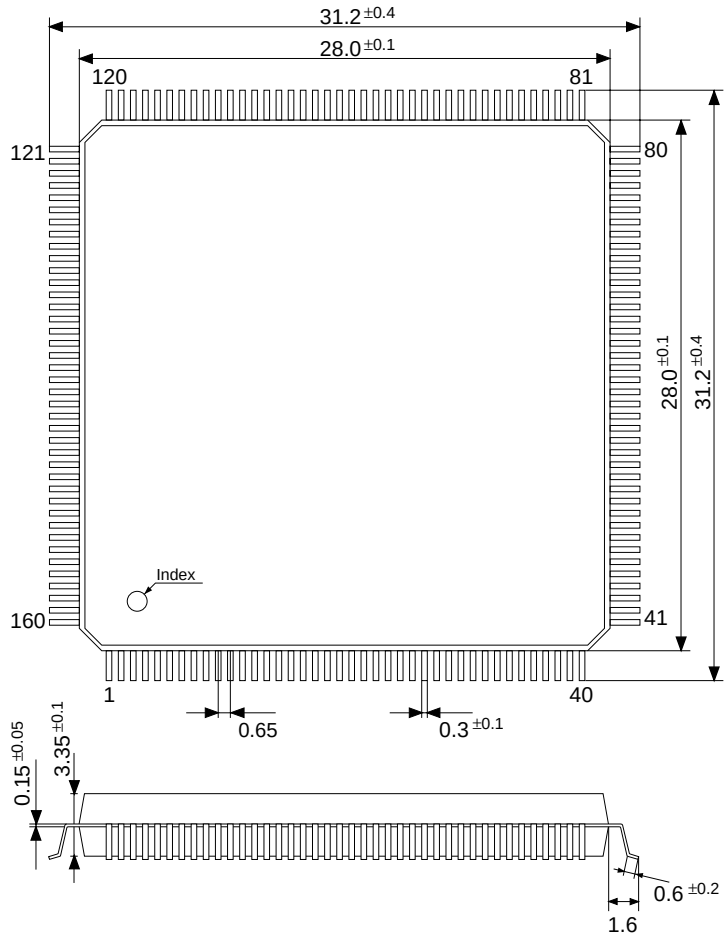
Note) VCSEL is used only when it is required.

CHAPTER 8 PACKAGE

8.1 Plastic Package

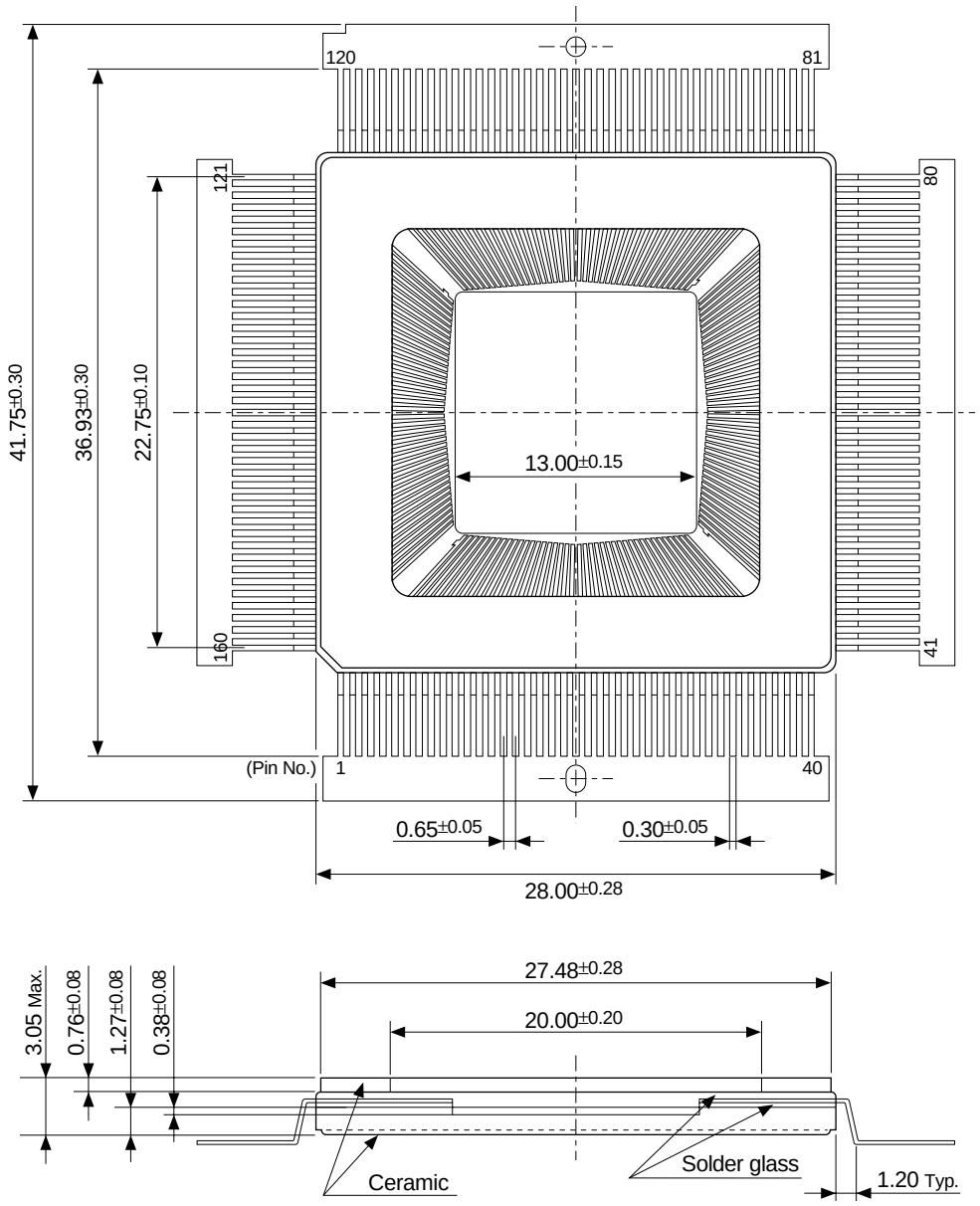
QFP8-160pin

(unit: mm)



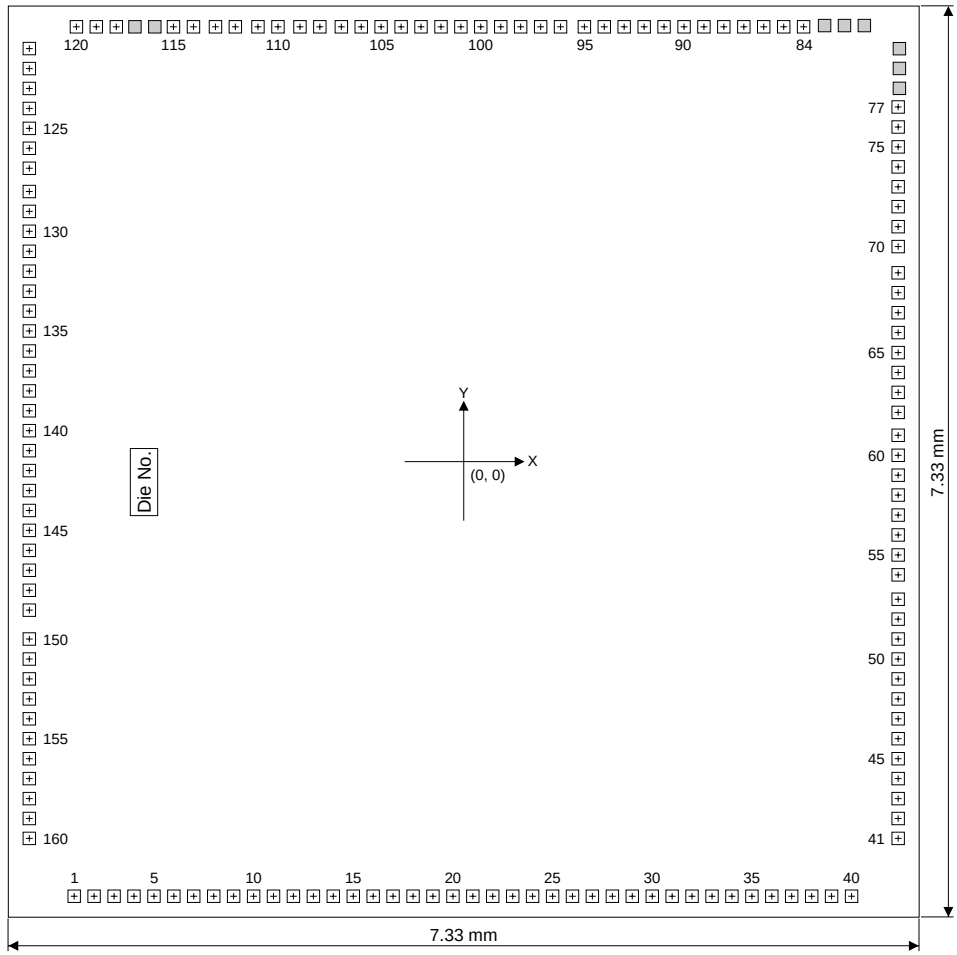
8.2 Ceramic Package for Test Samples

(unit: mm)



CHAPTER 9 PAD LAYOUT

9.1 Diagram of Pad Layout



Chip thickness: 400 µm
Pad opening: 98 µm

9.2 Pad Coordinates

(unit: mm)

Pad		Coordinate		Pad		Coordinate		Pad		Coordinate		Pad		Coordinate	
No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y
1	SEG52	-3,135	-3,498	41	SEG12	3,496	-3,031	81	N.C.	–	–	121	V_{DD}	-3,496	3,323
2	SEG51	-2,975	-3,498	42	SEG11	3,496	-2,871	82	N.C.	–	–	122	OSC4	-3,496	3,162
3	SEG50	-2,814	-3,498	43	SEG10	3,496	-2,711	83	N.C.	–	–	123	OSC3	-3,496	3,002
4	SEG49	-2,654	-3,498	44	SEG9	3,496	-2,550	84	P20	2,735	3,498	124	V_{D1}	-3,496	2,841
5	SEG48	-2,493	-3,498	45	SEG8	3,496	-2,390	85	P21	2,575	3,498	125	OSC2	-3,496	2,681
6	SEG47	-2,333	-3,498	46	SEG7	3,496	-2,229	86	P22	2,414	3,498	126	OSC1	-3,496	2,521
7	SEG46	-2,173	-3,498	47	SEG6	3,496	-2,069	87	P23	2,254	3,498	127	V_{SS}	-3,496	2,360
8	SEG45	-2,012	-3,498	48	SEG5	3,496	-1,909	88	P30	2,093	3,498	128	V_{D2}	-3,496	2,173
9	SEG44	-1,852	-3,498	49	SEG4	3,496	-1,748	89	P31	1,933	3,498	129	V_{C1}	-3,496	2,013
10	SEG43	-1,691	-3,498	50	SEG3	3,496	-1,588	90	P32	1,773	3,498	130	V_{C2}	-3,496	1,853
11	SEG42	-1,531	-3,498	51	SEG2	3,496	-1,427	91	P33	1,612	3,498	131	V_{C3}	-3,496	1,692
12	SEG41	-1,371	-3,498	52	SEG1	3,496	-1,267	92	P40	1,452	3,498	132	V_{C4}	-3,496	1,532
13	SEG40	-1,210	-3,498	53	SEG0	3,496	-1,107	93	P41	1,291	3,498	133	V_{C5}	-3,496	1,371
14	SEG39	-1,050	-3,498	54	COM15	3,496	-911	94	P42	1,131	3,498	134	CH	-3,496	1,211
15	SEG38	-889	-3,498	55	COM14	3,496	-751	95	P43	971	3,498	135	CG	-3,496	1,051
16	SEG37	-729	-3,498	56	COM13	3,496	-590	96	R00	779	3,498	136	CF	-3,496	890
17	SEG36	-569	-3,498	57	COM12	3,496	-430	97	R01	619	3,498	137	CE	-3,496	730
18	SEG35	-408	-3,498	58	COM11	3,496	-269	98	R02	458	3,498	138	CD	-3,496	569
19	SEG34	-248	-3,498	59	COM10	3,496	-109	99	R03	298	3,498	139	CC	-3,496	409
20	SEG33	-87	-3,498	60	COM9	3,496	51	100	R10	137	3,498	140	CB	-3,496	249
21	SEG32	73	-3,498	61	COM8	3,496	212	101	R11	-23	3,498	141	CA	-3,496	88
22	SEG31	233	-3,498	62	K00	3,496	396	102	R12	-183	3,498	142	COM0	-3,496	-72
23	SEG30	394	-3,498	63	K01	3,496	557	103	R13	-344	3,498	143	COM1	-3,496	-233
24	SEG29	554	-3,498	64	K02	3,496	717	104	R20	-504	3,498	144	COM2	-3,496	-393
25	SEG28	715	-3,498	65	K03	3,496	877	105	R21	-665	3,498	145	COM3	-3,496	-553
26	SEG27	875	-3,498	66	K10	3,496	1,038	106	R22	-825	3,498	146	COM4	-3,496	-714
27	SEG26	1,035	-3,498	67	K11	3,496	1,198	107	R23	-985	3,498	147	COM5	-3,496	-874
28	SEG25	1,196	-3,498	68	K12	3,496	1,359	108	R30	-1,158	3,498	148	COM6	-3,496	-1,035
29	SEG24	1,356	-3,498	69	K13	3,496	1,519	109	R31	-1,318	3,498	149	COM7	-3,496	-1,195
30	SEG23	1,517	-3,498	70	P00	3,496	1,730	110	R32	-1,495	3,498	150	SEG63	-3,496	-1,427
31	SEG22	1,677	-3,498	71	P01	3,496	1,890	111	R33	-1,656	3,498	151	SEG62	-3,496	-1,588
32	SEG21	1,837	-3,498	72	P02	3,496	2,051	112	R40	-1,838	3,498	152	SEG61	-3,496	-1,748
33	SEG20	1,998	-3,498	73	P03	3,496	2,211	113	R41	-1,998	3,498	153	SEG60	-3,496	-1,909
34	SEG19	2,158	-3,498	74	P10	3,496	2,371	114	R42	-2,175	3,498	154	SEG59	-3,496	-2,069
35	SEG18	2,319	-3,498	75	P11	3,496	2,532	115	R43	-2,336	3,498	155	SEG58	-3,496	-2,229
36	SEG17	2,479	-3,498	76	P12	3,496	2,692	116	N.C.	–	–	156	SEG57	-3,496	-2,390
37	SEG16	2,639	-3,498	77	P13	3,496	2,853	117	N.C.	–	–	157	SEG56	-3,496	-2,550
38	SEG15	2,800	-3,498	78	N.C.	–	–	118	$\overline{TEST}$	-2,796	3,498	158	SEG55	-3,496	-2,711
39	SEG14	2,960	-3,498	79	N.C.	–	–	119	$\overline{RESET}$	-2,957	3,498	159	SEG54	-3,496	-2,871
40	SEG13	3,121	-3,498	80	N.C.	–	–	120	V_{REF}	-3,117	3,498	160	SEG53	-3,496	-3,031

II. E0C6247 Technical Software

CONTENTS

CHAPTER 1 OVERVIEW

The E0C6247 is a single-chip microcomputer made up of the 4-bit core CPU E0C6200A, ROM (8,192 words, 12 bits to a word), RAM (1,792 words, 4 bits to a word), dot matrix LCD driver, serial interface, watchdog timer, programmable timer, time base counter and SVD circuit. Moreover, in the E0C6247 external memory device control is possible, and are most suitable for applications with equipment requiring large memory and dot matrix display functions such as a highly functional electronic pocketbook.

1.1 Block Diagram

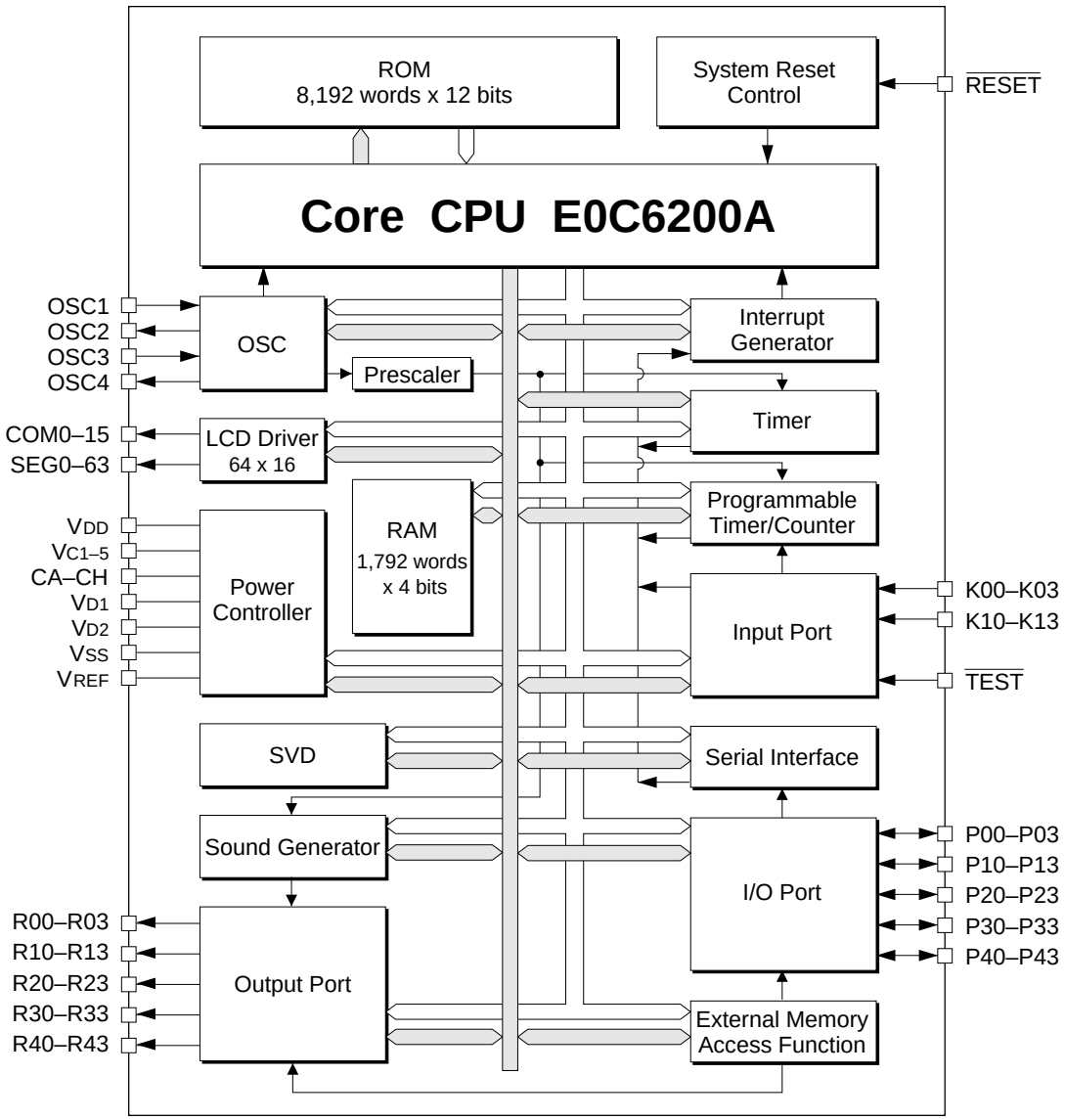


Fig. 1.1.1 Block diagram

1.2 Program Memory (ROM)

The E0C6247 has a built-in mask ROM for loading the program that has a capacity of 8,192 steps × 12 bits. Figure 1.2.1 shows the configuration of the ROM.

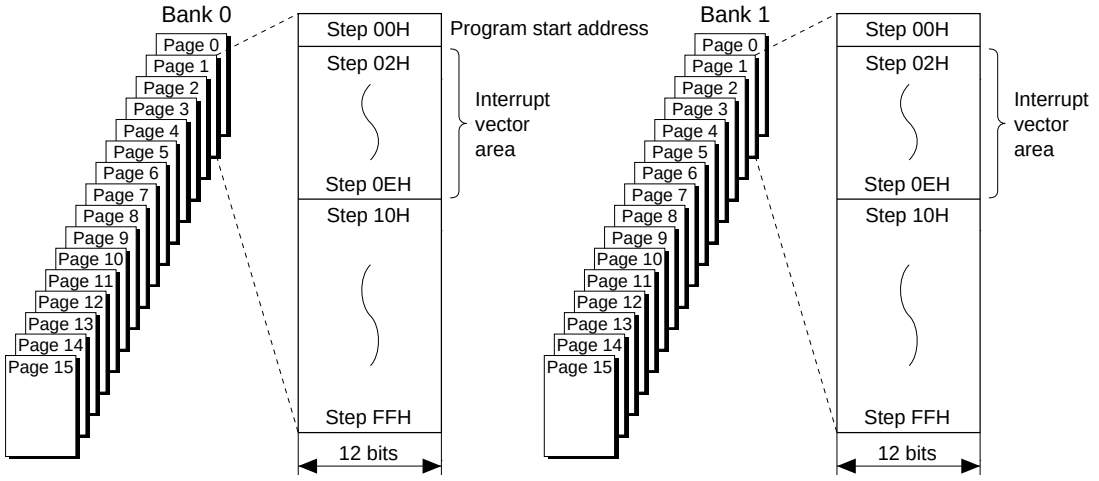


Fig. 1.2.1 ROM configuration

The program area is two banks, each of 16 (0–15) pages × 256 (00H–FFH) steps. After initial reset, the program beginning address is set to bank 0, page 1, step 00H. The interrupt vector is allocated to page 1 of each bank, steps 02H–0EH.

1.3 Interrupt Vector

Table 1.3.1 shows the correspondence of interrupt requests and interrupt vectors.

Table 1.3.1 Interrupt request and interrupt vectors

Interrupt vector (every Bank)	Interrupt factor	Priority
102H	Programmable timer	High
104H	Serial I/F (error generation)	↑
106H	Serial I/F (receiving completion)	
108H	Serial I/F (transmitting completion)	
10AH	K10–K13 input	
10CH	K00–K03 input	↓
10EH	Clock timer	Low

The four low-order bits of the program counter are indirectly addressed through the interrupt request.

1.4 Data Memory

Data memory of the E0C6247 is composed of 1,792-word RAM, 256-word display memory, 80-word I/O memory and 256-word external memory access area.
When programming, keep the following points in mind.

(1) Part of the data memory (RAM, page 0) can be used as stack area when subroutine calls and saving registers, so be careful not to overlap the data area and stack area. Subroutine calls and interrupts take up three words of the stack area.

(2) The data memory 000H–00FH is for the register pointers (RP), and is the addressable memory register area.

Figures 1.4.1(a) and (b) present the overall memory maps of the E0C6247, and Tables 1.4.1(a)–(h) the peripheral circuits' (I/O space) memory maps.

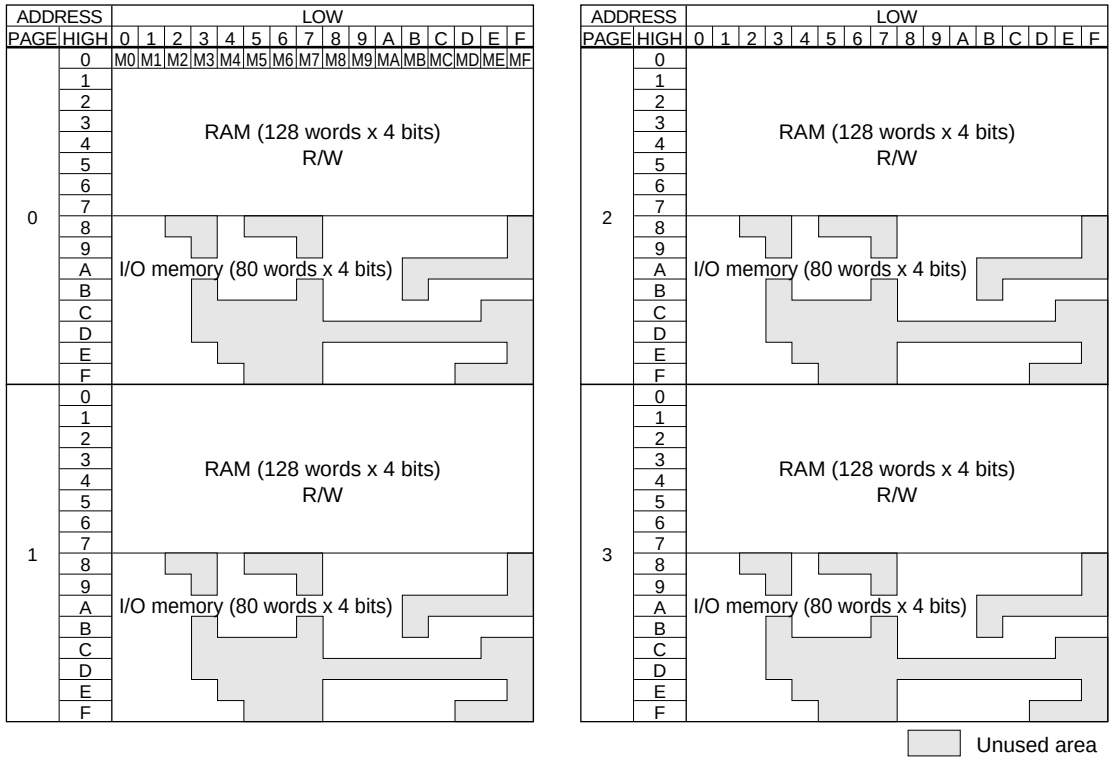


Fig. 1.4.1(a) Memory map

Note: Memory is not mounted in unused area within the memory map and in memory area not indicated in this chapter. For this reason, normal operation cannot be assured for programs that have been prepared with access to these areas.

ADDRESS		LOW													
PAGE	HIGH	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
4	0–F	RAM (256 words x 4 bits) R/W															
5	0–F	RAM (256 words x 4 bits) R/W															
6	0–F	RAM (256 words x 4 bits) R/W															
7	0–F	RAM (256 words x 4 bits) R/W															

ADDRESS		LOW													
PAGE	HIGH	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
8	0–F	RAM (256 words x 4 bits) R/W															
9	0–F	For external memory accessing (256 words x 4 bits) R/W															
A	0–F	Display memory (256 words x 4 bits) R/W															

Fig. 1.4.1(b) Memory map

Table 1.4.1(a) I/O memory map (80H–8EH)

Address *7	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
80H	SVDS3	SVDS2	SVDS1	SVDS0	SVDS3	0			SVD criteria voltage setting SVDS [3][2][1][0] Voltage (V) / SVDS [3][2][1][0] Voltage (V) 0 1 1 1 1.60 / 1 1 1 1 2.60 0 1 1 0 1.40 / 1 1 1 0 2.50 0 1 0 1 1.30 / 1 1 0 1 2.30 0 1 0 0 1.25 / 1 1 0 0 2.20 0 0 1 1 1.20 / 1 0 1 1 2.10 0 0 1 0 1.15 / 1 0 1 0 2.05 0 0 0 1 1.10 / 1 0 0 1 2.00 0 0 0 0 1.05 / 1 0 0 0 1.95
					SVDS2	0			
					SVDS1	0			
	R/W				SVDS0	0			
81H	0	0	SVDDT	SVDON	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R			R/W	SVDDT	0	Low	Normal	SVD evaluation data
					SVDON	0	On	Off	SVD circuit On/Off
84H	VCSEL	VDSEL	HLON	DBON	VCSEL	0	V_{D2}	V_{DD}	Power selection for LCD system voltage circuit
					VDSEL	0	V_{D2}	V_{DD}	Power selection for oscillation system regulated voltage circuit
	R/W				HLON	0	On	Off	Halver On/Off
					DBON	0	On	Off	Doubler On/Off
88H	0	0	PRSM1	PRSM0	0 *5	– *2			Unused PRSM[1][0] f_{OSC1} (kHz) 1 1 76.8 1 0 50.0 0 1 38.4 0 0 32.768
					0 *5	– *2			Unused
	R		R/W		PRSM1	0			OSC1 prescaler selection
					PRSM0	0			
89H	CLKCHG	OSCC	VDC1	VDC0	CLKCHG	0	OSC3	OSC1	CPU system clock switch
					OSCC	0	On	Off	OSC3 oscillation On/Off
	R/W				VDC1	0			CPU operating voltage switch VDC [1][0] V_{D1} Oscillation circuit 1 * 2.1 V OSC3 (1 MHz) 0 1 1.4 V OSC3 (200 kHz) 0 0 1.2 V OSC1
					VDC0	0			
8AH	FOUTE	0	FOFQ1	FOFQ0	FOUTE	0	Enable	Disable	FOUT output enable
					0 *5	– *2			Unused
	R/W	R	R/W		FOFQ1	0			FOUT frequency selection FOFQ[1][0] FOUT frequency 1 1 f_{OSC3} 1 0 f_{OSC1} 0 1 f_{OSC1}/8 (f_{OSC1}/16) 0 0 f_{OSC1}/64 (f_{OSC1}/128) (In case of f_{OSC1} = 76.8 kHz)
					FOFQ0	0			
8BH	0	0	0	WDRST	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R			W	0 *5	– *2			Unused
					WDRST *5	Reset	Reset	–	Watchdog timer reset
8CH	0	0	TMRUN	TMRST	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R		R/W	W	TMRUN	0	Run	Stop	Clock timer Run/Stop
					TMRST *5	Reset	Reset	–	Clock timer reset
8DH	TM3	TM2	TM1	TM0	TM3	0			Clock timer data (16 Hz) (f_{OSC1} = 50 kHz → (12.5 Hz) (25 Hz) (50 Hz) (100 Hz))
					TM2	0			Clock timer data (32 Hz)
	R				TM1	0			Clock timer data (64 Hz)
					TM0	0			Clock timer data (128 Hz)
8EH	TM7	TM6	TM5	TM4	TM7	0			Clock timer data (1 Hz)
					TM6	0			Clock timer data (2 Hz)
	R				TM5	0			Clock timer data (4 Hz)
					TM4	0			Clock timer data (8 Hz)

Remarks

*1 Initial value at the time of initial reset
*2 Not set in the circuit
*3 Undefined
*4 Reset (0) immediately after being read
*5 Constantly "0" when being read
*6 Refer to main manual
*7 I/O memory is allocated from page 0 to 3

Table 1.4.1(b) I/O memory map (90H–9EH)

Address *7	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
90H	SIK03	SIK02	SIK01	SIK00	SIK03	0	Enable	Disable	K00–K03 interrupt selection register
					SIK02	0	Enable	Disable	
	R/W				SIK01	0	Enable	Disable	
					SIK00	0	Enable	Disable	
91H	K03	K02	K01	K00	K03	– *2	High	Low	K00–K03 input port data
					K02	– *2	High	Low	
	R				K01	– *2	High	Low	
					K00	– *2	High	Low	
92H	KCP03	KCP02	KCP01	KCP00	KCP03	1	↓	↑	K00–K03 input comparison register
					KCP02	1	↓	↑	
	R/W				KCP01	1	↓	↑	
					KCP00	1	↓	↑	
94H	SIK13	SIK12	SIK11	SIK10	SIK13	0	Enable	Disable	K10–K13 interrupt selection register
					SIK12	0	Enable	Disable	
	R/W				SIK11	0	Enable	Disable	
					SIK10	0	Enable	Disable	
95H	K13	K12	K11	K10	K13	– *2	High	Low	K10–K13 input port data
					K12	– *2	High	Low	
	R				K11	– *2	High	Low	
					K10	– *2	High	Low	
96H	KCP13	KCP12	KCP11	KCP10	KCP13	1	↓	↑	K10–K13 input comparison register
					KCP12	1	↓	↑	
	R/W				KCP11	1	↓	↑	
					KCP10	1	↓	↑	
98H	EXTMF	0	MEMS1	MEMS0	EXTMF	0	On	Off	External memory access function control
					0 *5	– *2			Unused
					MEMS1	0			External memory size selection (MEMS [1][0]: 11 = 1M (R only) (A00–A16); 10 = 512K (R/W) (A00–A15); 01 = 256K (R/W) (A00–A14); 00 = 64K (R/W) (A00–A12))
	R/W	R	R/W		MEMS0	0			
99H	HZCS	HZBUS	ADINC	PICON	HZCS	0	High-Z	Output	$\overline{CS0}$–$\overline{CS3}$ output high-impedance control
					HZBUS	0	High-Z	Output	Address bus, $\overline{RD}$/$\overline{WR}$ high-impedance control
	R/W		W	R/W	ADINC	0	Increment	–	External memory address increment
					PICON	0	Auto inc.	Normal	External memory address auto increment mode
9AH	A03	A02	A01	A00	A03	– *2	1	0	External memory address A00–A03 (EXTMF = 1) Functions as a general-purpose register when EXTMF = 0.
					A02	– *2	1	0	
	R/W				A01	– *2	1	0	
					A00	– *2	1	0	
9BH	A07	A06	A05	A04	A07	– *2	1	0	External memory address A04–A07 (EXTMF = 1) Functions as a general-purpose register when EXTMF = 0.
					A06	– *2	1	0	
	R/W				A05	– *2	1	0	
					A04	– *2	1	0	
9CH	A11	A10	A09	A08	A11	– *2	1	0	External memory address A08–A11 (EXTMF = 1) Functions as a general-purpose register when EXTMF = 0.
					A10	– *2	1	0	
	R/W				A09	– *2	1	0	
					A08	– *2	1	0	
9DH	A15	A14	A13	A12	A15	– *2	1	0	External memory address A12–A15 (EXTMF = 1) Bits that are not used as an address for external memory access can also be used as a general-purpose register.
					A14	– *2	1	0	
	R/W				A13	– *2	1	0	
					A12	– *2	1	0	
9EH	0	0	0	A16	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R			R/W	0 *5	– *2			Unused
					A16	– *2	1	0	External memory address A16 *8

*8 When other than EXTMF = 1 and a memory less than 1M bits are used, it functions as a general-purpose register.

Table 1.4.1(c) I/O memory map (A0H–AAH)

Address *7	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
A0H	0	0	0	R0HIZ	0 *5	– *2			Unused
					0 *5	– *2			Unused * R0HIZ functions as a general-purpose
	R			R/W	0 *5	– *2			Unused register when EXTMF = 1.
					R0HIZ	0	High-Z	Output	R0 output high-impedance control (EXTMF = 0)
A1H	R03	R02	R01	R00	R03	1	High	Low	R00–R03 output port data (EXTMF = 0)
					R02	1	High	Low	Functions as a general-purpose register
	R/W				R01	1	High	Low	when EXTMF = 1.
					R00	1	High	Low	
A2H	0	0	0	R1HIZ	0 *5	– *2			Unused
					0 *5	– *2			Unused * R1HIZ functions as a general-purpose
	R			R/W	0 *5	– *2			Unused register when EXTMF = 1.
					R1HIZ	0	High-Z	Output	R1 output high-impedance control (EXTMF = 0)
A3H	R13	R12	R11	R10	R13	1	High	Low	R10–R13 output port data (EXTMF = 0)
					R12	1	High	Low	Functions as a general-purpose register
	R/W				R11	1	High	Low	when EXTMF = 1.
					R10	1	High	Low	
A4H	0	0	0	R2HIZ	0 *5	– *2			Unused
					0 *5	– *2			Unused * R2HIZ functions as a general-purpose
	R			R/W	0 *5	– *2			Unused register when EXTMF = 1.
					R2HIZ	0	High-Z	Output	R2 output high-impedance control (EXTMF = 0)
A5H	R23	R22	R21	R20	R23	1	High	Low	R20–R23 output port data (EXTMF = 0)
					R22	1	High	Low	Functions as a general-purpose register
	R/W				R21	1	High	Low	when EXTMF = 1.
					R20	1	High	Low	
A6H	R33HIZ	R32HIZ	R31HIZ	R30HIZ	R33HIZ	0	High-Z	Output	R30–R33 output high-impedance control
					R32HIZ	0	High-Z	Output	Bit corresponding to the address bus for external
	R/W				R31HIZ	0	High-Z	Output	memory can be used as a general-purpose register
					R30HIZ	0	High-Z	Output	when EXTMF = 1.
A7H	R33	R32	R31	R30	R33	1	High	Low	R30–R33 output port data
					R32	1	High	Low	Bit corresponding to the address bus for external
	R/W				R31	1	High	Low	memory can be used as a general-purpose register
					R30	1	High	Low	when EXTMF = 1.
A8H	R43HIZ	R42HIZ	R41HIZ	R40HIZ	R43HIZ	0	High-Z	Output	R43 output high-impedance control
					R42HIZ	0	High-Z	Output	R42 output high-impedance control
					R41HIZ	0	High-Z	Output	R41 output high-impedance control (EXTMF = 0)
									(General-purpose register when EXTMF = 1)
	R/W				R40HIZ	0	High-Z	Output	R40 output high-impedance control (EXTMF = 0)
									(General-purpose register when EXTMF = 1)
A9H	R43	R42	R41	R40	R43	0	High	Low	R43 output port data (SELR43 = 0)
									(General-purpose register when BZ output is selected)
					R42	0	High	Low	R42 output port data (SELR42 = 0)
									(General-purpose register when $\overline{BZ}$ output is selected)
	R/W				R41	1	High	Low	R41 output port data (EXTMF = 0)
									(General-purpose register when EXTMF = 1)
					R40	1	High	Low	R40 output port data (EXTMF = 0)
									(General-purpose register when EXTMF = 1)
AAH	SELR43	SELR42	0	0	SELR43	0	BZ	Normal	R43 function selection register (BZ or general-purpose output)
					SELR42	0	$\overline{BZ}$	Normal	R42 function selection register ($\overline{BZ}$ or general-purpose output)
	R/W		R		0 *5	– *2			Unused
					0 *5	– *2			Unused

Table 1.4.1(d) I/O memory map (B0H–BAH)

Address *7	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
B0H	IOC03	IOC02	IOC01	IOC00	IOC03	0	Output	Input	P00–P03 I/O control register (EXTMF = 0) Functions as a general-purpose register when EXTMF = 1.
					IOC02	0	Output	Input	
	R/W				IOC01	0	Output	Input	
					IOC00	0	Output	Input	
B1H	PUL03	PUL02	PUL01	PUL00	PUL03	1	On	Off	P00–P03 pull up control register (EXTMF = 0) Functions as a general-purpose register when EXTMF = 1.
					PUL02	1	On	Off	
	R/W				PUL01	1	On	Off	
					PUL00	1	On	Off	
B2H	P03	P02	P01	P00	P03	– *2	High	Low	P00–P03 I/O port data (EXTMF = 0)
					P02	– *2	High	Low	
	D03	D02	D01	D00	P01	– *2	High	Low	
					P00	– *2	High	Low	
	R/W				D03	– *2	1	0	External memory data D00–D03 (EXTMF = 1)
					D02	– *2	1	0	
					D01	– *2	1	0	
					D00	– *2	1	0	
B4H	IOC13	IOC12	IOC11	IOC10	IOC13	0	Output	Input	P10–P13 I/O control register (EXTMF = 0) Functions as a general-purpose register when EXTMF = 1.
					IOC12	0	Output	Input	
	R/W				IOC11	0	Output	Input	
					IOC10	0	Output	Input	
B5H	PUL13	PUL12	PUL11	PUL10	PUL13	1	On	Off	P10–P13 pull up control register (EXTMF = 0) Functions as a general-purpose register when EXTMF = 1.
					PUL12	1	On	Off	
	R/W				PUL11	1	On	Off	
					PUL10	1	On	Off	
B6H	P13	P12	P11	P10	P13	– *2	High	Low	P10–P13 I/O port data (EXTMF = 0)
					P12	– *2	High	Low	
	D07	D06	D05	D04	P11	– *2	High	Low	
					P10	– *2	High	Low	
	R/W				D07	– *2	1	0	External memory data D04–D07 (EXTMF = 1)
					D06	– *2	1	0	
					D05	– *2	1	0	
					D04	– *2	1	0	
B8H	IOC23	IOC22	IOC21	IOC20	IOC23	0	Output	Input	P20–P23 I/O control register (EXTMF = 0) Functions as a general-purpose register when EXTMF = 1.
					IOC22	0	Output	Input	
	R/W				IOC21	0	Output	Input	
					IOC20	0	Output	Input	
B9H	PUL23	PUL22	PUL21	PUL20	PUL23	1	On	Off	P20–P23 pull up control register (EXTMF = 0) Functions as a general-purpose register when EXTMF = 1.
					PUL22	1	On	Off	
	R/W				PUL21	1	On	Off	
					PUL20	1	On	Off	
BAH	P23	P22	P21	P20	P23	– *2	High	Low	P20–P23 I/O port data (EXTMF = 0)
					P22	– *2	High	Low	
	CS3	CS2	CS1	CS0	P21	– *2	High	Low	
					P20	– *2	High	Low	
	R/W				CS3	– *2	Disable	Active	Chip select $\overline{CS0}$–$\overline{CS3}$ active standby (EXTMF = 1)
					CS2	– *2	Disable	Active	
					CS1	– *2	Disable	Active	
					CS0	– *2	Disable	Active	

Table 1.4.1(e) I/O memory map (BCH–C2H)

Address *7	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
BCH	IOC33	IOC32	IOC31	IOC30	IOC33	0	Output	Input	P33 I/O control register (SELP33 = 0) (General-purpose register when FOUT output is selected)
					IOC32	0	Output	Input	P32 I/O control register (SELP32 = 0) (General-purpose register when PTOVF output is selected)
	R/W				IOC31	0	Output	Input	P31 I/O control register (SELP31 = 0) (General-purpose register when FR output is selected)
					IOC30	0	Output	Input	P30 I/O control register (SELP30 = 0) (General-purpose register when CL output is selected)
BDH	PUL33	PUL32	PUL31	PUL30	PUL33	1	On	Off	P33 pull up control register (SELP33 = 0) (General-purpose register when FOUT output is selected)
					PUL32	1	On	Off	P32 pull up control register (SELP32 = 0) (General-purpose register when PTOVF output is selected)
	R/W				PUL31	1	On	Off	P31 pull up control register (SELP31 = 0) (General-purpose register when FR output is selected)
					PUL30	1	On	Off	P30 pull up control register (SELP30 = 0) (General-purpose register when CL output is selected)
BEH	P33	P32	P31	P30	P33	– *2	High	Low	P33 I/O port data (SELP33 = 0) (General-purpose register when FOUT output is selected)
					P32	– *2	High	Low	P32 I/O port data (SELP32 = 0) (General-purpose register when PTOVF output is selected)
	R/W				P31	– *2	High	Low	P31 I/O port data (SELP31 = 0) (General-purpose register when FR output is selected)
					P30	– *2	High	Low	P30 I/O port data (SELP30 = 0) (General-purpose register when CL output is selected)
BFH	SELP33	SELP32	SELP31	SELP30	SELP33	0	FOUT	I/O	P33 function selection register (FOUT output or I/O)
					SELP32	0	PTOVF	I/O	P32 function selection register (PTOVF output or I/O)
	R/W				SELP31	0	FR	I/O	P31 function selection register (FR output or I/O)
					SELP30	0	CL	I/O	P30 function selection register (CL output or I/O)
C0H	IOC43	IOC42	IOC41	IOC40	IOC43	0	Output	Input	P43 I/O control register (General-purpose register when SI/F (sync. slave) is selected)
					IOC42	0	Output	Input	P42 I/O control register (General-purpose register when SI/F (sync.) is selected)
	R/W				IOC41	0	Output	Input	P41 I/O control register (ESIF = 0) (General-purpose register when SI/F is selected)
					IOC40	0	Output	Input	P40 I/O control register (ESIF = 0) (General-purpose register when SI/F is selected)
C1H	PUL43	PUL42	PUL41	PUL40	PUL43	1	On	Off	P43 pull up control register (General-purpose register when SI/F (sync. slave) is selected)
					PUL42	1	On	Off	P42 pull up control register (General-purpose register when SI/F (sync. master) is selected)
	R/W				PUL41	1	On	Off	P41 pull up control register (ESIF = 0) (General-purpose register when SI/F is selected)
					PUL40	1	On	Off	P40 pull up control register (ESIF = 0) SIN pull up control register (ESIF = 1)
C2H	P43	P42	P41	P40	P43	– *2	High	Low	P43 I/O port data (General-purpose register when SI/F (sync. slave) is selected)
					P42	– *2	High	Low	P42 I/O port data (General-purpose register when SI/F (sync.) is selected)
	R/W				P41	– *2	High	Low	P41 I/O port data (ESIF = 0) (General-purpose register when SI/F is selected)
					P40	– *2	High	Low	P40 I/O port data (ESIF = 0) (General-purpose register when SI/F is selected)

Table 1.4.1(f) I/O memory map (C8H–D2H)

Address *7	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
C8H	0	SMD1	SMD0	ESIF	0 *5	– *2			Unused
					SMD1	0			Serial I/F mode selection SMD[1][0] Mode 1 1 Asynchronous 8-bit 1 0 Asynchronous 7-bit 0 1 Clock synchronous slave 0 0 Clock synchronous master
					SMD0	0			
	R	R/W			ESIF	0	SI/F	I/O	Serial I/F enable (P4 port function selection)
C9H	EPR	PMD	SCS1	SCS0	EPR	0	WithParity	NonParity	Parity enable (only for asynchronous mode)
					PMD	0	Odd	Even	Parity mode selection
					SCS1	0			Clock source selection SCS[1][0] Clock source 1 1 PT × 1/2 1 0 CPU clock × 1/4 0 1 CPU clock × 1/8 0 0 CPU clock × 1/16
	R/W				SCS0	0			
CAH	RXTRG	RXEN	TXTRG	TXEN	RXTRG(R)	0	Run	Stop	Receive status (when reading)
					RXTRG(W)		Trigger	–	Receive trigger (when writing)
					RXEN	0	Enable	Disable	Receive enable
	R/W				TXTRG(R)	0	Run	Stop	Transmit status (when reading)
					TXTRG(W)		Trigger	–	Transmit trigger (when writing)
					TXEN	0	Enable	Disable	Transmit enable
CBH	0	FER	PER	OER	0 *5	– *2			Unused
					FER(R)	0	Error	NoError	Framing error flag (when reading)
					FER(W)		Reset	–	flag reset (when writing)
					PER(R)	0	Error	NoError	Parity error flag (when reading)
	R	R/W			PER(W)		Reset	–	flag reset (when writing)
					OER(R)	0	Error	NoError	Overrun error flag (when reading)
					OER(W)		Reset	–	flag reset (when writing)
CCH	TRXD3	TRXD2	TRXD1	TRXD0	TRXD3	– *2	High	Low	Transmit/Receive data (low-order 4 bits)
					TRXD2	– *2	High	Low	
					TRXD1	– *2	High	Low	
	R/W				TRXD0	– *2	High	Low	LSB
CDH	TRXD7	TRXD6	TRXD5	TRXD4	TRXD7	– *2	High	Low	MSB
					TRXD6	– *2	High	Low	Transmit/Receive data (high-order 4 bits)
					TRXD5	– *2	High	Low	
	R/W				TRXD4	– *2	High	Low	
D0H	LDUTY	VCCHG	0	LPWR	LDUTY	0	1/8	1/16	LCD drive duty switch
					VCCHG	0	V_{C2}	V_{C1}	LCD regulated voltage switch
	R/W				0 *5	– *2			Unused
					LPWR	0	On	Off	LCD power On/Off
D1H	0	ALOFF	ALON	0	0 *5	– *2			Unused
					ALOFF	1	AllOff	Normal	All LCD dots fade out control
	R	R/W		R	ALON	0	AllOn	Normal	All LCD dots displayed control
					0 *5	– *2			Unused
D2H	LC3	LC2	LC1	LC0	LC3	– *2			LCD contrast adjustment LC3–LC0 = 0 Light : LC3–LC0 = 15 Dark
					LC2	– *2			
	R/W				LC1	– *2			
					LC0	– *2			

Table 1.4.1(g) I/O memory map (E0H–EEH)

Address *7	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
E0H	ENRTM	ENRST	ENON	BZE	ENRTM	0	1 sec	0.5 sec	Envelope attenuation time selection
					ENRST *5	– *2	Reset	–	Envelope reset
	R/W	W	R/W		ENON	0	On	Off	Envelope On/Off
					BZE	0	Enable	Disable	BZ output enable
E1H	0	BZSTP	BZSHT	SHTPW	0 *5	– *2			Unused
					BZSTP *5	– *2	Stop	–	One-shot buzzer stop
					BZSHT(W)	– *2	Trigger	–	One-shot buzzer trigger (when writing)
	R	W	R/W		BZSHT(R)	0	Busy	Ready	One-shot buzzer status (when reading)
					SHTPW	0	125 msec	31.25 msec	One-shot buzzer pulse width selection (160/40 msec is in case of f_{OSC1} = 50 kHz)
E2H	0	BZFQ2	BZFQ1	BZFQ0	0 *5	– *2			Unused
					BZFQ2	0			Buzzer frequency selection
	R	R/W			BZFQ1	0			
					BZFQ0	0			

BZFQ [2][1][0]	Buzzer frequency	f_{OSC1} = 32 kHz (Hz)
1 1 1	f_{OSC1}/28	1170.3
1 1 0	f_{OSC1}/24	1365.3
1 0 1	f_{OSC1}/20	1638.4
1 0 0	f_{OSC1}/16	2048.0
0 1 1	f_{OSC1}/14	2340.6
0 1 0	f_{OSC1}/12	2730.7
0 0 1	f_{OSC1}/10	3276.8
0 0 0	f_{OSC1}/8	4096.0

E3H	0	BDTY2	BDTY1	BDTY0	0 *5	– *2			Unused
					BDTY2	0			Buzzer signal duty ratio selection *6
	R	R/W			BDTY1	0			
					BDTY0	0			
E8H	0	0	PTPS1	PTPS0	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R		R/W		PTPS1	0			Programmable timer clock dividing ratio selection
					PTPS0	0			

PTPS [1][0]	Dividing ratio
1 1	1/256
1 0	1/32
0 1	1/4
0 0	1/1

E9H	0	0	PTPC1	PTPC0	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R		R/W		PTPC1	0			PT prescaler clock source selection
					PTPC0	0			

PTPC [1][0]	CLK
1 1	OSC3
1 0	OSC1
0 1	K02
0 0	K02 (NR)

EAH	PNRFS	PTOE	PTRUN	PTRST	PNRFS	0	1024 Hz	256 Hz	Noise rejector clock frequency selection
					PTOE	0	Enable	Disable	PTOVF output enable
	R/W			W	PTRUN	0	Run	Stop	Programmable timer Run/Stop
					PTRST *5	– *2	Rst (reload)	–	Programmable timer reset (reload)
EBH	RD3	RD2	RD1	RD0	RD3	0			MSB Programmable timer reload data (low-order 4 bits) LSB
					RD2	0			
	R/W				RD1	0			
					RD0	0			
ECH	RD7	RD6	RD5	RD4	RD7	0			MSB Programmable timer reload data (high-order 4 bits) LSB
					RD6	0			
	R/W				RD5	0			
					RD4	0			
EDH	PT3	PT2	PT1	PT0	PT3	0			MSB Programmable timer data (low-order 4 bits) LSB
					PT2	0			
	R				PT1	0			
					PT0	0			
EEH	PT7	PT6	PT5	PT4	PT7	0			MSB Programmable timer data (high-order 4 bits) LSB
					PT6	0			
	R				PT5	0			
					PT4	0			

Table 1.4.1(h) I/O memory map (F0H–FCH)

Address *7	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
F0H	0	0	0	EIPT	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R			R/W	0 *5	– *2			Unused
					EIPT	0	Enable	Mask	Interrupt mask register (programmable timer)
F1H	0	EISIFE	EISIFT	EISIFR	0 *5	– *2			Unused
					EISIFE	0	Enable	Mask	Interrupt mask register (serial I/F error)
	R	R/W			EISIFT	0	Enable	Mask	Interrupt mask register (serial I/F transmitting)
					EISIFR	0	Enable	Mask	Interrupt mask register (serial I/F receiving)
F2H	0	0	0	EIK1	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R			R/W	0 *5	– *2			Unused
					EIK1	0	Enable	Mask	Interrupt mask register (K10–K13)
F3H	0	0	0	EIK0	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R			R/W	0 *5	– *2			Unused
					EIK0	0	Enable	Mask	Interrupt mask register (K00–K03)
F4H	EIT3	EIT2	EIT1	EIT0	EIT3	0	Enable	Mask	Interrupt mask register (clock timer 1 Hz)
					EIT2	0	Enable	Mask	Interrupt mask register (clock timer 2 Hz)
	R/W				EIT1	0	Enable	Mask	Interrupt mask register (clock timer 8 Hz)
					EIT0	0	Enable	Mask	Interrupt mask register (clock timer 16 Hz)
									* When f_{OSC1} = 50 kHz: 16 Hz → 12.5 Hz
F8H	0	0	0	IPT	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R				0 *5	– *2			Unused
					IPT *4	0	Yes	No	Interrupt factor flag (programmable timer)
F9H	0	ISIFE	ISIFT	ISIFR	0 *5	– *2			Unused
					ISIFE*4	0	Yes	No	Interrupt factor flag (serial I/F error)
	R				ISIFT*4	0	Yes	No	Interrupt factor flag (serial I/F transmitting)
					ISIFR*4	0	Yes	No	Interrupt factor flag (serial I/F receiving)
FAH	0	0	0	IK1	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R				0 *5	– *2			Unused
					IK1 *4	0	Yes	No	Interrupt factor flag (K10–K13)
FBH	0	0	0	IK0	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R				0 *5	– *2			Unused
					IK0 *4	0	Yes	No	Interrupt factor flag (K00–K03)
FCH	IT3	IT2	IT1	IT0	IT3 *4	0	Yes	No	Interrupt factor flag (clock timer 1 Hz)
					IT2 *4	0	Yes	No	Interrupt factor flag (clock timer 2 Hz)
	R				IT1 *4	0	Yes	No	Interrupt factor flag (clock timer 8 Hz)
					IT0 *4	0	Yes	No	Interrupt factor flag (clock timer 16 Hz)
									* When f_{OSC1} = 50 kHz: 16 Hz → 12.5 Hz

CHAPTER 2 INITIAL RESET

2.1 Internal Register at Initial Resetting

The CPU core and peripheral circuits are initialized by initial resetting as follows:

Table 2.1.1 Initial values

CPU core			
Name	Symbol	Number of bits	Setting value
Program counter step	PCS	8	00H
Program counter page	PCP	4	1H
Program counter bank	PCB	1	0
New page pointer	NPP	4	1H
New bank pointer	NBP	1	0
Stack pointer	SP	8	Undefined
Index register IX	IX	12	Undefined
Index register IY	IY	12	Undefined
Register pointer	RP	4	Undefined
General-purpose register A	A	4	Undefined
General-purpose register B	B	4	Undefined
Interrupt flag	I	1	0
Decimal flag	D	1	0
Zero flag	Z	1	Undefined
Carry flag	C	1	Undefined

Peripheral circuits		
Name	Number of bits	Setting value
RAM	4	Undefined
Display memory	4	Undefined
Other peripheral circuits	—	*

* See Tables 1.4.1(a)–(h).

Note: Undefined values must be defined by the program.

2.2 Example Program for the System Initialization

Following program shows the example of the procedure for system initialization.

```
Label     Mnemonic/operand          Comment
;
;INITIAL RESET PROGRAM FOR E0C6247
;
ORG     100H
        JP      INIT              ;Program initial routine

ORG     10EH
        JP      TINT              ;Timer interrupt routine

ORG     110H
INIT:   ;INITIAL RESET
        RST     F,0000B           ;Resets flags

        LD      A,0H
        LD      SPL,A
        LD      A,8H
        LD      SPH,A             ;Sets stack pointer to 80H

        LD      B,0H
        LD      XP,B              ;Sets to page 0
        LD      X,088H            ;OSC1 prescaler selection
        LD      MX,0H             ;When 32,768[Hz] is selected for OSC1
                                  When the OSC1 oscillation frequency is other
                                  than 32,768[Hz], set proper value accordingly.
        LD      X,0F4H
        LD      MX,1000B          ;Enables interrupt mask register (1Hz)

        LD      X,08CH
        LD      MX,0001B          ;Resets clock timer
        LD      MX,0010B          ;Shifts clock timer to RUN status

        EI                        ;Enables interrupts

;RAM CLEAR: Sets 100H-17FH, 200H-27FH, 300H-37FH and 400H-8FFH to 0H
        LD      A,1H              ;Sets to page 1
        LD      X,00H
RAMPSET:
        CP      A,9H              ;Goes to SRAM CLEAR if it is page 9
        JP      Z,SRAMCLR
        LD      XP,A              ;Page setting
RAMCLR:                           ;Clears X00H-X7FH
        LDPX    MX,0H
        CP      XH,08H
        JP      NZ,RAMCLR

        CP      A,4H              ;Checks current page (within 1 to 3 ?)
        JP      C,NEXTPAGE

RAMCLR80:                         ;Clears X80H-X8FH
        LDPX    MX,0H
        CP      XH,00H
        JP      NZ,RAMCLR80

NEXTPAGE:
        ADD     A,1H              ;Sets to next page
        LD      X,00H             ;Sets address to 00H
        JP      RAMPSET
```

```
;SRAM CLEAR: Sets A00H-AFFH to 0H
SRAMCLR:
        LD      A,0AH
        LD      XP,A            ;Sets to page 0AH
        LD      X,00H           ;Sets address to 00H
SRAMIN:
        LDPX    MX,0H
        CP      XH,0H
        JP      NZ,SRAMIN
        CP      XL,0H
        JP      NZ,SRAMIN
;
;
;
        :
        : (Application program)
        :
TINT:
        PUSH    YH
        PUSH    YL
        PUSH    A

        LD      Y,0FCH          ;Reads clock timer
        LD      A,MY            ;interrupt factor flag
        LD      Y,08BH          ;Resets watchdog timer
        LD      MY,0001B

        POP     A
        POP     YL
        POP     YH

        EI
        RET
```

2.3 Programming Notes for the System Initialization

(1) In some of initial registers and initial data memory area, the initial value is undefined after reset. Set them proper initial values by the program, as necessary.

(2) Be sure to set the OSC1 prescaler selection register (address 88H) to a value according to the OSC1 oscillation frequency before starting the clock timer. If it is not done properly, the frequency of the clock timer will differ from that indicated in the I/O memory map.

CHAPTER 3 PERIPHERAL CIRCUITS

3.1 Watchdog Timer

3.1.1 I/O memory of the watchdog timer

The control register of the watchdog timer is shown in Table 3.1.1.1.

Table 3.1.1.1 Control register of watchdog timer

Address *7	Register				Name	Init *1	1	0	Comment
	D3	D2	D1	D0					
8BH	0	0	0	WDRST	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R			W	0 *5	– *2			Unused
					WDRST *5	Reset	Reset	–	Watchdog timer reset

*1 Initial value at the time of initial reset
*2 Not set in the circuit
*3 Undefined
*4 Reset (0) immediately after being read
*5 Constantly "0" when being read
*6 Refer to main manual
*7 I/O memory is allocated from page 0 to 3

3.1.2 Example program for the watchdog timer

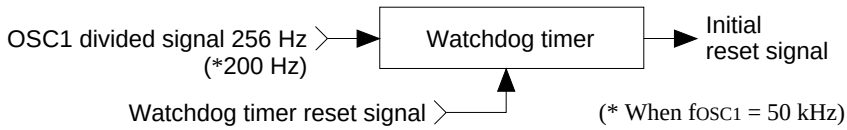


Fig. 3.1.2.1 Configuration of watchdog timer

Following program shows the reset procedure for watchdog timer.

```
Label     Mnemonic/operand          Comment
;
;RESET WATCHDOG TIMER
;
        LD      A,00H
        LD      XP,A              ;Sets to page 0
;
        LD      X,8BH
        OR      MX,0001B          ;Resets watchdog timer
;
```

3.1.3 Programming note

When the watchdog timer is being used, the software must reset it within 3-second cycles.
When "Not used" is selected for the watchdog timer by the mask option, it is unnecessary to reset the watchdog timer.

3.2 Oscillation Circuit

3.2.1 I/O memory of the oscillation circuit

The control registers of the oscillation circuit are shown in Table 3.2.1.1.

Table 3.2.1.1 Control registers of oscillation circuit

Address *7	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
88H	0	0	PRSM1	PRSM0	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R		R/W		PRSM1	0			OSC1 prescaler selection
					PRSM0	0			
89H	CLKCHG	OSCC	VDC1	VDC0	CLKCHG	0	OSC3	OSC1	CPU system clock switch
					OSCC	0	On	Off	OSC3 oscillation On/Off
	R/W				VDC1	0			CPU operating voltage switch
					VDC0	0			

PRSM[1][0] / fOSC1 (kHz): 1 1 — 76.8; 1 0 — 50.0; 0 1 — 38.4; 0 0 — 32.768

VDC[1][0] / VD1 / Oscillation circuit: 1 * — 2.1 V — OSC3 (1 MHz); 0 1 — 1.4 V — OSC3 (200 kHz); 0 0 — 1.2 V — OSC1

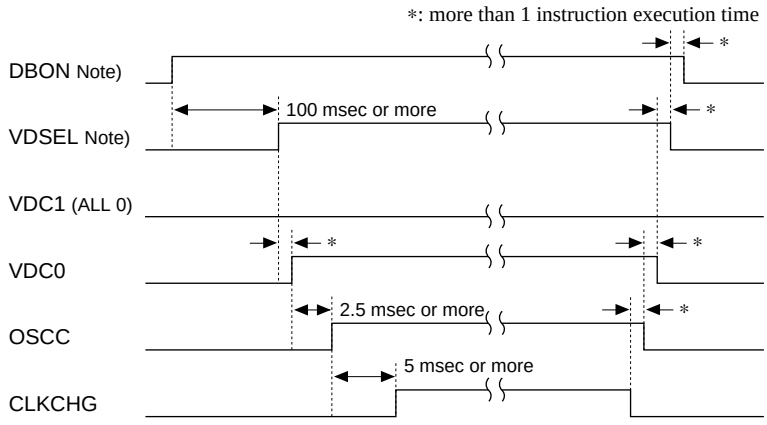
*1 Initial value at the time of initial reset
*2 Not set in the circuit
*3 Undefined
*4 Reset (0) immediately after being read
*5 Constantly "0" when being read
*6 Refer to main manual
*7 I/O memory is allocated from page 0 to 3

Table 3.2.1.2 shows the correspondence of the system clock and operating voltage.

Table 3.2.1.2 System clock and operating voltage

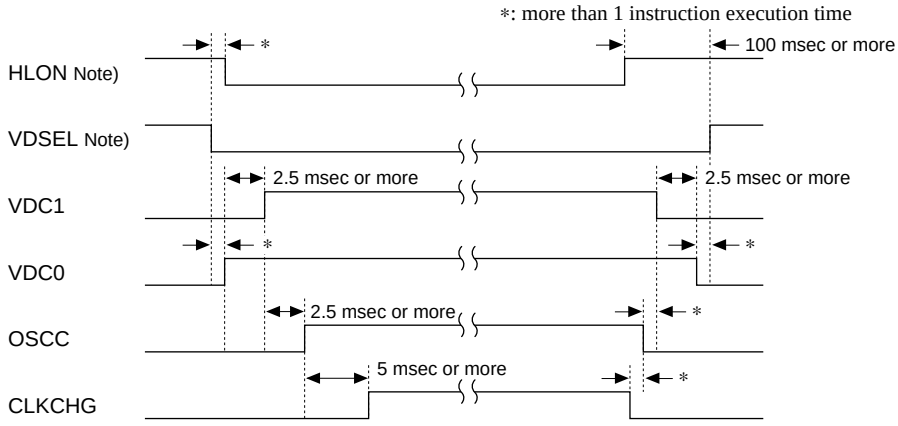
System clock	Operating voltage VD1 (V)	Operating mode according to VDD (V) 0.9–1.25	1.25–2.2	2.2–2.6	2.6–3.6
OSC1	1.2	Boost mode	Normal mode*		Reduce or normal mode
OSC3, 200 kHz	approx. 1.4	Boost mode		Normal mode*	
OSC3, 1 MHz	2.1	Cannot be used		Normal mode	

* Set the boost mode when supply voltage drop is detected by the SVD circuit, such as during heavy load operation (buzzer sounds or a lamp lights) or by the battery life.



Note) Use DBON and VDSEL only when changes are required.

Fig. 3.2.1.1(a) Timing chart of system clock switching OSC1 ↔ OSC3 (200 kHz)



Note) When the reduce mode is used. However, when using the reduce mode in the LCD system voltage circuit (VCSEL = "1"), HLON should be set to "1".

Fig. 3.2.1.1(b) Timing chart of system clock switching OSC1 ↔ OSC3 (1 MHz)

3.2.2 Example program for the oscillation circuit

Following programs show the CPU system clock switching procedure.

• Clock control when OSC3 = 200 kHz

```
Label     Mnemonic/operand          Comment
;
;OSCILLATION CLOCK CONTROL
;       SWITCHING FROM OSC1 TO OSC3 (200[kHz])
;
CLKOSC3:
        LD      A,0H
        LD      XP,A            ;Sets to page 0

        LD      X,084H          ;Sets address to 84H
        FAN     MX,0010B        ;Checks halver status: ON ?
        JP      Z,CHKVDD        ;Checks VDD if halver is OFF

;When halver is ON: Sets to VDSEL = VDD, OSC3 (200[kHz])
        AND     MX,1011B        ;Sets to VDSEL = VDD
        JP      OSC3SET         ;Goes to OSC3 (200[kHz]) setting

CHKVDD:
        LD      X,080H          ;Sets address to 80H
        LD      MX,1100B        ;Sets SVD criteria voltage to 2.20[V]
        LD      X,081H          ;Sets address to 81H
        LD      MX,0001B        ;Turns SVD circuit ON
;
        CALL    W100US          ;Waits for 100[µs]
;
        FAN     MX,0010B        ;Checks SVD data
        JP      Z,OSC3SET       ;Go to OSC3 setting if it is 2.20[V] or more
;
;When the voltage is less than 2.2[V]: Turns doubler ON, VDSEL = VD2
        LD      X,084H          ;Sets address 84H
        LD      MX,0001B        ;Doubler ON
        CALL    W100MS          ;Waits for 100[ms]
                                ;to stabilize doubling voltage
        OR      MX,0100B        ;Sets to VDSEL = VD2
```

```
OSC3SET:
        LD      X,089H          ;Sets address to 89H
        LD      MX,0001B        ;Sets to VD1 = 1.5[V], OSC3(200[kHz])
        CALL    W2_5MS          ;Waits for 2.5[ms]
        OR      MX,0100B        ;Turns OSC3 oscillation ON
        CALL    W5MS            ;Waits for 5[ms]
        OR      MX,1000B        ;Sets CPU clock to OSC3

        LD      X,081H          ;Sets address to 81H
        AND     MX,1110B        ;Turns SVD circuit OFF

        RET

W100MS:
        ;100[ms] wait routine
        RET

W100US:
        ;100[µs] wait routine
        RET

W2_5MS:
        ;2.5[ms] wait routine
        RET

W5MS:
        ;5[ms] wait routine
        RET
;
;OSCILLATION CLOCK CONTROL
;       SWITCHING FROM OSC3(200[kHz]) TO OSC1
;
CLKOSC1:
        LD      A,0H
        LD      XP,A            ;Sets to page 0
        LD      X,089H          ;Sets address to 89H
        AND     MX,0111B        ;Sets CPU clock to OSC1
        AND     MX,0011B        ;Turns OSC3 oscillation OFF
        AND     MX,0000B        ;Sets to VD1 = 1.2[V], OSC1

;OPERATING MODE SETTING FOR OSCILLATION SYSTEM REGULATED VOLTAGE CIRCUIT
        LD      X,080H          ;Sets address to 80H
        LD      MX,0100B        ;Sets SVD criteria voltage to 1.25[V]
        LD      X,081H          ;Sets address to 81H
        LD      MX,0001B        ;Turns SVD circuit ON
;
        CALL    W100US          ;Waits for 100[µs]
;
        FAN     MX,0010B        ;Checks SVD data
        JP      NZ,ENDOSC1      ;Terminates setting if it is 1.25[V] or less
;
        LD      X,080H          ;Sets address to 80H
        LD      MX,1111B        ;Sets SVD criteria voltage to 2.6[V]
        LD      X,081H          ;Sets address to 81H
        LD      MX,0001B        ;Turns SVD circuit ON
;
        CALL    W100US          ;Waits for 100[µs]
;
        FAN     MX,0010B        ;Checks SVD data
        JP      Z,HALVSET       ;Sets reduce mode if it is 2.6[V] or more
```

```
;When VDD is 1.25[V]-2.6[V]: Sets normal mode
        LD      X,084H          ;Sets address to 84H
        AND     MX,1011B        ;Sets to VDSEL = VDD
        AND     MX,1100B        ;Sets to DBON = OFF
        JP      ENDOSC1

;When VDD is 2.6[V] or more: Sets reduce mode
HALVSET:
        LD      X,084H          ;Sets address to 84H
        OR      MX,0010B        ;Halver ON
        CALL    W100MS          ;Waits for 100[ms] to stabilize halving voltage
        OR      MX,0100B        ;Sets to VDSEL = VD2
;
ENDOSC1:
        LD      X,081H          ;Sets address to 81H
        AND     MX,1110B        ;Turns SVD circuit OFF

        RET
```

• Clock control when OSC3 = 1 MHz

Label	Mnemonic/operand	Comment

```
;
;OSCILLATION CLOCK CONTROL
;       SWITCHING FROM OSC1 TO OSC3 (1[MHz])
;
CLK1M:
        LD      A,0H
        LD      XP,A        ;Sets to page 0
;
        LD      X,080H      ;Sets address to 80H
        LD      MX,1100B    ;Sets SVD criteria voltage to 2.20[V]
        LD      X,081H      ;Sets address to 81H
        LD      MX,0001B    ;Turns SVD circuit ON
;
        CALL    W100US      ;Waits for 100[µs]
;
        FAN     MX,0010B    ;Checks SVD data
        JP      NZ,END1M    ;OSC3 (1[MHz]) cannot be set if it is 2.20[V] or less

        LD      X,084H      ;Sets address to 84H
        AND     MX,1011B    ;Sets to VDSEL = VDD
        AND     MX,1000B
;
        LD      X,089H      ;Sets address to 89H
        LD      MX,0001B    ;Sets to VD1 = 1.5[V]
        CALL    W2_5MS      ;Waits for 2.5[ms]
        LD      MX,0011B    ;Sets to VD1 = 2.1[V], OSC3 (1[MHz])
        CALL    W2_5MS      ;Waits for 2.5[ms]
;
        OR      MX,0100B    ;Turns OSC3 oscillation ON
        CALL    W5MS        ;Waits for 5[ms]
        OR      MX,1000B    ;Sets CPU clock to OSC3
END1M:
        LD      X,081H      ;Sets address to 81H
        AND     MX,1110B    ;Turns SVD circuit OFF

        RET

W100US:
        ;100[µs] wait routine
        RET
```

```
W100MS:
        ;100[ms] wait routine
        RET

W2_5MS:
        ;2.5[ms] wait routine
        RET

W5MS:
        ;5[ms] wait routine
        RET
;
;OSCILLATION CLOCK CONTROL
;       SWITCHING FROM OSC3(1[MHz]) TO OSC1
;
SETOSC1:
        LD      A,0H
        LD      XP,A            ;Sets to page 0
        LD      X,089H          ;Sets address to 89H
        AND     MX,0111B        ;Sets CPU clock to OSC1
        AND     MX,0011B        ;Turns OSC3 oscillation OFF
        AND     MX,0001B        ;Sets to VD1 = 1.5[V], OSC1
        CALL    W2_5MS          ;Waits for 2.5[ms]
        AND     MX,0000B        ;Sets to VD1 = 1.2[V], OSC1

;OPERATING MODE SETTING
;FOR OSCILLATION SYSTEM REGULATED VOLTAGE CIRCUIT
        LD      X,080H          ;Sets address to 80H
        LD      MX,1111B        ;Sets SVD criteria voltage to 2.6[V]
        LD      X,081H          ;Sets address to 81H
        LD      MX,0001B        ;Turns SVD circuit ON
;
        CALL    W100US          ;Waits for 100[µs]
;
        FAN     MX,0010B        ;Checks SVD detection data
        JP      Z,OSC1END       ;Terminates setting if it is 2.6[V] or less

;When VDD is 2.6[V] or more: Sets reduce mode
        LD      X,084H          ;Turns address to 84H
        OR      MX,0010B        ;Halver ON
        CALL    W100MS          ;Waits for 100[ms]
                                ;to stabilize halving voltage
        OR      MX,0100B        ;Sets to VDSEL = VD2
;
OSC1END:
        LD      X,081H          ;Sets address to 81H
        AND     MX,1110B        ;Turns SVD circuit OFF

        RET

W100MS:
        ;100[ms] wait routine
        RET
```

3.2.3 Programming notes

(1) When switching the CPU system clock from OSC1 to OSC3, set V_{D1} and the operating mode before turning the OSC3 oscillation ON. After that maintain 2.5 msec or more, and then turn the OSC3 oscillation ON.
When switching from OSC3 to OSC1, set V_{D1} and the operating mode after switching to OSC1 and turning the OSC3 oscillation OFF.

(2) When switching V_{D1} from 1.2 V to 2.1 V, or vice versa, be sure to hold the 1.4 V setting for more than 2.5 msec or more first for voltage stabilization.

(3) It takes at least 5 msec from the time the OSC3 oscillation circuit goes ON until the oscillation stabilizes. Consequently, when switching the CPU operation clock from OSC1 to OSC3, do this after a minimum of 5 msec have elapsed since the OSC3 oscillation went ON.
Further, the oscillation stabilization time varies depending on the external oscillator characteristics and conditions of use, so allow ample margin when setting the wait time.

(4) When switching the clock form OSC3 to OSC1, use a separate instruction for switching the OSC3 oscillation OFF. An error in the CPU operation can result if this processing is performed at the same time by the one instruction.

(5) Switching the operating voltage when the supply voltage is lower than the set voltage (that can generate V_{D1}) may cause a malfunction. Switch the operating voltage only after making sure that supply voltage is more than the set voltage using the SVD circuit.

(6) The OSC1 oscillation circuit deal with four types of crystal oscillators (32.768 kHz, 38.4 kHz, 50 kHz or 76.8 kHz). To operate the timer and other circuits properly, the prescaler should be selected according to the frequency of the connected oscillator.

3.3 Input Ports

3.3.1 I/O memory of the input ports

The control registers of the input ports are shown in Table 3.3.1.1.

Table 3.3.1.1 Control registers of input ports

Address *7	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
90H	SIK03	SIK02	SIK01	SIK00	SIK03	0	Enable	Disable	K00–K03 interrupt selection register
					SIK02	0	Enable	Disable	
	R/W				SIK01	0	Enable	Disable	
					SIK00	0	Enable	Disable	
91H	K03	K02	K01	K00	K03	– *2	High	Low	K00–K03 input port data
					K02	– *2	High	Low	
	R				K01	– *2	High	Low	
					K00	– *2	High	Low	
92H	KCP03	KCP02	KCP01	KCP00	KCP03	1	↓	↑	K00–K03 input comparison register
					KCP02	1	↓	↑	
	R/W				KCP01	1	↓	↑	
					KCP00	1	↓	↑	
94H	SIK13	SIK12	SIK11	SIK10	SIK13	0	Enable	Disable	K10–K13 interrupt selection register
					SIK12	0	Enable	Disable	
	R/W				SIK11	0	Enable	Disable	
					SIK10	0	Enable	Disable	
95H	K13	K12	K11	K10	K13	– *2	High	Low	K10–K13 input port data
					K12	– *2	High	Low	
	R				K11	– *2	High	Low	
					K10	– *2	High	Low	
96H	KCP13	KCP12	KCP11	KCP10	KCP13	1	↓	↑	K10–K13 input comparison register
					KCP12	1	↓	↑	
	R/W				KCP11	1	↓	↑	
					KCP10	1	↓	↑	
F2H	0	0	0	EIK1	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R			R/W	0 *5	– *2			Unused
					EIK1	0	Enable	Mask	Interrupt mask register (K10–K13)
F3H	0	0	0	EIK0	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R			R/W	0 *5	– *2			Unused
					EIK0	0	Enable	Mask	Interrupt mask register (K00–K03)
FAH	0	0	0	IK1	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R				0 *5	– *2			Unused
					IK1 *4	0	Yes	No	Interrupt factor flag (K10–K13)
FBH	0	0	0	IK0	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R				0 *5	– *2			Unused
					IK0 *4	0	Yes	No	Interrupt factor flag (K00–K03)

*1 Initial value at the time of initial reset
*2 Not set in the circuit
*3 Undefined
*4 Reset (0) immediately after being read
*5 Constantly "0" when being read
*6 Refer to main manual
*7 I/O memory is allocated from page 0 to 3

3.3.2 Configuration of input port

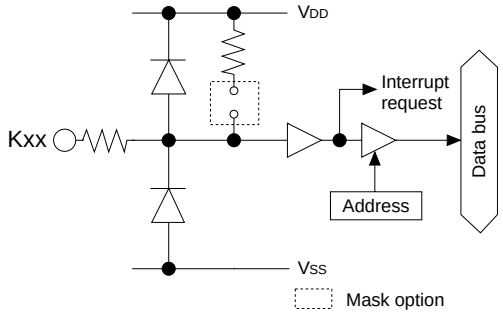


Fig. 3.3.2.1 Configuration of input port

3.3.3 Interrupt function

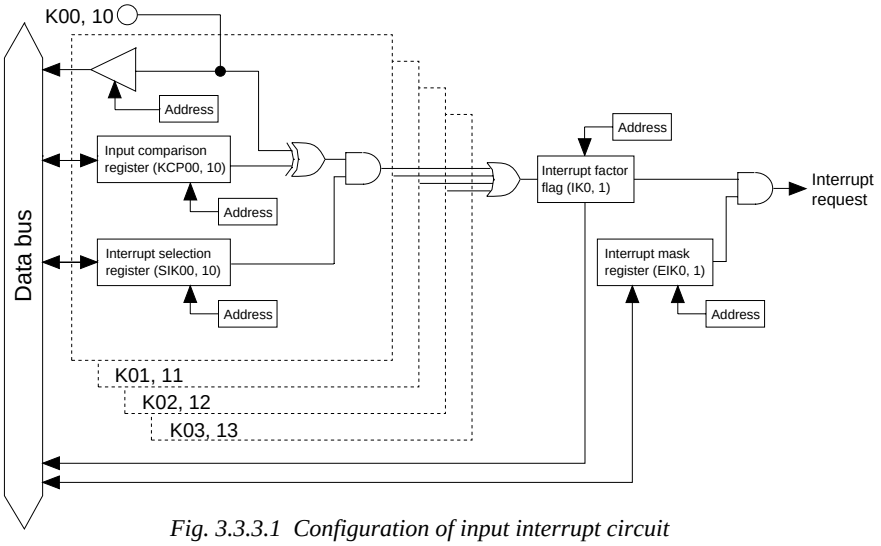


Fig. 3.3.3.1 Configuration of input interrupt circuit

Interrupt selection register

SIK03	SIK02	SIK01	SIK00
1	1	1	0

Input comparison register

KCP03	KCP02	KCP01	KCP00
1	0	1	0

With the above setting, the interrupt of K00–K03 is generated under the following condition:

Input port

	K03	K02	K01	K00	
(1)	1	0	1	0	(Initial value)
	↓				
(2)	K03	K02	K01	K00	
	1	0	1	1	
	↓				
(3)	K03	K02	K01	K00	
	0	0	1	1	→ Interrupt generation
	↓				
(4)	K03	K02	K01	K00	
	0	1	1	1	

Because K00 interrupt is set to disable, interrupt will be generated when no matching occurs between the contents of the 3 bits K01–K03 and the 3 bits input comparison register KCP01–KCP03.

Fig. 3.3.3.2 Example of interrupt for K00–K03

3.3.4 Example program for the input ports

Following program shows the input ports controlling procedure.

```
Label     Mnemonic/operand          Comment
;
;INPUT PORT
;

;EXAMPLE PROGRAM FOR INITIALIZATION OF INPUT PORT
KNINIT:
        LD      A,00H
        LD      XP,A            ;Sets to page 0
;
        LD      X,90H           ;Sets address to 90H
        LD      MX,0FH          ;Sets K0n interrupt selection register to enable
;
        LD      X,94H           ;Sets address to 94H
        LD      MX,0FH          ;Sets K1n interrupt selection register to enable
;
        DI
        LD      X,0F2H          ;Sets address to F2H
        LBPX    MX,0001B        ;Sets interrupt mask register (K10-K13) to enable
        LD      MX,0001B        ;Sets interrupt mask register (K00-K03) to enable
        EI
        RET
;
;
K0INT:
;K0n INTERRUPT PROCESSING
        PUSH    YP              ;Evacuates registers that are used in
        PUSH    YH              ;the interrupt processing routine (Y, A)
        PUSH    YL
        PUSH    A

        LD      A,00H
        LD      YP,A            ;Sets to page 0

        LD      Y,0FBH          ;Sets address to FBH
        LD      A,MY            ;Reads interrupt factor flag
;
;       Interrupt processing program
;
        POP     A
        POP     YL
        POP     YH
        POP     YP

        EI
        RET
;
;
K1INT:
;K1n INTERRUPT PROCESSING
        PUSH    YP              ;Evacuates registers that are used in
        PUSH    YH              ;the interrupt processing routine (Y, A)
        PUSH    YL
        PUSH    A

        LD      A,00H
        LD      YP,A            ;Sets to page 0

        LD      Y,0FAH          ;Sets address to FAH
        LD      A,MY            ;Reads interrupt factor flag
;
```

```
;       Interrupt processing program
;
        POP     A
        POP     YL
        POP     YH
        POP     YP

        EI
        RET
```

3.3.5 Programming notes

(1) When input ports are changed from low to high by pull up resistor, the rise of the waveform is delayed on account of the time constant of the pull up resistor and input gate capacitance. Hence, when fetching input ports, set an appropriate wait time.
Particular care needs to be taken of the key scan during key matrix configuration.
Make this waiting time the amount of time or more calculated by the following expression.
$10 \times C \times R$
C: terminal capacitance 5 pF + parasitic capacitance ? pF
R: pull up resistance 300 kΩ

(2) The K02 terminal functions as the clock input terminal for the programmable timer, and the input signal is combined with the input port and the programmable timer. Consequently, when the K02 terminal is set to the clock input terminal for the programmable timer, take care of the interrupt setting.

(3) Reading of interrupt factor flags is available at EI, but be careful in the following cases.
If the interrupt mask register value corresponding to the interrupt factor flags to be read is set to "1", an interrupt request will be generated by the interrupt factor flags set timing, or an interrupt request will not be generated.

(4) Write the interrupt mask register (EIK) only in the DI status (interrupt flag = "0"). Writing during EI status (interrupt flag = "1") will cause malfunction.

3.4 Output Ports

3.4.1 I/O memory of the output ports

The control registers of the output ports are shown in Table 3.4.1.1.

Table 3.4.1.1 Control registers of output ports

Address *7	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
98H	EXTMF	0	MEMS1	MEMS0	EXTMF	0	On	Off	External memory access function control
					0 *5	– *2			Unused
					MEMS1	0			External memory size selection: MEMS [1][0] — 1 1: 1M (R only) (A00–A16); 1 0: 512K (R/W) (A00–A15); 0 1: 256K (R/W) (A00–A14); 0 0: 64K (R/W) (A00–A12)
					MEMS0	0			
	R/W	R	R/W						
A0H	0	0	0	R0HIZ	0 *5	– *2			Unused
					0 *5	– *2			Unused
					0 *5	– *2			Unused
	R			R/W	R0HIZ	0	High-Z	Output	* R0HIZ functions as a general-purpose register when EXTMF = 1. R0 output high-impedance control (EXTMF = 0)
A1H	R03	R02	R01	R00	R03	1	High	Low	R00–R03 output port data (EXTMF = 0) Functions as a general-purpose register when EXTMF = 1.
					R02	1	High	Low	
					R01	1	High	Low	
	R/W				R00	1	High	Low	
A2H	0	0	0	R1HIZ	0 *5	– *2			Unused
					0 *5	– *2			Unused
					0 *5	– *2			Unused
	R			R/W	R1HIZ	0	High-Z	Output	* R1HIZ functions as a general-purpose register when EXTMF = 1. R1 output high-impedance control (EXTMF = 0)
A3H	R13	R12	R11	R10	R13	1	High	Low	R10–R13 output port data (EXTMF = 0) Functions as a general-purpose register when EXTMF = 1.
					R12	1	High	Low	
					R11	1	High	Low	
	R/W				R10	1	High	Low	
A4H	0	0	0	R2HIZ	0 *5	– *2			Unused
					0 *5	– *2			Unused
					0 *5	– *2			Unused
	R			R/W	R2HIZ	0	High-Z	Output	* R2HIZ functions as a general-purpose register when EXTMF = 1. R2 output high-impedance control (EXTMF = 0)
A5H	R23	R22	R21	R20	R23	1	High	Low	R20–R23 output port data (EXTMF = 0) Functions as a general-purpose register when EXTMF = 1.
					R22	1	High	Low	
					R21	1	High	Low	
	R/W				R20	1	High	Low	
A6H	R33HIZ	R32HIZ	R31HIZ	R30HIZ	R33HIZ	0	High-Z	Output	R30–R33 output high-impedance control Bit corresponding to the address bus for external memory can be used as a general-purpose register when EXTMF = 1.
					R32HIZ	0	High-Z	Output	
					R31HIZ	0	High-Z	Output	
	R/W				R30HIZ	0	High-Z	Output	
A7H	R33	R32	R31	R30	R33	1	High	Low	R30–R33 output port data Bit corresponding to the address bus for external memory can be used as a general-purpose register when EXTMF = 1.
					R32	1	High	Low	
					R31	1	High	Low	
	R/W				R30	1	High	Low	
A8H	R43HIZ	R42HIZ	R41HIZ	R40HIZ	R43HIZ	0	High-Z	Output	R43 output high-impedance control
					R42HIZ	0	High-Z	Output	R42 output high-impedance control
					R41HIZ	0	High-Z	Output	R41 output high-impedance control (EXTMF = 0) (General-purpose register when EXTMF = 1)
	R/W				R40HIZ	0	High-Z	Output	R40 output high-impedance control (EXTMF = 0) (General-purpose register when EXTMF = 1)
A9H	R43	R42	R41	R40	R43	0	High	Low	R43 output port data (SELR43 = 0) (General-purpose register when BZ output is selected)
					R42	0	High	Low	R42 output port data (SELR42 = 0) (General-purpose register when $\overline{BZ}$ output is selected)
					R41	1	High	Low	R41 output port data (EXTMF = 0) (General-purpose register when EXTMF = 1)
	R/W				R40	1	High	Low	R40 output port data (EXTMF = 0) (General-purpose register when EXTMF = 1)
AAH	SELR43	SELR42	0	0	SELR43	0	BZ	Normal	R43 function selection register (BZ or general-purpose output)
					SELR42	0	$\overline{BZ}$	Normal	R42 function selection register ($\overline{BZ}$ or general-purpose output)
	R/W		R		0 *5	– *2			Unused
					0 *5	– *2			Unused

*1 Initial value at the time of initial reset
*2 Not set in the circuit
*3 Undefined
*4 Reset (0) immediately after being read
*5 Constantly "0" when being read
*6 Refer to main manual
*7 I/O memory is allocated from page 0 to 3

3.4.2 Example program for the output ports

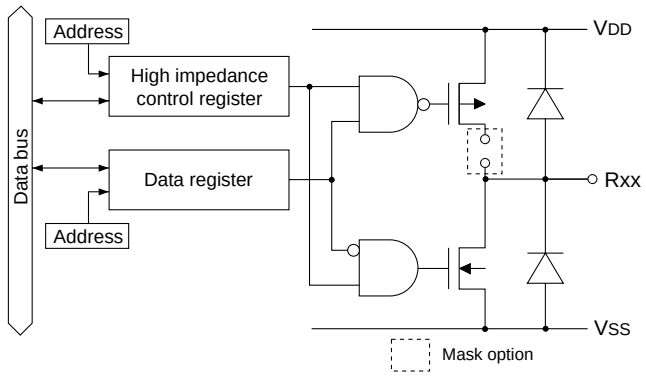


Fig. 3.4.2.1 Configuration of output port

Following program shows the output ports controlling procedure in ordinary DC output case.

```
Label     Mnemonic/operand          Comment
;
;OUTPUT PORT
;

;EXAMPLE PROGRAM FOR INITIALIZATION OF OUTPUT PORT
RNINIT:
        LD      A,00H
        LD      XP,A            ;Sets to page 0
;
        LD      X,98H           ;Sets address to 98H
        LD      MX,0000B        ;Sets external memory access function
                                ;to OFF
;
        LD      X,0AAH          ;Sets address AAH
        LD      MX,0000B        ;Sets R43 and R42 function selection
                                ;registers to NORMAL
;
        LD      X,0A0H          ;Sets address to A0H
        LD      MX,0001B        ;Sets R00-R03 to High-Z
;
        LD      X,0A2H          ;Sets address to A2H
        LD      MX,0001B        ;Sets R10-R13 to High-Z

;
        LD      X,0A4H          ;Sets address to A4H
        LD      MX,0001B        ;Sets R20-R23 to High-Z

;
        LD      X,0A6H          ;Sets address to A6H
        LD      MX,1111B        ;Sets R30-R33 to High-Z

;
        LD      X,0A8H          ;Sets address to A8H
        LD      MX,1111B        ;Sets R40-R43 to High-Z
;
;DATA SETTING
;Example:       K00-K03 ---> R00-R03, R20-R23, R40-R43
;               K10-K13 ---> R10-R13, R30-R33
;
        LD      X,91H           ;Sets address to 91H
        LD      A,MX            ;Sets K00-K03 input to A register
;
        LD      X,0A1H          ;Sets address to A1H
```

```
        LD      MX,A            ;Sets content of A register to R00-R03
;
        LD      X,0A5H          ;Sets address to A5H
        LD      MX,A            ;Sets content of A register to R20-R23
;
        LD      X,0A9H          ;Sets address to A9H
        LD      MX,A            ;Sets content of A register to R40-R43
;
        LD      X,95H           ;Sets address to 95H
        LD      B,MX            ;Sets K10-K13 input to B register
;
        LD      X,0A3H          ;Sets address to A3H
        LD      MX,B            ;Sets content of B register to R10-R13
;
        LD      X,0A7H          ;Sets address to A7H
        LD      MX,B            ;Sets contents of B register to R30-R33
;
        LD      X,0A0H          ;Sets address to A0H
        LD      MX,0000B        ;Outputs R00-R03
;
        LD      X,0A2H          ;Sets address to A2H
        LD      MX,0000B        ;Outputs R10-R13
;
        LD      X,0A4H          ;Sets address to A4H
        LD      MX,0000B        ;Outputs R20-R23
;
        LD      X,0A6H          ;Sets address to A6H
        LD      MX,0000B        ;Outputs R30-R33
;
        LD      X,0A8H          ;Sets address to A8H
        LD      MX,0000B        ;Outputs R40-R43

        RET
```

See Section 3.11, "External Memory Access", for control of external bus signals and see Section 3.10, "Sound Generator", for control of buzzer signals.

3.5 I/O Ports

3.5.1 I/O memory of the I/O ports

The control registers of the I/O ports are shown in Tables 3.5.1.1(a)–(c).

Table 3.5.1.1(a) Control registers of I/O ports

Address *7	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
B0H	IOC03	IOC02	IOC01	IOC00	IOC03	0	Output	Input	P00–P03 I/O control register (EXTMF = 0)
					IOC02	0	Output	Input	Functions as a general-purpose register
	R/W				IOC01	0	Output	Input	when EXTMF = 1.
					IOC00	0	Output	Input	
B1H	PUL03	PUL02	PUL01	PUL00	PUL03	1	On	Off	P00–P03 pull up control register (EXTMF = 0)
					PUL02	1	On	Off	Functions as a general-purpose register
	R/W				PUL01	1	On	Off	when EXTMF = 1.
					PUL00	1	On	Off	
B2H	P03	P02	P01	P00	P03	– *2	High	Low	P00–P03 I/O port data (EXTMF = 0)
					P02	– *2	High	Low	
	D03	D02	D01	D00	P01	– *2	High	Low	
					P00	– *2	High	Low	
	R/W				D03	– *2	1	0	External memory data D00–D03 (EXTMF = 1)
					D02	– *2	1	0	
					D01	– *2	1	0	
					D00	– *2	1	0	
B4H	IOC13	IOC12	IOC11	IOC10	IOC13	0	Output	Input	P10–P13 I/O control register (EXTMF = 0)
					IOC12	0	Output	Input	Functions as a general-purpose register
	R/W				IOC11	0	Output	Input	when EXTMF = 1.
					IOC10	0	Output	Input	
B5H	PUL13	PUL12	PUL11	PUL10	PUL13	1	On	Off	P10–P13 pull up control register (EXTMF = 0)
					PUL12	1	On	Off	Functions as a general-purpose register
	R/W				PUL11	1	On	Off	when EXTMF = 1.
					PUL10	1	On	Off	
B6H	P13	P12	P11	P10	P13	– *2	High	Low	P10–P13 I/O port data (EXTMF = 0)
					P12	– *2	High	Low	
	D07	D06	D05	D04	P11	– *2	High	Low	
					P10	– *2	High	Low	
	R/W				D07	– *2	1	0	External memory data D04–D07 (EXTMF = 1)
					D06	– *2	1	0	
					D05	– *2	1	0	
					D04	– *2	1	0	
B8H	IOC23	IOC22	IOC21	IOC20	IOC23	0	Output	Input	P20–P23 I/O control register (EXTMF = 0)
					IOC22	0	Output	Input	Functions as a general-purpose register
	R/W				IOC21	0	Output	Input	when EXTMF = 1.
					IOC20	0	Output	Input	
B9H	PUL23	PUL22	PUL21	PUL20	PUL23	1	On	Off	P20–P23 pull up control register (EXTMF = 0)
					PUL22	1	On	Off	Functions as a general-purpose register
	R/W				PUL21	1	On	Off	when EXTMF = 1.
					PUL20	1	On	Off	
BAH	P23	P22	P21	P20	P23	– *2	High	Low	P20–P23 I/O port data (EXTMF = 0)
					P22	– *2	High	Low	
	CS3	CS2	CS1	CS0	P21	– *2	High	Low	
					P20	– *2	High	Low	
	R/W				CS3	– *2	Disable	Active	Chip select $\overline{CS0}$–$\overline{CS3}$ active standby (EXTMF = 1)
					CS2	– *2	Disable	Active	
					CS1	– *2	Disable	Active	
					CS0	– *2	Disable	Active	

*1 Initial value at the time of initial reset
*2 Not set in the circuit
*3 Undefined
*4 Reset (0) immediately after being read
*5 Constantly "0" when being read
*6 Refer to main manual
*7 I/O memory is allocated from page 0 to 3

Table 3.5.1.1(b) Control registers of I/O ports

Address *7	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
BCH	IOC33	IOC32	IOC31	IOC30	IOC33	0	Output	Input	P33 I/O control register (SELP33 = 0) (General-purpose register when FOUT output is selected)
					IOC32	0	Output	Input	P32 I/O control register (SELP32 = 0) (General-purpose register when PTOVF output is selected)
	R/W				IOC31	0	Output	Input	P31 I/O control register (SELP31 = 0) (General-purpose register when FR output is selected)
					IOC30	0	Output	Input	P30 I/O control register (SELP30 = 0) (General-purpose register when CL output is selected)
BDH	PUL33	PUL32	PUL31	PUL30	PUL33	1	On	Off	P33 pull up control register (SELP33 = 0) (General-purpose register when FOUT output is selected)
					PUL32	1	On	Off	P32 pull up control register (SELP32 = 0) (General-purpose register when PTOVF output is selected)
	R/W				PUL31	1	On	Off	P31 pull up control register (SELP31 = 0) (General-purpose register when FR output is selected)
					PUL30	1	On	Off	P30 pull up control register (SELP30 = 0) (General-purpose register when CL output is selected)
BEH	P33	P32	P31	P30	P33	– *2	High	Low	P33 I/O port data (SELP33 = 0) (General-purpose register when FOUT output is selected)
					P32	– *2	High	Low	P32 I/O port data (SELP32 = 0) (General-purpose register when PTOVF output is selected)
	R/W				P31	– *2	High	Low	P31 I/O port data (SELP31 = 0) (General-purpose register when FR output is selected)
					P30	– *2	High	Low	P30 I/O port data (SELP30 = 0) (General-purpose register when CL output is selected)
BFH	SELP33	SELP32	SELP31	SELP30	SELP33	0	FOUT	I/O	P33 function selection register (FOUT output or I/O)
					SELP32	0	PTOVF	I/O	P32 function selection register (PTOVF output or I/O)
	R/W				SELP31	0	FR	I/O	P31 function selection register (FR output or I/O)
					SELP30	0	CL	I/O	P30 function selection register (CL output or I/O)
C0H	IOC43	IOC42	IOC41	IOC40	IOC43	0	Output	Input	P43 I/O control register (General-purpose register when SI/F (sync. slave) is selected)
					IOC42	0	Output	Input	P42 I/O control register (General-purpose register when SI/F (sync.) is selected)
	R/W				IOC41	0	Output	Input	P41 I/O control register (ESIF = 0) (General-purpose register when SI/F is selected)
					IOC40	0	Output	Input	P40 I/O control register (ESIF = 0) (General-purpose register when SI/F is selected)
C1H	PUL43	PUL42	PUL41	PUL40	PUL43	1	On	Off	P43 pull up control register (General-purpose register when SI/F (sync. slave) is selected)
					PUL42	1	On	Off	P42 pull up control register (General-purpose register when SI/F (sync. master) is selected)
	R/W				PUL41	1	On	Off	P41 pull up control register (ESIF = 0) (General-purpose register when SI/F is selected)
					PUL40	1	On	Off	P40 pull up control register (ESIF = 0) SIN pull up control register (ESIF = 1)
C2H	P43	P42	P41	P40	P43	– *2	High	Low	P43 I/O port data (General-purpose register when SI/F (sync. slave) is selected)
					P42	– *2	High	Low	P42 I/O port data (General-purpose register when SI/F (sync.) is selected)
	R/W				P41	– *2	High	Low	P41 I/O port data (ESIF = 0) (General-purpose register when SI/F is selected)
					P40	– *2	High	Low	P40 I/O port data (ESIF = 0) (General-purpose register when SI/F is selected)

*1 Initial value at the time of initial reset
*2 Not set in the circuit
*3 Undefined
*4 Reset (0) immediately after being read
*5 Constantly "0" when being read
*6 Refer to main manual
*7 I/O memory is allocated from page 0 to 3

Table 3.5.1.1(c) Control registers of I/O ports

Address *7	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
8AH	FOUTE	0	FOFQ1	FOFQ0	FOUTE	0	Enable	Disable	FOUT output enable
					0 *5	– *2			Unused
					FOFQ1	0			FOUT frequency selection: FOFQ[1][0] 1 1 fOSC3; 1 0 fOSC1; 0 1 fOSC1/8 (fOSC1/16); 0 0 fOSC1/64 (fOSC1/128) (In case of fOSC1 = 76.8 kHz)
	R/W	R	R/W		FOFQ0	0			
98H	EXTMF	0	MEMS1	MEMS0	EXTMF	0	On	Off	External memory access function control
					0 *5	– *2			Unused
					MEMS1	0			External memory size selection: MEMS[1][0] 1 1 1M (R only) (A00–A16); 1 0 512K (R/W) (A00–A15); 0 1 256K (R/W) (A00–A14); 0 0 64K (R/W) (A00–A12)
	R/W	R	R/W		MEMS0	0			
C8H	0	SMD1	SMD0	ESIF	0 *5	– *2			Unused
					SMD1	0			Serial I/F mode selection: SMD[1][0] 1 1 Asynchronous 8-bit; 1 0 Asynchronous 7-bit; 0 1 Clock synchronous slave; 0 0 Clock synchronous master
	R	R/W			SMD0	0			
					ESIF	0	SI/F	I/O	Serial I/F enable (P4 port function selection)
EAH	PNRFS	PTOE	PTRUN	PTRST	PNRFS	0	1024 Hz	256 Hz	Noise rejector clock frequency selection
					PTOE	0	Enable	Disable	PTOVF output enable
	R/W			W	PTRUN	0	Run	Stop	Programmable timer Run/Stop
					PTRST *5	– *2	Rst (reload)	–	Programmable timer reset (reload)

*1 Initial value at the time of initial reset
*2 Not set in the circuit
*3 Undefined
*4 Reset (0) immediately after being read
*5 Constantly "0" when being read
*6 Refer to main manual
*7 I/O memory is allocated from page 0 to 3

3.5.2 Configuration of I/O port

The E0C6247 has 20 bits general-purpose I/O ports. Figure 3.5.2.1 shows the configuration of the I/O port.

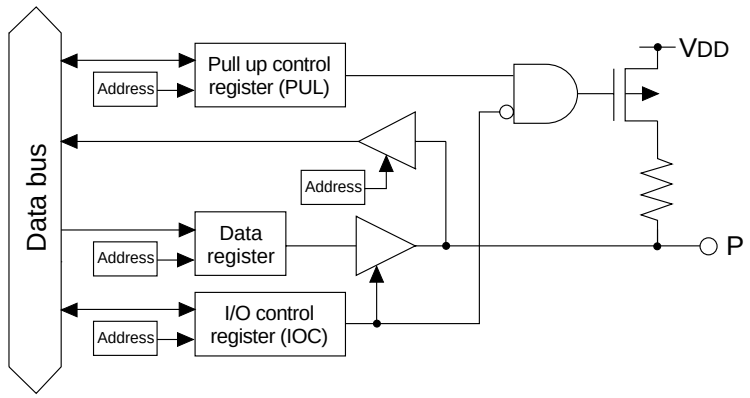


Fig. 3.5.2.1 Configuration of I/O port

20-bit I/O port terminals are shared with bus signal input/output terminals for external memory accessing, special output (CL, FR, PTOVF and FOUT) terminals and serial interface input/output terminals and these functions are selected by the software. At initial reset, these are all set to the I/O port.

Table 3.5.2.1 shows the setting of the input/output terminals by function selection.

Table 3.5.2.1 Function setting of input/output terminals

Terminal name	Terminal status at initial reset	When external memory is used *1				Special output *2				Serial interface *3		
		1M-bit	512K-bit	256K-bit	64K-bit	CL	FR	PTOVF	FOUT	Master	Slave	Async.
P00–P03	P00–P03 (Input & pull up)	D00–D03	D00–D03	D00–D03	D00–D03							
P10–P13	P10–P13 (Input & pull up)	D04–D07	D04–D07	D04–D07	D04–D07							
P20–P23	P20–P23 (Input & pull up)	$\overline{CS0}$–$\overline{CS3}$	$\overline{CS0}$–$\overline{CS3}$	$\overline{CS0}$–$\overline{CS3}$	$\overline{CS0}$–$\overline{CS3}$							
P30	P30 (Input & pull up)					CL						
P31	P31 (Input & pull up)						FR					
P32	P32 (Input & pull up)							PTOVF				
P33	P33 (Input & pull up)								FOUT			
P40	P40 (Input & pull up)									SIN(I)	SIN(I)	SIN(I)
P41	P41 (Input & pull up)									SOUT(O)	SOUT(O)	SOUT(O)
P42	P42 (Input & pull up)									$\overline{SCLK}$(O)	$\overline{SCLK}$(I)	P42
P43	P43 (Input & pull up)									P43	$\overline{SRDY}$(O)	P43

*1: EXTMF = "1" (external memory access function is ON)
*2: SELP30 = "1" (CL Output), SELP31 = "1" (FR output), SELP32 = "1" (PTOVF output), SELP33 = "1" (FOUT output)
*3: EISF = "1", Master: Clock synchronous master mode, Slave: Clock synchronous slave mode, Async.: Asynchronous mode

When these ports are used as I/O ports, each ports can be set to either input mode or output mode in a bit unit. Modes can be set by writing data to the I/O control register. Moreover, pull up resistor which is turned ON during input mode can be controlled by the software (pull up control register).

When the external memory access function is used, the data registers of P00–P03 and P10–P13 are used as the registers for the external data bus, and the data registers of P20–P23 are used to control the chip select signal outputs. The I/O control registers and pull up control registers of these ports can be used as general purpose registers.
The data registers, I/O control registers and pull up control registers of the I/O ports that are set in special outputs or input/output for the serial interface can be used as general purpose registers.
However, the pull up control registers of the port set as input for the serial interface (SIN, $\overline{SCLK}$ in the slave mode) functions as is.
See Section 3.11, "External Memory Access", for control of the input/output signals for the external bus, and see Section 3.9, "Serial Interface", for control of the serial interface.

3.5.3 Example program for the I/O ports

Following program shows the I/O ports controlling procedure.

```
Label     Mnemonic/operand          Comment
;
;I/O PORT
;

;EXAMPLE PROGRAM FOR INITIALIZATION OF I/O PORT
;Example: Sets P00-P03 to input mode
;               P10-P13 to input mode
;               P20-P23 to output mode
;               P30-P33 to special output
;               P40-P43 to output mode
PINIT:
        LD      A,00H
        LD      XP,A            ;Sets to page 0
;
        LD      X,98H           ;Sets address to 98H
        LD      MX,0000B        ;Sets external memory access function to OFF
;
        LD      X,0B0H          ;Sets address to B0H
        LD      MX,0000B        ;Sets P00-P03 to input mode
        LD      X,0B1H          ;Sets address to B1H
        LD      MX,1111B        ;Sets P00-P03 pull up control register to ON
;
        LD      X,0B4H          ;Sets address to B4H
```

```
        LD      MX,0000B        ;Sets P10-P13 to input mode
        LD      X,0B5H          ;Sets address to B5H
        LD      MX,1111B        ;Sets P10-P13 pull up control register to ON
;
        LD      X,0B8H          ;Sets address to B8H
        LD      MX,1111B        ;Sets P20-P23 to output mode
        LD      X,0BAH          ;Sets address to BAH
        LD      MX,1010B        ;Outputs data from P20-P23 port
;
        LD      X,0BFH          ;Sets address to BFH
        LD      MX,1111B        ;Sets P30-P33 as special output port
;
        LD      X,0C8H          ;Sets address to C8H
        LD      MX,0000B        ;Sets P40-P43 as I/O port
        LD      X,0C0H          ;Sets address to C0H
        LD      MX,1111B        ;Sets P40-P43 to output mode
        LD      X,0C2H          ;Sets address to C2H
        LD      MX,0101B        ;Outputs data from P40-P43 port

        RET
```

See Section 4.7, "I/O Ports", in the "Technical Hardware" for the special outputs.

3.5.4 Programming notes

(1) When in the input mode, I/O ports are changed from low to high by pull up resistor, the rise of the waveform is delayed on account of the time constant of the pull up resistor and input gate capacitance. Hence, when fetching input ports, set an appropriate wait time.
Particular care needs to be taken of the key scan during key matrix configuration.
Make this waiting time the amount of time or more calculated by the following expression.
$10 \times C \times R$
C: terminal capacitance 5 pF + parasitic capacitance ? pF
R: pull up resistance 300 kΩ

(2) When special output has been selected, a hazard may occur when the signal is turned ON or OFF.

(3) When f_{OSC3} is selected for the FOUT output clock, it is necessary to turn the OSC3 oscillation ON before output.

(4) When Nch open drain has been selected for the P10–P13 output specifications by the mask option and during output mode, read data from the P10–P13 registers (address B6H•D0–D3) may differ from the data written to them.

3.6 LCD Driver

3.6.1 I/O memory of the LCD driver

The control registers of the LCD driver are shown in Table 3.6.1.1.

Table 3.6.1.1 Control registers of LCD driver

Address *7	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
D0H	LDUTY	VCCHG	0	LPWR	LDUTY	0	1/8	1/16	LCD drive duty switch
					VCCHG	0	VC2	VC1	LCD regulated voltage switch
	R/W				0 *5	– *2			Unused
					LPWR	0	On	Off	LCD power On/Off
D1H	0	ALOFF	ALON	0	0 *5	– *2			Unused
					ALOFF	1	AllOff	Normal	All LCD dots fade out control
	R	R/W		R	ALON	0	AllOn	Normal	All LCD dots displayed control
					0 *5	– *2			Unused
D2H	LC3	LC2	LC1	LC0	LC3	– *2			LCD contrast adjustment
					LC2	– *2			LC3–LC0 = 0 Light
	R/W				LC1	– *2			:
					LC0	– *2			LC3–LC0 = 15 Dark

*1 Initial value at the time of initial reset
*2 Not set in the circuit
*3 Undefined
*4 Reset (0) immediately after being read
*5 Constantly "0" when being read
*6 Refer to main manual
*7 I/O memory is allocated from page 0 to 3

3.6.2 Display memory

The display memory is allocated to page 0AH (10) in the data memory area and the addresses and the data bits correspond to COM and SEG outputs as shown in Figure 3.6.2.1.

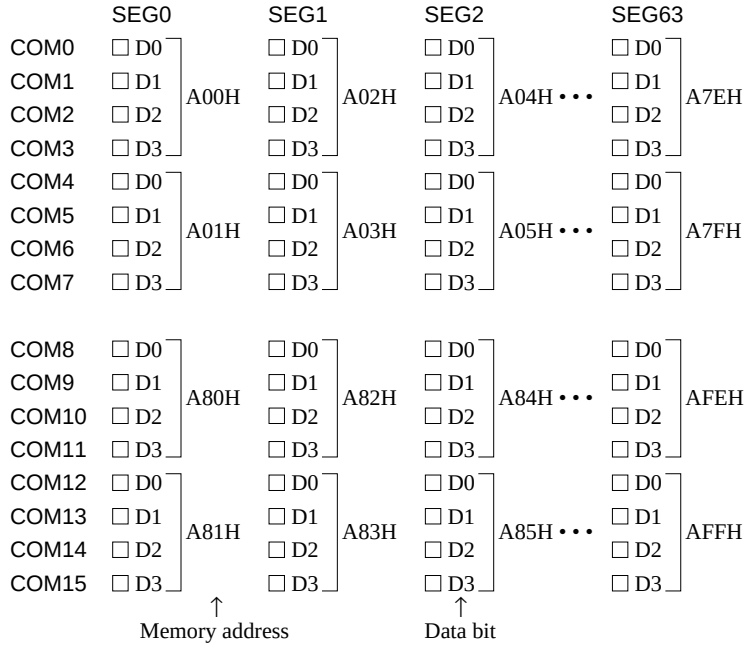


Fig. 3.6.2.1 Correspondence between display memory and LCD dot matrix

When the display memory bit is assigned as "1", the corresponding LCD dot goes ON, and when assigned as "0", the dot goes OFF.
At 1/16 duty drive, all data of COM0–COM15 is output.
At 1/8 duty drive, data only corresponding to COM0–COM7 is output.
At initial reset, the data memory content becomes undefined hence, there is need to initialize using the software.
The display memory has read/write capability, and the addresses that have not been used for LCD display can be used as general purpose registers.

3.6.3 Example program for the LCD driver

Following program shows the LCD driver initialization procedure.

```
Label     Mnemonic/operand          Comment
;
;LCD DRIVER
;

;EXAMPLE PROGRAM FOR INITIALIZATION OF LCD DRIVER
LCDINIT:
        LD      A,00H
        LD      XP,A            ;Sets to page 0
;
        LD      X,0D2H          ;Sets address to D2H
        LD      MX,0111B        ;Sets LCD contrast adjustment value
;
        LD      X,0D0H          ;Sets address to D0H
        LD      MX,0001B        ;Turn LCD power ON
        CALL    W100MS          ;Waits for 100[ms] to stabilize
                                ;LCD system voltage
        LD      X,0D1H          ;Sets address to D1H
        LD      MX,0000B        ;Sets to normal display

        RET
```

3.6.4 Programming note

Because at initial reset, the contents of display memory and LC3–LC0 (LCD contrast) are undefined, there is need to initialize by the software. Furthermore, take care of the registers LPWR and ALOFF because these are set so that the display goes OFF.

3.7 Clock Timer

3.7.1 I/O memory of the clock timer

The control registers of the clock timer are shown in Table 3.7.1.1.

Table 3.7.1.1 Control registers of clock timer

Address *7	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
88H	0	0	PRSM1	PRSM0	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R		R/W		PRSM1	0			OSC1 prescaler selection
					PRSM0	0			
8CH	0	0	TMRUN	TMRST	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R		R/W	W	TMRUN	0	Run	Stop	Clock timer Run/Stop
					TMRST *5	Reset	Reset	–	Clock timer reset
8DH	TM3	TM2	TM1	TM0	TM3	0			Clock timer data (16 Hz)
					TM2	0			Clock timer data (32 Hz)
	R				TM1	0			Clock timer data (64 Hz)
					TM0	0			Clock timer data (128 Hz)
8EH	TM7	TM6	TM5	TM4	TM7	0			Clock timer data (1 Hz)
					TM6	0			Clock timer data (2 Hz)
	R				TM5	0			Clock timer data (4 Hz)
					TM4	0			Clock timer data (8 Hz)
F4H	EIT3	EIT2	EIT1	EIT0	EIT3	0	Enable	Mask	Interrupt mask register (clock timer 1 Hz)
					EIT2	0	Enable	Mask	Interrupt mask register (clock timer 2 Hz)
	R/W				EIT1	0	Enable	Mask	Interrupt mask register (clock timer 8 Hz)
					EIT0	0	Enable	Mask	Interrupt mask register (clock timer 16 Hz)
FCH	IT3	IT2	IT1	IT0	IT3 *4	0	Yes	No	Interrupt factor flag (clock timer 1 Hz)
					IT2 *4	0	Yes	No	Interrupt factor flag (clock timer 2 Hz)
	R				IT1 *4	0	Yes	No	Interrupt factor flag (clock timer 8 Hz)
					IT0 *4	0	Yes	No	Interrupt factor flag (clock timer 16 Hz)

Comment (88H): PRSM[1][0] / fOSC1 (kHz): 1 1 — 76.8; 1 0 — 50.0; 0 1 — 38.4; 0 0 — 32.768

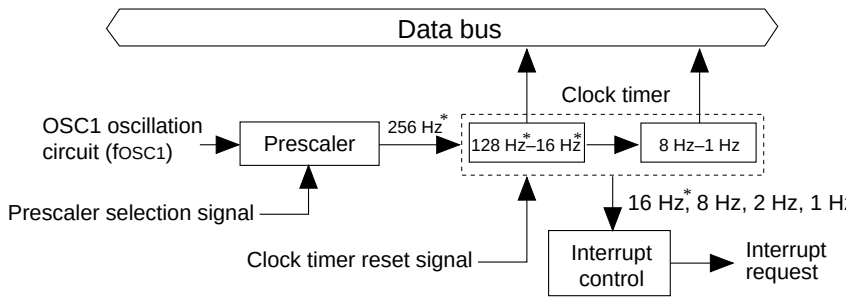
Comment (8DH): fOSC1 = 50 kHz → Clock timer data (16 Hz) (12.5 Hz); Clock timer data (32 Hz) (25 Hz); Clock timer data (64 Hz) (50 Hz); Clock timer data (128 Hz) (100 Hz)

Comment (F4H): * When fosc1 = 50 kHz: 16 Hz → 12.5 Hz

Comment (FCH): * When fOSC1 = 50 kHz: 16 Hz → 12.5 Hz

*1 Initial value at the time of initial reset
*2 Not set in the circuit
*3 Undefined
*4 Reset (0) immediately after being read
*5 Constantly "0" when being read
*6 Refer to main manual
*7 I/O memory is allocated from page 0 to 3

3.7.2 Example program for the clock timer



* indicate the frequency when fOSC1 = 32.768 kHz.

Fig. 3.7.2.1 Configuration of clock timer

Following program shows the clock timer interrupt controlling procedure.

```
Label     Mnemonic/operand          Comment
;
;CLOCK TIMER
;

;EXAMPLE PROGRAM FOR INITIALIZATION OF CLOCK TIMER
TIMINIT:
        LD      A,00H
        LD      XP,A            ;Sets to page 0
;
        LD      X,088H          ;Selects OSC1 prescaler
        LD      MX,0H           ;Setting when OSC1 = 32,768[Hz]

        LD      X,0F4H          ;Sets address to F4H
        LD      MX,1000B        ;Sets interrupt mask register (1 Hz) to enable

        LD      X,08CH          ;Sets address to 8CH
        LD      MX,0001B        ;Resets clock timer
        LD      MX,0010B        ;Shifts clock timer to RUN status

        EI                      ;Enables interrupts

        RET

;EXAMPLE PROGRAM FOR CLOCK TIMER INTERRUPT
TIINT:
        PUSH    YP
        PUSH    YH
        PUSH    YL
        PUSH    A
        PUSH    B

        LD      A,0
        LD      YP,A            ;Sets to page 0
        LD      Y,0FCH          ;Sets address to FCH
        LD      A,MY            ;Reads clock timer interrupt factor flags
        LD      Y,08DH          ;Sets address to 8DH
        LD      A,MY            ;Reads clock timer data
        LD      Y,08EH          ;Sets address to 8EH
        LD      B,MY            ;Reads clock timer data
;
;
;       Interrupt processing program
;
;
        POP     B
        POP     A
        POP     YL
        POP     YH
        POP     YP

        EI
        RET
```

3.7.3 Programming notes

(1) The prescaler must be set correctly to suit the crystal oscillator to be used for the OSC1 oscillation circuit.

(2) Be sure to data reading in the order of low-order data (TM0–TM3) then high-order data (TM4–TM7).

(3) When the clock timer has been reset, the interrupt factor flag (IT) may sometimes be set to "1". Consequently, perform flag reading (reset the flag) as necessary at reset.

(4) Reading of interrupt factor flags is available at EI, but be careful in the following cases.
If the interrupt mask register value corresponding to the interrupt factor flags to be read is set to "1", an interrupt request will be generated by the interrupt factor flags set timing, or an interrupt request will not be generated. Be very careful when interrupt factor flags are in the same address.

(5) Write the interrupt mask register (EIT) only in the DI status (interrupt flag = "0"). Writing during EI status (interrupt flag = "1") will cause malfunction.

3.8 Programmable Timer

3.8.1 I/O memory of the programmable timer

The control registers of the programmable timer are shown in Table 3.8.1.1.

Table 3.8.1.1 Control registers of programmable timer

Address *7	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
E8H	0	0	PTPS1	PTPS0	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R		R/W		PTPS1	0			Programmable timer clock dividing ratio selection
					PTPS0	0			
E9H	0	0	PTPC1	PTPC0	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R		R/W		PTPC1	0			PT prescaler clock source selection
					PTPC0	0			
EAH	PNRFS	PTOE	PTRUN	PTRST	PNRFS	0	1024 Hz	256 Hz	Noise rejector clock frequency selection
					PTOE	0	Enable	Disable	PTOVF output enable
	R/W			W	PTRUN	0	Run	Stop	Programmable timer Run/Stop
					PTRST *5	– *2	Rst (reload)	–	Programmable timer reset (reload)
EBH	RD3	RD2	RD1	RD0	RD3	0			MSB
					RD2	0			Programmable timer reload data
	R/W				RD1	0			(low-order 4 bits)
					RD0	0			LSB
ECH	RD7	RD6	RD5	RD4	RD7	0			MSB
					RD6	0			Programmable timer reload data
	R/W				RD5	0			(high-order 4 bits)
					RD4	0			LSB
EDH	PT3	PT2	PT1	PT0	PT3	0			MSB
					PT2	0			Programmable timer data
	R				PT1	0			(low-order 4 bits)
					PT0	0			LSB
EEH	PT7	PT6	PT5	PT4	PT7	0			MSB
					PT6	0			Programmable timer data
	R				PT5	0			(high-order 4 bits)
					PT4	0			LSB
BFH	SELP33	SELP32	SELP31	SELP30	SELP33	0	FOUT	I/O	P33 function selection register (FOUT output or I/O)
					SELP32	0	PTOVF	I/O	P32 function selection register (PTOVF output or I/O)
	R/W				SELP31	0	FR	I/O	P31 function selection register (FR output or I/O)
					SELP30	0	CL	I/O	P30 function selection register (CL output or I/O)
F0H	0	0	0	EIPT	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R			R/W	0 *5	– *2			Unused
					EIPT	0	Enable	Mask	Interrupt mask register (programmable timer)
F8H	0	0	0	IPT	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R				0 *5	– *2			Unused
					IPT *4	0	Yes	No	Interrupt factor flag (programmable timer)

PTPS [1][0] Dividing ratio: 1 1 1/256; 1 0 1/32; 0 1 1/4; 0 0 1/1

PTPC [1][0] CLK: 1 1 OSC3; 1 0 OSC1; 0 1 K02; 0 0 K02 (NR)

*1 Initial value at the time of initial reset
*2 Not set in the circuit
*3 Undefined
*4 Reset (0) immediately after being read
*5 Constantly "0" when being read
*6 Refer to main manual
*7 I/O memory is allocated from page 0 to 3

3.8.2 Example program for the programmable timer

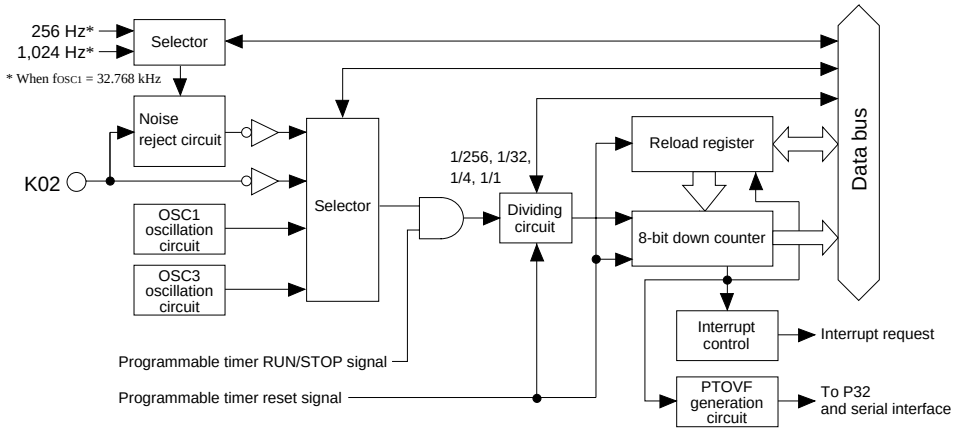


Fig. 3.8.2.1 Configuration of programmable timer

Following program shows the programmable timer interrupt controlling procedure.

```
Label     Mnemonic/operand          Comment
;
;PROGRAMMABLE TIMER
;

;EXAMPLE PROGRAM FOR INITIALIZATION OF PROGRAMMABLE TIMER
PTINIT:
        LD      A,00H
        LD      XP,A            ;Sets to page 0
;
        LD      X,0BFH          ;Sets address to BFH
        OR      MX,0100B        ;Sets P32 as PTOVF output port
;
        LD      X,0F0H          ;Sets address to F0H
        LD      MX,1H           ;Sets interrupt mask register
                                ;(programmable timer) to enable
;
        LD      X,0E8H          ;Sets address to E8H
        LDPX    MX,0011B        ;Sets programmable timer clock dividing
                                ;ratio to 1/256
        LDPX    MX,0010B        ;Sets clock source for programmable
                                ;timer prescaler to OSC1
        LD      MX,0EH          ;Shifts programmable timer to
                                ;RUN status

        EI
        RET

;EXAMPLE PROGRAM FOR PROGRAMMABLE TIMER INTERRUPT
PTINT:
        PUSH    YP
        PUSH    YH
        PUSH    YL
        PUSH    A

        LD      A,0
        LD      YP,A            ;Sets to page 0
        LD      Y,0F8H          ;Sets address to F8H
        LD      A,MY            ;Reads programmable timer
                                ;interrupt factor flag
;
;
```

```
;       Interrupt processing program
;
;
        POP     A
        POP     YL
        POP     YH
        POP     YP

        EI
        RET
```

See Section 4.10, "Programmable Timer", in the "Technical Hardware" for the clock source selection, operation and interrupt function.

3.8.3 Programming notes

(1) Be sure to data reading in the order of low-order data (PT0–PT3) then high-order data (PT4–PT7).

(2) When data of reload registers is set at "00H", the down-counter becomes a 256-value counter.

(3) Reading of interrupt factor flags is available at EI, but be careful in the following cases.
If the interrupt mask register value corresponding to the interrupt factor flags to be read is set to "1", an interrupt request will be generated by the interrupt factor flags set timing, or an interrupt request will not be generated.

(4) Write the interrupt mask register (EIPT) only in the DI status (interrupt flag = "0"). Writing during EI status (interrupt flag = "1") will cause malfunction.

3.9 Serial Interface

3.9.1 I/O memory of the serial interface

The control registers of the serial interface are shown in Table 3.9.1.1.

Table 3.9.1.1 Control registers of serial interface

Address *7	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
C8H	0	SMD1	SMD0	ESIF	0 *5	– *2			Unused
					SMD1	0			Serial I/F mode selection (SMD[1][0]: 1 1 Asynchronous 8-bit; 1 0 Asynchronous 7-bit; 0 1 Clock synchronous slave; 0 0 Clock synchronous master)
	R	R/W			SMD0	0			
					ESIF	0	SI/F	I/O	Serial I/F enable (P4 port function selection)
C9H	EPR	PMD	SCS1	SCS0	EPR	0	WithParity	NonParity	Parity enable (only for asynchronous mode)
					PMD	0	Odd	Even	Parity mode selection
	R/W				SCS1	0			Clock source selection (SCS[1][0]: 1 1 PT × 1/2; 1 0 CPU clock × 1/4; 0 1 CPU clock × 1/8; 0 0 CPU clock × 1/16)
					SCS0	0			
CAH	RXTRG	RXEN	TXTRG	TXEN	RXTRG(R)	0	Run	Stop	Receive status (when reading)
					RXTRG(W)		Trigger	–	Receive trigger (when writing)
					RXEN	0	Enable	Disable	Receive enable
	R/W				TXTRG(R)	0	Run	Stop	Transmit status (when reading)
					TXTRG(W)		Trigger	–	Transmit trigger (when writing)
					TXEN	0	Enable	Disable	Transmit enable
CBH	0	FER	PER	OER	0 *5	– *2			Unused
					FER(R)	0	Error	NoError	Framing error flag (when reading)
					FER(W)		Reset	–	flag reset (when writing)
	R	R/W			PER(R)	0	Error	NoError	Parity error flag (when reading)
					PER(W)		Reset	–	flag reset (when writing)
					OER(R)	0	Error	NoError	Overrun error flag (when reading)
					OER(W)		Reset	–	flag reset (when writing)
CCH	TRXD3	TRXD2	TRXD1	TRXD0	TRXD3	– *2	High	Low	Transmit/Receive data (low-order 4 bits)
					TRXD2	– *2	High	Low	
	R/W				TRXD1	– *2	High	Low	
					TRXD0	– *2	High	Low	LSB
CDH	TRXD7	TRXD6	TRXD5	TRXD4	TRXD7	– *2	High	Low	MSB
					TRXD6	– *2	High	Low	Transmit/Receive data (high-order 4 bits)
	R/W				TRXD5	– *2	High	Low	
					TRXD4	– *2	High	Low	
C1H	PUL43	PUL42	PUL41	PUL40	PUL43	1	On	Off	P43 pull up control register (General-purpose register when SI/F (sync. slave) is selected)
					PUL42	1	On	Off	P42 pull up control register (General-purpose register when SI/F (sync. master) is selected)
	R/W				PUL41	1	On	Off	P41 pull up control register (ESIF = 0) (General-purpose register when SI/F is selected)
					PUL40	1	On	Off	P40 pull up control register (ESIF = 0) SIN pull up control register (ESIF = 1)
F1H	0	EISIFE	EISIFT	EISIFR	0 *5	– *2			Unused
					EISIFE	0	Enable	Mask	Interrupt mask register (serial I/F error)
	R	R/W			EISIFT	0	Enable	Mask	Interrupt mask register (serial I/F transmitting)
					EISIFR	0	Enable	Mask	Interrupt mask register (serial I/F receiving)
F9H	0	ISIFE	ISIFT	ISIFR	0 *5	– *2			Unused
					ISIFE*4	0	Yes	No	Interrupt factor flag (serial I/F error)
	R				ISIFT*4	0	Yes	No	Interrupt factor flag (serial I/F transmitting)
					ISIFR*4	0	Yes	No	Interrupt factor flag (serial I/F receiving)

*1 Initial value at the time of initial reset
*2 Not set in the circuit
*3 Undefined
*4 Reset (0) immediately after being read
*5 Constantly "0" when being read
*6 Refer to main manual
*7 I/O memory is allocated from page 0 to 3

3.9.2 Example program for the serial interface

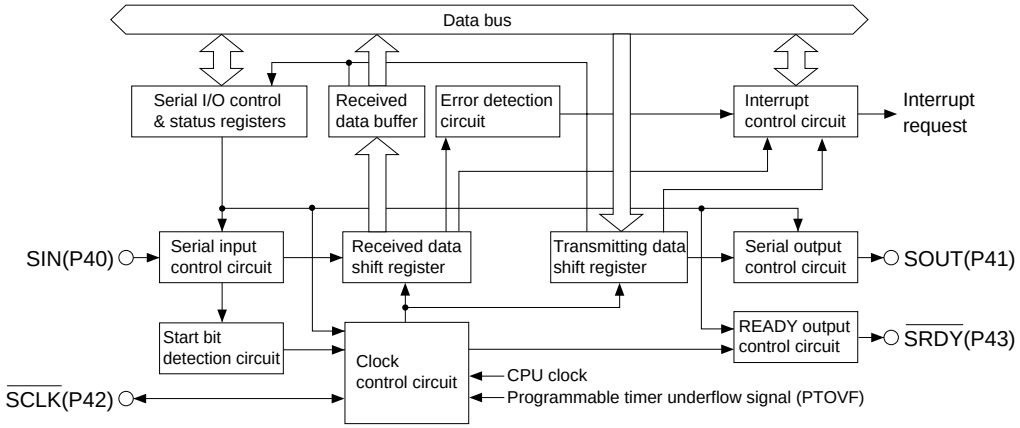
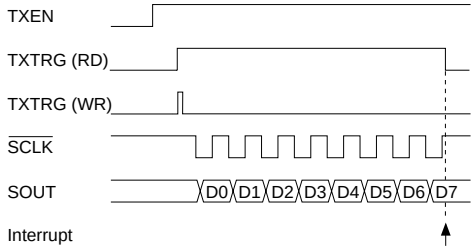
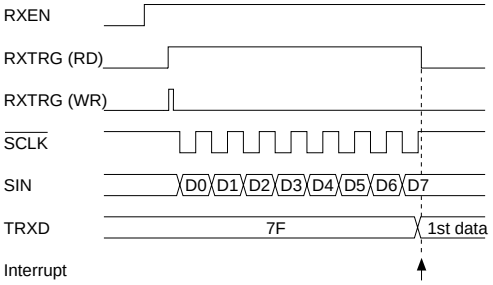


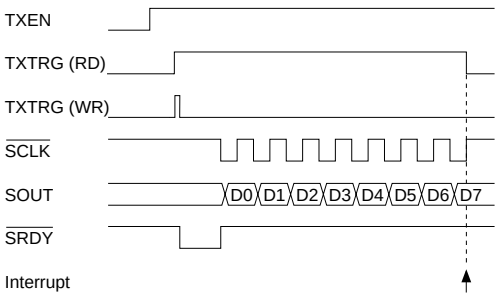
Fig. 3.9.2.1 Configuration of serial interface



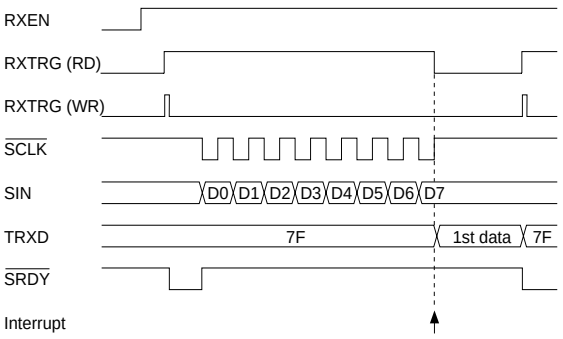
(a) Transmit timing for master mode



(c) Receive timing for master mode

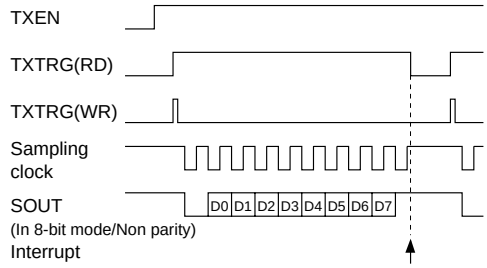


(b) Transmit timing for slave mode

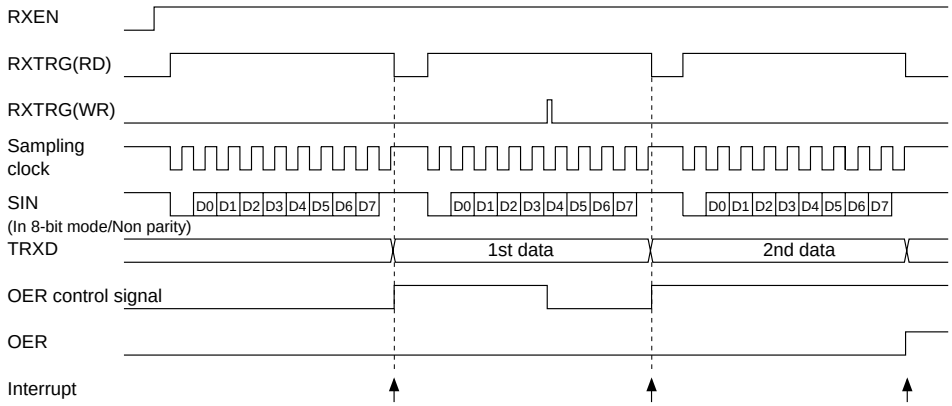


(d) Receive timing for slave mode

Fig. 3.9.2.2 Timing chart (clock synchronous transfer)



(a) Transmit timing



(b) Receive timing

Fig. 3.9.2.3 Timing chart (asynchronous transfer)

Following program shows the serial interface controlling procedure.

```
Label       Mnemonic/operand            Comment
;
;SERIAL INTERFACE
;

;EXAMPLE PROGRAM FOR INITIALIZATION OF SERIAL INTERFACE
;       When transmitting in clock synchronous master mode
;       Sets K00 as /READY
SIFINIT:
        LD      A,00H
        LD      XP,A            ;Sets to page 0
;
        LD      X,0CAH          ;Sets address CAH
        LDPX    MX,0000B        ;Disables transmitting/receiving
        LD      X,0F1H          ;Sets address to F1H
        LD      MX,0110B        ;Sets interrupt mask register to enable
        LD      X,0C8H          ;Sets address to C8H
        LDPX    MX,0001B        ;Sets SIF to clock synchronous master mode
        LDPX    MX,0010B        ;Sets clock to CPU clock x 1/4
        LDPX    MX,0001B        ;Enables transmitting
        LD      X,0CCH          ;Sets address to CCH
        LDPX    MX,1010B        ;Sets data 1010B to TRXD3-0
        LD      MX,0011B        ;Sets 0011B to TRXD7-4
RDY_CHK:
        LD      X,91H           ;Sets address to CAH
        LD      B,MX            ;Loads K00-K03 data to B register
        FAN     B,0001B         ;Checks K00 data
        JP      NZ,RDY_CHK      ;Loops if it is HIGH
        LD      X,0CAH          ;Sets address to CAH
        OR      MX,0010B        ;Sets to TXTRG = 1
        EI                      ;Enables interrupts
        RET
```

```
;EXAMPLE PROGRAM FOR INITIALIZATION OF SERIAL INTERFACE
;       When receiving in clock synchronous slave mode
SIFINIT2:
        LD      A,00H
        LD      XP,A            ;Sets to page 0
;
        LD      X,0CAH          ;Sets address to CAH
        LDPX    MX,0000B        ;Disables transmitting/receiving
        LD      X,0F1H          ;Sets address to F1H
        LD      MX,0101B        ;Sets interrupt mask register to enable
        LD      X,0C8H          ;Sets address to C8H
        LDPX    MX,0011B        ;Sets SIF to clock synchronous slave mode
        LDPX    MX,0001B        ;Sets clock to CPU clock x 1/8
        LD      MX,0100B        ;Enables receiving
        OR      MX,1000B        ;Sets to RXTRG = 1
        EI                      ;Enables interrupts
        RET

;EXAMPLE PROGRAM FOR INITIALIZATION OF SERIAL INTERFACE
;       Asynchronous mode
SIFINIT3:
        LD      A,00H
        LD      XP,A            ;Sets to page 0
;
        LD      X,0CAH          ;Sets address to CAH
        LDPX    MX,0000B        ;Disables transmitting/receiving
        LD      MX,0000B        ;Resets error flags

        LD      X,0F1H          ;Sets address to F1H
        LD      MX,0101B        ;Sets interrupt mask register to enable
        LD      X,0C8H          ;Sets address to C8H
        LDPX    MX,0111B        ;Sets SIF to Asynchronous 8-bit mode
        LDPX    MX,1101B        ;Sets to "with parity (odd)",
                                ;and clock to CPU clock x 1/8
        LD      MX,0100B        ;Enables receiving
        OR      MX,1000B        ;Sets to RXTRG = 1
        EI                      ;Enables interrupts
        RET
```

3.9.3 Programming notes

(1) Be sure to initialize the serial interface mode in the transmitting/receiving disable status (TXEN = RXEN = "0").

(2) Do not perform double trigger (writing "1") to TXTRG (RXTRG) when the serial interface is in the transmitting (receiving) operation.

(3) In the clock synchronous mode, since one clock line ($\overline{SCLK}$) is shared for both transmitting and receiving, transmitting and receiving cannot be performed simultaneously.
Consequently, be sure not to write "1" to RXTRG (TXTRG) when TXTRG (RXTRG) is "1".

(4) When a parity error or flaming error is generated during receiving in the asynchronous mode, the receiving error interrupt factor flag ISIFE is set to "1" prior to the receiving complete interrupt factor flag ISIFR for the time indicated in Table 3.9.3.1. Consequently, you should reset the receiving complete interrupt factor flag ISIFR to "0" by providing a wait time in error processing routines and similar routines.
When an overrun error is generated, the receiving complete interrupt factor flag ISIFR is not set to "1" and a receiving complete interrupt is not generated.

Table 3.9.3.1 Time difference between ISIFE and ISIFR on error generation

Clock source	Time difference
CPU clock / n	1/2 cycles of CPU clock / n
Programmable timer × 1/2	1 cycle of programmable timer underflow

(5) When the demultiplied signal of the OSC3 oscillation circuit is made the clock source, it is necessary to turn the OSC3 oscillation ON, prior to using the serial interface.
A time interval of 5 msec, from the turning ON of the OSC3 oscillation circuit to until the oscillation stabilizes, is necessary, due to the oscillation element that is used. Consequently, you should allow an adequate waiting time after turning ON of the OSC3 oscillation, before starting transmitting/receiving of serial interface. (The oscillation start time will vary somewhat depending on the oscillator and on the externally attached parts. Refer to the oscillation start time example indicated in Chapter 7, "ELECTRICAL CHARACTERISTICS", in the "Technical Hardware".)
At initial reset, the OSC3 oscillation circuit is set to OFF status.

(6) Write the interrupt mask register only in the DI status (interrupt flag = "0"). Writing during EI status (interrupt flag = "1") will cause malfunction.

(7) Reading of interrupt factor flags is available at EI, but be careful in the following cases.
If the interrupt mask register value corresponding to the interrupt factor flags to be read is set to "1", an interrupt request will be generated by the interrupt factor flags set timing, or an interrupt request will not be generated. Be very careful when interrupt factor flags are in the same address.

3.10 Sound Generator

3.10.1 I/O memory of the sound generator

The control registers of the sound generator are shown in Table 3.10.1.1.

Table 3.10.1.1 Control registers of sound generator

Address *7	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
E0H	ENRTM	ENRST	ENON	BZE	ENRTM	0	1 sec	0.5 sec	Envelope attenuation time selection
					ENRST *5	– *2	Reset	–	Envelope reset
	R/W	W	R/W		ENON	0	On	Off	Envelope On/Off
					BZE	0	Enable	Disable	BZ output enable
E1H	0	BZSTP	BZSHT	SHTPW	0 *5	– *2			Unused
					BZSTP *5	– *2	Stop	–	One-shot buzzer stop
					BZSHT(W)	– *2	Trigger	–	One-shot buzzer trigger (when writing)
	R	W	R/W		BZSHT(R)	0	Busy	Ready	One-shot buzzer status (when reading)
					SHTPW	0	125 msec	31.25 msec	One-shot buzzer pulse width selection (160/40 msec is in case of fOSC1 = 50 kHz)
E2H	0	BZFQ2	BZFQ1	BZFQ0	0 *5	– *2			Unused
					BZFQ2	0			Buzzer frequency selection
					BZFQ1	0			
	R	R/W			BZFQ0	0			
E3H	0	BDTY2	BDTY1	BDTY0	0 *5	– *2			Unused
					BDTY2	0			Buzzer signal duty ratio selection *6
	R	R/W			BDTY1	0			
					BDTY0	0			
A8H	R43HIZ	R42HIZ	R41HIZ	R40HIZ	R43HIZ	0	High-Z	Output	R43 output high-impedance control
					R42HIZ	0	High-Z	Output	R42 output high-impedance control
					R41HIZ	0	High-Z	Output	R41 output high-impedance control (EXTMF = 0) (General-purpose register when EXTMF = 1)
	R/W				R40HIZ	0	High-Z	Output	R40 output high-impedance control (EXTMF = 0) (General-purpose register when EXTMF = 1)
AAH	SELR43	SELR42	0	0	SELR43	0	BZ	Normal	R43 function selection register (BZ or general-purpose output)
					SELR42	0	$\overline{BZ}$	Normal	R42 function selection register ($\overline{BZ}$ or general-purpose output)
	R/W		R		0 *5	– *2			Unused
					0 *5	– *2			Unused

Buzzer frequency selection:

BZFQ [2][1][0]	Buzzer frequency	fOSC1 = 32 kHz (Hz)
1 1 1	fOSC1/28	1170.3
1 1 0	fOSC1/24	1365.3
1 0 1	fOSC1/20	1638.4
1 0 0	fOSC1/16	2048.0
0 1 1	fOSC1/14	2340.6
0 1 0	fOSC1/12	2730.7
0 0 1	fOSC1/10	3276.8
0 0 0	fOSC1/8	4096.0

*1 Initial value at the time of initial reset
*2 Not set in the circuit
*3 Undefined
*4 Reset (0) immediately after being read
*5 Constantly "0" when being read
*6 Refer to main manual
*7 I/O memory is allocated from page 0 to 3

Table 3.10.1.2 Setting of buzzer signal frequency

BZFQ2	BZFQ1	BZFQ0	Dividing ratio	Buzzer frequency (Hz) fOSC1 = 32.768 kHz	fOSC1 = 38.4 kHz	fOSC1 = 50.0 kHz	fOSC1 = 76.8 kHz
0	0	0	fOSC1 /8	4096.0	4800.0	6250.0	9600.0
0	0	1	fOSC1 /10	3276.8	3840.0	5000.0	7680.0
0	1	0	fOSC1 /12	2730.7	3200.0	4166.7	6400.0
0	1	1	fOSC1 /14	2340.6	2742.9	3571.4	5485.7
1	0	0	fOSC1 /16	2048.0	2400.0	3125.0	4800.0
1	0	1	fOSC1 /20	1638.4	1920.0	2500.0	3840.0
1	1	0	fOSC1 /24	1365.3	1600.0	2083.3	3200.0
1	1	1	fOSC1 /28	1170.3	1371.4	1785.7	2742.9

3.10.2 Example program for the sound generator

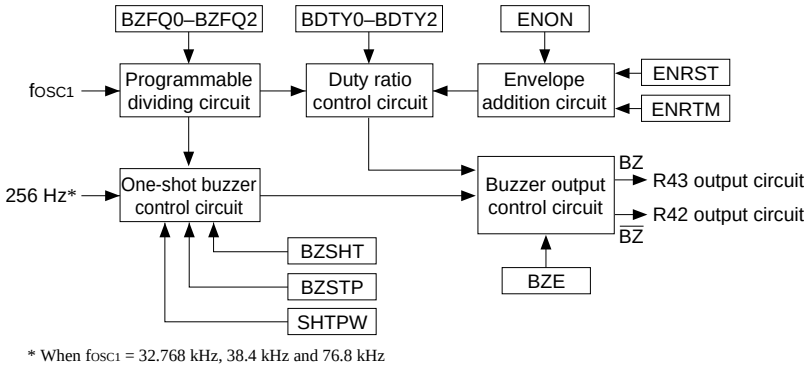


Fig. 3.10.2.1 Configuration of sound generator

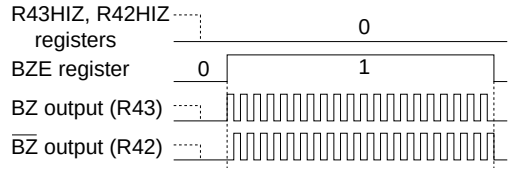


Fig. 3.10.2.2 Timing chart for buzzer signal output

Table 3.10.2.1 Duty ratio selection

Level	BDTY2	BDTY1	BDTY0	Duty ratio by buzzer frequency			
				fosc1 /8 fosc1 /16	fosc1 /10 fosc1 /20	fosc1 /12 fosc1 /24	fosc1 /14 fosc1 /28
Level 1 (maximum)	0	0	0	8/16	8/20	12/24	12/28
Level 2	0	0	1	7/16	7/20	11/24	11/28
Level 3	0	1	0	6/16	6/20	10/24	10/28
Level 4	0	1	1	5/16	5/20	9/24	9/28
Level 5	1	0	0	4/16	4/20	8/24	8/28
Level 6	1	0	1	3/16	3/20	7/24	7/28
Level 7	1	1	0	2/16	2/20	6/24	6/28
Level 8 (minimum)	1	1	1	1/16	1/20	5/24	5/28

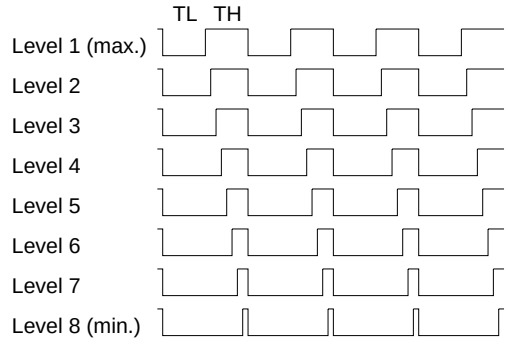


Fig. 3.10.2.3 Duty ratio of buzzer signal waveform

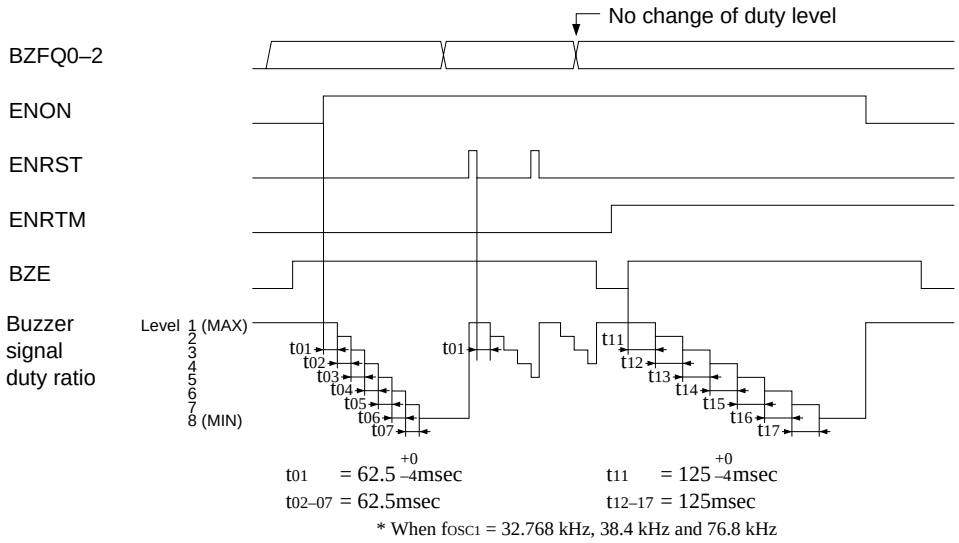


Fig. 3.10.2.4 Timing chart for digital envelope

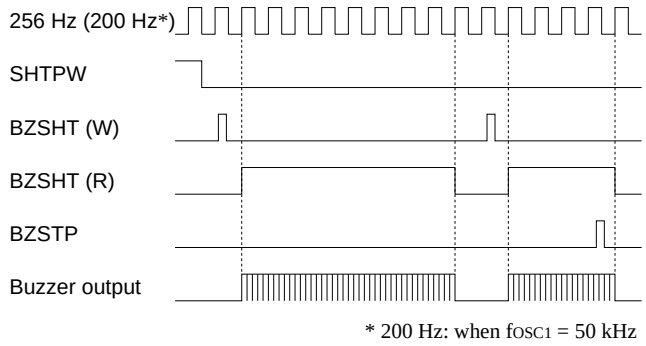


Fig. 3.10.2.5 Timing chart for one-shot output

Following program shows the sound generator controlling procedure.

```
Label     Mnemonic/operand          Comment
;
;SOUND GENERATOR
;

;EXAMPLE PROGRAM FOR SOUND GENERATOR
;       One-shot buzzer setting
SNDINIT:
        LD      A,00H
        LD      XP,A            ;Sets to page 0
        LD      X,0A8H          ;Sets address to A8H
        AND     MX,0011B        ;Sets R43 and R42 to output
        LD      X,0AAH          ;Sets address to AAH
        LD      MX,1100B        ;Sets R43 as BZ output
                                ;and R42 as /BZ output
        LD      X,0E1H          ;Sets address to E1H
        LD      MX,0011B        ;One-shot buzzer setting
        LD      X,0E3H          ;Sets address to E3H
        LD      MX,0100B        ;Sets buzzer signal duty ratio
        LD      X,0E0H          ;Sets address to E0H
        OR      MX,0001B        ;Enables BZ output
        RET

;BUZZER ENVELOPE SETTING
SNDINIT2:
        LD      A,00H
        LD      XP,A            ;Sets to page 0
        LD      X,0A8H          ;Sets address to A8H
        AND     MX,0011B        ;Sets R43 and R42 to output
        LD      X,0AAH          ;Sets address to AAH
        LD      MX,1100B        ;Sets R43 as BZ output
                                ;and R42 as /BZ output
        LD      X,0E0H          ;Sets address to E0H
        LD      MX,1111B        ;Turns envelope ON
        RET
```

3.10.3 Programming note

A hazard may occur when data of the BZE register or the buzzer frequency selection registers (BZFQ0–BZFQ2) are changed.

3.11 External Memory Access

3.11.1 I/O memory of the external memory access control

The control registers of the external memory access are shown in Table 3.11.1.1.

Table 3.11.1.1 Control registers of external memory access function

Address *7	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
98H	EXTMF	0	MEMS1	MEMS0	EXTMF	0	On	Off	External memory access function control
					0 *5	– *2			Unused
					MEMS1	0			External memory size selection: MEMS [1][0] 1 1 1M (R only) (A00–A16); 1 0 512K (R/W) (A00–A15); 0 1 256K (R/W) (A00–A14); 0 0 64K (R/W) (A00–A12)
	R/W	R	R/W		MEMS0	0			
99H	HZCS	HZBUS	ADINC	PICON	HZCS	0	High-Z	Output	$\overline{CS0}$–$\overline{CS3}$ output high-impedance control
					HZBUS	0	High-Z	Output	Address bus, $\overline{RD}$/$\overline{WR}$ high-impedance control
	R/W		W	R/W	ADINC	0	Increment	–	External memory address increment
					PICON	0	Auto inc.	Normal	External memory address auto increment mode
9AH	A03	A02	A01	A00	A03	– *2	1	0	External memory address A00–A03 (EXTMF = 1) Functions as a general-purpose register when EXTMF = 0.
					A02	– *2	1	0	
	R/W				A01	– *2	1	0	
					A00	– *2	1	0	
9BH	A07	A06	A05	A04	A07	– *2	1	0	External memory address A04–A07 (EXTMF = 1) Functions as a general-purpose register when EXTMF = 0.
					A06	– *2	1	0	
	R/W				A05	– *2	1	0	
					A04	– *2	1	0	
9CH	A11	A10	A09	A08	A11	– *2	1	0	External memory address A08–A11 (EXTMF = 1) Functions as a general-purpose register when EXTMF = 0.
					A10	– *2	1	0	
	R/W				A09	– *2	1	0	
					A08	– *2	1	0	
9DH	A15	A14	A13	A12	A15	– *2	1	0	External memory address A12–A15 (EXTMF = 1) Bits that are not used as an address for external memory access can also be used as a general-purpose register.
					A14	– *2	1	0	
	R/W				A13	– *2	1	0	
					A12	– *2	1	0	
9EH	0	0	0	A16	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R			R/W	0 *5	– *2			Unused
					A16	– *2	1	0	External memory address A16 *8
B2H	P03	P02	P01	P00	P03	– *2	High	Low	P00–P03 I/O port data (EXTMF = 0)
					P02	– *2	High	Low	
	D03	D02	D01	D00	P01	– *2	High	Low	
					P00	– *2	High	Low	
	R/W				D03	– *2	1	0	External memory data D00–D03 (EXTMF = 1)
					D02	– *2	1	0	
					D01	– *2	1	0	
					D00	– *2	1	0	
B6H	P13	P12	P11	P10	P13	– *2	High	Low	P10–P13 I/O port data (EXTMF = 0)
					P12	– *2	High	Low	
	D07	D06	D05	D04	P11	– *2	High	Low	
					P10	– *2	High	Low	
	R/W				D07	– *2	1	0	External memory data D04–D07 (EXTMF = 1)
					D06	– *2	1	0	
					D05	– *2	1	0	
					D04	– *2	1	0	
BAH	P23	P22	P21	P20	P23	– *2	High	Low	P20–P23 I/O port data (EXTMF = 0)
					P22	– *2	High	Low	
	CS3	CS2	CS1	CS0	P21	– *2	High	Low	
					P20	– *2	High	Low	
	R/W				CS3	– *2	Disable	Active	Chip select $\overline{CS0}$–$\overline{CS3}$ active standby (EXTMF = 1)
					CS2	– *2	Disable	Active	
					CS1	– *2	Disable	Active	
					CS0	– *2	Disable	Active	

*1 Initial value at the time of initial reset
*2 Not set in the circuit
*3 Undefined
*4 Reset (0) immediately after being read
*5 Constantly "0" when being read
*6 Refer to main manual
*7 I/O memory is allocated from page 0 to 3
*8 When other than EXTMF = 1 and a memory less than 1M bits are used, it functions as a general purpose register.

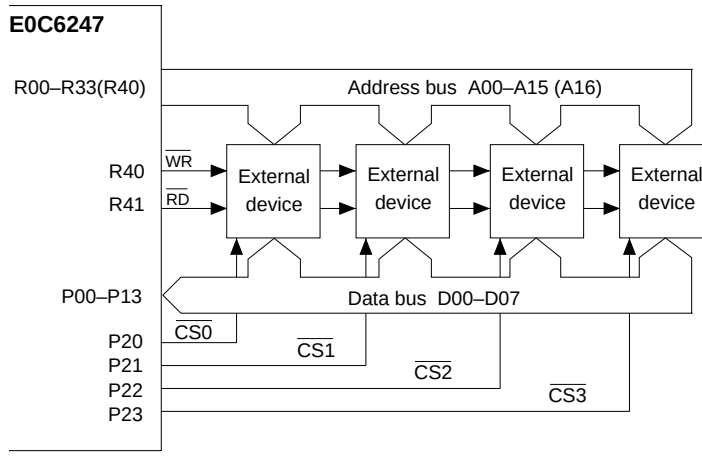


Fig. 3.11.1.1 External bus block diagram

Table 3.11.1.2 Setting of memory size and address bus

MEMS1	MEMS0	Memory size	Address bus
1	1	1M-bit (R only)	A00–A16
1	0	512K-bit (R/W)	A00–A15
0	1	256K-bit (R/W)	A00–A14
0	0	64K-bit (R/W)	A00–A12

Table 3.11.1.3 Configuration of output terminal depending on memory size

Terminal name	Function of terminals			
	1M-bit	512K-bit	256K-bit	64K-bit
R00–R03	A00–A03	A00–A03	A00–A03	A00–A03
R10–R13	A04–A07	A04–A07	A04–A07	A04–A07
R20–R23	A08–A11	A08–A11	A08–A11	A08–A11
R30	A12	A12	A12	A12
R31	A13	A13	A13	R31
R32	A14	A14	A14	R32
R33	A15	A15	R33	R33
R40	A16	$\overline{WR}$	$\overline{WR}$	$\overline{WR}$
R41	$\overline{RD}$	$\overline{RD}$	$\overline{RD}$	$\overline{RD}$

Output port terminals that are not used as address outputs depending on the selected memory size are not changed.
The data registers and high impedance control registers of the output port set for the address bus can be used as general purpose registers that do not affect output.
At initial reset, all the terminals above are set to the output port terminals, and they output a high level.

Table 3.11.1.4 Relation of I/O port and data bus

I/O port	Data bus
P00–P03	D00–A03
P10–P13	D04–D07

Data is written or read in the order of low-order bits D00 to D03 (P00 to P03) then high-order bits D04 to D07 (P10 to P13). Through writing/reading operations to these registers, the chip select signal ($\overline{CS0}$–$\overline{CS3}$), write signal ($\overline{WR}$) and read signal ($\overline{RD}$) to the external memory are automatically output.

Consecutive access of data and virtual data register

Output or input of external memory data to the external data bus is done by accessing registers P00–P03 and P10–P13. It requires access of low-order data and high-order data, and is related to the increase of program steps.
Hence, the E0C6247 allows even and odd number addresses in the RAM addresses (900H–9FFH) to be logically allocated to P00–P03 and P10–P13, respectively, as virtual data; E0C6247 also makes consecutive access by LBPX and RETD instructions possible.
The memory map of this logical space is shown on Figure 3.11.1.2.

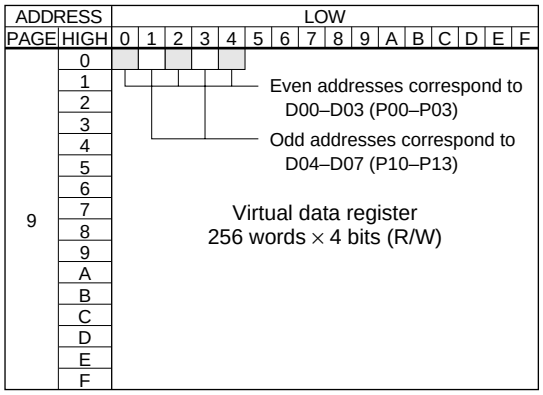


Fig. 3.11.1.2 Memory map (virtual data registers)

Note: The virtual data register is a logical space and no memory is physically allocated. The actual writing/reading through access of this space is done for registers P00–P03 and P10–P13.

Chip select signals ($\overline{CS0}$–$\overline{CS3}$)

The E0C6247 can output maximum four chip select signals ($\overline{CS0}$–$\overline{CS3}$). Therefore, there is no need to connect an address decoder externally.
The chip select signals are assigned to the I/O ports shown in Table 3.11.1.5 when the external memory access function is selected (EXTMF = "1").

Table 3.11.1.5 Relation of I/O port and chip select signal

I/O port	Chip select signal
P20	$\overline{CS0}$
P21	$\overline{CS1}$
P22	$\overline{CS2}$
P23	$\overline{CS3}$

The data registers of the I/O port (P20–P23) that are set to the chip select signal output are used to select the chip select signal to be output. The I/O control registers and the pull up control registers can be used as general purpose registers that do not affect output.
The assignment of chip select signals take four bits all together, it cannot be selected with one bit. The data register of the I/O port that is assigned to an unused chip select signal can be used as a general purpose register.
At initial reset, all the terminals above are set to the I/O port terminals, and the input mode (terminals are pulled up) is set.

By writing "0" to the chip select register CSx (P2x), the $\overline{CSx}$ signal goes into active standby status ($\overline{CSx}$ output enable status); writing "1" will make it output disabled. It does not mean that writing of this register directly changes a $\overline{CSx}$ signal.
Set only one $\overline{CSx}$ signal corresponding to the device to be accessed to active standby. Writing "0" to two or more CSx registers causes a bus conflict.

By writing "0" to the chip select register CSx (P2x) to correspond with the device to be accessed and then performing data reading/writing, the $\overline{CSx}$ terminal that is set to active standby will be automatically set to low level, in the same manner as $\overline{RD}$ and $\overline{WR}$ signals. Moreover, after the access, it automatically returns to high level.

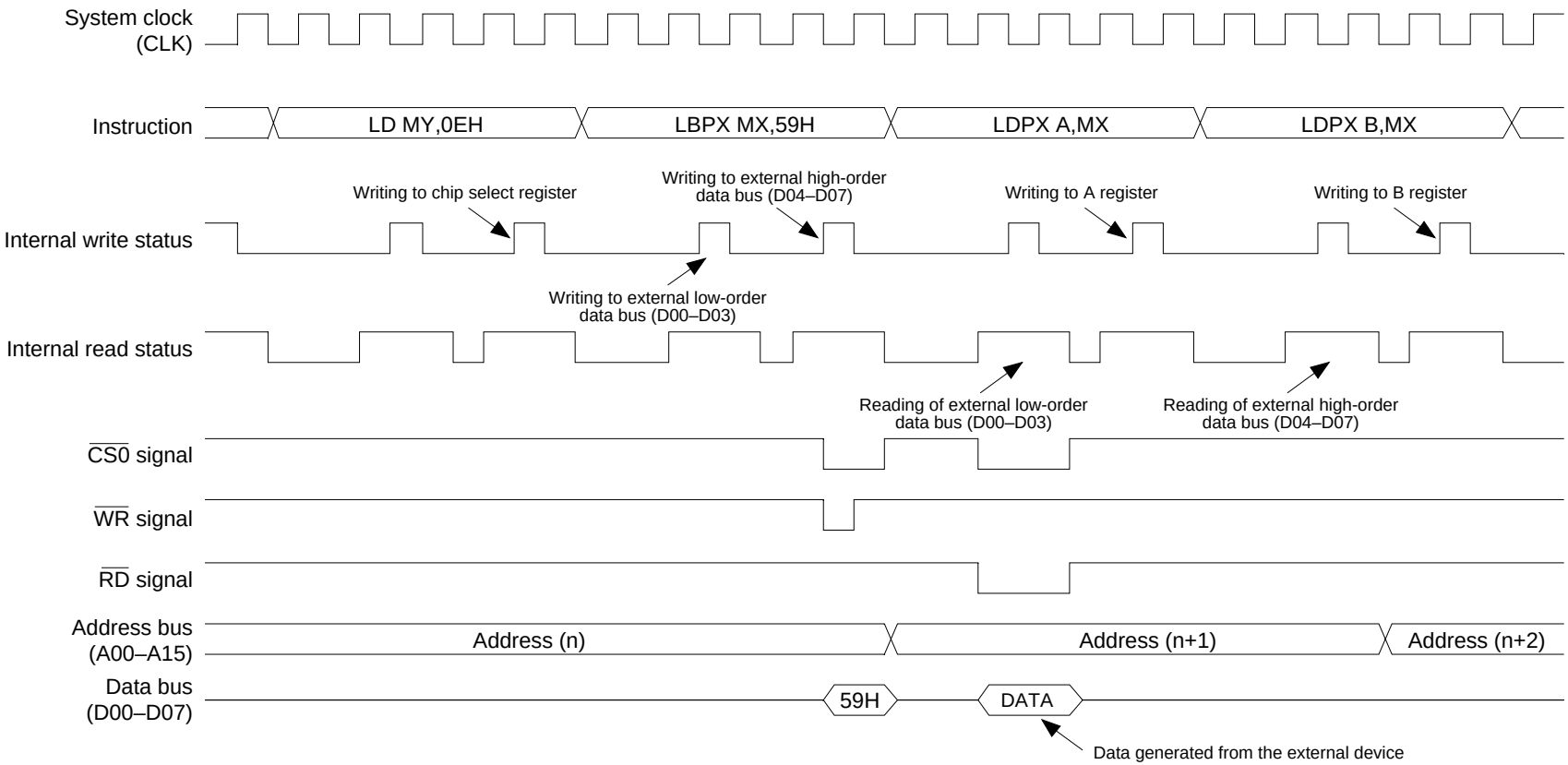


Fig. 3.11.1.3 Timing chart of external memory access

High impedance control for external bus

High impedance control can be done for the external bus signal lines using the HZBUS register and the HZCS registers.
When "1" is written to the HZBUS register, the address bus and $\overline{RD}$/$\overline{WR}$ signal output terminals shift into high impedance status. When reading/writing of the external data bus is done in high impedance status, the address and $\overline{RD}$/$\overline{WR}$ signals are not output.
When "0" is written to the HZBUS register, the external data set in the address register is output on the address bus, and the $\overline{RD}$/$\overline{WR}$ signal output terminals go to high level. The $\overline{RD}$/$\overline{WR}$ signal becomes active (low level) during reading/writing.

When "1" is written to the HZCS register, the chip select signal ($\overline{CS0}$–$\overline{CS3}$) output terminals shift into high impedance status. However, the built-in pull up resistors go ON to avoid malfunction of external devices.
When "0" is written to the HZCS register, the chip select signal ($\overline{CS0}$–$\overline{CS3}$) output terminals go to high level. The specified chip select signal becomes active (low level) during external memory accessing.

The data bus lines shift to high impedance status except during reading/writing of external device data. There is no need to control using the software.

For high impedance control, follow the requirements of the external circuit.
Figure 3.11.1.3 shows the timing chart of external memory access.

3.11.2 Example program for the external memory access

Following program shows the external memory access controlling procedure.

```
Label     Mnemonic/operand          Comment
;
;EXTERNAL MEMORY ACCESS
;

;EXAMPLE PROGRAM FOR INITIALIZATION OF
;EXTERNAL MEMORY ACCESS FUNCTION
EXMINIT:
        LD      A,00H
        LD      XP,A            ;Sets to page 0
;
        LD      X,98H           ;Sets address 98H
        LDPX    MX,1010B        ;Turns external memory access
                                ;function ON, 512K(R/W)
        LDPX    MX,1100B        ;Sets /CS0-/CS3 and A00-A15 to High-Z
        LDPX    MX,0000B        ;Sets A00-A03 to 0000B
        LDPX    MX,0000B        ;Sets A04-A07 to 0000B
        LDPX    MX,0000B        ;Sets A08-A11 to 0000B
        LD      MX,0000B        ;Sets A11-A15 to 0000B
        LD      X,0BAH          ;Sets address to BAH
        LD      MX,1110B        ;Sets /CS0 to active standby
        LD      X,99H           ;Sets address to 99H
        LD      MX,0001B        ;Outputs /CS0-/CS3 and  A00-A15
        RET

;EXAMPLE FOR EXTERNAL MEMORY DATA READING
DATA_RD:
        LD      A,9
        LD      YP,A            ;Sets to page 9
        LD      Y,0
        LDPY    A,MY            ;Reads P00-P03(D00-D03) to A register
        LDPY    B,MY            ;Reads P10-P13(D04-D07) to B register
;
;       Read data processing program
;
        RET

;EXAMPLE FOR EXTERNAL MEMORY DATA WRITING
```

```
DATA_WR:
        LD      A,9
        LD      YP,A            ;Sets to page 9
        LD      Y,0
;
;       Sets writing data to A and B registers
;       D00-D03 ---> A, D04-D07 ---> B
;
        LDPY    MY,A            ;Writes data
        LDPY    MY,B
        RET
```

3.11.3 Programming note

Be sure to data writing/reading for external memory in the order of low-order bits (D00–D03) then high-order bits (D04–D07).

3.12 SVD (Supply Voltage Detection) Circuit

3.12.1 I/O memory of the SVD circuit

The control registers of the SVD circuit are shown in Table 3.12.1.1.

Table 3.12.1.1 Control registers of sound generator

Address *7	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
80H	SVDS3	SVDS2	SVDS1	SVDS0	SVDS3	0			SVD criteria voltage setting (see below)
					SVDS2	0			
	R/W				SVDS1	0			
					SVDS0	0			
81H	0	0	SVDDT	SVDON	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R			R/W	SVDDT	0	Low	Normal	SVD evaluation data
					SVDON	0	On	Off	SVD circuit On/Off

SVD criteria voltage setting

SVDS [3][2][1][0]	Voltage (V)	SVDS [3][2][1][0]	Voltage (V)
0 1 1 1	1.60	1 1 1 1	2.60
0 1 1 0	1.40	1 1 1 0	2.50
0 1 0 1	1.30	1 1 0 1	2.30
0 1 0 0	1.25	1 1 0 0	2.20
0 0 1 1	1.20	1 0 1 1	2.10
0 0 1 0	1.15	1 0 1 0	2.05
0 0 0 1	1.10	1 0 0 1	2.00
0 0 0 0	1.05	1 0 0 0	1.95

*1 Initial value at the time of initial reset
*2 Not set in the circuit
*3 Undefined
*4 Reset (0) immediately after being read
*5 Constantly "0" when being read
*6 Refer to main manual
*7 I/O memory is allocated from page 0 to 3

The criteria voltage can be set for the 16 types shown in Table 3.12.1.2 by SVDS3–SCDS0.

Table 3.12.1.2 Criteria voltage setting

SVDS3	SVDS2	SVDS1	SVDS0	Criteria voltage	SVDS3	SVDS2	SVDS1	SVDS0	Criteria voltage
0	1	1	1	1.60 V	1	1	1	1	2.60 V
0	1	1	0	1.40 V	1	1	1	0	2.50 V
0	1	0	1	1.30 V	1	1	0	1	2.30 V
0	1	0	0	1.25 V	1	1	0	0	2.20 V
0	0	1	1	1.20 V	1	0	1	1	2.10 V
0	0	1	0	1.15 V	1	0	1	0	2.05 V
0	0	0	1	1.10 V	1	0	0	1	2.00 V
0	0	0	0	1.05 V	1	0	0	0	1.95 V

3.12.2 Example program for the SVD circuit

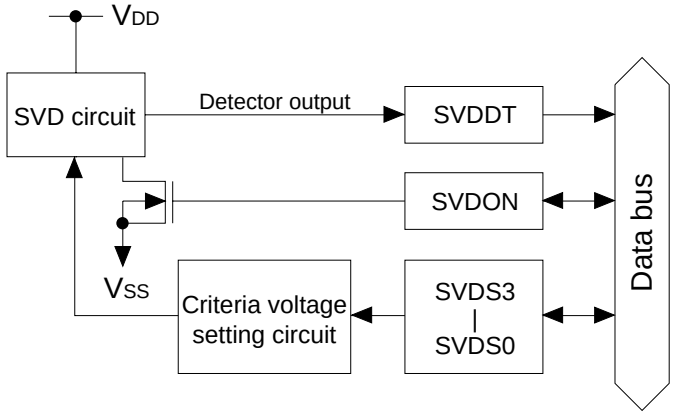


Fig. 3.12.2.1 Configuration of SVD circuit

Following program shows the SVD circuit controlling procedure.

```
Label     Mnemonic/operand          Comment
;
;SVD CIRCUIT
;

;EXAMPLE PROGRAM FOR SUPPLY VOLTAGE DETECTION
SVDCHK:
        LD      A,00H
        LD      XP,A            ;Sets to page 0
;
        LD      X,80H           ;Sets address to 80H
        LD      MX,0110B        ;Example: Sets criteria voltage to 1.40[V]
        LD      X,81H           ;Sets address to 81H
        LD      MX,0001B        ;Turns SVD circuit ON
        CALL    W100US          ;Waits for 100[µs]
;
        LD      X,81H           ;Sets address to 81H
        AND     MX,0010B        ;Turns SVD circuit OFF
        FAN     MX,0010B        ;Checks SVDDT register
        JP      Z,SVDEND        ;Go to SVDEND if SVD data is normal
;
;       Processing when SVD data is LOW
;
SVDEND:
        RET
```

3.12.3 Programming notes

(1) To obtain a stable SVD detection result, the SVD circuit must be on for at least l00 µsec. So, to obtain the SVD detection result, follow the programming sequence below.

① Set SVDON to "1"
② Maintain for 100 µsec minimum
③ Set SVDON to "0"
④ Read SVDDT

However, when f_{OSC1} (32.768 kHz, 38.4 kHz or 50 kHz) is selected for CPU system clock, the instruction cycles are long enough, so there is no need to worry about maintaining 100 µsec or more for SVDON = "1" in the software.

(2) The SVD circuit should normally be turned OFF as the consumption current of the IC becomes large when it is ON.

3.13 Interrupt

3.13.1 Interrupt vector, factor flag and mask register

When an interrupt request is input to the CPU, the CPU begins interrupt processing. After the program being executed is terminated, the interrupt processing is executed in the following order.

① The address data (value of program counter) of the program to be executed next is saved in the stack area (RAM).

② The interrupt request causes the value of the interrupt vector (page 1, 02H–0EH) to be set in the program counter.

③ The program at the specified address is executed (execution of interrupt processing routine by software).

Note: The processing in ① and ② above take 12 cycles of the CPU system clock.

Table 3.13.1.1 shows the correspondence of interrupt requests and interrupt vectors.

Table 3.13.1.1 Interrupt request and interrupt vectors

Interrupt vector (every Bank)	Interrupt factor	Priority
102H	Programmable timer	High
104H	Serial I/F (error generation)	↑
106H	Serial I/F (receiving completion)	
108H	Serial I/F (transmitting completion)	
10AH	K10–K13 input	
10CH	K00–K03 input	↓
10EH	Clock timer	Low

The four low-order bits of the program counter are indirectly addressed through the interrupt request.

Table 3.13.1.2 Interrupt factors

Interrupt factor	Interrupt factor flag	
Programmable timer (counter = 0)	IPT	(F8H•D0)
Serial interface (error generation)	ISIFE	(F9H•D2)
Serial interface (data receiving completion)	ISIFR	(F9H•D0)
Serial interface (data transmitting completion)	ISIFT	(F9H•D1)
K10–K13 input (falling or rising edge)	IK1	(FAH•D0)
K00–K03 input (falling or rising edge)	IK0	(FBH•D0)
Clock timer 1 Hz (falling edge)	IT3	(FCH•D3)
Clock timer 2 Hz (falling edge)	IT2	(FCH•D2)
Clock timer 8 Hz (falling edge)	IT1	(FCH•D1)
Clock timer 16 Hz (falling edge)	IT0	(FCH•D0)

Table 3.13.1.3 Interrupt mask registers and interrupt factor flags

Interrupt mask register		Interrupt factor flag	
EIPT	(F0H•D0)	IPT	(F8H•D0)
EISIFE	(F1H•D2)	ISIFE	(F9H•D2)
EISIFR	(F1H•D0)	ISIFR	(F9H•D0)
EISIFT	(F1H•D1)	ISIFT	(F9H•D1)
EIK1	(F2H•D0)	IK1	(FAH•D0)
EIK0	(F3H•D0)	IK0	(FBH•D0)
EIT3	(F4H•D3)	IT3	(FCH•D3)
EIT2	(F4H•D2)	IT2	(FCH•D2)
EIT1	(F4H•D1)	IT1	(FCH•D1)
EIT0	(F4H•D0)	IT0	(FCH•D0)

3.13.2 Example program for the interrupt

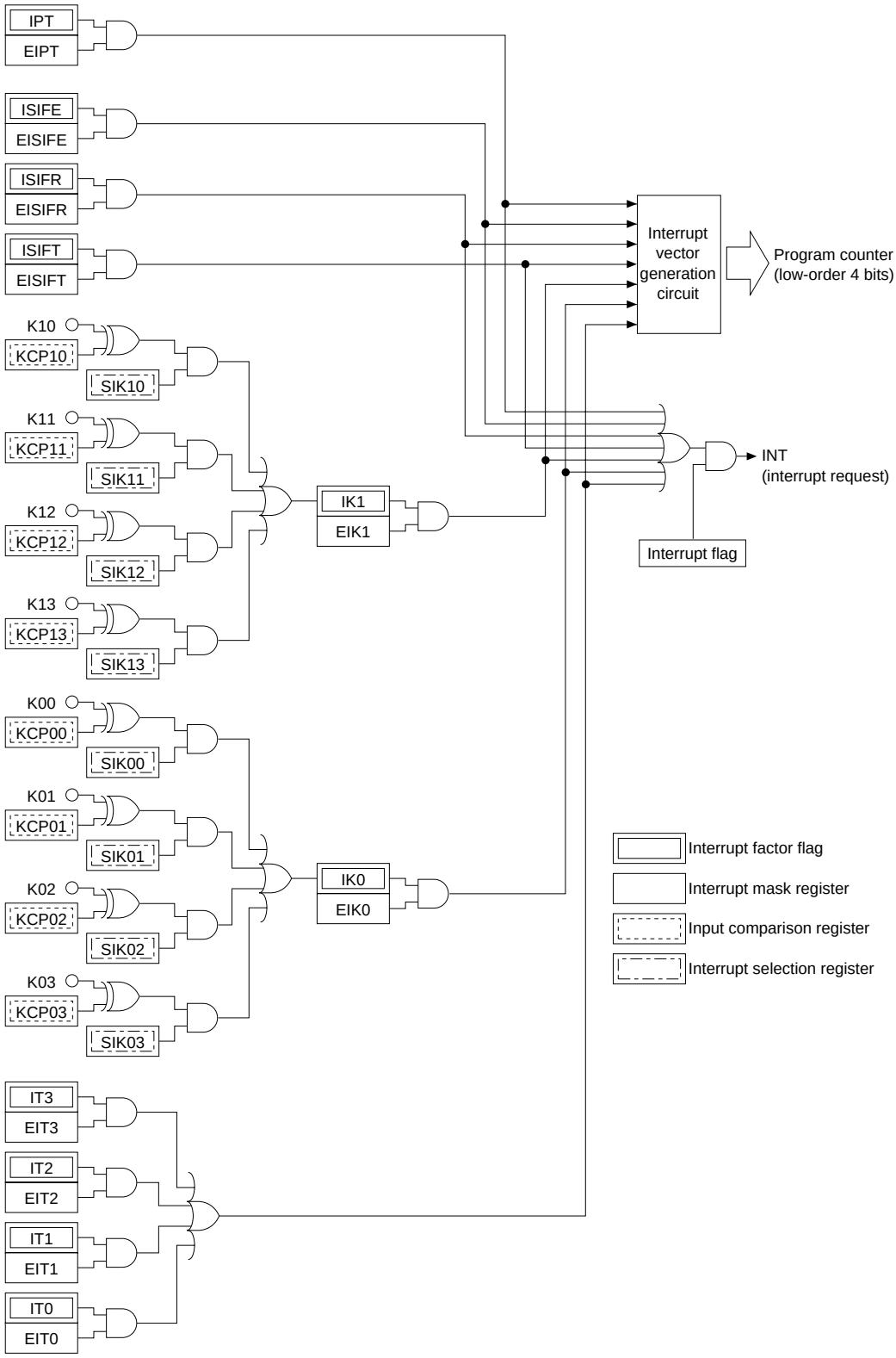


Fig. 3.13.2.1 Configuration of the interrupt circuit

Following program shows the interrupt processing procedure.

```
Label     Mnemonic/operand          Comment
;
;INTERRUPT
;

;EXAMPLE PROGRAM FOR INTERRUPT PROCESSING
        ORG     102H

        PSET    PTINT             ;Jump to programmable timer
        JP      PTINT             ;interrupt processing routine

        PSET    SIF_ERR           ;Jump to serial I/F (error)
        JP      SIF_ERR           ;interrupt processing routine

        PSET    SIF_RX            ;Jump to serial I/F (receiving)
        JP      SIF_RX            ;interrupt processing routine

        PSET    SIF_TX            ;Jump to serial I/F (transmitting)
        JP      SIF_TX            ;interrupt processing routine

        PSET    K1INT             ;Jump to K10-K13 input
        JP      K1INT             ;interrupt processing routine

        PSET    K0INT             ;Jump to K00-K03 input
        JP      K0INT             ;interrupt processing routine

        PSET    TIINT             ;Jump to clock timer
        JP      TIINT             ;interrupt processing routine

;EXAMPLE PROGRAM FOR PROGRAMMABLE TIMER INTERRUPT
PTINT:
        PUSH    YP
        PUSH    YH
        PUSH    YL
        PUSH    A

        LD      A,0
        LD      YP,A              ;Sets to page 0
        LD      Y,0F8H            ;Sets address to F8H
        LD      A,MY              ;Reads programmable timer interrupt factor flag
;
;       Interrupt processing program
;
        POP     A
        POP     YL
        POP     YH
        POP     YP

        EI
        RET

;EXAMPLE PROGRAM FOR SERIAL INTERFACE (ERROR) INTERRUPT
SIF_ERR:
        PUSH    YP
        PUSH    YH
        PUSH    YL
        PUSH    A

        LD      A,0
        LD      YP,A              ;Sets to page 0
        LD      Y,0F9H            ;Sets address to F9H
        LD      A,MY              ;Reads SIF interrupt factor flag
;
;       Interrupt processing program
;
        POP     A
        POP     YL
        POP     YH
```

```
        POP     YP

        EI
        RET

;EXAMPLE PROGRAM FOR SERIAL INTERFACE (RECEIVE) INTERRUPT
SIF_RX:
        PUSH    YP
        PUSH    YH
        PUSH    YL
        PUSH    A

        LD      A,0
        LD      YP,A            ;Sets to page 0
        LD      Y,0F9H          ;Sets address to F9H
        LD      A,MY            ;Reads SIF interrupt factor flag
;
;       Interrupt processing program
;
        POP     A
        POP     YL
        POP     YH
        POP     YP

        EI
        RET

;EXAMPLE PROGRAM FOR SERIAL INTERFACE (TRANSMIT) INTERRUPT
SIF_TX:
        PUSH    YP
        PUSH    YH
        PUSH    YL
        PUSH    A

        LD      A,0
        LD      YP,A            ;Sets to page 0
        LD      Y,0F9H          ;Sets address to F9H
        LD      A,MY            ;Reads SIF interrupt factor flag
;
;       Interrupt processing program
;
        POP     A
        POP     YL
        POP     YH
        POP     YP

        EI
        RET

;EXAMPLE PROGRAM FOR K1n INTERRUPT
K1INT:
        PUSH    YP
        PUSH    YH
        PUSH    YL
        PUSH    A

        LD      A,0
        LD      YP,A            ;Sets to page 0
        LD      Y,0FAH          ;Sets address FAH
        LD      A,MY            ;Reads K10-K13 input interrupt factor flag
;
;       Interrupt processing program
;
        POP     A
        POP     YL
        POP     YH
        POP     YP

        EI
        RET
```

```
;EXAMPLE PROGRAM FOR K0n INTERRUPT
K0INT:
        PUSH    YP
        PUSH    YH
        PUSH    YL
        PUSH    A

        LD      A,0
        LD      YP,A            ;Sets to page 0
        LD      Y,0FBH          ;Sets address FBH
        LD      A,MY            ;Reads K00-K03 input interrupt factor flag
;
;       Interrupt processing program
;
        POP     A
        POP     YL
        POP     YH
        POP     YP

        EI
        RET

;EXAMPLE PROGRAM FOR CLOCK TIMER INTERRUPT
TIINT:
        PUSH    YP
        PUSH    YH
        PUSH    YL
        PUSH    A
        PUSH    B

        LD      A,0
        LD      YP,A            ;Sets to page 0
        LD      Y,0FCH          ;Sets address to FCH
        LD      A,MY            ;Reads clock timer interrupt factor flag
        LD      Y,08DH          ;Sets address to 8DH
        LD      A,MY            ;Reads clock timer data
        LD      Y,08EH          ;Sets address to 8EH
        LD      B,MY            ;Reads clock timer data
;
;       Interrupt processing program
;
        POP     B
        POP     A
        POP     YL
        POP     YH
        POP     YP

        EI
        RET
```

3.13.3 Programming notes

(1) The interrupt factor flags are set when the timing condition is established, even if the interrupt mask registers are set to "0".

(2) Write the interrupt mask register only in the DI status (interrupt flag = "0"). Writing during EI status (interrupt flag = "1") will cause malfunction.

(3) Reading of interrupt factor flags is available at EI, but be careful in the following cases.
If the interrupt mask register value corresponding to the interrupt factor flags to be read is set to "1", an interrupt request will be generated by the interrupt factor flags set timing, or an interrupt request will not be generated. Be very careful when interrupt factor flags are in the same address.

(4) The interrupt vector address will be an interrupt vector within the bank that is specified by the program counter when an interrupt occurs.

CHAPTER 4 SUMMARY OF NOTES

Here, the cautionary notes are summed up by function category. Keep these notes well in mind when programming.

Memory

Memory is not mounted in unused area within the memory map and in memory area not indicated in this manual. For this reason, normal operation cannot be assured for programs that have been prepared with access to these areas.

Power supply and operating mode

(1) When operating with 0.9–1.25 V supply voltage, the boost mode must be set in the initial routine before controlling the peripheral circuits.

(2) When the supply voltage is out of the specified voltage range of an operating mode, do not switch into the operating mode. It may cause a malfunction or increase current consumption.

(3) Do not set HLON (halves) and DBON (doubling) to "1" at the same time.

(4) When switching from the normal mode to the boost/reduce mode, VDSEL or VCSEL should be set to "1" wait 100 msec or more for V_{D2} to stabilize after setting DBON or HLON to "1".

(5) When switching from the boost/reduce mode to the normal mode, use separate instructions to switch the mode (VDSEL = "0" or VCSEL = "0") and turn the voltage doubler/halver off (HLON = "0" or DBON = "0"). Simultaneous processing with a single instruction may cause malfunction.

Watchdog timer

When the watchdog timer is being used, the software must reset it within 3-second cycles.
When "Not used" is selected for the watchdog timer by the mask option, it is unnecessary to reset the watchdog timer.

Oscillation circuit

(1) When switching the CPU system clock from OSC1 to OSC3, set V_{D1} and the operating mode before turning the OSC3 oscillation ON. After that maintain 2.5 msec or more, and then turn the OSC3 oscillation ON.
When switching from OSC3 to OSC1, set V_{D1} and the operating mode after switching to OSC1 and turning the OSC3 oscillation OFF.

(2) When switching V_{D1} from 1.2 V to 2.1 V, or vice versa, be sure to hold the 1.4 V setting for more than 2.5 msec or more first for voltage stabilization.

(3) It takes at least 5 msec from the time the OSC3 oscillation circuit goes ON until the oscillation stabilizes. Consequently, when switching the CPU operation clock from OSC1 to OSC3, do this after a minimum of 5 msec have elapsed since the OSC3 oscillation went ON.
Further, the oscillation stabilization time varies depending on the external oscillator characteristics and conditions of use, so allow ample margin when setting the wait time.

(4) When switching the clock form OSC3 to OSC1, use a separate instruction for switching the OSC3 oscillation OFF. An error in the CPU operation can result if this processing is performed at the same time by the one instruction.

(5) Switching the operating voltage when the supply voltage is lower than the set voltage (that can generate V_{D1}) may cause a malfunction. Switch the operating voltage only after making sure that supply voltage is more than the set voltage using the SVD circuit.

(6) The OSC1 oscillation circuit deal with four types of crystal oscillators (32.768 kHz, 38.4 kHz, 50 kHz or 76.8 kHz). To operate the timer and other circuits properly, the prescaler should be selected according to the frequency of the connected oscillator.

Input ports

(1) When input ports are changed from low to high by pull up resistor, the rise of the waveform is delayed on account of the time constant of the pull up resistor and input gate capacitance. Hence, when fetching input ports, set an appropriate wait time.

Particular care needs to be taken of the key scan during key matrix configuration.
Make this waiting time the amount of time or more calculated by the following expression.
$10 \times C \times R$
C: terminal capacitance 5 pF + parasitic capacitance ? pF
R: pull up resistance 300 kΩ

(2) The K02 terminal functions as the clock input terminal for the programmable timer, and the input signal is combined with the input port and the programmable timer. Consequently, when the K02 terminal is set to the clock input terminal for the programmable timer, take care of the interrupt setting.

I/O ports

(1) When in the input mode, I/O ports are changed from low to high by pull up resistor, the rise of the waveform is delayed on account of the time constant of the pull up resistor and input gate capacitance. Hence, when fetching input ports, set an appropriate wait time.
Particular care needs to be taken of the key scan during key matrix configuration.
Make this waiting time the amount of time or more calculated by the following expression.
$10 \times C \times R$
C: terminal capacitance 5 pF + parasitic capacitance ? pF
R: pull up resistance 300 kΩ

(2) When special output has been selected, a hazard may occur when the signal is turned ON or OFF.

(3) When f_{OSC3} is selected for the FOUT output clock, it is necessary to turn the OSC3 oscillation ON before output.

(4) When Nch open drain has been selected for the P10–P13 output specifications by the mask option and during output mode, read data from the P10–P13 registers (address B6H•D0–D3) may differ from the data written to them.

LCD driver

Because at initial reset, the contents of display memory and LC3–LC0 (LCD contrast) are undefined, there is need to initialize by the software. Furthermore, take care of the registers LPWR and ALOFF because these are set so that the display goes OFF.

Clock timer

(1) The prescaler must be set correctly to suit the crystal oscillator to be used for the OSC1 oscillation circuit.

(2) Be sure to data reading in the order of low-order data (TM0–TM3) then high-order data (TM4–TM7).

(3) When the clock timer has been reset, the interrupt factor flag (IT) may sometimes be set to "1". Consequently, perform flag reading (reset the flag) as necessary at reset.

Programmable timer

(1) Be sure to data reading in the order of low-order data (PT0–PT3) then high-order data (PT4–PT7).

(2) When data of reload registers is set at "00H", the down-counter becomes a 256-value counter.

Serial interface

(1) Be sure to initialize the serial interface mode in the transmitting/receiving disable status (TXEN = RXEN = "0").

(2) Do not perform double trigger (writing "1") to TXTRG (RXTRG) when the serial interface is in the transmitting (receiving) operation.

(3) In the clock synchronous mode, since one clock line ($\overline{SCLK}$) is shared for both transmitting and receiving, transmitting and receiving cannot be performed simultaneously.
Consequently, be sure not to write "1" to RXTRG (TXTRG) when TXTRG (RXTRG) is "1".

(4) When a parity error or flaming error is generated during receiving in the asynchronous mode, the receiving error interrupt factor flag ISIFE is set to "1" prior to the receiving complete interrupt factor flag ISIFR for the time indicated in Table 4.1. Consequently, you should reset the receiving complete interrupt factor flag ISIFR to "0" by providing a wait time in error processing routines and similar routines.

When an overrun error is generated, the receiving complete interrupt factor flag ISIFR is not set to "1" and a receiving complete interrupt is not generated.

Table 4.1 Time difference between ISIFE and ISIFR on error generation

Clock source	Time difference
CPU clock / n	1/2 cycles of CPU clock / n
Programmable timer × 1/2	1 cycle of programmable timer underflow

(5) When the demultiplied signal of the OSC3 oscillation circuit is made the clock source, it is necessary to turn the OSC3 oscillation ON, prior to using the serial interface.
A time interval of 5 msec, from the turning ON of the OSC3 oscillation circuit to until the oscillation stabilizes, is necessary, due to the oscillation element that is used. Consequently, you should allow an adequate waiting time after turning ON of the OSC3 oscillation, before starting transmitting/receiving of serial interface. (The oscillation start time will vary somewhat depending on the oscillator and on the externally attached parts. Refer to the oscillation start time example indicated in Chapter 7, "ELECTRICAL CHARACTERISTICS", in the "Technical Hardware".)
At initial reset, the OSC3 oscillation circuit is set to OFF status.

Sound generator

A hazard may occur when data of the BZE register or the buzzer frequency selection registers (BZFQ0–BZFQ2) are changed.

External memory access

Be sure to data writing/reading for external memory in the order of low-order bits (D00–D03) then high-order bits (D04–D07).

SVD circuit

(1) To obtain a stable SVD detection result, the SVD circuit must be on for at least l00 μsec. So, to obtain the SVD detection result, follow the programming sequence below.

① Set SVDON to "1"
② Maintain for 100 μsec minimum
③ Set SVDON to "0"
④ Read SVDDT

However, when f_{OSC1} (32.768 kHz, 38.4 kHz or 50 kHz) is selected for CPU system clock, the instruction cycles are long enough, so there is no need to worry about maintaining 100 μsec or more for SVDON = "1" in the software.

(2) The SVD circuit should normally be turned OFF as the consumption current of the IC becomes large when it is ON.

Interrupt

(1) The interrupt factor flags are set when the timing condition is established, even if the interrupt mask registers are set to "0".

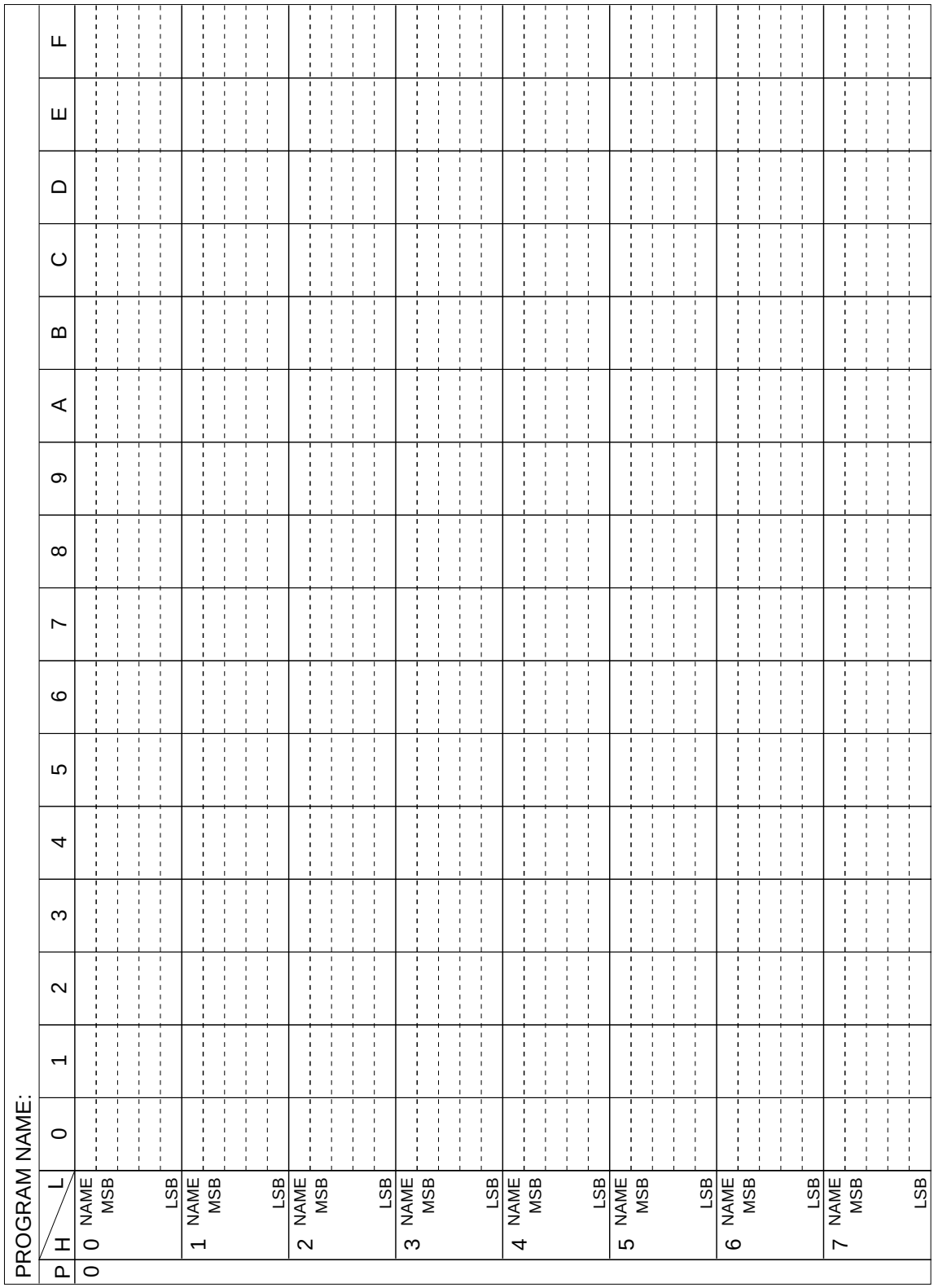
(2) Write the interrupt mask register only in the DI status (interrupt flag = "0"). Writing during EI status (interrupt flag = "1") will cause malfunction.

(3) Reading of interrupt factor flags is available at EI, but be careful in the following cases.
If the interrupt mask register value corresponding to the interrupt factor flags to be read is set to "1", an interrupt request will be generated by the interrupt factor flags set timing, or an interrupt request will not be generated. Be very careful when interrupt factor flags are in the same address.

(4) The interrupt vector address will be an interrupt vector within the bank that is specified by the program counter when an interrupt occurs.

APPENDIX A E0C6247 DATA MEMORY (RAM) MAP

RAM map - 1 (000H–07FH)



RAM map - 2 (100H–17FH)

PROGRAM NAME:

P	H \ L	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
1	0	NAME MSB															
		LSB															
	1	NAME MSB															
		LSB															
	2	NAME MSB															
		LSB															
	3	NAME MSB															
		LSB															
	4	NAME MSB															
		LSB															
	5	NAME MSB															
		LSB															
	6	NAME MSB															
		LSB															
	7	NAME MSB															
		LSB															

RAM map - 3 (200H–27FH)

PROGRAM NAME:

P	H \ L	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
2	0	NAME MSB															
		LSB															
	1	NAME MSB															
		LSB															
	2	NAME MSB															
		LSB															
	3	NAME MSB															
		LSB															
	4	NAME MSB															
		LSB															
	5	NAME MSB															
		LSB															
	6	NAME MSB															
		LSB															
	7	NAME MSB															
		LSB															

RAM map - 4 (300H–37FH)

PROGRAM NAME:

P	H \ L	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
3	0	NAME MSB															LSB
	1	NAME MSB															LSB
	2	NAME MSB															LSB
	3	NAME MSB															LSB
	4	NAME MSB															LSB
	5	NAME MSB															LSB
	6	NAME MSB															LSB
	7	NAME MSB															LSB

RAM map - 5 (400H–47FH)

PROGRAM NAME:

P	H \ L	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
4	0	NAME MSB															LSB
	1	NAME MSB															LSB
	2	NAME MSB															LSB
	3	NAME MSB															LSB
	4	NAME MSB															LSB
	5	NAME MSB															LSB
	6	NAME MSB															LSB
	7	NAME MSB															LSB

RAM map - 6 (480H–4FFH)

PROGRAM NAME:

P	H \ L	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
4	8	NAME MSB															LSB
	9	NAME MSB															LSB
	A	NAME MSB															LSB
	B	NAME MSB															LSB
	C	NAME MSB															LSB
	D	NAME MSB															LSB
	E	NAME MSB															LSB
	F	NAME MSB															LSB

RAM map - 7 (500H–57FH)

PROGRAM NAME:

P	H \ L	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
5	0	NAME MSB															LSB
	1	NAME MSB															LSB
	2	NAME MSB															LSB
	3	NAME MSB															LSB
	4	NAME MSB															LSB
	5	NAME MSB															LSB
	6	NAME MSB															LSB
	7	NAME MSB															LSB

RAM map - 8 (580H–5FFH)

PROGRAM NAME:

P	H \ L	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
5	8	NAME MSB															LSB
	9	NAME MSB															LSB
	A	NAME MSB															LSB
	B	NAME MSB															LSB
	C	NAME MSB															LSB
	D	NAME MSB															LSB
	E	NAME MSB															LSB
	F	NAME MSB															LSB

RAM map - 9 (600H–67FH)

PROGRAM NAME:

P	H \ L	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
6	0	NAME MSB															
		LSB															
	1	NAME MSB															
		LSB															
	2	NAME MSB															
		LSB															
	3	NAME MSB															
		LSB															
	4	NAME MSB															
		LSB															
	5	NAME MSB															
		LSB															
	6	NAME MSB															
		LSB															
	7	NAME MSB															
		LSB															

RAM map - 10 (680H–6FFH)

PROGRAM NAME:

P	H \ L	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
6	8	NAME MSB															LSB
	9	NAME MSB															LSB
	A	NAME MSB															LSB
	B	NAME MSB															LSB
	C	NAME MSB															LSB
	D	NAME MSB															LSB
	E	NAME MSB															LSB
	F	NAME MSB															LSB

RAM map - 11 (700H–77FH)

PROGRAM NAME:

P	H \ L	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
7	0	NAME MSB															LSB
	1	NAME MSB															LSB
	2	NAME MSB															LSB
	3	NAME MSB															LSB
	4	NAME MSB															LSB
	5	NAME MSB															LSB
	6	NAME MSB															LSB
	7	NAME MSB															LSB

RAM map - 12 (780H–7FFH)

PROGRAM NAME:

P	H \ L	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
7	8	NAME MSB															
		LSB															
	9	NAME MSB															
		LSB															
	A	NAME MSB															
		LSB															
	B	NAME MSB															
		LSB															
	C	NAME MSB															
		LSB															
	D	NAME MSB															
		LSB															
	E	NAME MSB															
		LSB															
	F	NAME MSB															
		LSB															

RAM map - 13 (800H–87FH)

PROGRAM NAME:																
P	H \ L	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
8	0	NAME MSB															LSB
	1	NAME MSB															LSB
	2	NAME MSB															LSB
	3	NAME MSB															LSB
	4	NAME MSB															LSB
	5	NAME MSB															LSB
	6	NAME MSB															LSB
	7	NAME MSB															LSB

RAM map - 14 (880H–8FFH)

PROGRAM NAME:

P	H \ L	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
8	8	NAME MSB LSB															
	9	NAME MSB LSB															
	A	NAME MSB LSB															
	B	NAME MSB LSB															
	C	NAME MSB LSB															
	D	NAME MSB LSB															
	E	NAME MSB LSB															
	F	NAME MSB LSB															

Display memory (A00H–A7FH)

PROGRAM NAME:

P	H \ L	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
A	0	NAME MSB															
		LSB															
	1	NAME MSB															
		LSB															
	2	NAME MSB															
		LSB															
	3	NAME MSB															
		LSB															
	4	NAME MSB															
		LSB															
	5	NAME MSB															
		LSB															
	6	NAME MSB															
		LSB															
	7	NAME MSB															
		LSB															

Display memory (A80H–AFFH)

PROGRAM NAME:

P \ L	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
A 8	NAME MSB															LSB
9	NAME MSB															LSB
A	NAME MSB															LSB
B	NAME MSB															LSB
C	NAME MSB															LSB
D	NAME MSB															LSB
E	NAME MSB															LSB
F	NAME MSB															LSB

I/O memory (Page 0 to 3, 80H–FFH)

PROGRAM NAME:

P	H \ L		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	8	NAME			–	–		–	–	–								–
		MSB	SVDS3	0	–	–	VCSEL	–	–	–	0	CLKCHG	FOUTE	0	0	TM3	TM7	–
1			SVDS2	0	–	–	VDSEL	–	–	–	0	OSCC	0	0	0	TM2	TM6	–
			SVDS1	SVDDT	–	–	HLON	–	–	–	PRSM1	VDC1	FOFQ1	0	TMRUN	TM1	TM5	–
2		LSB	SVDS0	SVDON	–	–	DBON	–	–	–	PRSM0	VDC0	FOFQ0	WDRST	TMRST	TM0	TM4	–
3	9	NAME				–				–								–
		MSB	SIK03	K03	KCP03	–	SIK13	K13	KCP13	–	EXTMF	HZCS	A03	A07	A11	A15	0	–
			SIK02	K02	KCP02	–	SIK12	K12	KCP12	–	0	HZBUS	A02	A06	A10	A14	0	–
			SIK01	K01	KCP01	–	SIK11	K11	KCP11	–	MEMS1	ADINC	A01	A05	A09	A13	0	–
		LSB	SIK00	K00	KCP00	–	SIK10	K10	KCP10	–	MEMS0	PICON	A00	A04	A08	A12	A16	–
	A	NAME												–	–	–	–	–
		MSB	0	R03	0	R13	0	R23	R33HIZ	R33	R43HIZ	R43	SELR43	–	–	–	–	–
			0	R02	0	R12	0	R22	R32HIZ	R32	R42HIZ	R42	SELR42	–	–	–	–	–
			0	R01	0	R11	0	R21	R31HIZ	R31	R41HIZ	R41	0	–	–	–	–	–
		LSB	R0HIZ	R00	R1HIZ	R10	R2HIZ	R20	R30HIZ	R30	R40HIZ	R40	0	–	–	–	–	–
	B	NAME				–				–				–				
		MSB	IOC03	PUL03	P03/D03	–	IOC13	PUL13	P13/D07	–	IOC23	PUL23	P23/CS3	–	IOC33	PUL33	P33	SELP33
			IOC02	PUL02	P02/D02	–	IOC12	PUL12	P12/D06	–	IOC22	PUL22	P22/CS2	–	IOC32	PUL32	P32	SELP32
			IOC01	PUL01	P01/D01	–	IOC11	PUL11	P11/D05	–	IOC21	PUL21	P21/CS1	–	IOC31	PUL31	P31	SELP31
		LSB	IOC00	PUL00	P00/D00	–	IOC10	PUL10	P10/D04	–	IOC20	PUL20	P20/CS0	–	IOC30	PUL30	P30	SELP30
	C	NAME				–	–	–	–	–							–	–
		MSB	IOC43	PUL43	P43	–	–	–	–	–	0	EPR	RXTRG	0	TRXD3	TRXD7	–	–
			IOC42	PUL42	P42	–	–	–	–	–	SMD1	PMD	RXEN	FER	TRXD2	TRXD6	–	–
			IOC41	PUL41	P41	–	–	–	–	–	SMD0	SCS1	TXTRG	PER	TRXD1	TRXD5	–	–
		LSB	IOC40	PUL40	P40	–	–	–	–	–	ESIF	SCS0	TXEN	OER	TRXD0	TRXD4	–	–
	D	NAME				–	–	–	–	–	–	–	–	–	–	–	–	–
		MSB	LDUTY	0	LC3	–	–	–	–	–	–	–	–	–	–	–	–	–
			VCCHG	ALOFF	LC2	–	–	–	–	–	–	–	–	–	–	–	–	–
			–	ALON	LC1	–	–	–	–	–	–	–	–	–	–	–	–	–
		LSB	LPWR	0	LC0	–	–	–	–	–	–	–	–	–	–	–	–	–
	E	NAME					–	–	–	–								–
		MSB	ENRTM	0	0	0	–	–	–	–	0	0	PNRFS	RD3	RD7	PT3	PT7	–
			ENRST	BZSTP	BZFQ2	BDTY2	–	–	–	–	0	0	PTOE	RD2	RD6	PT2	PT6	–
			ENON	BZSHT	BZFQ1	BDTY1	–	–	–	–	PTPS1	PTPC1	PTRUN	RD1	RD5	PT1	PT5	–
		LSB	BZE	SHTPW	BZFQ0	BDTY0	–	–	–	–	PTPS0	PTPC0	PTRST	RD0	RD4	PT0	PT4	–
	F	NAME						–	–	–							–	–
		MSB	0	0	0	0	EIT3	–	–	–	0	0	0	0	IT3	–	–	–
			0	EISIFE	0	0	EIT2	–	–	–	0	ISIFE	0	0	IT2	–	–	–
			0	EISIFT	0	0	EIT1	–	–	–	0	ISIFT	0	0	IT1	–	–	–
		LSB	EIPT	EISIFR	EIK1	EIK0	EIT0	–	–	–	IPT	ISIFR	IK1	IK0	IT0	–	–	–

APPENDIX B E0C6247 INSTRUCTION SET

Instruction set - 1

Classification	Mnemonic	Operand	Operation Code												Flag				Clock	Operation
			B	A	9	8	7	6	5	4	3	2	1	0	I	D	Z	C		
Branch instructions	PSET	p	1	1	1	0	0	1	0	p4	p3	p2	p1	p0					5	NBP ← p4, NPP ← p3~p0
	JP	s	0	0	0	0	s7	s6	s5	s4	s3	s2	s1	s0					5	PCB ← NBP, PCP ← NPP, PCS ← s7~s0
		C, s	0	0	1	0	s7	s6	s5	s4	s3	s2	s1	s0					5	PCB ← NBP, PCP ← NPP, PCS ← s7~s0 if C=1
		NC, s	0	0	1	1	s7	s6	s5	s4	s3	s2	s1	s0					5	PCB ← NBP, PCP ← NPP, PCS ← s7~s0 if C=0
		Z, s	0	1	1	0	s7	s6	s5	s4	s3	s2	s1	s0					5	PCB ← NBP, PCP ← NPP, PCS ← s7~s0 if Z=1
		NZ, s	0	1	1	1	s7	s6	s5	s4	s3	s2	s1	s0					5	PCB ← NBP, PCP ← NPP, PCS ← s7~s0 if Z=0
	JPBA		1	1	1	1	1	1	1	0	1	0	0	0					5	PCB ← NBP, PCP ← NPP, PCSH ← B, PCSL ← A
	CALL	s	0	1	0	0	s7	s6	s5	s4	s3	s2	s1	s0					7	M(SP-1) ← PCP, M(SP-2) ← PCSH, M(SP-3) ← PCSL+1 SP ← SP-3, PCP ← NPP, PCS ← s7~s0
	CALZ	s	0	1	0	1	s7	s6	s5	s4	s3	s2	s1	s0					7	M(SP-1) ← PCP, M(SP-2) ← PCSH, M(SP-3) ← PCSL+1 SP ← SP-3, PCP ← 0, PCS ← s7~s0
	RET		1	1	1	1	1	1	0	1	1	1	1	1					7	PCSL ← M(SP), PCSH ← M(SP+1), PCP ← M(SP+2) SP ← SP+3
	RETS		1	1	1	1	1	1	0	1	1	1	1	0					12	PCSL ← M(SP), PCSH ← M(SP+1), PCP ← M(SP+2) SP ← SP+3, PC ← PC+1
	RETD	*l*	0	0	0	1	*l*7	*l*6	*l*5	*l*4	*l*3	*l*2	*l*1	*l*0					12	PCSL ← M(SP), PCSH ← M(SP+1), PCP ← M(SP+2) SP ← SP+3, M(X) ← *l*3~*l*0, M(X+1) ← *l*7~*l*4, X ← X+2
System control instructions	NOP5		1	1	1	1	1	1	1	1	1	0	1	1					5	No operation (5 clock cycles)
	NOP7		1	1	1	1	1	1	1	1	1	1	1	1					7	No operation (7 clock cycles)
	HALT		1	1	1	1	1	1	1	1	1	0	0	0					5	Halt (stop clock)
Index operation instructions	INC	X	1	1	1	0	1	1	1	0	0	0	0	0					5	X ← X+1
		Y	1	1	1	0	1	1	1	1	0	0	0	0					5	Y ← Y+1
	LD	X, x	1	0	1	1	x7	x6	x5	x4	x3	x2	x1	x0					5	XH ← x7~x4, XL ← x3~x0
		Y, y	1	0	0	0	y7	y6	y5	y4	y3	y2	y1	y0					5	YH ← y7~y4, YL ← y3~y0
		XP, r	1	1	1	0	1	0	0	0	0	0	r1	r0					5	XP ← r
		XH, r	1	1	1	0	1	0	0	0	0	1	r1	r0					5	XH ← r
		XL, r	1	1	1	0	1	0	0	0	1	0	r1	r0					5	XL ← r
		YP, r	1	1	1	0	1	0	0	1	0	0	r1	r0					5	YP ← r
		YH, r	1	1	1	0	1	0	0	1	0	1	r1	r0					5	YH ← r
		YL, r	1	1	1	0	1	0	0	1	1	0	r1	r0					5	YL ← r
		r, XP	1	1	1	0	1	0	1	0	0	0	r1	r0					5	r ← XP
		r, XH	1	1	1	0	1	0	1	0	0	1	r1	r0					5	r ← XH
		r, XL	1	1	1	0	1	0	1	0	1	0	r1	r0					5	r ← XL
		r, YP	1	1	1	0	1	0	1	1	0	0	r1	r0					5	r ← YP
		r, YH	1	1	1	0	1	0	1	1	0	1	r1	r0					5	r ← YH
		r, YL	1	1	1	0	1	0	1	1	1	0	r1	r0					5	r ← YL
	ADC	XH, i	1	0	1	0	0	0	0	0	i3	i2	i1	i0			↕	↕	7	XH ← XH+i3~i0+C
		XL, i	1	0	1	0	0	0	0	1	i3	i2	i1	i0			↕	↕	7	XL ← XL+i3~i0+C
		YH, i	1	0	1	0	0	0	1	0	i3	i2	i1	i0			↕	↕	7	YH ← YH+i3~i0+C
		YL, i	1	0	1	0	0	0	1	1	i3	i2	i1	i0			↕	↕	7	YL ← YL+i3~i0+C

Instruction set - 2

Classification	Mnemonic	Operand	Operation Code												Flag				Clock	Operation
			B	A	9	8	7	6	5	4	3	2	1	0	I	D	Z	C		
Index operation instructions	CP	XH, i	1	0	1	0	0	1	0	0	i3	i2	i1	i0			↕	↕	7	XH-i3~i0
		XL, i	1	0	1	0	0	1	0	1	i3	i2	i1	i0			↕	↕	7	XL-i3~i0
		YH, i	1	0	1	0	0	1	1	0	i3	i2	i1	i0			↕	↕	7	YH-i3~i0
		YL, i	1	0	1	0	0	1	1	1	i3	i2	i1	i0			↕	↕	7	YL-i3~i0
Data transfer instructions	LD	r, i	1	1	1	0	0	0	r1	r0	i3	i2	i1	i0					5	r ← i3~i0
		r, q	1	1	1	0	1	1	0	0	r1	r0	q1	q0					5	r ← q
		A, Mn	1	1	1	1	1	0	1	0	n3	n2	n1	n0					5	A ← M(n3~n0)
		B, Mn	1	1	1	1	1	0	1	1	n3	n2	n1	n0					5	B ← M(n3~n0)
		Mn, A	1	1	1	1	1	0	0	0	n3	n2	n1	n0					5	M(n3~n0) ← A
		Mn, B	1	1	1	1	1	0	0	1	n3	n2	n1	n0					5	M(n3~n0) ← B
	LDPX	MX, i	1	1	1	0	0	1	1	0	i3	i2	i1	i0					5	M(X) ← i3~i0, X ← X+1
		r, q	1	1	1	0	1	1	1	0	r1	r0	q1	q0					5	r ← q, X ← X+1
	LDPY	MY, i	1	1	1	0	0	1	1	1	i3	i2	i1	i0					5	M(Y) ← i3~i0, Y ← Y+1
		r, q	1	1	1	0	1	1	1	1	r1	r0	q1	q0					5	r ← q, Y ← Y+1
	LBPX	MX, *l*	1	0	0	1	*l*7	*l*6	*l*5	*l*4	*l*3	*l*2	*l*1	*l*0					5	M(X) ← *l*3~*l*0, M(X+1) ← *l*7~*l*4, X ← X+2
Flag operation instructions	SET	F, i	1	1	1	1	0	1	0	0	i3	i2	i1	i0	↑	↑	↑	↑	7	F ← F∨i3~i0
	RST	F, i	1	1	1	1	0	1	0	1	i3	i2	i1	i0	↓	↓	↓	↓	7	F ← F∧i3~i0
	SCF		1	1	1	1	0	1	0	0	0	0	0	1				↑	7	C ← 1
	RCF		1	1	1	1	0	1	0	1	1	1	1	0				↓	7	C ← 0
	SZF		1	1	1	1	0	1	0	0	0	0	1	0			↑		7	Z ← 1
	RZF		1	1	1	1	0	1	0	1	1	1	0	1			↓		7	Z ← 0
	SDF		1	1	1	1	0	1	0	0	0	1	0	0		↑			7	D ← 1 (Decimal Adjuster ON)
	RDF		1	1	1	1	0	1	0	1	1	0	1	1		↓			7	D ← 0 (Decimal Adjuster OFF)
	EI		1	1	1	1	0	1	0	0	1	0	0	0	↑				7	I ← 1 (Enables Interrupt)
	DI		1	1	1	1	0	1	0	1	0	1	1	1	↓				7	I ← 0 (Disables Interrupt)
Stack operation instructions	INC	SP	1	1	1	1	1	1	0	1	1	0	1	1					5	SP ← SP+1
	DEC	SP	1	1	1	1	1	1	0	0	1	0	1	1					5	SP ← SP-1
	PUSH	r	1	1	1	1	1	1	0	0	0	0	r1	r0					5	SP ← SP-1, M(SP) ← r
		XP	1	1	1	1	1	1	0	0	0	1	0	0					5	SP ← SP-1, M(SP) ← XP
		XH	1	1	1	1	1	1	0	0	0	1	0	1					5	SP ← SP-1, M(SP) ← XH
		XL	1	1	1	1	1	1	0	0	0	1	1	0					5	SP ← SP-1, M(SP) ← XL
		YP	1	1	1	1	1	1	0	0	0	1	1	1					5	SP ← SP-1, M(SP) ← YP
		YH	1	1	1	1	1	1	0	0	1	0	0	0					5	SP ← SP-1, M(SP) ← YH
		YL	1	1	1	1	1	1	0	0	1	0	0	1					5	SP ← SP-1, M(SP) ← YL
		F	1	1	1	1	1	1	0	0	1	0	1	0					5	SP ← SP-1, M(SP) ← F
	POP	r	1	1	1	1	1	1	0	1	0	0	r1	r0					5	r ← M(SP), SP ← SP+1
		XP	1	1	1	1	1	1	0	1	0	1	0	0					5	XP ← M(SP), SP ← SP+1
		XH	1	1	1	1	1	1	0	1	0	1	0	1					5	XH ← M(SP), SP ← SP+1
		XL	1	1	1	1	1	1	0	1	0	1	1	0					5	XL ← M(SP), SP ← SP+1
		YP	1	1	1	1	1	1	0	1	0	1	1	1					5	YP ← M(SP), SP ← SP+1

Instruction set - 3

Classification	Mnemonic	Operand	Operation Code												Flag				Clock	Operation
			B	A	9	8	7	6	5	4	3	2	1	0	I	D	Z	C		
Stack operation instructions	POP	YH	1	1	1	1	1	1	0	1	1	0	0	0					5	YH← M(SP), SP← SP+1
		YL	1	1	1	1	1	1	0	1	1	0	0	1					5	YL← M(SP), SP← SP+1
		F	1	1	1	1	1	1	0	1	1	0	1	0	↕	↕	↕	↕	5	F← M(SP), SP← SP+1
	LD	SPH, r	1	1	1	1	1	1	1	0	0	0	r1	r0					5	SPH← r
		SPL, r	1	1	1	1	1	1	1	1	0	0	r1	r0					5	SPL ← r
		r, SPH	1	1	1	1	1	1	1	0	0	1	r1	r0					5	r← SPH
		r, SPL	1	1	1	1	1	1	1	1	0	1	r1	r0					5	r← SPL
Arithmetic instructions	ADD	r, i	1	1	0	0	0	0	r1	r0	i3	i2	i1	i0	★	↕	↕		7	r← r+i3~i0
		r, q	1	0	1	0	1	0	0	0	r1	r0	q1	q0	★	↕	↕		7	r← r+q
	ADC	r, i	1	1	0	0	0	1	r1	r0	i3	i2	i1	i0	★	↕	↕		7	r← r+i3~i0+C
		r, q	1	0	1	0	1	0	0	1	r1	r0	q1	q0	★	↕	↕		7	r← r+q+C
	SUB	r, q	1	0	1	0	1	0	1	0	r1	r0	q1	q0	★	↕	↕		7	r← r-q
	SBC	r, i	1	1	0	1	0	1	r1	r0	i3	i2	i1	i0	★	↕	↕		7	r← r-i3~i0-C
		r, q	1	0	1	0	1	0	1	1	r1	r0	q1	q0	★	↕	↕		7	r← r-q-C
	AND	r, i	1	1	0	0	1	0	r1	r0	i3	i2	i1	i0		↕			7	r← r∧ i3~i0
		r, q	1	0	1	0	1	1	0	0	r1	r0	q1	q0		↕			7	r← r∧ q
	OR	r, i	1	1	0	0	1	1	r1	r0	i3	i2	i1	i0		↕			7	r← r∨i3~i0
		r, q	1	0	1	0	1	1	0	1	r1	r0	q1	q0		↕			7	r← r∨q
	XOR	r, i	1	1	0	1	0	0	r1	r0	i3	i2	i1	i0		↕			7	r← r∀i3~i0
		r, q	1	0	1	0	1	1	1	0	r1	r0	q1	q0		↕			7	r← r∀q
	CP	r, i	1	1	0	1	1	1	r1	r0	i3	i2	i1	i0		↕	↕		7	r-i3~i0
		r, q	1	1	1	1	0	0	0	0	r1	r0	q1	q0		↕	↕		7	r-q
	FAN	r, i	1	1	0	1	1	0	r1	r0	i3	i2	i1	i0		↕			7	r∧i3~i0
		r, q	1	1	1	1	0	0	0	1	r1	r0	q1	q0		↕			7	r∧q
	RLC	r	1	0	1	0	1	1	1	1	r1	r0	r1	r0		↕	↕		7	d3←d2, d2←d1, d1←d0, d0←C, C←d3
	RRC	r	1	1	1	0	1	0	0	0	1	1	r1	r0		↕	↕		5	d3←C, d2←d3, d1←d2, d0←d1, C←d0
	INC	Mn	1	1	1	1	0	1	1	0	n3	n2	n1	n0		↕	↕		7	M(n3~n0) ←M(n3~n0)+1
	DEC	Mn	1	1	1	1	0	1	1	1	n3	n2	n1	n0		↕	↕		7	M(n3~n0) ←M(n3~n0)-1
	ACPX	MX, r	1	1	1	1	0	0	1	0	1	0	r1	r0	★	↕	↕		7	M(X) ←M(X)+r+C, X ←X+1
	ACPY	MY, r	1	1	1	1	0	0	1	0	1	1	r1	r0	★	↕	↕		7	M(Y) ←M(Y)+r+C, Y ←Y+1
	SCPX	MX, r	1	1	1	1	0	0	1	1	1	0	r1	r0	★	↕	↕		7	M(X) ←M(X)-r-C, X← X+1
	SCPY	MY, r	1	1	1	1	0	0	1	1	1	1	r1	r0	★	↕	↕		7	M(Y) ←M(Y)-r-C, Y ← Y+1
	NOT	r	1	1	0	1	0	0	r1	r0	1	1	1	1		↕			7	r←$\overline{r}$

Abbreviations used in the explanations have the following meanings.

Symbols associated with registers and memory

A A register
B B register
X XHL register
(low order eight bits of index register IX)
Y YHL register
(low order eight bits of index register IY)
XH XH register
(high order four bits of XHL register)
XL XL register
(low order four bits of XHL register)
YH YH register
(high order four bits of YHL register)
YL YL register
(low order four bits of YHL register)
XP XP register
(high order four bits of index register IX)
YP YP register
(high order four bits of index register IY)
SP Stack pointer SP
SPH High-order four bits of stack pointer SP
SPL Low-order four bits of stack pointer SP
MX, M(X) Data memory whose address is specified with index register IX
MY, M(Y) Data memory whose address is specified with index register IY
Mn, M(n) Data memory address 000H–00FH (address specified with immediate data n of 00H–0FH)
M(SP) Data memory whose address is specified with stack pointer SP
r, q Two-bit register code
r, q is two-bit immediate data; according to the contents of these bits, they indicate registers A, B, and MX and MY (data memory whose addresses are specified with index registers IX and IY)

r		q		Register
r1	r0	q1	q0	specified
0	0	0	0	A
0	1	0	1	B
1	0	1	0	MX
1	1	1	1	MY

Symbols associated with program counter

NBP New bank pointer
NPP New page pointer
PCB Program counter bank
PCP Program counter page
PCS Program counter step
PCSH Four high order bits of PCS
PCSL Four low order bits of PCS

Symbols associated with flags

F Flag register (I, D, Z, C)
C Carry flag
Z Zero flag
D Decimal flag
I Interrupt flag
↓ Flag reset
↑ Flag set
↕ Flag set or reset

Associated with immediate data

p Five-bit immediate data or label 00H–1FH
s Eight-bit immediate data or label 00H–0FFH
l Eight-bit immediate data 00H–0FFH
i Four-bit immediate data 00H–0FH

Associated with arithmetic and other operations

+ Add
- Subtract
∧ Logical AND
∨ Logical OR
∀ Exclusive-OR
★ Add-subtract instruction for decimal operation when the D flag is set

APPENDIX C PSEUDO-INSTRUCTION TABLE OF THE CROSS ASSEMBLER

Item No.	Pseudo-instruction	Meaning	Example of Use
1	EQU (Equation)	To allocate data to label	`ABC EQU 9` `BCD EQU ABC+1`
2	ORG (Origin)	To define location counter	`ORG 100H` `ORG 256`
3	SET (Set)	To allocate data to label (data can be changed)	`ABC SET 0001H` `ABC SET 0002H`
4	DW (Define Word)	To define ROM data	`ABC DW 'AB'` `BCD DW 0FFBH`
5	PAGE (Page)	To define boundary of page	`PAGE 1H` `PAGE 15`
6	SECTION (Section)	To define boundary of section	`SECTION`
7	BANK (Bank)	To define boundary of bank	`BANK 0` `BANK 1H`
8	END (End)	To terminate assembly	`END`

9	MACRO
	(Macro)
		To define macro	`CHECK MACRO DATA`
			`LOCAL LOOP`
			`LOOP CP MX,DATA`
			`JP NZ,LOOP`
			`ENDM`
			
			`CHECK 1`

10	LOCAL (Local)	To make local specification of label during macro definition	
11	ENDM (End Macro)	To end macro definition	

APPENDIX D COMMAND TABLE OF ICE6200

ICE6200 command table - 1

Item No.	Function	Command Format	Outline of Operation
1	Assemble	#A,a ↵	Assemble command mnemonic code and store at address "a"
2	Disassemble	#L,a1,a2 ↵	Contents of addresses a1 to a2 are disassembled and displayed
3	Dump	#DP,a1,a2 ↵	Contents of program area a1 to a2 are displayed
		#DD,a1,a2 ↵	Content of data area a1 to a2 are displayed
4	Fill	#FP,a1,a2,d ↵	Data d is set in addresses a1 to a2 (program area)
		#FD,a1,a2,d ↵	Data d is set in addresses a1 to a2 (data area)
5	Set Run Mode	#G,a ↵	Program is executed from the "a" address
		#TIM ↵	Execution time and step counter selection
		#OTF ↵	On-the-fly display selection
6	Trace	#T,a,n ↵	Executes program while displaying results of step instruction from "a" address
		#U,a,n ↵	Displays only the final step of #T,a,n
7	Break	#BA,a ↵ #BAR,a ↵	Sets Break at program address "a" Breakpoint is canceled
		#BD ↵ #BDR ↵	Break condition is set for data RAM Breakpoint is canceled
		#BR ↵ #BRR ↵	Break condition is set for EVA62XXCPU internal registers Breakpoint is canceled
		#BM ↵ #BMR ↵	Combined break conditions set for program data RAM address and registers Cancel combined break conditions for program data ROM address and registers
		#BRES ↵	All break conditions canceled
		#BC ↵	Break condition displayed
		#BE ↵	Enter break enable mode
		#BSYN ↵	Enter break disable mode
		#BT ↵	Set break stop/trace modes
		#BRKSEL,REM ↵	Set BA condition clear/remain modes
8	Move	#MP,a1,a2,a3 ↵	Contents of program area addresses a1 to a2 are moved to addresses a3 and after
		#MD,a1,a2,a3 ↵	Contents of data area addresses a1 to a2 are moved to addresses a3 and after
9	Data Set	#SP,a ↵	Data from program area address "a" are written to memory
		#SD,a ↵	Data from data area address "a" are written to memory
10	Change CPU Internal Registers	#DR ↵	Display EVA62XXCPU internal registers
		#SR ↵	Set EVA62XXCPU internal registers
		#I ↵	Reset EVA62XXCPU
		#DXY ↵	Display X, Y, MX and MY
		#SXY ↵	Set data for X and Y display and MX, MY

ICE6200 command table - 2

Item No.	Function	Command Format	Outline of Operation
11	History	#H,p1,p2 ↵	Display history data for pointer 1 and pointer 2
		#HB ↵	Display upstream history data
		#HG ↵	Display 21 line history data
		#HP ↵	Display history pointer
		#HPS,a ↵	Set history pointer
		#HC,S/C/E ↵	Sets up the history information acquisition before (S), before/after (C) and after (E)
		#HA,a1,a2 ↵	Sets up the history information acquisition from program area a1 to a2
		#HAR,a1,a2 ↵	Sets up the prohibition of the history information acquisition from program area a1 to a2
		#HAD ↵	Indicates history acquisition program area
		#HS,a ↵	Retrieves and indicates the history information which executed a program address "a"
		#HSW,a ↵ #HSR,a ↵	Retrieves and indicates the history information which wrote or read the data area address "a"
12	File	#RF,file ↵	Move program file to memory
		#RFD,file ↵	Move data file to memory
		#VF,file ↵	Compare program file and contents of memory
		#VFD,file ↵	Compare data file and contents of memory
		#WF,file ↵	Save contents of memory to program file
		#WFD,file ↵	Save contents of memory to data file
		#CL,file ↵	Load ICE6200 set condition from file
		#CS,file ↵	Save ICE6200 set condition to file
13	Coverage	#CVD ↵	Indicates coverage information
		#CVR ↵	Clears coverage information
14	ROM Access	#RP ↵	Move contents of ROM to program memory
		#VP ↵	Compare contents of ROM with contents of program memory
		#ROM ↵	Set ROM type
15	Terminate ICE	#Q ↵	Terminate ICE and return to operating system control
16	Command Display	#HELP ↵	Display ICE6200 instruction
17	Self Diagnosis	#CHK ↵	Report results of ICE6200 self diagnostic test

↵ means press the RETURN key.

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