MF761-03

EPSON

CMOS 4-BIT SINGLE CHIP MICROCOMPUTER

E0C6256 TECHNICAL MANUAL

E0C6256 Technical Hardware

E0C6256 Technical Software

ENERGY SAVING EPSON

SEIKO EPSON CORPORATION

PREFACE

This manual is individualy described about the hardware and the software of the E0C6256.

I. E0C6256 Technical Hardware

This part explains the function of the E0C6256, the circuit configurations, and details the controlling method.

II. E0C6256 Technical Software

This part explains the programming method of the principal functions of the E0C6256.

I. E0C6256 Technical Hardware

CONTENTS

Hardware

CHAPTER 1 OVERVIEW

The E0C6256 is a single-chip microcomputer made up of the 4-bit core CPU E0C6200A, ROM (6,144 words, 12 bits to a word), RAM (640 words, 4 bits to a word), A/D converter (R/f conversion type), SVD circuit, LCD driver, serial interface, watchdog timer, programmable timer and time base counter.
It can realize system to measure temperature and humidity by the internal A/D converter and externally attached parts.
Because of its low-voltage operation and low power consumption, this series is ideal for a wide range of applications, and is especially suitable for battery-driven systems.

1.1 Features

OSC1 oscillation circuit	Crystal oscillation circuit: 32.768 kHz (Typ.)		
OSC3 oscillation circuit	CR or ceramic oscillation circuit (*1): 1 MHz (Typ.)		
Instruction set	108 types		
Instruction execution time (differ depending on instruction)	During operation at 32 kHz: 153 µsec, 214 µsec, 366 µsec During operation at 1 MHz: 5 µsec, 7 µsec, 12 µsec		
ROM capacity	6,144 words × 12 bits		
RAM capacity	640 words × 4 bits		
Input port	8 bits (pull down resistors may be supplemented *1)		
Output port	8 bits (BZ, FOUT and PTOVF outputs are possible *2)		
I/O port	8 bits (4 bits are shared with serial input/output port *2)		
Serial interface	1 port (8 bits serial, synchronous type clock)		
A/D converter	R/f (resistance/frequency) conversion type, 2 channels		
LCD driver	60 segments × 5 / 4 / 3 / 2 commons (*2) LCD drive voltage: 1.05 to 1.40 V, programmable (0.05 V unit)		
Time base counter	Clock timer: 1 system 1/1000 sec stopwatch timer: 1 system		
Programmable timer	Built-in, 1 input × 8 bits, with event counter function		
Watchdog timer	Built-in (It is possible to exclude *1)		
SVD circuit (supply voltage detection)	1.05 / 1.20 / 1.35 V, programmable (for 1.5 V system, *1) 2.30 / 2.45 / 2.60 V, programmable (for 3.0 V system, *1)		
External interrupt	Input port interrupt: 2 systems		
Internal interrupt	Timer interrupt: 3 systems Serial interface interrupt: 1 system A/D converter interrupt: 1 system		
Supply voltage	0.9–3.6 V (2.2–3.6 V when OSC3 is used, 1.3–3.6 V when A/D converter is used)		
Current consumption (Typ.)	During HALT:	1.2 µA	(1.5 V, 32 kHz, normal mode)
		650 nA	(3 V, 32 kHz, halver mode)
	During operation:	3.5 µA	(1.5 V, 32 kHz, normal mode)
		2.0 µA	(3 V, 32 kHz, halver mode)
		170 µA	(3 V, 1 MHz ceramic oscillation)
		220 µA	(3 V, 1 MHz CR oscillation)
Package	QFP5-128pin / QFP5-100pin (plastic) or chip		

*1 May be selected with mask option.
*2 May be selected with software.

1.2 Block Diagram

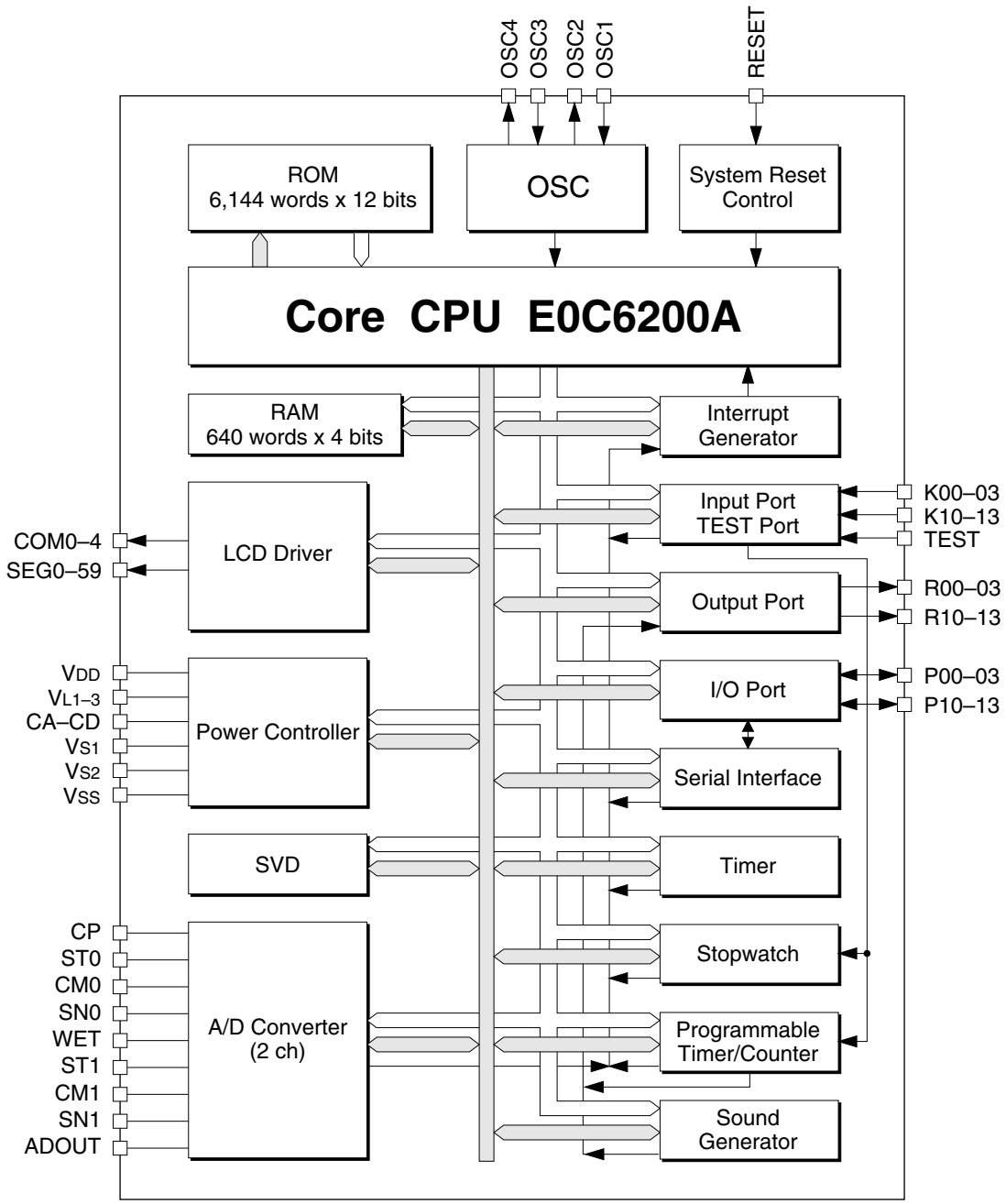
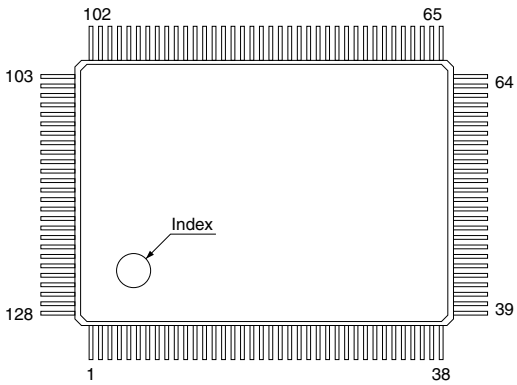


Fig. 1.2.1 Block diagram

1.3 Pin Layout Diagram

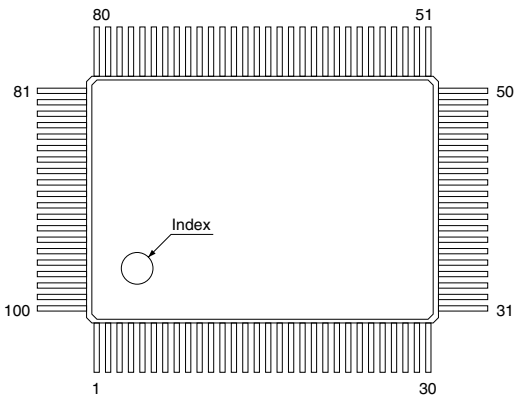
QFP5-128pin (plastic)



Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name
1	N.C.	33	OSC4	65	SEG58	97	V_{SS}
2	SEG27	34	V_{S1}	66	SEG59	98	N.C.
3	SEG28	35	SEG30	67	N.C.	99	N.C.
4	SEG29	36	SEG31	68	N.C.	100	N.C.
5	COM0	37	SEG32	69	N.C.	101	SEG0
6	COM1	38	N.C.	70	V_{DD}	102	SEG1
7	COM2	39	N.C.	71	RESET	103	SEG2
8	COM3	40	SEG33	72	TEST	104	SEG3
9	COM4	41	SEG34	73	K00	105	SEG4
10	CB	42	SEG35	74	K01	106	SEG5
11	CA	43	SEG36	75	K02	107	SEG6
12	V_{L3}	44	SEG37	76	K03	108	SEG7
13	V_{L2}	45	SEG38	77	K10	109	SEG8
14	V_{L1}	46	SEG39	78	K11	110	SEG9
15	CC	47	SEG40	79	K12	111	SEG10
16	CD	48	SEG41	80	K13	112	SEG11
17	V_{S2}	49	SEG42	81	R00	113	SEG12
18	V_{SS}	50	SEG43	82	R01	114	SEG13
19	ADOUT	51	SEG44	83	R02	115	SEG14
20	SN1	52	SEG45	84	R03	116	SEG15
21	WET	53	SEG46	85	R10	117	SEG16
22	ST1	54	SEG47	86	R11	118	SEG17
23	CM1	55	SEG48	87	R12	119	SEG18
24	SN0	56	SEG49	88	R13	120	SEG19
25	CM0	57	SEG50	89	P00	121	SEG20
26	ST0	58	SEG51	90	P01	122	SEG21
27	CP	59	SEG52	91	P02	123	SEG22
28	V_{DD}	60	SEG53	92	P03	124	SEG23
29	N.C.	61	SEG54	93	P10	125	SEG24
30	OSC1	62	SEG55	94	P11	126	SEG25
31	OSC2	63	SEG56	95	P12	127	SEG26
32	OSC3	64	SEG57	96	P13	128	N.C.

Fig. 1.3.1 Pin layout diagram (QFP5-128pin)

QFP5-100pin (plastic)



Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name
1	SEG29	26	OSC2	51	SEG59	76	P11
2	COM0	27	OSC3	52	V_{DD}	77	P12
3	COM1	28	OSC4	53	RESET	78	P13
4	COM2	29	V_{S1}	54	TEST	79	V_{SS}
5	COM3	30	SEG30	55	K00	80	SEG0
6	COM4	31	SEG31	56	K01	81	SEG1
7	CB	32	SEG32	57	K02	82	SEG2
8	CA	33	SEG34	58	K03	83	SEG4
9	V_{L3}	34	SEG36	59	K10	84	SEG6
10	V_{L2}	35	SEG38	60	K11	85	SEG8
11	V_{L1}	36	SEG40	61	K12	86	SEG10
12	CC	37	SEG41	62	K13	87	SEG12
13	CD	38	SEG42	63	R00	88	SEG13
14	V_{S2}	39	SEG43	64	R01	89	SEG14
15	ADOUT	40	SEG44	65	R02	90	SEG15
16	SN1	41	SEG45	66	R03	91	SEG16
17	WET	42	SEG46	67	R10	92	SEG17
18	ST1	43	SEG47	68	R11	93	SEG18
19	CM1	44	SEG48	69	R12	94	SEG19
20	SN0	45	SEG49	70	R13	95	SEG21
21	CM0	46	SEG51	71	P00	96	SEG23
22	ST0	47	SEG53	72	P01	97	SEG25
23	CP	48	SEG55	73	P02	98	SEG26
24	V_{DD}	49	SEG57	74	P03	99	SEG27
25	OSC1	50	SEG58	75	P10	100	SEG28

Fig. 1.3.2 Pin layout diagram (QFP5-100pin)

1.4 Pin Description

Table 1.4.1 Pin description

Pin name	Pin No.		In/ Out	Function
	QFP5-128pin	QFP5-100pin		
V_{DD}	28, 70	24, 52	(I)	Power supply pin (+)
V_{SS}	18, 97	79	(I)	Power supply pin (–)
V_{S1}	34	29	O	Oscillation and internal logic system regulated voltage output pin
V_{S2}	17	14	O	Supply voltage doubler/halver output pin
V_{L1}	14	11	O	LCD system regulated voltage output pin
V_{L2}	13	10	O	LCD system booster voltage output pin ($V_{L1} \times 2$)
V_{L3}	12	9	O	LCD system booster voltage output pin ($V_{L1} \times 3$)
CA, CB	11, 10	8, 7	–	LCD system voltage booster capacitor connecting pin
CC, CD	15, 16	12, 13	–	Supply voltage doubler/halver capacitor connecting pin
OSC1	30	25	I	Crystal oscillation input pin
OSC2	31	26	O	Crystal oscillation output pin
OSC3	32	27	I	Ceramic or CR oscillation input pin (selected by mask option)
OSC4	33	28	O	Ceramic or CR oscillation output pin (selected by mask option)
K00–K03	73–76	55–58	I	Input port pin
K10–K13	77–80	59–62	I	Input port pin
P00–P03	89–92	71–74	I/O	I/O port pin
P10–P13	93–96	75–78	I/O	I/O port pin (switching to SIN, SOUT, SCLK, SRDY pin is possible by software)
R00–R03	81–84	63–66	O	Output port pin
R10–R13	85–88	67–70	O	Output port pin (switching to BZ, PTOVF, FOUT output is possible by software)
COM0–COM4	5–9	2–6	O	LCD common output pin (1/5, 1/4, 1/3, 1/2 duty, programmable)
SEG0–SEG59*	101–127, 2–4 35–37, 40–66	80–100 1, 30–51	O	LCD segment output pin (DC output may be selected by mask option)
CP	27	23	O	A/D converter test output pin
ST0	26	22	O	A/D converter CH0 CR oscillation output pin
CM0	25	21	O	A/D converter CH0 CR oscillation output pin
SN0	24	20	I	A/D converter CH0 CR oscillation input pin
WET	21	17	O	A/D converter CH1 CR oscillation output pin
ST1	22	18	O	A/D converter CH1 CR oscillation output pin
CM1	23	19	O	A/D converter CH1 CR oscillation output pin
SN1	20	16	I	A/D converter CH1 CR oscillation input pin
ADOUT	19	15	O	A/D converter oscillation frequency output pin
RESET	71	53	I	Initial reset input pin
TEST	72	54	I	Testing input pin

* The following SEG pins are not included in the QFP5-100pin package, so they cannot be used.

  SEG3, SEG5, SEG7, SEG9, SEG11, SEG20, SEG22, SEG24, SEG33, SEG35, SEG37, SEG39, SEG50, SEG52, SEG54, SEG56

CHAPTER 2 POWER SUPPLY AND INITIAL RESET

2.1 Power Supply

The E0C6256 operating power voltage is as follows:

0.9 V to 3.6 V

Note:
- *When using a supply voltage within the range of 0.9 to 1.4 V, it is necessary to use software to control it.*
- *When using the OSC3 oscillation circuit, a supply voltage within the range of 2.2 to 3.6 V is required.*
- *When using the A/D converter, a supply voltage within the range of 1.3 to 3.6 V is required.*

The E0C6256 operates when a single power supply within the above range is applied between V_{DD} and V_{SS}. The IC itself can generate the voltage necessary for the internal circuits with the following built-in power supply circuit.

Circuit	Power supply circuit	Output voltage
Oscillation and internal circuits	Oscillation system regulated voltage circuit	V_{S1}
LCD driver	LCD system regulated voltage circuit	V_{L1}–V_{L3}
Oscillation system regulated voltage circuit, LCD system regulated voltage circuit	Supply voltage doubler/halver circuit	V_{S2}

Note:
- *External loads cannot be driven by the regulated voltage, voltage booster and voltage doubler/halver circuits' output voltages.*
- *See Chapter 7, "ELECTRICAL CHARACTERISTICS" for voltage values.*

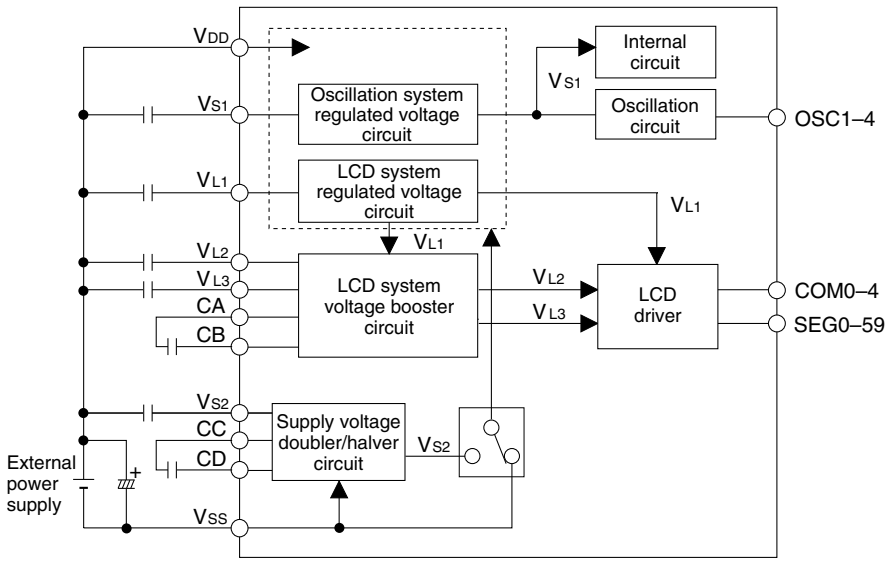


Fig. 2.1.1 Configuration of power supply

2.1.1 Supply voltage doubler/halver and operating mode

The power supply circuit has the supply voltage doubler/halver built-in. The supply voltage doubler/halver doubles or halves the voltage (V_{SS}) supplied from outside, and generates the V_{S2} voltage for the internal power supply circuits (oscillation system regulated voltage circuit and LCD system regulated voltage circuit). Anyone of the following three operating modes can be set according to the status of the supply voltage doubler/halver, and switching between them is done by the software.

(1) Doubler mode

The E0C6256 operates with 0.9 to 3.6 V supply voltage. However, a minimum 1.4 V supply voltage is needed for the internal powr supply circuit of oscillation and LCD systems. Therefore, when operating with the supply voltage within the range of 0.9 to 1.4 V, it is necessary to double the supply voltage using the supply voltage doubler/halver. Operating mode at this time is the doubler mode. The internal power supply circuit operates by the V_{S2} voltage (1.8 to 2.8 V) output from the supply voltage doubler/halver.
When the supply voltage is more than 1.4 V, do not set in this mode because doubling voltage increases current consumption.

Note: The OSC3 oscillation circuit cannot be used in this mode even when 2.2 V or more voltage is generated by doubling. Turning the OSC3 oscillation circuit ON in this mode may cause malfunction.

(2) Normal mode

In this mode, the internal power supply circuit directly operates by the supply voltage V_{SS} within the range of 1.3 to 3.6 V without the supply voltage doubler/halver. The OSC3 oscillation circuit can be used when a 2.2 V or more voltage is supplied. At initial reset, this mode is set.

(3) Halver mode

The halver mode can be set when a 2.55 to 3.6 V supply voltage is used to operate. This mode halves the supply voltage using the supply voltage doubler/halver, and operates the internal power supply circuit using its output voltage V_{S2}. Therefore, current consumption can be reduced to about half of the normal mode.

Note: The OSC3 oscillation circuit cannot be used in this mode even when 2.2 V or more voltage is generated by halving. Turning the OSC3 oscillation circuit ON in this mode may cause malfunction.

See Section 4.2, "Power Supply and Operating Mode Settings", for the control of the operating mode.

2.1.2 Voltage <V_{S1}> for oscillation circuit and internal circuits

V_{S1} is the voltage for the oscillation circuit and the internal circuits, and is generated by the oscillation system regulated voltage circuit for stabilizing the oscillation.
Making V_{DD} the standard (GND level), the oscillation system regulated voltage circuit generates V_{S1} from the supply voltage that is input from the V_{DD}–V_{SS} terminals. However, when the supply voltage doubler/halver is used, V_{S1} is generated from the voltage between the V_{DD} and V_{S2} terminals.
The E0C6256 is designed with twin clock specification; it has two types of oscillation circuits OSC1 and OSC3 built-in. Use OSC1 clock for normal operation, and switch it to OSC3 by the software when high-speed operation is necessary. When switching the clock, the operating voltage V_{S1} must be switched by the software to stabilize the operation of the oscillation circuit and internal circuits. The V_{S1} voltage must be set to -1.05 V when operating with the OSC1 clock or to -2.10 V when operating with the OSC3 clock.
See Section 4.4, "Oscillation Circuit", for the V_{S1} switching procedure.

2.1.3 Voltage <V_{L1}, V_{L2} and V_{L3}> for LCD driving

V_{L1}, V_{L2} and V_{L3} are the voltages for LCD drive, and are generated by the LCD system regulated voltage circuit and the LCD system voltage booster circuit to stabilize the display quality.
V_{L1} is generated by the LCD system regulated voltage circuit with V_{DD} as the standard from the supply voltage input from the V_{DD}–V_{SS} terminals. However, when the supply voltage doubler/halver is used, V_{L1} is generated from the voltage between the V_{DD} and V_{S2} terminals.
The V_{L1} voltage can be adjusted within the range from -1.05 to -1.40 V in unit of 0.05 V to match the LCD panel characteristics by the software. To generate V_{L1}, V_{SS} (V_{S2} when the supply voltage doubler/halver is used) voltage (V_{DD} standard) must be lower than V_{L1} - 0.2 V.

V_{SS}/V_{S2} (absolute value) ≥ V_{L1} (absolute value) + 0.2 V

See Section 4.2, "Power Supply and Operation Mode Settings", for the V_{L1} setting.
V_{L2} and V_{L3} are respectively double and triple obtained from the LCD system voltage booster circuit.

2.2 Initial Reset

To initialize the E0C6256 circuits, initial reset must be executed. There are four ways of doing this.

(1) External initial reset by the RESET terminal
(2) External initial reset by simultaneous high input to terminals K00–K03 (mask option setting)
(3) Initial reset by the oscillation detection circuit
(4) Initial reset by the watchdog timer (mask option setting)

Be sure to use reset functions (1) or (2) when turning the power on and be sure to initialize securely. In normal operation, the circuit may be initialized by any of the above four types.

Figure 2.2.1 shows the configuration of the initial reset circuit.

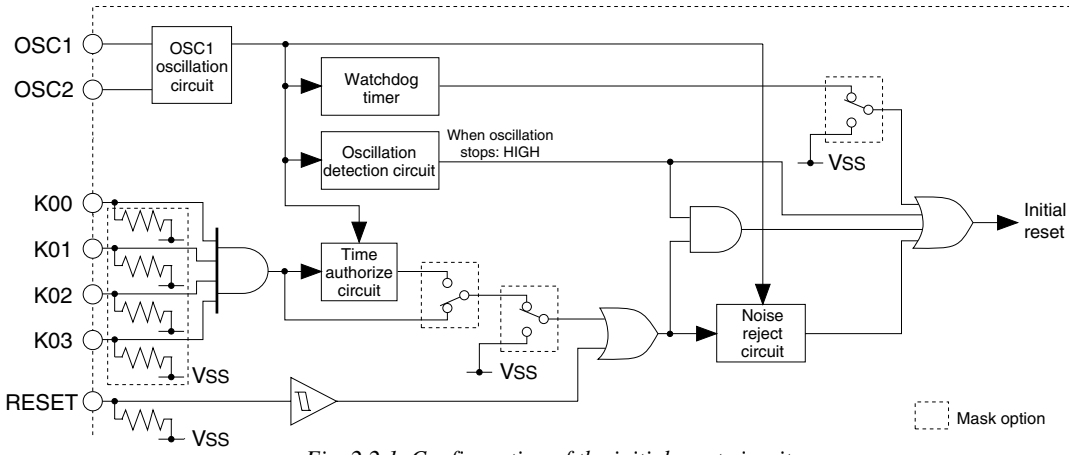


Fig. 2.2.1 Configuration of the initial reset circuit

2.2.1 Reset terminal (RESET)

Initial reset can be executed externally by setting the reset terminal to a high level. However, be sure to observe the following precautions, because the RESET signal passes through the noise reject circuit.
When the reset terminal is used for initial resetting during operation, a pulse (high level) of 0.4 msec or less is considered to be noise by the noise reject circuit. Maintain a high level of 1.5 msec (when the oscillation frequency f_{OSC1} = 32 kHz) to securely perform the initial reset. When the reset terminal goes low, the CPU begins to operate.
Since the noise reject circuit does not operate when oscillation is stopped, the noise reject circuit is bypassed until it starts oscillation. For this reason, be sure to maintain a high level the reset input in the oscillation stopped status, such as at power-on, until starting oscillation.

2.2.2 Simultaneous high input to terminals K00–K03

Another way of executing initial reset externally is to input a high signal simultaneously to the input ports (K00–K03) selected with the mask option.
Since this initial reset also passes through the same noise reject circuit as the reset terminal, you should maintain the specified input port terminal at high level for 1.5 msec (when oscillation frequency f_{OSC1} = 32 kHz) or more during operation and until it begins oscillation at times such as when turning the power on.
Table 2.2.2.1 shows the combinations of input ports (K00–K03) that can be selected with the mask option.

Table 2.2.2.1 Combinations of input ports

1	Not use
2	K00*K01*K02*K03
3	K00*K01*K02
4	K00*K01

When, for instance, mask option 2 (K00*K01*K02*K03) is selected, initial reset is executed when the signals input to the four ports K00–K03 are all high at the same time. The initial reset is done, even when a key entry including a combination of selected input ports is made.

Further, the time authorize circuit can be selected with the mask option. The time authorize circuit performs initial reset, when the input time of the simultaneous high input is authorized and found to be the same or more than the defined time (1 to 2 sec).
If you use this function, make sure that the specified ports do not go high at the same time during ordinary operation.

2.2.3 Oscillation detection circuit

The oscillation detection circuit outputs the initial reset signal at power-on until the oscillation circuit starts oscillating, or when the oscillation circuit stops oscillating for some reason.
However, this circuit may not operate properly depending on the power-on procedure. Consequently, use a simultaneous high input of the input ports (K00–K03) or reset terminal for the initial reset at power-on and you should not execute it by this function alone.

2.2.4 Watchdog timer

If the CPU runs away for some reason, the watchdog timer will detect this situation and output an initial reset signal. See Section 4.3, "Resetting Watchdog Timer", for details.
As with the oscillation detection circuit, you should not do an initial reset at power-on using this function.

2.2.5 Internal register at initial resetting

Initial reset initializes the CPU as shown in the table below.

Table 2.2.5.1 Initial values

CPU core			
Name	Symbol	Number of bits	Setting value
Program counter step	PCS	8	00H
Program counter page	PCP	4	1H
Program counter bank	PCB	1	0
New page pointer	NPP	4	1H
New bank pointer	NBP	1	0
Stack pointer	SP	8	Undefined
Index register IX	IX	11	Undefined
Index register IY	IY	11	Undefined
Register pointer	RP	4	Undefined
General-purpose register A	A	4	Undefined
General-purpose register B	B	4	Undefined
Interrupt flag	I	1	0
Decimal flag	D	1	0
Zero flag	Z	1	Undefined
Carry flag	C	1	Undefined

Peripheral circuits		
Name	Number of bits	Setting value
RAM	4	Undefined
Display memory	4	Undefined
Other peripheral circuits	—	*

* See Section 4.1, "Memory Map".

2.3 Test Terminals (TEST, CP)

These terminals are used at the time of the factory inspection of the IC. During normal operation, connect the TEST to VSS, and do not connect anything to the CP terminal.

CHAPTER 3 CPU, ROM, RAM

3.1 CPU

The E0C6256 employs the 4-bit core CPU E0C6200A for the CPU, so that register configuration, instructions and so forth are virtually identical to those in other family processors using the E0C6200A.
Refer to "E0C6200/6200A Core CPU Manual" for details about the E0C6200A.
Note the following points with regard to the E0C6256:

(1) The SLEEP operation is not assumed, so the SLP instruction cannot be used.

(2) RAM is set up to five pages, so only the three low-order bits are valid for the page portion (XP, YP) of the index register that specifies addresses. (The one high-order bit is ignored.)

3.2 ROM

The built-in ROM, a mask ROM for loading the program, has a capacity of 6,144 steps, 12 bits each. The program area is divided into two banks. Bank 0 is configured of 16 pages (0–15) with 256 steps each (00H–FFH), and bank 1 of 8 pages (0–7) with 256 steps each. After initial reset, the program beginning address is bank 0, page 1, step 00H. The interrupt vector is allocated to each page 1, steps 01H–0FH.

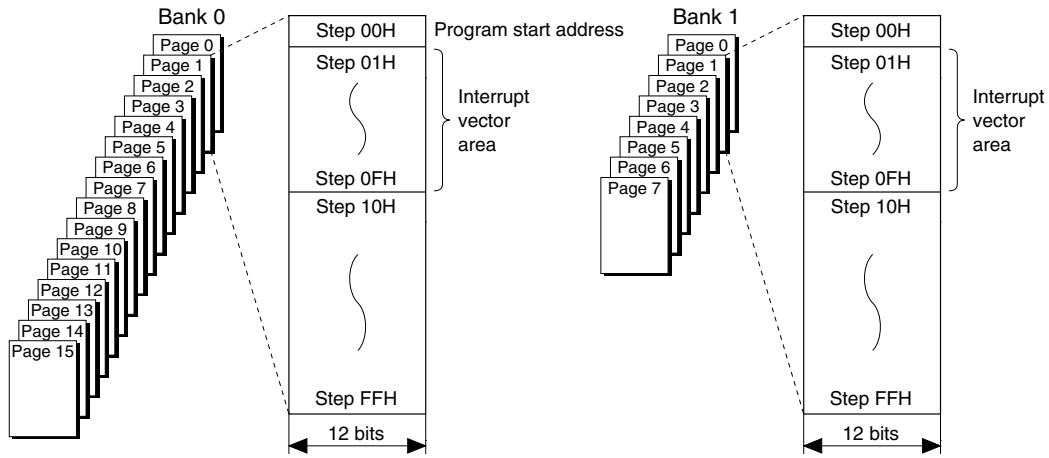


Fig. 3.2.1 ROM configuration

3.3 RAM

The RAM, a data memory storing a variety of data, has a capacity of 640 words, each of four bits. When programming, keep the following points in mind.

(1) Part of the data memory can be used as stack area when subroutine calls and saving registers, so be careful not to overlap the data area and stack area.

(2) Subroutine calls and interrupts take up three words of the stack area.

(3) The data memory 000H–00FH is for the register pointers (RP), and is the addressable memory register area.

CHAPTER 4 PERIPHERAL CIRCUITS AND OPERATION

Peripheral circuits (timer, I/O, and so on) of the E0C6256 are memory mapped, and interfaced with the CPU. Thus, all the peripheral circuits can be controlled by using the memory operation command to access the I/O memory in the memory map.
The following sections describe how the peripheral circuits operation.

4.1 Memory Map

Data memory of the E0C6256 has an address space of 795 words (715 words when the display memory is assigned in page 1), of which 80 words are allocated to display memory and 75 words to I/O memory. Figures 4.1.1(a) and (b) present the overall memory maps of the E0C6256, and Tables 4.1.1(a)–(h) the peripheral circuits' (I/O space) memory maps.
In the E0C6256 the same I/O memory has been laid out for each page 80H–FFH. As a result, the I/O memory can be accessed without changing over the data memory page. The same result is obtained for I/O memory changes and for readable/writable address references, no matter on what page it is done.

Note: • *The display memory area can be assigned to 130H–17FH or 530H–57FH by software.*

When page 1 (130H–17FH) is selected: read/write is enabled.
When page 5 (530H–57FH) is selected: write only is enabled.

If page 1 is selected, RAM (80 words) is used as the display memory area.

- *Memory is not mounted in unused area within the memory map and in memory area not indicated in this chapter. For this reason, normal operation cannot be assured for programs that have been prepared with access to these areas.*

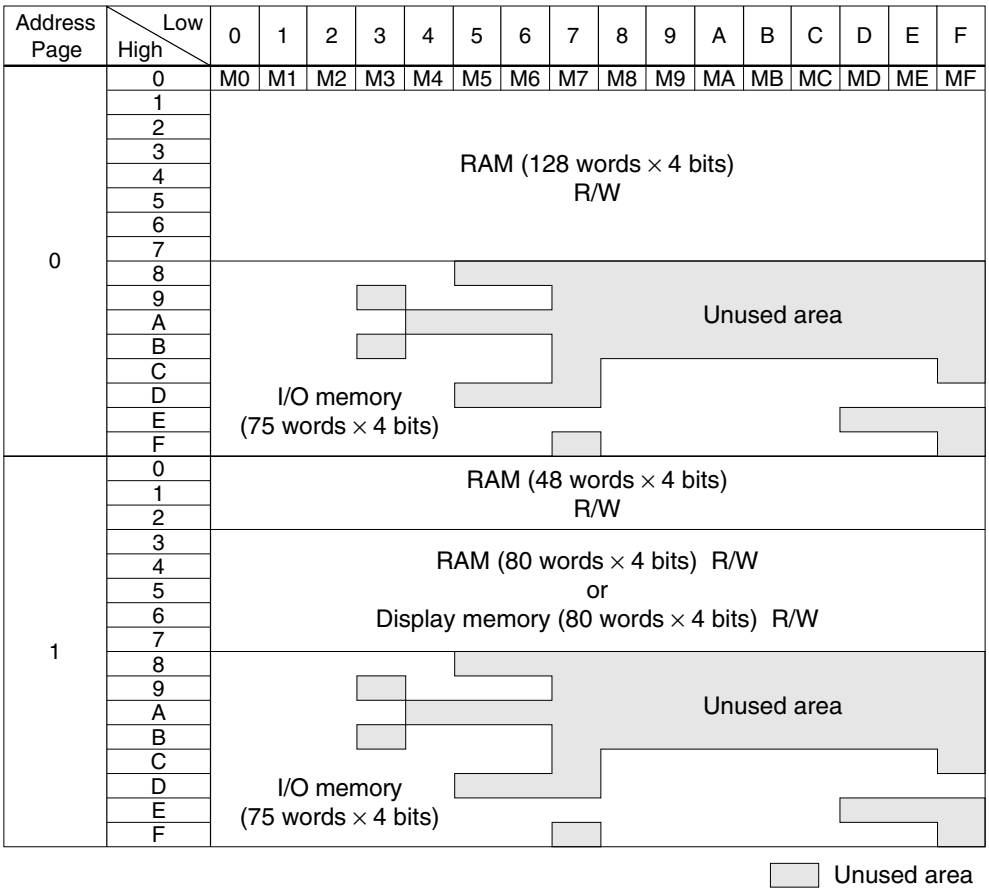


Fig. 4.1.1(a) Memory map

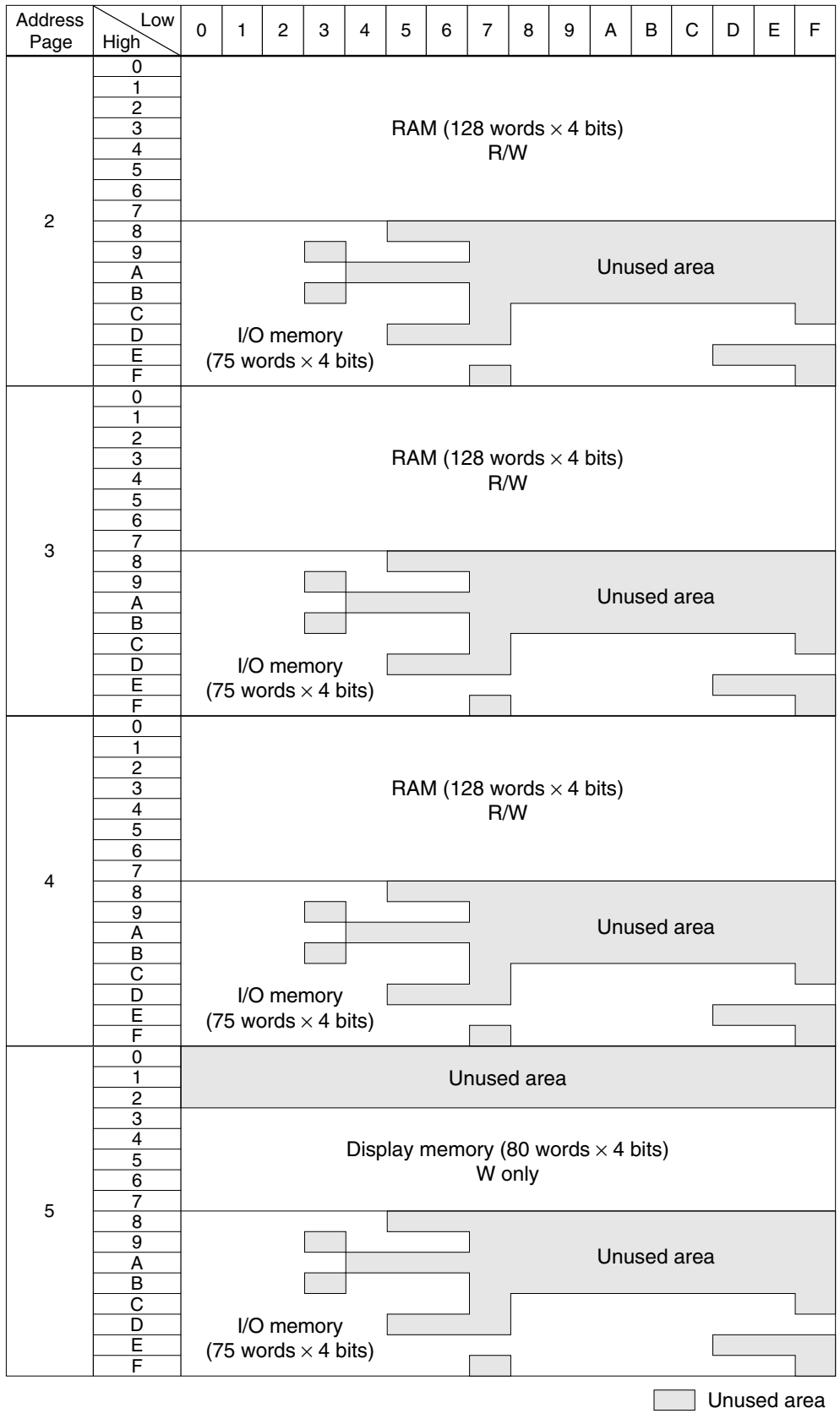


Fig. 4.1.1(b) Memory map

Table 4.1.1(a) I/O memory map (80H–84H)

Address *7	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
80H	0	0	SVDS1	SVDS0	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R		R/W		SVDS1	0			SVD criteria voltage setting (1.5 V/3.0 V)
					SVDS0	0			0: 1.05/2.30, 1: 1.20/2.45, 2 & 3: 1.35/2.60 (V)
81H	0	0	SVDDT	SVDON	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R			R/W	SVDDT	0	Low	Normal	Supply voltage detection data
					SVDON	0	On	Off	SVD circuit On/Off
82H	0	VSEL	HLON	DBON	0 *5	– *2			Unused
					VSEL	0	V_{S2}	V_{SS}	Voltage regulator power source selection
	R	R/W			HLON	0	On	Off	Halver On/Off
					DBON	0	On	Off	Doubler On/Off
83H	0	CLKCHG	OSCC	VSCHG	0 *5	– *2			Unused
					CLKCHG	0	OSC3	OSC1	CPU clock selection
	R	R/W			OSCC	0	On	Off	OSC3 oscillation On/Off
					VSCHG	0	-2.1V	-1.05V	V_{S1} output voltage change
84H	0	VLCHG2	VLCHG1	VLCHG0	0 *5	– *2			Unused
					VLCHG2	0			V_{L1} output voltage change
	R	R/W			VLCHG1	0			0: 1.05, 1: 1.10, 2: 1.15, 3: 1.20,
					VLCHG0	0			4: 1.25, 5: 1.30, 6: 1.35, 7: 1.40 (V)

Table 4.1.1(b) I/O memory map (90H–96H)

Address *7	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
90H	SIK03	SIK02	SIK01	SIK00	SIK03	0	Enable	Disable	Interrupt selection register (K03)
					SIK02	0	Enable	Disable	Interrupt selection register (K02)
	R/W				SIK01	0	Enable	Disable	Interrupt selection register (K01)
					SIK00	0	Enable	Disable	Interrupt selection register (K00)
91H	K03	K02	K01	K00	K03	– *2	High	Low	Input port (K00–K03)
					K02	– *2	High	Low	
	R				K01	– *2	High	Low	
					K00	– *2	High	Low	
92H	KCP03	KCP02	KCP01	KCP00	KCP03	0	↓	↑	Input comparison register (K00–K03)
					KCP02	0	↓	↑	
	R/W				KCP01	0	↓	↑	
					KCP00	0	↓	↑	
94H	SIK13	SIK12	SIK11	SIK10	SIK13	0	Enable	Disable	Interrupt selection register (K13)
					SIK12	0	Enable	Disable	Interrupt selection register (K12)
	R/W				SIK11	0	Enable	Disable	Interrupt selection register (K11)
					SIK10	0	Enable	Disable	Interrupt selection register (K10)
95H	K13	K12	K11	K10	K13	– *2	High	Low	Input port (K10–K13)
					K12	– *2	High	Low	
	R				K11	– *2	High	Low	
					K10	– *2	High	Low	
96H	KCP13	KCP12	KCP11	KCP10	KCP13	0	↓	↑	Input comparison register (K10–K13)
					KCP12	0	↓	↑	
	R/W				KCP11	0	↓	↑	
					KCP10	0	↓	↑	

*1 Initial value at the time of initial reset
*2 Not set in the circuit
*3 Undefined
*4 Reset (0) immediately after being read
*5 Constantly "0" when being read
*6 Refer to main manual
*7 Page switching in I/O memory is not necessary

Table 4.1.1(c) I/O memory map (A0H–A3H)

Address *7	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
A0H	0	0	0	R0HIZ	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R			R/W	0 *5	– *2			Unused
					R0HIZ	0	High-Z	Output	R0 output high-impedance control
A1H	R03	R02	R01	R00	R03	0	High	Low	Output port (R00–R03)
					R02	0	High	Low	
	R/W				R01	0	High	Low	
					R00	0	High	Low	
A2H	0	0	0	R1HIZ	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R			R/W	0 *5	– *2			Unused
					R1HIZ	0	High-Z	Output	R1 output high-impedance control
A3H	R13	R12	R11	R10	R13	0	High	Low	Output port (R13)
					R12	0	High	Low	Output port (R12)
		BZ	PTOVF	FOUT	BZ	0	Off	On	Buzzer output
	R/W				R11	0	High	Low	Output port (R11)
					PTOVF	0	Off	On	PTOVF output
					R10	0	High	Low	Output port (R10)
					FOUT	0	Off	On	FOUTоutput

Table 4.1.1(d) I/O memory map (B0H–B6H)

Address *7	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
B0H	IOC03	IOC02	IOC01	IOC00	IOC03	0	Output	Input	I/O control register (P00–P03)
					IOC02	0	Output	Input	
	R/W				IOC01	0	Output	Input	
					IOC00	0	Output	Input	
B1H	PUL03	PUL02	PUL01	PUL00	PUL03	1	On	Off	Pull down control register (P00–P03)
					PUL02	1	On	Off	
	R/W				PUL01	1	On	Off	
					PUL00	1	On	Off	
B2H	P03	P02	P01	P00	P03	– *2	High	Low	I/O port (P00–P03)
					P02	– *2	High	Low	
	R/W				P01	– *2	High	Low	
					P00	– *2	High	Low	
B4H	IOC13	IOC12	IOC11	IOC10	IOC13	0	Output	Input	I/O control register (P10–P13) (ESIF = 0)
					IOC12	0	Output	Input	
	R/W				IOC11	0	Output	Input	
					IOC10	0	Output	Input	
	When the serial I/F is used (ESIF = 1):				IOC13	0	Output	Input	Master mode: P13 I/O control register
	P10 = SIN (in), P11 = SOUT (out),				IOC13	0	1	0	Slave mode: General-purpose register
	P12 = SCLK (master: out, slave: in),				IOC12	0	1	0	General-purpose register
	P13 = SRDY (slave: out),				IOC11	0	1	0	
	P13 = I/O port (master: in/out)				IOC10	0	1	0	
B5H	PUL13	PUL12	PUL11	PUL10	PUL13	1	On	Off	Pull down control register (P10–P13) (ESIF = 0)
					PUL12	1	On	Off	
	R/W				PUL11	1	On	Off	
					PUL10	1	On	Off	
	When the serial I/F is used (ESIF = 1):				PUL13	1	On	Off	Master mode: P13 pull down control register
	P10 = SIN (in), P11 = SOUT (out),				PUL13	1	1	0	Slave mode: General-purpose register
	P12 = SCLK (master: out, slave: in),				PUL12	1	1	0	Master mode: General-purpose register
	P13 = SRDY (slave: out),				PUL12	1	On	Off	Slave mode: SCKL pull down control register
	P13 = I/O port (master: in/out)				PUL11	1	1	0	General-purpose register
					PUL10	1	On	Off	SIN pull down control register
B6H	P13	P12	P11	P10	P13	– *2	High	Low	I/O port (P10–P13) (ESIF = 0)
					P12	– *2	High	Low	
	R/W				P11	– *2	High	Low	
					P10	– *2	High	Low	
	When the serial I/F is used (ESIF = 1):				P13	– *2	High	Low	Master mode: I/O port P13
	P10 = SIN (in), P11 = SOUT (out),				P13	– *2	1	0	Slave mode: General-purpose register
	P12 = SCLK (master: out, slave: in),				P12	– *2	1	0	General-purpose register
	P13 = SRDY (slave: out),				P11	– *2	1	0	
	P13 = I/O port (master: in/out)				P10	– *2	1	0	

Table 4.1.1(e) I/O memory map (C0H–CEH)

Address *7	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
C0H	FOUTE	0	FOFQ1	FOFQ0	FOUTE	0	Enable	Disable	FOUT output enable
					0 *5	– *2			Unused
	R/W	R	R/W		FOFQ1	0			FOUT frequency selection
					FOFQ0	0			0: 512 Hz, 1: 4096 Hz, 2: $fosc_1$, 3: $fosc_3$
C1H	0	0	0	WDRST	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R			W	0 *5	– *2			Unused
					WDRST *5	Reset	Reset	–	Wachdog timer reset
C2H	LDMS	STCD	LDTY1	LDTY0	LDMS	0	1p(R/W)	5p(W)	LCD data memory area selection
					STCD	0	Static	Dynamic	LCD drive switch
	R/W				LDTY1	0			LCD drive duty selection
					LDTY0	0			0: 1/2, 1: 1/3, 2: 1/4, 3: 1/5
C3H	0	0	LOFF	LPWR	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R		R/W		LOFF	0	All Off	Normal	LCD display control
					LPWR	0	On	Off	LCD power supply On/Off
C4H	0	0	TMRUN	TMRST	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R		R/W	W	TMRUN	0	Run	Stop	Clock timer Run/Stop
					TMRST *5	Reset	Reset	–	Clock timer reset
C5H	TM3	TM2	TM1	TM0	TM3	0			Clock timer data (16 Hz)
					TM2	0			Clock timer data (32 Hz)
	R				TM1	0			Clock timer data (64 Hz)
					TM0	0			Clock timer data (128 Hz)
C6H	TM7	TM6	TM5	TM4	TM7	0			Clock timer data (1 Hz)
					TM6	0			Clock timer data (2 Hz)
	R				TM5	0			Clock timer data (4 Hz)
					TM4	0			Clock timer data (8 Hz)
C8H	0	0	PTPS1	PTPS0	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R		R/W		PTPS1	0			Prog. timer prescaler selection
					PTPS0	0			0: 1/1, 1: 1/4, 2: 1/32, 3: 1/256
C9H	0	0	PTPC1	PTPC0	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R		R/W		PTPC1	0			Prog. timer prescaler clock source selection
					PTPC0	0			0: OSC1, 1: OSC3, 2: K02, 3: K02(NR)
CAH	PNRFS	PTOE	PTRUN	PTRST	PNRFS	0	1024Hz	256Hz	Noise rejector clock frequency selection
					PTOE	0	Enable	Disable	PTOVF output enable
	R/W			W	PTRUN	0	Run	Stop	Programmable timer Run/Stop
					PTRST *5	Rst (reload)	Rst (reload)	–	Programmable timer reset (reload)
CBH	RD3	RD2	RD1	RD0	RD3	0			MSB
					RD2	0			Programmable timer reload data
	R/W				RD1	0			(low-order 4 bits)
					RD0	0			LSB
CCH	RD7	RD6	RD5	RD4	RD7	0			MSB
					RD6	0			Programmable timer reload data
	R/W				RD5	0			(high-order 4 bits)
					RD4	0			LSB
CDH	PT3	PT2	PT1	PT0	PT3	0			MSB
					PT2	0			Programmable timer data
	R				PT1	0			(low-order 4 bits)
					PT0	0			LSB
CEH	PT7	PT6	PT5	PT4	PT7	0			MSB
					PT6	0			Programmable timer data
	R				PT5	0			(high-order 4 bits)
					PT4	0			LSB

Table 4.1.1(f) I/O memory map (D0H–DFH)

Address *7	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
D0H	EDIR	DKM2	DKM1	DKM0	EDIR	0	Enable	Disable	Enable direct input function
					DKM2	0			Direct key mask factor 0: Non, 1: K02,
	R/W				DKM1	0			2: K02-03, 3: K02-03-10, 4: K10, 5: K10-11,
					DKM0	0			6: K10-11-12, 7: K10-11-12-13
D1H	LCURF	CRNWF	SWRUN	SWRST	LCURF	0	Reqest	No	Lap data carry-up request flag
					CRNWF	0	Renewal	No	Capture renewal flag
	R		R/W	W	SWRUN	0	Run	Stop	Stopwatch timer Run/Stop
					SWRST *5	Reset	Reset	–	Stopwatch timer reset
D2H	SWL3	SWL2	SWL1	SWL0	SWL3	0			MSB
					SWL2	0			Stopwatch timer data 1/1000 sec (BCD)
	R				SWL1	0			
					SWL0	0			LSB
D3H	SWM3	SWM2	SWM1	SWM0	SWM3	0			MSB
					SWM2	0			Stopwatch timer data 1/100 sec (BCD)
	R				SWM1	0			
					SWM0	0			LSB
D4H	SWH3	SWH2	SWH1	SWH0	SWH3	0			MSB
					SWH2	0			Stopwatch timer data 1/10 sec (BCD)
	R				SWH1	0			
					SWH0	0			LSB
D8H	0	0	SCTRG	ESIF	0 *5	– *2			Unused
					0 *5	– *2			Unused
					SCTRG(W)	– *2	Trigger	–	Serial interface clock trigger (writing)
	R		R/W		SCTRG(R)	0	Run	Stop	Serial interface clock status (reading)
					ESIF	0	SIF port	I/O port	P1 port function selection
D9H	SDP	SCPS	SCS1	SCS0	SDP	0	LSB first	MSB first	Serial data input/output permutation
					SCPS	0	↑	↓	Serial interface clock phase selection
	R/W				SCS1	0			Serial interface clock mode selection
					SCS0	0			0: Slave, 1: PTOVF, 2: CLK/2, 3: CLK
DAH	SD3	SD2	SD1	SD0	SD3	– *3			MSB
					SD2	– *3			Serial interface data (low-order 4 bits)
	R/W				SD1	– *3			
					SD0	– *3			LSB
DBH	SD7	SD6	SD5	SD4	SD7	– *3			MSB
					SD6	– *3			Serial interface data (high-order 4 bits)
	R/W				SD5	– *3			
					SD4	– *3			LSB
DCH	ENRTM	ENRST	ENON	BZE	ENRTM	0	1sec	0.5sec	Envelope releasing time
					ENRST *5	Reset	Reset	–	Envelope reset
	R/W	W	R/W		ENON	0	On	Off	Envelope On/Off
					BZE	0	Enable	Disable	Buzzer output enable
DDH	0	BZSTP	BZSHT	SHTPW	0 *5	– *2			Unused
					BZSTP *5	– *2	Stop	–	1-shot buzzer stop
					BZSHT(W)	– *2	Trigger	–	1-shot buzzer trigger (writing)
	R	W	R/W		BZSHT(R)	0	Busy	Ready	1-shot buzzer status (reading)
					SHTPW	0	125msec	31.25msec	1-shot buzzer pulse width setting
DEH	0	BZFQ2	BZFQ1	BZFQ0	0 *5	– *2			Unused
					BZFQ2	0			Buzzer frequency selection
	R	R/W			BZFQ1	0			0: 4096.0, 1: 3276.8, 2: 2730.7, 3: 2340.6,
					BZFQ0	0			4: 2048.0, 5: 1638.4, 6: 1365.3, 7: 1170.3 (Hz)
DFH	0	BDTY2	BDTY1	BDTY0	0 *5	– *2			Unused
					BDTY2	0			Buzzer signal duty ratio selection *6
	R	R/W			BDTY1	0			
					BDTY0	0			

Table 4.1.1(g) I/O memory map (E0H–ECH)

Address *7	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
E0H	0	APWR	SENSEL	ADMODE	0 *5	– *2			Unused
					APWR	0	On	Off	A/D converter power supply On/Off
	R	R/W			SENSEL	0	Sensor	Reference	Sensor/reference resistance selection
					ADMODE	0	Continuous	Normal	A/D converter operation mode selection
E1H	WRSEL	0	ADCLK1	ADCLK0	WRSEL	0	Humidity	Resistance	CH1 sensor selection (resistance/humidity)
					0 *5	– *2			Unused
	R/W	R	R/W		ADCLK1	0	OSC3	OSC1	CH1 clock selection
					ADCLK0	0	OSC3	OSC1	CH0 clock selection
E2H	0	0	0	CHSEL	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R			R/W	0 *5	– *2			Unused
					CHSEL	0	CH1	CH0	Channel 1/0 selection
E3H	TC3	TC2	TC1	TC0	TC3	– *3			Up/down counter data (TC0–TC3)
					TC2	– *3			
	R/W				TC1	– *3			
					TC0	– *3			LSB
E4H	TC7	TC6	TC5	TC4	TC7	– *3			Up/down counter data (TC4–TC7)
					TC6	– *3			
	R/W				TC5	– *3			
					TC4	– *3			
E5H	TC11	TC10	TC9	TC8	TC11	– *3			Up/down counter data (TC8–TC11)
					TC10	– *3			
	R/W				TC9	– *3			
					TC8	– *3			
E6H	TC15	TC14	TC13	TC12	TC15	– *3			MSB
					TC14	– *3			Up/down counter data (TC12–TC15)
	R/W				TC13	– *3			
					TC12	– *3			
E7H	C3	C2	C1	C0	C3	– *3			Up-counter data (C0–C3)
					C2	– *3			
	R/W				C1	– *3			
					C0	– *3			LSB
E8H	C7	C6	C5	C4	C7	– *3			Up-counter data (C4–C7)
					C6	– *3			
	R/W				C5	– *3			
					C4	– *3			
E9H	C11	C10	C9	C8	C11	– *3			Up-counter data (C8–C11)
					C10	– *3			
	R/W				C9	– *3			
					C8	– *3			
EAH	C15	C14	C13	C12	C15	– *3			Up-counter data (C12–C15)
					C14	– *3			
	R/W				C13	– *3			
					C12	– *3			
EBH	C19	C18	C17	C16	C19	– *3			MSB
					C18	– *3			Up-counter data (C16–C19)
	R/W				C17	– *3			
					C16	– *3			
ECH	0	OVF2	OVF1	ADRUN	0 *5	– *2			Unused
					OVF2(R)	0	Yes	No	Up/down counter overflow flag
					OVF2(W)	Reset	Reset	–	Up/down counter overflow flag reset
	R	R/W			OVF1(R)	0	Yes	No	Up-counter overflow flag
					OVF1(W)	Reset	Reset	–	Up-counter overflow flag reset
					ADRUN	0	Start	Stop	A/D conversion Start/Stop

Table 4.1.1(h) I/O memory map (F0H–FEH)

Address *7	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
F0H	0	0	0	EIAD	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R			R/W	0 *5	– *2			Unused
					EIAD	0	Enable	Mask	Interrupt mask register (A/D converter)
F1H	0	0	0	EIK1	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R			R/W	0 *5	– *2			Unused
					EIK1	0	Enable	Mask	Interrupt mask register (K10–K13)
F2H	0	0	0	EIK0	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R			R/W	0 *5	– *2			Unused
					EIK0	0	Enable	Mask	Interrupt mask register (K00–K03)
F3H	0	0	0	EISIF	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R			R/W	0 *5	– *2			Unused
					EISIF	0	Enable	Mask	Interrupt mask register (Serial interface)
F4H	0	0	0	EIPT	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R			R/W	0 *5	– *2			Unused
					EIPT	0	Enable	Mask	Interrupt mask register (Programmable timer)
F5H	EIRUN	EILAP	EISW1	EISW0	EIRUN	0	Enable	Mask	Interrupt mask register (Stopwatch direct RUN)
					EILAP	0	Enable	Mask	Interrupt mask register (Stopwatch direct LAP)
	R/W				EISW1	0	Enable	Mask	Interrupt mask register (Stopwatch 1 Hz)
					EISW0	0	Enable	Mask	Interrupt mask register (Stopwatch 10 Hz)
F6H	EIT3	EIT2	EIT1	EIT0	EIT3	0	Enable	Mask	Interrupt mask register (Clock timer 2 Hz)
					EIT2	0	Enable	Mask	Interrupt mask register (Clock timer 8 Hz)
	R/W				EIT1	0	Enable	Mask	Interrupt mask register (Clock timer 16 Hz)
					EIT0	0	Enable	Mask	Interrupt mask register (Clock timer 32 Hz)
F8H	0	0	0	IAD	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R				0 *5	– *2			Unused
					IAD *4	0	Yes	No	Interrupt factor flag (A/D converter)
F9H	0	0	0	IK1	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R				0 *5	– *2			Unused
					IK1 *4	0	Yes	No	Interrupt factor flag (K10–K13)
FAH	0	0	0	IK0	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R				0 *5	– *2			Unused
					IK0 *4	0	Yes	No	Interrupt factor flag (K00–K03)
FBH	0	0	0	ISIF	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R				0 *5	– *2			Unused
					ISIF *4	0	Yes	No	Interrupt factor flag (Serial interface)
FCH	0	0	0	IPT	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R				0 *5	– *2			Unused
					IPT *4	0	Yes	No	Interrupt factor flag (Programmable timer)
FDH	IRUN	ILAP	ISW1	ISW0	IRUN *4	0	Yes	No	Interrupt factor flag (Stopwatch direct RUN)
					ILAP *4	0	Yes	No	Interrupt factor flag (Stopwatch direct LAP)
	R				ISW1 *4	0	Yes	No	Interrupt factor flag (Stopwatch 1 Hz)
					ISW0 *4	0	Yes	No	Interrupt factor flag (Stopwatch 10 Hz)
FEH	IT3	IT2	IT1	IT0	IT3 *4	0	Yes	No	Interrupt factor flag (Clock timer 2 Hz)
					IT2 *4	0	Yes	No	Interrupt factor flag (Clock timer 8 Hz)
	R				IT1 *4	0	Yes	No	Interrupt factor flag (Clock timer 16 Hz)
					IT0 *4	0	Yes	No	Interrupt factor flag (Clock timer 32 Hz)

4.2 Power Supply and Operating Mode Settings

This section explains the control of the operating mode and the LCD drive voltage. See Section 2.1, "Power Supply", for the configuration of the power supply circuit.

4.2.1 Operating mode

As explained in Section 2.1, "Power Supply", the supply voltage doubler/halver and the operating modes are set in the E0C6256 to deal with a wide supply voltage range (0.9 to 3.6 V).

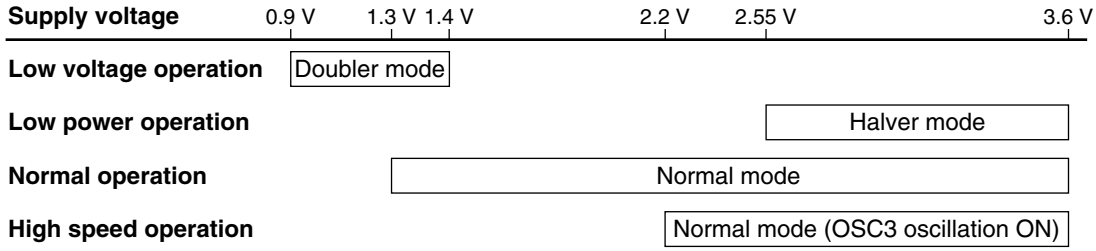


Fig. 4.2.1.1 Corresponding between supply voltage and operating mode

The operating mode can be set by the registers VSEL, HLON and DBON.

Table 4.2.1.1 Operating mode setting

VSEL	HLON	DBON	Operating mode	Supply voltage
0	0	0	Normal mode	1.3 V to 3.6 V
1	1	0	Halver mode	2.55 V to 3.6 V
1	0	1	Doubler mode	0.9 V to 1.4 V
1	0	0	Cannot be used	
×	1	1	Cannot be used	

The HLON register and the DBON registers are used to turn halving and doubling ON or OFF, respectively. By turning either one ON, the supply voltage doubler/halver circuit generates V_{S2}.
The VSEL register is used to select the drive voltage for the internal power supply circuit (oscillation system regulated voltage circuit, LCD system regulated voltage circuit). When it is set to "0", V_{SS} is used as the drive voltage, and when it is set to "1", V_{S2} output from the supply voltage doubler/halver circuit is used.
After turning the supply voltage doubler/halver ON using the HLON or DBON, about 100 msec is necessary until the V_{S2} voltage stabilizes. Therefore, switching of the operating mode should be done in the following sequence.

Normal mode → Halver/Doubler mode

1. Turn the supply voltage doubler/halver ON (Set HLON or DBON to "1")
2. Maintain 100 msec or more
3. Set VSEL to "1"

Halver/Doubler mode → Normal mode

1. Set VSEL to "0"
2. Turn the supply voltage doubler/halver OFF (Set HLON or DBON to "0")

Note:
- *When the supply voltage is out of the specified voltage range of an operating mode, do not switch into the operating mode. It may cause malfunction or increase current consumption.*
- *Do not set HLON and DBON to "1" at the same time.*
- *When switching from the doubler/halver mode to the normal mode, use separate instructions to switch the mode (VSEL = "0") and turn the supply voltage doubler/halver OFF (HLON = "0" or DBON = "0"). Simultaneous processing with a single instruction may cause malfunction.*

4.2.2 LCD drive voltage

The LCD drive voltage V_{L1} is generated by the LCD system regulated voltage circuit, and V_{L2} and V_{L3} are also internally generated by boosting the V_{L1} voltage.
The V_{L1} voltage can be adjusted to match the LCD panel characteristics using the registers VLCHG0–VLCHG2. To generate V_{L1}, V_{SS} (V_{S2} when the supply voltage doubler/halver is used) voltage (V_{DD} standard) must be lower than V_{L1} - 0.2 V.

$$V_{SS}/V_{S2} \text{ (absolute value)} \geq V_{L1} \text{ (absolute value)} + 0.2 \text{ V}$$

Table 4.2.2.1 V_{L1} setting

VLCHG2	VLCHG1	VLCHG0	V_{L1} voltage	V_{SS}/V_{S2} voltage range
0	0	0	-1.05 V	-1.25 V to -3.6 V
0	0	1	-1.10 V	-1.30 V to -3.6 V
0	1	0	-1.15 V	-1.35 V to -3.6 V
0	1	1	-1.20 V	-1.40 V to -3.6 V
1	0	0	-1.25 V	-1.45 V to -3.6 V
1	0	1	-1.30 V	-1.50 V to -3.6 V
1	1	0	-1.35 V	-1.55 V to -3.6 V
1	1	1	-1.40 V	-1.60 V to -3.6 V

(Voltage value: V_{DD} reference)

4.2.3 Control of power supply and operating mode

Table 4.2.3.1 lists the power supply and the operating mode control bits and their addresses.

Table 4.2.3.1 Control bits of power supply and operating mode

Address *7	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
82H	0	VSEL	HLON	DBON	0 *5	– *2			Unused
					VSEL	0	V_{S2}	V_{SS}	Voltage regulator power source selection
	R	R/W			HLON	0	On	Off	Halver On/Off
					DBON	0	On	Off	Doubler On/Off
84H	0	VLCHG2	VLCHG1	VLCHG0	0 *5	– *2			Unused
					VLCHG2	0			V_{L1} output voltage change
	R	R/W			VLCHG1	0			0: 1.05, 1: 1.10, 2: 1.15, 3: 1.20,
					VLCHG0	0			4: 1.25, 5: 1.30, 6: 1.35, 7: 1.40 (V)

*1 Initial value at the time of initial reset
*2 Not set in the circuit
*3 Undefined
*4 Reset (0) immediately after being read
*5 Constantly "0" when being read
*6 Refer to main manual
*7 Page switching in I/O memory is not necessary

DBON: Doubler ON/OFF (82H•D0)

Controls doubling ON/OFF for the supply voltage doubler/halver.

When "1" is written: Doubler ON
When "0" is written: Doubler OFF
Reading: Valid

When supply voltage is in a range of 0.9 to 1.4 V, generate V_{S2} by doubling the supply voltage to drive the internal power supply circuit. When "1" is written to DBON, the supply voltage doubler/halver circuit generates V_{S2} doubling with supply voltage. When "0" is written, V_{S2} will be the same voltage as V_{SS}.
When supply voltage is 1.4 V or more, do not double the supply voltage.
At initial reset, this register is set to "0".

HLON: Halver ON/OFF (82H•D1)

Controls halves ON/OFF for the supply voltage doubler/halver.

When "1" is written: Halver ON
When "0" is written: Halver OFF
Reading: Valid

When supply voltage is in a range of 2.55 to 3.6 V, the internal power supply circuit can be driven by the halved voltage to reduce current consumption. When "1" is written to HLON, the supply voltage doubler/halver circuit generates V_{S2} halving with supply voltage. When "0" is written, V_{S2} will be the same voltage as V_{SS}.
When supply voltage is 2.55 V or less, or when the OSC3 clock is used, do not halve the supply voltage.
At initial reset, this register is set to "0".

VSEL: Voltage regulator power source selection (82H•D2)
Selects the power source for two internal power supply circuit (oscillation system regulated voltage circuit and LCD system regulated voltage circuit).

When "1" is written: V_{S2}
When "0" is written: V_{SS}
Reading: Valid

When "1" is written to VSEL, the internal power supply circuit operates with V_{S2} output from the supply voltage doubler/halver circuit. It becomes the doubler mode or the halver mode according to the DBON and HLON settings. When "0" is written to VSEL, the internal power supply circuit operates with V_{SS} and it becomes the normal mode.
When switching from the normal mode to the doubler/halver mode,VSEL should be set to "1" wait 100 msec or more for the V_{S2} to stabilize after setting DBON or HLON to "1".
At initial reset, this register is set to "0".

VLCHG0–VLCHG2: VL1 output voltage change (84H•D0–D2)
The voltage value of the LCD drive voltage V_{L1} can be selected from among 8 types as shown in Table 4.2.2.1.
At initial reset, these registers are set to "0".

4.2.4 Programming notes

(1) When the supply voltage is out of the specified voltage range of an operating mode, do not switch into the operating mode. It may cause malfunction or increase current consumption.

(2) Do not set HLON (halving) and DBON (doubling) to "1" at the same time.

(3) When switching from the normal mode to the doubler/halver mode, VSEL should be set to "1" wait 100 msec or more for the V_{S2} to stabilize after setting DBON or HLON to "1".

(4) When switching from the doubler/halver mode to the normal mode, use separate instructions to switch the mode (VSEL = "0") and turn the supply voltage doubler/halver OFF (HLON = "0" or DBON = "0"). Simultaneous processing with a single instruction may cause malfunction.

4.3 Resetting Watchdog Timer

4.3.1 Configuration of watchdog timer

The E0C6256 incorporates a watchdog timer as the source oscillator for OSC1 (dividing clock = 256 Hz). The watchdog timer must be reset cyclically by the software. If reset is not executed in at least 3 or 4 seconds, the initial reset signal is output automatically for the CPU.
Figure 4.3.1.1 is the block diagram of the watchdog timer.

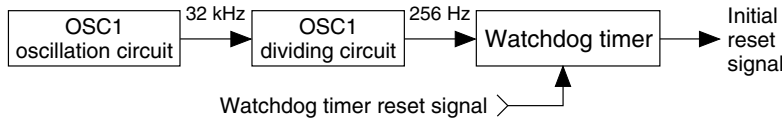


Fig. 4.3.1.1 Watchdog timer block diagram

The watchdog timer, configured of a 10-bit binary counter, generates the initial reset signal internally by overflow of the last stage (1/4 Hz).
Watchdog timer reset processing in the program's main routine enables detection of program overrun, such as when the main routine's watchdog timer processing is bypassed. Ordinarily this routine is incorporated where periodic processing takes place, just as for the timer interrupt routine.
The watchdog timer operates in the HALT mode. If the HALT status continues for 3 or 4 seconds, the initial reset signal restarts operation.

4.3.2 Mask option

You can select whether or not to use the watchdog timer with the mask option. When "Not use" is selected, there is no need to reset the watchdog timer.

4.3.3 Control of watchdog timer

Table 4.3.3.1 lists the watchdog timer's control bit and its address.

Table 4.3.3.1 Control bit of watchdog timer

Address *7	Register								Comment
	D3	D2	D1	D0	Name	Init *1	1	0	
C1H	0	0	0	WDRST	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R			W	0 *5	– *2			Unused
					WDRST *5	Reset	Reset	–	Wachdog timer reset

*1 Initial value at the time of initial reset
*2 Not set in the circuit
*3 Undefined
*4 Reset (0) immediately after being read
*5 Constantly "0" when being read
*6 Refer to main manual
*7 Page switching in I/O memory is not necessary

WDRST: Watchdog timer reset (C1H•D0)
This is the bit for resetting the watchdog timer.

When "1" is written: Watchdog timer is reset
When "0" is written: No operation
Reading: Always "0"

When "1" is written to WDRST, the watchdog timer is reset, and the operation restarts immediately after this. When "0" is written to WDRST, no operation results.
This bit is dedicated for writing, and is always "0" for reading.

4.3.4 Programming note

When the watchdog timer is being used, the software must reset it within 3-second cycles.

4.4 Oscillation Circuit

4.4.1 Configuration of oscillation circuit

The E0C6256 has two oscillation circuits (OSC1 and OSC3). OSC1 is a crystal oscillation circuit that supplies the operating clock to the CPU and peripheral circuits. OSC3 is either a CR or ceramic oscillation circuit. When processing with the E0C6256 requires high-speed operation, the CPU operating clock can be switched from OSC1 to OSC3. When the OSC3 clock is used, to obtain stable operation, the operating voltage V_{S1} of the internal circuit is changed by the software.
Figure 4.4.1.1 is the block diagram of this oscillation system.

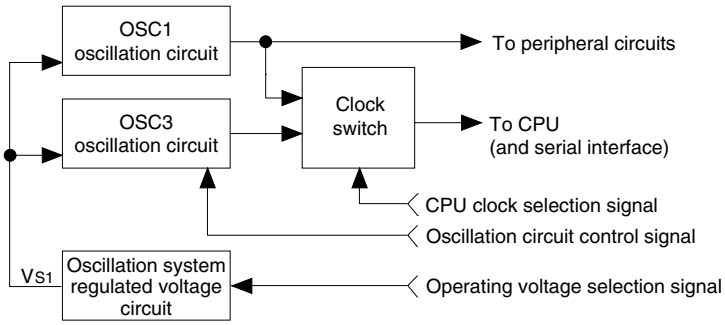


Fig. 4.4.1.1 Oscillation system

Selection of either OSC1 or OSC3 for the CPU's operating clock can be made by the software.

4.4.2 OSC1 oscillation circuit

The E0C6256 has a built-in crystal oscillation circuit (OSC1 oscillation circuit). As an external element, the OSC1 oscillation circuit generates the operating clock for the CPU and peripheral circuits by connecting the crystal oscillator (Typ. 32.768 kHz) and trimmer capacitor (5–25 pF).
Figure 4.4.2.1 is the block diagram of the OSC1 oscillation circuit.

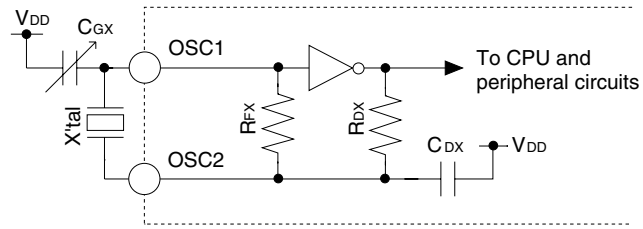
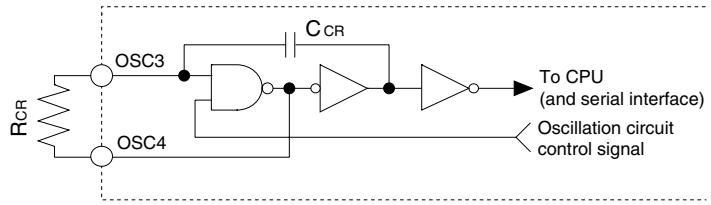


Fig. 4.4.2.1 OSC1 oscillation circuit

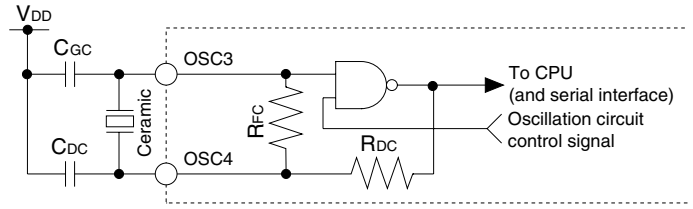
As Figure 4.4.2.1 indicates, the crystal oscillation circuit can be configured simply by connecting the crystal oscillator (X'tal) between terminals OSC1 and OSC2 to the trimmer capacitor (C_{GX}) between terminals OSC1 and V_{DD}.

4.4.3 OSC3 oscillation circuit

The E0C6256 has twin clock specification. The mask option enables selection of either the CR or ceramic oscillation circuit (OSC3 oscillation circuit) as the CPU's sub-clock. Because the oscillation circuit itself is built-in, it provides the resistance as an external element when CR oscillation is selected, but when ceramic oscillation is selected both the ceramic oscillator and two capacitors (gate and drain capacitance) are required.
Figure 4.4.3.1 is the block diagram of the OSC3 oscillation circuit.



(a) CR oscillation circuit



(b) Ceramic oscillation circuit

Fig. 4.4.3.1 OSC3 oscillation circuit

As indicated in Figure 4.4.3.1, the CR oscillation circuit can be configured simply by connecting the resistor (R_{CR}) between terminals OSC3 and OSC4 when CR oscillation is selected. When 40 kΩ is used for R_{CR}, the oscillation frequency is about 900 kHz. When ceramic oscillation is selected, the ceramic oscillation circuit can be configured by connecting the ceramic oscillator (Typ. 1 MHz) between terminals OSC3 and OSC4 to the two capacitors (C_{GC} and C_{DC}) located between terminals OSC3 and OSC4 and V_{DD}. For both C_{GC} and C_{DC}, connect capacitors that are about 100 pF. To lower current consumption of the OSC3 oscillation circuit, stop the oscillation by the software when it is not used.

4.4.4 Operating voltage switching

When switching the CPU system clock between OSC1 and OSC3 by the software, the operating voltage V_{S1} for the oscillation circuit must also be switched by the software to obtain stable operation.
System clock and the corresponding operating voltage V_{S1} are shown in Table 4.4.4.1.

Table 4.4.4.1 System clock and operating voltage

System clock	Operating voltage V_{S1}
OSC1 (32.768 kHz)	-1.05 V
OSC3 (1 MHz)	-2.1 V

(Operating voltage value: V_{DD} reference)

When using OSC3 as the CPU system clock, it should be done using the software as in the following procedure: first switch the operating voltage V_{S1} to -2.1 V, turn the OSC3 oscillation ON, then after waiting 5 msec or more switch the clock for oscillation stabilization. When switching from OSC3 to OSC1, turn the OSC3 oscillation circuit OFF after switching the clock, then set the operating voltage V_{S1} to -1.05 V.

Note: Switching the operating voltage when the supply voltage is lower than 2.2 V (absolute value) may cause a malfunction. Switch the operating voltage only after making sure that supply voltage is more than 2.2 V (absolute value) using the SVD circuit.
Do not switch the operating voltage during operating in the doubler mode or the halver mode, even if the V_{S2} voltage is more than 2.2 V (absolute value). The OSC3 clock can be used only in the normal mode.

4.4.5 Clock frequency and instruction execution time

Table 4.4.5.1 shows the instruction execution time according to each frequency of the system clock.

Table 4.4.5.1 Clock frequency and instruction execution time

Clock frequency	Instruction execution time (µsec)		
	5-clock instruction	7-clock instruction	12-clock instruction
OSC1: 32.768 kHz	152.6	213.6	366.2
OSC3: 1 MHz	5.0	7.0	12.0

4.4.6 Control of oscillation circuit

Table 4.4.6.1 lists the control bits and their addresses for the oscillation circuit.

Table 4.4.6.1 Control bits of oscillation circuit

Address *7	Register								Comment
	D3	D2	D1	D0	Name	Init *1	1	0	
83H	0	CLKCHG	OSCC	VSCHG	0 *5	– *2			Unused
					CLKCHG	0	OSC3	OSC1	CPU clock selection
	R	R/W			OSCC	0	On	Off	OSC3 oscillation On/Off
					VSCHG	0	-2.1V	-1.05V	VS1 output voltage change

*1 Initial value at the time of initial reset
*2 Not set in the circuit
*3 Undefined
*4 Reset (0) immediately after being read
*5 Constantly "0" when being read
*6 Refer to main manual
*7 Page switching in I/O memory is not necessary

VSCHG: VS1 output voltage change (83H•D0)

Switches the operating voltage VS1.

When "1" is written: -2.1 V
When "0" is written: -1.05 V
Reading: Valid

When switching the CPU system clock, the operating voltage VS1 should also be switched according to the clock.
When switching from OSC1 to OSC3, first set VS1 to -2.1 V (VSCHG = "1"), then turn the OSC3 oscillation ON.
When switching from OSC3 to OSC1, set VS1 to -1.05 V (VSCHG = "0") after switching to OSC1 and turning the OSC3 oscillation OFF.
At initial reset, this register is set to "0".

OSCC: OSC3 oscillation ON/OFF (83H•D1)

Controls oscillation ON/OFF for the OSC3 oscillation circuit.

When "1" is written: OSC3 oscillation ON
When "0" is written: OSC3 oscillation OFF
Reading: Valid

When it is necessary to operate the CPU at high speed, set OSCC to "1". At other times, set it to "0" to resume current consumption. Furthermore, when performing this setting, it is necessary to switch the operating voltage VS1.
At initial reset, this register is set to "0".

CLKCHG: CPU clock switch (83H•D2)

The CPU's operation clock is selected with this register.

When "1" is written: OSC3 clock is selected
When "0" is written: OSC1 clock is selected
Reading: Valid

When the CPU clock is to be OSC3, set CLKCHG to "1"; for OSC1, set CLKCHG to "0".
When switching the CPU operation clock from OSC1 to OSC3, do this after a minimum of 5 msec have elapsed since the OSC3 oscillation went ON (OSCC = "1"). This time is necessary to stabilize the OSC3 oscillation.
At initial reset, this register is set to "0".

4.4.7 Programming notes

(1) When switching the CPU system clock from OSC1 to OSC3, set V_{S1} to -2.1 V (VSCHG = "1") before turning the OSC3 oscillation ON.
When switching from OSC3 to OSC1, set V_{S1} to -1.05 V (VSCHG = "0") after switching to OSC1 and turning the OSC3 oscillation OFF.

(2) It takes at least 5 msec from the time the OSC3 oscillation circuit goes ON until the oscillation stabilizes. Consequently, when switching the CPU operation clock from OSC1 to OSC3, do this after a minimum of 5 msec have elapsed since the OSC3 oscillation went ON.
Further, the oscillation stabilization time varies depending on the external oscillator characteristics and conditions of use, so allow ample margin when setting the wait time.

OSC1 → OSC3

1. Set VSCHG to "1" (-1.05 V → -2.1 V)
2. Set OSCC to "1" (OSC3 oscillation ON)
3. Maintain 5 msec or more
4. Set CLKCHG to "1" (OSC1 → OSC3)

OSC3 → OSC1

1. Set CLKCHG to "0" (OSC3 → OSC1)
2. Set OSCC to "0" (OSC3 oscillation OFF)
3. Set VSCHG to "0" (-2.1 V → -1.05 V)

(3) When switching the clock form OSC3 to OSC1, use a separate instruction for turning the OSC3 oscillation OFF. An error in the CPU operation can result if this processing is performed at the same time by the one instruction.

(4) Switching the operating voltage when the supply voltage is lower than 2.2 V (absolute value) may cause a malfunction. Switch the operating voltage only after making sure that supply voltage is more than 2.2 V (absolute value) using the SVD circuit.
Do not switch the operating voltage during operating in the doubler mode or the halver mode, even if the V_{S2} voltage is more than 2.2 V (absolute value). The OSC3 clock can be used only in the normal mode.

4.5 Input Ports (K00–K03, K10–K13)

4.5.1 Configuration of input ports

The E0C6256 has 8 bits (4-bit × 2) general-purpose input ports. Each of the input port terminals (K00–K03, K10–K13) provides internal pull down resistor. Pull down resistor can be selected for each bit with the mask option.
Figure 4.5.1.1 shows the configuration of input port.

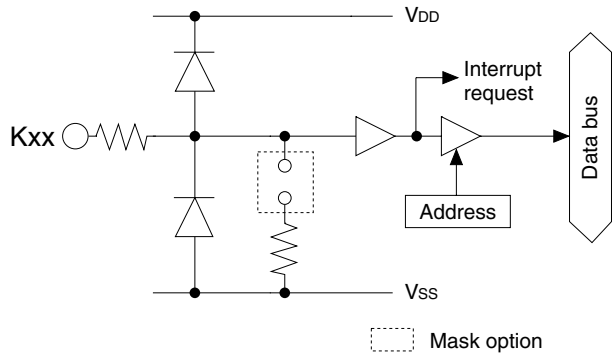


Fig. 4.5.1.1 Configuration of input port

Selection of "With pull down resistor" with the mask option suits input from the push switch, key matrix, and so forth. When "Gate direct" is selected, the port can be used for slide switch input and interfacing with other LSIs.

4.5.2 Interrupt function

All 8 bits of the input ports (K00–K03, K10–K13) provide the interrupt function. The conditions for issuing an interrupt can be set by the software. Further, whether to mask the interrupt function can be selected by the software.
Figure 4.5.2.1 shows the configuration of K00–K03 (K10–K13) interrupt circuit.

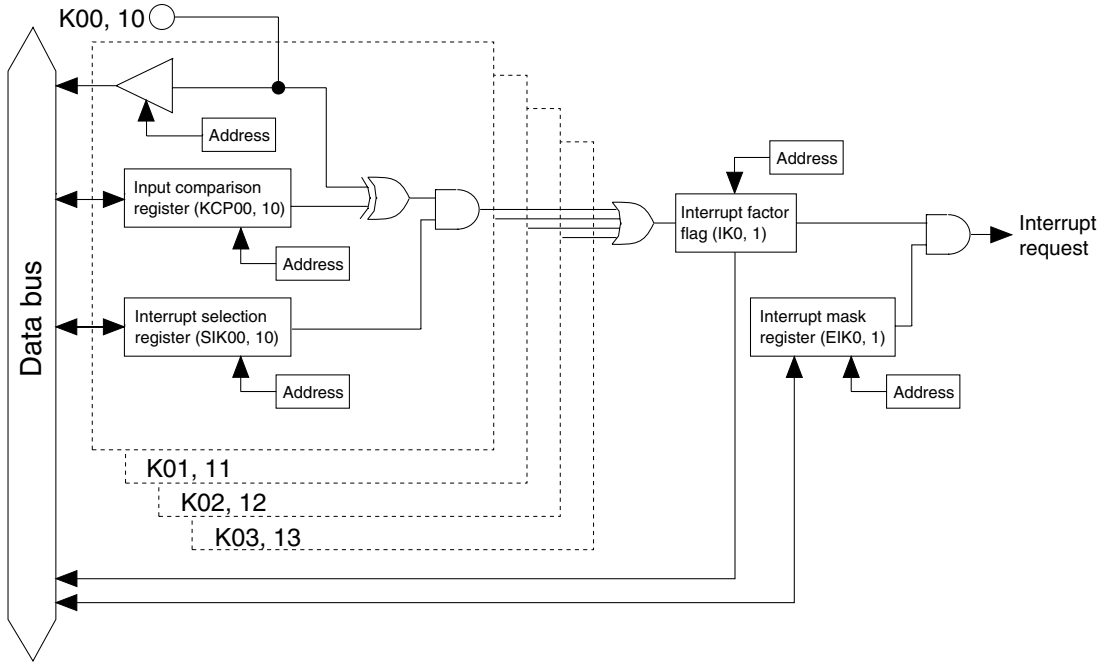


Fig. 4.5.2.1 Input interrupt circuit configuration

The interrupt selection register (SIK) and input comparison register (KCP) are individually set for the input ports K00–K03 and K10–K13, and can specify the terminal for generating interrupt and interrupt timing.
The interrupt selection register (SIK00–SIK03, SIK10–SIK13) select what input of K00–K03 and K10–K13 to use for the interrupt. Writing "1" into an interrupt selection register incorporates that input port into the interrupt generation conditions. The changing the input port where the interrupt selection register has been set to "0" does not affect the generation of the interrupt.
The input interrupt timing can select that the interrupt be generated at the rising edge of the input or that it be generated at the falling edge according to the set value of the input comparison register (KCP00–KCP03).
By setting these two conditions, the interrupt for K00–K03 and K10–K13 (4 bits unit) are generated when an input port in which an interrupt has been enabled by the input selection register and the content of the input comparison register have been changed from matching to no matching.
The interrupt mask registers EIK0 and EIK1 enable the interrupt mask to be selected for K00–K03 and K10–K13, respectively.
When the interrupt is generated, the interrupt factor flag (IK0 for K00–K03, IK1 for K10–K13) is set to "1".
Figure 4.5.2.2 shows an example of an interrupt for K00–K03.

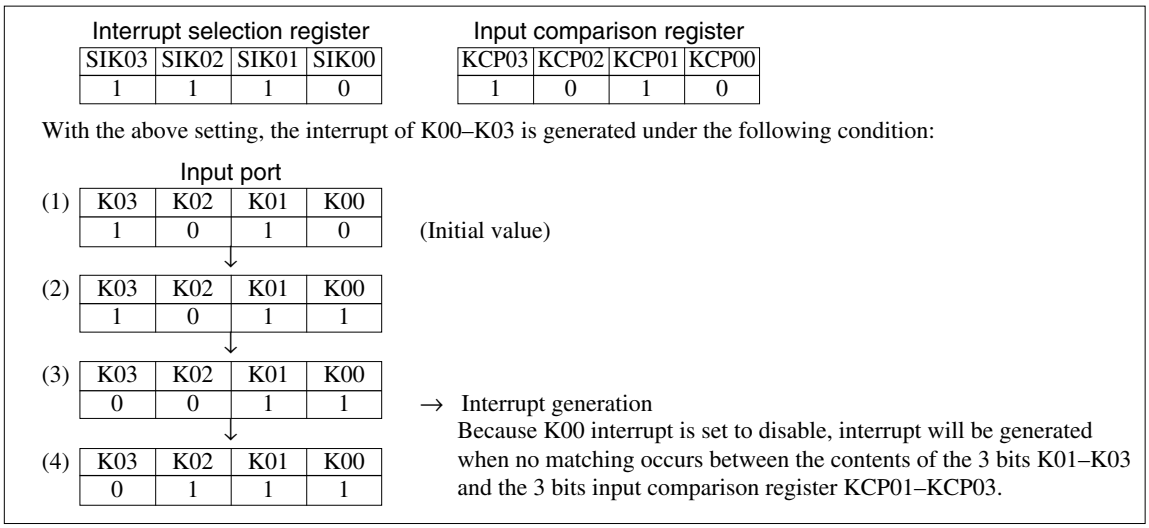


Fig. 4.5.2.2 Example of interrupt of K00–K03

K00 interrupt is disabled by the interrupt selection register (SIK00), so that an interrupt does not occur at (2). At (3), K03 changes to "0"; the data of the terminal that is interrupt enabled no longer matches the data of the input comparison register, so that interrupt occurs. As already explained, the condition for the interrupt to occur is the change in the port data and contents of the input comparison register from matching to no matching. Hence, in (4), when the no matching status changes to another no matching status, an interrupt does not occur. Further, terminals that have been masked for interrupt do not affect the conditions for interrupt generation.

4.5.3 Mask option

Internal pull down resistor can be selected for each of the 8 bits of the input ports (K00–K03, K10–K13) with the input port mask option.
When you have selected "Gate direct", take care that the floating status does not occur for the input. Select "With pull down resistor" for input ports that are not being used.

4.5.4 Control of input ports

Table 4.5.4.1 lists the input ports control bits and their addresses.

Table 4.5.4.1 Input port control bits

Address *7	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
90H	SIK03	SIK02	SIK01	SIK00	SIK03	0	Enable	Disable	Interrupt selection register (K03)
					SIK02	0	Enable	Disable	Interrupt selection register (K02)
	R/W				SIK01	0	Enable	Disable	Interrupt selection register (K01)
					SIK00	0	Enable	Disable	Interrupt selection register (K00)
91H	K03	K02	K01	K00	K03	– *2	High	Low	Input port (K00–K03)
					K02	– *2	High	Low	
	R				K01	– *2	High	Low	
					K00	– *2	High	Low	
92H	KCP03	KCP02	KCP01	KCP00	KCP03	0	↓	↑	Input comparison register (K00–K03)
					KCP02	0	↓	↑	
	R/W				KCP01	0	↓	↑	
					KCP00	0	↓	↑	
94H	SIK13	SIK12	SIK11	SIK10	SIK13	0	Enable	Disable	Interrupt selection register (K13)
					SIK12	0	Enable	Disable	Interrupt selection register (K12)
	R/W				SIK11	0	Enable	Disable	Interrupt selection register (K11)
					SIK10	0	Enable	Disable	Interrupt selection register (K10)
95H	K13	K12	K11	K10	K13	– *2	High	Low	Input port (K10–K13)
					K12	– *2	High	Low	
	R				K11	– *2	High	Low	
					K10	– *2	High	Low	
96H	KCP13	KCP12	KCP11	KCP10	KCP13	0	↓	↑	Input comparison register (K10–K13)
					KCP12	0	↓	↑	
	R/W				KCP11	0	↓	↑	
					KCP10	0	↓	↑	
F1H	0	0	0	EIK1	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R			R/W	0 *5	– *2			Unused
					EIK1	0	Enable	Mask	Interrupt mask register (K10–K13)
F2H	0	0	0	EIK0	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R			R/W	0 *5	– *2			Unused
					EIK0	0	Enable	Mask	Interrupt mask register (K00–K03)
F9H	0	0	0	IK1	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R				0 *5	– *2			Unused
					IK1 *4	0	Yes	No	Interrupt factor flag (K10–K13)
FAH	0	0	0	IK0	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R				0 *5	– *2			Unused
					IK0 *4	0	Yes	No	Interrupt factor flag (K00–K03)

*1 Initial value at the time of initial reset
*2 Not set in the circuit
*3 Undefined
*4 Reset (0) immediately after being read
*5 Constantly "0" when being read
*6 Refer to main manual
*7 Page switching in I/O memory is not necessary

K00–K03, K10–K13: Input port data (91H, 95H)

Input data of the input port terminals can be read with these registers.

When "1" is read:	High level
When "0" is read:	Low level
Writing:	Invalid

The reading is "1" when the terminal voltage of the 8 bits of the input ports (K00–K03, K10–K13) goes high (V_{DD}), and "0" when the voltage goes low (V_{SS}).
These bits are dedicated for reading, so writing cannot be done.

KCP00–KCP03, KCP10–KCP13: Input comparison registers (92H, 96H)

Interrupt conditions for terminals K00–K03 and K10–K13 can be set with these registers.

When "1" is written:	Falling edge
When "0" is written:	Rising edge
Reading:	Valid

The interrupt conditions can be set for the rising or falling edge of input for each of the eight bits (K00–K03 and K10–K13), through the input comparison registers (KCP00–KCP03 and KCP10–KCP13).
For KCP00–KCP03, a comparison is done only with the ports that are enabled by the interrupt among K00–K03 by means of the SIK00–SIK03 registers. For KCP10–KCP13, a comparison is done only with the ports that are enabled by the interrupt among K10–K13 by means of the SIK10–SIK13 registers.
At initial reset, these registers are set to "0".

SIK00–SIK03, SIK10–SIK13: Interrupt selection registers (90H, 94H)

Selects the port to be used for the K00–K03 and K10–K13 input interrupt.

When "1" is written:	Enable
When "0" is written:	Disable
Reading:	Valid

Enables the interrupt for the input ports (K00–K03, K10–K13) for which "1" has been written into the interrupt selection register (SIK00–SIK03, SIK10–SIK13). The input port set for "0" does not affect the interrupt generation condition.
At initial reset, these registers are set to "0".

EIK0, EIK1: Interrupt mask registers (F2H•D0, F1H•D0)

Masking the interrupt of the input port can be selected with these registers.

When "1" is written:	Enable
When "0" is written:	Mask
Reading:	Valid

With these registers, masking of the input port can be selected for each of the two systems (K00–K03, K10–K13).
At initial reset, these registers are all set to "0".

IK0, IK1: Interrupt factor flags (FAH•D0, F9H•D0)

These flags indicate the occurrence of input interrupt.

When "1" is read:	Interrupt has occurred
When "0" is read:	Interrupt has not occurred
Writing:	Invalid

The interrupt factor flags IK0 and IK1 are associated with K00–K03 and K10–K13, respectively. From the status of these flags, the software can decide whether an input interrupt has occurred.
These flags are set to "1" by generating the corresponding interrupt factor regardless of the interrupt mask register setting.
Reading of interrupt factor flags is available at EI, but be careful in the following cases.
If the interrupt mask register value corresponding to the interrupt factor flags to be read is set to "1", an interrupt request will be generated by the interrupt factor flags set timing, or an interrupt request will not be generated.
These flags are reset when the software reads them.
At initial reset, these flags are set to "0".

4.5.5 Programming notes

(1) When input ports are changed from high to low by pull down resistor, the fall of the waveform is delayed on account of the time constant of the pull down resistor and input gate capacitance. Hence, when fetching input ports, set an appropriate wait time.
Particular care needs to be taken of the key scan during key matrix configuration. Aim for a wait time of about 1 msec.

(2) When the input comparison register (KCP00–KCP03, KCP10–KCP13) is set, the interrupt factor flag (IK0, IK1) may be set to "1" depending on the status of the input port terminal. Consequently, when setting this register, do it in the DI status (interrupt flag = "0") and then read the interrupt factor flag in order to reset, or after setting the interrupt selection register (SIK00–SIK03, SIK10–SIK13) to the interrupt disabled status.

(3) Reading of interrupt factor flags is available at EI, but be careful in the following cases.
If the interrupt mask register value corresponding to the interrupt factor flags to be read is set to "1", an interrupt request will be generated by the interrupt factor flags set timing, or an interrupt request will not be generated.

4.6 Output Ports (R00–R03, R10–R13)

4.6.1 Configuration of output ports

The E0C6256 has 8 bits (4-bit × 2) general output ports.
Output specifications of the output ports can be selected individually with the mask option. Two kinds of output specifications are available: complementary output and Pch open drain output.
Further, the output port R10–R12 to be used as special output ports by the software setting.
Figure 4.6.1.1 shows the configuration of the output port.

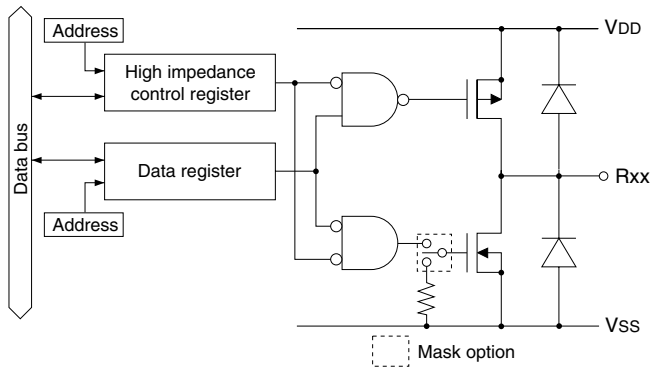


Fig. 4.6.1.1 Configuration of output port

4.6.2 Mask option

Output specifications of the output ports can be selected with the mask option.
Output specifications for the output ports (R00–R03, R10–R13) enable selection of either complementary output or Pch open drain output for each of the 8 bits.
However, even when Pch open drain output is selected, voltage exceeding source voltage must not be applied to the output port.

4.6.3 High impedance control

The terminal output state of output ports R00–R03 and R10–R13 may be selected for high impedance state by the software in 4-bit groups. Control is done with the high impedance control registers R0HIZ and R1HIZ.

4.6.4 Special output

In addition to the regular DC output, special output can be selected for the output ports R10–R12 as shown in Table 4.6.4.1 with the software. Figure 4.6.4.1 shows the configuration of the special output.

Table 4.6.4.1 Special output

Terminal	Special output	Output enable register
R10	FOUT	FOUTE
R11	PTOVF	PTOE
R12	BZ	BZE

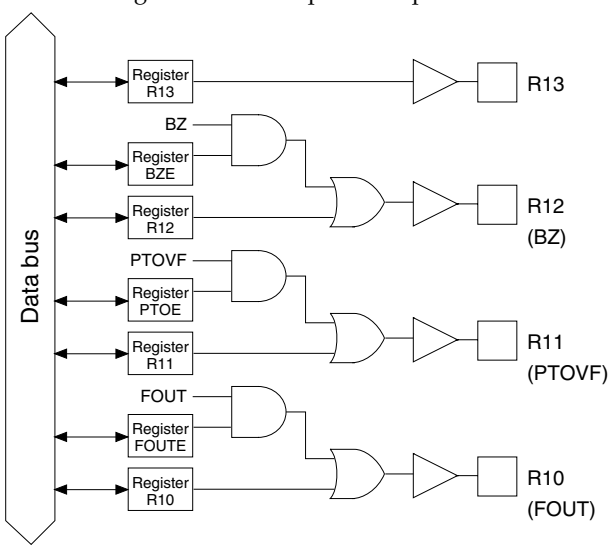


Fig. 4.6.4.1 Configuration of special output

At initial reset, the output terminals are set to low (V_{SS}).
When an R10–R12 is used as the special output port, fix the output port register R10–R12 at "0" and turn the signal ON or OFF using the special output enable register.

Note: Be sure that the output terminal is fixed at a high (V_{DD}) level the same with the DC output if "1" is written to the R10–R12 register when the special output has been selected.

• FOUT (R10)

FOUT signal can be output from the R10 terminal.
FOUT signal is a clock output from the oscillation circuit or a clock that the f_{OSC1} (32.768 kHz) output from the OSC1 oscillation circuit has divided in the internal circuit.
When R10 is used for FOUT output, keep R10 register set to "0". ON/OFF of the signal output can be controlled using the FOUT output enable register FOUTE.
The frequency of clock output signal may be selected from among 4 types as Table 4.6.4.2 by setting of the FOFQ0 and FOFQ1 registers. "f_{OSC3}" is the output clock of the OSC3 oscillation circuit.

Table 4.6.4.2 FOUT clock frequency

FOFQ1	FOFQ0	Clock frequency (Hz)
0	0	512
0	1	4,096
1	0	f_{OSC1}
1	1	f_{OSC3}

Note: A hazard may occur when the FOUT signal is turned ON or OFF.

Figure 4.6.4.2 shows the output waveform of FOUT.

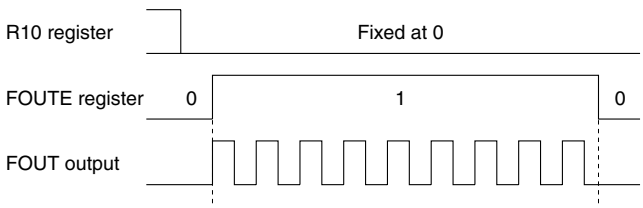


Fig. 4.6.4.2 Output waveform of FOUT

• PTOVF (R11)

PTOVF signal can be output from the R11 terminal.
The PTOVF signal is the output clock of the programmable timer.
When R11 is used for PTOVF output, keep R11 register set to "0". ON/OFF of the signal output can be controlled using the PTOE register. However, control of the programmable timer is necessary.
See Section 4.11, "Programmable Timer", for details of the programmable timer.

Note: A hazard may occur when the PTOVF signal is turned ON or OFF.

Figure 4.6.4.3 shows the output waveform of PTOVF.

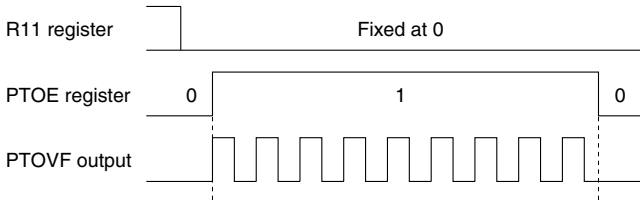


Fig. 4.6.4.3 Output waveform of PTOVF

• BZ (R12)

BZ is the buzzer signal output for driving the piezo-electric buzzer, and it can be output from the R12 terminal.
When R12 is used for BZ output, keep R12 register set to "0". ON/OFF of the signal output can be controlled by the BZE register.
The buzzer frequency and duty ratio may be selected by the software. Moreover, digital envelope may be added to the buzzer signal.
See Section 4.13, "Sound Generator", for details of the buzzer output.

4.6.5 Control of output ports

Table 4.6.5.1 lists the output ports' control bits and their addresses.

Table 4.6.5.1 Control bits of output ports

Address *7	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
A0H	0	0	0	R0HIZ	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R			R/W	0 *5	– *2			Unused
					R0HIZ	0	High-Z	Output	R0 output high-impedance control
A1H	R03	R02	R01	R00	R03	0	High	Low	Output port (R00–R03)
					R02	0	High	Low	
	R/W				R01	0	High	Low	
					R00	0	High	Low	
A2H	0	0	0	R1HIZ	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R			R/W	0 *5	– *2			Unused
					R1HIZ	0	High-Z	Output	R1 output high-impedance control
A3H	R13	R12	R11	R10	R13	0	High	Low	Output port (R13)
					R12	0	High	Low	Output port (R12)
		BZ	PTOVF	FOUT	BZ	0	Off	On	Buzzer output
	R/W				R11	0	High	Low	Output port (R11)
					PTOVF	0	Off	On	PTOVF output
					R10	0	High	Low	Output port (R10)
					FOUT	0	Off	On	FOUToutput
C0H	FOUTE	0	FOFQ1	FOFQ0	FOUTE	0	Enable	Disable	FOUT output enable
					0 *5	– *2			Unused
	R/W	R	R/W		FOFQ1	0			FOUT frequency selection
					FOFQ0	0			0: 512 Hz, 1: 4096 Hz, 2: fosc1, 3: fosc3
CAH	PNRFS	PTOE	PTRUN	PTRST	PNRFS	0	1024Hz	256Hz	Noise rejector clock frequency selection
					PTOE	0	Enable	Disable	PTOVF output enable
	R/W			W	PTRUN	0	Run	Stop	Programmable timer Run/Stop
					PTRST *5	Rst (reload)	Rst (reload)	–	Programmable timer reset (reload)
DCH	ENRTM	ENRST	ENON	BZE	ENRTM	0	1sec	0.5sec	Envelope releasing time
					ENRST *5	Reset	Reset	–	Envelope reset
	R/W	W	R/W		ENON	0	On	Off	Envelope On/Off
					BZE	0	Enable	Disable	Buzzer output enable

*1 Initial value at the time of initial reset
*2 Not set in the circuit
*3 Undefined
*4 Reset (0) immediately after being read
*5 Constantly "0" when being read
*6 Refer to main manual
*7 Page switching in I/O memory is not necessary

R0HIZ, R1HIZ: High impedance control registers (A0H•D0, A2H•D0)

Controls high impedance loading to output ports R00–R03 and R10–R13 in units of 4 bits groups.

When "1" is written: High impedance
When "0" is written: Data output
Reading: Valid

By writing "0" in the control registers (R0HIZ, R1HIZ) corresponding to the groups (R00–R03, R10–R13), the output signal is generated in the terminal; writing "1" will generate high impedance state.
At initial reset, these registers are set to "0".

R00–R03, R10–R13: Output port data (A1H, A3H)

Sets the output data for the output ports.

When "1" is written: High output
When "0" is written: Low output
Reading: Valid

The output port terminals output the data written in the corresponding registers (R00–R03, R10–R13) without changing it. When "1" is written in the register, the output port terminal goes high (V_{DD}), and when "0" is written, the output port terminal goes low (V_{SS}).
The registers R10–R12 that are used as special output should be fixed at "0".
At initial reset, these registers are set to "0".

FOUTE: FOUT output enable register (C0H•D3)
Controls the FOUT output ON or OFF.

When "1" is written: FOUT output enable
When "0" is written: FOUT output disable
Reading: Valid

By writing "1" to FOUTE when "0" has been set to the R10 register, the FOUT signal is output from the R10 terminal. When "0" is written, the R10 terminal goes to a low (VSS) level.
When R10 is used for DC output, keep FOUTE register set to "0".
At initial reset, this register is set to "0".

FOFQ0, FOFQ1: FOUT frequency selection register (C0H•D0, D1)
Selects the FOUT frequency.

Table 4.6.5.2 FOUT clock frequency

FOFQ1	FOFQ0	Clock frequency (Hz)
0	0	512
0	1	4,096
1	0	fOSC1
1	1	fOSC3

At initial reset, these registers are set to "0".

PTOE: PTOVF output enable register (CAH•D2)
Controls the PTOVF output ON or OFF.

When "1" is written: PTOVF output enable
When "0" is written: PTOVF output disable
Reading: Valid

By writing "1" to PTOE when "0" has been set to the R11 register, the PTOVF signal is output from the R11 terminal. When "0" is written, the R11 terminal goes to a low (VSS) level.
When R11 is used for DC output, keep PTOE register set to "0".
At initial reset, this register is set to "0".
See Section 4.11, "Programmable Timer" for the PTOVF signal.

BZE: BZ output enable register (DCH•D0)
Controls the BZ output ON or OFF.

When "1" is written: BZ output enable
When "0" is written: BZ output disable
Reading: Valid

By writing "1" to BZE when "0" has been set to the R12 register, the BZ signal is output from the R12 terminal. When "0" is written, the R12 terminal goes to a low (VSS) level.
When R12 is used for DC output, keep BZE register set to "0".
At initial reset, this register is set to "0".
See Section 4.13, "Sound Generator" for the buzzer signal.

4.6.6 Programming notes

(1) When R10–R12 are used for DC output, the special output enable registers FOUTE (C0H•D3), PTOE (CAH•D2) and BZE (DCH•D0) should be fixed at "0".

(2) When the special output is selected, the corresponding output port register (R10–R12) should be fixed at "0". Be sure that the output terminal is fixed at a high (VDD) level the same with the DC output if "1" is written to the R10–R12 register when the special output has been selected.

(3) When BZ, FOUT and PTOVF are selected, a hazard may be observed in the output waveform when the data of the output register changes.

(4) When selecting fOSC3 as the FOUT clock frequency, it is necessary to control the OSC3 oscillation circuit and the oscillation system regulated voltage circuit.
See Section 4.4, "Oscillation Circuit" for details of the control.

4.7 I/O Ports (P00–P03, P10–P13)

4.7.1 Configuration of I/O ports

The E0C6256 has 8 bits (4-bit × 2) general-purpose I/O ports. Figure 4.7.1.1 shows the configuration of the I/O port.
The 8 bits of the I/O ports P00–P03 and P10–P13 can be set to either input mode or output mode. Modes can be set by writing data to the I/O control register.
Moreover, pull down resistor which is turned ON during input mode can be controlled by the software.

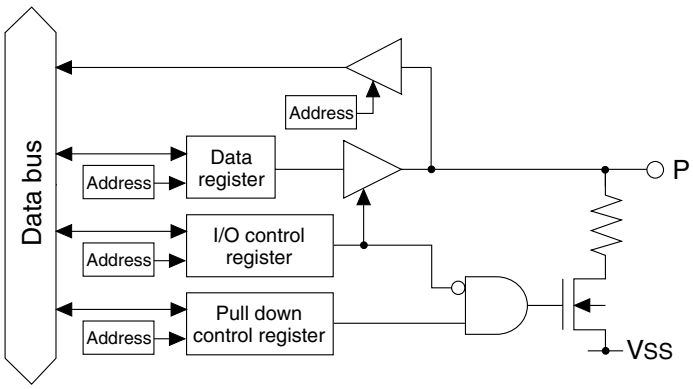


Fig. 4.7.1.1 Configuration of I/O port

The I/O ports P10–P13 are common used with the input/output ports of the serial interface, and function of these ports can be selected by the software.
See Section 4.12, "Serial Interface", for details of the serial interface.

4.7.2 I/O control registers and input/output mode

Input or output mode can be set for the 8 bits of I/O ports P00–P03 and P10–P13 by writing data into the corresponding I/O control register IOC00–IOC03 and IOC10–IOC13.

To set the input mode, write "0" to the I/O control register. When an I/O port is set to input mode, it becomes high impedance status and works as an input port.
However, when the pull down explained in the following section has been set by software, the input line is pulled down only during this input mode.

The output mode is set when "1" is written to the I/O control register. When an I/O port set to output mode works as an output port, it outputs a high level (V_{DD}) when the port output data is "1", and a low level (V_{SS}) when the port output data is "0".

If perform the read out in each mode; when output mode, the register value is read out, and when input mode, the port value is read out.

At initial reset, the I/O control registers are set to "0", and the I/O port enters the input mode.

4.7.3 Pull down during input mode

A pull down resistor that operates during the input mode is built into the I/O ports of the E0C6256. Software can set the use or non-use of this pull down. The pull down resistor becomes effective by writing "1" into the pull down control registers PUL00–PUL03 and PUL10–PUL13 that correspond to each of P00–P03 and P10–P13, and the input line is pulled down during the input mode. When "0" has been written, no pull down is done.
At initial reset, the pull down control registers are set to "1".

4.7.4 Mask option

Output specifications during the output mode (IOC = "1") can be selected with the mask option.
Output specifications for the I/O ports (P00–P03, P10–P13) enable selection of either complementary output or Pch open drain output for each of the 8 bits.
However, even when Pch open drain output is selected, voltage exceeding source voltage must not be applied to the output port.

4.7.5 Control of I/O ports

Table 4.7.5.1 lists the I/O ports' control bits and their addresses.

Table 4.7.5.1 Control bits of I/O ports

Address *7	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
B0H	IOC03	IOC02	IOC01	IOC00	IOC03	0	Output	Input	I/O control register (P00–P03)
					IOC02	0	Output	Input	
	R/W				IOC01	0	Output	Input	
					IOC00	0	Output	Input	
B1H	PUL03	PUL02	PUL01	PUL00	PUL03	1	On	Off	Pull down control register (P00–P03)
					PUL02	1	On	Off	
	R/W				PUL01	1	On	Off	
					PUL00	1	On	Off	
B2H	P03	P02	P01	P00	P03	– *2	High	Low	I/O port (P00–P03)
					P02	– *2	High	Low	
	R/W				P01	– *2	High	Low	
					P00	– *2	High	Low	
B4H	IOC13	IOC12	IOC11	IOC10	IOC13	0	Output	Input	I/O control register (P10–P13) (ESIF = 0)
					IOC12	0	Output	Input	
	R/W				IOC11	0	Output	Input	
					IOC10	0	Output	Input	
	When the serial I/F is used (ESIF = 1):				IOC13	0	Output	Input	Master mode: P13 I/O control register
	P10 = SIN (in), P11 = SOUT (out),				IOC13	0	1	0	Slave mode: General-purpose register
	P12 = SCLK (master: out, slave: in),				IOC12	0	1	0	General-purpose register
	P13 = SRDY (slave: out),				IOC11	0	1	0	
	P13 = I/O port (master: in/out)				IOC10	0	1	0	
B5H	PUL13	PUL12	PUL11	PUL10	PUL13	1	On	Off	Pull down control register (P10–P13) (ESIF = 0)
					PUL12	1	On	Off	
	R/W				PUL11	1	On	Off	
					PUL10	1	On	Off	
	When the serial I/F is used (ESIF = 1):				PUL13	1	On	Off	Master mode: P13 pull down control register
	P10 = SIN (in), P11 = SOUT (out),				PUL13	1	1	0	Slave mode: General-purpose register
	P12 = SCLK (master: out, slave: in),				PUL12	1	1	0	Master mode: General-purpose register
	P13 = SRDY (slave: out),				PUL12	1	On	Off	Slave mode: SCKL pull down control register
	P13 = I/O port (master: in/out)				PUL11	1	1	0	General-purpose register
					PUL10	1	On	Off	SIN pull down control register
B6H	P13	P12	P11	P10	P13	– *2	High	Low	I/O port (P10–P13) (ESIF = 0)
					P12	– *2	High	Low	
	R/W				P11	– *2	High	Low	
					P10	– *2	High	Low	
	When the serial I/F is used (ESIF = 1):				P13	– *2	High	Low	Master mode: I/O port P13
	P10 = SIN (in), P11 = SOUT (out),				P13	– *2	1	0	Slave mode: General-purpose register
	P12 = SCLK (master: out, slave: in),				P12	– *2	1	0	General-purpose register
	P13 = SRDY (slave: out),				P11	– *2	1	0	
	P13 = I/O port (master: in/out)				P10	– *2	1	0	

*1 Initial value at the time of initial reset
*2 Not set in the circuit
*3 Undefined
*4 Reset (0) immediately after being read
*5 Constantly "0" when being read
*6 Refer to main manual
*7 Page switching in I/O memory is not necessary

P00–P03, P10–P13: I/O port data (B2H, B6H)

I/O port data can be read and output data can be set through these ports.

- ***When writing data***

  When "1" is written: High level
  When "0" is written: Low level

When an I/O port is set to the output mode, the written data is output unchanged from the I/O port terminal. When "1" is written as the port data, the port terminal goes high (V_{DD}), and when "0" is written, the level goes low (V_{SS}).
Port data can be written also in the input mode.

• ***When reading data out***

When "1" is read: High level
When "0" is read: Low level

When the I/O port is in the input mode the voltage level being input to the port terminal can be read out; in the output mode the register value can be read. When the terminal voltage in the input mode is high (V_{DD}) the port data that can be read is "1", and when the terminal voltage is low (V_{SS}) the data is "0".
When PUL register is set to "1", the built-in pull down resister goes ON during input mode, so that the I/O port terminal is pulled down. The gate floating has not occur by the input control signal even if the PUL register is set to "0" and no pull down register is set.

When the serial input/output function is selected for P10–P13 ports, the registers P10–P13 in the slave mode and the registers P10–P12 in the master mode can be used as a general register having both read and write functions, and data of these registers exert no affect on the input/output signal. In the master mode, since P13 is not used for the serial interface and can be used as an I/O port, the P13 register becomes the I/O port data register.

IOC00–IOC03, IOC10–IOC13: I/O control registers (B0H, B4H)

The input and output modes of the I/O ports can be set with these registers.

When "1" is written: Output mode
When "0" is written: Input mode
Reading: Valid

The input and output modes of the I/O ports are set in units of one bit. IOC00–IOC03 and IOC10–IOC13 set the mode for P00–P03 and P10–P13, respectively.
Writing "1" to the I/O control register makes the corresponding I/O port enter the output mode, and writing "0" induces the input mode.
At initial reset, these registers are set to "0", so the I/O ports are in the input mode.

When the serial input/output function is selected for P10–P13 ports, the registers IOC10–IOC13 in the slave mode and the registers IOC10–IOC12 in the master mode can be used as a general register having both read and write functions, and data of these registers exert no affect on the input/output signal. In the master mode, since P13 is not used for the serial interface and can be used as an I/O port, the IOC13 register becomes the I/O control register.

PUL00–PUL03, PUL10–PUL13: Pull down control registers (B1H, B5H)

The pull down during the input mode can be set with these registers.

When "1" is written: Pull down ON
When "0" is written: Pull down OFF
Reading: Valid

The built-in pull down resistor which is turned ON during input mode is set to enable in units of one bit. PUL00–PUL03 and PUL10–PUL13 set the pull down for P00–P03 and P10–P13, respectively.
By writing "1" to the pull down control register, the corresponding I/O ports are pulled down (during input mode), while writing "0" turns the pull down function OFF.
At initial reset, these registers are set to "1", so the pull down function is set to ON.

When the serial input/output function is selected for P10–P13 ports, the PUL11 register, the PUL12 register in the master mode and the PUL13 register in the slave mode can be used as general registers having both read and write functions, and data of these registers exert no affect on the input/output signal. In the master mode, since P13 is not used for the serial interface and can be used as an I/O port, the PUL13 register becomes the pull down control register.

4.7.6 Programming note

When the I/O ports are changed from high to low by pull down resistor during input mode, the fall of the waveform is delayed on account of the time constant of the pull down resistor and input gate capacitance. Hence, when fetching input data, set an appropriate wait time.
Particular care needs to be taken of the key scan during key matrix configuration. Aim for a wait time of about 1 msec.

4.8 LCD Driver (COM0–COM4, SEG0–SEG59)

4.8.1 Configuration of LCD driver

The E0C6256 has 5 common terminals (COM0–COM4) and 60 segment terminals (SEG0–SEG59), so that it can drive an LCD with a maximum of 300 (60 × 5) segments.
The power for driving the LCD is generated by the internal circuit so that there is no need to apply power especially from outside.
The driving method is 1/2 duty dynamic drive depending on the four types of potential, V_{DD}, V_{L1}, V_{L2} and V_{L3}. In addition to the 1/2 duty, 1/3, 1/4 and 1/5 drive duty can be selected by the software. The frame frequency is 25.6 Hz for 1/5 duty, 32 Hz for 1/4 and 1/2 duty, and 42.7 Hz for 1/3 duty (f_{OSC1} = 32.768 kHz).
LCD display ON/OFF may be controlled by the software.

Note: "f_{OSC1}" indicates the oscillation frequency of the OSC1 oscillation circuit.

4.8.2 LCD drive voltage

The LCD drive voltage V_{L1} is generated by the LCD system regulated voltage circuit, and V_{L2} and V_{L3} are generated by boosting the V_{L1} voltage with the LCD system voltage booster circuit.
The V_{L1} voltage can be adjusted to match the LCD panel characteristics using the registers VLCHG0–VLCHG2. To generate V_{L1}, V_{SS} (V_{S2} when the supply voltage doubler/halver is used) voltage (V_{DD} standard) must be lower than V_{L1} - 0.2 V.

V_{SS}/V_{S2} (absolute value) ≥ V_{L1} (absolute value) + 0.2 V

Table 4.8.2.1 V_{L1} setting

VLCHG2	VLCHG1	VLCHG0	V_{L1} voltage	V_{SS}/V_{S2} voltage range
0	0	0	-1.05 V	-1.25 V to -3.6 V
0	0	1	-1.10 V	-1.30 V to -3.6 V
0	1	0	-1.15 V	-1.35 V to -3.6 V
0	1	1	-1.20 V	-1.40 V to -3.6 V
1	0	0	-1.25 V	-1.45 V to -3.6 V
1	0	1	-1.30 V	-1.50 V to -3.6 V
1	1	0	-1.35 V	-1.55 V to -3.6 V
1	1	1	-1.40 V	-1.60 V to -3.6 V

(Voltage value: V_{DD} reference)

The LCD system power circuit that generates V_{L1}–V_{L3} is turned ON and OFF by the LCD power control register LPWR and the A/D converter power control register APWR.
By setting LPWR or APWR to "1", the LCD system power circuit generates V_{L1}–V_{L3}. When LPWR and APWR are both set to "0", V_{L1}–V_{L3} becomes V_{DD} level. In this case, all outputs from the COM terminals and SEG terminals go to V_{DD} level. When setting LPWR to "0" and APWR to "1", all outputs from the COM terminals and SEG terminals go to V_{L1} level.
To display the LCD, the LCD drive power must be ON by previously setting LPWR to "1".
SEG output ports that are set for DC output by the mask option operate same as the output (R) port regardless of the power ON/OFF control.

Note: The LCD driver cannot be used even if the power is on (when only the A/D converter power control register APWR has been set to "1"), unless the LCD power control register LPWR has been set to "1".

4.8.3 LCD display ON/OFF control and duty switching

(1) Display ON/OFF control

In the E0C6256, ON/OFF of the LCD display can be controlled by the LOFF register.
At initial reset, LOFF is set to "0", and the LCD display is set to the ON status.
The LCD power is OFF at initial reset, so the display is actually performed when the LCD power is turned ON (LPWR = "1").
To set all of the LCD display OFF, write "1" to LOFF. With this, the SEG terminals output an OFF waveform.

(2) Switching of drive duty

By setting the registers LDTY0 and LDTY1, the LCD drive duty can be selected from among 4 types, 1/5, 1/4, 1/3 and 1/2 duty. Table 4.8.3.1 shows the LCD drive duty setting.

Table 4.8.3.1 LCD drive duty setting

LDTY1	LDTY0	Duty	Terminals used in common	Maximum number of segments	Frame frequency *
0	0	1/2	COM0, COM1	120 (60 × 2)	fosc1/1,024 (32 Hz)
0	1	1/3	COM0–COM2	180 (60 × 3)	fosc1/768 (42.7 Hz)
1	0	1/4	COM0–COM3	240 (60 × 4)	fosc1/1,024 (32 Hz)
1	1	1/5	COM0–COM4	300 (60 × 5)	fosc1/1,280 (25.6 Hz)

* In case of fosc1 = 32.728 kHz

Basically you should select the drive duty with the smallest drive segment number (for example, 1/3 duty for 160 segments and 1/2 duty for 100 segments) from among the drive duties permitting driving of the segment number of the LCD panel.
Figures 4.8.3.1–4.8.3.4 show the dynamic drive waveform for 1/5 duty, 1/4 duty, 1/3 duty and 1/2 duty.

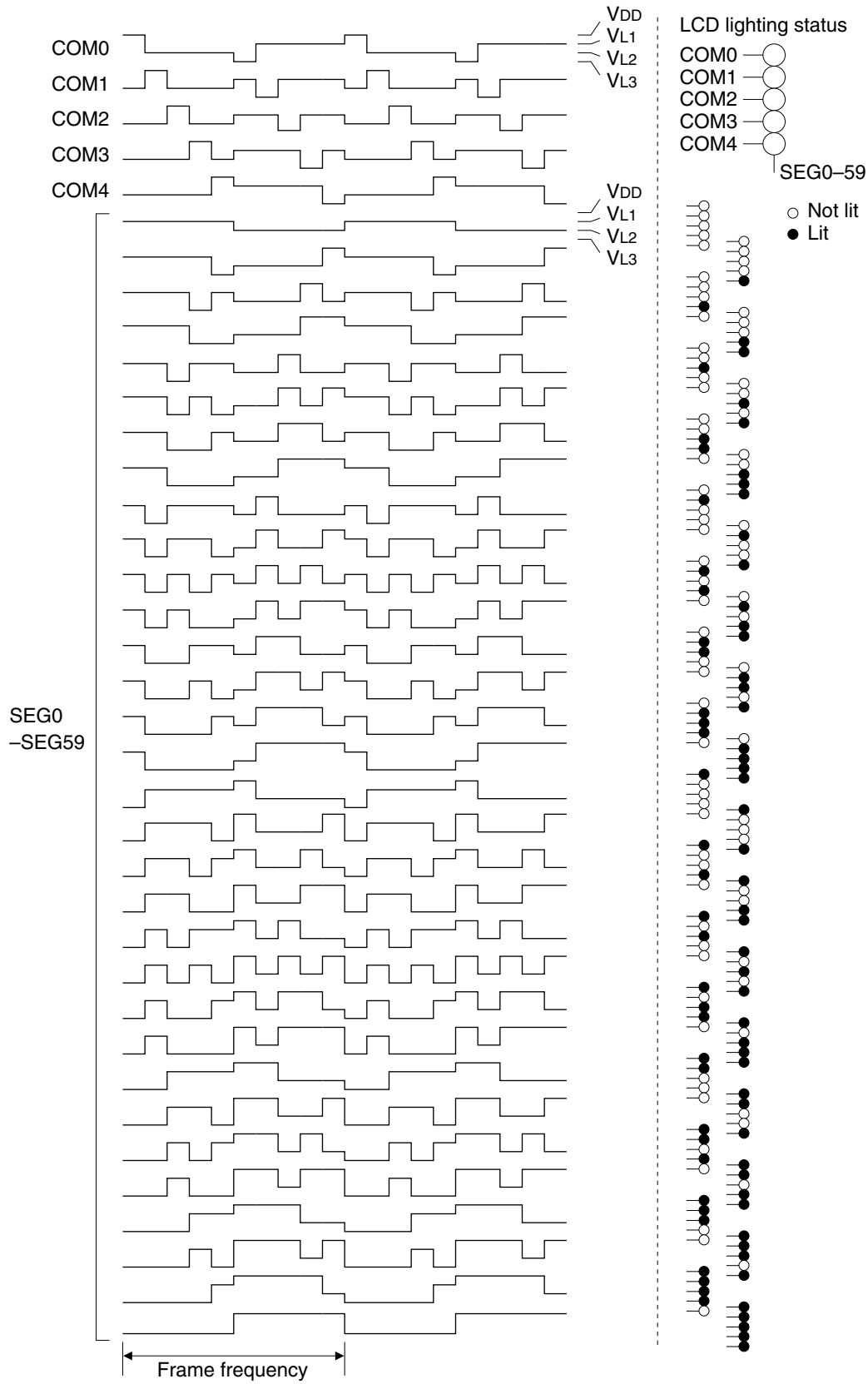


Fig. 4.8.3.1 Drive waveform for 1/5 duty

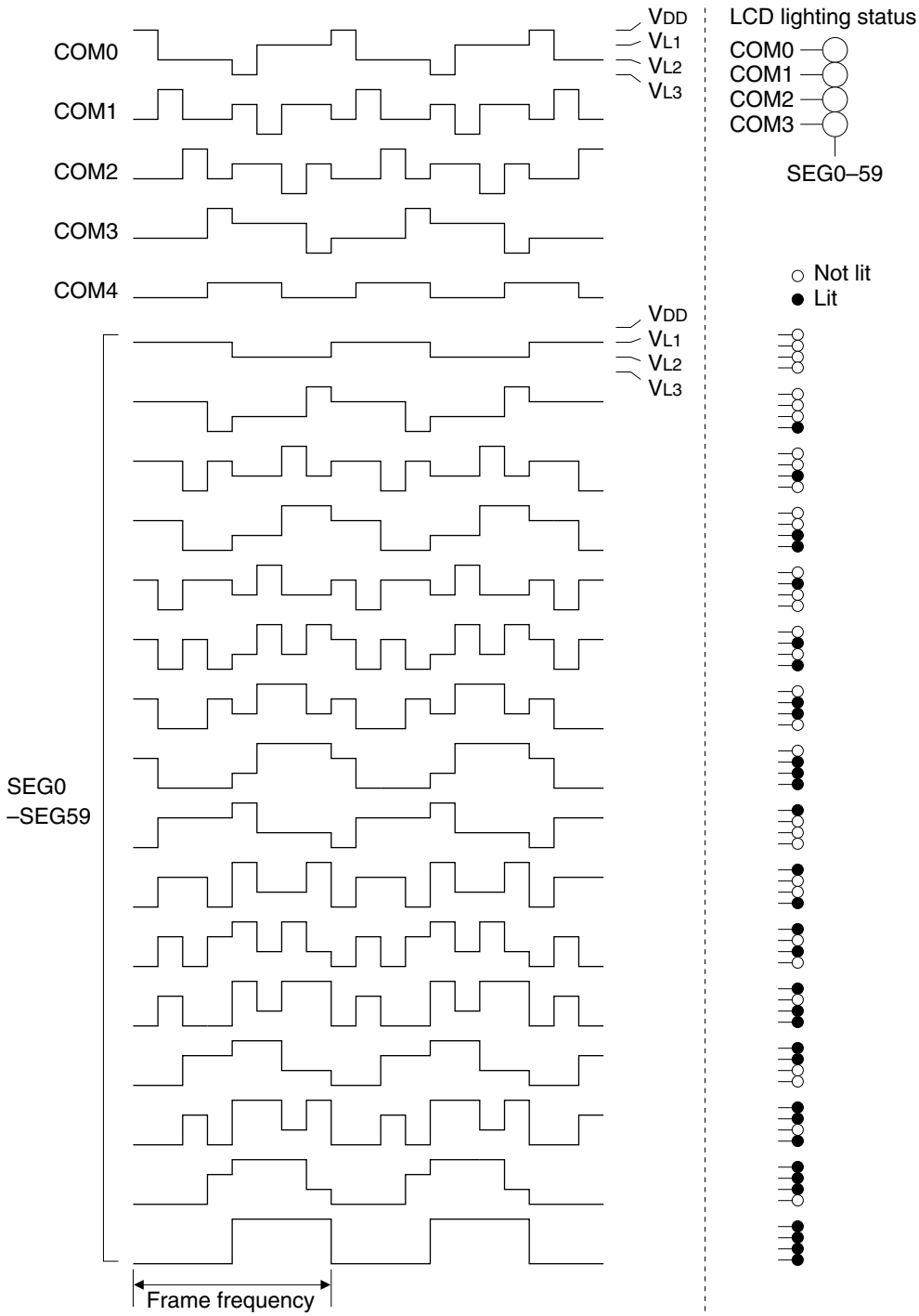


Fig. 4.8.3.2 Drive waveform for 1/4 duty

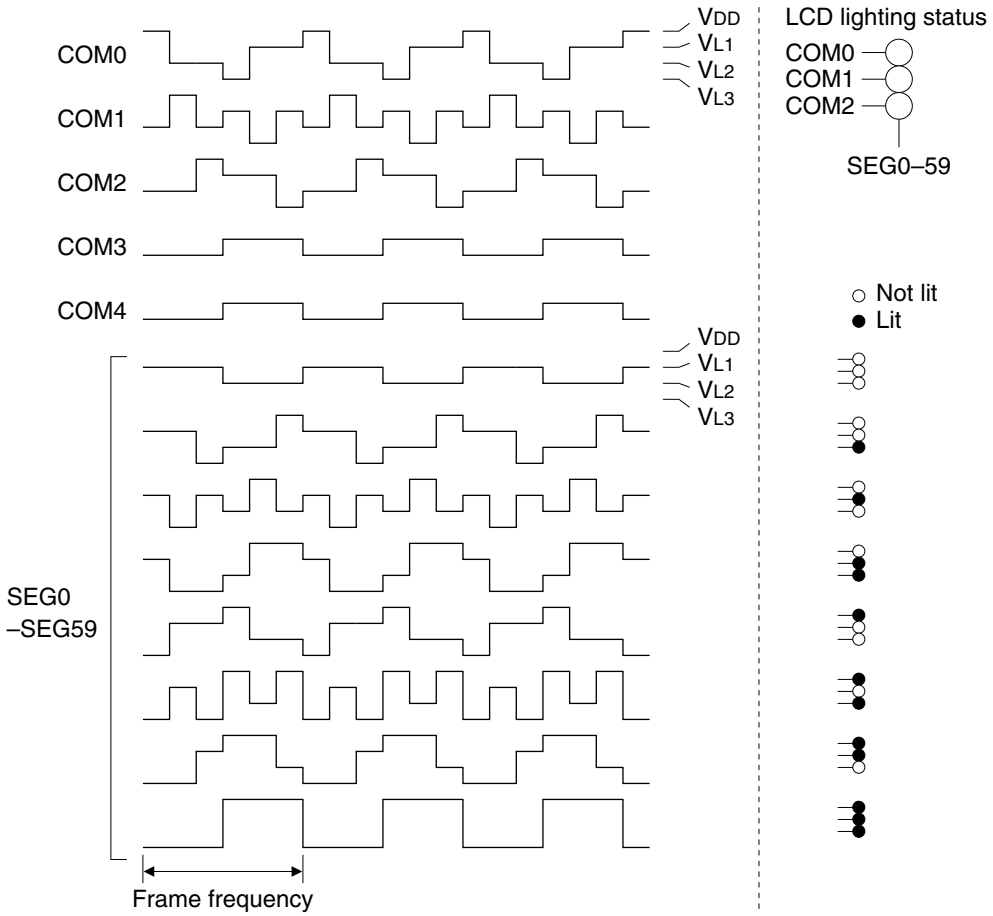


Fig. 4.8.3.3 Drive waveform for 1/3 duty

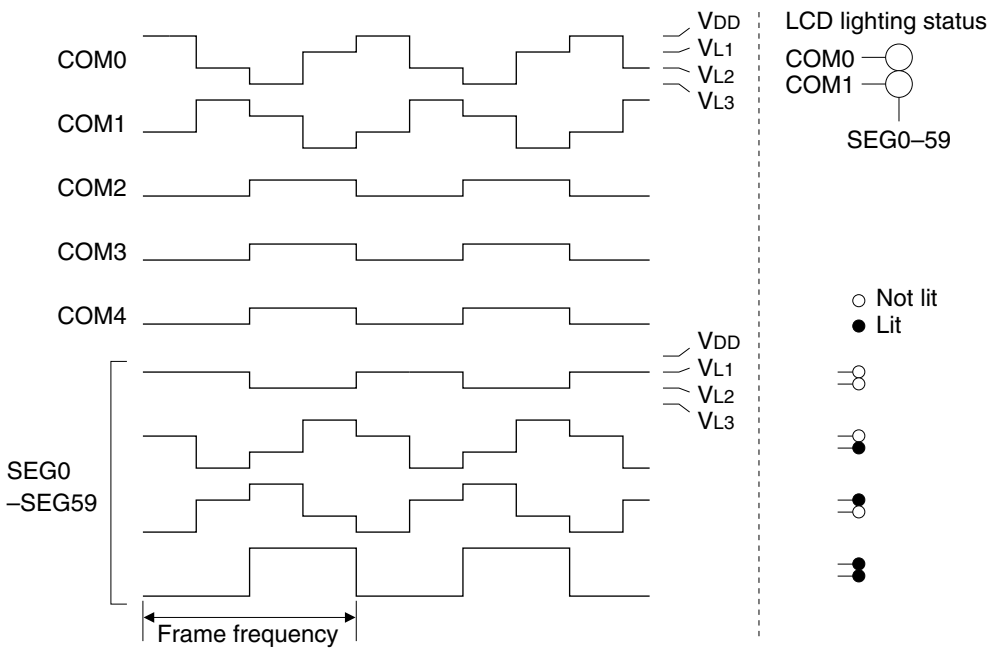


Fig. 4.8.3.4 Drive waveform for 1/2 duty

4.8.4 Switching between dynamic and static drive

The E0C6256 provides software setting of the LCD static drive.
The frame frequency during static driving is fixed at 32 Hz (when f_{OSC1} = 32.768 kHz) regardless of the drive duty selection.
This function enables easy adjustment (cadence adjustment) of the oscillation frequency of the OSC1 oscillation circuit (crystal oscillation circuit).

The procedure for executing static drive of the LCD is as follows:

① Write "1" to register STCD at address C2H•D2.

② Write the same value to all registers corresponding to COM0–COM4 of the display memory.

Note: • When setting the static drive, all the COM outputs become effective regardless of the drive duty selection. Hence, for static drive, set the same value to all display memory corresponding to COM0–COM4 even when a drive duty other than 1/5 duty has been selected.

• For cadence adjustment, set the display data corresponding to COM0–COM4, so that all the LCDs light.

Figure 4.8.4.1 shows the drive waveform for static drive.

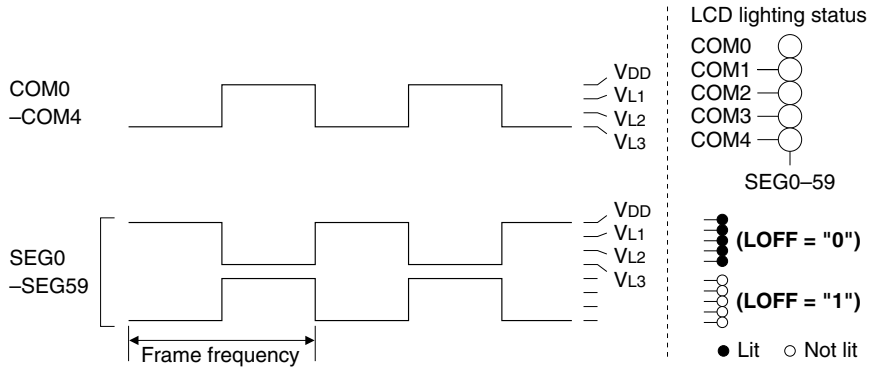


Fig. 4.8.4.1 LCD static drive waveform

4.8.5 Display memory area

The display memory is allocated in the data memory area, addresses 30H–7FH in page 1 or page 5. Either of the areas used can be selected using the software (LDMS register).
By setting LDMS to "1", page 1 is selected and addresses 130H–17FH become the display memory. Since a RAM has been allocated in this area, it can be used as the display memory for reading/writing. For this reason, control in a bit unit can simply be done using an arithmetic instruction. However, this area should not be used for general purpose RAM.
At initial reset, LDMS is set to "0" and page 5 (530H–57FH) becomes the display memory. When this area is selected, all the internal RAM (0 to 4 page) can be used as general purpose RAM. However, since the display memory is write only, data modification by arithmetic instructions cannot be done.
Correspondence between segment outputs and bits within the display memory can be optionally set by the mask option explained in the next section.

4.8.6 Mask option (segment allocation)

(1) Segment allocation

The LCD driver has a segment decoder built-in, and the data bit (D0–D3) of the optional address in the display memory area (30H–7FH) can be allocated to the optional segment. This makes design easy by increasing the degree of freedom with which the liquid crystal panel can be designed.
The allocated segment displays when the bit for the display memory is set to "1", and goes out when bit is set to "0".

Figure 4.8.6.1 shows an example of the relationship between the LCD segments (on the panel) and the display memory for the case of 1/3 duty.

Address	Data			
	D3	D2	D1	D0
7AH	d	c	b	a
7BH	p	g	f	e
7CH	d'	c'	b'	a'
7DH	p'	g'	f'	e'

Display memory allocation

	Common 0	Common 1	Common 2
SEG10	7A, D0 (a)	7B, D1 (f)	7B, D0 (e)
SEG11	7A, D1 (b)	7B, D2 (g)	7A, D3 (d)
SEG12	7D, D1 (f')	7A, D2 (c)	7B, D3 (p)

Pin address allocation

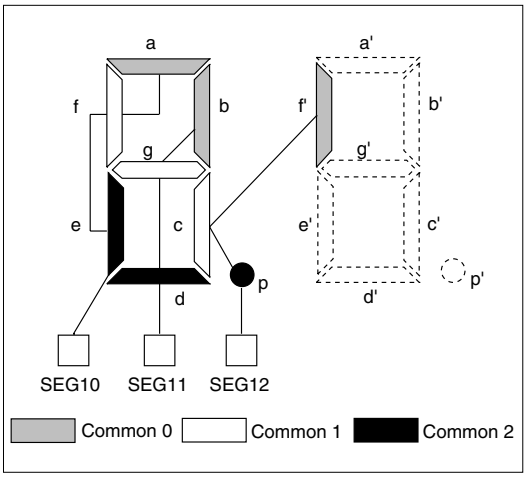


Fig. 4.8.6.1 Segment allocation

(2) Output specification

① The segment terminals (SEG0–SEG59) can be selected with the mask option par two terminals for either segment signal output or DC output (VDD and VSS binary output).
When DC output is selected, the data corresponding to COM0 of each segment terminal is output.

② When DC output is selected, either complementary output or Pch open drain output can be selected for each terminal with the mask option.

4.8.7 Control of LCD driver

Table 4.8.7.1 shows the LCD driver's control bits and their addresses. Figure 4.8.7.1 shows the display memory map.

Table 4.8.7.1 LCD driver control bits

Address *7	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
84H	0	VLCHG2	VLCHG1	VLCHG0	0 *5	– *2			Unused
					VLCHG2	0			VL1 output voltage change
	R	R/W			VLCHG1	0			0: 1.05, 1: 1.10, 2: 1.15, 3: 1.20,
					VLCHG0	0			4: 1.25, 5: 1.30, 6: 1.35, 7: 1.40 (V)
C2H	LDMS	STCD	LDTY1	LDTY0	LDMS	0	1p(R/W)	5p(W)	LCD data memory area selection
					STCD	0	Static	Dynamic	LCD drive switch
	R/W				LDTY1	0			LCD drive duty selection
					LDTY0	0			0: 1/2, 1: 1/3, 2: 1/4, 3: 1/5
C3H	0	0	LOFF	LPWR	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R		R/W		LOFF	0	All Off	Normal	LCD display control
					LPWR	0	On	Off	LCD power supply On/Off

*1 Initial value at the time of initial reset
*2 Not set in the circuit
*3 Undefined
*4 Reset (0) immediately after being read
*5 Constantly "0" when being read
*6 Refer to main manual
*7 Page switching in I/O memory is not necessary

Address Page	Low / High	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
1 or 5	3	Display memory (80 words × 4 bits) Page 1: R/W Page 5: W only															
	4																
	5																
	6																
	7																

Fig. 4.8.7.1 Display memory map

VLCHG0–VLCHG2: VL1 output voltage change (84H•D0–D2)

The voltage value of the LCD drive voltage VL1 can be selected among 8 types as shown in Table 4.8.7.2.

Table 4.8.7.2 VL1 setting

VLCHG2	VLCHG1	VLCHG0	VL1 voltage
0	0	0	-1.05 V
0	0	1	-1.10 V
0	1	0	-1.15 V
0	1	1	-1.20 V
1	0	0	-1.25 V
1	0	1	-1.30 V
1	1	0	-1.35 V
1	1	1	-1.40 V

(Voltage value: VDD reference)

At initial reset, these registers are set to "0".

LPWR: LCD power supply ON/OFF (C3H•D0)

Controls the LCD power ON and OFF

When "1" is written: Power ON
When "0" is written: Power OFF
Reading: Valid

By writing "1" to LPWR, the LCD power goes ON.
When "0" is written, the LCD power goes OFF and all terminals of the COM output and SEG output become VDD level.
When the LCD power is set to OFF and the A/D converter power is set to ON (APWR = "1"), COM and SEG terminals become VL1 level.
This control does not affect to SEG terminals that have been set for DC output.
At initial reset, this register is set to "0".

LOFF: LCD display control (C3H•D1)

Controls the LCD display

When "1" is written: Display all OFF
When "0" is written: Display ON
Reading: Valid

When "1" is written to LOFF, all LCD dots will fade out; writing "0" will set it back to normal.
All fading out of LCD at LOFF = "1" is due to light out signals and does not affect the content of the segment data memory.
Flashing on the entire LCD panel is performed by this function.
At initial reset, this register is set to "0".

STCD: LCD drive switch (C2H•D2)

Switches the LCD driving method.

When "1" is written: Static drive
When "0" is written: Dynamic drive
Reading: Valid

By writing "1" to STCD, static drive is selected, and dynamic drive is selected when "0" is written.
At initial reset, this register is set to "0".

LDTY1, LDTY0: LCD drive duty selection (C2H•D1, D0)

Sets the LCD drive duty as shown in Table 4.8.7.3.

Table 4.8.7.3 LCD drive duty setting

LDTY1	LDTY0	Duty	Terminals used in common	Maximum number of segments	Frame frequency *
0	0	1/2	COM0, COM1	120 (60 × 2)	fosc1/1,024 (32 Hz)
0	1	1/3	COM0–COM2	180 (60 × 3)	fosc1/768 (42.7 Hz)
1	0	1/4	COM0–COM3	240 (60 × 4)	fosc1/1,024 (32 Hz)
1	1	1/5	COM0–COM4	300 (60 × 5)	fosc1/1,280 (25.6 Hz)

* In case of fosc1 = 32.728 kHz

At initial reset, these registers are set to "0".

LDMS: LCD display memory area selection (C2H•D3)

Selects the display memory area.

When "1" is written: Page 1 (R/W)
When "0" is written: Page 5 (W)
Reading: Valid

By writing "1" to LDMS, page 1 is selected and addresses 130H–17FH become the display memory. Since a RAM has been allocated in this area, it can be used as the display memory for reading/writing.
When LDMS is set to "0", page 5 (530H–57FH) becomes the display memory. This ares is write only.
At initial reset, this register is set to "0".

Display memory (30H–7FH)

The LCD segments are lit or turned off depending on this data.

When "1" is written: Lit
When "0" is written: Not lit
Reading: Invalid

By writing data into the display memory allocated to the LCD segment (on the panel), the segment can be lit or put out.
At initial reset, the contents of the display memory are undefined.

4.8.8 Programming notes

(1) The contents of the display memory are undefined until the area is initialized (through, for instance, memory clear processing by the CPU). Initialize the display memory by executing initial processing.

(2) When page 5 is selected for the display memory area, since the display memory area is write-only, display data cannot be rewritten by arithmetic operations (such as AND, OR, ADD, SUB).

(3) 100 msec or more time is necessary for stabilizing the LCD drive voltages V_{L1}, V_{L2} and V_{L3} after setting the LCD power control register LPWR to "1". Be careful of the segment-on right after the power is turned on.

4.9 Clock Timer

4.9.1 Configuration of clock timer

The E0C6256 has a built-in clock timer with OSC1 divided clock as clock source. The clock timer is configured of a 8-bit binary counter and the timer data (128–16 Hz and 8–1 Hz) can be read out by the software.
Figure 4.9.1.1 is the block diagram for the clock timer.

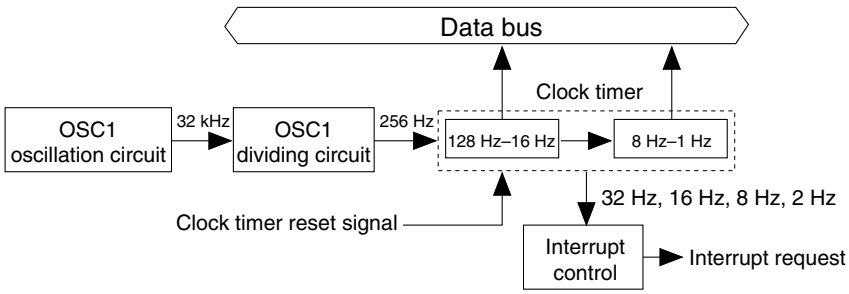


Fig. 4.9.1.1 Block diagram for the clock timer

Ordinarily, this clock timer is used for all types of timing functions such as clocks.

4.9.2 Data reading and hold function

The 8 bits timer data are allocated to the address C5H and C6H.

C5H	D0: TM0 (128 Hz)	D1: TM1 (64 Hz)	D2: TM2 (32 Hz)	D3: TM3 (16 Hz)
C6H	D0: TM4 (8 Hz)	D1: TM5 (4 Hz)	D2: TM6 (2 Hz)	D3: TM7 (1 Hz)

Since the clock timer data has been allocated to two addresses, a carry is generated from the low-order data within the count (TM0–TM3: 128–16 Hz) to the high-order data (TM4–TM7: 8–1 Hz). When this carry is generated between the reading of the low-order data and the high-order data, a content combining the two does not become the correct value (the low-order data is read as 0FH and the high-order data becomes the value that is counted up 1 from that point).
The high-order data hold function in the E0C6256 is designed to operate to avoid this. This function temporarily stops the counting up of the high-order data (by carry from the low-order data) at the point where the low-order data has been read and consequently the time during which the high-order data is held is the shorter of the two indicated here following.

1. Period until it reads the high-order data.
2. 0.48–1.5 msec (varies due to the timing of the reading)

Note: When the high-order data has previously been read, since the low-order data is not held, you should be sure to first read from the low-order data.

4.9.3 Interrupt function

The clock timer can cause interrupts at the falling edge of 32 Hz, 16 Hz, 8 Hz and 2 Hz signals. Software can set whether to mask any of these frequencies.
Figure 4.9.3.1 is the timing chart of the clock timer.

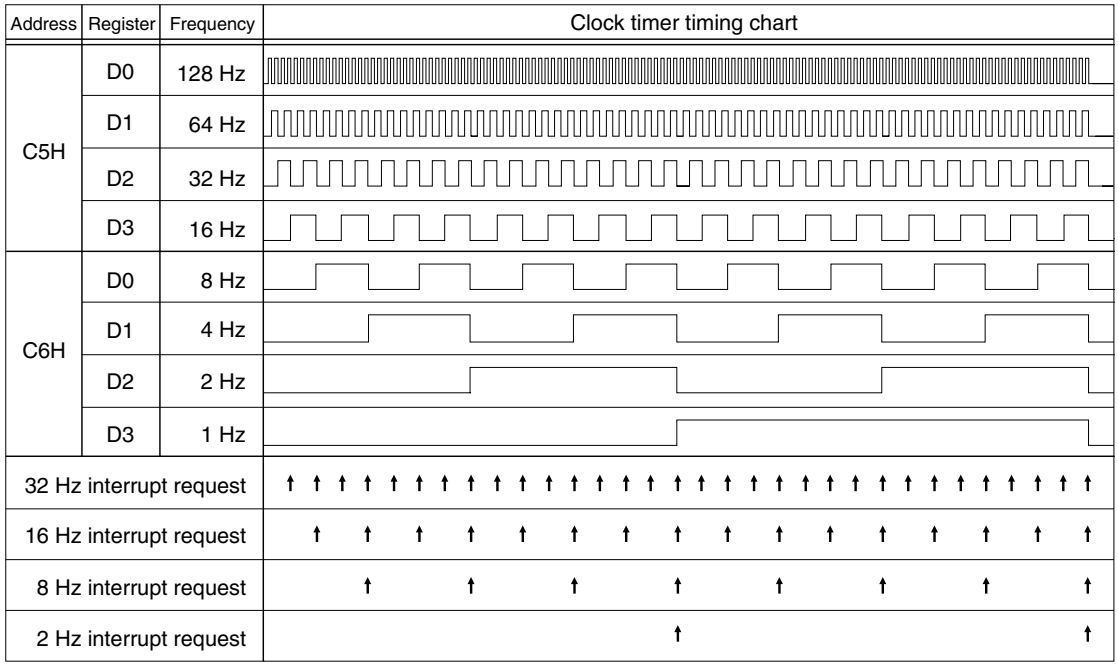


Fig. 4.9.3.1 Timing chart of clock timer

As shown in Figure 4.9.3.1, interrupt is generated at the falling edge of the frequencies (32 Hz, 16 Hz, 8 Hz, 2 Hz). At this time, the corresponding interrupt factor flag (IT0, IT1, IT2, IT3) is set to "1". Selection of whether to mask the separate interrupts can be made with the interrupt mask registers (EIT0, EIT1, EIT2, EIT3). However, regardless of the interrupt mask register setting, the interrupt factor flag is set to "1" at the falling edge of the corresponding signal.

4.9.4 Control of clock timer

Table 4.9.4.1 shows the clock timer control bits and their addresses.

Table 4.9.4.1 Control bits of clock timer

Address *7	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
C4H	0	0	TMRUN	TMRST	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R		R/W	W	TMRUN	0	Run	Stop	Clock timer Run/Stop
					TMRST *5	Reset	Reset	–	Clock timer reset
C5H	TM3	TM2	TM1	TM0	TM3	0			Clock timer data (16 Hz)
					TM2	0			Clock timer data (32 Hz)
	R				TM1	0			Clock timer data (64 Hz)
					TM0	0			Clock timer data (128 Hz)
C6H	TM7	TM6	TM5	TM4	TM7	0			Clock timer data (1 Hz)
					TM6	0			Clock timer data (2 Hz)
	R				TM5	0			Clock timer data (4 Hz)
					TM4	0			Clock timer data (8 Hz)
F6H	EIT3	EIT2	EIT1	EIT0	EIT3	0	Enable	Mask	Interrupt mask register (Clock timer 2 Hz)
					EIT2	0	Enable	Mask	Interrupt mask register (Clock timer 8 Hz)
	R/W				EIT1	0	Enable	Mask	Interrupt mask register (Clock timer 16 Hz)
					EIT0	0	Enable	Mask	Interrupt mask register (Clock timer 32 Hz)
FEH	IT3	IT2	IT1	IT0	IT3 *4	0	Yes	No	Interrupt factor flag (Clock timer 2 Hz)
					IT2 *4	0	Yes	No	Interrupt factor flag (Clock timer 8 Hz)
	R				IT1 *4	0	Yes	No	Interrupt factor flag (Clock timer 16 Hz)
					IT0 *4	0	Yes	No	Interrupt factor flag (Clock timer 32 Hz)

*1 Initial value at the time of initial reset
*2 Not set in the circuit
*3 Undefined
*4 Reset (0) immediately after being read
*5 Constantly "0" when being read
*6 Refer to main manual
*7 Page switching in I/O memory is not necessary

TM0–TM7: Timer data (C5H, C6H)

The 128 Hz–1 Hz timer data of the clock timer can be read out with these registers. These eight bits are read only, and writing operations are invalid.
By reading the low-order data (C5H), the high-order data (C6H) is held while the shorter of the two indicated here following.

1. Period until it reads the high-order data.
2. 0.48–1.5 msec (varies due to the timing of the reading)

At initial reset, the timer data is initialized to "00H".

TMRST: Clock timer reset (C4H•D0)

This bit resets the clock timer.

When "1" is written:	Clock timer reset
When "0" is written:	No operation
Reading:	Always "0"

The clock timer is reset by writing "1" to TMRST. When the clock timer is reset in the RUN status, operation restarts immediately. Also, in the STOP status the reset data is maintained.
This bit is write-only, and so is always "0" at reading.

TMRUN: Clock timer RUN/STOP (C4H•D1)

This bit controls RUN/STOP of the clock timer.

When "1" is written:	RUN
When "0" is written:	STOP
Reading:	Valid

The clock timer enters the RUN status when "1" is written to TMRUN, and the STOP status when "0" is written.
In the STOP status, the timer data is maintained until the next RUN status or resets timer. Also, when the STOP status changes to the RUN status, the data that was maintained can be used for resuming the count.
At initial reset, this register is set to "0".

EIT0, EIT1, EIT2, EIT3: Interrupt mask registers (F6H)

These registers are used to select whether to mask the clock timer interrupt.

When "1" is written:	Enabled
When "0" is written:	Masked
Reading:	Valid

The interrupt mask registers (EIT0, EIT1, EIT2, EIT3) are used to select whether to mask the interrupt to the separate frequencies (32 Hz, 16 Hz, 8 Hz, 2 Hz).
At initial reset, these registers are all set to "0".

IT0, IT1, IT2, IT3: Interrupt factor flags (FEH)

These flags indicate the status of the clock timer interrupt.

When "1" is read:	Interrupt has occurred
When "0" is read:	Interrupt has not occurred
Writing:	Invalid

The interrupt factor flags (IT0, IT1, IT2, IT3) correspond to the clock timer interrupts of the respective frequencies (32 Hz, 16 Hz, 8 Hz, 2 Hz). The software can judge from these flags whether there is a clock timer interrupt. However, even if the interrupt is masked, the flags are set to "1" at the falling edge of the signal.
These flags can be reset through being read out by the software.
Reading of interrupt factor flags is available at EI, but be careful in the following cases.
If the interrupt mask register value corresponding to the interrupt factor flags to be read is set to "1", an interrupt request will be generated by the interrupt factor flags set timing, or an interrupt request will not be generated.
At initial reset, these flags are set to "0".

4.9.5 Programming notes

(1) Be sure to data reading in the order of low-order data (TM0–TM3) then high-order data (TM4–TM7).

(2) When the clock timer has been reset, the interrupt factor flag (IT) may sometimes be set to "1". Consequently, perform flag reading (reset the flag) as necessary at reset.

(3) Reading of interrupt factor flags is available at EI, but be careful in the following cases.
If the interrupt mask register value corresponding to the interrupt factor flags to be read is set to "1", an interrupt request will be generated by the interrupt factor flags set timing, or an interrupt request will not be generated.

4.10 Stopwatch Timer

4.10.1 Configuration of stopwatch timer

The E0C6256 has a 1/1,000 sec stopwatch timer. The stopwatch timer is configured of a 3-stage, 4-bit BCD counter serving as the input clock of a 1,000 Hz signal output from the prescaler. Data can be read out four bits (1/1,000 sec, 1/100 sec and 1/10 sec) at a time by the software.
In addition it has a direct input function that controls the stopwatch timer RUN/STOP and LAP using the input ports K00 and K01.
Figure 4.10.1.1 is the block diagram of the stopwatch timer.

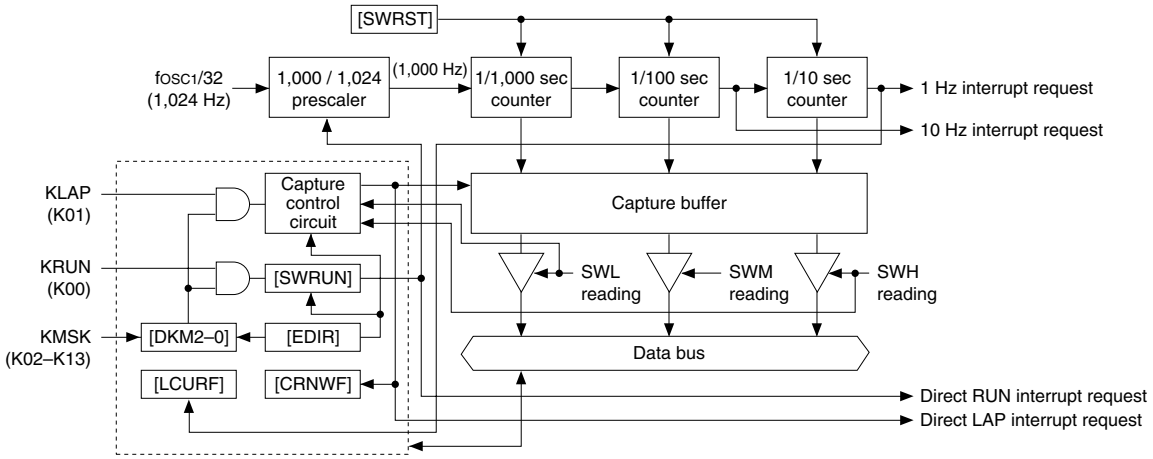


Fig. 4.10.1.1 Block diagram of stopwatch timer

The stopwatch timer can be used as a separate timer from the clock timer. In particular, digital watch stopwatch functions can be realized easily with software.

4.10.2 Counter and prescaler

The stopwatch timer is configured of four-bit BCD counters SWL, SWM and SWH.
The counter SWL, at the stage preceding the stopwatch timer, has a 1,000 Hz signal generated by the prescaler for the input clock. It counts up every 1/1,000 sec, and generates 100 Hz signal. The counter SWM has a 100 Hz signal generated by the counter SWL for the input clock. It count-up every 1/100 sec, and generated 10 Hz signal. The counter SWH has an approximated 10 Hz signal generated by the counter SWM for the input clock. It count-up every 1/10 sec, and generated 1 Hz signal.

The prescaler inputs a 1,024 Hz clock dividing fOSC1 (output from the OSC1 oscillation circuit), and outputs 1,000 Hz counting clock for SWL. To generate a 1,000 Hz clock from 1,024 Hz, 24 pulses from 1,024 pulses that are input to the prescaler every second are taken out.
When the counter becomes the value indicated below, one pulse (1,024 Hz) that is input immediately after to the prescaler will be pulled out.

<Counter value (msec) in which the pulse correction is performed>
39, 79, 139, 179, 219, 259, 299, 319, 359, 399, 439, 479, 539, 579, 619, 659, 699, 719, 759, 799, 839, 879, 939, 979

Figure 4.10.2.1 shows the operation of the prescaler.

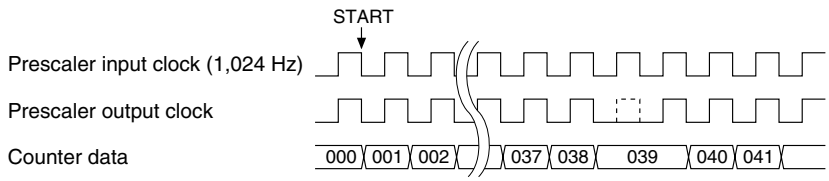


Fig. 4.10.2.1 Timing of the prescaler operation

For the above reason, the counting clock is 1,024 Hz (0.9765625 msec) except during pulse correction. Consequently, frequency of the prescaler output clock (1,000 Hz) , 100 Hz generated by SWL and 10 Hz generated by SWM are approximate values.

4.10.3 Capture buffer and hold function

The stopwatch data, 1/1,000 sec, 1/100 sec and 1/10 sec, can be read from SWL (D2H), SWM (D3H) and SWH (D4H), respectively. The counter data are latched in the capture buffer when reading, and are held until reading of three words is completed. For this reason, correct data can be read even when a carry from lower digits occurs during reading the three words. Further, three counter data are latched in the capture buffer at the same time when SWL (1/1,000 sec) is read. The data hold is released when SWH (1/10 sec) reading is completed. Therefore, data should be read in order of SWL→SWM→SWH. If SWM or SWH is first read when data have not been held, the hold function does not work and data in the counter is directly read out. When data that has not been held is read in the stopwatch timer RUN status, you cannot judge whether it is correct or not.

The stopwatch timer has a LAP function using an external key input (explained later). The capture buffer is also used to hold LAP data. In this case, data is held until SWH is read. However, when a LAP input is performed before completing the reading, the content of the capture buffer is renewed at that point. Remaining data that have not been read become invalid by the renewal, and the hold status is not released if SWH is read. When SWH is read after the capture buffer is updated, the capture renewal flag is set to "1" at that point. In this case, it is necessary to read from SWL again. The capture renewal flag is renewed by reading SWH.

Figure 4.10.3.1 shows the timing for data holding and reading.

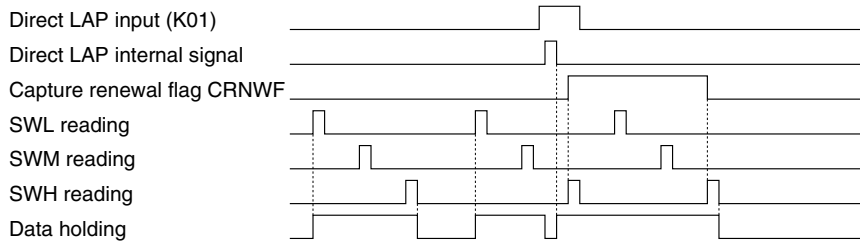


Fig. 4.10.3.1 Timing for data holding and reading

4.10.4 Stopwatch timer RUN/STOP and reset

RUN/STOP control and reset of the stopwatch timer can be done by the software.

(1) Stopwatch timer RUN/STOP

The stopwatch timer enters the RUN status when "1" is written to SWRUN, and the STOP status when "0" is written.

In the STOP status, the timer data is maintained until the next RUN status or resets timer. Also, when the STOP status changes to the RUN status, the data that was maintained can be used for resuming the count.

The RUN/STOP operation of the stopwatch timer by writing to the SWRUN register is performed in synchronization with the falling edge of the 1,024 Hz same as the prescaler input clock.

The SWRUN register can be read, and in this case it indicates the operating status of the stopwatch timer.

Figure 4.10.4.1 shows the operating timing when controlling the SWRUN register.

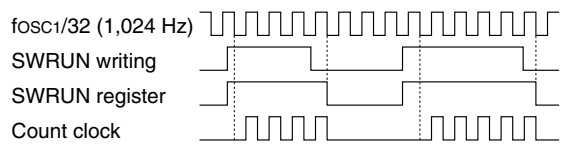


Fig. 4.10.4.1 Operating timing when controlling SWRUN

When the direct input function (explained in next section) is set, RUN/STOP control is done by an external key input. In this case, SWRUN becomes read only register that indicates the operating status of the stopwatch timer.

(2) Stopwatch timer reset

The stopwatch timer is reset when "1" is written to SWRST. With this, the counter value is cleared to "000".
Since this resetting does not affect the capture buffer, data that has been held in the capture buffer is not cleared and is maintained as is.
When the stopwatch timer is reset in the RUN status, counting restarts from count "000". Also, in the STOP status the reset data "000" is maintained until the next RUN.

4.10.5 Direct input function and key mask

The stopwatch timer has a direct input function that can control the RUN/STOP and LAP operation of the stopwatch timer by external key input. This function is set by writing "1" to the EDIR register. When EDIR is set to "0", only the software control is possible as explained in the previous section.

(1) Direct RUN

When the direct input function is selected, RUN/STOP operation of the stopwatch timer can be controlled by using the key connected to the input port K00. K00 works as a normal input port, but the input signal is sent to the stopwatch control circuit. The key input signal from the K00 port works as a toggle switch. When it is input in STOP status, the stopwatch timer runs, and in RUN status, the stopwatch timer stops. RUN/STOP status of the stopwatch timer can be checked by reading the SWRUN register.
An interrupt is generated by direct RUN input.
The sampling for key input signal is performed at the falling edge of 1,024 Hz signal same as the SWRUN control. The chattering judgment is performed at the point where the key turns OFF, and a chattering less than 46.8–62.5 msec is removed. Therefore, more time is needed for an interval between RUN and STOP key inputs.
Figure 4.10.5.1 shows the operating timing for the direct RUN input.

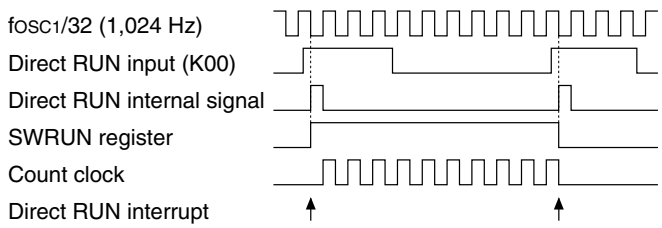


Fig. 4.10.5.1 Operating timing for direct RUN input

(2) Direct LAP

Control for the LAP can also be done by key input same as the direct RUN. When the direct input function is selected, the input port K01 becomes the LAP key input port. Sampling for the input signal and the chattering judgment are the same as a direct RUN.
By entering the LAP key, the counter data at that point is latched into the capture buffer and is held. The counter continues counting operation. Furthermore, an interrupt occurs by direct LAP input.
As stated above, the capture buffer data is held until SWH is read. If the LAP key is input when data has been already held, it renews the content of the capture buffer. When SWH is read after renewing, the capture renewal flag is set to "1". In this case, the hold status is not released by reading SWH, and it continues. Normally the LAP data should be read after the interrupt is generated. After that, be sure to check the capture renewal flag. When the capture renewal flag is set, renewed data is held in the capture buffer. So it is necessary to read from SWL again.
The stopwatch timer sets the 1 Hz interrupt factor flag ISW1 to "1" when requiring a carry-up to 1-sec digit by an SWH overflow. If the capture buffer shifts into hold status (when SWL is read or when LAP is input) while the 1 Hz interrupt factor flag ISW1 is set to "1", the lap data carry-up request flag LCURF is set to "1" to indicate that a carry-up to 1-sec digit is required for the processing of LAP input. In normal software processing, LAP processing may take precedence over 1-sec or higher digits processing by a 1 Hz interrupt, therefore carry-up processing using this flag should be used for time display in the LAP processing to prevent the 1-sec digit data decreasing by 1 second. This flag is renewed when the capture buffer shifts into hold status.

Figure 4.10.5.2 shows the operating timing for the direct LAP input, and Figure 4.10.5.3 shows the timings for data holding and reading during a direct LAP input and reading.

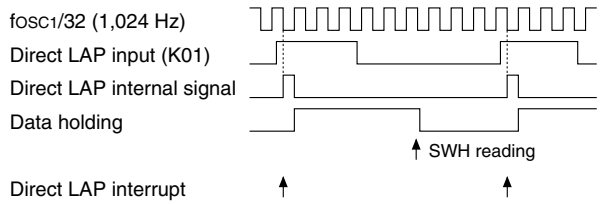


Fig. 4.10.5.2 Operating timing for direct LAP input

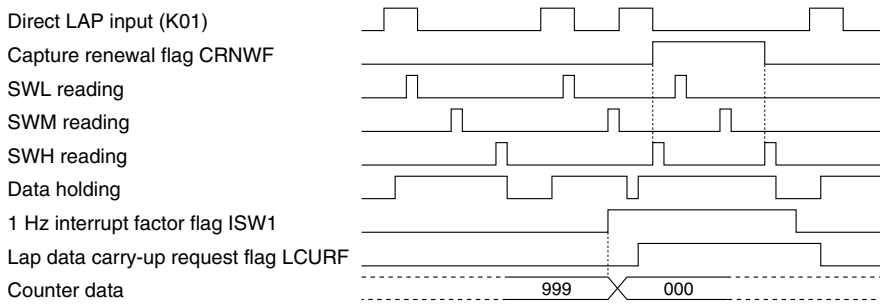


Fig. 4.10.5.3 Timing for data holding and reading during direct LAP input

(3) Key mask

In stopwatch applications, some functions may be controlled by a combination of keys including direct RUN or direct LAP. For instance, the RUN key can be used for other functions, such as reset and setting a watch, by pressing the RUN key with another key. In this case, the direct RUN function or direct LAP function must be invalid so that it does not function. For this purpose, the key mask function is set so that it judges concurrence of input keys and invalidates RUN and LAP functions. A combination of the key inputs for this judgment can be selected using the DKM0–DKM2 registers.

Table 4.10.5.1 Key mask selection

DKM2	DKM1	DKM0	Mask key combination
0	0	0	None (at initial reset)
0	0	1	K02
0	1	0	K02, K03
0	1	1	K02, K03, K10
1	0	0	K10
1	0	1	K10, K11
1	1	0	K10, K11, K12
1	1	1	K10, K11, K12, K13

RUN or LAP inputs become invalid in the following status.

1. The RUN or LAP key is pressed when one or more keys that are included in the selected combination (here in after referred to as mask) are held down.
2. The RUN or LAP key has been pressed when the mask is released.

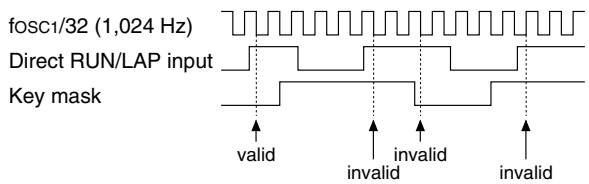


Fig. 4.10.5.4 Operation of key mask

RUN or LAP inputs become valid in the following status.

1. Either the RUN or LAP key is pressed independently if no other key is been held down.
2. Both the RUN and LAP keys are pressed at the same time if no other key is held down. (RUN and LAP functions are effective.)
3. The RUN or LAP key is pressed if either is held down. (RUN and LAP functions are effective.)
4. Either the RUN or LAP key and the mask key are pressed at the same time if no other key is held down.
5. Both the RUN and LAP keys and the mask key are pressed at the same time if no other key is held down. (RUN and LAP functions are effective.)

* Simultaneous key input is referred to as two or more key inputs are sampled at the same falling edge of 1,024 Hz clock.

4.10.6 Interrupt function

(1) 10 Hz and 1 Hz interrupts

The 10 Hz and 1 Hz interrupts can be generated through the overflow of stopwatch timers SWM and SWH respectively. Also, software can set whether to separately mask the frequencies described earlier. Figure 4.10.6.1 is the timing chart for the counters.

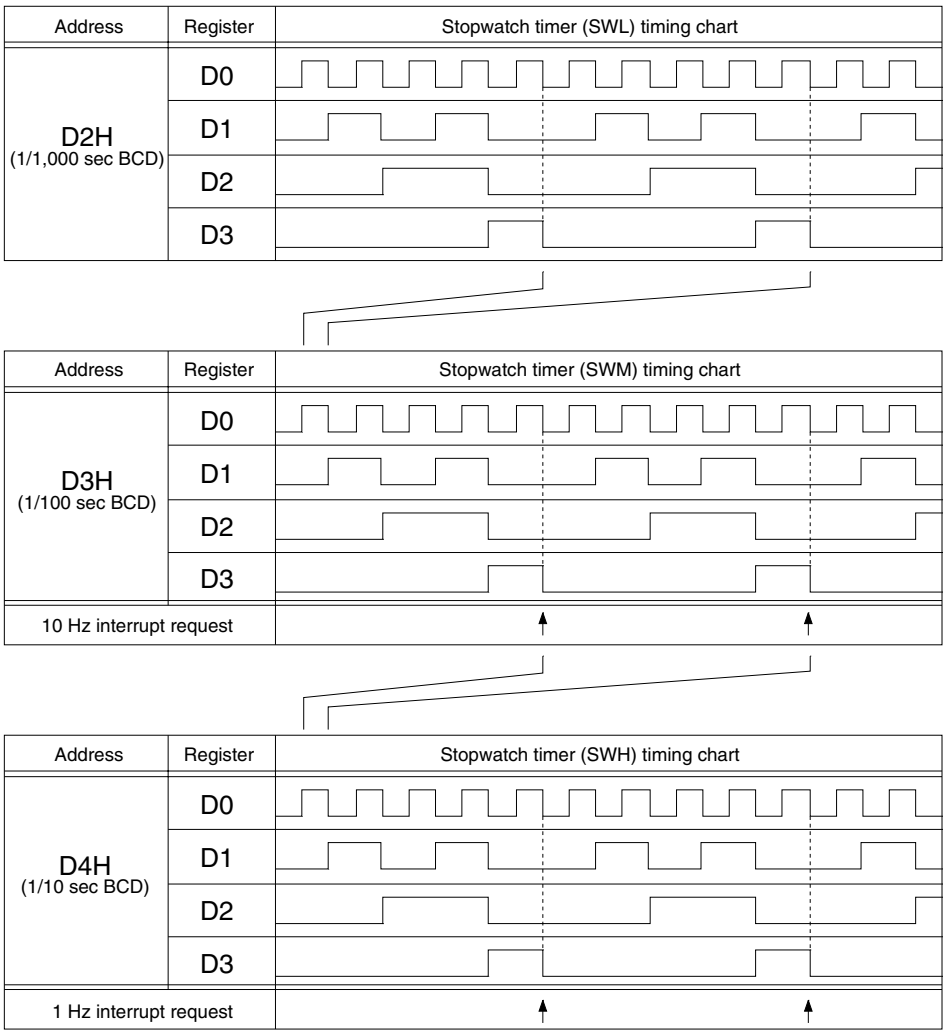


Fig. 4.10.6.1 Timing chart for counters

As shown in Figure 4.10.6.1, the interrupts are generated by the overflow of their respective counters ("9" changing to "0"). Also, at this time the corresponding interrupt factor flags (ISW0, ISW1) are set to "1". The respective interrupts can be masked separately through the interrupt mask registers (EISW0, EISW1). However, regardless of the setting of the interrupt mask registers, the interrupt factor flags are set to "1" by the overflow of their corresponding counters.

(2) Direct RUN and direct LAP interrupts

When the direct input function is selected, the direct RUN and direct LAP interrupts can be generated. The respective interrupts occur at the rising edge of the internal signal for direct RUN and direct LAP after sampling the direct input signal in the falling edge of 1,024 Hz signal. Also, at this time the corresponding interrupt factor flags (IRUN, ILAP) are set to "1".
The respective interrupts can be masked separately through the interrupt mask registers (EIRUN, EILAP). However, regardless of the setting of the interrupt mask registers, the interrupt factor flags are set to "1" by the inputs of the RUN and LAP.

The direct RUN function uses the K00 port and the direct LAP function uses the K01 port. Therefore, the direct input interrupt and the K00–K03 inputs interrupt may generate at the same time depending on the interrupt condition setting for the input port K00–K03. Consequently, when using the direct input interrupt, set the interrupt selection registers SIK00 and SIK01 to "0" so that the input interrupt does not generate by K00 and K01 inputs.

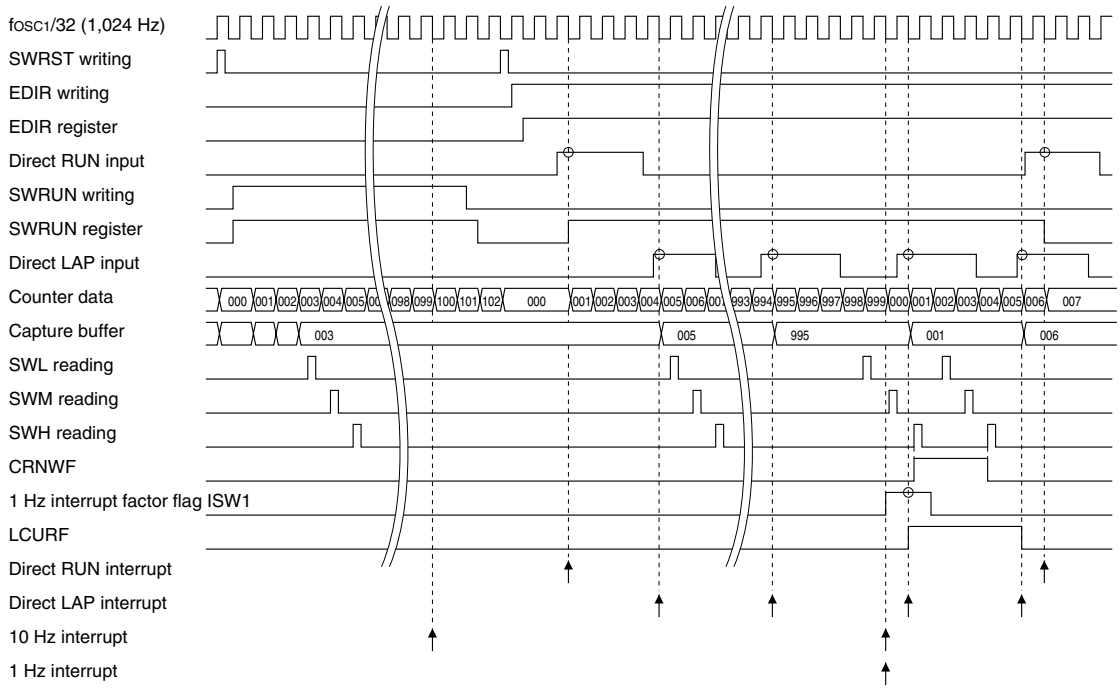


Fig. 4.10.6.2 Timing chart for stopwatch timer

4.10.7 Control of stopwatch timer

Table 4.10.7.1 lists the stopwatch timer control bits and their addresses.

Table 4.10.7.1 Control bits of stopwatch timer

Address *7	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
D0H	EDIR	DKM2	DKM1	DKM0	EDIR	0	Enable	Disable	Enable direct input function
					DKM2	0			Direct key mask factor 0: Non, 1: K02,
	R/W				DKM1	0			2: K02-03, 3: K02-03-10, 4: K10, 5: K10-11,
					DKM0	0			6: K10-11-12, 7: K10-11-12-13
D1H	LCURF	CRNWF	SWRUN	SWRST	LCURF	0	Reqest	No	Lap data carry-up request flag
					CRNWF	0	Renewal	No	Capture renewal flag
	R		R/W	W	SWRUN	0	Run	Stop	Stopwatch timer Run/Stop
					SWRST *5	Reset	Reset	–	Stopwatch timer reset
D2H	SWL3	SWL2	SWL1	SWL0	SWL3	0			MSB
					SWL2	0			Stopwatch timer data 1/1000 sec (BCD)
	R				SWL1	0			
					SWL0	0			LSB
D3H	SWM3	SWM2	SWM1	SWM0	SWM3	0			MSB
					SWM2	0			Stopwatch timer data 1/100 sec (BCD)
	R				SWM1	0			
					SWM0	0			LSB
D4H	SWH3	SWH2	SWH1	SWH0	SWH3	0			MSB
					SWH2	0			Stopwatch timer data 1/10 sec (BCD)
	R				SWH1	0			
					SWH0	0			LSB
F5H	EIRUN	EILAP	EISW1	EISW0	EIRUN	0	Enable	Mask	Interrupt mask register (Stopwatch direct RUN)
					EILAP	0	Enable	Mask	Interrupt mask register (Stopwatch direct LAP)
	R/W				EISW1	0	Enable	Mask	Interrupt mask register (Stopwatch 1 Hz)
					EISW0	0	Enable	Mask	Interrupt mask register (Stopwatch 10 Hz)
FDH	IRUN	ILAP	ISW1	ISW0	IRUN *4	0	Yes	No	Interrupt factor flag (Stopwatch direct RUN)
					ILAP *4	0	Yes	No	Interrupt factor flag (Stopwatch direct LAP)
	R				ISW1 *4	0	Yes	No	Interrupt factor flag (Stopwatch 1 Hz)
					ISW0 *4	0	Yes	No	Interrupt factor flag (Stopwatch 10 Hz)

*1 Initial value at the time of initial reset
*2 Not set in the circuit
*3 Undefined
*4 Reset (0) immediately after being read
*5 Constantly "0" when being read
*6 Refer to main manual
*7 Page switching in I/O memory is not necessary

SWL0–SWL3: Stopwatch timer data 1/1,000 sec (D2H)

Data (BCD) of the 1/1,000 sec column of the capture buffer can be read out.
The hold function of the capture buffer works by reading this data.
These 4 bits are read-only, and cannot be used for writing operations.
At initial reset, the timer data is set to "0".

SWM0–SWM3: Stopwatch timer data 1/100 sec (D3H)

Data (BCD) of the 1/100 sec column of the capture buffer can be read out. These 4 bits are read-only, and cannot be used for writing operations.
At initial reset, the timer data is set to "0".

SWH0–SWH3: Stopwatch timer data 1/10 sec (D4H)

Data (BCD) of the 1/10 sec column of the capture buffer can be read out. These 4 bits are read-only, and cannot be used for writing operations.
At initial reset, the timer data is set to "0".

Note: Be sure to data reading in the order of SWL→SWM→SWH.

EDIR: Direct input function enable register (D0H•D3)

Set the direct input (RUN/LAP) function to enable or disable.

When "1" is written: Enabled
When "0" is written: Disabled
Reading: Valid

The direct input function is set to enable by writing "1" to EDIR, and then RUN/STOP and LAP control can be done by external key input. When "0" is written, the direct input function is invalid, and the stopwatch timer is controlled by the software only.
Further the function switching is actually done by synchronizing with the falling edge of $f_{OSC1}/32$ (1,024 Hz) after the data is written to this register (after 977 µsec maximum).
At initial reset, this register is set to "0".

DKM2, DKM1, DKM0: Direct key mask factor setting (D0H•D2, D1, D0)

Selects a combination of the key inputs for concurrence judgment with RUN and LAP inputs when the direct input function is set.

Table 4.10.7.2 Key mask selection

DKM2	DKM1	DKM0	Mask key combination
0	0	0	None (at initial reset)
0	0	1	K02
0	1	0	K02, K03
0	1	1	K02, K03, K10
1	0	0	K10
1	0	1	K10, K11
1	1	0	K10, K11, K12
1	1	1	K10, K11, K12, K13

When the concurrence is detected, RUN and LAP inputs cannot be accepted until the concurrence is released.
At initial reset, these registers are set to "0".

SWRST: Stopwatch timer reset (D1H•D0)

This bit resets the stopwatch timer.

When "1" is written: Stopwatch timer reset
When "0" is written: No operation
Reading: Always "0"

The stopwatch timer is reset when "1" is written to SWRST. When the stopwatch timer is reset in the RUN status, operation restarts immediately. Also, in the STOP status the reset data is maintained.
Since this reset does not affect the capture buffer, the capture buffer data in hold status is not cleared and is maintained.
This bit is write-only, and is always "0" at reading.

SWRUN: Stopwatch timer RUN/STOP (D1H•D1)

This register controls the RUN/STOP of the stopwatch timer, and the operating status can be monitored by reading this register.

• ***When writing data***

When "1" is written: RUN
When "0" is written: STOP

The stopwatch timer enters the RUN status when "1" is written to SWRUN, and the STOP status when "0" is written.
In the STOP status, the timer data is maintained until the next RUN status or resets timer. Also, when the STOP status changes to the RUN status, the data that was maintained can be used for resuming the count.
RUN/STOP control with this register is valid only when the direct input function is set to disable. When the direct input function is set, it becomes invalid.

• ***When reading data***

When "1" is read: RUN
When "0" is read: STOP

Reading is always valid regardless of the direct input function setting. "1" is read when the stopwatch timer is in the RUN status, and "0" is read in the STOP status.
At initial reset, this register is set to "0".

LCURF: Lap data carry-up request flag (D1H•D3)

This flag indicates a carry that has been generated to 1 sec-digit when the data is held.

When "1" is read: Carry is required
When "0" is read: Carry is not required
Writing: Invalid

If the capture buffer shifts into hold status while the 1 Hz interrupt factor flag ISW1 is set to "1", LCURF is set to "1" to indicate that a carry-up to 1-sec digit is required. When performing a processing such as a LAP input preceding with 1 Hz interrupt processing, read this flag before processing and check whether carry-up is needed or not.
This flag is renewed (set/reset) every time the capture buffer shifts into hold status.
At initial reset, this flag is set to "0".

CRNWF: Capture renewal flag (D1H•D2)

This flag indicates that the content of the capture buffer has been renewed.

When "1" is read: Renewed
When "0" is read: Not renewed
Writing: Invalid

The content of the capture buffer is renewed if the LAP key is input when the data held into the capture buffer has not yet been read. Reading SWH in that status sets this flag to "1", and the hold status is maintained. Consequently, when data that is held by a LAP input is read, read this flag after reading the SWH and check whether the data has been renewed or not.
This flag is renewed when SWH is read.
At initial reset, this flag is set to "0".

EIRUN, EILAP, EISW1, EISW0: Interrupt mask registers (F5H)

These registers are used to select whether to mask the stopwatch timer interrupt.

When "1" is written: Enabled
When "0" is written: Masked
Reading: Valid

The interrupt mask registers EIRUN, EILAP, EISW1 and EISW0 are used to separately select whether to mask the direct RUN, direct LAP, 1 Hz and 10 Hz interrupts.
At initial reset, these registers are both set to "0".

IRUN, ILAP, ISW1, ISW0: Interrupt factor flags (FDH)

These flags indicate the status of the stopwatch timer interrupt.

When "1" is read: Interrupt has occurred
When "0" is read: Interrupt has not occurred
Writing: Invalid

The interrupt factor flags IRUN, ILAP, ISW0 and ISW1 correspond to the direct RUN, direct LAP, 1 Hz and 10 Hz interrupts respectively. With these flags, the software can judge whether a stopwatch timer interrupt has occurred. However, regardless of the interrupt mask register setting, these flags are set to "1" when the timing condition is established.
These flags are reset when read out by the software.
Reading of interrupt factor flags is available at EI, but be careful in the following cases.
If the interrupt mask register value corresponding to the interrupt factor flags to be read is set to "1", an interrupt request will be generated by the interrupt factor flags set timing, or an interrupt request will not be generated.
At initial reset, these flags are set to "0".

4.10.8 Programming notes

(1) The interrupt factor flag should be reset after resetting the stopwatch timer.

(2) Be sure to data reading in the order of SWL→SWM→SWH.

(3) When data that is held by a LAP input is read, read the capture buffer renewal flag CRNWF after reading the SWH and check whether the data has been renewed or not.

(4) When performing a processing such as a LAP input preceding with 1 Hz interrupt processing, read the LAP data carry-up request flag LCURF before processing and check whether carry-up is needed or not.

(5) When the interrupt factor flag ISW1 is set to "1", if reading it (reading FDH) before the capture buffer shifts into hold status, the LAP data carry-up request flag is not set to "1". Pay attention to the interrupt processing.

(6) Reading of interrupt factor flags is available at EI, but be careful in the following cases.
If the interrupt mask register value corresponding to the interrupt factor flags to be read is set to "1", an interrupt request will be generated by the interrupt factor flags set timing, or an interrupt request will not be generated.

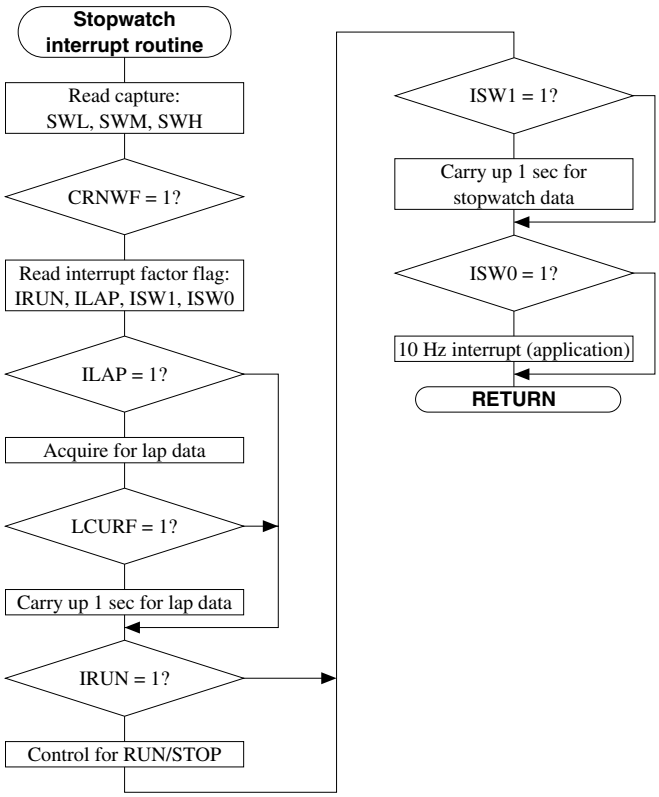


Fig. 4.10.8.1 Flow chart of stopwatch timer interrupt processing

4.11 Programmable Timer

4.11.1 Configuration of programmable timer

E0C6256 has a programmable timer which is configured with an 8 bits pre-settable down counter.
Aside from the count by the built-in clock (fOSC1/fOSC3), this programmable timer also possesses an event counter function that performs counting by making the signal input from the input port K02 as the clock.
The initial value of count data can be set by software to the reload register; at the point where the down-counter value is "0", the programmable timer reloads the initial value and continues to down-count.
In addition, the clock created by the underflow of the down counter can be output to the serial interface and to the output port R11.
Figure 4.11.1.1 shows the configuration of the programmable timer.

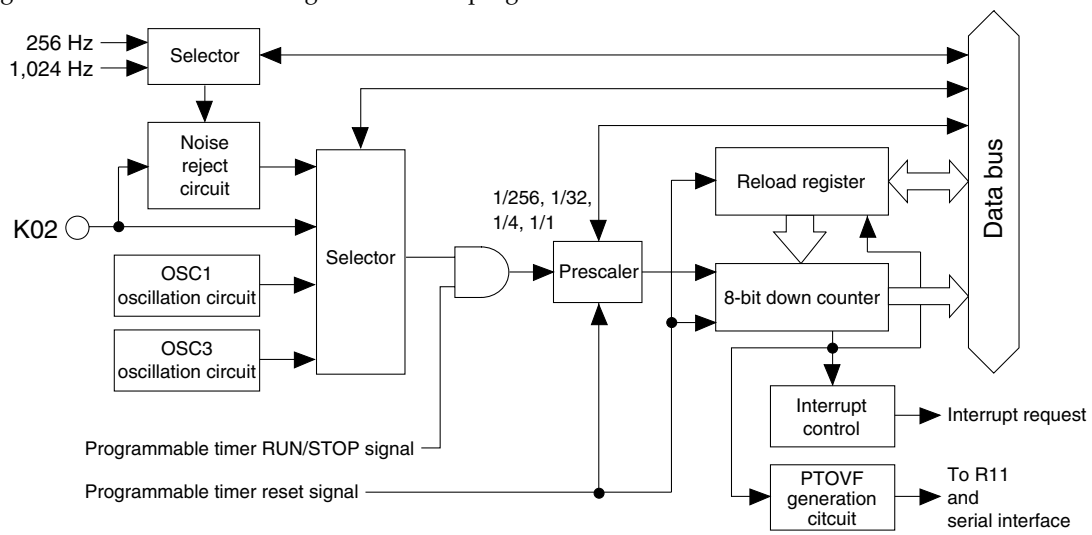


Fig. 4.11.1.1 Configuration of programmable timer

4.11.2 Input clock and prescaler

(1) Clock source selection

The counter clock source can be selected among four types shown in Table 4.11.2.1 by registers PTPC0 and PTPC1.

Table 4.11.2.1 Clock source selection

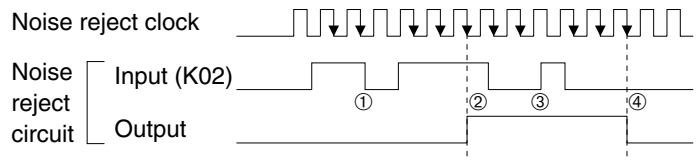
PTPC1	PTPC0	Clock source
0	0	fOSC1 (32 kHz)
0	1	fOSC3 (1 MHz)
1	0	K02 input (direct)
1	1	K02 input (with noise reject circuit)

fOSC1 and fOSC3 are the respective output clocks of the OSC1 and OSC3 oscillation circuit.
When using fOSC3, you must turn ON the OSC3 oscillation circuit in advance. If the OSC3 oscillation circuit is ON, counting can be done by fOSC3, even when the CPU clock is fOSC1.

The K02 input is an external input when used as an event counter and when K02 input (with noise rejecter) has been selected it passes through the noise reject circuit. In case such as when counting by a key input, this causes it to eliminate noise such as chattering.
This noise reject circuit can perform an input signal sampling using two types of frequencies 256 Hz or 1,024 Hz. Either frequency to be used can be selected by the register PNRFS. Further a signal less than 3 clocks of the selected frequency is regarded as noise, and it is not input as the count clock.

Table 4.11.2.2 Noise reject clock selection

PNRFS	Frequency	Sampling time
0	256 Hz	12 msec
1	1,024 Hz	3 msec



① High level is less than 3 clocks: the rising edge is not accepted
② High level is 3 clocks or more: the rising edge is accepted
③ Low level is less than 3 clocks: the falling edge is not accepted
④ Low level is 3 clocks or more: the falling edge is accepted

Fig. 4.11.2.1 Sampling timing of noise reject circuit

The K02 input (direct) is bypassed by this noise reject circuit. When it inputs a clock of 3 msec or less, you should select direct.

(2) Clock dividing ratio selection

For the programmable timer, the prescaler is established after the selector for the above mentioned clock source and the input clock dividing ratio can be selected from four types. As shown in Table 4.11.2.3, this selection can be done by registers PTPS0 and PTPS1.

Table 4.11.2.3 Clock dividing ratio selection

PTPS1	PTPS0	Dividing ratio
0	0	1/1
0	1	1/4
1	0	1/32
1	1	1/256

4.11.3 Operation of programmable timer

(1) Down-count

The 8-bit down counter counts down the divided input clock explained in the foregoing clause as the clock.
The down count timing becomes the falling edge of the clock.

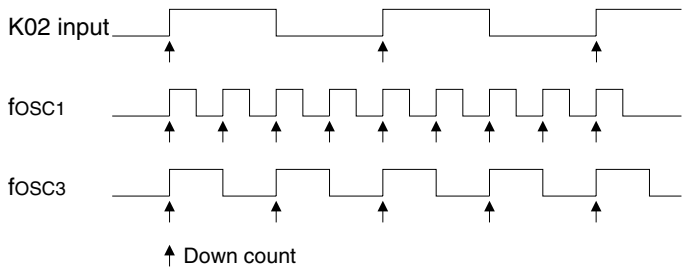


Fig. 4.11.3.1 Timing of down-counts

Run/Stop of the programmable timer can be controlled by register PTRUN.
When initiating programmable timer count, perform programming by the following steps:

1. Set the initial data to RD0–RD7.
2. Reset the programmable timer by writing "1" to PTRST.
3. Start the down-count by writing "1" to PTRUN.

(2) Data reload

The reload register (8 bits) for the initial value setting of the down counter is built into the programmable timer. The data set into the reload register is loaded into the down counter in the following instances and the count down is done from that value.

1. When the programmable timer has been reset by software
2. When the count down advances and the down counter becomes 00H

(3) Data reading

The low-order 4 bits of the down counter data is allocated to the address CDH and the high-order 4 bits are allocated to CEH and they can respectively be read.
At the time of this reading as well, the high-order data hold function operates the same as the clock timer. Refer to Section 4.9, "Clock Timer" for details of the hold function.

(4) PTOVF signal

The programmable timer generates a PTOVF signal by inverting the level each time the down counter becomes 00H.

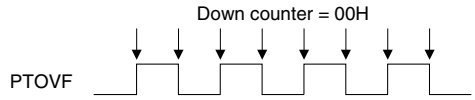


Fig. 4.11.3.2 PTOVF signal

The cycles (frequency) for this signal can be set according to the input clock, the dividing ratio and initial value that has been set for the reload register. The frequency of the output clock is indicated by the following expression.

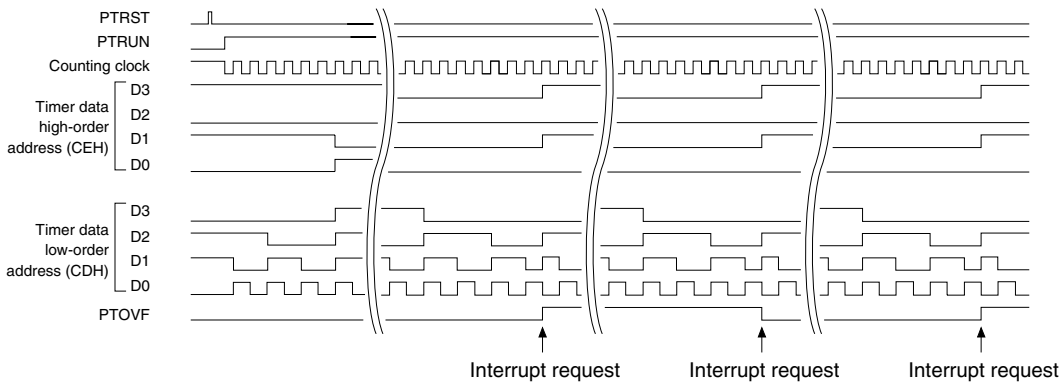
$fout = fin \times dv / (RD \times 2)$

fout: PTOVF frequency
fin: Input clock frequency
dv: Dividing ratio (1/256, 1/32, 1/4, 1/1)
RD: Reload data (1–256(0))

This PTOVF signal is input into the serial interface and can be used as the transfer clock. In addition, it can also be output externally through the output port R11.

4.11.4 Interrupt function

The programmable timer generates interrupt after the down-count from the initial setting is completed and the content of the down-counter indicates 00H.
After interrupt generation, the programmable timer reloads the initial count value into the down-counter and resumes counting.
Figure 4.11.4.1 shows the timing chart of the programmable timer.



Note: • When "A6H" is set into the reload register
• The counting clock is output of the prescaler

Fig. 4.11.4.1 Timing chart of programmable timer

When the down-counter values PT0–PT7 have become 00H the interrupt factor flag IPT is set to "1" and an interrupt is generated. The interrupt can be masked through the interrupt mask register EIPT. However, regardless of the setting of the interrupt mask register, the interrupt factor flag is set to "1" when the down-counter equals 00H.

4.11.5 Control of programmable timer

Table 4.11.5.1 lists the programmable timer control bits and their addresses.

Table 4.11.5.1 Control bits of programmable timer

Address *7	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
C8H	0	0	PTPS1	PTPS0	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R		R/W		PTPS1	0			Prog. timer prescaler selection
					PTPS0	0			0: 1/1, 1: 1/4, 2: 1/32, 3: 1/256
C9H	0	0	PTPC1	PTPC0	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R		R/W		PTPC1	0			Prog. timer prescaler clock source selection
					PTPC0	0			0: OSC1, 1: OSC3, 2: K02, 3: K02(NR)
CAH	PNRFS	PTOE	PTRUN	PTRST	PNRFS	0	1024Hz	256Hz	Noise rejector clock frequency selection
					PTOE	0	Enable	Disable	PTOVF output enable
	R/W			W	PTRUN	0	Run	Stop	Programmable timer Run/Stop
					PTRST *5	Rst (reload)	Rst (reload)	–	Programmable timer reset (reload)
CBH	RD3	RD2	RD1	RD0	RD3	0			MSB
					RD2	0			Programmable timer reload data
	R/W				RD1	0			(low-order 4 bits)
					RD0	0			LSB
CCH	RD7	RD6	RD5	RD4	RD7	0			MSB
					RD6	0			Programmable timer reload data
	R/W				RD5	0			(high-order 4 bits)
					RD4	0			LSB
CDH	PT3	PT2	PT1	PT0	PT3	0			MSB
					PT2	0			Programmable timer data
	R				PT1	0			(low-order 4 bits)
					PT0	0			LSB
CEH	PT7	PT6	PT5	PT4	PT7	0			MSB
					PT6	0			Programmable timer data
	R				PT5	0			(high-order 4 bits)
					PT4	0			LSB
F4H	0	0	0	EIPT	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R			R/W	0 *5	– *2			Unused
					EIPT	0	Enable	Mask	Interrupt mask register (Programmable timer)
FCH	0	0	0	IPT	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R				0 *5	– *2			Unused
					IPT *4	0	Yes	No	Interrupt factor flag (Programmable timer)

*1 Initial value at the time of initial reset
*2 Not set in the circuit
*3 Undefined
*4 Reset (0) immediately after being read
*5 Constantly "0" when being read
*6 Refer to main manual
*7 Page switching in I/O memory is not necessary

PTPC0, PTPC1: Prescaler clock source selection (C9H•D0, D1)

Selects the input clock for the prescaler.

Table 4.11.5.2 Clock source selection

PTPC1	PTPC0	Clock source
0	0	f_{OSC1} (32 kHz)
0	1	f_{OSC3} (1 MHz)
1	0	K02 input (direct)
1	1	K02 input (with noise reject circuit)

At initial reset, these registers are set to "0".

PNRFS: Noise reject clock frequency selection (CAH•D3)

Selects the noise reject frequency.

When "1" is written: 1,024 Hz
When "0" is written: 256 Hz
Reading: Valid

When K02 (with resistor) is selected as clock source, the frequency of the noise reject clock is selected from 1,024 Hz or 256 Hz. By writing "1" to PNRFS, 1,024 Hz is selected and K02 input signal more than 3 msec will be accepted. When "0" is written to PNRFS, 256 Hz is selected and K02 input signal more than 12 msec will be accepted.
At initial reset, this register is set to "0".

PTPS0, PTPS1: Prescaler dividing ratio selection (C8H•D0, D1)

Selects the dividing ratio for input clock.

Table 4.11.5.3 Clock dividing ratio selection

PTPS1	PTPS0	Dividing ratio
0	0	1/1
0	1	1/4
1	0	1/32
1	1	1/256

At initial reset, these registers are set to "0".

RD0–RD3, RD4–RD7: Reload register (CBH, CCH)

These are reload registers for setting the initial value of the timer.
Sets the low-order 4 bits of the 8 bits timer data to RD0–RD3, and the high-order 4 bits to RD4–RD7.
The set timer data is loaded to the down-counter when the programmable timer is reset or when the content of the down-counter is "00H".
When data of reload registers is set at "00H", the down-counter becomes a 256-value counter.
At initial reset, these registers are set to "0".

PTRST: Programmable timer reset (CAH•D0)

This bit resets the programmable timer.

When "1" is written: Programmable timer reset
When "0" is written: No operation
Reading: Always "0"

By writing "1" on PTRST, the programmable timer is reset.
The contents set in RD0–RD7 are loaded into the down-counter.
When the programmable timer is reset in the RUN mode, it will re-start counting immediately after loading and at STOP mode, the load data is maintained.
Because this bit is only for writing, it is always "0" during reading.

PTRUN: Programmable timer RUN/STOP (CAH•D1)

This register controls RUN/STOP of the programmable timer.

When "1" is written: RUN
When "0" is written: STOP
Reading: Valid

By writing "1" on PTRUN, the programmable timer performs counting operation. Writing "0" will make the programmable timer stop counting.
Even if the programmable timer is stopped, the timer data at that point is kept.
At initial reset, PTRUN is set to "0".

PT0–PT3, PT4–PT7: Programmable timer data (CDH, CEH)

Will read the data from the down-counter of the programmable timer.
Will read the low-order 4 bits of the 8 bits counter data PT0–PT3, and the high-order 4 bits PT4–PT7.
Because these 8 bits are only for reading, writing operation is rendered invalid.
By reading the low-order 4 bits, hold function works for the high-order 4 bits.
At initial reset, these registers are set to "0".

PTOE: PTOVF output enable (CAH•D2)
Controls the PTOVF output ON and OFF.

When "1" is written:	PTOVF output enable
When "0" is written:	PTOVF output disable (DC output)
Reading:	Valid

By writing "1" to PTOE when "0" has been set to the R11 register, the PTOVF signal is output from the R11 terminal. When "0" is written, the R11 terminal goes to a low (V_{SS}) level.
When R11 is used for DC output, keep PTOE register set to "0".
At initial reset, this register is set to "0".

EIPT: Interrupt mask register (F4H•D0)
This register is used to select whether to mask the programmable timer interrupt.

When "1" is written:	Enabled
When "0" is written:	Masked
Reading:	Valid

With this register, masking of the programmable timer can be selected.
At initial reset, this register is set to "0".

IPT: Interrupt factor flag (FCH•D0)
This is the interrupt factor flag of the programmable timer.

When "1" is read:	Interrupt has occurred
When "0" is read:	Interrupt has not occurred
Writing:	Invalid

From the status of this flag, the software can decide whether the programmable timer interrupt. Note, however, that even if the interrupt is masked, this flag will be set to "1" by the counter value will become "00H".
This flag is reset when read out by the software.
Reading of interrupt factor flags is available at EI, but be careful in the following cases.
If the interrupt mask register value corresponding to the interrupt factor flags to be read is set to "1", an interrupt request will be generated by the interrupt factor flags set timing, or an interrupt request will not be generated.
At initial reset, this flag is set to "0".

4.11.6 Programming notes

(1) Be sure to read the counter data in the order of low-order data (PT0–PT3) then high-order data (PT4–PT7).

(2) When data of reload registers is set at "00H", the down-counter becomes a 256-value counter.

(3) Set the V_{S1} voltage to -2.1 V (VSCHG = "1") when using the programmable timer as an event counter.

(4) Reading of interrupt factor flags is available at EI, but be careful in the following cases.
If the interrupt mask register value corresponding to the interrupt factor flags to be read is set to "1", an interrupt request will be generated by the interrupt factor flags set timing, or an interrupt request will not be generated.

4.12 Serial Interface (SIN, SOUT, SCLK, SRDY)

4.12.1 Configuration of serial interface

The E0C6256 has a synchronous clock type 8 bits serial interface built-in.
The configuration of the serial interface is shown in Figure 4.12.1.1.
The CPU, via the 8 bits shift register, can read the serial input data from the SIN terminal. Moreover, via the same 8 bits shift register, it can convert parallel data to serial data and output it to the SOUT terminal.
The synchronous clock for serial data input/output may be set by selecting by software any one of 3 types of master mode (internal clock mode: when the E0C6256 is to be the master for serial input/output) and a type of slave mode (external clock mode: when the E0C6256 is to be the slave for serial input/output).
Also, when the serial interface is used at slave mode, SRDY signal which indicates whether or not the serial interface is available to transmit or receive can be output to the SRDY terminal.

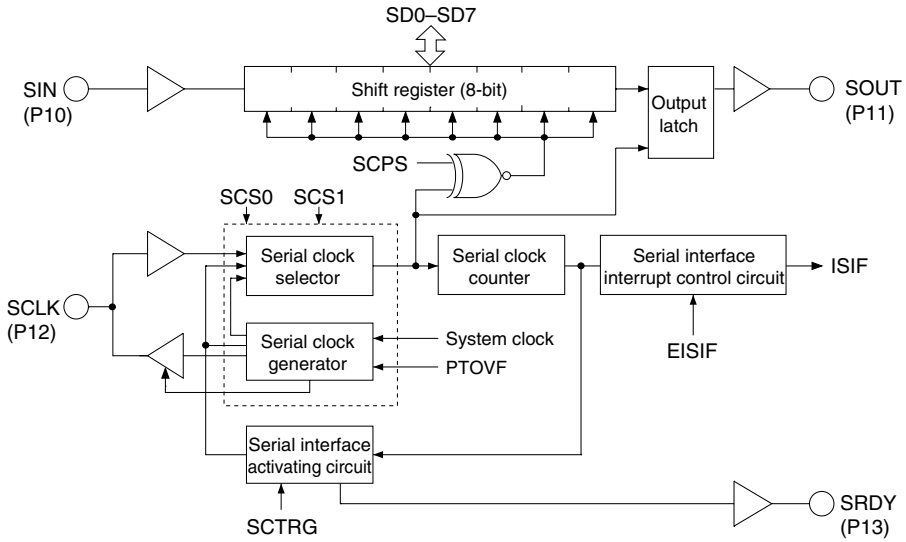


Fig. 4.12.1.1 Configuration of serial interface

The input/output ports of the serial interface are common used with the I/O ports P10–P13, and function of these ports can be selected through the software.
P10–P13 terminals and serial input/output correspondence are as follows:

Master mode	***Slave mode***
P10 = SIN (I)	P10 = SIN (I)
P11 = SOUT (O)	P11 = SOUT (O)
P12 = SCLK (O)	P12 = SCLK (I)
P13 = I/O port (I/O)	P13 = SRDY (O)

Note: At initial reset, P10–P13 are set to I/O ports.
When using the serial interface, switch the function (ESIF = "1") in the initial routine.

4.12.2 Master mode and slave mode of serial interface

The serial interface of the E0C6256 has two types of operation mode: master mode and slave mode.
In the master mode, it uses an internal clock as synchronous clock of the built-in shift register, generates this internal clock at the SCLK (P12) terminal and controls the external (slave side) serial device.
In the slave mode, the synchronous clock output from the external (master side) serial device is input from the SCLK (P12) terminal and uses it as the synchronous clock to the built-in shift register.
The master mode and slave mode are selected by writing data to registers SCS1 and SCS0.
When the master mode is selected, a synchronous clock may be selected from among 3 types as shown in Table 4.12.2.1.

Table 4.12.2.1 Synchronous clock selection

SCS1	SCS0	Mode	Synchronous clock
0	0	Slave mode	External clock
0	1	Master mode	PTOVF
1	0		CLK/2
1	1		CLK

CLK: CPU system clock
PTOVF: Programmable timer output clock (See Section 4.11.)

At initial reset, the slave mode (external clock mode) is selected.
Moreover, the synchronous clock, along with the input/output of the 8 bits serial data, is controlled as follows:

- At master mode, after output of 8 clocks from the SCLK (P12) terminal, clock output is automatically suspended and SCLK (P12) terminal is fixed at low level.
- At slave mode, after input of 8 clocks to the SCLK (P12) terminal, subsequent clock inputs are masked.

Note: When using the serial interface in the master mode, CPU system clock is used as the synchronous clock. Accordingly, when the serial interface is operating, system clock switching ($f_{OSC1} \leftrightarrow f_{OSC3}$) should not be performed.

A sample basic serial input/output portion connection is shown in Figure 4.12.2.1.

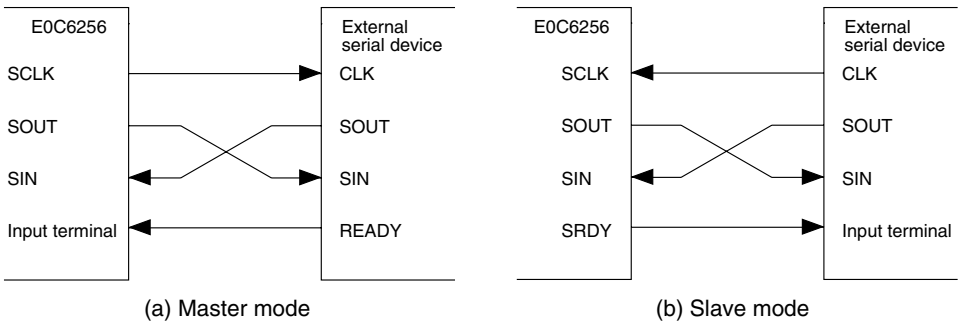


Fig. 4.12.2.1 Sample basic connection of serial input/output section

4.12.3 Data input/output and interrupt function

The serial interface of E0C6256 can input/output data via the internal 8 bits shift register. The shift register operates by synchronizing with either the synchronous clock output from SCLK (P12) terminal (master mode), or the synchronous clock input to SCLK (P12) terminal (slave mode).
The serial interface generates interrupt on completion of the 8 bits serial data input/output. Detection of serial data input/output is done by the counting of the synchronous clock SCLK; the clock completes input/output operation when 8 counts (equivalent to 8 cycles) have been made and then generates interrupt.
The serial data input/output procedure data is explained below:

(1) Serial data output procedure and interrupt

The E0C6256 serial interface is capable of outputting parallel data as serial data, in units of 8 bits.
By setting the parallel data to 4 bits registers SD0–SD3 (DAH) and SD4–SD7 (DBH) individually and writing "1" to SCTRG bit (D8H•D1), it synchronizes with the synchronous clock and serial data is output at the SOUT (P11) terminal. The synchronous clock used here is as follows: in the master mode, internal clock which is output to the SCLK (P12) terminal while in the slave mode, external clock which is input from the SCLK (P12) terminal. The serial data to the built-in shift register is shifted with the rising edge of the SCLK signal when SCSP register (D9H•D2) is "1" and is shifted with the falling edge of the SCLK signal when SCSP register is "0".

When the output of the 8 bits data from SD0 to SD7 is completed, the interrupt factor flag ISIF (FBH•D0) is set to "1" and interrupt is generated. Moreover, the interrupt can be masked by the interrupt mask register EISIF (F3H•D0). Note, however, that regardless of the setting of the interrupt mask register, the interrupt factor flag is set to "1" after output of the 8 bits data.

(2) Serial data input procedure and interrupt

The E0C6256 serial interface is capable of inputting serial data as parallel data, in units of 8 bits.
The serial data is input from the SIN (P10) terminal, synchronizes with the synchronous clock, and is sequentially read in the 8 bits shift register. As in the above item (1), the synchronous clock used here is as follows: in the master mode, internal clock which is output to the SCLK (P12) terminal while in the slave mode, external clock which is input from the SCLK (P12) terminal.
The serial data to the built-in shift register is read with the rising edge of the SCLK signal when SCPS register is "1" and is read with the falling edge of the SCLK signal when SCPS register is "0". Moreover, the shift register is sequentially shifted as the data is fetched.

When the input of the 8 bits data from SD0 to SD7 is completed, the interrupt factor flag ISIF is set to "1" and interrupt is generated. Moreover, the interrupt can be masked by the interrupt mask register EISIF. Note, however, that regardless of the setting of the interrupt mask register, the interrupt factor flag is set to "1" after input of the 8 bits data.

The data input in the shift register can be read from data registers SD0–SD7 by software.

(3) Serial data input/output permutation

E0C6256 allows the input/output permutation of serial data to be selected by register SDP (D9H•D3) as to either LSB first or MSB first. The block diagram showing input/output permutation in case of LSB first and MSB first is provided in Figure 4.12.3.1.

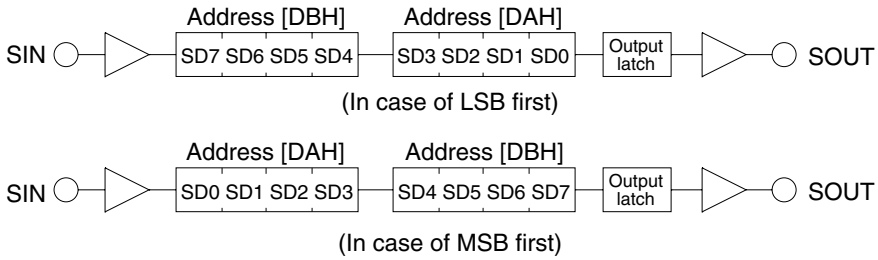


Fig. 4.12.3.1 Serial data input/output permutation

(4) SRDY signal

When the E0C6256 serial interface is used in the slave mode (external clock mode), SRDY is used to indicate whether the internal serial interface is available to transmit or receive data for the master side (external) serial device. SRDY signal is output from SRDY (P13) terminal.
SRDY signal becomes "1" (high) when the E0C6256 serial interface becomes available to transmit or receive data; normally, it is at "0" (low).
SRDY signal changes from "0" to "1" immediately after "1" is written to SCTRG and returns from "1" to "0" when "1" is input to SCLK (P12) terminal (i.e., when the serial input/output begins transmitting or receiving data). Moreover, when data is read from or written to SD4–SD7, the SRDY signal returns to "0".

(5) Timing chart

The E0C6256 serial interface timing chart is shown in Figure 4.12.3.2.

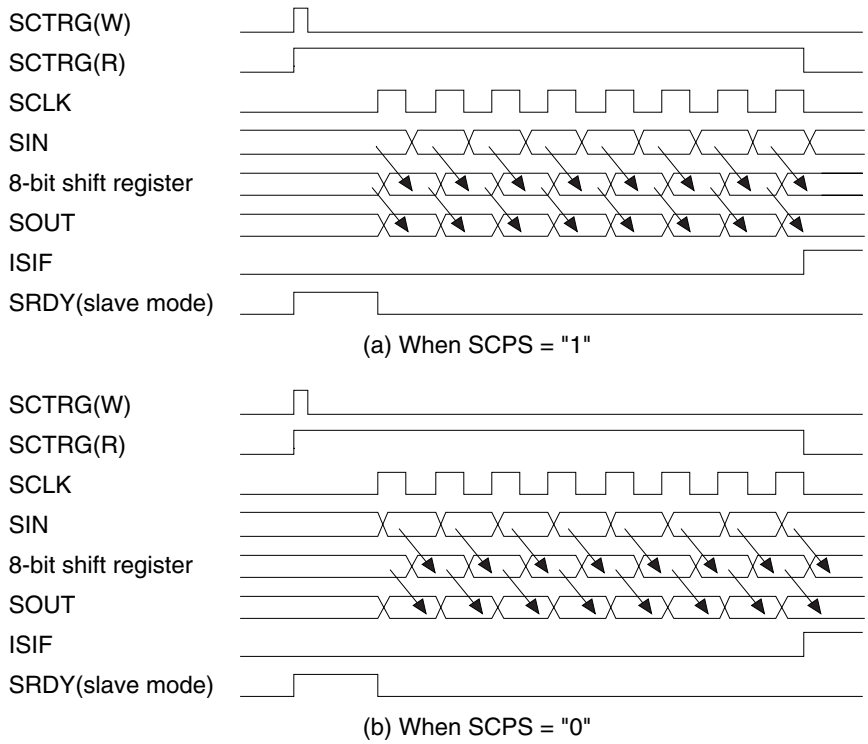


Fig. 4.12.3.2 Serial interface timing chart

4.12.4 Mask option

Since the input/output terminal of the serial interface is dual used with the I/O ports (P10–P13), the mask option that selects the output specification for the I/O port is also applied to the serial interface.

The output specification of the terminals SOUT, SCLK (during the master mode) and SRDY (during the slave mode) that is used as output in the input/output port of the serial interface is respectively selected by the mask options of P11, P12 and P13.
Either complementary output or P channel (Pch) open drain as output specification may be selected. However, even if Pch open drain has been selected, application on the terminal of voltage exceeding power source voltage is not permitted.

4.12.5 Control of serial interface

Table 4.12.5.1 list the serial interface control bits and their addresses.

Table 4.12.5.1 Control bits of serial interface

Address *7	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
D8H	0	0	SCTRG	ESIF	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R		R/W		SCTRG(W)	– *2	Trigger	–	Serial interface clock trigger (writing)
					SCTRG(R)	0	Run	Stop	Serial interface clock status (reading)
					ESIF	0	SIF port	I/O port	P1 port function selection
D9H	SDP	SCPS	SCS1	SCS0	SDP	0	LSB first	MSB first	Serial data input/output permutation
					SCPS	0	⌐	¬	Serial interface clock phase selection
	R/W				SCS1	0			Serial interface clock mode selection
					SCS0	0			0: Slave, 1: PTOVF, 2: CLK/2, 3: CLK
DAH	SD3	SD2	SD1	SD0	SD3	– *3			MSB
					SD2	– *3			Serial interface data (low-order 4 bits)
	R/W				SD1	– *3			
					SD0	– *3			LSB
DBH	SD7	SD6	SD5	SD4	SD7	– *3			MSB
					SD6	– *3			Serial interface data (high-order 4 bits)
	R/W				SD5	– *3			
					SD4	– *3			LSB
B5H	PUL13	PUL12	PUL11	PUL10	PUL13	1	On	Off	Master mode: P13 pull down control register
					PUL13	1	1	0	Slave mode: General-purpose register
					PUL12	1	1	0	Master mode: General-purpose register
	R/W				PUL12	1	On	Off	Slave mode: SCKL pull down control register
					PUL11	1	1	0	General-purpose register
					PUL10	1	On	Off	SIN pull down control register
F3H	0	0	0	EISIF	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R			R/W	0 *5	– *2			Unused
					EISIF	0	Enable	Mask	Interrupt mask register (Serial interface)
FBH	0	0	0	ISIF	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R				0 *5	– *2			Unused
					ISIF *4	0	Yes	No	Interrupt factor flag (Serial interface)

*1 Initial value at the time of initial reset
*2 Not set in the circuit
*3 Undefined
*4 Reset (0) immediately after being read
*5 Constantly "0" when being read
*6 Refer to main manual
*7 Page switching in I/O memory is not necessary

ESIF: P1 port function selection (D8H•D0)

Sets P10–P13 to the input/output port for the serial interface.

When "1" is written: Serial interface
When "0" is written: I/O port
Reading: Valid

P10, P11, P12 and P13 will function as SIN, SOUT, SCLK, SRDY, respectively.
In the slave mode, the R13 terminal functions as SRDY output terminal, and in the master mode, it functions as the I/O port terminal.
At initial reset, this register is set to "0".

PUL10, PUL12: Pull down control registers (B5H•D0, D2)

Sets the pull down of SIN terminal and SCLK terminal (in the slave mode).

When "1" is written: Pull down ON
When "0" is written: Pull down OFF
Reading: Valid

Sets the pull down resistor built into the SIN (P10) and SCLK (P12) ports to ON or OFF. SCLK pull down is effective during the slave mode.
At initial reset, these registers are set to "1" and pull down goes ON.

SCS0, SCS1: Synchronous clock selection (D9H•D0, D1)

Selects the synchronous clock for the serial interface (SCLK).

Table 4.12.5.2 Synchronous clock selection

SCS1	SCS0	Mode	Synchronous clock
0	0	Slave mode	External clock
0	1	Master mode	PTOVF
1	0		CLK/2
1	1		CLK

CLK: CPU system clock

PTOVF: Programmable timer output clock (See Section 4.11.)

Synchronous clock (SCLK) is selected from among the above 4 types: 3 types of internal clock and external clock.
When using the serial interface in the master mode, CPU system clock is used as the synchronous clock. Accordingly, when the serial interface is operating, system clock switching ($f_{OSC1} \leftrightarrow f_{OSC3}$) should not be performed.
Also, when PTOVF is used, it is necessary to generate a clock on the programmable timer side prior to sending and receiving.
At initial reset, external clock is selected.

SCPS: Shift clock phase selection (D9H•D2)

Selects the timing for reading in the serial data input from SIN (P10) terminal.

When "1" is written: Rising edge of SCLK
When "0" is written: Falling edge of SCLK
Reading: Valid

Selects whether the fetching for the serial input data to registers (SD0–SD7) at the rising edge (at "1" writing) or falling edge (at "0" writing) of the SCLK signal.
The input data fetching timing may be selected but output timing for output data is fixed at SCLK rising edge.
When the internal clock is selected as the synchronous clock (SCLK), a hazard occurs in the synchronous clock (SCLK) when data is written to register SCPS.
At initial reset, this register is set to "0".

SDP: Data input/output permutation selection (D9H•D3)

Selects the serial data input/output permutation.

When "1" is written: LSB first
When "0" is written: MSB first
Reading: Valid

Select whether the data input/output permutation will be MSB first or LSB first.
At initial reset, this register is set to "0".

SCTRG: Clock trigger/status (D8H•D1)

This is a trigger to start input/output of synchronous clock (SCLK).

• ***During writing operation***

When "1" is written: Trigger
When "0" is written: No operation

When this trigger is supplied to the serial interface activating circuit, the synchronous clock (SCLK) input/output is started.
As a trigger condition, it is required that data writing or reading on data registers SD0–SD7 be performed prior to writing "1" to SCTRG. (The internal circuit of the serial interface is initiated through data writing/reading on data registers SD0–SD7.)
Supply trigger only once every time the serial interface is placed in the RUN state. Refrain from performing trigger input multiple times, as leads to malfunctioning.
Moreover, when the synchronous clock SCLK is external clock, start to input the external clock after the trigger.

• ***During reading operation***

When "1" is read: RUN status
When "0" is read: STOP status
Writing: Invalid

When read out this bit, it indicates the status of serial interface clock.
After "1" is written to SCTRG, this value is latched till serial interface clock stops (8 clock counts). Therefore, if "1" is read, it indicates that the synchronous clock is in input/output operation.
When the synchronous clock input/output is completed, this latch is reset to "0".
At initial reset, this register is set to "0".

SD0–SD3, SD4–SD7: Serial interface data register (DAH, DBH)

These registers are used for writing and reading serial data.

• ***During writing operation***

When "1" is written: High level
When "0" is written: Low level

Writes serial data will be output to SOUT (P11) terminal. From the SOUT (P11) terminal, the data converted to serial data as high (V_{DD}) level bit for bits set at "1" and as low (V_{SS}) level bit for bits set at "0".

• ***During reading operation***

When "1" is read: High level
When "0" is read: Low level

The serial data input from the SIN (P10) terminal can be read by this register.
The data converted to parallel data, as high (V_{DD}) level bit "1" and as low (V_{SS}) level bit "0" input from SIN (P10) terminal. Perform data reading only while the serial interface is halted (i.e., the synchronous clock is neither being input or output).

At initial reset, these registers will be undefined.

EISIF: Interrupt mask register (F3H•D0)

This is the interrupt mask register of the serial interface.

When "1" is written: Enabled
When "0" is written: Masked
Reading: Valid

With this register, masking of the serial interface interrupt can be selected.
At initial reset, this register is set to "0".

ISIF: Interrupt factor flag (FBH•D0)

This is the interrupt factor flag of the serial interface.

When "1" is read: Interrupt has occurred
When "0" is read: Interrupt has not occurred
Writing: Invalid

From the status of this flag, the software can decide whether the serial interface interrupt.
The interrupt factor flag is reset when it has been read out.
Note, however, that even if the interrupt is masked, this flag will be set to "1" after the 8 bits data input/output.
Reading of interrupt factor flags is available at EI, but be careful in the following cases.
If the interrupt mask register value corresponding to the interrupt factor flags to be read is set to "1", an interrupt request will be generated by the interrupt factor flags set timing, or an interrupt request will not be generated.
At initial reset, this flag is set to "0".

4.12.6 Programming notes

(1) When using the serial interface in the master mode, the synchronous clock uses the CPU system clock. Accordingly, do not change the system clock ($f_{OSC1} \leftrightarrow f_{OSC3}$) while the serial interface is operating.

(2) Perform data writing/reading to data registers SD0–SD7 only while the serial interface is halted (i.e., the synchronous clock is neither being input or output).

(3) As a trigger condition, it is required that data writing or reading on data registers SD0–SD7 be performed prior to writing "1" to SCTRG. (The internal circuit of the serial interface is initiated through data writing/reading on data registers SD0–SD7.) Supply trigger only once every time the serial interface is placed in the RUN state. Moreover, when the synchronous clock SCLK is external clock, start to input the external clock after the trigger.

(4) Set the V_{S1} voltage to -2.1 V (VSCHG = "1") when using the serial interface in slave mode.

(5) Reading of interrupt factor flags is available at EI, but be careful in the following cases.
If the interrupt mask register value corresponding to the interrupt factor flags to be read is set to "1", an interrupt request will be generated by the interrupt factor flags set timing, or an interrupt request will not be generated.

4.13 Sound Generator

4.13.1 Configuration of sound generator

The E0C6256 has a built-in sound generator for generating buzzer signals.
Hence, generated buzzer signals (BZ) can be output from the R12 terminal.
Aside permitting the respective setting of the buzzer signal frequency and sound level to 8 stages, it permits the adding of a digital envelope by means of duty ratio control. It also has a one-shot output function for outputting key operated sounds.
Figure 4.13.1.1 shows the configuration of the sound generator.

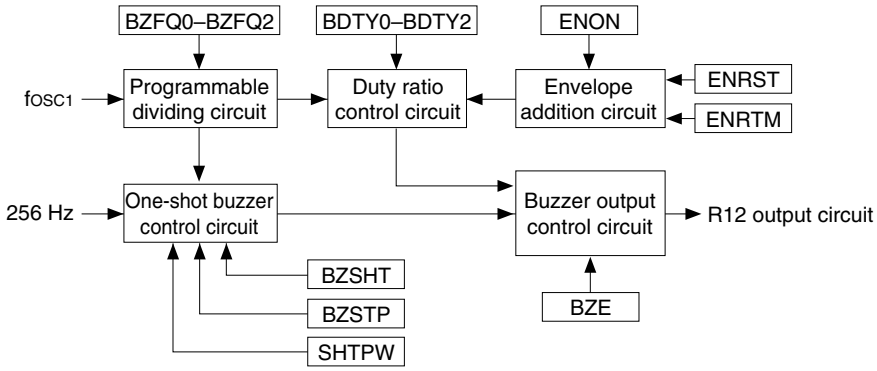


Fig. 4.13.1.1 Configuration of sound generator

4.13.2 Control of buzzer output

A buzzer (BZ) signal can be output from the output port terminal R12.
The configuration of the buzzer output port is shown in Figure 4.13.2.1.

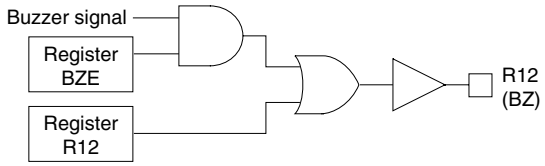


Fig. 4.13.2.1 Configuration of buzzer output port

The BZ signal generated by the sound generator is output from the R12 terminal by setting "1" for the buzzer output enable register BZE when the output port register R12 is set to"0". When "0" is set to BZE, the R12 terminal shifts to the low (VSS) level.

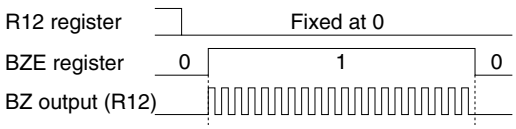


Fig. 4.13.2.2 Buzzer signal output timing chart

Note:
- *Pay attention to the output because it is fixed at HIGH level when the R12 register is set to "1".*
- *Since it generates a BZ signal that is out of synchronization with the BZE register, hazards may at times be produced when the signal goes ON/OFF due to the setting of the register.*

4.13.3 Setting of buzzer frequency and sound level

The divide signal of the OSC1 clock (32.768 kHz) is used for the buzzer (BZ) signal and it is set up such that 8 types of frequencies can be selected by changing this dividing ratio. Frequency selection is done by setting the buzzer frequency selection registers BZFQ0–BZFQ2 as shown in Table 4.13.3.1.

Table 4.13.3.1 Buzzer signal frequency setting

BZFQ2	BZFQ1	BZFQ0	Buzzer frequency (Hz)
0	0	0	4096.0
0	0	1	3276.8
0	1	0	2730.7
0	1	1	2340.6
1	0	0	2048.0
1	0	1	1638.4
1	1	0	1365.3
1	1	1	1170.3

The buzzer sound level is changed by controlling the duty ratio of the buzzer signal.
The duty ratio can be selected from among the 8 types shown in Table 4.13.3.2 according to the setting of the buzzer duty selection registers BDTY0–BDTY2.

Table 4.13.3.2 Duty ratio setting

Level	BDTY2	BDTY1	BDTY0	Duty ratio by buzzer frequency (Hz)			
				4096.0	3276.8	2730.7	2340.6
				2048.0	1638.4	1365.3	1170.3
Level 1 (maximum)	0	0	0	8/16	8/20	12/24	12/28
Level 2	0	0	1	7/16	7/20	11/24	11/28
Level 3	0	1	0	6/16	6/20	10/24	10/28
Level 4	0	1	1	5/16	5/20	9/24	9/28
Level 5	1	0	0	4/16	4/20	8/24	8/28
Level 6	1	0	1	3/16	3/20	7/24	7/28
Level 7	1	1	0	2/16	2/20	6/24	6/28
Level 8 (minimum)	1	1	1	1/16	1/20	5/24	5/28

When the HIGH level output time has been made TH and when the LOW level output time has been made TL due to the ratio of the pulse width to the pulse synchronization, the duty ratio becomes TH/(TH+TL).
When BDTY0–BDTY2 have all been set to "0", the duty ratio becomes maximum and the sound level also becomes maximum. Conversely, when BDTY0–BDTY2 have all been set to "1", the duty ratio becomes minimum and the sound level also becomes minimum.
The duty ratio that can be set is different depending on the frequency that has been set, so see Table 4.13.3.2.

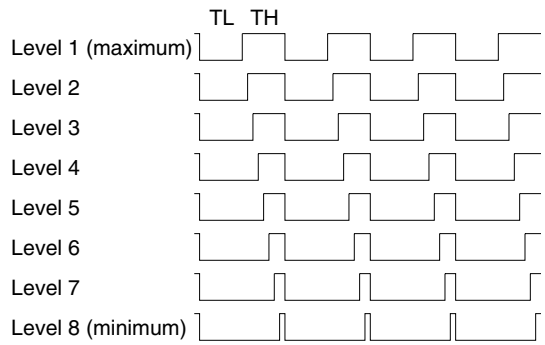


Fig. 4.13.3.1 Duty ratio of the buzzer signal waveform

Note: When a digital envelope has been added to the buzzer signal, the BDTY0–BDTY2 settings will be invalid due to the control of the duty ratio.

4.13.4 Digital envelope

A digital envelope for duty control can be added to the buzzer signal.
The envelope can be controlled by staged changing of the same duty envelope as detailed in Table 4.13.3.2 in the preceding item from level 1 (maximum) to level 8 (minimum).
The addition of an envelope to the buzzer signal can be done by writing "1" into ENON, but when "0" has been written it is not added.
When a buzzer signal output is begun (writing "1" into BZE) after setting ENON, the duty ratio shifts to level 1 (maximum) and changes in stages to level 8.
When attenuated down to level 8 (minimum), it is retained at that level. The duty ratio can be returned to maximum, by writing "1" into register ENRST during output of a envelope attached buzzer signal.
The envelope attenuation time (time for changing of the duty ratio) can be selected by the register ENRTM. The time for a 1 stage level change is 62.5 msec (16 Hz), when "0" has been written into ENRTM and 125 msec (8 Hz), when to "1" has been written. However, there is also a max. 4 msec error from envelope ON, up to the first change.
Figure 4.13.4.1 Shows the timing chart of the digital envelope.

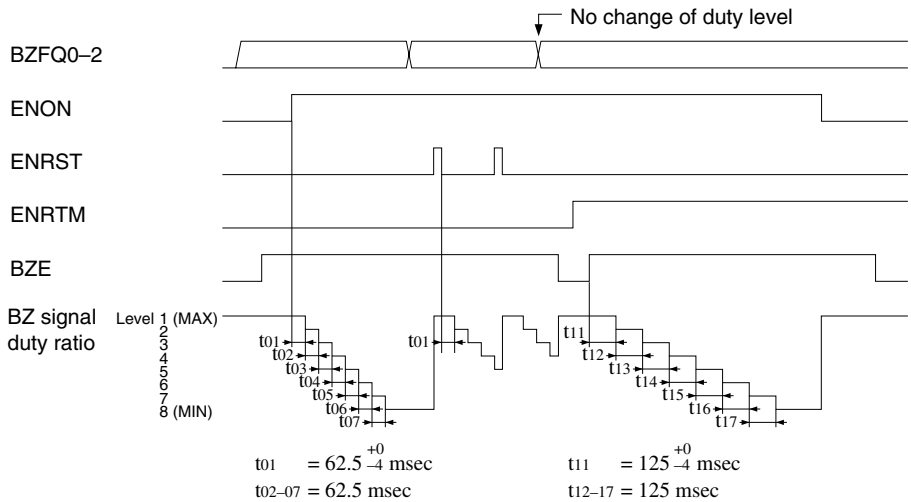


Fig. 4.13.4.1 Timing chart for digital envelope

4.13.5 One-shot output

The sound generator has a one-shot output function for outputting a short duration buzzer signal for key operation sounds and similar effects. Either 125 msec or 31.25 msec can be selected by register SHTPW for buzzer signal output time.
The output of the one-shot buzzer is controlled by writing "1" into the one-shot buzzer trigger BZSHT. When this trigger has been assigned, a buzzer signal in synchronization with the internal 256 Hz signal is output from the BZ (R12) terminal. Thereafter, when the set time has elapsed, a buzzer signal in synchronization with the 256 Hz signal goes off in the same manner as for the start of output.
The BZSHT also permits reading. When BZSHT is "1", the one-shot output circuit is in operation (during one-shot output) and when it is "0", it shows that the circuit is in the ready (outputtable) status.

In addition, it can also terminate one-shot output prior to the elapsing of the set time. This is done by writing a "1" into the one-shot buzzer stop BZSTP. In this case as well, the buzzer signal goes OFF in synchronization with the 256 Hz signal.

The one-shot output cannot add an envelope for short durations. However, the sound level can be set by selecting the duty ratio, and the frequency can also be set.
One-shot output is invalid during normal buzzer output.

Figure 4.13.5.1 shows timing chart for one-shot output.

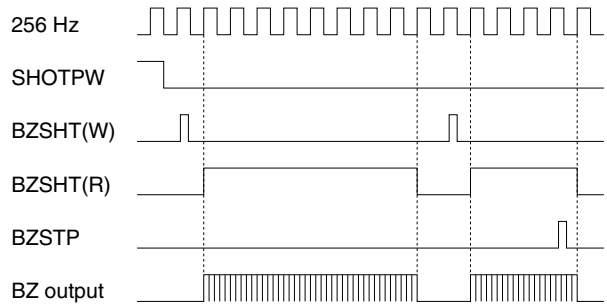


Fig. 4.13.5.1 Timing chart for one-shot output

4.13.6 Control of sound generator

Table 4.13.6.1 lists the control bits and their addresses for the sound generator.

Table 4.13.6.1 Control bits of sound generator

Address *7	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
DCH	ENRTM	ENRST	ENON	BZE	ENRTM	0	1sec	0.5sec	Envelope releasing time
					ENRST *5	Reset	Reset	–	Envelope reset
	R/W	W	R/W		ENON	0	On	Off	Envelope On/Off
					BZE	0	Enable	Disable	Buzzer output enable
DDH	0	BZSTP	BZSHT	SHTPW	0 *5	– *2			Unused
					BZSTP *5	– *2	Stop	–	1-shot buzzer stop
					BZSHT(W)	– *2	Trigger	–	1-shot buzzer trigger (writing)
	R	W	R/W		BZSHT(R)	0	Busy	Ready	1-shot buzzer status (reading)
					SHTPW	0	125msec	31.25msec	1-shot buzzer pulse width setting
DEH	0	BZFQ2	BZFQ1	BZFQ0	0 *5	– *2			Unused
					BZFQ2	0			Buzzer frequency selection
	R	R/W			BZFQ1	0			0: 4096.0, 1: 3276.8, 2: 2730.7, 3: 2340.6,
					BZFQ0	0			4: 2048.0, 5: 1638.4, 6: 1365.3, 7: 1170.3 (Hz)
DFH	0	BDTY2	BDTY1	BDTY0	0 *5	– *2			Unused
					BDTY2	0			Buzzer signal duty ratio selection *6
	R	R/W			BDTY1	0			
					BDTY0	0			
A3H	R13	R12	R11	R10	R13	0	High	Low	Output port (R13)
					R12	0	High	Low	Output port (R12)
		BZ	PTOVF	FOUT	BZ	0	Off	On	Buzzer output
	R/W				R11	0	High	Low	Output port (R11)
					PTOVF	0	Off	On	PTOVF output
					R10	0	High	Low	Output port (R10)
					FOUT	0	Off	On	FOUToutput

*1 Initial value at the time of initial reset
*2 Not set in the circuit
*3 Undefined
*4 Reset (0) immediately after being read
*5 Constantly "0" when being read
*6 Refer to main manual
*7 Page switching in I/O memory is not necessary

R12: Output port data register (A3H•D2)

Fix it at "0" when performing the buzzer signal (BZ) output.
At initial reset, this register is set to "0".

BZE: BZ output enable register (DCH•D0)

Controls the buzzer (BZ) signal output.

When "1" is written: BZ signal output enable
When "0" is written: BZ signal output disable
Reading: Valid

By writing "1" to BZE when the R12 register is set to "0", the BZ signal is output from the R12 terminal. When "0" is written, R12 terminal becomes the LOW (V_{SS}) level.
When the R12 port is used as the DC output, fix this register at "0".
At initial reset, this register is set to "0".

BZFQ0–BZFQ2: Buzzer frequency selection (DEH•D0–D2)

Selects the buzzer signal frequency.

Table 4.13.6.2 Buzzer signal frequency setting

BZFQ2	BZFQ1	BZFQ0	Buzzer frequency (Hz)
0	0	0	4096.0
0	0	1	3276.8
0	1	0	2730.7
0	1	1	2340.6
1	0	0	2048.0
1	0	1	1638.4
1	1	0	1365.3
1	1	1	1170.3

Select the buzzer frequency from among the above 8 types that have divided the OSC1 clock.
At initial reset, these registers are set to "0".

BDTY0–BDTY2: Duty level selection (DFH•D0–D2)

Selects the duty ratio of the buzzer signal as shown in Table 4.13.6.3.

Table 4.13.6.3 Duty ratio setting

Level	BDTY2	BDTY1	BDTY0	Duty ratio by buzzer frequency (Hz)			
				4096.0	3276.8	2730.7	2340.6
				2048.0	1638.4	1365.3	1170.3
Level 1 (maximum)	0	0	0	8/16	8/20	12/24	12/28
Level 2	0	0	1	7/16	7/20	11/24	11/28
Level 3	0	1	0	6/16	6/20	10/24	10/28
Level 4	0	1	1	5/16	5/20	9/24	9/28
Level 5	1	0	0	4/16	4/20	8/24	8/28
Level 6	1	0	1	3/16	3/20	7/24	7/28
Level 7	1	1	0	2/16	2/20	6/24	6/28
Level 8 (minimum)	1	1	1	1/16	1/20	5/24	5/28

The sound level of this buzzer can be set by selecting this duty ratio.
However, when the envelope has been set to ON (ENON = "1"), this setting becomes invalid.
At initial reset, these registers are set to "0".

ENRST: Envelope reset (DCH•D2)

Resets the envelope.

When "1" is written: Reset
When "0" is written: No operation
Reading: Always "0"

Writing "1" into ENRST resets envelope and the duty ratio becomes maximum. If an envelope has not been added (ENON = "0") and if no buzzer signal is being output, the reset becomes invalid. Writing "0" is also invalid.
This bit is dedicated for writing, and is always "0" for reading.

ENON: Envelope ON/OFF (DCH•D1)

Controls the addition of an envelope onto the buzzer signal.

When "1" is written: ON
When "0" is written: OFF
Reading: Valid

Writing "1" into the ENON causes an envelope to be added during buzzer signal output. When a "0" has been written, an envelope is not added.
At initial reset, this register is set to "0".

ENRTM: Envelope releasing time selection (DCH•D3)
Selects the envelope releasing time that is added to the buzzer signal.

When "1" is written: 1.0 sec (125 msec × 7 = 875 msec)
When "0" is written: 0.5 sec (62.5 msec × 7 = 437.5 msec)
Reading: Valid

The releasing time of the digital envelope is determined by the time for converting the duty ratio.
When "1" has been written in ENRTM, it becomes 125 msec (8 Hz) units and when "0" has been written, it becomes 62.5 msec (16 Hz) units.
At initial reset, this register is set to "0".

SHTPW: One-shot buzzer pulse width setting (DDH•D0)
Selects the output time of the one-shot buzzer.

When "1" is written: 125 msec
When "0" is written: 31.25 msec
Reading: Valid

Writing "1" into SHTPW causes the one-short output time to be set at 125 msec, and writing "0" causes it to be set to 31.25 msec. It does not affect normal buzzer output.
At initial reset, this register is set to "0".

BZSHT: One-shot buzzer trigger/status (DDH•D1)
Controls the one-shot buzzer output.

• ***During writing operation***
When "1" is written: Trigger
When "0" is written: No operation

Writing "1" into BZSHT causes the one-short output circuit to operate and a buzzer signal to be output. This output is automatically turned OFF after the time set by SHTPW has elapsed. At this time, the R12 register has to be set to "0".
The one-shot output is only valid when the normal buzzer output is OFF (BZE = "0") and will be invalid when the normal buzzer output is ON (BZE = "1"). When a re-trigger is assigned during a one-shot output, the one-shot output time set with SHTPW is measured again from that point (time extension).

• ***During reading operation***
When "1" is read: BUSY
When "0" is read: READY

During reading BZSHT shows the operation status of the one-shot output circuit. During one-shot output, BZSHT becomes "1" and the output goes OFF, it shifts to "0".
At initial reset, this bit is set to "0".

BZSTP: One-shot buzzer stop (DDH•D2)
Stop the one-shot buzzer output.

When "1" is written: Stop
When "0" is written: No operation
Reading: Always "0"

Writing "1" into BZSTP permits the one-shot buzzer output to be turned OFF prior to the elapsing of the time set by SHTPW. Writing "0" is invalid and writing "1" is also invalid except during one-shot output. This bit is dedicated for writing, and is always "0" for reading.

4.13.7 Programming notes

(1) Pay attention to the output because it is fixed at HIGH level when the R12 register is set to "1".

(2) Since it generates a BZ signal that is out of synchronization with the BZE register, hazards may at times be produced when the signal goes ON/OFF due to the setting of the register.

(3) The one-shot output is only valid when the normal buzzer output is OFF (BZE = "0") and will be invalid when the normal buzzer output is ON (BZE = "1").

4.14 A/D Converter

4.14.1 Configuration of A/D converter

The E0C6256 has CR oscillation type A/D converter.
Two systems (channel 0 and channel 1) of CR oscillation circuit are built into this A/D converter, so it is possible to compose two types of A/D conversion circuits by connecting different sensors to each CR oscillation circuit.
Channel 0 can be used as an R/f (resistor/frequency) conversion circuit using a resistive sensor such as a thermistor, and channel 1 can be used as an R/f conversion circuit same as channel 0, or an R/f conversion circuit for humidity conversion using a resistive humidity sensor.
The channel to be used and sensor type for channel 1 are selected using software.
The built-in up counter counts data that is converted into frequency by the CR oscillation circuit. By reading the counted value, digital converted data can be obtained.
Various sensor circuits such as temperature/humidity measurement circuits can be easily realized using this A/D converter.
The configuration of the A/D converter is shown in Figure 4.14.1.1.

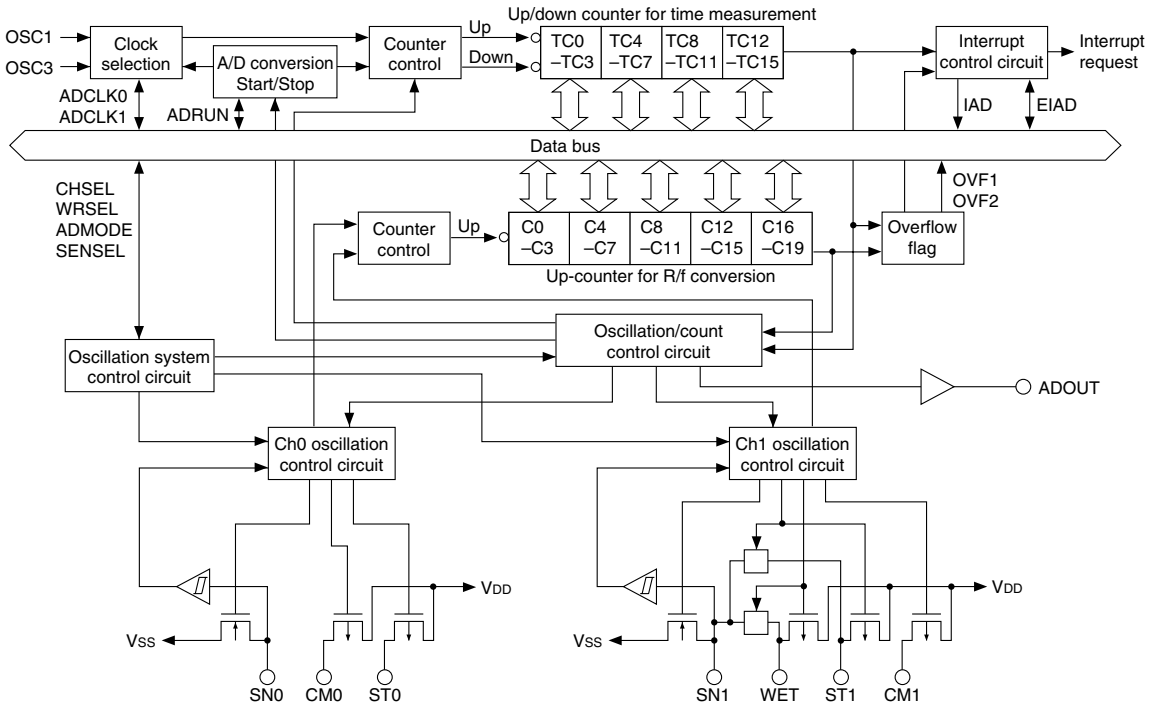


Fig. 4.14.1.1 Configuration of A/D converter

4.14.2 CR oscillation circuit

Two systems of CR oscillation circuit, channel 0 and channel 1, are built into the A/D converter and perform CR oscillation with external resistor and capacitor.
The counter that is used to obtain an A/D converted value is shared with channel 0 and channel 1. Therefore, operation for two systems is realized by switching the CR oscillation circuit that performs A/D conversion. The channel selection is done using the register CHSEL. When CHSEL is set to "0", channel 0 is selected and when "1" is set, channel 1 is selected.
The sensor type to be A/D converted in the channel 1 can also be selected by the software, and it should be previously set using the register WRSEL.

Channel selection CHSEL = "0": Channel 0
CHSEL = "1": Channel 1
Sensor selection for channel 1 WRSEL = "0": R/f conversion using a resistive sensor such as thermistor
WRSEL = "1": R/f conversion using a resistive humidity sensor *

* The operation of the oscillation circuit differs from the normal resistive sensor. (Refer to the following.)

(1) R/f conversion using a resistive sensor such as thermistor

Channel 0 is set only for this conversion method, and channel 1 is selected into this method by setting WRSEL (channel 1) to "0". This method should be selected for A/D conversion using a normal resistive sensor (DC bias), such as temperature measurement using thermistor. At initial reset, channel 1 is set into this conversion method.
Figure 4.14.2.1 shows the connection diagram of external elements.

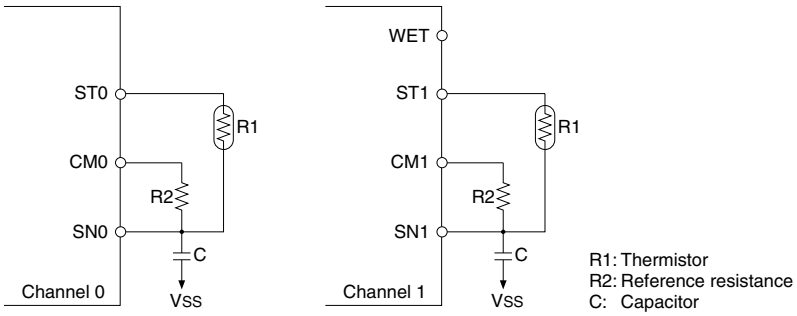


Fig. 4.14.2.1 Connection diagram in case of R/f conversion

Connect a resistive sensor (such as a thermistor) between the ST0 (ST1) and SN0 (SN1) terminals. Next, set the reference value of the item to be measured (e.g. reference temperature in the case of temperature measurement) and connect the reference resistance equivalent to the sensor resistance value at the above reference value between the CM0 (CM1) and SN0 (SN1) terminals. An element that does not change due to temperature or other environmental conditions must be used as the reference resistance.
Connect an oscillating capacitor that is used for CR oscillation of both the reference resistance and the sensor between the SN0 (SN1) and VSS terminals.
The WET terminal should be opened because it is not used in this method.

The A/D converter performs CR oscillation using each of the two resistances (sensor and reference resistance) in the same period, and counts the CR oscillation clock. Difference in counted oscillation frequency can be evaluated in terms of the difference between the respective resistance values. Measurement results can be obtained from the changes in resistance values after correcting the difference according to the program.

The CR oscillation circuit is designed so that either the reference resistance side or the sensor side can be operated independently by the oscillation control circuit.
Each circuit performs the same oscillating operation as follows:

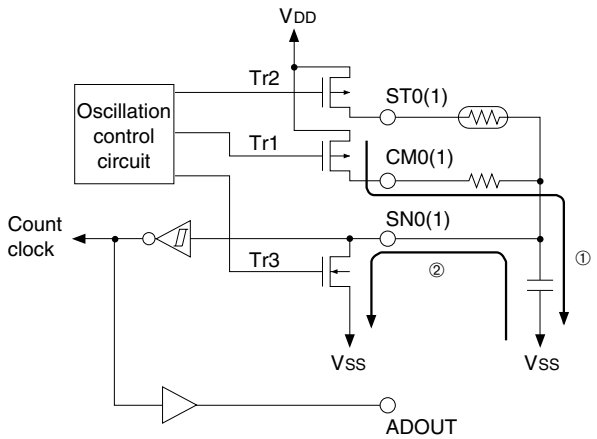


Fig. 4.14.2.2 CR oscillation circuit in case of R/f conversion

The Tr1 (Tr2) turns on first, and the capacitor connected between the CM (ST) and VSS terminals is charged through the reference resistance (sensor). If the voltage level of the SN terminal decreases, the Tr1 (Tr2) turns off and the Tr3 turns on. As a result, the capacitor becomes discharged, and oscillation is performed according to CR time constant. The time constant changes as the sensor resistance value fluctuates, producing a difference from the oscillation frequency of the reference resistance.

Oscillation waveforms are shaped by the schmitt trigger and transmitted to counter. The clock transmitted to the counter is also output from the ADOUT terminal. As a result, oscillation frequency can be identified by the frequency counter. Since this monitor has no effect on oscillation frequency, it can be used to adjust CR oscillation frequency.
Oscillation waveforms and waveforms output from the ADOUT terminal are shown in Figure 4.14.2.3.

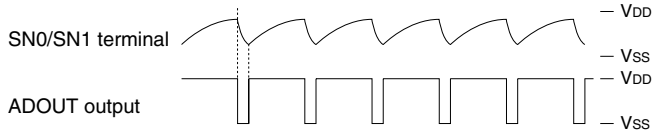


Fig. 4.14.2.3 Oscillation waveform

(2) R/f conversion using a resistive humidity sensor

This conversion is possible only in channel 1, and this method is selected by setting the register WRSEL to "1". This is basically the same as the R/f conversion described above (1), but the AC bias circuit works for the humidity sensor.
Figure 4.14.2.4 shows the connection diagram of external devices.

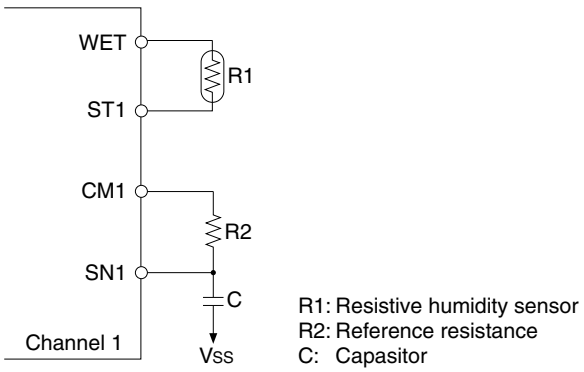


Fig. 4.14.2.4 Connection diagram of resistive humidity sensor

Connect a humidity sensor between the WET and ST1 terminals, and connect a reference resistance between the CM1 and SN1 terminals.
Connect an oscillating capacitor that is used for CR oscillation of both the reference resistance and the sensor between the SN1 and VSS terminals.
The oscillating operation by reference resistance is the same as the R/f conversion described above (1).
The humidity sensor cannot be DC biased for a long time, therefore this method powers the WET and ST1 terminals alternately.

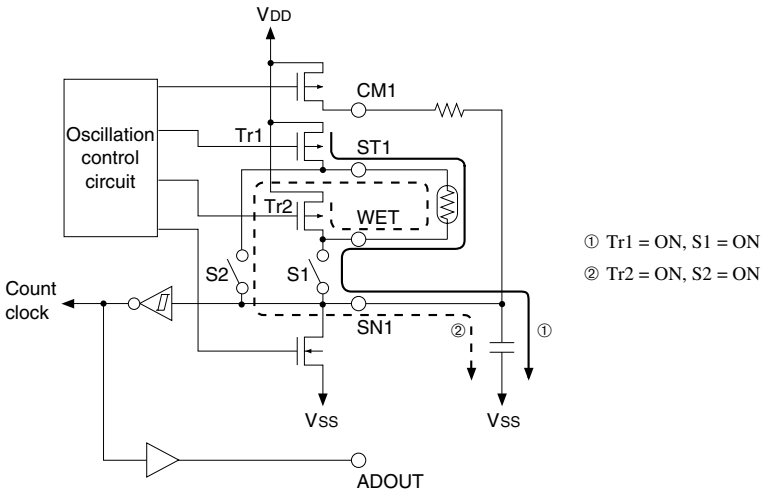


Fig. 4.14.2.5 CR oscillation circuit for resistive humidity sensor

The oscillation waveform is the same as Figure 4.14.2.3.

4.14.3 Operation of A/D conversion

(1) Power supply

In the A/D converter, it is necessary to control the power on/off, and it is done by using the register APWR. When APWR is set to "1", the power turns on and when set to "0", it turns off. Further, set to "1" for the LPWR register, because the A/D converter uses the LCD power supply.
To reduce current consumption, turn the power off if not in use.

(2) Counter

The A/D converter incorporates two types of counters. One is the 20-bit up-counter C0–C19 that counts the aforementioned oscillation clock, and the other is 16-bit up/down counter TC0–TC15 that counts the internal clock for reference counting. Each counter permits reading and writing on a 4-bit basis.

The up-counter C0–C19 is used to count the CR oscillation clock by the reference resistance and sensor, and the results of A/D conversion can be obtained by reading this counter.
This counter is designed so that it counts serially in order of the reference resistance and the sensor. Also it switches the CR oscillation from reference resistance to sensor at the point an overflow occurs during counting of the reference resistance oscillation. Furthermore, both of the oscillation times of the reference resistance and sensor are designed to be the same by the up/down counter described later. Therefore, by converting a proper initial value for counting of the oscillation of the reference resistance into a complement (value subtracted from 0000H) and setting it into the counter before starting to count, the number of counts for the sensor oscillation is obtained by reading this counter after the A/D conversion. In other words, the difference between the reference resistance and sensor oscillation frequencies can be found easily. For instance, if resistance values of the reference resistance and the sensor are equivalent, the same value as the initial value before converting into a complement will be obtained as the result. So this means that the difference between oscillation frequencies is Zero.

The up/down counter TC0–TC15 is a counter to equal both oscillation times for the reference resistance and the sensor. For the input clock, either OSC1 clock (Typ. 32.768 kHz) or OSC3 clock (Typ. 1 MHz) can be selected using the software. This selection can be done for each channel; the register ADCLK0 is used for channel 0 and the register ADCLK1 for channel 1. When "1" is set to the register, OSC3 clock is selected and when "0" is set, OSC1 clock is selected.
This counter must be set to "0000H" before starting the A/D conversion. This is due to the following reasons. This counter starts counting-up at the same time the up-counter C0–C19 starts counting for oscillation by reference resistance. After that, when the oscillation switches to the sensor side, this counter also switches to counting-down mode and counts down oppositely from the value that is counted during oscillation of the reference resistance. The counting-down continues until the counter value is "0000H". When the counter becomes "0000H", the counter stops and the sensor oscillation also stops. In other words, the oscillation times of reference resistance and sensor can be made the same by setting "0000H" previously to the conversion.

(3) A/D conversion sequence

A/D conversion starts by writing "1" to the register ADRUN.
Further the following settings must be done before starting the A/D conversion.

1. Sensor selection (WRSEL) ...When the channel 1 is used.
2. Channel selection (CHSEL)
3. Turning the A/D converter power on (APWR)
4. Clearing the up/down counter TC0–TC15
5. Initial value setting to the up-counter C0–C19

When A/D conversion is initiated by the ADRUN register, oscillation by the reference resistance begins first, and the up-counter C0–C19 starts counting up according to the oscillation clock. The up/down counter TC0–TC15 also starts counting up by the internal clock.
Timing in starting oscillation and starting counting up are shown in Figure 4.14.3.1.
The up-counter C0–C19 is enabled at the falling edge of the first clock after CR oscillation is initiated and starts counting up from the falling edge of the next clock.
The up/down counter TC0–TC15 becomes enable at the falling edge of the internal clock which is input immediately after starting the A/D conversion. Then, it starts counting up from the falling edge of the next internal clock.

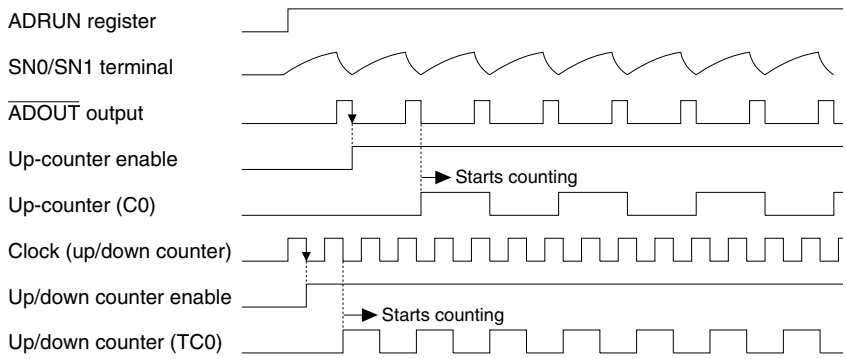


Fig. 4.14.3.1 Counting up start timing

If the up-counter C0–C19 becomes "00000H" due to overflow, the oscillation is switched from the reference resistance side to the sensor side, and the up-counter starts counting up according to the oscillation clock on the sensor side.
The up/down counter TC0–TC15 shifts to the counting-down mode at this point and starts counting down from the value that has been counted while the reference resistance was oscillating.
Timing in starting counting when oscillation is switched, is same as Figure 4.14.3.1.

When the up/down counter TC0–TC15 has counted down to "0000H", the counting operation of both counters and CR oscillation stops, and an interrupt occurs. At the same time, the ADRUN register is set to "0", and the A/D converter circuit stops operation completely.

Since the reference resistance is oscillated until the up-counter C0–C19 overflows, an appropriate initial value needs to be set before A/D conversion is started. If a smaller initial value is set, a longer counting period is possible, thereby ensuring more accurate detection. However, the up/down counter TC0–TC15 may overflow while counting the oscillation frequency of the reference resistance.
If an overflow occurs, CR oscillation and A/D conversion is terminated immediately. Also in such cases, interrupt occurs. Moreover, the up-counter may overflow while counting the sensor oscillation depending on initial value setting. If the up-counter overflows, CR oscillation and A/D conversion is terminated at that point and an interrupt occurs.
When these overflows occur, the correct value cannot be read. Therefore, the overflow flags are provided to judge whether the read data is correct or an overflow occurs. There are two overflow flags; OVF1 that indicates an up-counter overflow and OVF2 that indicates an up/down counter overflow. These flags are set to "1" if respective counter overflows. When the interrupt occurs, be sure to read the overflow flags and check overflow.
The initial value to be set depends on the measurable range by the sensor or where to set the reference resistance value within that range.
The initial value must be set taking the above into consideration.

Convert the initial value into a complement (value subtracted from 00000H) before setting it on the up-counter C0–C19. Since the data output from the up-counter C0–C19 after A/D conversion matches data detected by the sensor, process the difference between that value and the initial value before it is converted into a complement according to the program and calculate the target value.

The above operations are shown in Figure 4.14.3.2.

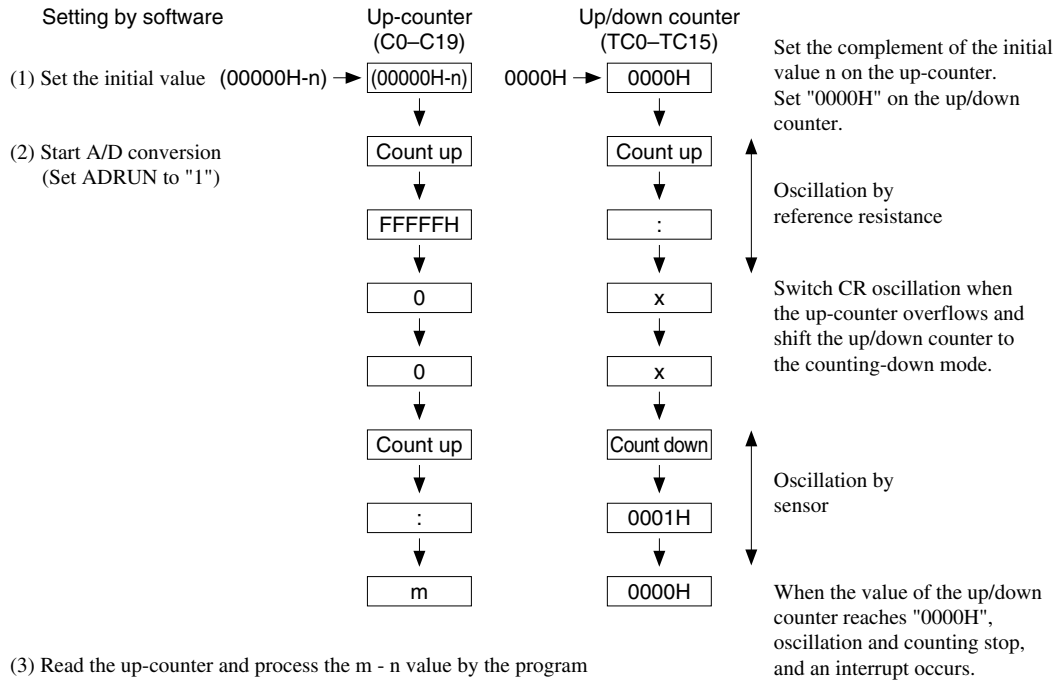


Fig. 4.14.3.2 Sequence of A/D conversion

Note:
- *Set the initial value of the up-counter C0–C19 taking into account the measurable range and the overflow of counters.*
- *When the up/down counter TC0–TC15 is read after A/D conversion, it may not indicate "0000H". This is not due to incorrect timing in terminating A/D conversion but because the counting down clock is input after the control signal is output to the up-counter to terminate counting.*

(4) Operation mode

Thus far we explained the A/D converter to be operated in the normal mode.
The continuous mode is set as an operating mode for the A/D converter in addition to the normal mode, and can be set by writing "1" to the register ADMODE. To return to the normal mode, write "0" to the ADMODE.
The continuous mode is provided for hardware/software debugging. It functions to continuously oscillate only the reference resistance side or sensor side. The oscillating operation starts by writing "1" to the ADRUN and is continued until "0" is written to the ADRUN.
Whether to oscillate the reference resistance or sensor is selected using the register SENSEL.
Settings of the registers WRSEL and CHSEL are valid even in the continuous mode. They should be set according to the content of debugging.
Further both the up-counter and the up/down counter do not operate for counting in this mode, and an interrupt does not occur.

4.14.4 Interrupt function

The A/D converter has a function which allows interrupt to occur after A/D conversion.
When the up/down counter TC0–TC15 is counted down to "0000H", both counters stop counting. The interrupt factor flag IAD is set to "1" at the rising edge of the next clock.
If the up/down counter TC0–TC15 overflows during counting of the reference resistance oscillation, or the up-counter C0–C19 overflows during counting of the sensor oscillation, the interrupt factor flag IAD is also set to "1".
This interrupt factor allows masking by the interrupt mask register EIAD. When the EIAD has been set at "1", an interrupt occurs in the CPU. When the EIAD is set at "0", no interrupt will occur in the CPU even if the interrupt factor flag is set to "1".
The interrupt factor flag is reset to "0" by reading.
Timing of interrupt by the A/D converter is shown in Figure 4.14.4.1.

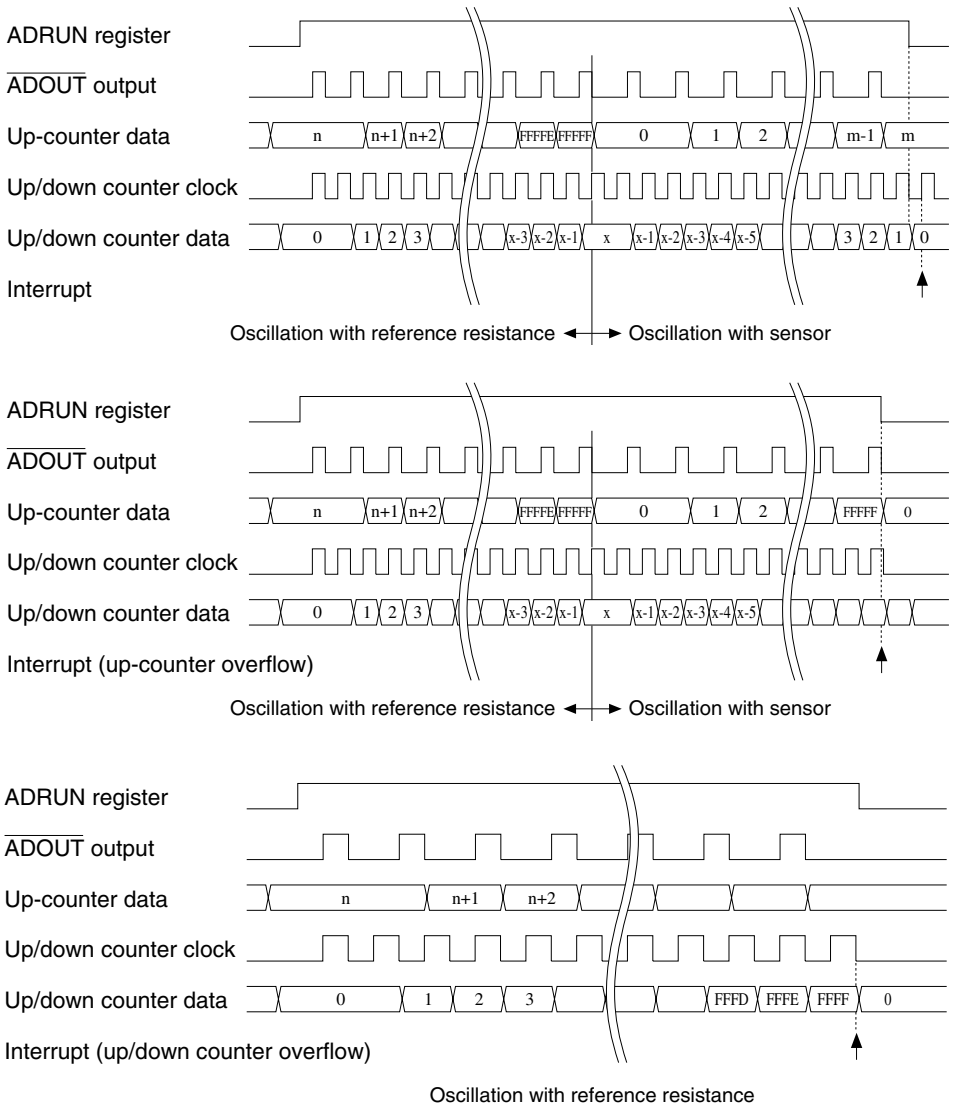


Fig. 4.14.4.1 Timing of A/D converter interrupt

Note: When an interrupt occurs by the counter overflow, the same interrupt will occur if the overflow flag (OVF1 or OVF2) is not reset. Be sure to check and reset the overflow flag when the A/D converter interrupt occurs.

4.14.5 Control of A/D converter

Tables 4.14.5.1(a) and (b) list the control bits and their addresses for the A/D converter.

Table 4.14.5.1(a) Control bits of A/D converter

Address *7	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
E0H	0	APWR	SENSEL	ADMODE	0 *5	– *2			Unused
					APWR	0	On	Off	A/D converter power supply On/Off
	R	R/W			SENSEL	0	Sensor	Reference	Sensor/reference resistance selection
					ADMODE	0	Continuous	Normal	A/D converter operation mode selection
E1H	WRSEL	0	ADCLK1	ADCLK0	WRSEL	0	Humidity	Resistance	CH1 sensor selection (resistance/humidity)
					0 *5	– *2			Unused
	R/W	R	R/W		ADCLK1	0	OSC3	OSC1	CH1 clock selection
					ADCLK0	0	OSC3	OSC1	CH0 clock selection
E2H	0	0	0	CHSEL	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R			R/W	0 *5	– *2			Unused
					CHSEL	0	CH1	CH0	Channel 1/0 selection
E3H	TC3	TC2	TC1	TC0	TC3	– *3			Up/down counter data (TC0–TC3)
					TC2	– *3			
	R/W				TC1	– *3			
					TC0	– *3			LSB
E4H	TC7	TC6	TC5	TC4	TC7	– *3			Up/down counter data (TC4–TC7)
					TC6	– *3			
	R/W				TC5	– *3			
					TC4	– *3			
E5H	TC11	TC10	TC9	TC8	TC11	– *3			Up/down counter data (TC8–TC11)
					TC10	– *3			
	R/W				TC9	– *3			
					TC8	– *3			
E6H	TC15	TC14	TC13	TC12	TC15	– *3			MSB
					TC14	– *3			Up/down counter data (TC12–TC15)
	R/W				TC13	– *3			
					TC12	– *3			
E7H	C3	C2	C1	C0	C3	– *3			Up-counter data (C0–C3)
					C2	– *3			
	R/W				C1	– *3			
					C0	– *3			LSB
E8H	C7	C6	C5	C4	C7	– *3			Up-counter data (C4–C7)
					C6	– *3			
	R/W				C5	– *3			
					C4	– *3			
E9H	C11	C10	C9	C8	C11	– *3			Up-counter data (C8–C11)
					C10	– *3			
	R/W				C9	– *3			
					C8	– *3			
EAH	C15	C14	C13	C12	C15	– *3			Up-counter data (C12–C15)
					C14	– *3			
	R/W				C13	– *3			
					C12	– *3			
EBH	C19	C18	C17	C16	C19	– *3			MSB
					C18	– *3			Up-counter data (C16–C19)
	R/W				C17	– *3			
					C16	– *3			
ECH	0	OVF2	OVF1	ADRUN	0 *5	– *2			Unused
					OVF2(R)	0	Yes	No	Up/down counter overflow flag
					OVF2(W)	Reset	Reset	–	Up/down counter overflow flag reset
	R	R/W			OVF1(R)	0	Yes	No	Up-counter overflow flag
					OVF1(W)	Reset	Reset	–	Up-counter overflow flag reset
					ADRUN	0	Start	Stop	A/D conversion Start/Stop

*1 Initial value at the time of initial reset
*2 Not set in the circuit
*3 Undefined
*4 Reset (0) immediately after being read
*5 Constantly "0" when being read
*6 Refer to main manual
*7 Page switching in I/O memory is not necessary

Table 4.14.5.1(b) Control bits of A/D converter

Address *7	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
F0H	0	0	0	EIAD	0 *5	– *2			Unused
					0 *5	– *2			Unused
					0 *5	– *2			Unused
	R			R/W	EIAD	0	Enable	Mask	Interrupt mask register (A/D converter)
F8H	0	0	0	IAD	0 *5	– *2			Unused
					0 *5	– *2			Unused
					0 *5	– *2			Unused
	R				IAD *4	0	Yes	No	Interrupt factor flag (A/D converter)

*1 Initial value at the time of initial reset
*2 Not set in the circuit
*3 Undefined
*4 Reset (0) immediately after being read
*5 Constantly "0" when being read
*6 Refer to main manual
*7 Page switching in I/O memory is not necessary

APWR: A/D converter power ON/OFF (E0H•D2)

Controls the A/D converter power ON and OFF.

When "1" is written: Power ON
When "0" is written: Power OFF
Reading: Valid

When "1" is written to APWR, the A/D converter power goes ON, and when "0" is written, it goes OFF. To reduce current consumption, turn the power OFF when it is not necessary.
At initial reset, this register is set to "0"

SENSEL: Sensor/reference resistance selection (E0H•D1)

Selects an element to be oscillated during the continuous mode.

When "1" is written: Sensor
When "0" is written: reference resistance
Reading: Valid

When "1" is written to SENSEL, sensor is selected, and when "0" is written, reference resistance is selected. This selection is valid only in the continuous mode.
At initial reset, this register is set to "0".

ADMODE: Operating mode selection (E0H•D0)

Selects the operating mode of the A/D converter.

When "1" is written: Continuous mode
When "0" is written: Normal mode
Reading: Valid

When "1" is written to ADMODE, the continuous mode is selected, and when "0" is written, the normal mode is selected. When the continuous mode is set, the oscillating operation of the element side selected by the SENSEL register can be done continuously.
At initial reset, this register is set to "0".

ADCLK0, ADCLK1: Input clock selection (E1H•D0, D1)

Select an input clock of the up/down counter TC0–TC15.

When "1" is written: OSC3
When "0" is written: OSC1
Reading: Valid

Select a clock for the counting operation of the up/down counter TC0–TC15. ADCLK0 is used for channel 0, and ADCLK1 is for channel 1. Each channel can use a separate clock.
When "1" is written to ADCLK0(1), the OSC3 clock (Typ. 1 MHz) is selected. When "0" is written, the OSC1 clock (Typ. 32 kHz) is selected.
When the OSC1 clock (32 kHz) is used, up to 2 sec oscillation can be made. When the OSC3 (1 MHz) clock is used, up to 66.5 msec oscillation can be made.
The initial value must be set on the up-counter C0–C19 so that the up/down counter TC0–TC15 will not overflow while CR oscillation is being counted.
At initial reset, these registers are set to "0".

WRSEL: Sensor selection for channel 1 (E1H•D3)
Selects a sensor type to be used for channel 1.

When "1" is written: Resistive humidity sensor
When "0" is written: Resistive sensor
Reading: Valid

When "1" is written to WRSEL, a resistive humidity sensor is selected as the sensor for channel 1. When "0" is written, a normal resistive sensor is selected.
At initial reset, this register is set to "0".

CHSEL: Channel selection (E2H•D0)
Selects a channel to be A/D converted.

When "1" is written: Channel 1
When "0" is written: Channel 0
Reading: Valid

When "1" is written to CHSEL, the channel 1 is selected, and when "0" is written, the channel 0 is selected.
At initial reset, this register is set to "0".

TC0–TC15: Up/down counter (E3H–E6H)
Writing and reading is possible on a 4-bit basis by the up/down counter that is used to adjust the CR oscillation time between the reference resistance and the sensor.
The up/down counter counts up during oscillation of the reference resistance and counts down from the value it reached when counting up to "0000H" during oscillation of the sensor.
"0000H" needs to be entered in the counter prior to A/D conversion in order to adjust the CR oscillating time (number of clocks) of both counts.
After an initial reset, data in this counter become indefinite.

C0–C19: Up-counter (E7H–EBH)
This counter counts up according to the CR oscillation clock. It permits writing and reading on a 4-bit basis. The complement of the number of clocks to be counted by the oscillation of the reference resistance, must be entered in this counter prior to A/D conversion.
If A/D conversion is initiated, the counter counts up from the set initial value, first according to the oscillation clock of the reference resistance. When the counter reaches "00000H" due to overflow, the oscillation of the reference resistance stops, and the sensor starts oscillating. The counter continues counting according to the sensor oscillation clock. Counting time during the CR oscillation of the reference resistance is calculated by the up/down counter TC0–TC15. Up-counter C0–C19 stops counting when the same period of time elapses. Number of clocks counted by the sensor oscillation can be evaluated from the value indicated by the counter when it stops. Calculate the target value by processing the above counted number according to the program.
Measurable range and the overflow of the counter must be taken into account when setting an initial value to be entered prior to A/D conversion.
After an initial reset, data in this counter become indefinite.

ADRUN: A/D conversion START/STOP (ECH•D0)
Starts A/D conversion.

When "1" is written: A/D conversion starts
When "0" is written: A/D conversion stops
Reading: Valid

When "1" is written to ADRUN, A/D conversion starts. The register remains at "1" during A/D conversion and is set to "0" when A/D conversion is terminated.
When "0" is written to ADRUN during A/D conversion, A/D conversion is paused.
This register is set to "0" at initial reset, when the up/down counter or up-counter overflows, or when measurement is finished.

OVF1: Up-counter overflow flag (ECH•D1)

Indicates whether the up-counter has overflown.

When "1" is read: Overflow has occurred
When "0" is read: Overflow has not occurred

When "1" is written: Flag reset
When "0" is written: No operation

If an overflow occurs while counting the oscillation of the sensor, OVF1 is set to "1" and the interrupt occurs at the same time.
Since this flag is not reset by reading, write "1" to reset by the software. Further it is reset when "1" is written to ADRUN.

OVF2: Up/down counter overflow flag (ECH•D2)

Indicates whether the up/down counter has overflown.

When "1" is read: Overflow has occurred
When "0" is read: Overflow has not occurred

When "1" is written: Flag reset
When "0" is written: No operation

If an overflow occurs while counting the oscillation of the reference resistance, OVF2 is set to "1" and the interrupt occurs at the same time.
Since this flag is not reset by reading, write "1" to reset by the software. Further it is reset when "1" is written to ADRUN.

EIAD: Interrupt mask register (F0H•D0)

Select whether to mask interrupt with the A/D converter.

When "1" is written: Enable
When "0" is written: Mask
Reading: Valid

The A/D converter interrupt is permitted when "1" is written to EIAD. When "0" is written, interrupt is masked.
At initial reset, this register is set to "0".

IAD: Interrupt factor flag (F8H•D0)

This flag indicates the status of the A/D converter interrupt.

When "1" is read: Interrupt has occurred
When "0" is read: Interrupt has not occurred
Writing: Invalid

IAD is set to "1" when A/D conversion is terminated (when the up/down counter counted up or down to "0000H"), when the up/down counter TC0–TC15 overflows while counting the oscillation of the reference resistance, or the up-counter C0–C19 overflows while counting the oscillation of the sensor.
From the status of this flag, the software can decide whether an A/D converter interrupt has occurred.
Further this flag is set in the above timing regardless of the interrupt mask register setting.
This flag is reset when the software has read it.
Reading of interrupt factor flag is available at EI, but be careful in the following cases.
If the interrupt mask register value corresponding to the interrupt factor flag to be read is set to "1", an interrupt request will be generated by the interrupt factor flag set timing, or an interrupt request will not be generated.
After an initial reset, this flag is set to "0".

4.14.6 Programming notes

(1) Depending on the initial value of the up-counter C0–C19, the up-counter or the up/down counter may overflow while the CR oscillation clock is being counted. When setting the initial value, pay attention to CR oscillation frequency, its fluctuation range and the input clock frequency of the up/down counter. If an overflow occurs, A/D conversion is terminated immediately. When the A/D conversion result (up-counter value) is read, check the overflow flag.

(2) When the up/down counter TC0–TC15 is read after A/D conversion, it may not indicate "0000H". This is not due to incorrect timing in terminating A/D conversion but because the counting down clock is input after the control signal is output to the up-counter to terminate counting.

(3) When an interrupt occurs by the counter overflow, the same interrupt will occur if the overflow flag (OVF1 or OVF2) is not reset. Be sure to check and reset the overflow flag when the A/D converter interrupt occurs.

(4) When reading the up-counter data (TC0–TC15), be sure to read from the low-order address first.

(5) Pay attention when using the OSC3 oscillation clock as the input clock for the up/down counter. It is necessary to switch the V_{S1} output voltage, control the OSC3 oscillation circuit and switch the CPU clock.

(6) The A/D converter uses the LCD power supply as its power source. If starting A/D conversion when the LPWR register (C3H) has been set to "0" and the LCD power is OFF, the LCD power supply circuit activates at the time of the APWR register is set to "1". In such a case, be sure to secure 100 msec or more time to stabilize the power. (The LCD power supply is also turned ON by setting the APWR register to "1".)
Setting of the APWR register (E0H) is necessary even if the LPWR register (C3H) has been set to "1" and the LCD power has already been turned ON. Be sure to set "1" prior to A/D conversion.

(7) Reading of interrupt factor flag is available at EI, but be careful in the following cases.
If the interrupt mask register value corresponding to the interrupt factor flag to be read is set to "1", an interrupt request will be generated by the interrupt factor flag set timing, or an interrupt request will not be generated.

4.15 SVD (Supply Voltage Detection) Circuit

4.15.1 Configuration of SVD circuit

The E0C6256 has a built-in SVD (supply voltage detection) circuit, so that the software can find when the source voltage lowers. Turning the SVD circuit ON/OFF and the SVD criteria voltage setting can be controlled by the software.
Figure 4.15.1.1 shows the configuration of the SVD circuit.

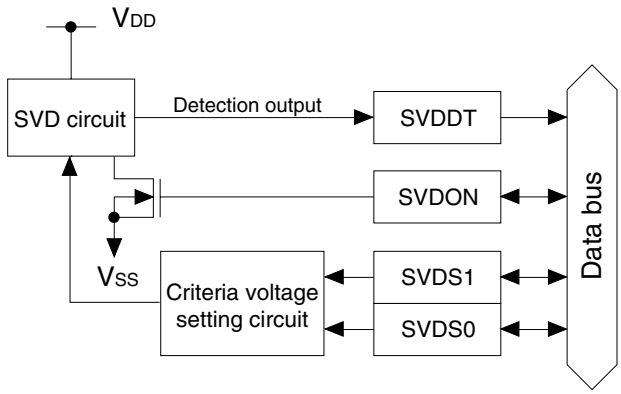


Fig. 4.15.1.1 Configuration of SVD circuit

4.15.2 Mask option

For the criteria voltage setting, either 1.5 V system or 3.0 V system can be selected by the mask option. Select it to match the specifications, such as batteries, to be used.

4.15.3 SVD operation

The SVD circuit compares the criteria voltage set by the software and the supply voltage (V_{DD}–V_{SS}) and sets its results into the SVDDT latch. By reading the data of this SVDDT latch, it can be determined by means of software whether the supply voltage is normal or has dropped.
The criteria voltage can be set for the three types shown in Table 4.15.3.1 by SVDS0 and SCDS1.

Table 4.15.3.1 Criteria voltage setting

SVDS1	SVDS0	Criteria voltage (1.5 V system/ 3.0 V system)*
0	0	1.05 V / 2.30 V
0	1	1.20 V / 2.45 V
1	0	1.35 V / 2.60 V
1	1	1.35 V / 2.60 V

* Selected by mask option

When SVDON is set to "1", source voltage detection by the SVD circuit is executed. As soon as SVDON is reset to "0", the result is loaded to in the SVDDT latch and SVD circuit goes OFF.
To obtain a stable SVD detection result, the SVD circuit must be on for at least l00 µsec. So, to obtain the SVD detection result, follow the programming sequence below.

① Set SVDON to "1"
② Maintain for 100 µsec minimum
③ Set SVDON to "0"
④ Read SVDDT

However, when f_{OSC1} is selected for CPU system clock, the instruction cycles are long enough, so there is no need to worry about maintaining 100 µsec for SVDON = "1" in the software.
When SVD is on, the IC draws a large current, so keep SVD off unless it is.

4.15.4 Control of SVD circuit

Table 4.15.4.1 shows the control bits and their addresses for the SVD circuit.

Table 4.15.4.1 Control bits for SVD circuit

Address *7	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
80H	0	0	SVDS1	SVDS0	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R		R/W		SVDS1	0			SVD criteria voltage setting (1.5 V/3.0 V)
					SVDS0	0			0: 1.05/2.30, 1: 1.20/2.45, 2 & 3: 1.35/2.60 (V)
81H	0	0	SVDDT	SVDON	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R			R/W	SVDDT	0	Low	Normal	Supply voltage detection data
					SVDON	0	On	Off	SVD circuit On/Off

*1 Initial value at the time of initial reset
*2 Not set in the circuit
*3 Undefined
*4 Reset (0) immediately after being read
*5 Constantly "0" when being read
*6 Refer to main manual
*7 Page switching in I/O memory is not necessary

SVDS0, SVDS1: SVD criteria voltage setting (80H•D0, D1)

Criteria voltage for SVD is set as shown in Table 4.15.4.2.

Table 4.15.4.2 Criteria voltage setting

SVDS1	SVDS0	Criteria voltage (1.5 V system/ 3.0 V system)*
0	0	1.05 V / 2.30 V
0	1	1.20 V / 2.45 V
1	0	1.35 V / 2.60 V
1	1	1.35 V / 2.60 V

* Selected by mask option

At initial reset, these registers are set to "0".

Note: 1.05 V or 1.20 V of the 1.5 V system criteria voltage must be used in the doubler mode, so the doubler mode has to be set when using these criteria voltages. Using the normal mode may cause a malfunction or will be unable to detect the supply voltage correctly. See Section 4.2, "Power Supply and Operating Mode Settings" for the operating mode switching.

SVDON: SVD ON/OFF (81H•D0)

Turns the SVD circuit ON and OFF.

When "1" is written: SVD circuit ON
When "0" is written: SVD circuit OFF
Reading: Valid

When SVDON is set to "1", source voltage detection by the SVD circuit is executed. As soon as SVDON is reset to "0", the result is loaded to in the SVDDT latch. To obtain a stable SVD detection result, the SVD circuit must be on for at least l00 µsec.
At initial reset, this register is set to "0".

SVDDT: SVD data (81H•D1)

This is the result of supply voltage detection.

When "0" is read: Supply voltage (V_{DD}–V_{SS}) ≥ Criteria voltage
When "1" is read: Supply voltage (V_{DD}–V_{SS}) < Criteria voltage
Writing: Invalid

The result of supply voltage detection at time of SVDON is set to "0" can be read from this latch.
At initial reset, SVDDT is set to "0".

4.15.5 Programming notes

(1) To obtain a stable SVD detection result, the SVD circuit must be on for at least l00 µsec. So, to obtain the SVD detection result, follow the programming sequence below.

① Set SVDON to "1"
② Maintain for 100 µsec minimum
③ Set SVDON to "0"
④ Read SVDDT

However, when f_{OSC1} is selected for CPU system clock, the instruction cycles are long enough, so there is no need to worry about maintaining 100 µsec for SVDON = "1" in the software.

(2) The SVD circuit should normally be turned OFF as the consumption current of the IC becomes large when it is ON.

(3) 1.05 V or 1.20 V of the 1.5 V system criteria voltage must be used in the doubler mode, so the doubler mode has to be set when using these criteria voltages. Using the normal mode may cause a malfunction or will be unable to detect the supply voltage correctly. See Section 4.2, "Power Supply and Operating Mode Settings" for the operating mode switching.

4.16 Interrupt and HALT

<Interrupt types>

The E0C6256 provides the following interrupt settings, each of which is maskable.

External interrupt:	•Input port interrupt	(2 systems)
Internal interrupt:	•Clock timer interrupt	(4 systems)
	•Stopwatch timer interrupt	(4 systems)
	•Programmable timer interrupt	(1 system)
	•Serial interface interrupt	(1 system)
	•A/D converter interrupt	(1 system)

To authorize interrupt, the interrupt flag must be set to "1" (EI) and the necessary related interrupt mask registers must be set to "1" (enable).
When an interrupt occurs the interrupt flag is automatically reset to "0" (DI), and interrupts after that are inhibited.
Figure 4.16.1 shows the configuration of the interrupt circuit.

<HALT>

The E0C6256 has HALT function that considerably reduce the current consumption when it is not necessary.

The CPU enters the HALT status when the HALT instruction is executed.
In the HALT status, the operation of the CPU is stopped. However, the oscillation circuit operates. Reactivating the CPU from the HALT status is done by generating an interrupt request. When it does not reactivate upon an interrupt request, the watchdog timer will cause it to restart from the initial reset status. (When "Use" is selected in the mask option of the watchdog timer.)

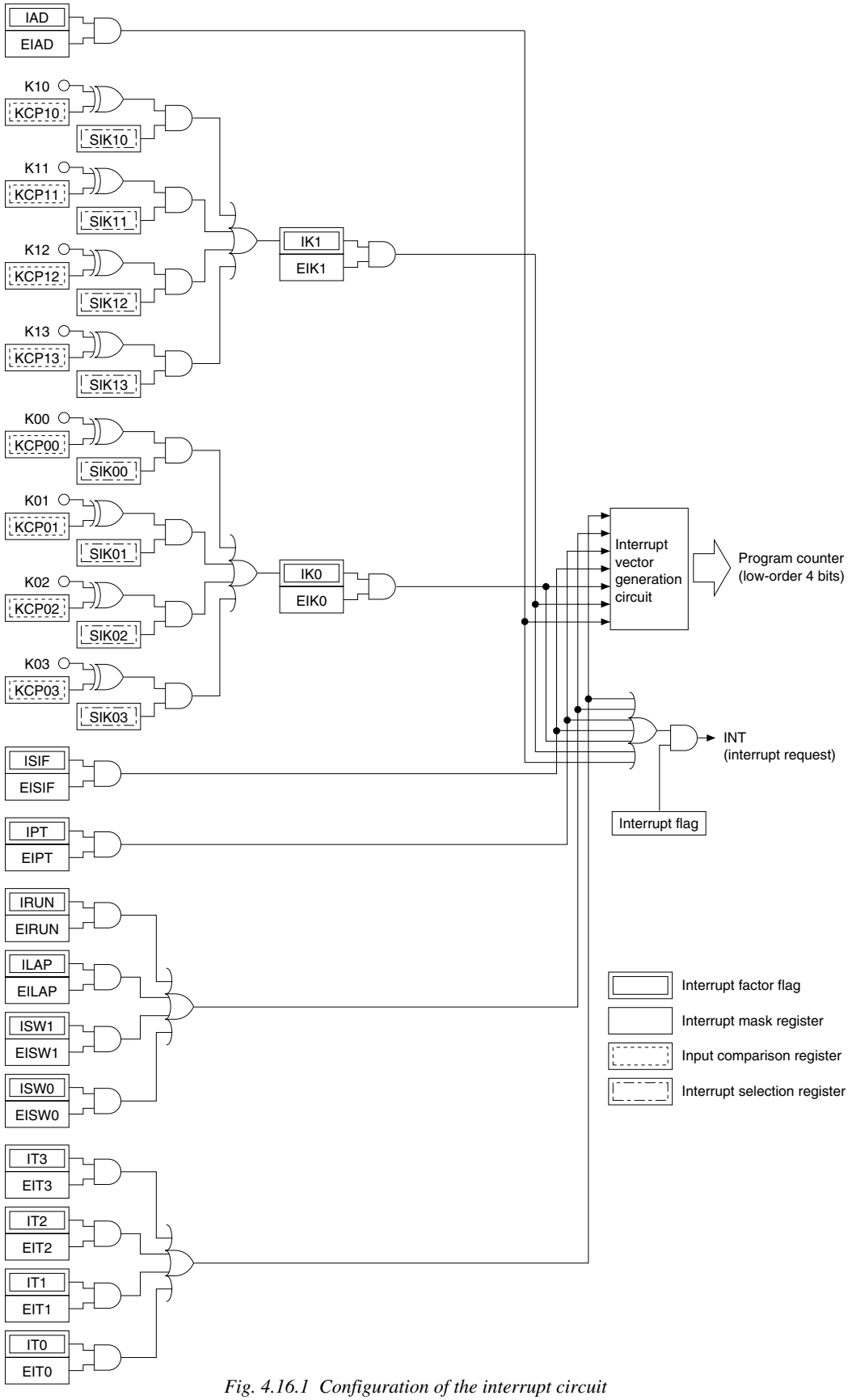


Fig. 4.16.1 Configuration of the interrupt circuit

4.16.1 Interrupt factor

Table 4.16.1.1 shows the factors for generating interrupt requests.

The interrupt flags are set to "1" depending on the corresponding interrupt factors.
The CPU operation is interrupted when any of the conditions below set an interrupt factor flag to "1".

- The corresponding mask register is "1" (enabled)
- The interrupt flag is "1" (EI)

The interrupt factor flag is a read-only register, but can be reset to "0" when the register data is read out.
At initial reset, the interrupt factor flags are reset to "0".

Table 4.16.1.1 Interrupt factors

Interrupt factor	Interrupt factor flag
Clock timer 2 Hz (falling edge)	IT3 (FEH•D3)
Clock timer 8 Hz (falling edge)	IT2 (FEH•D2)
Clock timer 16 Hz (falling edge)	IT1 (FEH•D1)
Clock timer 32 Hz (falling edge)	IT0 (FEH•D0)
Stopwatch timer direct RUN (input)	IRUN (FDH•D3)
Stopwatch timer direct LAP (input)	ILAP (FDH•D2)
Stopwatch timer 1 Hz (falling edge)	ISW1 (FDH•D1)
Stopwatch timer 10 Hz (falling edge)	ISW0 (FDH•D0)
Programmable timer (counter = 0)	IPT (FCH•D0)
Serial interface (8-bit data input/output has completed)	ISIF (FBH•D0)
K00–K03 input (falling or rising edge)	IK0 (FAH•D0)
K10–K13 input (falling or rising edge)	IK1 (F9H•D0)
A/D converter (A/D conversion has completed)	IAD (F8H•D0)

Note: Reading of interrupt factor flags is available at EI, but be careful in the following cases.
If the interrupt mask register value corresponding to the interrupt factor flags to be read is set to "1", an interrupt request will be generated by the interrupt factor flags set timing, or an interrupt request will not be generated.

4.16.2 Interrupt mask

The interrupt factor flags can be masked by the corresponding interrupt mask registers.
The interrupt mask registers are read/write registers. They are enabled (interrupt authorized) when "1" is written to them, and masked (interrupt inhibited) when "0" is written to them.
At initial reset, the interrupt mask register is set to "0".
Table 4.16.2.1 shows the correspondence between interrupt mask registers and interrupt factor flags.

Table 4.16.2.1 Interrupt mask registers and interrupt factor flags

Interrupt mask register		Interrupt factor flag	
EIT3	(F6H•D3)	IT3	(FEH•D3)
EIT2	(F6H•D2)	IT2	(FEH•D2)
EIT1	(F6H•D1)	IT1	(FEH•D1)
EIT0	(F6H•D0)	IT0	(FEH•D0)
EIRUN	(F5H•D3)	IRUN	(FDH•D3)
EILAP	(F5H•D2)	ILAP	(FDH•D2)
EISW1	(F5H•D1)	ISW1	(FDH•D1)
EISW0	(F5H•D0)	ISW0	(FDH•D0)
EIPT	(F4H•D0)	IPT	(FCH•D0)
EISIF	(F3H•D0)	ISIF	(FBH•D0)
EIK0	(F2H•D0)	IK0	(FAH•D0)
EIK1	(F1H•D0)	IK1	(F9H•D0)
EIAD	(F0H•D0)	IAD	(F8H•D0)

4.16.3 Interrupt vector

When an interrupt request is input to the CPU, the CPU begins interrupt processing. After the program being executed is terminated, the interrupt processing is executed in the following order.

① The address data (value of program counter) of the program to be executed next is saved in the stack area (RAM).

② The interrupt request causes the value of the interrupt vector (page 1, 02H–0EH) to be set in the program counter.

③ The program at the specified address is executed (execution of interrupt processing routine by software).

Table 4.16.3.1 shows the correspondence of interrupt requests and interrupt vectors.

Note: The processing in ① and ② above take 12 cycles of the CPU system clock.

Table 4.16.3.1 Interrupt request and interrupt vectors

Interrupt vector	Interrupt request	Priority
102H	A/D converter	High
104H	K10–K13 input	↑
106H	K00–K03 input	
108H	Serial interface	
10AH	Programmable timer	
10CH	Stopwatch timer	↓
10EH	Clock timer	Low

The four low-order bits of the program counter are indirectly addressed through the interrupt request.

4.16.4 Control of interrupt

Tables 4.16.4.1(a) and (b) show the interrupt control bits and their addresses.

Table 4.16.4.1(a) Control bits of interrupt (1)

Address *7	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
90H	SIK03	SIK02	SIK01	SIK00	SIK03	0	Enable	Disable	Interrupt selection register (K03)
					SIK02	0	Enable	Disable	Interrupt selection register (K02)
					SIK01	0	Enable	Disable	Interrupt selection register (K01)
	R/W				SIK00	0	Enable	Disable	Interrupt selection register (K00)
92H	KCP03	KCP02	KCP01	KCP00	KCP03	0	↓	↑	Input comparison register (K00–K03)
					KCP02	0	↓	↑	
					KCP01	0	↓	↑	
	R/W				KCP00	0	↓	↑	
94H	SIK13	SIK12	SIK11	SIK10	SIK13	0	Enable	Disable	Interrupt selection register (K13)
					SIK12	0	Enable	Disable	Interrupt selection register (K12)
					SIK11	0	Enable	Disable	Interrupt selection register (K11)
	R/W				SIK10	0	Enable	Disable	Interrupt selection register (K10)
96H	KCP13	KCP12	KCP11	KCP10	KCP13	0	↓	↑	Input comparison register (K10–K13)
					KCP12	0	↓	↑	
					KCP11	0	↓	↑	
	R/W				KCP10	0	↓	↑	

*1 Initial value at the time of initial reset
*2 Not set in the circuit
*3 Undefined
*4 Reset (0) immediately after being read
*5 Constantly "0" when being read
*6 Refer to main manual
*7 Page switching in I/O memory is not necessary

Table 4.16.4.1(b) Control bits of interrupt (2)

Address *7	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
F0H	0	0	0	EIAD	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R			R/W	0 *5	– *2			Unused
					EIAD	0	Enable	Mask	Interrupt mask register (A/D converter)
F1H	0	0	0	EIK1	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R			R/W	0 *5	– *2			Unused
					EIK1	0	Enable	Mask	Interrupt mask register (K10–K13)
F2H	0	0	0	EIK0	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R			R/W	0 *5	– *2			Unused
					EIK0	0	Enable	Mask	Interrupt mask register (K00–K03)
F3H	0	0	0	EISIF	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R			R/W	0 *5	– *2			Unused
					EISIF	0	Enable	Mask	Interrupt mask register (Serial interface)
F4H	0	0	0	EIPT	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R			R/W	0 *5	– *2			Unused
					EIPT	0	Enable	Mask	Interrupt mask register (Programmable timer)
F5H	EIRUN	EILAP	EISW1	EISW0	EIRUN	0	Enable	Mask	Interrupt mask register (Stopwatch direct RUN)
					EILAP	0	Enable	Mask	Interrupt mask register (Stopwatch direct LAP)
	R/W				EISW1	0	Enable	Mask	Interrupt mask register (Stopwatch 1 Hz)
					EISW0	0	Enable	Mask	Interrupt mask register (Stopwatch 10 Hz)
F6H	EIT3	EIT2	EIT1	EIT0	EIT3	0	Enable	Mask	Interrupt mask register (Clock timer 2 Hz)
					EIT2	0	Enable	Mask	Interrupt mask register (Clock timer 8 Hz)
	R/W				EIT1	0	Enable	Mask	Interrupt mask register (Clock timer 16 Hz)
					EIT0	0	Enable	Mask	Interrupt mask register (Clock timer 32 Hz)
F8H	0	0	0	IAD	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R				0 *5	– *2			Unused
					IAD *4	0	Yes	No	Interrupt factor flag (A/D converter)
F9H	0	0	0	IK1	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R				0 *5	– *2			Unused
					IK1 *4	0	Yes	No	Interrupt factor flag (K10–K13)
FAH	0	0	0	IK0	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R				0 *5	– *2			Unused
					IK0 *4	0	Yes	No	Interrupt factor flag (K00–K03)
FBH	0	0	0	ISIF	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R				0 *5	– *2			Unused
					ISIF *4	0	Yes	No	Interrupt factor flag (Serial interface)
FCH	0	0	0	IPT	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R				0 *5	– *2			Unused
					IPT *4	0	Yes	No	Interrupt factor flag (Programmable timer)
FDH	IRUN	ILAP	ISW1	ISW0	IRUN *4	0	Yes	No	Interrupt factor flag (Stopwatch direct RUN)
					ILAP *4	0	Yes	No	Interrupt factor flag (Stopwatch direct LAP)
	R				ISW1 *4	0	Yes	No	Interrupt factor flag (Stopwatch 1 Hz)
					ISW0 *4	0	Yes	No	Interrupt factor flag (Stopwatch 10 Hz)
FEH	IT3	IT2	IT1	IT0	IT3 *4	0	Yes	No	Interrupt factor flag (Clock timer 2 Hz)
					IT2 *4	0	Yes	No	Interrupt factor flag (Clock timer 8 Hz)
	R				IT1 *4	0	Yes	No	Interrupt factor flag (Clock timer 16 Hz)
					IT0 *4	0	Yes	No	Interrupt factor flag (Clock timer 32 Hz)

*1 Initial value at the time of initial reset
*2 Not set in the circuit
*3 Undefined
*4 Reset (0) immediately after being read
*5 Constantly "0" when being read
*6 Refer to main manual
*7 Page switching in I/O memory is not necessary

EIT3, EIT2, EIT1, EIT0: Interrupt mask registers (F6H)
IT3, IT2, IT1, IT0: Interrupt factor flags (FEH)

..... See Section 4.9, "Clock Timer".

EIRUN, EILAP, EISW1, EISW0: Interrupt mask registers (F5H)
IRUN, ILAP, ISW1, ISW0: Interrupt factor flags (FDH)

..... See Section 4.10, "Stopwatch Timer".

EIPT: Interrupt mask register (F4H•D0)
IPT: Interrupt factor flag (FCH•D0)

..... See Section 4.11, "Programmable Timer".

EISIF: Interrupt mask register (F3H•D0)
ISIF: Interrupt factor flag (FBH•D0)

..... See Section 4.12, "Serial Interface".

KCP03–KCP00: Input comparison registers (92H)
SIK03–SIK00: Interrupt selection registers (90H)
EIK0: Interrupt mask register (F2H•D0)
IK0: Interrupt factor flag (FAH•D0)

..... See Section 4.5, "Input Ports".

KCP13–KCP10: Input comparison registers (96H)
SIK13–SIK10: Interrupt selection registers (94H)
EIK1: Interrupt mask register (F1H•D0)
IK1: Interrupt factor flag (F9H•D0)

..... See Section 4.5, "Input Ports".

EIAD: Interrupt mask register (F0H•D0)
IAD: Interrupt factor flag (F8H•D0)

..... See Section 4.14, "A/D Converter".

4.16.5 Programming notes

(1) The interrupt factor flags are set when the timing condition is established, even if the interrupt mask registers are set to "0".

(2) Reading of interrupt factor flags is available at EI, but be careful in the following cases.
If the interrupt mask register value corresponding to the interrupt factor flags to be read is set to "1", an interrupt request will be generated by the interrupt factor flags set timing, or an interrupt request will not be generated.

CHAPTER 5 SUMMARY OF NOTES

5.1 Notes for Low Current Consumption

The E0C6256 contains control registers for each of the circuits so that current consumption can be lowered. These control registers lower the current consumption through programs that operate the circuits at the minimum levels.
The following text explains the circuits that can control operation and their control registers. Refer to these when putting programs together.

Table 5.1.1 Circuits and control registers

Circuit (and Item)	Control register
CPU	HALT instruction
CPU operating frequency	CLKCHG, OSCC
Oscillation system regulated voltage circuit	VSCHG
LCD system regulated voltage circuit	LPWR, APWR
Voltage doubler/halver	DBON, HLON, VSEL
A/D converter	APWR
SVD circuit	SVDON

See Chapter 7, "ELECTRICAL CHARACTERISTICS", for order of current consumption.

Below are the circuit statuses at initial reset.

CPU: Operating status

CPU operating frequency: Low speed side (CLKCHG = "0"),
OSC3 oscillation circuit OFF status (OSCC = "0")

Oscillation system regulated voltage circuit: Low speed side, -1.05 V (VSCHG = "0")

LCD system regulated voltage circuit: OFF status (LPWR = "0", APWR = "0")

Voltage doubler/halver circuit: Regulated circuit is driven by VSS,
Normal mode (DBON = "0", HLON = "0", VSEL = "0")

A/D converter: OFF status (APWR = "0")

SVD circuit: OFF status (SVDON = "0")

Also, be careful about panel selection because the current consumption can differ by the order of several µA on account of the LCD panel characteristics.

5.2 Summary of Notes by Function

Here, the cautionary notes are summed up by function category. Keep these notes well in mind when programming.

Memory

Memory is not mounted in unused area within the memory map and in memory area not indicated in this manual. For this reason, normal operation cannot be assured for programs that have been prepared with access to these areas.

Operating mode and power supply control

(1) When the supply voltage is out of the specified voltage range of an operating mode, do not switch into the operating mode. It may cause malfunction or increase current consumption.

(2) Do not set HLON (halving) and DBON (doubling) to "1" at the same time.

(3) When switching from the normal mode to the doubler/halver mode, VSEL should be set to "1" wait 100 msec or more for the V_{S2} to stabilize after setting DBON or HLON to "1".

(4) When switching from the doubler/halver mode to the normal mode, use separate instructions to switch the mode (VSEL = "0") and turn the supply voltage doubler/halver OFF (HLON = "0" or DBON = "0"). Simultaneous processing with a single instruction may cause malfunction.

Watchdog timer

When the watchdog timer is being used, the software must reset it within 3-second cycles.

Oscillation circuit

(1) When switching the CPU system clock from OSC1 to OSC3, set V_{S1} to -2.1 V (VSCHG = "1") before turning the OSC3 oscillation ON.
When switching from OSC3 to OSC1, set V_{S1} to -1.05 V (VSCHG = "0") after switching to OSC1 and turning the OSC3 oscillation OFF.

(2) It takes at least 5 msec from the time the OSC3 oscillation circuit goes ON until the oscillation stabilizes. Consequently, when switching the CPU operation clock from OSC1 to OSC3, do this after a minimum of 5 msec have elapsed since the OSC3 oscillation went ON.
Further, the oscillation stabilization time varies depending on the external oscillator characteristics and conditions of use, so allow ample margin when setting the wait time.

OSC1 → OSC3
1. Set VSCHG to "1" (-1.05 V → -2.1 V)
2. Set OSCC to "1" (OSC3 oscillation ON)
3. Maintain 5 msec or more
4. Set CLKCHG to "1" (OSC1 → OSC3)

OSC3 → OSC1
1. Set CLKCHG to "0" (OSC3 → OSC1)
2. Set OSCC to "0" (OSC3 oscillation OFF)
3. Set VSCHG to "0" (-2.1 V → -1.05 V)

(3) When switching the clock form OSC3 to OSC1, use a separate instruction for turning the OSC3 oscillation OFF. An error in the CPU operation can result if this processing is performed at the same time by the one instruction.

(4) Switching the operating voltage when the supply voltage is lower than 2.2 V (absolute value) may cause a malfunction. Switch the operating voltage only after making sure that supply voltage is more than 2.2 V (absolute value) using the SVD circuit.
Do not switch the operating voltage during operating in the doubler mode or the halver mode, even if the V_{S2} voltage is more than 2.2 V (absolute value). The OSC3 clock can be used only in the normal mode.

Input ports

(1) When input ports are changed from high to low by pull down resistor, the fall of the waveform is delayed on account of the time constant of the pull down resistor and input gate capacitance. Hence, when fetching input ports, set an appropriate wait time.
Particular care needs to be taken of the key scan during key matrix configuration. Aim for a wait time of about 1 msec.

(2) When the input comparison register (KCP00–KCP03, KCP10–KCP13) is set, the interrupt factor flag (IK0, IK1) may be set to "1" depending on the status of the input port terminal. Consequently, when setting this register, do it in the DI status (interrupt flag = "0") and then read the interrupt factor flag in order to reset, or after setting the interrupt selection register (SIK00–SIK03, SIK10–SIK13) to the interrupt disabled status.

Output ports

(1) When R10–R12 are used for DC output, the special output enable registers FOUTE (C0H•D3), PTOE (CAH•D2) and BZE (DCH•D0) should be fixed at "0".

(2) When the special output is selected, the corresponding output port register (R10–R12) should be fixed at "0". Be sure that the output terminal is fixed at a high (V_{DD}) level the same with the DC output if "1" is written to the R10–R12 register when the special output has been selected.

(3) When BZ, FOUT and PTOVF are selected, a hazard may be observed in the output waveform when the data of the output register changes.

(4) When selecting f_{OSC3} as the FOUT clock frequency, it is necessary to control the OSC3 oscillation circuit and the oscillation system regulated voltage circuit.
See Section 4.4, "Oscillation Circuit" for details of the control.

I/O ports

When the I/O ports are changed from high to low by pull down resistor during input mode, the fall of the waveform is delayed on account of the time constant of the pull down resistor and input gate capacitance. Hence, when fetching input data, set an appropriate wait time.
Particular care needs to be taken of the key scan during key matrix configuration. Aim for a wait time of about 1 msec.

LCD driver

(1) The contents of the display memory are undefined until the area is initialized (through, for instance, memory clear processing by the CPU). Initialize the display memory by executing initial processing.

(2) When page 5 is selected for the display memory area, since the display memory area is write-only, display data cannot be rewritten by arithmetic operations (such as AND, OR, ADD, SUB).

(3) 100 msec or more time is necessary for stabilizing the LCD drive voltages V_{L1}, V_{L2} and V_{L3} after setting the LCD power control register LPWR to "1". Be careful of the segment-on right after the power is turned on.

Clock timer

(1) Be sure to data reading in the order of low-order data (TM0–TM3) then high-order data (TM4–TM7).

(2) When the clock timer has been reset, the interrupt factor flag (IT) may sometimes be set to "1". Consequently, perform flag reading (reset the flag) as necessary at reset.

Stopwatch timer

(1) The interrupt factor flag should be reset after resetting the stopwatch timer.

(2) Be sure to data reading in the order of SWL→SWM→SWH.

(3) When data that is held by a LAP input is read, read the capture buffer renewal flag CRNWF after reading the SWH and check whether the data has been renewed or not.

(4) When performing a processing such as a LAP input preceding with 1 Hz interrupt processing, read the LAP data carry-up request flag LCURF before processing and check whether carry-up is needed or not.

(5) When the interrupt factor flag ISW1 is set to "1", if reading it (reading FDH) before the capture buffer shifts into hold status, the LAP data carry-up request flag is not set to "1". Pay attention to the interrupt processing.

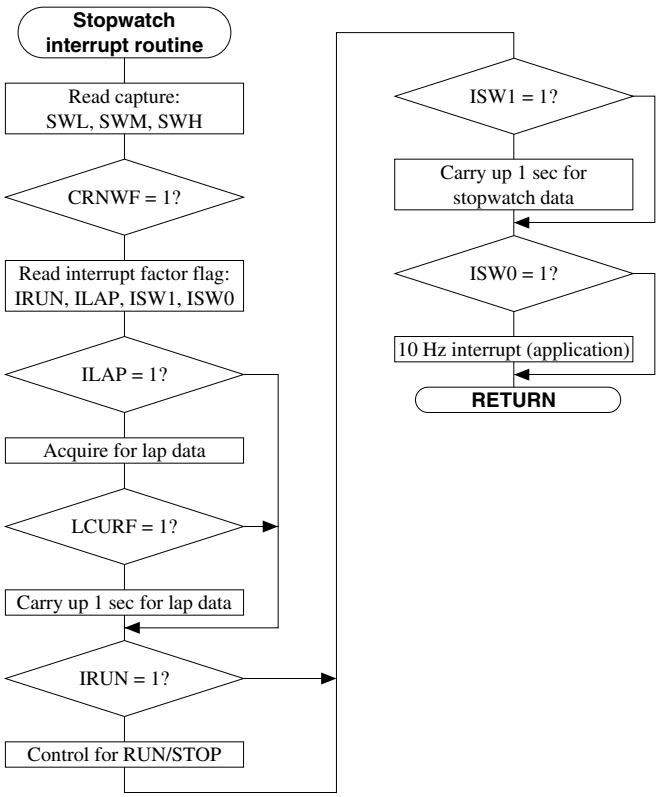


Fig. 5.2.1 Flow chart of stopwatch timer interrupt processing

Programmable timer

(1) Be sure to read the counter data in the order of low-order data (PT0–PT3) then high-order data (PT4–PT7).

(2) When data of reload registers is set at "00H", the down-counter becomes a 256-value counter.

(3) Set the V_{S1} voltage to -2.1 V (VSCHG = "1") when using the programmable timer as an event counter.

Serial interface

(1) When using the serial interface in the master mode, the synchronous clock uses the CPU system clock. Accordingly, do not change the system clock ($f_{OSC1} \leftrightarrow f_{OSC3}$) while the serial interface is operating.

(2) Perform data writing/reading to data registers SD0–SD7 only while the serial interface is halted (i.e., the synchronous clock is neither being input or output).

(3) As a trigger condition, it is required that data writing or reading on data registers SD0–SD7 be performed prior to writing "1" to SCTRG. (The internal circuit of the serial interface is initiated through data writing/reading on data registers SD0–SD7.) Supply trigger only once every time the serial interface is placed in the RUN state. Moreover, when the synchronous clock SCLK is external clock, start to input the external clock after the trigger.

(4) Set the V_{S1} voltage to -2.1 V (VSCHG = "1") when using the serial interface in slave mode.

Sound generator

(1) Pay attention to the output because it is fixed at HIGH level when the R12 register is set to "1".

(2) Since it generates a BZ signal that is out of synchronization with the BZE register, hazards may at times be produced when the signal goes ON/OFF due to the setting of the register.

(3) The one-shot output is only valid when the normal buzzer output is OFF (BZE = "0") and will be invalid when the normal buzzer output is ON (BZE = "1").

A/D converter

(1) Depending on the initial value of the up-counter C0–C19, the up-counter or the up/down counter may overflow while the CR oscillation clock is being counted. When setting the initial value, pay attention to CR oscillation frequency, its fluctuation range and the input clock frequency of the up/down counter. If an overflow occurs, A/D conversion is terminated immediately. When the A/D conversion result (up-counter value) is read, check the overflow flag.

(2) When the up/down counter TC0–TC15 is read after A/D conversion, it may not indicate "0000H". This is not due to incorrect timing in terminating A/D conversion but because the counting down clock is input after the control signal is output to the up-counter to terminate counting.

(3) When an interrupt occurs by the counter overflow, the same interrupt will occur if the overflow flag (OVF1 or OVF2) is not reset. Be sure to check and reset the overflow flag when the A/D converter interrupt occurs.

(4) When reading the up-counter data (TC0–TC15), be sure to read from the low-order address first.

(5) Pay attention when using the OSC3 oscillation clock as the input clock for the up/down counter. It is necessary to switch the V_{S1} output voltage, control the OSC3 oscillation circuit and switch the CPU clock.

(6) The A/D converter uses the LCD power supply as its power source. If starting A/D conversion when the LPWR register (C3H) has been set to "0" and the LCD power is OFF, the LCD power supply circuit activates at the time of the APWR register is set to "1". In such a case, be sure to secure 100 msec or more time to stabilize the power. (The LCD power supply is also turned ON by setting the APWR register to "1".) Setting of the APWR register (E0H) is necessary even if the LPWR register (C3H) has been set to "1" and the LCD power has already been turned ON. Be sure to set "1" prior to A/D conversion.

SVD circuit

(1) To obtain a stable SVD detection result, the SVD circuit must be on for at least l00 µsec. So, to obtain the SVD detection result, follow the programming sequence below.

① Set SVDON to "1"
② Maintain for 100 µsec minimum
③ Set SVDON to "0"
④ Read SVDDT

However, when f_{OSC1} is selected for CPU system clock, the instruction cycles are long enough, so there is no need to worry about maintaining 100 µsec for SVDON = "1" in the software.

(2) The SVD circuit should normally be turned OFF as the consumption current of the IC becomes large when it is ON.

(3) 1.05 V or 1.20 V of the 1.5 V system criteria voltage must be used in the doubler mode, so the doubler mode has to be set when using these criteria voltages. Using the normal mode may cause a malfunction or will be unable to detect the supply voltage correctly. See Section 4.2, "Power Supply and Operating Mode Settings" for the operating mode switching.

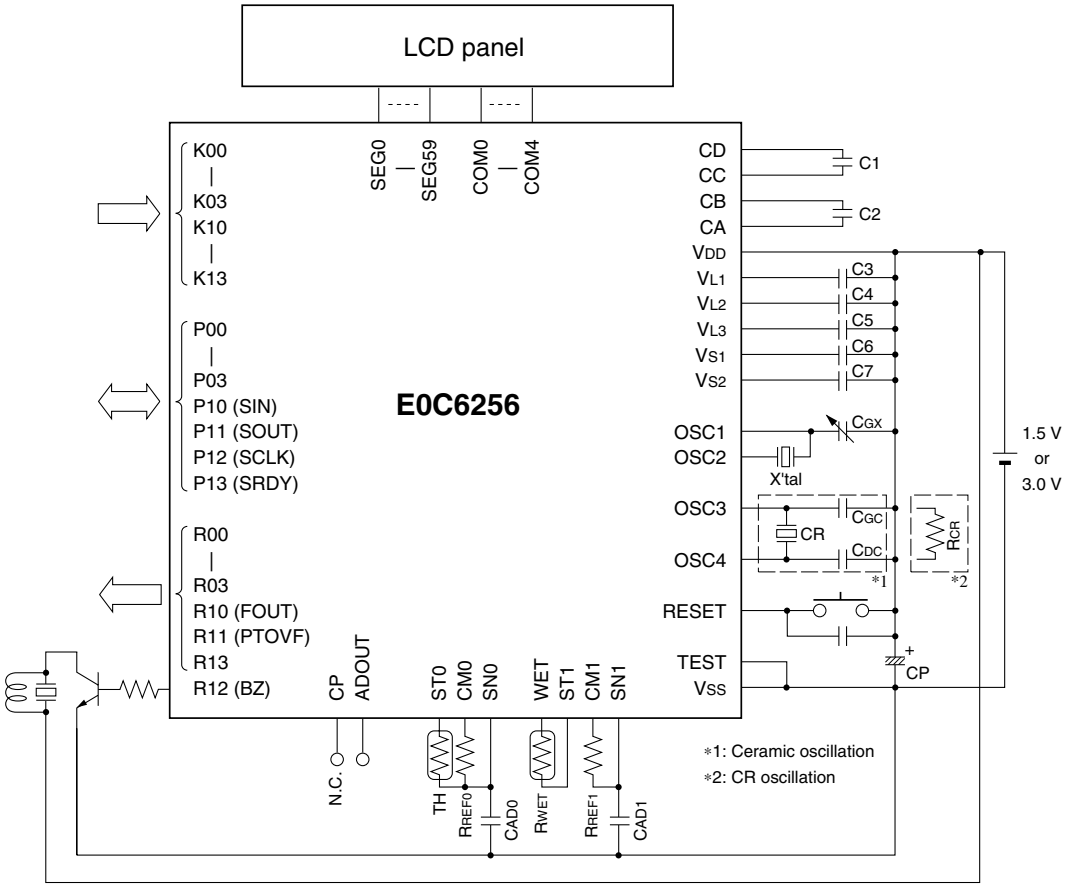
Interrupt and HALT

(1) The interrupt factor flags are set when the timing condition is established, even if the interrupt mask registers are set to "0".

(2) Reading of interrupt factor flags is available at EI, but be careful in the following cases.
If the interrupt mask register value corresponding to the interrupt factor flags to be read is set to "1", an interrupt request will be generated by the interrupt factor flags set timing, or an interrupt request will not be generated.

CHAPTER 6 DIAGRAM OF BASIC EXTERNAL CONNECTIONS

- **For temperature measurement using thermistor (CH0) and humidity measurement using resistive humidity sensor (CH1)**



X'tal	Crystal oscillator	32.768 kHz , CI (MAX) = 35 kΩ
C_{GX}	Trimmer capacitor	5–25 pF
CR	Ceramic oscillator	1 MHz
C_{GC}	Gate capacitor	100 pF
C_{DC}	Drain capacitor	100 pF
R_{CR}	Resistor for CR oscillation	40 kΩ ($f_{OSC3} \approx$ 900 kHz)
TH	Thermistor	Ishizuka Electronics Corp. 503-AT
R_{REF0}	Reference resistance for A/D conversion (CH0)	10 kΩ
C_{AD0}	Capacitor for A/D conversion (CH0)	2,200 pF
R_{WET}	Resistive humidity sensor	
R_{REF1}	Reference resistance for A/D conversion (CH1)	10 kΩ
C_{AD1}	Capacitor for A/D conversion (CH1)	2,200 pF
C1–C7 *	Capacitors	0.1 µF
CP	Capacitor	3.3 µF

* When the operating mode is only used at normal mode, the capacitors C1 and C7 are not necessary.

Note: • *The above table is simply an example, and is not guaranteed to work.*

• *In order to prevent unstable operation of the OSC1 oscillation circuit due to current leak between OSC1 and Vss, please keep enough distance between Vss and other signals on the board pattern.*

CHAPTER 7 ELECTRICAL CHARACTERISTICS

7.1 Absolute Maximum Rating

(V_{DD} = 0 V)

Item	Symbol	Rated value	Unit
Power voltage	V_{SS}	-7.0 to 0.5	V
Input voltage (1)	V_I	V_{SS} - 0.3 to 0.5	V
Input voltage (2)	V_{IOSC}	V_{S1} - 0.3 to 0.5	V
Permissible total output current *1	ΣI_{VSS}	10	mA
Operating temperature	Topr	-20 to 70	°C
Storage temperature	Tstg	-65 to 150	°C
Soldering temperature / time	Tsol	260°C, 10sec (lead section)	–
Permissible dissipation *2	P_D	250	mW

*1 The permissible total output current is the sum total of the current (average current) that simultaneously flows from the output pins (or is drawn in).

*2 In case of plastic package (QFP5-100pin, QFP5-128pin).

7.2 Recommended Operating Conditions

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Power voltage	V_{SS}	V_{DD} = 0 V	Normal mode (OSC3: OFF)	-3.6	-3.0/-1.5	-1.3	V
			Normal mode (OSC3: ON)	-3.6	-3.0	-2.2	V
			Halver mode	-3.6	-3.0	-2.55	V
			Doubler mode	-1.4	-1.1	-0.9	V
Oscillation frequency (1)	f_{OSC1}			–	32.768	–	kHz
Oscillation frequency (2)	f_{OSC3}	Duty 50±5%		300	1,000	1,200	kHz

7.3 DC Characteristics

Unless otherwise specified:

V_{DD} = 0 V, V_{SS} = -3.0 V, f_{OSC1} = 32.768 kHz, Ta = 25°C, V_{S1}/V_{L1}/V_{L2}/V_{L3} are internal voltage, C1–C7 = 0.1 µF

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
High level input voltage (1)	V_{IH1}		K00–K03, K10–K13 P00–P03, P10–P13	0.2·Vss		0	V
High level input voltage (2)	V_{IH2}		RESET, TEST	0.1·Vss		0	V
Low level input voltage (1)	V_{IL1}		K00–K03, K10–K13 P00–P03, P10–P13	Vss		0.8·Vss	V
Low level input voltage (2)	V_{IL2}		RESET, TEST	Vss		0.9·Vss	V
High level input current (1)	I_{IH1}	V_{IH1} = 0 V Without pull down resistor	K00–K03, K10–K13 P00–P03, P10–P13 RESET, TEST	0		0.5	µA
High level input current (2)	I_{IH2}	V_{IH2} = 0 V With pull down resistor	K00–K03, K10–K13 P00–P03, P10–P13 RESET, TEST	4		16	µA
Low level input current	I_{IL}	V_{IL} = Vss	K00–K03, K10–K13 P00–P03, P10–P13 RESET, TEST	-0.5		0	µA
High level output current	I_{OH1}	V_{OH1} = 0.1·Vss	P00–P03, P10–P13 R00–R03, R10–R13			-0.9	mA
Low level output current	I_{OL1}	V_{OL1} = 0.9·Vss	P00–P03, P10–P13 R00–R03, R10–R13	1.8			mA
Common output current	I_{OH2}	V_{OH2} = -0.05 V	COM0–COM4			-3	µA
	I_{OL2}	V_{OL2} = V_{L3} + 0.05 V		3			µA
Segment output current	I_{OH3}	V_{OH3} = -0.05 V	SEG0–SEG59			-3	µA
(during LCD output)	I_{OL3}	V_{OL3} = V_{L3} + 0.05 V		3			µA
Segment output current	I_{OH4}	V_{OH4} = 0.1·Vss	SEG0–SEG59			-200	µA
(during DC output)	I_{OL4}	V_{OL4} = 0.9·Vss		200			µA

Unless otherwise specified:

V_{DD} = 0 V, V_{SS} = -1.5 V, f_{OSC1} = 32.768 kHz, Ta = 25°C, V_{S1}/V_{L1}/V_{L2}/V_{L3} are internal voltage, C1–C7 = 0.1 µF

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
High level input voltage (1)	V_{IH1}		K00–K03, K10–K13 P00–P03, P10–P13	0.2·Vss		0	V
High level input voltage (2)	V_{IH2}		RESET, TEST	0.1·Vss		0	V
Low level input voltage (1)	V_{IL1}		K00–K03, K10–K13 P00–P03, P10–P13	Vss		0.8·Vss	V
Low level input voltage (2)	V_{IL2}		RESET, TEST	Vss		0.9·Vss	V
High level input current (1)	I_{IH1}	V_{IH1} = 0 V Without pull down resistor	K00–K03, K10–K13 P00–P03, P10–P13 RESET, TEST	0		0.5	µA
High level input current (2)	I_{IH2}	V_{IH2} = 0 V With pull down resistor	K00–K03, K10–K13 P00–P03, P10–P13 RESET, TEST	2		10	µA
Low level input current	I_{IL}	V_{IL} = Vss	K00–K03, K10–K13 P00–P03, P10–P13 RESET, TEST	-0.5		0	µA
High level output current	I_{OH1}	V_{OH1} = 0.1·Vss	P00–P03, P10–P13 R00–R03, R10–R13			-150	µA
Low level output current	I_{OL1}	V_{OL1} = 0.9·Vss	P00–P03, P10–P13 R00–R03, R10–R13	400			µA
Common output current	I_{OH2}	V_{OH2} = -0.05 V	COM0–COM4			-3	µA
	I_{OL2}	V_{OL2} = V_{L3} + 0.05 V		3			µA
Segment output current	I_{OH3}	V_{OH3} = -0.05 V	SEG0–SEG59			-3	µA
(during LCD output)	I_{OL3}	V_{OL3} = V_{L3} + 0.05 V		3			µA
Segment output current	I_{OH4}	V_{OH4} = 0.1·Vss	SEG0–SEG59			-100	µA
(during DC output)	I_{OL4}	V_{OL4} = 0.9·Vss		100			µA

7.4 Analog Characteristics and Consumed Current

Unless otherwise specified: V_{DD} = 0 V, V_{SS} = -1.5 V / -3.0 V, f_{OSC1} = 32.768 kHz, C_G = 25 pF, Ta = 25°C, V_{S1}/V_{L1}/V_{L2}/V_{L3} are internal voltage, C1–C7 = 0.1 µF, (During A/D operation: C = 2,200 pF, Reference resistance = 10 kΩ, Sensor = 10 kΩ)

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
LCD drive voltage *6	V_{L1}	Connect 1MΩ load resistor between V_{DD} and V_{L1} (Without panel load)	VLCHG2–VLCHG0 = "0"	-1.15	-1.05	-0.95	V
			VLCHG2–VLCHG0 = "1"	-1.20	-1.10	-1.00	V
			VLCHG2–VLCHG0 = "2"	-1.25	-1.15	-1.05	V
			VLCHG2–VLCHG0 = "3"	-1.30	-1.20	-1.10	V
			VLCHG2–VLCHG0 = "4"	-1.35	-1.25	-1.15	V
			VLCHG2–VLCHG0 = "5"	-1.40	-1.30	-1.20	V
			VLCHG2–VLCHG0 = "6"	-1.45	-1.35	-1.25	V
			VLCHG2–VLCHG0 = "7"	-1.50	-1.40	-1.30	V
	V_{L2}	Connect 1MΩ load resistor between V_{DD} and V_{L2} (Without panel load)		$2 \cdot V_{L1}$ - 0.1		$2 \cdot V_{L1} \times 0.9$	V
	V_{L3}	Connect 1MΩ load resistor between V_{DD} and V_{L3} (Without panel load)		$3 \cdot V_{L1}$ - 0.1		$3 \cdot V_{L1} \times 0.9$	V
SVD voltage (1)	V_{SVD1}	1.5 V system	SVDS1 = "0", SVDS0 = "0"	-1.10	-1.05	-1.00	V
			SVDS1 = "0", SVDS0 = "1"	-1.25	-1.20	-1.15	V
			SVDS1 = "1", SVDS0 = "0"	-1.40	-1.35	-1.30	V
			SVDS1 = "1", SVDS0 = "1"	-1.40	-1.35	-1.30	V
SVD voltage (2)	V_{SVD2}	3.0 V system	SVDS1 = "0", SVDS0 = "0"	-2.35	-2.30	-2.25	V
			SVDS1 = "0", SVDS0 = "1"	-2.50	-2.45	-2.40	V
			SVDS1 = "1", SVDS0 = "0"	-2.65	-2.60	-2.55	V
			SVDS1 = "1", SVDS0 = "1"	-2.65	-2.60	-2.55	V
SVD circuit response time	t_{SVD}					100	µsec
Power current consumption *1	I_{OP}	During HALT (32 kHz) Without panel load, OSCC = "0" VSCHG = "0"	Normal mode		1.2	2.5	µA
			Halver mode		650	1200	nA
			Doubler mode		2.5	5.0	µA
		During execution (32 kHz) *2 Without panel load, OSCC = "0" VSCHG = "0"	Normal mode		3.5	6.0	µA
			Halver mode		2.0	4.0	µA
			Doubler mode		7.5	15.0	µA
		During A/D operation (32 kHz, V_{SS} = -1.5 V) *3 Without panel load, OSCC = "0", VSCHG = "0", Normal mode			100	150	µA
		During A/D operation (32 kHz, V_{SS} = -3.0 V) *3 Without panel load, OSCC = "0", VSCHG = "0", Normal mode			200	300	µA
		During SVD operation (32 kHz) *4 Without panel load, OSCC = "0", VSCHG = "0", Normal mode			10	20	µA
		During execution (1 MHz, ceramic oscillation) *2 Without panel load			170	300	µA
		During execution (1 MHz, CR oscillation) *2 Without panel load *5			220	350	µA

*1 LPWR = "1", VLCHG2–VLCHG0 = "0", within the operating voltage in each operating mode.

*2 The A/D converter and SVD circuit are OFF status.

*3 The SVD circuit is OFF status. Current consumed during HALT (32 kHz, Normal mode) + A/D operating current

*4 The A/D converter is OFF status. Current consumed during HALT (32 kHz, Normal mode) + SVD operating current

*5 The value in χ MHz can be found by the following expression: I_{OP} (f_{OSC3} = χ MHz) = I_{OP} (f_{OSC3} = 1 MHz) × χ

*6 V_{SS}/$V_{S2} \leq V_{L1}$ - 0.2 V

7.5 Oscillation Characteristics

The oscillation characteristics change depending on the conditions (components used, board pattern, etc.). Use the following characteristics as reference values.

OSC1 crystal oscillation circuit

Unless otherwise specified:

V_{DD} = 0 V, V_{SS} = -1.5 V / -3.0 V, Crystal: C-002R (CI = 35 kΩ), C_G = 25 pF, C_D = built-in, Ta = 25°C

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Oscillation start voltage	Vsta	tsta ≤ 5 sec (Vss)		-1.35			V
Oscillation stop voltage	Vstp	tstp ≤ 10 sec (Vss)		-1.35 (-0.9) *1			V
Built-in capacitance (drain)	C_D	Including incidental capacitance inside IC			20		pF
Frequency/voltage deviation	∂f/∂V	Vss = -0.9 to -3.6 V	without VSCHG switching			5	ppm
			with VSCHG switching			10	ppm
Frequency/IC deviation	∂f/∂IC			-10		10	ppm
Frequency adjustment range	∂f/∂C_G	C_G = 5 to 25 pF		35	45		ppm
Harmonic oscillation start voltage	V_{hho}	C_G = 5 pF (Vss)				-3.5	V
Permitted leak resistance	R_{leak}	Between OSC1 and V_{DD}		200			MΩ

*1 Parentheses indicate value for operation in the doubler mode.

OSC3 CR oscillation circuit

Unless otherwise specified:

V_{DD} = 0 V, V_{SS} = -3.0 V, R_{CR} = 40 kΩ, Ta = 25°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation frequency dispersion	f_{OSC3}		-30	900 kHz	30	%
Oscillation start voltage	Vsta	(Vss)	-2.2			V
Oscillation start time	tsta	Vss = -2.2 to -3.6 V			3	msec
Oscillation stop voltage	Vstp	(Vss)	-2.2			V

OSC3 ceramic oscillation circuit

Unless otherwise specified:

V_{DD} = 0 V, V_{SS} = -3.0 V, Ceramic oscillator: 1 MHz, C_{GC} = C_{DC} = 100 pF, Ta = 25°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start voltage	Vsta	(Vss)	-2.2			V
Oscillation start time	tsta	Vss = -2.2 to -3.6 V			3	msec
Oscillation stop voltage	Vstp	(Vss)	-2.2			V

7.6 Characteristics Curves

(1) CR oscillation frequency characteristic

The oscillation characteristics change depending on the conditions (components used, board pattern, etc.). Use the following characteristics as reference values and evaluate the characteristics on the actual product.

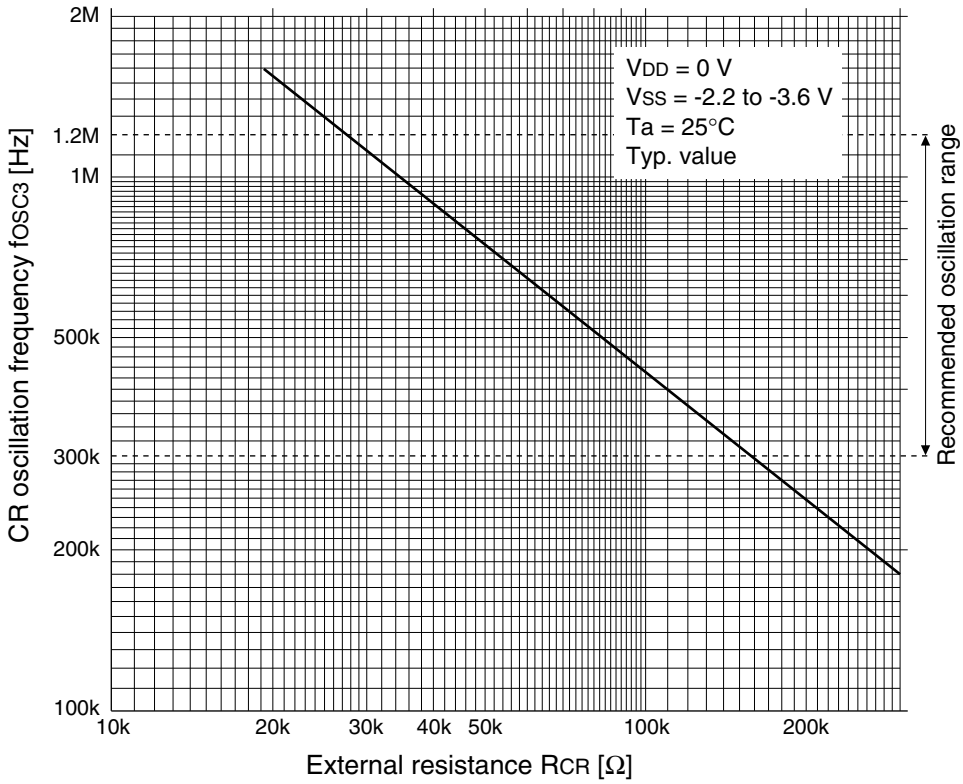


Fig. 7.6.1 CR oscillation characteristic

(2) A/D converter Sensor resistance-Oscillation frequency ratio characteristic

Figure 7.6.2 shows the oscillation frequency ratio (ratio of oscillation frequency by the reference resistance to oscillation frequency by the sensor resistance) when the following elements are connected. (Typ.)

Reference resistance ..... 10 kΩ
Sensor resistance ..... 10 kΩ to 20 MΩ
Oscillating capacitor ..... 2,200 pF

Note: If the R/f conversion uses a resistive sensor for channel 0 and channel 1, and the R/f conversion uses a resistive humidity sensor for channel 1, both characteristics will be the same.

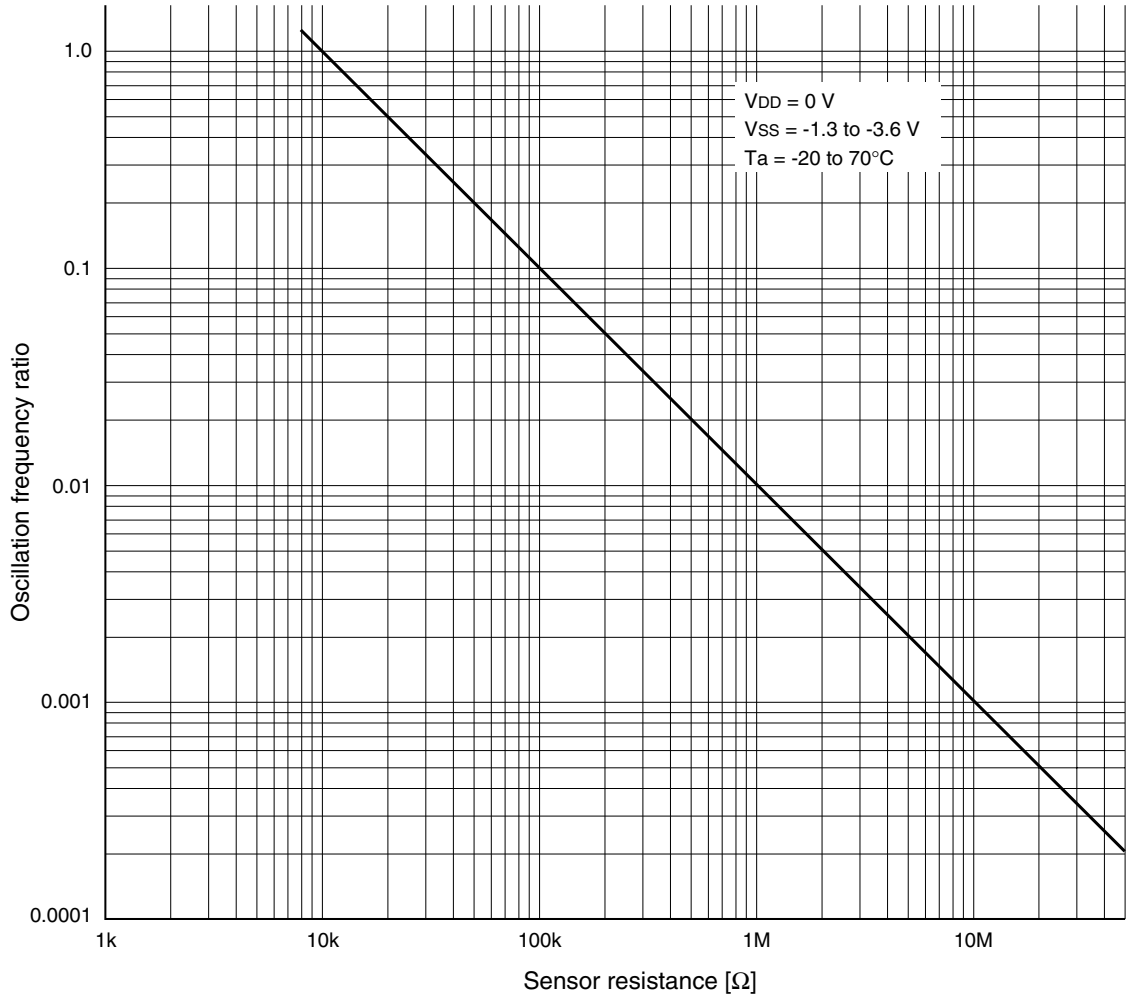


Fig. 7.6.2 Sensor resistance-oscillation frequency ratio curve

(3) A/D converter Resistance-Oscillation frequency characteristic

CR oscillation frequency of the A/D converter disperses in each sampling. Therefore, the count number of the up-counter should be decided after considering the fluctuation margin of the CR oscillation frequency by the reference resistance and sensor resistance to be used for the measurement. Figure 7.6.3 shows the resistance-oscillation frequency curve.

Note:
- *The following curves are characteristic when the oscillating capacitor is 2,200 pF.*
- *Typical oscillation frequency is characteristic when V_{SS} = -3.0 V.*
- *The resistance value applies to both reference resistance and sensor resistance.*
- *If the R/f conversion uses a resistive sensor for channel 0 and channel 1, and the R/f conversion uses a resistive humidity sensor for channel 1, both characteristics will be the same.*

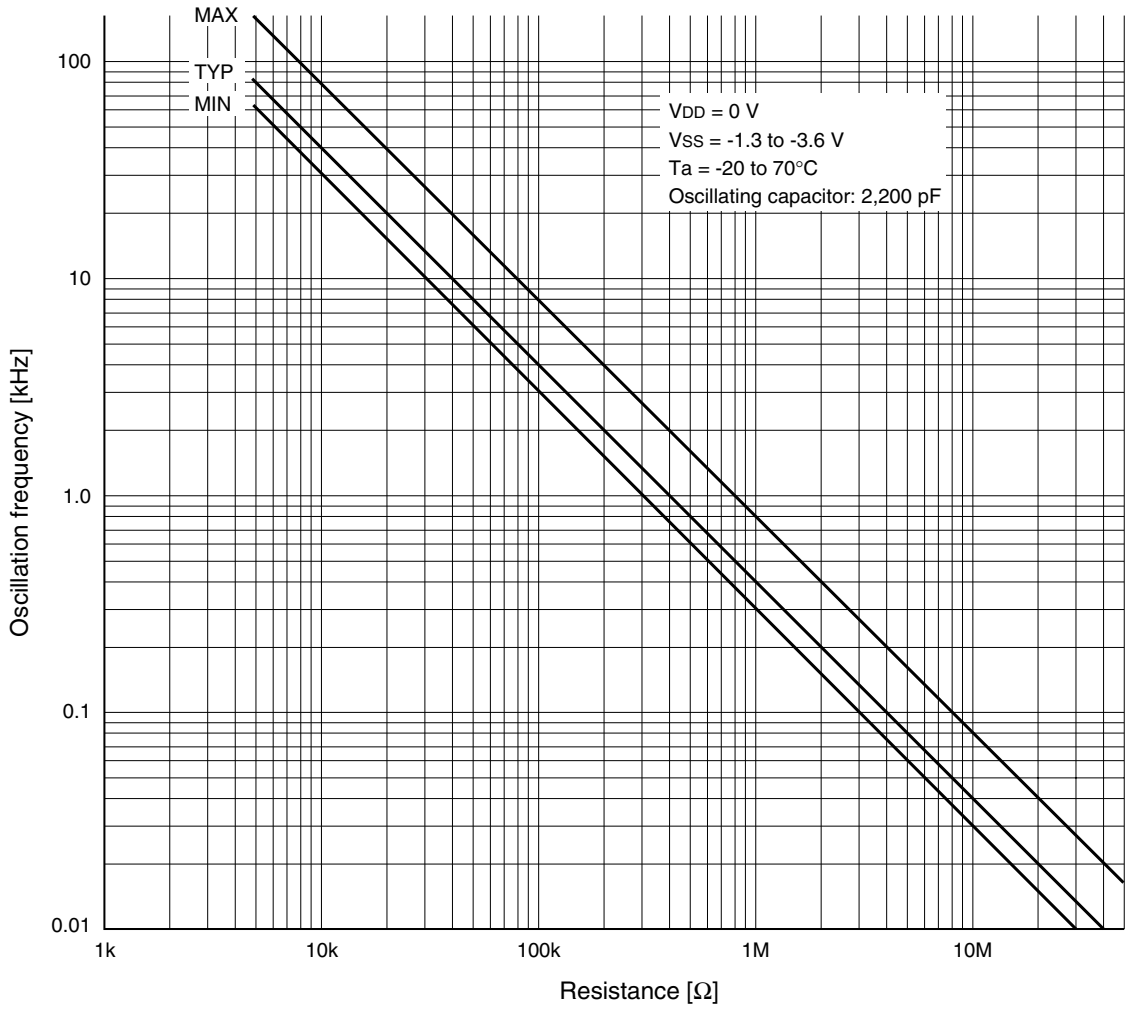


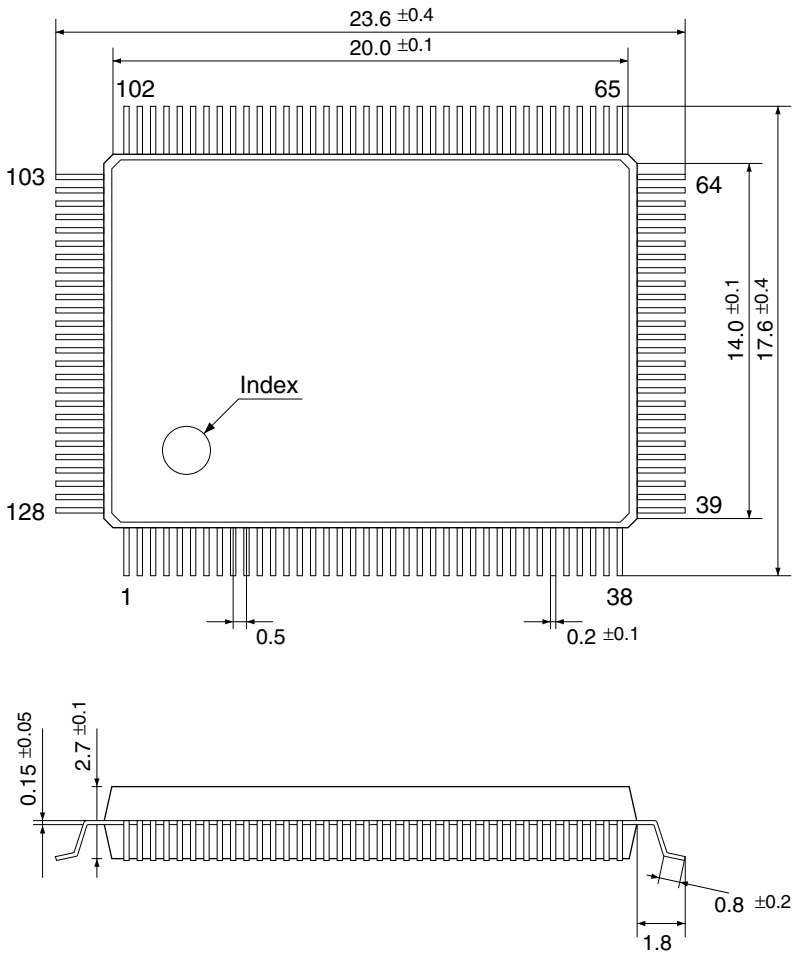
Fig. 7.6.3 Resistance-oscillation frequency curve

CHAPTER 8 PACKAGE

8.1 Plastic Package

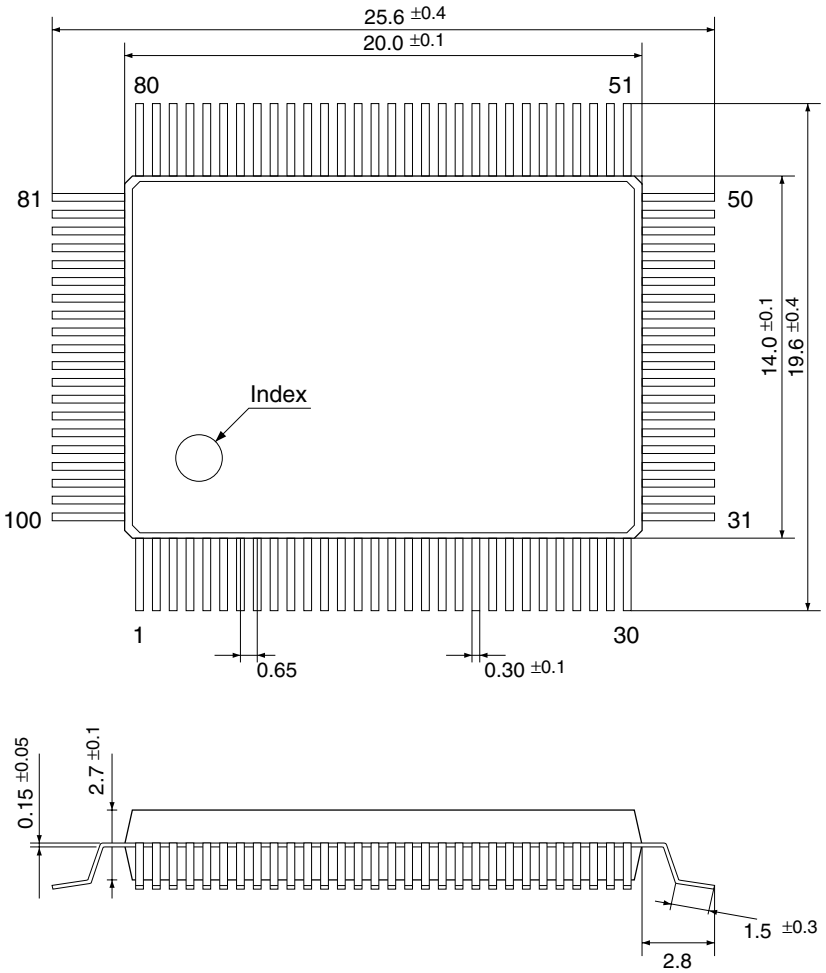
QFP5-128pin

(Unit: mm)



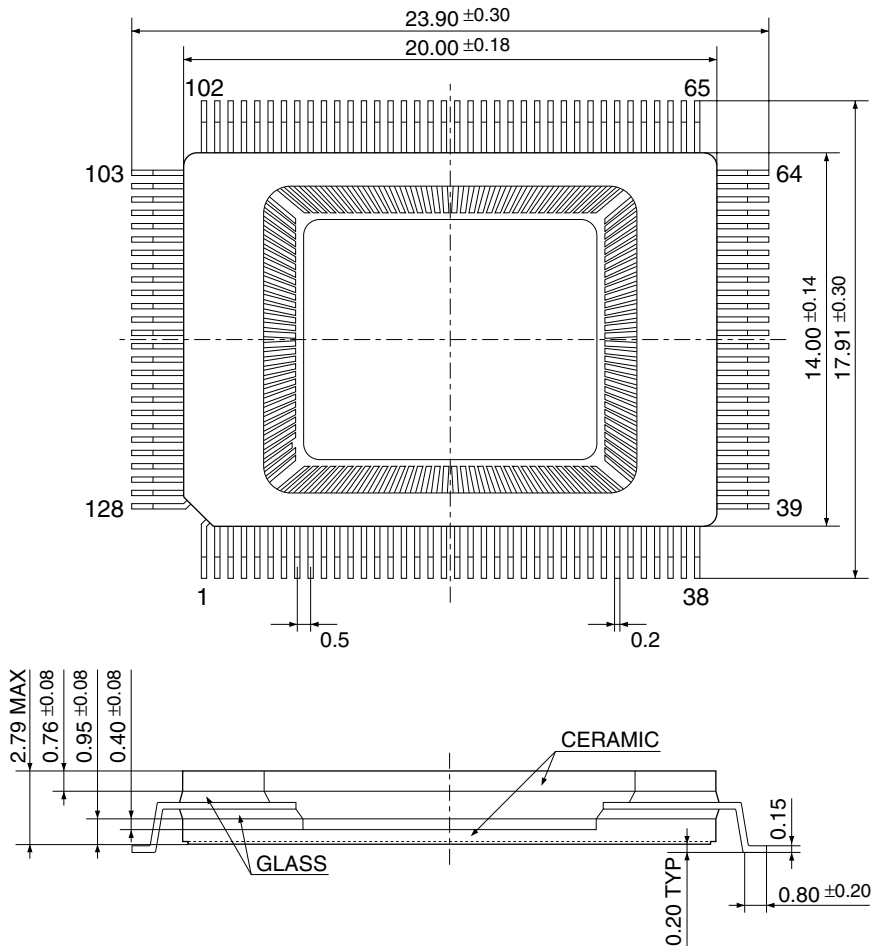
QFP5-100pin

(Unit: mm)



8.2 Ceramic Package for Test Samples

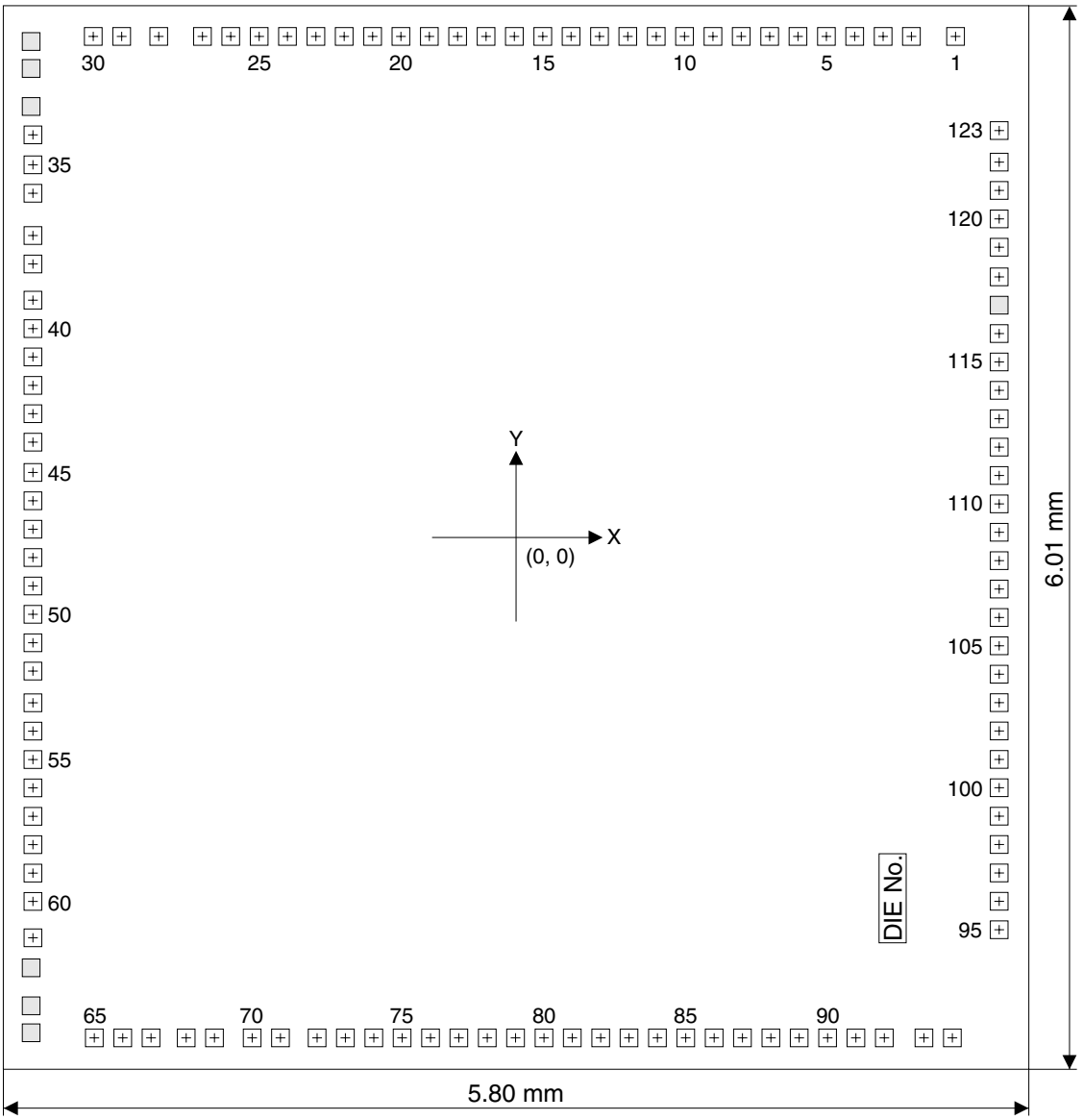
(Unit: mm)



Note: The ceramic package is fixed in this form regardless selecting of the plastic package form.

CHAPTER 9 PAD LAYOUT

9.1 Diagram of Pad Layout



Chip thickness: 400 µm
Pad opening: 100 µm

9.2 Pad Coordinates

(Unit: µm)

Pad		Coordinate		Pad		Coordinate		Pad		Coordinate	
No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y
1	SEG30	2486	2830	42	K11	-2732	858	83	SEG18	639	-2830
2	SEG31	2236	2830	43	K12	-2732	698	84	SEG19	800	-2830
3	SEG32	2076	2830	44	K13	-2732	537	85	SEG20	960	-2830
4	SEG33	1915	2830	45	R00	-2732	366	86	SEG21	1120	-2830
5	SEG34	1755	2830	46	R01	-2732	206	87	SEG22	1280	-2830
6	SEG35	1594	2830	47	R02	-2732	45	88	SEG23	1441	-2830
7	SEG36	1434	2830	48	R03	-2732	-115	89	SEG24	1601	-2830
8	SEG37	1274	2830	49	R10	-2732	-276	90	SEG25	1762	-2830
9	SEG38	1114	2830	50	R11	-2732	-436	91	SEG26	1922	-2830
10	SEG39	953	2830	51	R12	-2732	-597	92	SEG27	2083	-2830
11	SEG40	793	2830	52	R13	-2732	-757	93	SEG28	2307	-2830
12	SEG41	632	2830	53	P00	-2732	-936	94	SEG29	2468	-2830
13	SEG42	472	2830	54	P01	-2732	-1096	95	COM0	2732	-2218
14	SEG43	311	2830	55	P02	-2732	-1257	96	COM1	2732	-2058
15	SEG44	151	2830	56	P03	-2732	-1417	97	COM2	2732	-1898
16	SEG45	-10	2830	57	P10	-2732	-1578	98	COM3	2732	-1737
17	SEG46	-170	2830	58	P11	-2732	-1738	99	COM4	2732	-1577
18	SEG47	-330	2830	59	P12	-2732	-1898	100	CB	2732	-1416
19	SEG48	-490	2830	60	P13	-2732	-2058	101	CA	2732	-1256
20	SEG49	-651	2830	61	V_{SS}	-2732	-2264	102	V_{L3}	2732	-1095
21	SEG50	-811	2830	62	—*	-2742	-2434	103	V_{L2}	2732	-935
22	SEG51	-972	2830	63	—*	-2742	-2648	104	V_{L1}	2732	-774
23	SEG52	-1132	2830	64	—*	-2742	-2801	105	CC	2732	-614
24	SEG53	-1293	2830	65	SEG0	-2385	-2830	106	CD	2732	-454
25	SEG54	-1453	2830	66	SEG1	-2224	-2830	107	V_{S2}	2732	-293
26	SEG55	-1614	2830	67	SEG2	-2064	-2830	108	V_{SS}	2732	-133
27	SEG56	-1774	2830	68	SEG3	-1866	-2830	109	ADOUT	2732	28
28	SEG57	-2021	2830	69	SEG4	-1706	-2830	110	SN1	2732	188
29	SEG58	-2230	2830	70	SEG5	-1492	-2830	111	WET	2732	348
30	SEG59	-2391	2830	71	SEG6	-1332	-2830	112	ST1	2732	509
31	—*	-2742	2801	72	SEG7	-1125	-2830	113	CM1	2732	669
32	—*	-2742	2648	73	SEG8	-965	-2830	114	SN0	2732	830
33	—*	-2742	2434	74	SEG9	-804	-2830	115	CM0	2732	990
34	V_{DD}	-2732	2273	75	SEG10	-644	-2830	116	ST0	2732	1150
35	RESET	-2732	2104	76	SEG11	-484	-2830	117	CP	2732	1311
36	TEST	-2732	1943	77	SEG12	-324	-2830	118	V_{DD}	2732	1471
37	K00	-2732	1704	78	SEG13	-163	-2830	119	OSC1	2732	1638
38	K01	-2732	1544	79	SEG14	-3	-2830	120	OSC2	2732	1798
39	K02	-2732	1339	80	SEG15	158	-2830	121	OSC3	2732	1959
40	K03	-2732	1178	81	SEG16	318	-2830	122	OSC4	2732	2119
41	K10	-2732	1018	82	SEG17	479	-2830	123	V_{S1}	2732	2298

* Do not bond No. 31–33 and 62–64 pads because they are used only for factory testing.

II. E0C6256 Technical Software

CONTENTS

CHAPTER 1 INITIAL RESET

1.1 Internal Register Status on Initial Reset

Following an initial reset, the internal registers and internal data memory area are initialized to the values shown in Tables 1.1.1 and 1.1.2.

Table 1.1.1 Initial values of internal registers

CPU core			
Name	Symbol	Number of bits	Setting value
Program counter step	PCS	8	00H
Program counter page	PCP	4	1H
Program counter bank	PCB	1	0
New page pointer	NPP	4	1H
New bank pointer	NBP	1	0
Stack pointer	SP	8	Undefined
Index register IX	IX	11	Undefined
Index register IY	IY	11	Undefined
Register pointer	RP	4	Undefined
General-purpose register A	A	4	Undefined
General-purpose register B	B	4	Undefined
Interrupt flag	I	1	0
Decimal flag	D	1	0
Zero flag	Z	1	Undefined
Carry flag	C	1	Undefined

Table 1.1.2 Initial values of internal data memory area

Peripheral circuits		
Name	Number of bits	Setting value
RAM	4	Undefined
Display memory	4	Undefined
Other peripheral circuits	—	*

* See Tables 1.1.3(a)–(h)

Table 1.1.3(a) I/O memory map (80H–84H)

Address *7	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
80H	0	0	SVDS1	SVDS0	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R		R/W		SVDS1	0			SVD criteria voltage setting (1.5 V/3.0 V)
					SVDS0	0			0: 1.05/2.30, 1: 1.20/2.45, 2 & 3: 1.35/2.60 (V)
81H	0	0	SVDDT	SVDON	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R			R/W	SVDDT	0	Low	Normal	Supply voltage detection data
					SVDON	0	On	Off	SVD circuit On/Off
82H	0	VSEL	HLON	DBON	0 *5	– *2			Unused
					VSEL	0	V_{S2}	V_{SS}	Voltage regulator power source selection
	R	R/W			HLON	0	On	Off	Halver On/Off
					DBON	0	On	Off	Doubler On/Off
83H	0	CLKCHG	OSCC	VSCHG	0 *5	– *2			Unused
					CLKCHG	0	OSC3	OSC1	CPU clock selection
	R	R/W			OSCC	0	On	Off	OSC3 oscillation On/Off
					VSCHG	0	-2.1V	-1.05V	V_{S1} output voltage change
84H	0	VLCHG2	VLCHG1	VLCHG0	0 *5	– *2			Unused
					VLCHG2	0			V_{L1} output voltage change
	R	R/W			VLCHG1	0			0: 1.05, 1: 1.10, 2: 1.15, 3: 1.20,
					VLCHG0	0			4: 1.25, 5: 1.30, 6: 1.35, 7: 1.40 (V)

Table 1.1.3(b) I/O memory map (90H–96H)

Address *7	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
90H	SIK03	SIK02	SIK01	SIK00	SIK03	0	Enable	Disable	Interrupt selection register (K03)
					SIK02	0	Enable	Disable	Interrupt selection register (K02)
	R/W				SIK01	0	Enable	Disable	Interrupt selection register (K01)
					SIK00	0	Enable	Disable	Interrupt selection register (K00)
91H	K03	K02	K01	K00	K03	– *2	High	Low	Input port (K00–K03)
					K02	– *2	High	Low	
	R				K01	– *2	High	Low	
					K00	– *2	High	Low	
92H	KCP03	KCP02	KCP01	KCP00	KCP03	0	↓	↑	Input comparison register (K00–K03)
					KCP02	0	↓	↑	
	R/W				KCP01	0	↓	↑	
					KCP00	0	↓	↑	
94H	SIK13	SIK12	SIK11	SIK10	SIK13	0	Enable	Disable	Interrupt selection register (K13)
					SIK12	0	Enable	Disable	Interrupt selection register (K12)
	R/W				SIK11	0	Enable	Disable	Interrupt selection register (K11)
					SIK10	0	Enable	Disable	Interrupt selection register (K10)
95H	K13	K12	K11	K10	K13	– *2	High	Low	Input port (K10–K13)
					K12	– *2	High	Low	
	R				K11	– *2	High	Low	
					K10	– *2	High	Low	
96H	KCP13	KCP12	KCP11	KCP10	KCP13	0	↓	↑	Input comparison register (K10–K13)
					KCP12	0	↓	↑	
	R/W				KCP11	0	↓	↑	
					KCP10	0	↓	↑	

*1 Initial value at the time of initial reset
*2 Not set in the circuit
*3 Undefined
*4 Reset (0) immediately after being read
*5 Constantly "0" when being read
*6 Refer to main manual
*7 Page switching in I/O memory is not necessary

Table 1.1.3(c) I/O memory map (A0H–A3H)

Address *7	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
A0H	0	0	0	R0HIZ	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R			R/W	0 *5	– *2			Unused
					R0HIZ	0	High-Z	Output	R0 output high-impedance control
A1H	R03	R02	R01	R00	R03	0	High	Low	Output port (R00–R03)
					R02	0	High	Low	
	R/W				R01	0	High	Low	
					R00	0	High	Low	
A2H	0	0	0	R1HIZ	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R			R/W	0 *5	– *2			Unused
					R1HIZ	0	High-Z	Output	R1 output high-impedance control
A3H	R13	R12	R11	R10	R13	0	High	Low	Output port (R13)
					R12	0	High	Low	Output port (R12)
		BZ	PTOVF	FOUT	BZ	0	Off	On	Buzzer output
	R/W				R11	0	High	Low	Output port (R11)
					PTOVF	0	Off	On	PTOVF output
					R10	0	High	Low	Output port (R10)
					FOUT	0	Off	On	FOUToutput

Table 1.1.3(d) I/O memory map (B0H–B6H)

Address *7	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
B0H	IOC03	IOC02	IOC01	IOC00	IOC03	0	Output	Input	I/O control register (P00–P03)
					IOC02	0	Output	Input	
	R/W				IOC01	0	Output	Input	
					IOC00	0	Output	Input	
B1H	PUL03	PUL02	PUL01	PUL00	PUL03	1	On	Off	Pull down control register (P00–P03)
					PUL02	1	On	Off	
	R/W				PUL01	1	On	Off	
					PUL00	1	On	Off	
B2H	P03	P02	P01	P00	P03	– *2	High	Low	I/O port (P00–P03)
					P02	– *2	High	Low	
	R/W				P01	– *2	High	Low	
					P00	– *2	High	Low	
B4H	IOC13	IOC12	IOC11	IOC10	IOC13	0	Output	Input	I/O control register (P10–P13) (ESIF = 0)
					IOC12	0	Output	Input	
	R/W				IOC11	0	Output	Input	
					IOC10	0	Output	Input	
	When the serial I/F is used (ESIF = 1):				IOC13	0	Output	Input	Master mode: P13 I/O control register
	P10 = SIN (in), P11 = SOUT (out),				IOC13	0	1	0	Slave mode: General-purpose register
	P12 = SCLK (master: out, slave: in),				IOC12	0	1	0	General-purpose register
	P13 = SRDY (slave: out),				IOC11	0	1	0	
	P13 = I/O port (master: in/out)				IOC10	0	1	0	
B5H	PUL13	PUL12	PUL11	PUL10	PUL13	1	On	Off	Pull down control register (P10–P13) (ESIF = 0)
					PUL12	1	On	Off	
	R/W				PUL11	1	On	Off	
					PUL10	1	On	Off	
	When the serial I/F is used (ESIF = 1):				PUL13	1	On	Off	Master mode: P13 pull down control register
	P10 = SIN (in), P11 = SOUT (out),				PUL13	1	1	0	Slave mode: General-purpose register
	P12 = SCLK (master: out, slave: in),				PUL12	1	1	0	Master mode: General-purpose register
	P13 = SRDY (slave: out),				PUL12	1	On	Off	Slave mode: SCKL pull down control register
	P13 = I/O port (master: in/out)				PUL11	1	1	0	General-purpose register
					PUL10	1	On	Off	SIN pull down control register
B6H	P13	P12	P11	P10	P13	– *2	High	Low	I/O port (P10–P13) (ESIF = 0)
					P12	– *2	High	Low	
	R/W				P11	– *2	High	Low	
					P10	– *2	High	Low	
	When the serial I/F is used (ESIF = 1):				P13	– *2	High	Low	Master mode: I/O port P13
	P10 = SIN (in), P11 = SOUT (out),				P13	– *2	1	0	Slave mode: General-purpose register
	P12 = SCLK (master: out, slave: in),				P12	– *2	1	0	General-purpose register
	P13 = SRDY (slave: out),				P11	– *2	1	0	
	P13 = I/O port (master: in/out)				P10	– *2	1	0	

Table 1.1.3(e) I/O memory map (C0H–CEH)

Address *7	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
C0H	FOUTE	0	FOFQ1	FOFQ0	FOUTE	0	Enable	Disable	FOUT output enable
					0 *5	– *2			Unused
	R/W	R	R/W		FOFQ1	0			FOUT frequency selection
					FOFQ0	0			0: 512 Hz, 1: 4096 Hz, 2: fosc1, 3: fosc3
C1H	0	0	0	WDRST	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R			W	0 *5	– *2			Unused
					WDRST *5	Reset	Reset	–	Wachdog timer reset
C2H	LDMS	STCD	LDTY1	LDTY0	LDMS	0	1p(R/W)	5p(W)	LCD data memory area selection
					STCD	0	Static	Dynamic	LCD drive switch
	R/W				LDTY1	0			LCD drive duty selection
					LDTY0	0			0: 1/2, 1: 1/3, 2: 1/4, 3: 1/5
C3H	0	0	LOFF	LPWR	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R		R/W		LOFF	0	All Off	Normal	LCD display control
					LPWR	0	On	Off	LCD power supply On/Off
C4H	0	0	TMRUN	TMRST	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R		R/W	W	TMRUN	0	Run	Stop	Clock timer Run/Stop
					TMRST *5	Reset	Reset	–	Clock timer reset
C5H	TM3	TM2	TM1	TM0	TM3	0			Clock timer data (16 Hz)
					TM2	0			Clock timer data (32 Hz)
	R				TM1	0			Clock timer data (64 Hz)
					TM0	0			Clock timer data (128 Hz)
C6H	TM7	TM6	TM5	TM4	TM7	0			Clock timer data (1 Hz)
					TM6	0			Clock timer data (2 Hz)
	R				TM5	0			Clock timer data (4 Hz)
					TM4	0			Clock timer data (8 Hz)
C8H	0	0	PTPS1	PTPS0	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R		R/W		PTPS1	0			Prog. timer prescaler selection
					PTPS0	0			0: 1/1, 1: 1/4, 2: 1/32, 3: 1/256
C9H	0	0	PTPC1	PTPC0	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R		R/W		PTPC1	0			Prog. timer prescaler clock source selection
					PTPC0	0			0: OSC1, 1: OSC3, 2: K02, 3: K02(NR)
CAH	PNRFS	PTOE	PTRUN	PTRST	PNRFS	0	1024Hz	256Hz	Noise rejector clock frequency selection
					PTOE	0	Enable	Disable	PTOVF output enable
	R/W			W	PTRUN	0	Run	Stop	Programmable timer Run/Stop
					PTRST *5	Rst (reload)	Rst (reload)	–	Programmable timer reset (reload)
CBH	RD3	RD2	RD1	RD0	RD3	0			MSB
					RD2	0			Programmable timer reload data
	R/W				RD1	0			(low-order 4 bits)
					RD0	0			LSB
CCH	RD7	RD6	RD5	RD4	RD7	0			MSB
					RD6	0			Programmable timer reload data
	R/W				RD5	0			(high-order 4 bits)
					RD4	0			LSB
CDH	PT3	PT2	PT1	PT0	PT3	0			MSB
					PT2	0			Programmable timer data
	R				PT1	0			(low-order 4 bits)
					PT0	0			LSB
CEH	PT7	PT6	PT5	PT4	PT7	0			MSB
					PT6	0			Programmable timer data
	R				PT5	0			(high-order 4 bits)
					PT4	0			LSB

Table 1.1.3(f) I/O memory map (D0H–DFH)

Address *7	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
D0H	EDIR	DKM2	DKM1	DKM0	EDIR	0	Enable	Disable	Enable direct input function
					DKM2	0			Direct key mask factor 0: Non, 1: K02,
	R/W				DKM1	0			2: K02-03, 3: K02-03-10, 4: K10, 5: K10-11,
					DKM0	0			6: K10-11-12, 7: K10-11-12-13
D1H	LCURF	CRNWF	SWRUN	SWRST	LCURF	0	Reqest	No	Lap data carry-up request flag
					CRNWF	0	Renewal	No	Capture renewal flag
	R		R/W	W	SWRUN	0	Run	Stop	Stopwatch timer Run/Stop
					SWRST *5	Reset	Reset	–	Stopwatch timer reset
D2H	SWL3	SWL2	SWL1	SWL0	SWL3	0			MSB
					SWL2	0			Stopwatch timer data 1/1000 sec (BCD)
	R				SWL1	0			
					SWL0	0			LSB
D3H	SWM3	SWM2	SWM1	SWM0	SWM3	0			MSB
					SWM2	0			Stopwatch timer data 1/100 sec (BCD)
	R				SWM1	0			
					SWM0	0			LSB
D4H	SWH3	SWH2	SWH1	SWH0	SWH3	0			MSB
					SWH2	0			Stopwatch timer data 1/10 sec (BCD)
	R				SWH1	0			
					SWH0	0			LSB
D8H	0	0	SCTRG	ESIF	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R		R/W		SCTRG(W)	– *2	Trigger	–	Serial interface clock trigger (writing)
					SCTRG(R)	0	Run	Stop	Serial interface clock status (reading)
					ESIF	0	SIF port	I/O port	P1 port function selection
D9H	SDP	SCPS	SCS1	SCS0	SDP	0	LSB first	MSB first	Serial data input/output permutation
					SCPS	0	↑	↓	Serial interface clock phase selection
	R/W				SCS1	0			Serial interface clock mode selection
					SCS0	0			0: Slave, 1: PTOVF, 2: CLK/2, 3: CLK
DAH	SD3	SD2	SD1	SD0	SD3	– *3			MSB
					SD2	– *3			Serial interface data (low-order 4 bits)
	R/W				SD1	– *3			
					SD0	– *3			LSB
DBH	SD7	SD6	SD5	SD4	SD7	– *3			MSB
					SD6	– *3			Serial interface data (high-order 4 bits)
	R/W				SD5	– *3			
					SD4	– *3			LSB
DCH	ENRTM	ENRST	ENON	BZE	ENRTM	0	1sec	0.5sec	Envelope releasing time
					ENRST *5	Reset	Reset	–	Envelope reset
	R/W	W	R/W		ENON	0	On	Off	Envelope On/Off
					BZE	0	Enable	Disable	Buzzer output enable
DDH	0	BZSTP	BZSHT	SHTPW	0 *5	– *2			Unused
					BZSTP *5	– *2	Stop	–	1-shot buzzer stop
	R	W	R/W		BZSHT(W)	– *2	Trigger	–	1-shot buzzer trigger (writing)
					BZSHT(R)	0	Busy	Ready	1-shot buzzer status (reading)
					SHTPW	0	125msec	31.25msec	1-shot buzzer pulse width setting
DEH	0	BZFQ2	BZFQ1	BZFQ0	0 *5	– *2			Unused
					BZFQ2	0			Buzzer frequency selection
	R	R/W			BZFQ1	0			0: 4096.0, 1: 3276.8, 2: 2730.7, 3: 2340.6,
					BZFQ0	0			4: 2048.0, 5: 1638.4, 6: 1365.3, 7: 1170.3 (Hz)
DFH	0	BDTY2	BDTY1	BDTY0	0 *5	– *2			Unused
					BDTY2	0			Buzzer signal duty ratio selection *6
	R	R/W			BDTY1	0			
					BDTY0	0			

Table 1.1.3(g) I/O memory map (E0H–ECH)

Address *7	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
E0H	0	APWR	SENSEL	ADMODE	0 *5	– *2			Unused
					APWR	0	On	Off	A/D converter power supply On/Off
	R	R/W			SENSEL	0	Sensor	Reference	Sensor/reference resistance selection
					ADMODE	0	Continuous	Normal	A/D converter operation mode selection
E1H	WRSEL	0	ADCLK1	ADCLK0	WRSEL	0	Humidity	Resistance	CH1 sensor selection (resistance/humidity)
					0 *5	– *2			Unused
	R/W	R	R/W		ADCLK1	0	OSC3	OSC1	CH1 clock selection
					ADCLK0	0	OSC3	OSC1	CH0 clock selection
E2H	0	0	0	CHSEL	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R			R/W	0 *5	– *2			Unused
					CHSEL	0	CH1	CH0	Channel 1/0 selection
E3H	TC3	TC2	TC1	TC0	TC3	– *3			Up/down counter data (TC0–TC3)
					TC2	– *3			
	R/W				TC1	– *3			
					TC0	– *3			LSB
E4H	TC7	TC6	TC5	TC4	TC7	– *3			Up/down counter data (TC4–TC7)
					TC6	– *3			
	R/W				TC5	– *3			
					TC4	– *3			
E5H	TC11	TC10	TC9	TC8	TC11	– *3			Up/down counter data (TC8–TC11)
					TC10	– *3			
	R/W				TC9	– *3			
					TC8	– *3			
E6H	TC15	TC14	TC13	TC12	TC15	– *3			MSB
					TC14	– *3			Up/down counter data (TC12–TC15)
	R/W				TC13	– *3			
					TC12	– *3			
E7H	C3	C2	C1	C0	C3	– *3			Up-counter data (C0–C3)
					C2	– *3			
	R/W				C1	– *3			
					C0	– *3			LSB
E8H	C7	C6	C5	C4	C7	– *3			Up-counter data (C4–C7)
					C6	– *3			
	R/W				C5	– *3			
					C4	– *3			
E9H	C11	C10	C9	C8	C11	– *3			Up-counter data (C8–C11)
					C10	– *3			
	R/W				C9	– *3			
					C8	– *3			
EAH	C15	C14	C13	C12	C15	– *3			Up-counter data (C12–C15)
					C14	– *3			
	R/W				C13	– *3			
					C12	– *3			
EBH	C19	C18	C17	C16	C19	– *3			MSB
					C18	– *3			Up-counter data (C16–C19)
	R/W				C17	– *3			
					C16	– *3			
ECH	0	OVF2	OVF1	ADRUN	0 *5	– *2			Unused
					OVF2(R)	0	Yes	No	Up/down counter overflow flag
					OVF2(W)	Reset	Reset	–	Up/down counter overflow flag reset
	R	R/W			OVF1(R)	0	Yes	No	Up-counter overflow flag
					OVF1(W)	Reset	Reset	–	Up-counter overflow flag reset
					ADRUN	0	Start	Stop	A/D conversion Start/Stop

Table 1.1.3(h) I/O memory map (F0H–FEH)

Address *7	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
F0H	0	0	0	EIAD	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R			R/W	0 *5	– *2			Unused
					EIAD	0	Enable	Mask	Interrupt mask register (A/D converter)
F1H	0	0	0	EIK1	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R			R/W	0 *5	– *2			Unused
					EIK1	0	Enable	Mask	Interrupt mask register (K10–K13)
F2H	0	0	0	EIK0	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R			R/W	0 *5	– *2			Unused
					EIK0	0	Enable	Mask	Interrupt mask register (K00–K03)
F3H	0	0	0	EISIF	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R			R/W	0 *5	– *2			Unused
					EISIF	0	Enable	Mask	Interrupt mask register (Serial interface)
F4H	0	0	0	EIPT	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R			R/W	0 *5	– *2			Unused
					EIPT	0	Enable	Mask	Interrupt mask register (Programmable timer)
F5H	EIRUN	EILAP	EISW1	EISW0	EIRUN	0	Enable	Mask	Interrupt mask register (Stopwatch direct RUN)
					EILAP	0	Enable	Mask	Interrupt mask register (Stopwatch direct LAP)
	R/W				EISW1	0	Enable	Mask	Interrupt mask register (Stopwatch 1 Hz)
					EISW0	0	Enable	Mask	Interrupt mask register (Stopwatch 10 Hz)
F6H	EIT3	EIT2	EIT1	EIT0	EIT3	0	Enable	Mask	Interrupt mask register (Clock timer 2 Hz)
					EIT2	0	Enable	Mask	Interrupt mask register (Clock timer 8 Hz)
	R/W				EIT1	0	Enable	Mask	Interrupt mask register (Clock timer 16 Hz)
					EIT0	0	Enable	Mask	Interrupt mask register (Clock timer 32 Hz)
F8H	0	0	0	IAD	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R				0 *5	– *2			Unused
					IAD *4	0	Yes	No	Interrupt factor flag (A/D converter)
F9H	0	0	0	IK1	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R				0 *5	– *2			Unused
					IK1 *4	0	Yes	No	Interrupt factor flag (K10–K13)
FAH	0	0	0	IK0	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R				0 *5	– *2			Unused
					IK0 *4	0	Yes	No	Interrupt factor flag (K00–K03)
FBH	0	0	0	ISIF	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R				0 *5	– *2			Unused
					ISIF *4	0	Yes	No	Interrupt factor flag (Serial interface)
FCH	0	0	0	IPT	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R				0 *5	– *2			Unused
					IPT *4	0	Yes	No	Interrupt factor flag (Programmable timer)
FDH	IRUN	ILAP	ISW1	ISW0	IRUN *4	0	Yes	No	Interrupt factor flag (Stopwatch direct RUN)
					ILAP *4	0	Yes	No	Interrupt factor flag (Stopwatch direct LAP)
	R				ISW1 *4	0	Yes	No	Interrupt factor flag (Stopwatch 1 Hz)
					ISW0 *4	0	Yes	No	Interrupt factor flag (Stopwatch 10 Hz)
FEH	IT3	IT2	IT1	IT0	IT3 *4	0	Yes	No	Interrupt factor flag (Clock timer 2 Hz)
					IT2 *4	0	Yes	No	Interrupt factor flag (Clock timer 8 Hz)
	R				IT1 *4	0	Yes	No	Interrupt factor flag (Clock timer 16 Hz)
					IT0 *4	0	Yes	No	Interrupt factor flag (Clock timer 32 Hz)

1.2 Initialize Program Example

The following shows a program example and the flow chart (Figure 1.2.1) for initialization after an initial reset.

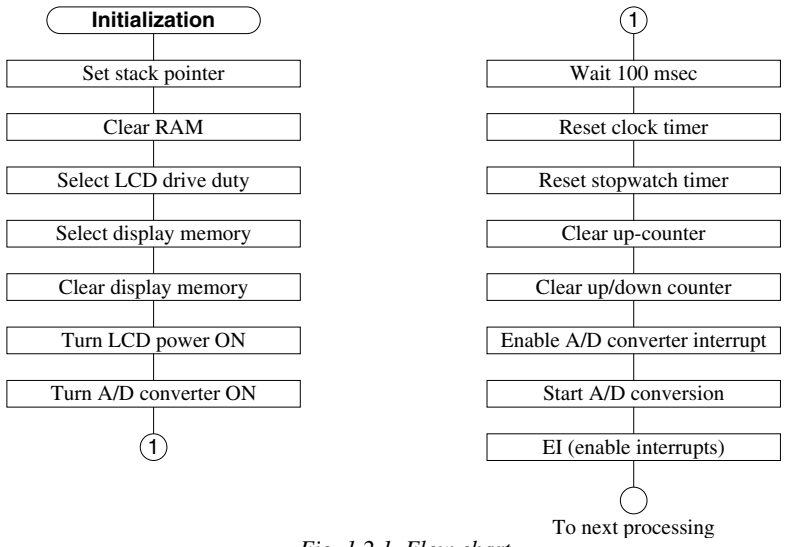


Fig. 1.2.1 Flow chart

Program example

Label	Mnemonic/operand		Comment

```
;
INIT:   LD      A,0             ;Sets page 0 with X and Y registers
        LD      XP,A
        LD      YP,A
;
        LD      A,08H           ;Sets stack pointer
        LD      SPH,A
        LD      A,0
        LD      SPL,A
;
        LD      X,00H           ;Clears RAM page 0, 00H-7FH
CLRAM0: LBPX    MX,0
        CP      XH,8
        JP      NZ,CLRAM0
;
        LD      A,1
        LD      XP,A
;
        LD      X,00H           ;Clears RAM page 1, 00H-2FH
CLRAM1: LBPX    MX,0
        CP      XH,3
        JP      NZ,CLRAM1
;
        LD      A,2
        LD      XP,A
;
        LD      X,00H           ;Clears RAM page 2, 00H-7FH
CLRAM2: LBPX    MX,0
        CP      XH,8
        JP      NZ,CLRAM2
;
        LD      A,3
        LD      XP,A
;
        LD      X,00H           ;Clears RAM page 3, 00H-7FH
CLRAM3: LBPX    MX,0
        CP      XH,8
        JP      NZ,CLRAM3
;
        LD      A,4
```

```
        LD      XP,A
;
        LD      X,00H           ;Clears RAM page 4, 00H-7FH
CLRAM4: LBPX    MX,0
        CP      XH,8
        JP      NZ,CLRAM4
;
        LD      A,0
        LD      XP,A
;
        LD      X,0C2H          ;Sets LCD duty to 1/4
        LD      MX,1010B        ;Sets LCD display memory in page 1
;
        LD      A,1
        LD      XP,A
;
        LD      X,30H           ;Turns all LCD dots OFF
CLLCD:  LBPX    MX,0
        CP      XH,8
        JP      NZ,CLLCD
;
        LD      A,0
        LD      XP,A
;
        LD      X,0C3H          ;Turns LCD power ON
        OR      MX,0010B
;
        LD      X,0E0H          ;Turns A/D converter ON
        OR      MX,0100B
;
        LD      X,0D1H          ;Waits 100 mS
        LD      MX,0001B
        OR      MX,0010B
;
WAIT100:LD      X,0FDH          ;Have 100 mS passed ?
        FAN     MX,0010B
        JP      Z,WAIT100       ;NO
;
        LD      A,MX
;
        LD      X,0C4H          ;Resets clock timer
        LD      MX,0001B
;
        LD      X,0D1H          ;Resets stopwatch timer
        LD      MX,0001B
;
        LD      X,0E3H          ;Sets up-counter to 0
        LBPX    MX,00H          ;Sets up/down counter to 0
        LBPX    MX,00H
        LBPX    MX,00H
        LBPX    MX,00H
        LD      MX,0
;
;
        LD      X,0E7H          ;Sets up-counter to 10000D
        LBPX    MX,0F0H
        LBPX    MX,0D8H
        LD      MX,0
;
        LD      X,0F4H          ;Enables A/D interrupt
        OR      MX,0001B
;
        LD      X,0E0H          ;Turns A/D converter to RUN status
        OR      MX,0001B
;
        EI
;
```

The above program is a basic initialization program for the E0C6256. When using this program, add setting items necessary for each specific application.

CHAPTER 2 OSCILLATION CIRCUITS

2.1 Control Registers for Oscillation Circuit

Table 2.1.1 shows the control registers for the oscillation circuit.

Table 2.1.1 I/O memory map (oscillation circuit)

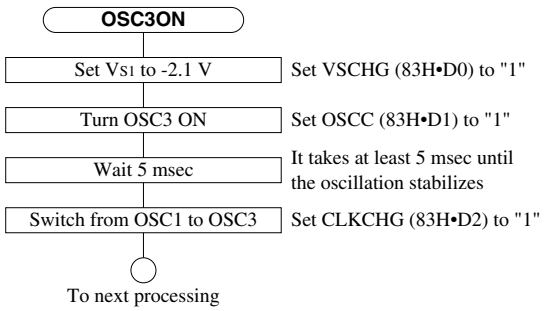
Address *7	Register								Comment
	D3	D2	D1	D0	Name	Init *1	1	0	
83H	0	CLKCHG	OSCC	VSCHG	0 *5	– *2			Unused
					CLKCHG	0	OSC3	OSC1	CPU clock selection
	R	R/W			OSCC	0	On	Off	OSC3 oscillation On/Off
					VSCHG	0	-2.1V	-1.05V	VS1 output voltage change

*1 Initial value at the time of initial reset
*2 Not set in the circuit
*3 Undefined
*4 Reset (0) immediately after being read
*5 Constantly "0" when being read
*6 Refer to main manual
*7 Page switching in I/O memory is not necessary

2.2 Program Example

The CPU system clock should be switched by software between OSC1 and OSC3 depending on which one is used. The following shows a program example and the flow chart (Figure 2.2.1) for the switching.

• Switching from OSC1 to OSC3



• Switching from OSC3 to OSC1

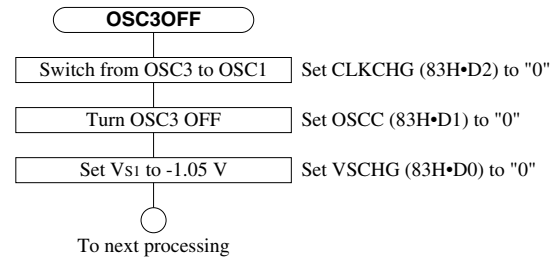


Fig. 2.2.1 Flow chart

Note: Switching the operating voltage when the supply voltage is lower than 2.2 V (absolute value) may cause a malfunction. Switch the operating voltage only after making sure that supply voltage is more than 2.2 V (absolute value) using the SVD circuit.
Furthermore, do not switch the operating voltage during operating in the doubler mode or the halver mode. The OSC3 clock can be used only in the normal mode.

Program example

• Switching from OSC1 to OSC3

```
Label     Mnemonic/operand          Comment
;
OSC3ON:
          LD      X,80H             ;SVD check
          LD      MX,0
;
          LD      X,81H
          OR      MX,0001B
;
          NOP5                      ;100 µS delay
;
          AND     MX,1110B
;
          FAN     MX,0010B
```

```
        JP      NZ,OSC3ONE
;
        LD      X,83H           ;Sets VSCHG to 1
        OR      MX,0001B
;
        OR      MX,0010B        ;Sets OSCC  to 1
;
        CALL    DLY5MS          ;Waits 5 mS
;
        LD      X,83H           ;Sets CLKCHG to 1
        OR      MX,0100B
;
OSC3ONE:RET
;
DLY5MS: .                       ;5 mS delay subroutine
        .
        .
        RET
;
```

• Switching from OSC3 to OSC1

Label	Mnemonic/operand	Comment

```
;
OSC3OFF:
        LD      X,80H           ;SVD check
        LD      MX,0
;
        LD      X,81H
        OR      MX,0001B
;
        CALL    DLY100U         ;100 µS delay
;
        AND     MX,1110B
;
        FAN     MX,0010B
        JP      NZ,OSC3OFE
;
        LD      X,83H           ;Sets CLKCHG to 0
        AND     MX,1011B
;
        LD      X,83H           ;Sets OSCC to 0
        AND     MX,1101B
;
        LD      X,83H           ;Sets VSCHG to 0
        AND     MX,1110B
;
OSC3OFE:RET
;
;
DLY100U:.                       ;100 µS delay subroutine
        .
        .
        RET
;
```

CHAPTER 3 A/D CONVERTER

3.1 Control Registers for A/D Converter

Tables 3.1.1(a) and (b) show the control registers for the A/D converter.

Table 3.1.1(a) I/O memory map (A/D converter)

Address *7	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
E0H	0	APWR	SENSEL	ADMODE	0 *5	– *2			Unused
					APWR	0	On	Off	A/D converter power supply On/Off
	R	R/W			SENSEL	0	Sensor	Reference	Sensor/reference resistance selection
					ADMODE	0	Continuous	Normal	A/D converter operation mode selection
E1H	WRSEL	0	ADCLK1	ADCLK0	WRSEL	0	Humidity	Resistance	CH1 sensor selection (resistance/humidity)
					0 *5	– *2			Unused
	R/W	R	R/W		ADCLK1	0	OSC3	OSC1	CH1 clock selection
					ADCLK0	0	OSC3	OSC1	CH0 clock selection
E2H	0	0	0	CHSEL	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R			R/W	0 *5	– *2			Unused
					CHSEL	0	CH1	CH0	Channel 1/0 selection
E3H	TC3	TC2	TC1	TC0	TC3	– *3			Up/down counter data (TC0–TC3)
					TC2	– *3			
	R/W				TC1	– *3			
					TC0	– *3			LSB
E4H	TC7	TC6	TC5	TC4	TC7	– *3			Up/down counter data (TC4–TC7)
					TC6	– *3			
	R/W				TC5	– *3			
					TC4	– *3			
E5H	TC11	TC10	TC9	TC8	TC11	– *3			Up/down counter data (TC8–TC11)
					TC10	– *3			
	R/W				TC9	– *3			
					TC8	– *3			
E6H	TC15	TC14	TC13	TC12	TC15	– *3			MSB
					TC14	– *3			Up/down counter data (TC12–TC15)
	R/W				TC13	– *3			
					TC12	– *3			
E7H	C3	C2	C1	C0	C3	– *3			Up-counter data (C0–C3)
					C2	– *3			
	R/W				C1	– *3			
					C0	– *3			LSB
E8H	C7	C6	C5	C4	C7	– *3			Up-counter data (C4–C7)
					C6	– *3			
	R/W				C5	– *3			
					C4	– *3			
E9H	C11	C10	C9	C8	C11	– *3			Up-counter data (C8–C11)
					C10	– *3			
	R/W				C9	– *3			
					C8	– *3			
EAH	C15	C14	C13	C12	C15	– *3			Up-counter data (C12–C15)
					C14	– *3			
	R/W				C13	– *3			
					C12	– *3			
EBH	C19	C18	C17	C16	C19	– *3			MSB
					C18	– *3			Up-counter data (C16–C19)
	R/W				C17	– *3			
					C16	– *3			
ECH	0	OVF2	OVF1	ADRUN	0 *5	– *2			Unused
					OVF2(R)	0	Yes	No	Up/down counter overflow flag
					OVF2(W)	Reset	Reset	–	Up/down counter overflow flag reset
	R	R/W			OVF1(R)	0	Yes	No	Up-counter overflow flag
					OVF1(W)	Reset	Reset	–	Up-counter overflow flag reset
					ADRUN	0	Start	Stop	A/D conversion Start/Stop

Table 3.1.1(b) I/O memory map (A/D converter)

Address *7	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
F0H	0	0	0	EIAD	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R			R/W	0 *5	– *2			Unused
					EIAD	0	Enable	Mask	Interrupt mask register (A/D converter)
F8H	0	0	0	IAD	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R				0 *5	– *2			Unused
					IAD *4	0	Yes	No	Interrupt factor flag (A/D converter)

*1 Initial value at the time of initial reset
*2 Not set in the circuit
*3 Undefined
*4 Reset (0) immediately after being read
*5 Constantly "0" when being read
*6 Refer to main manual
*7 Page switching in I/O memory is not necessary

3.2 Control of A/D Converter

The E0C6256 has CR oscillation type A/D converter.
Two systems (channel 0 and channel 1) of CR oscillation circuit are built into this A/D converter, so it is possible to compose two types of A/D conversion circuit by connecting different sensors to each CR oscillation circuit.

The A/D converter incorporates two types of counters. One is the 16-bit up/down counter TC0–TC15 that counts the internal clock for reference counting, and the other is 20-bit up-counter C0–C19 that counts the external resistance oscillation clock. Each counter permits reading and writing on a 4-bit basis.

Figure 3.2.1 shows the control and operation flow of the A/D converter, and Figure 3.2.2 shows the timing chart of the operation.

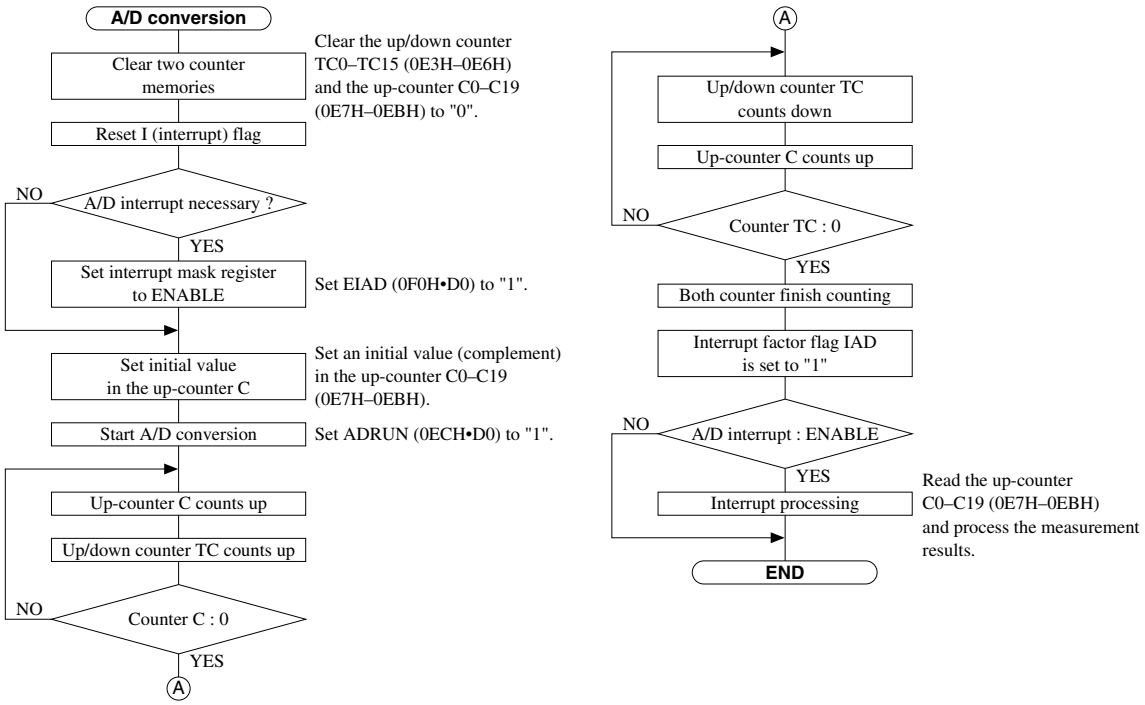


Fig. 3.2.1 Flow chart for controlling A/D converter

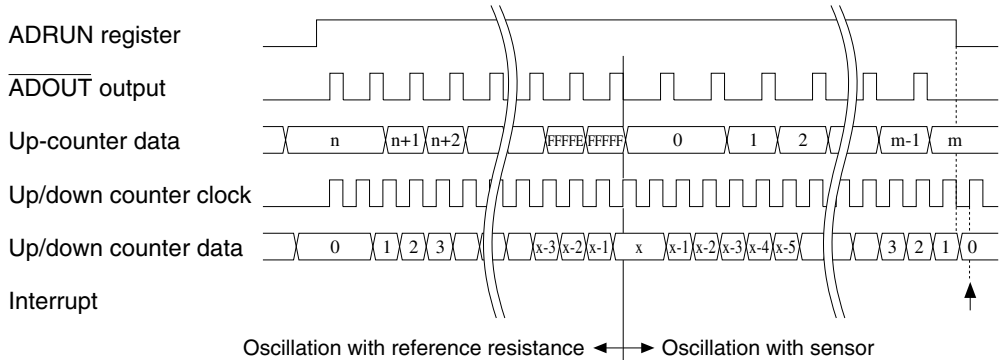


Fig. 3.2.2 Timing chart of A/D converter operation

Basic control and operation of the A/D converter are described in the flowchart in Figure 3.2.2. In order to prepare a program, add items required according to application.

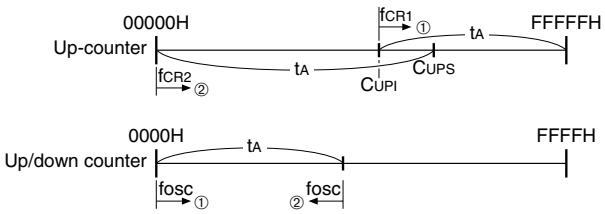
After A/D conversion, the value counted during oscillation of the sensor is set on the up-counter C0–C9. This value is the sensor oscillation clock number during a time period equal to that during which the reference resistance is oscillated according to the initial value set on the up-counter. The difference between the reference resistance and the sensor resistance value can be obtained indirectly from the initial value and results.
Correct it according to the characteristics of the connected elements and calculate the target measurement results.

Note: When the up/down counter TC0–TC15 is read after A/D conversion, it may not indicate "0000H". This is not due to incorrect timing in terminating A/D conversion but because the counting down clock is input after the control signal is output to the up-counter to terminate counting.

Since interruption is possible after A/D conversion, reading of the up-counter and data processing are basically performed using the interrupt function.
If interrupt is not used, A/D converter operation can be checked by reading the ADRUN register. After "1" is written to this register to start A/D conversion, the register remains at "1" during A/D conversion and is reset to "0" when the A/D conversion is finished.

3.3 Software Specification

When programming for A/D conversion, be sure to set the initial value of the up-counter after due consideration.
Figure 3.3.1 shows the relationship between the up-counter and the up/down counter.



fosc: Internal clock frequency
f_{CR1}: CR oscillation frequency on reference side
f_{CR2}: Oscillation frequency on sensor side
C_{UPI}: Count value of CR oscillation on reference side (complement)
C_{UPS}: Count value of oscillation on sensor side
FFFFFH: Max. up-counter value
FFFFH: Max. up/down counter value
t_A: Count time

Fig. 3.3.1 Relationship between up-counter and up/down counter

The following conditions should be satisfied during counting-up (①) and counting-down (②):

Condition (A): The up/down counter should not overflow during counting-up at ①.
Condition (B): The up-counter should not overflow during counting-down at ②.

If the above conditions are not satisfied, A/D conversion is terminated at that point and the correct result cannot be obtained.

When programming, a proper initial value should be set to the up-counter according to these conditions.

3.4 Program Example for Controlling A/D Converter

This section explains a temperature measurement program for a usage example of the A/D converter.
The temperature measurement is performed using a thermistor. After comparing the oscillation frequencies of the thermistor and the reference resistance, the difference is corrected by linear approximation method and the temperature is found.
The following shows the linear approximation equation to derive the temperature.

Temperature (°C) = (① Up-counter value after A/D conversion
- ② Count value for minimum temperature within the range)
×③ Linear approximation coefficient
+④ Minimum temperature within the range

<① Up-counter value after A/D conversion>

This is the value counted in the up-counter when an A/D conversion is completed.

<② Count value for minimum temperature within the range> and <④ Minimum temperature within the range>

To derive the temperature by the linear approximation, the temperature range must be determined for the linear approximation. For example, in case of the range of entire measured temperature is -30 to 70°C and the temperature range is set for every 10°C, the temperature ranges are -30 to -20°C, -20 to -10°C · · · and 60 to 70°C. The smallest value of each temperature range segment is the minimum temperature within the range (④).
The count value for minimum temperature within range (②) is expressed by the following equation:

$$\text{A/D converter count value} = \frac{f_{CR2}}{f_{CR1}} \times \text{up-counter initial value}$$

$$= \frac{\frac{K}{CR2}}{\frac{K}{CR1}} \times \text{up-counter initial value}$$

$$= \frac{R1}{R2} \times \text{up-counter initial value}$$

f_{CR1}: Reference oscillation frequency
f_{CR2}: Sensor oscillation frequency
K: Oscillation coefficient
C: Capacitance
R1: Reference resistance value
R2: Resistance value of thermistor
Up-counter initial value:
Value of which the CR oscillation by the reference resistance has been counted.

By substituting R2 (resistance value of thermistor at minimum temperature within the range), R2 (reference resistance value), and the up-counter initial value into the equation, the count value for the minimum temperature within the range is obtained.

<③ Linear approximation coefficient>

The linear approximation coefficient is the value that shows how many degrees (centigrade) there are for one count in the temperature range.
The linear approximation coefficient is expressed by the following equation:

$$\text{Linear approximation coefficient} = \frac{\text{Absolute value of the temperature range}}{\text{Count value for maximum temperature within the range} - \text{Count value for minimum temperature within the range}}$$

As you can see, the temperature range is smaller, the precision is higher.

* However, in the high temperature part, the ON-resistance of the IC's transistor affects the measurement results because the sensor resistance decreases and chances of error increase. Therefore, correct it using software if necessary.

These values used in the program example are shown in Table 3.4.1.
In the example, 10 kΩ of the external reference resistance and 22,000 pF of capacitor are used, and the initial value of the up-counter is set to 10,000.

Table 3.4.1 Temperature characteristics of thermistor used in example

Temperature (°C)	Thermistor resistance (kΩ)	Linear approximation coefficiant in the measurement temperature range	Up-counter count value (DEC)
-30	111.3		898
-20	67.74	0.0173	1476
-10	42.45	0.0114	2355
0	27.28	0.00763	3665
10	17.96	0.00526	5567
20	12.09	0.00370	8271
30	8.313	0.00266	12029
40	5.828	0.00195	17158
50	4.161	0.00145	24032
60	3.021	0.00110	33101
70	2.229	0.000850	44863

The following shows a program example that is created using the values from the above table, and the flow chart (Figure 3.4.1).

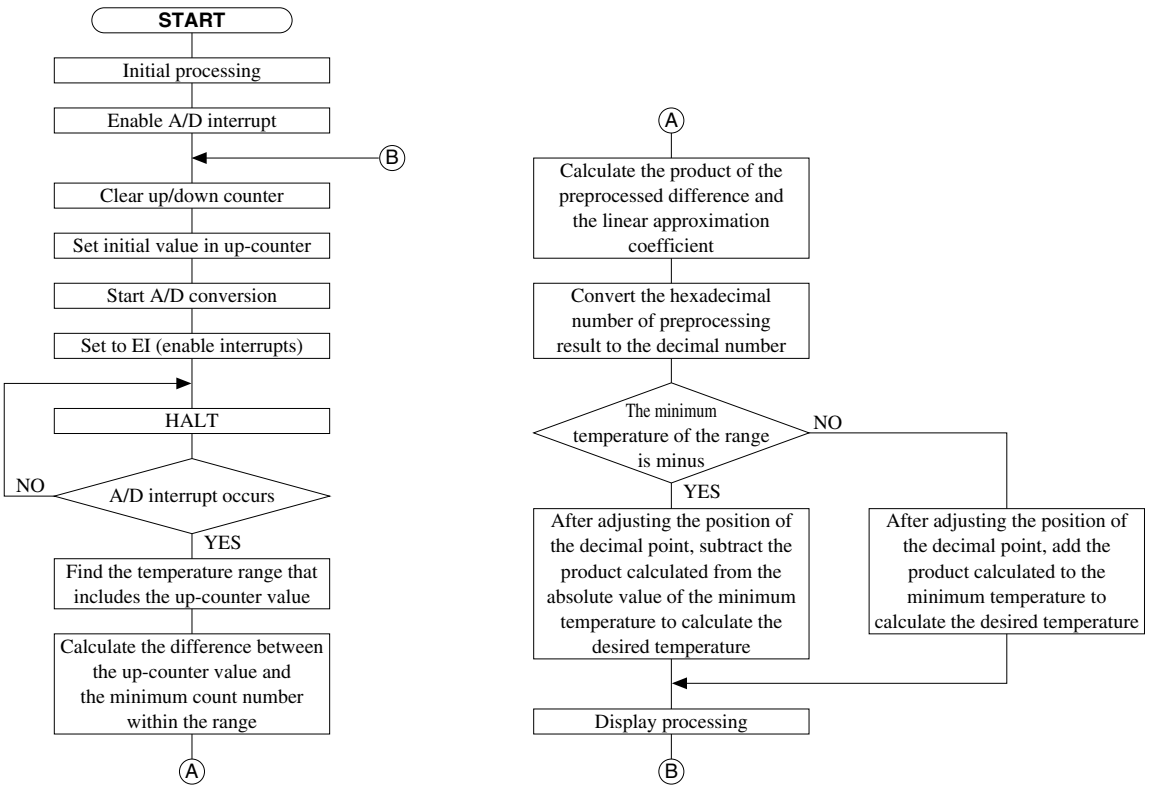


Fig. 3.4.1 Flow chart

Program example

```
Label     Mnemonic/operand          Comment
;*************************************************************************
;*      E0C6256  TEMPERATURE MEASUREMENT SOFTWARE                        *
;*************************************************************************
;
HEXDEC: MACRO   ARG1,ARG2,ARG3
        LOCAL   HXDC1,HXDC2
;
;************************************************************************
;*         HEC-->DEC            1--13DIGIT                              *
;*                                                                      *
;************************************************************************
;
        RST     F,8             ;Resets D, Z, C flags
        LD      A,ARG3
        ADD     A,1             ;Digit ← Digit + 1
;
;    ***** ARG2 ZERO CLEAR *****
;    ***** ARG2 DATA <--ARG1 TOP DATA *****
;
        LD      X,ARG1+ARG3-1
        LD      Y,ARG2
        LD      MY,MX           ;ARG2 data ← ARG1 data
        CP      MY,0AH
        JP      C,$+5           ;Jump if ARG2 data < 0AH
        ADD     MY,6            ;ARG2 data ← ARG2 data + 6
        INC     Y               ;Increments ARG2 address (+1)
        LDPY    MY,1            ;Increments ARG2 data (+1)
        JP      $+3
        INC     Y
        LDPY    MY,0            ;Zero clear
        ADD     A,0FH           ;Decrements digit counter (-1)
        JP      NZ,$-2          ;Jump if digit   0
        LD      B,ARG3-1        ;B register ← Digit - 1
        CP      B,0
        JP      Z,HXDC2         ;Jump if digit = 1
HXDC1:  PUSH    B
;
;   *****  ARG2 DATA <-- ARG2 DATA * 16D  *****
;
        LD      B,4             ;Loop counter setting
        LD      Y,ARG2
        LD      A,ARG3+2        ;A register ← Digit + 2
        RCF                     ;Resets C flag
        SDF                     ;Resets D flag
        ACPY    MY,MY           ;ARG2 data ← 2 * ARG2 data
        PUSH    F
        ADD     A,9             ;Decrements A register (-1)
        JP      Z,$+3           ;Jump if A register   0
        POP     F
        JP      $-5
        POP     F
        ADD     B,9             ;Decrements loop counter (-1)
        JP      NZ,$-12         ;Jump if loop counter   0
;
;   ******  ARG DATA <-- ARG DATA + ARG1 1 DIGIT DATA  *****
;
        RST     F,8             ;Resets D, Z, C flags
        ADC     XL,0FH
        ADC     XH,0FH          ;Decrements ARG1 address (-1)
        LD      Y,ARG2
        LD      B,ARG3+1        ;Digit counter setting
```

```
        CP      MX,0AH
        JP      C,$+7           ;Jump if ARG1 data (1 digit) < 0AH
        ADD     MX,6            ;ARG1 data (1 digit) + 6
        SDF                     ;Sets D flag
        RCF                     ;Resets C flag
        ACPY    MY,MX
        ADC     MY,1            ;ARG2 data ← ARG1 data (1 digit)
        JP      $+5
        RCF                     ;Resets C flag
        SDF                     ;Sets D flag
        ACPY    MY,MX           ;ARG2 data ← ARG1 data (1 digit)
        ADC     MY,0            ;Increments if carry is generated (+1)
        INC     Y
        PUSH    F
        ADD     B,9             ;Decrements digit counter (-1)
        JP      Z,$+3           ;Jump if digit counter   0
        POP     F
        JP      $-6
        POP     F
;
;  *****  DIGIT DECREMENT *****
;
        POP     B
        ADD     B,9             ;Decrements digit number (-1)
        JP      NZ,HXDC1        ;Jump if digit counter   0
HXDC2   RDF                     ;Resets D flag
;
        ENDM

;
;
;
        PAGE    1
;
        ORG     100H
;
        JP      INIT            ;Starts program
;
        JP      INT             ;Interrupt vectors
        JP      INT
        JP      INT
        JP      INT
        JP      INT
        JP      INT
        JP      INT
        JP      INT
        JP      INT
        JP      INT
        JP      INT
        JP      INT
        JP      INT
        JP      INT
        JP      INT
        JP      INT
;
INIT:   LD      A,0             ;Sets page 0 with X and Y registers
        LD      XP,A
        LD      YP,A
;
        LD      A,08H           ;Sets stack pointer
        LD      SPH,A
        LD      A,0
        LD      SPL,A
;
        LD      X,0C2H          ;Sets LCD duty to 1/4
```

```
        LD      MX,1010B        ;Sets LCD display memory in page 1
;
        LD      X,0C3H          ;Turns LCD power ON
        OR      MX,0010B
;
        LD      X,0E0H          ;Turns A/D converter ON
        OR      MX,0100B
;
        LD      X,0             ;Clears RAM page 0, 00H-7FH
CLRAM:  LBPX    MX,0
        CP      XH,8
        JP      NZ,CLRAM
;
        LD      X,0D1H          ;Waits 100 mS
        LD      MX,0001B
        OR      MX,0010B
;
WAIT100:LD      X,0FDH          ;Have 100 mS passed ?
        FAN     MX,0010B
        JP      Z,WAIT100       ;NO
;
        LD      A,MX
;
        LD      A,1
        LD      XP,A
;
        LD      X,30H           ;Turns all LCD dots OFF
CLLCD:  LBPX    MX,0
        CP      XH,8
        JP      NZ,CLLCD
;
        LD      A,0
        LD      XP,A
;
        LD      X,0C4H          ;Resets clock timer
        LD      MX,0001B
;
        LD      X,0D1H          ;Resets stopwatch timer
        LD      MX,0001B
;
        LD      X,0F0H          ;Enables A/D interrupt
        OR      MX,0001B
;
MAIN:
        LD      X,0E3H          ;Sets up-counter to 0
        LBPX    MX,00H          ;Sets up/down counter to 0
        LBPX    MX,00H
        LBPX    MX,00H
        LBPX    MX,00H
        LD      MX,0
;
;
;
        LD      X,0E7H          ;Sets up-counter to 10000D
        LBPX    MX,0F0H
        LBPX    MX,0D8H
        LD      MX,0FH
;
        LD      X,0ECH          ;Turns A/D converter to RUN status
        OR      MX,0001B
;
        EI
        HALT
        JP      MAIN
```

```
;
INT:
        LD      X,0F8H
        LD      A,MX
        FAN     A,0001B
        JP      Z,AD3
        CALL    SETTEMP
AD3:
        RET
;
        PAGE    2
;
SETTEMP:
        RST     F,8
        LD      A,0
        LD      B,0
READKN:
        CALL    $+3
        JP      READEND
        RET
        LD      X,10H
        PSET    3
        JPBA
READEND:
        PUSH    B
        LD      B,5
        LD      X,0EBH
        LD      Y,14H
COMP:
        CP      MX,MY
        JP      C,MULTI
        JP      Z,$+2
        JP      NC,NEXTRD
        RCF
        ADC     XL,15
        RCF
        ADC     YL,15
        ADD     B,15
        JP      NZ,COMP
;       POP     B
        JP      MULTI
;
NEXTRD:
        POP     B
        ADD     A,7             ;Sets address of following setting value
        ADC     B,0
        JP      READKN
;
MULTI:
        POP     B
        RCF
        SBC     A,7
        SBC     B,0
        CALL    $+2
        JP      $+4
        LD      X,10H
        PSET    3
        JPBA
        LD      X,0E7H
        LD      Y,40H
        LD      B,5
        LDPX    MY,MX
        INC     Y
        ADD     B,15
```

```
        JP      NZ,$-3
;
        RCF
        LD      X,10H
        LD      Y,40H
        SCPY    MY,MX
        INC     X
        SCPY    MY,MX
        INC     X
        SCPY    MY,MX
        INC     X
        SCPY    MY,MX
        INC     X
        SCPY    MY,MX
;
;
;  ************  INITIALIZE WORK MEMORY  ************
;
        LD      X,25H
        LD      B,5
WMCLR:
        LBPX    MX,00
        ADD     B,15
        JP      NZ,WMCLR
;
;  ************  CALCULATE An X K  ***************
;
        LD      X,40H
        LD      Y,0AH
        LD      B,5
        LDPX    MY,MX
        INC     Y
        ADD     B,15
        JP      NZ,$-3
        LD      MY,0
        LD      B,1
MULTI00:
        LD      Y,15H
MULTI01:
        FAN     MY,B
        LD      X,40H
        PUSH    YL
        JP      Z,MULTI02
        LD      X,0AH
        LD      A,2
        LD      YH,A
        CALL    SUBADD
        LD      A,1
        LD      YH,A
MULTI02:
        POP     YL
        INC     Y
        CP      YL,9
        JP      NZ,MULTI01
        RCF
        RLC     B
        JP      C,SUBTRA
;
;  *************  WORK MEMORY X 2  ************
;
        LD      X,0AH
        RCF
        ACPX    MX,MX
        ACPX    MX,MX
```

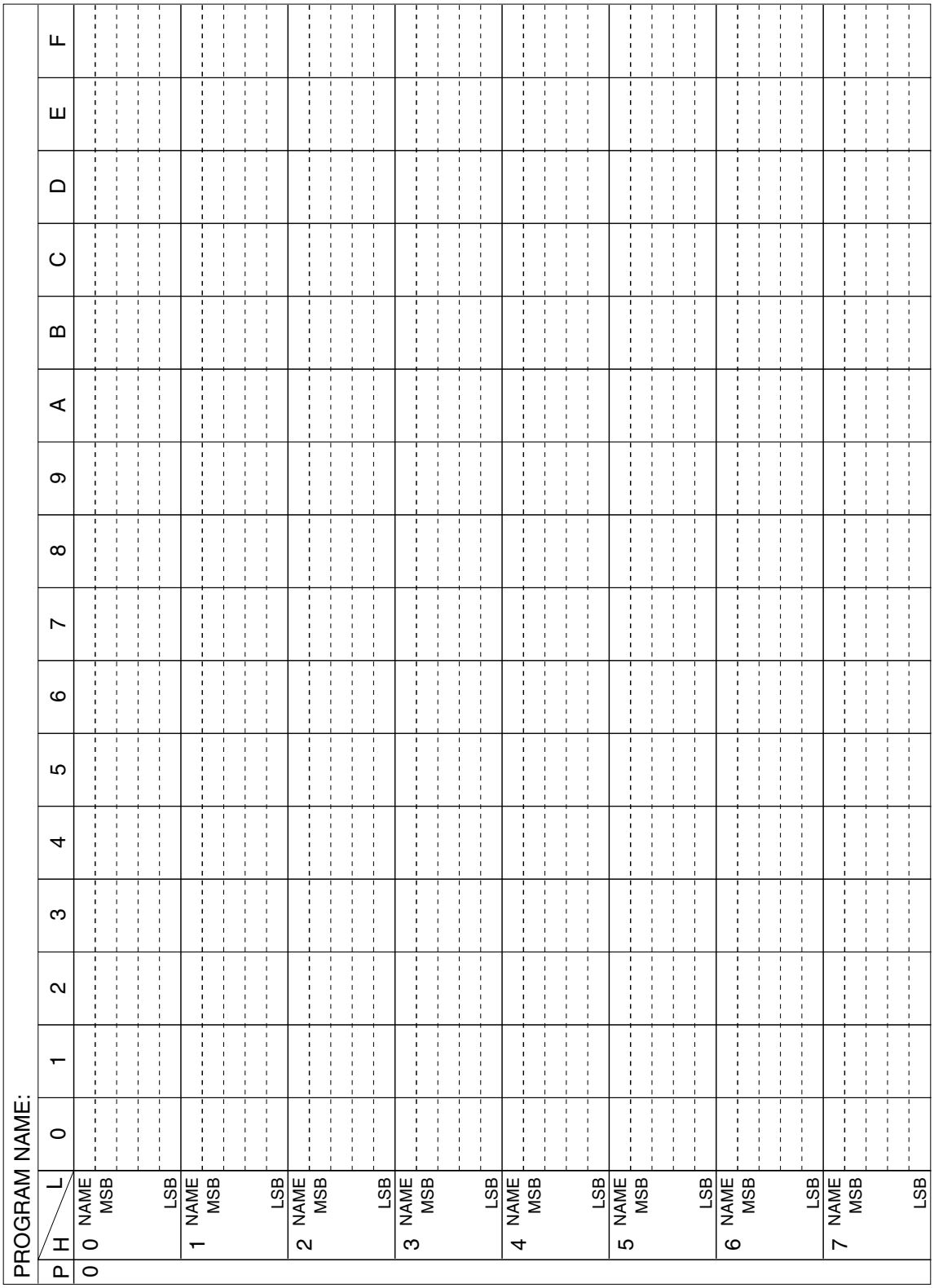
```
        ACPX    MX,MX
        ACPX    MX,MX
        ACPX    MX,MX
        ACPX    MX,MX
        JP      MULTI00
;
;   ************  ADD Bn  *************
;
SUBTRA:
        HEXDEC  25H,30H,11      ;8-digit HEX → DEC
        LD      X,18H           ;Substitutes decimal point position
        LD      A,MX
        SDF
;
        LD      X,1CH
        CP      MX,1
        JP      Z,MINUS
;
PLUS:
        RCF
        LD      X,19H
        LD      Y,30H
PLUS3:
        LD      YL,A
        ACPY    MY,MX
        INC     X
        PUSH    F
        CP      XL,0BH
        JP      Z,$+4
        POP     F
        ADD     A,1             ;OM
        JP      PLUS3
        POP     F
        RDF
        JP      ENDPROG+1
;
MINUS:
        RCF
        LD      X,19H
        LD      Y,30H
MINUS1:
        PUSH    F
        LD      B,YL
        CP      B,A
        JP      Z,MINUS2
        LD      B,0
        POP     F
        SBC     B,MY
        LD      MY,B
        INC     Y
        JP      MINUS1
MINUS2:
        POP     F
        SBC     MX,MY
        LD      MY,MX
        INC     X
        INC     Y
;
        PUSH    F
        CP      XL,0BH
        JP      Z,$+2
        JP      MINUS2
        POP     F
        RDF
```

```
        JP      ENDPROG+1
;
;   ***********  16-BIT ADDITION  **********
;
SUBADD:
        RCF
        ACPY    MY,MX
        INC     X
        ACPY    MY,MX
        INC     X
        ACPY    MY,MX
        INC     X
        ACPY    MY,MX
        INC     X
        ACPY    MY,MX
        INC     X
        ACPY    MY,MX
;
ENDPROG:
        RET
        RET
;
        PAGE    3
;
        ORG     300H
;
;-30°C TO -20°C
        LBPX    MX,82H          ;K1 = 382 (898)
        LBPX    MX,03H
        LDPX    MX,0
        LBPX    MX,0ADH         ;A1 = 40AD (0,0173)
        LBPX    MX,40H
        LBPX    MX,30H          ;B1 = 1030 (-30°C)
        RETD    10H
;
;-20°C TO -10°C
        LBPX    MX,0C4H         ;K1 = 5C4 (1476)
        LBPX    MX,05H
        LDPX    MX,0
        LBPX    MX,72H          ;A1 = 4072 (0,0114)
        LBPX    MX,40H
        LBPX    MX,20H          ;B1 = 1020 (-20°C)
        RETD    10H
;
;-10°C TO   0°C
        LBPX    MX,33H          ;K1 = 933 (2355)
        LBPX    MX,09H
        LDPX    MX,0
        LBPX    MX,0FBH         ;A1 = 52FB (0,00763)
        LBPX    MX,52H
        LBPX    MX,10H          ;B1 = 1010 (-10°C)
        RETD    10H
;
;  0°C TO  10°C
        LBPX    MX,51H          ;K1 = E51 (3665)
        LBPX    MX,0EH
        LDPX    MX,0
        LBPX    MX,0EH          ;A1 = 520E (0,00526)
        LBPX    MX,52H
        LBPX    MX,00H          ;B1 = 0000 (0°C)
        RETD    00H
;
; 10°C TO  20°C
        LBPX    MX,0BFH         ;K1 = 15BF (5567)
```

```
        LBPX    MX,15H
        LDPX    MX,0
        LBPX    MX,72H          ;A1 = 5172 (0,00370)
        LBPX    MX,51H
        LBPX    MX,10H          ;B1 = 0010 (10°C)
        RETD    00H
;
; 20°C TO  30°C
        LBPX    MX,4FH          ;K1 = 204F (8271)
        LBPX    MX,20H
        LDPX    MX,0
        LBPX    MX,0AH          ;A1 = 510A (0,00266)
        LBPX    MX,51H
        LBPX    MX,20H          ;B1 = 0020 (20°C)
        RETD    00H
;
; 30°C TO  40°C
        LBPX    MX,0FDH         ;K1 = 2EFD (12029)
        LBPX    MX,2EH
        LDPX    MX,0
        LBPX    MX,0C3H         ;A1 = 50C3 (0,00195)
        LBPX    MX,50H
        LBPX    MX,30H          ;B1 = 0030 (30°C)
        RETD    00H
;
; 40°C TO  50°C
        LBPX    MX,06H          ;K1 = 430 6(17158)
        LBPX    MX,43H
        LDPX    MX,0
        LBPX    MX,91H          ;A1 = 5091 (0,00145)
        LBPX    MX,50H
        LBPX    MX,40H          ;B1 = 0040 (40°C)
        RETD    00H
;
; 50°C TO  60°C
        LBPX    MX,0E0H         ;K1 = 5DE0 (24032)
        LBPX    MX,5DH
        LDPX    MX,0
        LBPX    MX,6EH          ;A1 = 506E (0,00110)
        LBPX    MX,50H
        LBPX    MX,50H          ;B1 = 0050 (50°C)
        RETD    00H
;
; 60°C TO  70°C
        LBPX    MX,4DH          ;K1 = 814D (33101)
        LBPX    MX,81H
        LDPX    MX,0
        LBPX    MX,52H          ;A1 = 6352 (0,000850)
        LBPX    MX,63H
        LBPX    MX,60H          ;B1 = 0060 (60°C)
        RETD    00H
;
; 70°C
        LBPX    MX,3FH          ;K1 = AF3F (44863)
        LBPX    MX,0AFH
        LDPX    MX,0
        RET
;
;
        ORG     34DH
        RETS
;
;
        END
;
```

APPENDIX A. E0C6256 RAM MAP

RAM map - 1 (000H–07FH)



RAM map - 2 (100H–17FH)

PROGRAM NAME:

P	H \ L	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
1	0	NAME MSB															LSB
	1	NAME MSB															LSB
	2	NAME MSB															LSB
	3	NAME MSB															LSB
	4	NAME MSB															LSB
	5	NAME MSB															LSB
	6	NAME MSB															LSB
	7	NAME MSB															LSB

RAM map - 3 (200H–27FH)

PROGRAM NAME:

P	H \ L	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
2	0	NAME															
		MSB															
		LSB															
	1	NAME															
		MSB															
		LSB															
	2	NAME															
		MSB															
		LSB															
	3	NAME															
		MSB															
		LSB															
	4	NAME															
		MSB															
		LSB															
	5	NAME															
		MSB															
		LSB															
	6	NAME															
		MSB															
		LSB															
	7	NAME															
		MSB															
		LSB															

RAM map - 4 (300H–37FH)

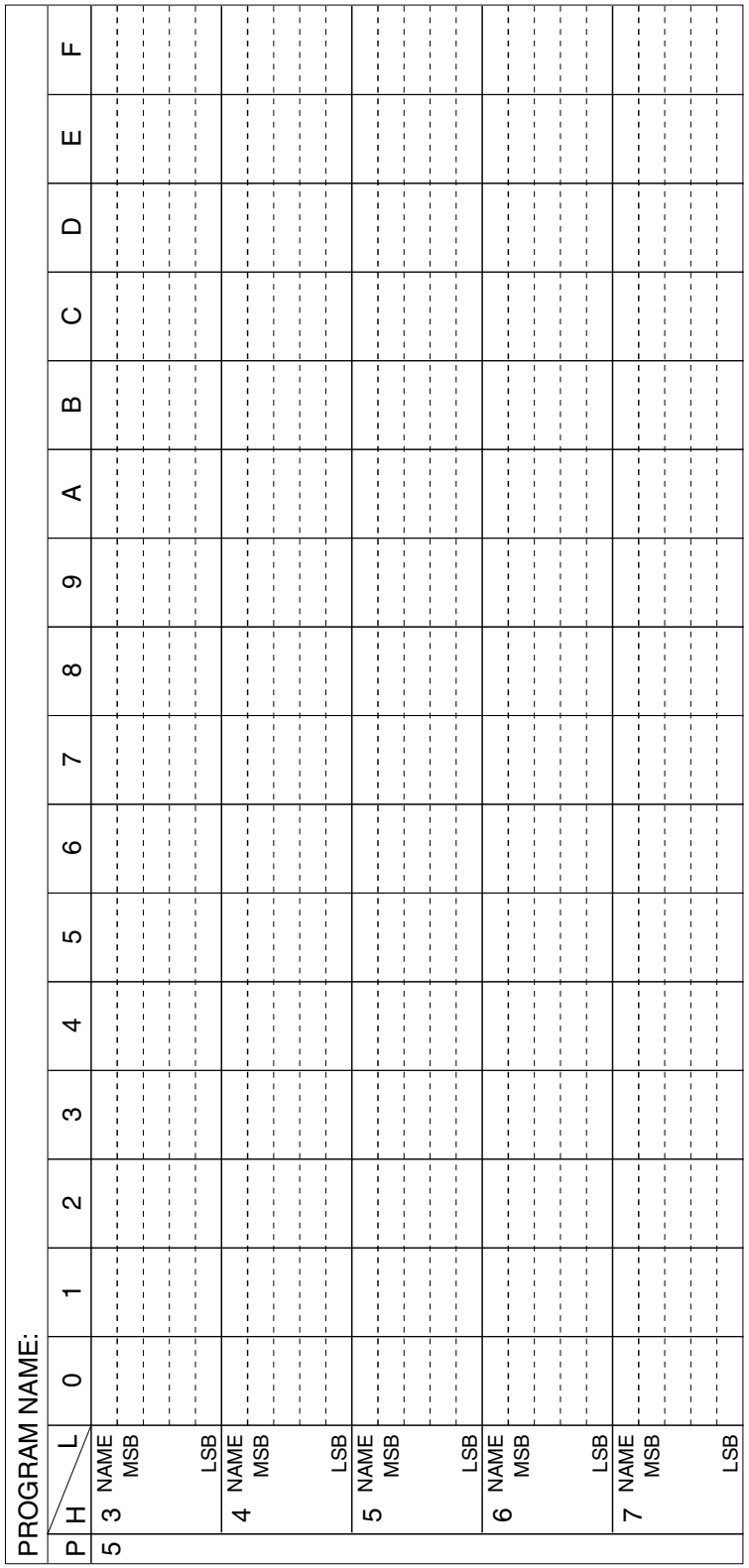
PROGRAM NAME:																
P	H \ L	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
3	0	NAME MSB															LSB
	1	NAME MSB															LSB
	2	NAME MSB															LSB
	3	NAME MSB															LSB
	4	NAME MSB															LSB
	5	NAME MSB															LSB
	6	NAME MSB															LSB
	7	NAME MSB															LSB

RAM map - 5 (400H–47FH)

PROGRAM NAME:

P	H \ L	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
4	0	NAME MSB															
		LSB															
	1	NAME MSB															
		LSB															
	2	NAME MSB															
		LSB															
	3	NAME MSB															
		LSB															
	4	NAME MSB															
		LSB															
	5	NAME MSB															
		LSB															
	6	NAME MSB															
		LSB															
	7	NAME MSB															
		LSB															

Display memory map (530H–57FH, W only)



I/O memory map (80H–FEH)

PROGRAM NAME:

P	H \ L		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	8	NAME																
		MSB	0	0	0	0	0											
1			0	0	VSEL	CLKCHG	VLCHG2											
			SVDS1	SVDDT	HLON	OSCC	VLCHG1											
2		LSB	SVDS0	SVDON	DBON	VSCHG	VLCHG0											
3	9	NAME																
		MSB	SIK03	K03	KCP03		SIK13	K13	KCP13									
4			SIK02	K02	KCP02		SIK12	K12	KCP12									
			SIK01	K01	KCP01		SIK11	K11	KCP11									
5		LSB	SIK00	K00	KCP00		SIK10	K10	KCP10									
	A	NAME																
		MSB	0	R03	0	R13												
			0	R02	0	R12												
			0	R01	0	R11												
		LSB	R0HIZ	R00	R1HIZ	R10												
	B	NAME																
		MSB	IOC03	PUL03	P03		IOC13	PUL13	P13									
			IOC02	PUL02	P02		IOC12	PUL12	P12									
			IOC01	PUL01	P01		IOC11	PUL11	P11									
		LSB	IOC00	PUL00	P00		IOC10	PUL10	P10									
	C	NAME																
		MSB	FOUTE	0	LDMS	0	0	TM3	TM7		0	0	PNRFS	RD3	RD7	PT3	PT7	
			0	0	STCD	0	0	TM2	TM6		0	0	PTOE	RD2	RD6	PT2	PT6	
			FOFQ1	0	LDTY1	LOFF	TMRUN	TM1	TM5		PTPS1	PTPC1	PTRUN	RD1	RD5	PT1	PT5	
		LSB	FOFQ0	WDRST	LDTY0	LPWR	TMRST	TM0	TM4		PTPS0	PTPC0	PTRST	RD0	RD4	PT0	PT4	
	D	NAME																
		MSB	EDIR	LCURF	SWL3	SWM3	SWH3				0	SDP	SD3	SD7	ENRTM	0	0	0
			DKM2	CRNWF	SWL2	SWM2	SWH2				0	SCPS	SD2	SD6	ENRST	BZSTP	BZFQ2	BDTY2
			DKM1	SWRUN	SWL1	SWM1	SWH1				SCTRG	SCS1	SD1	SD5	ENON	BZSHT	BZFQ1	BDTY1
		LSB	DKM0	SWRST	SWL0	SWM0	SWH0				ESIF	SCS0	SD0	SD4	BZE	SHTPW	BZFQ0	BDTY0
	E	NAME																
		MSB	0	WRSEL	0	TC3	TC7	TC11	TC15	C3	C7	C11	C15	C19	0			
			APWR	0	0	TC2	TC6	TC10	TC14	C2	C6	C10	C14	C18	OVF2			
			SENSEL	ADCLK1	0	TC1	TC5	TC9	TC13	C1	C5	C9	C13	C17	OVF1			
		LSB	ADMODE	ADCLK0	CHSEL	TC0	TC4	TC8	TC12	C0	C4	C8	C12	C16	ADRUN			
	F	NAME																
		MSB	0	0	0	0	0	EIRUN	EIT3		0	0	0	0	0	IRUN	IT3	
			0	0	0	0	0	EILAP	EIT2		0	0	0	0	0	ILAP	IT2	
			0	0	0	0	0	EISW1	EIT1		0	0	0	0	0	ISW1	IT1	
		LSB	EIAD	EIK1	EIK0	EISIF	EIPT	EISW0	EIT0		IAD	IK1	IK0	ISIF	IPT	ISW0	IT0	

Unused area

APPENDIX B. E0C6256 INSTRUCTION SET

Classification	Mnemonic	Operand	Operation Code												Flag				Clock	Operation
			B	A	9	8	7	6	5	4	3	2	1	0	I	D	Z	C		
Branch instructions	PSET	p	1	1	1	0	0	1	0	p4	p3	p2	p1	p0					5	NBP ← p4, NPP ← p3~p0
	JP	s	0	0	0	0	s7	s6	s5	s4	s3	s2	s1	s0					5	PCB ← NBP, PCP ← NPP, PCS ← s7~s0
		C, s	0	0	1	0	s7	s6	s5	s4	s3	s2	s1	s0					5	PCB ← NBP, PCP ← NPP, PCS ← s7~s0 if C=1
		NC, s	0	0	1	1	s7	s6	s5	s4	s3	s2	s1	s0					5	PCB ← NBP, PCP ← NPP, PCS ← s7~s0 if C=0
		Z, s	0	1	1	0	s7	s6	s5	s4	s3	s2	s1	s0					5	PCB ← NBP, PCP ← NPP, PCS ← s7~s0 if Z=1
		NZ, s	0	1	1	1	s7	s6	s5	s4	s3	s2	s1	s0					5	PCB ← NBP, PCP ← NPP, PCS ← s7~s0 if Z=0
	JPBA		1	1	1	1	1	1	1	0	1	0	0	0					5	PCB ← NBP, PCP ← NPP, PCSH ← B, PCSL ← A
	CALL	s	0	1	0	0	s7	s6	s5	s4	s3	s2	s1	s0					7	M(SP-1) ← PCP, M(SP-2) ← PCSH, M(SP-3) ← PCSL+1 SP ← SP-3, PCP ← NPP, PCS ← s7~s0
	CALZ	s	0	1	0	1	s7	s6	s5	s4	s3	s2	s1	s0					7	M(SP-1) ← PCP, M(SP-2) ← PCSH, M(SP-3) ← PCSL+1 SP ← SP-3, PCP ← 0, PCS ← s7~s0
	RET		1	1	1	1	1	1	0	1	1	1	1	1					7	PCSL ← M(SP), PCSH ← M(SP+1), PCP ← M(SP+2) SP ← SP+3
	RETS		1	1	1	1	1	1	0	1	1	1	1	0					12	PCSL ← M(SP), PCSH ← M(SP+1), PCP ← M(SP+2) SP ← SP+3, PC ← PC+1
	RETD	*l*	0	0	0	1	*l*7	*l*6	*l*5	*l*4	*l*3	*l*2	*l*1	*l*0					12	PCSL ← M(SP), PCSH ← M(SP+1), PCP ← M(SP+2) SP ← SP+3, M(X) ← *l*3~*l*0, M(X+1) ← *l*7~*l*4, X ← X+2
System control instructions	NOP5		1	1	1	1	1	1	1	1	1	0	1	1					5	No operation (5 clock cycles)
	NOP7		1	1	1	1	1	1	1	1	1	1	1	1					7	No operation (7 clock cycles)
	HALT		1	1	1	1	1	1	1	1	1	0	0	0					5	Halt (stop clock)
Index operation instructions	INC	X	1	1	1	0	1	1	1	0	0	0	0	0					5	X ← X+1
		Y	1	1	1	0	1	1	1	1	0	0	0	0					5	Y ← Y+1
	LD	X, x	1	0	1	1	x7	x6	x5	x4	x3	x2	x1	x0					5	XH ← x7~x4, XL ← x3~x0
		Y, y	1	0	0	0	y7	y6	y5	y4	y3	y2	y1	y0					5	YH ← y7~y4, YL ← y3~y0
		XP, r	1	1	1	0	1	0	0	0	0	0	r1	r0					5	XP ← r
		XH, r	1	1	1	0	1	0	0	0	0	1	r1	r0					5	XH ← r
		XL, r	1	1	1	0	1	0	0	0	1	0	r1	r0					5	XL ← r
		YP, r	1	1	1	0	1	0	0	1	0	0	r1	r0					5	YP ← r
		YH, r	1	1	1	0	1	0	0	1	0	1	r1	r0					5	YH ← r
		YL, r	1	1	1	0	1	0	0	1	1	0	r1	r0					5	YL ← r
		r, XP	1	1	1	0	1	0	1	0	0	0	r1	r0					5	r ← XP
		r, XH	1	1	1	0	1	0	1	0	0	1	r1	r0					5	r ← XH
		r, XL	1	1	1	0	1	0	1	0	1	0	r1	r0					5	r ← XL
		r, YP	1	1	1	0	1	0	1	1	0	0	r1	r0					5	r ← YP
		r, YH	1	1	1	0	1	0	1	1	0	1	r1	r0					5	r ← YH
		r, YL	1	1	1	0	1	0	1	1	1	0	r1	r0					5	r ← YL
	ADC	XH, i	1	0	1	0	0	0	0	0	i3	i2	i1	i0			↕	↕	7	XH ← XH+i3~i0+C
		XL, i	1	0	1	0	0	0	0	1	i3	i2	i1	i0			↕	↕	7	XL ← XL+i3~i0+C
		YH, i	1	0	1	0	0	0	1	0	i3	i2	i1	i0			↕	↕	7	YH ← YH+i3~i0+C
		YL, i	1	0	1	0	0	0	1	1	i3	i2	i1	i0			↕	↕	7	YL ← YL+i3~i0+C

Classification	Mnemonic	Operand	Operation Code												Flag				Clock	Operation
			B	A	9	8	7	6	5	4	3	2	1	0	I	D	Z	C		
Index operation instructions	CP	XH, i	1	0	1	0	0	1	0	0	i3	i2	i1	i0			↕	↕	7	XH-i3~i0
		XL, i	1	0	1	0	0	1	0	1	i3	i2	i1	i0			↕	↕	7	XL-i3~i0
		YH, i	1	0	1	0	0	1	1	0	i3	i2	i1	i0			↕	↕	7	YH-i3~i0
		YL, i	1	0	1	0	0	1	1	1	i3	i2	i1	i0			↕	↕	7	YL-i3~i0
Data transfer instructions	LD	r, i	1	1	1	0	0	0	r1	r0	i3	i2	i1	i0					5	r←i3~i0
		r, q	1	1	1	0	1	1	0	0	r1	r0	q1	q0					5	r←q
		A, Mn	1	1	1	1	1	0	1	0	n3	n2	n1	n0					5	A←M(n3~n0)
		B, Mn	1	1	1	1	1	0	1	1	n3	n2	n1	n0					5	B←M(n3~n0)
		Mn, A	1	1	1	1	1	0	0	0	n3	n2	n1	n0					5	M(n3~n0)←A
		Mn, B	1	1	1	1	1	0	0	1	n3	n2	n1	n0					5	M(n3~n0)←B
	LDPX	MX, i	1	1	1	0	0	1	1	0	i3	i2	i1	i0					5	M(X)←i3~i0, X←X+1
		r, q	1	1	1	0	1	1	1	0	r1	r0	q1	q0					5	r←q, X←X+1
	LDPY	MY, i	1	1	1	0	0	1	1	1	i3	i2	i1	i0					5	M(Y)←i3~i0, Y←Y+1
		r, q	1	1	1	0	1	1	1	1	r1	r0	q1	q0					5	r←q, Y←Y+1
	LBPX	MX, *l*	1	0	0	1	*l*7	*l*6	*l*5	*l*4	*l*3	*l*2	*l*1	*l*0					5	M(X)←*l*3~*l*0, M(X+1)←*l*7~*l*4, X←X+2
Flag operation instructions	SET	F, i	1	1	1	1	0	1	0	0	i3	i2	i1	i0	↑	↑	↑	↑	7	F←F∨i3~i0
	RST	F, i	1	1	1	1	0	1	0	1	i3	i2	i1	i0	↓	↓	↓	↓	7	F←F∧i3~i0
	SCF		1	1	1	1	0	1	0	0	0	0	0	1				↑	7	C←1
	RCF		1	1	1	1	0	1	0	1	1	1	1	0				↓	7	C←0
	SZF		1	1	1	1	0	1	0	0	0	0	1	0			↑		7	Z←1
	RZF		1	1	1	1	0	1	0	1	1	1	0	1			↓		7	Z←0
	SDF		1	1	1	1	0	1	0	0	0	1	0	0		↑			7	D←1 (Decimal Adjuster ON)
	RDF		1	1	1	1	0	1	0	1	1	0	1	1		↓			7	D←0 (Decimal Adjuster OFF)
	EI		1	1	1	1	0	1	0	0	1	0	0	0	↑				7	I ←1 (Enables Interrupt)
	DI		1	1	1	1	0	1	0	1	0	1	1	1	↓				7	I ←0 (Disables Interrupt)
Stack operation instructions	INC	SP	1	1	1	1	1	1	0	1	1	0	1	1					5	SP← SP+1
	DEC	SP	1	1	1	1	1	1	0	0	1	0	1	1					5	SP← SP-1
	PUSH	r	1	1	1	1	1	1	0	0	0	0	r1	r0					5	SP← SP-1, M(SP)←r
		XP	1	1	1	1	1	1	0	0	0	1	0	0					5	SP← SP-1, M(SP)←XP
		XH	1	1	1	1	1	1	0	0	0	1	0	1					5	SP← SP-1, M(SP)←XH
		XL	1	1	1	1	1	1	0	0	0	1	1	0					5	SP← SP-1, M(SP)←XL
		YP	1	1	1	1	1	1	0	0	0	1	1	1					5	SP← SP-1, M(SP)←YP
		YH	1	1	1	1	1	1	0	0	1	0	0	0					5	SP← SP-1, M(SP)←YH
		YL	1	1	1	1	1	1	0	0	1	0	0	1					5	SP← SP-1, M(SP)←YL
		F	1	1	1	1	1	1	0	0	1	0	1	0					5	SP← SP-1, M(SP)←F
	POP	r	1	1	1	1	1	1	0	1	0	0	r1	r0					5	r←M(SP), SP←SP+1
		XP	1	1	1	1	1	1	0	1	0	1	0	0					5	XP←M(SP), SP←SP+1
		XH	1	1	1	1	1	1	0	1	0	1	0	1					5	XH←M(SP), SP←SP+1
		XL	1	1	1	1	1	1	0	1	0	1	1	0					5	XL←M(SP), SP←SP+1
		YP	1	1	1	1	1	1	0	1	0	1	1	1					5	YP←M(SP), SP←SP+1

Classification	Mnemonic	Operand	Operation Code												Flag				Clock	Operation
			B	A	9	8	7	6	5	4	3	2	1	0	I	D	Z	C		
Stack operation instructions	POP	YH	1	1	1	1	1	1	0	1	1	0	0	0					5	YH← M(SP), SP ← SP+1
		YL	1	1	1	1	1	1	0	1	1	0	0	1					5	YL ← M(SP), SP ← SP+1
		F	1	1	1	1	1	1	0	1	1	0	1	0	↕	↕	↕	↕	5	F ← M(SP), SP ← SP+1
	LD	SPH, r	1	1	1	1	1	1	1	0	0	0	r1	r0					5	SPH ← r
		SPL, r	1	1	1	1	1	1	1	1	0	0	r1	r0					5	SPL ← r
		r, SPH	1	1	1	1	1	1	1	0	0	1	r1	r0					5	r ← SPH
		r, SPL	1	1	1	1	1	1	1	1	0	1	r1	r0					5	r ← SPL
Arithmetic instructions	ADD	r, i	1	1	0	0	0	0	r1	r0	i3	i2	i1	i0	★	↕	↕		7	r ← r+i3~i0
		r, q	1	0	1	0	1	0	0	0	r1	r0	q1	q0	★	↕	↕		7	r ← r+q
	ADC	r, i	1	1	0	0	0	1	r1	r0	i3	i2	i1	i0	★	↕	↕		7	r ← r+i3~i0+C
		r, q	1	0	1	0	1	0	0	1	r1	r0	q1	q0	★	↕	↕		7	r ← r+q+C
	SUB	r, q	1	0	1	0	1	0	1	0	r1	r0	q1	q0	★	↕	↕		7	r ← r-q
	SBC	r, i	1	1	0	1	0	1	r1	r0	i3	i2	i1	i0	★	↕	↕		7	r ← r-i3~i0-C
		r, q	1	0	1	0	1	0	1	1	r1	r0	q1	q0	★	↕	↕		7	r ← r-q-C
	AND	r, i	1	1	0	0	1	0	r1	r0	i3	i2	i1	i0		↕			7	r ← r∧i3~i0
		r, q	1	0	1	0	1	1	0	0	r1	r0	q1	q0		↕			7	r ← r∧q
	OR	r, i	1	1	0	0	1	1	r1	r0	i3	i2	i1	i0		↕			7	r ← r∨i3~i0
		r, q	1	0	1	0	1	1	0	1	r1	r0	q1	q0		↕			7	r ← r∨q
	XOR	r, i	1	1	0	1	0	0	r1	r0	i3	i2	i1	i0		↕			7	r ← r∀i3~i0
		r, q	1	0	1	0	1	1	1	0	r1	r0	q1	q0		↕			7	r ← r∀q
	CP	r, i	1	1	0	1	1	1	r1	r0	i3	i2	i1	i0		↕	↕		7	r-i3~i0
		r, q	1	1	1	1	0	0	0	0	r1	r0	q1	q0		↕	↕		7	r-q
	FAN	r, i	1	1	0	1	1	0	r1	r0	i3	i2	i1	i0		↕			7	r∧i3~i0
		r, q	1	1	1	1	0	0	0	1	r1	r0	q1	q0		↕			7	r∧q
	RLC	r	1	0	1	0	1	1	1	1	r1	r0	r1	r0		↕	↕		7	d3 ← d2, d2 ← d1, d1 ← d0, d0 ← C, C ← d3
	RRC	r	1	1	1	0	1	0	0	0	1	1	r1	r0		↕	↕		5	d3 ← C, d2 ← d3, d1 ← d2, d0 ← d1, C ← d0
	INC	Mn	1	1	1	1	0	1	1	0	n3	n2	n1	n0		↕	↕		7	M(n3~n0) ← M(n3~n0)+1
	DEC	Mn	1	1	1	1	0	1	1	1	n3	n2	n1	n0		↕	↕		7	M(n3~n0) ← M(n3~n0)-1
	ACPX	MX, r	1	1	1	1	0	0	1	0	1	0	r1	r0	★	↕	↕		7	M(X) ← M(X)+r+C, X ← X+1
	ACPY	MY, r	1	1	1	1	0	0	1	0	1	1	r1	r0	★	↕	↕		7	M(Y) ← M(Y)+r+C, Y ← Y+1
	SCPX	MX, r	1	1	1	1	0	0	1	1	1	0	r1	r0	★	↕	↕		7	M(X) ← M(X)-r-C, X ← X+1
	SCPY	MY, r	1	1	1	1	0	0	1	1	1	1	r1	r0	★	↕	↕		7	M(Y) ← M(Y)-r-C, Y ← Y+1
	NOT	r	1	1	0	1	0	0	r1	r0	1	1	1	1		↕			7	r ← $\overline{r}$

Abbreviations used in the explanations have the following meanings.

Symbols associated with registers and memory

A A register
B B register
X XHL register
(low order eight bits of index register IX)
Y YHL register
(low order eight bits of index register IY)
XH XH register
(high order four bits of XHL register)
XL XL register
(low order four bits of XHL register)
YH YH register
(high order four bits of YHL register)
YL YL register
(low order four bits of YHL register)
XP XP register
(high order four bits of index register IX)
YP YP register
(high order four bits of index register IY)
SP Stack pointer SP
SPH High-order four bits of stack pointer SP
SPL Low-order four bits of stack pointer SP
MX, M(X) Data memory whose address is specified with index register IX
MY, M(Y) Data memory whose address is specified with index register IY
Mn, M(n) Data memory address 000H–00FH (address specified with immediate data n of 00H–0FH)
M(SP) Data memory whose address is specified with stack pointer SP
r, q Two-bit register code
r, q is two-bit immediate data; according to the contents of these bits, they indicate registers A, B, and MX and MY (data memory whose addresses are specified with index registers IX and IY)

r		q		Register
r1	r0	q1	q0	specified
0	0	0	0	A
0	1	0	1	B
1	0	1	0	MX
1	1	1	1	MY

Symbols associated with program counter

NBP New bank pointer
NPP New page pointer
PCB Program counter bank
PCP Program counter page
PCS Program counter step
PCSH Four high order bits of PCS
PCSL Four low order bits of PCS

Symbols associated with flags

F Flag register (I, D, Z, C)
C Carry flag
Z Zero flag
D Decimal flag
I Interrupt flag
↓ Flag reset
↑ Flag set
↕ Flag set or reset

Associated with immediate data

p Five-bit immediate data or label 00H–1FH
s Eight-bit immediate data or label 00H–0FFH
l Eight-bit immediate data 00H–0FFH
i Four-bit immediate data 00H–0FH

Associated with arithmetic and other operations

+ Add
- Subtract
∧ Logical AND
∨ Logical OR
∀ Exclusive-OR
★ Add-subtract instruction for decimal operation when the D flag is set

APPENDIX C. PSEUDO-INSTRUCTION TABLE OF THE CROSS ASSEMBLER

Item No.	Pseudo-instruction	Meaning	Example of use
1	EQU (Equation)	To allocate data to label	`ABC EQU 9` `BCD EQU ABC+1`
2	ORG (Origin)	To define location counter	`ORG 100H` `ORG 256`
3	SET (Set)	To allocate data to label (data can be changed)	`ABC SET 0001H` `ABC SET 0002H`
4	DW (Define Word)	To define ROM data	`ABC DW 'AB'` `BCD DW 0FFBH`
5	BANK (Bank)	To define boundary of bank	`BANK 0` `BANK 1H`
6	PAGE (Page)	To define boundary of page	`PAGE 1H` `PAGE 4`
7	SECTION (Section)	To define boundary of section	`SECTION`
8	END (End)	To terminate assembly	`END`

9	MACRO
	(Macro)
		To define macro	`CHECK MACRO DATA`
			`LOCAL LOOP`
			`LOOP CP MX,DATA`
			`JP NZ,LOOP`
			`ENDM`
			
			`CHECK 1`

10	LOCAL (Local)	To make local specification of label during macro definition	
11	ENDM (End Macro)	To end macro definition	

APPENDIX D. COMMAND TABLE OF ICE6200

Item No.	Function	Command Format	Outline of Operation
1	Assemble	#A,a ↵	Assemble command mnemonic code and store at address "a"
2	Disassemble	#L,a1,a2 ↵	Contents of addresses a1 to a2 are disassembled and displayed
3	Dump	#DP,a1,a2 ↵	Contents of program area a1 to a2 are displayed
		#DD,a1,a2 ↵	Content of data area a1 to a2 are displayed
4	Fill	#FP,a1,a2,d ↵	Data d is set in addresses a1 to a2 (program area)
		#FD,a1,a2,d ↵	Data d is set in addresses a1 to a2 (data area)
5	Set Run Mode	#G,a ↵	Program is executed from the "a" address
		#TIM ↵	Execution time and step counter selection
		#OTF ↵	On-the-fly display selection
6	Trace	#T,a,n ↵	Executes program while displaying results of step instruction from "a" address
		#U,a,n ↵	Displays only the final step of #T,a,n
7	Break	#BA,a ↵	Sets Break at program address "a"
		#BAR,a ↵	Breakpoint is canceled
		#BD ↵	Break condition is set for data RAM
		#BDR ↵	Breakpoint is canceled
		#BR ↵	Break condition is set for EVA6256 CPU internal registers
		#BRR ↵	Breakpoint is canceled
		#BM ↵	Combined break conditions set for program data RAM address and registers
		#BMR ↵	Cancel combined break conditions for program data ROM address and registers
		#BRES ↵	All break conditions canceled
		#BC ↵	Break condition displayed
		#BE ↵	Enter break enable mode
		#BSYN ↵	Enter break disable mode
		#BT ↵	Set break stop/trace modes
		#BRKSEL,REM ↵	Set BA condition clear/remain modes
8	Move	#MP,a1,a2,a3 ↵	Contents of program area addresses a1 to a2 are moved to addresses a3 and after
		#MD,a1,a2,a3 ↵	Contents of data area addresses a1 to a2 are moved to addresses a3 and after
9	Data Set	#SP,a ↵	Data from program area address "a" are written to memory
		#SD,a ↵	Data from data area address "a" are written to memory
10	Change CPU Internal Registers	#DR ↵	Display EVA6256 CPU internal registers
		#SR ↵	Set EVA6256 CPU internal registers
		#I ↵	Reset EVA6256 CPU
		#DXY ↵	Display X, Y, MX and MY
		#SXY ↵	Set data for X and Y display and MX, MY

Item No.	Function	Command Format	Outline of Operation
11	History	#H,p1,p2 ↵	Display history data for pointer 1 and pointer 2
		#HB ↵	Display upstream history data
		#HG ↵	Display 21 line history data
		#HP ↵	Display history pointer
		#HPS,a ↵	Set history pointer
		#HC,S/C/E ↵	Sets up the history information acquisition before (S), before/after (C) and after (E)
		#HA,a1,a2 ↵	Sets up the history information acquisition from program area a1 to a2
		#HAR,a1,a2 ↵	Sets up the prohibition of the history information acquisition from program area a1 to a2
		#HAD ↵	Indicates history acquisition program area
		#HS,a ↵	Retrieves and indicates the history information which executed a program address "a"
		#HSW,a ↵ #HSR,a ↵	Retrieves and indicates the history information which wrote or read the data area address "a"
12	File	#RF,file ↵	Move program file to memory
		#RFD,file ↵	Move data file to memory
		#VF,file ↵	Compare program file and contents of memory
		#VFD,file ↵	Compare data file and contents of memory
		#WF,file ↵	Save contents of memory to program file
		#WFD,file ↵	Save contents of memory to data file
		#CL,file ↵	Load ICE6200 set condition from file
		#CS,file ↵	Save ICE6200 set condition to file
		#OPTLD,1,file ↵ #OPTLD,2,file ↵	Load function option data from file Load segment option data from file
13	Coverage	#CVD ↵	Indicates coverage information
		#CVR ↵	Clears coverage information
14	ROM Access	#RP ↵	Move contents of ROM to program memory
		#VP ↵	Compare contents of ROM with contents of program memory
		#ROM ↵	Set ROM type
15	Terminate ICE	#Q ↵	Terminate ICE and return to operating system control
16	Command Display	#HELP ↵	Display ICE6200 instruction
17	Self Diagnosis	#CHK ↵	Report results of ICE6200 self diagnostic test

↵ means press the RETURN key.

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