MF697-04

EPSON

CMOS 4-BIT SINGLE CHIP MICROCOMPUTER

E0C62T3 TECHNICAL MANUAL

E0C62T3 Technical Hardware

E0C62T3 Technical Software

ENERGY SAVING EPSON

SEIKO EPSON CORPORATION

PREFACE

This manual is individualy described about the hardware and the software of the E0C62T3.

I. E0C62T3 Technical Hardware

This part explains the function of the E0C62T3, the circuit configurations, and details the controlling method.

II. E0C62T3 Technical Software

This part explains the programming method of the E0C62T3.

I. E0C62T3 Technical Hardware

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CHAPTER 1 OVERVIEW

The E0C62T3 is a single-chip microcomputer made up of the 4-bit core CPU E0C6200A, ROM (3,072 words, 12 bits to a word), RAM (640 words, 4 bits to a word), LCD driver, watchdog timer, time base counter, SVD circuit and DTMF/DP generator.
The E0C62T3 can be applied to telephone set which has feature as DTMF/DP switchable, repertory dial, ON/OFF hook dial, etc.

1.1 Features

OSC1 oscillation circuit .... Crystal oscillation circuit: 32,768 Hz (Typ.)
OSC3 oscillation circuit .... Crystal or ceramic oscillation circuit (selected by mask option):
3.579545 MHz (Typ.)
Instruction set .... 108 types
Instruction execution time .... During operation at 32 kHz: 153 µsec, 214 µsec, 366 µsec
(depending on instruction) During operation at 3.58 MHz: 11.1 µsec, 15.6 µsec, 26.7 µsec
ROM capacity .... 3,072 words × 12 bits
RAM capacity .... 640 words × 4 bits
Input port .... 11 bits (pull up resistors available by mask option)
Output port .... 8 bits (buzzer, hold-line and handfree output available by software control)
I/O port .... 4 bits (pull up resistors available by software control)
LCD driver .... 32 segments × 4 / 3 / 2 / 1 commons
(the drive duty can be selected by software)
Regulated voltage circuit and booster voltage circuit built-in
(compatible with 3–4.5 V LCD, VR adjustable)
DTMF generator .... Built-in
DP generator .... Built-in
Time base counter .... Built-in
Watchdog timer .... Built-in
SVD (supply voltage detection) .... 1.8 V
External interrupt .... Input port interrupt: 4 systems
Internal interrupt .... Timer interrupt: 1 system
Dialling interrupt: 1 system
Supply voltage .... 1.6 V to 5.5 V (32 kHz)
2.5 V to 5.5 V (OSC3 = ON, DTMF)
Current consumption (Typ.) .... During HALT: 2 µA (3 V, 32 kHz)
During operation: 5 µA (3 V, 32 kHz)
200 µA (3 V, 3.58 MHz)
During DTMF operation: 1.3 mA (3 V, 3.58 MHz)
Package .... QFP5-80pin / QFP14-80pin (plastic) or die form

1.2 Block Diagram

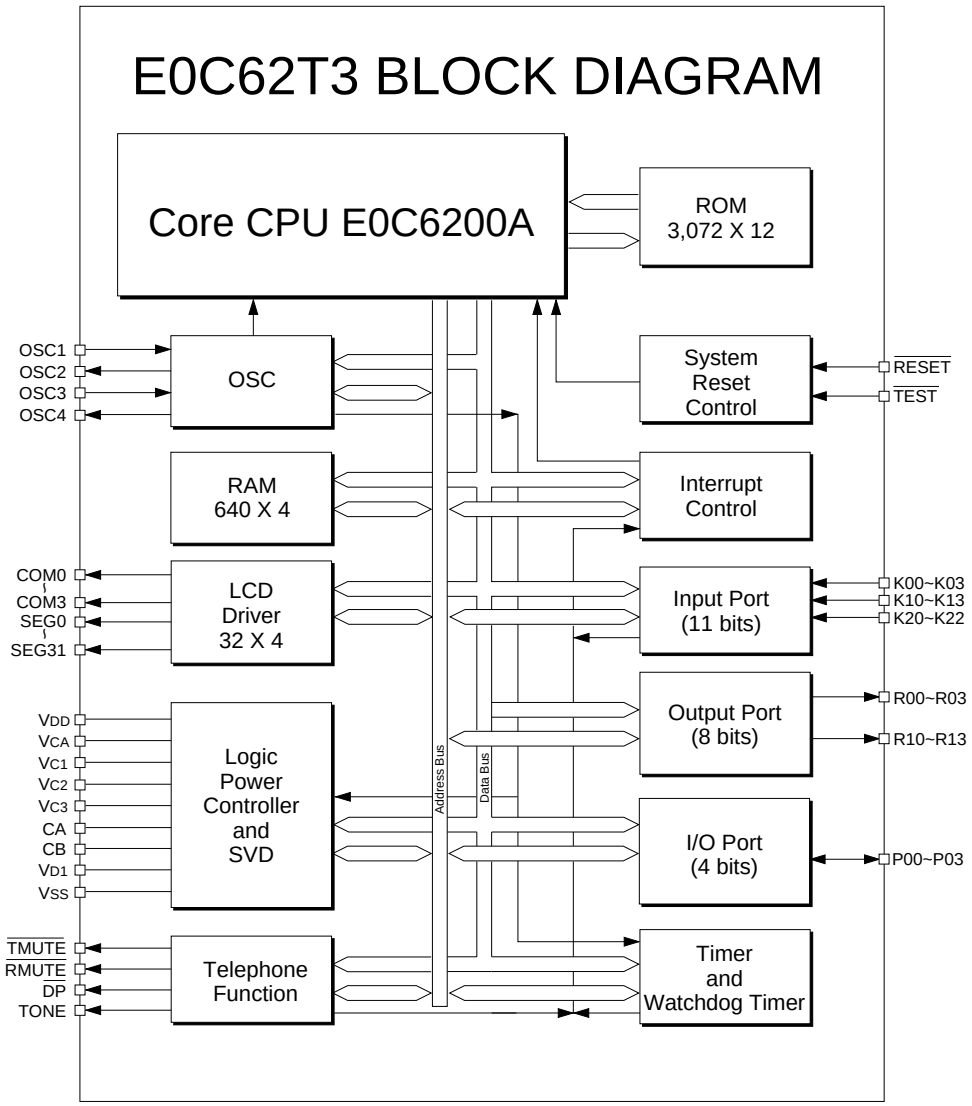


Fig. 1.2.1
E0C62T3 block diagram

1.3 Pin Layout Diagram

QFP5-80pin

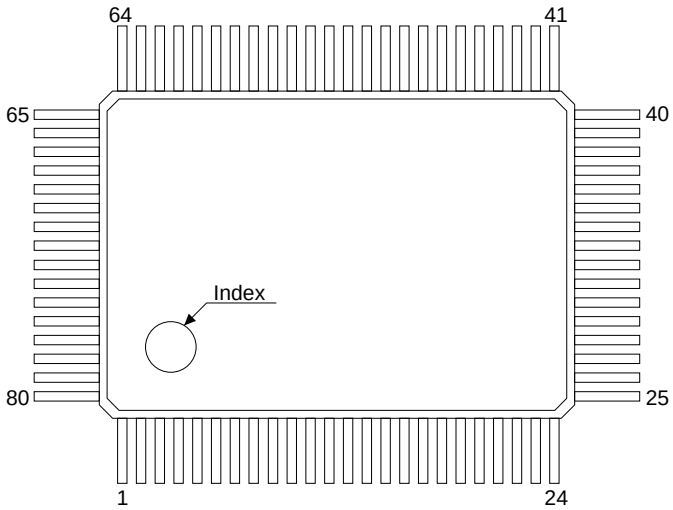


Fig. 1.3.1
Pin layout diagram (QFP5-80pin)

Table 1.3.1
Pin name (QFP5-80pin)

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	SEG14	21	P02	41	R12	61	V_{C3}
2	SEG15	22	P03	42	R13	62	V_{C2}
3	SEG16	23	$\overline{TEST}$	43	$\overline{RESET}$	63	COM0
4	SEG17	24	K00	44	V_{DD}	64	COM1
5	SEG18	25	K01	45	$\overline{RMUTE}$	65	COM2
6	SEG19	26	K02	46	$\overline{TMUTE}$	66	COM3
7	SEG20	27	K03	47	$\overline{DP}$	67	SEG0
8	SEG21	28	K10	48	V_{SS}	68	SEG1
9	SEG22	29	K11	49	OSC1	69	SEG2
10	SEG23	30	K12	50	OSC2	70	SEG3
11	SEG24	31	K13	51	OSC3	71	SEG4
12	SEG25	32	K20	52	OSC4	72	SEG5
13	SEG26	33	K21	53	V_{D1}	73	SEG6
14	SEG27	34	K22	54	TONE	74	SEG7
15	SEG28	35	R00	55	N.C.	75	SEG8
16	SEG29	36	R01	56	N.C.	76	SEG9
17	SEG30	37	R02	57	CA	77	SEG10
18	SEG31	38	R03	58	CB	78	SEG11
19	P00	39	R10	59	V_{C1}	79	SEG12
20	P01	40	R11	60	V_{CA}	80	SEG13

N.C. = No Connection

QFP14-80pin

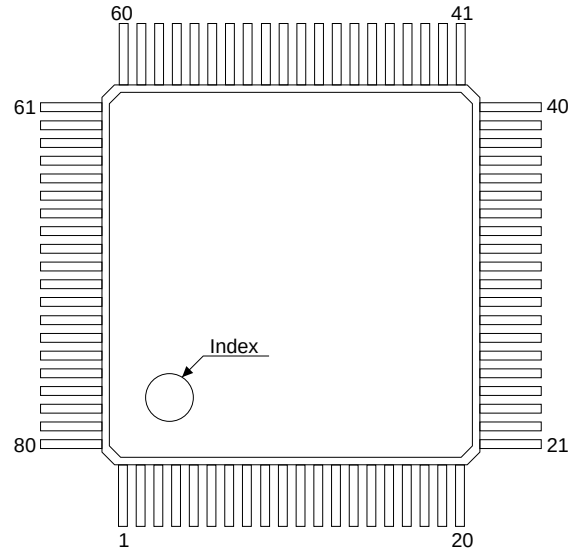


Fig. 1.3.2
Pin layout diagram
(QFP14-80pin)

Table 1.3.2
Pin name (QFP14-80pin)

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	N.C.	21	COM0	41	SEG16	61	$\overline{\text{TEST}}$
2	$\overline{\text{RESET}}$	22	COM1	42	SEG17	62	K00
3	V_{DD}	23	COM2	43	SEG18	63	K01
4	$\overline{\text{RMUTE}}$	24	COM3	44	SEG19	64	K02
5	$\overline{\text{TMUTE}}$	25	SEG0	45	SEG20	65	K03
6	$\overline{\text{DP}}$	26	SEG1	46	SEG21	66	K10
7	V_{SS}	27	SEG2	47	SEG22	67	K11
8	OSC1	28	SEG3	48	SEG23	68	K12
9	OSC2	29	SEG4	49	SEG24	69	K13
10	OSC3	30	SEG5	50	SEG25	70	K20
11	OSC4	31	SEG6	51	SEG26	71	K21
12	V_{D1}	32	SEG7	52	SEG27	72	K22
13	TONE	33	SEG8	53	SEG28	73	R00
14	N.C.	34	SEG9	54	SEG29	74	R01
15	CA	35	SEG10	55	SEG30	75	R02
16	CB	36	SEG11	56	SEG31	76	R03
17	V_{C1}	37	SEG12	57	P00	77	R10
18	V_{CA}	38	SEG13	58	P01	78	R11
19	V_{C3}	39	SEG14	59	P02	79	R12
20	V_{C2}	40	SEG15	60	P03	80	R13

N.C. = No Connection

1.4 Pin Description

Table 1.4.1 Pin description

Pin Name	QFP5-80	QFP14-80	I/O	Function
V_{DD}	44	3		Power supply terminal (+)
V_{SS}	48	7		Power supply terminal (–)
V_{D1}	53	12	O	Internal logic system regulated voltage output terminal
V_{CA}	60	18	I	LCD system voltage adjustment terminal
V_{C1}	59	17	O	LCD system regulated voltage output terminal
V_{C2}	62	20	O	LCD system booster voltage output terminal (V_{C1} x 2)
V_{C3}	61	19	O	LCD system booster voltage output terminal (V_{C1} x 3)
CA,CB	57,58	15,16	–	LCD system voltage booster capacitor connecting terminals
OSC1	49	8	I	32.768 kHz crystal oscillator input terminal
OSC2	50	9	O	32.768 kHz crystal oscillator output terminal
OSC3	51	10	I	3.58 MHz crystal or ceramic oscillator input terminal (selected by mask option)
OSC4	52	11	O	3.58 MHz crystal or ceramic oscillator output terminal (selected by mask option)
K00~K03	24~27	62~65	I	Input terminals
K10~K13	28~31	66~69	I	Input terminals
K20~K22	32~34	70~72	I	Input terminals
P00~P03	19~22	57~60	I/O	I/O terminals (at input mode, pull-up resistors are selected by software)
R00~R03	35~38	73~76	O	Output terminals
R10~R13	39~42	77~80	O	Output terminals (buzzer, hold-line and handfree are selected by software)
SEG0~SEG31	67~18	25~56	O	LCD segment output terminals (DC output is selected by mask option)
COM0~COM3	63~66	21~24	O	LCD common output terminals (1/4, 1/3, 1/2, 1/1 duty programmable)
$\overline{\text{RESET}}$	43	2	I	Initial setting input terminal
$\overline{\text{TEST}}$	23	61	I	Test input terminal
$\overline{\text{RMUTE}}$	45	4	O	Receiver mute output terminal
$\overline{\text{TMUTE}}$	46	5	O	Transmitter mute output terminal
$\overline{\text{DP}}$	47	6	O	Dialing pulse output terminal
TONE	54	13	O	DTMF output terminal

CHAPTER 2 POWER SUPPLY AND INITIAL RESET

2.1 Power Supply

With a single external power supply (2 V to 5.5 V) supplied to VDD through VSS, the E0C62T3 generates the necessary internal voltage with the regulated voltage circuit (<VD1> for oscillators and internal circuit, <VC1> for LCDs) and the voltage booster circuit (<VC2, VC3> for LCDs).
A voltage reduction can be detected by the on-chip supply voltage detection circuit. (See Section 4.9, "SVD Circuit".)
Figure 2.1.1 shows the configuration of power supply.

Note: • *External loads cannot be driven by the regulated voltage and voltage booster circuit's output voltage.*

• *See Chapter 7, "ELECTRICAL CHARACTERISTICS" for voltage values.*

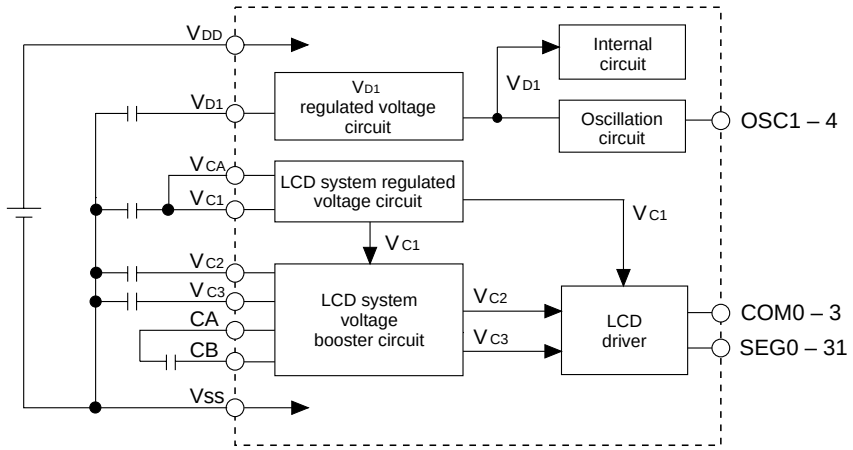


Fig. 2.1.1
Configuration of power supply

Voltage <V_{D1}> for oscillation circuit and internal circuit

V_{D1} is the voltage of the oscillation circuit and the internal logic circuit, and is generated by the V_{D1} regulated voltage circuit for stabilizing the oscillation.
Making V_{SS} the standard (logic level 0), the V_{D1} regulated voltage circuit generates V_{D1} from the supply voltage that is input from the V_{DD}–V_{SS} terminals.
See Chapter 7, "ELECTRICAL CHARACTERISTICS" for voltage values.

Voltage <V_{C1}, V_{C2} and V_{C3}> for LCD driving

V_{C1}, V_{C2} and V_{C3} are the voltages for LCD drive, and are generated by the LCD system regulated voltage circuit and the voltage booster circuit to stabilize the display quality.
V_{C1} is generated by the LCD system regulated voltage circuit with V_{SS} as the standard from the supply voltage input from the V_{DD}–V_{SS} terminals.
V_{C2} and V_{C3} are respectively double and triple obtained from the voltage booster circuit.
The V_{C1} voltage can be adjusted to match the LCD panel characteristics by applying feedback to the V_{CA} terminal using resistances RA1 and RA2 as shown in Figure 2.1.2.
The voltage V_C ($\approx V_{C1}$–V_{SS}) of V_{C1} at this time is shown by the following expression:

$$V_C \approx 1 \times (R_{A1} + R_{A2}) / R_{A1}$$

Example:

V_C	R_{A1}	R_{A2}
About 1 V	∞	0 Ω
About 1.5 V	2 MΩ	1 MΩ

See Chapter 7, "ELECTRICAL CHARACTERISTICS" for voltage values.

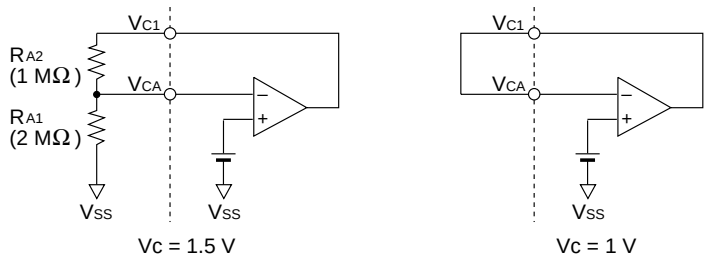


Fig. 2.1.2
Vc adjustment circuit

2.2 Initial Reset

To initialize the E0C62T3 circuits, initial reset must be executed. There are four ways of doing this.

(1) External initial reset by the $\overline{\text{RESET}}$ terminal
(2) External initial reset by simultaneous low input to terminals K00–K03
(3) Initial reset by the oscillation detection circuit
(4) Initial reset by watchdog timer

Be sure to use reset functions (1) or (2) when making the power and be sure to initialize securely. In normal operation, the circuit may be initialized by any of the above four types.

Figure 2.2.1 shows the configuration of the initial reset circuit.

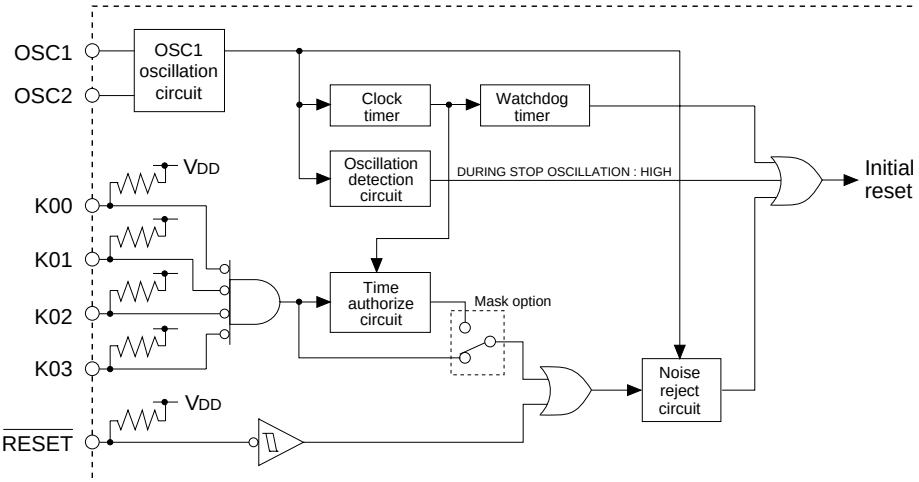


Fig. 2.2.1
Configuration of the initial reset circuit

Reset terminal ($\overline{\text{RESET}}$)

Initial reset can be executed externally by setting the reset terminal to the low level.
The initial resetting can be done by externally setting the reset terminal to a low level. However, be sure to observe the following precautions, because the $\overline{\text{RESET}}$ signal passes through the noise reject circuit.
When the reset terminal is used for initial resetting during operation, a pulse (low level) of 0.4 msec or less is considered to be noise by the noise reject circuit. Maintain a low level of 1.5 msec (when the oscillation frequency f_{OSC1} = 32 kHz) to securely perform the initial reset. When the reset terminal goes high, the CPU begins to operate.
Since the noise reject circuit does not operate when oscillation is stopped, the noise reject circuit is bypassed until it starts oscillation. For this reason, be sure to maintain a low level the reset input in the oscillation stopped status, such as at the time of power making, until starting oscillation.

Simultaneous low input to terminals K00–K03

Another way of executing initial reset externally is to input a low signal simultaneously to the input ports (K00–K03) selected with the mask option.
Since this initial reset also passes through the same noise reject circuit as the reset terminal, you should maintain the specified input port terminal at low level for 1.5 msec (when oscillation frequency f_{OSC1} = 32 kHz) or more during operation and until it begins oscillation at times such as when making power.
Table 2.2.1 shows the combinations of input ports (K00–K03) that can be selected with the mask option.

Table 2.2.1
Combinations of input ports

A	Not use
B	K00*K01
C	K00*K01*K02
D	K00*K01*K02*K03

When, for instance, mask option D (K00*K01*K02*K03) is selected, initial reset is executed when the signals input to the four ports K00–K03 are all low at the same time. The initial reset is done, even when a key entry including a combination of selected input ports is made.
Further, the time authorize circuit can be selected with the mask option. The time authorize circuit performs initial reset, when the input time of the simultaneous low input is authorized and found to be the same or more than the defined time (1 to 2 sec). Since clock timer output is used for time authorization, when the clock timer is reset during time authorization, the authorization time is also reduced. (The shortest is 1.5 msec due to the noise reject circuit.)

If you use this function, make sure that the specified ports do not go low at the same time during ordinary operation.

Oscillation detection circuit

When the oscillation detection circuit detects the stoppage of oscillation of the crystal oscillation circuit (OSC1), it generates an initial reset within 10 seconds.
This is a reset function in cases where oscillation is stopped due to such things as a drop in the supply voltage.
In addition, it uses a simultaneous low input of the input ports (K00–K03) or reset terminal for the initial reset at the time of making power and you should not execute it by this function alone.

Watchdog timer

If the CPU runs away for some reason, the watchdog timer will detect this situation and output an initial reset signal. See Section 4.2, "Watchdog Timer" for details.
As with the oscillation detection circuit, you should not do an initial reset at the time of making power using this function.

Internal register at initial resetting

Initial reset initializes the CPU as shown in the table below.

Table 2.2.2 Initial values

CPU core			
Name	Symbol	Number of bits	Setting value
Program counter step	PCS	8	00H
Program counter page	PCP	4	1H
New page pointer	NPP	4	1H
Stack pointer	SP	8	Undefined
Index register IX	IX	11	Undefined
Index register IY	IY	11	Undefined
Register pointer	RP	4	Undefined
General-purpose register A	A	4	Undefined
General-purpose register B	B	4	Undefined
Interrupt flag	I	1	0
Decimal flag	D	1	0
Zero flag	Z	1	Undefined
Carry flag	C	1	Undefined

Peripheral circuits		
Name	Number of bits	Setting value
RAM	640 x 4	Undefined
Display memory	32 x 4	Undefined
Other peripheral circuits	–	*1

*1 See Section 4.1, "Memory Map".

2.3 Test Terminals ($\overline{\text{TEST}}$)

This is the terminal that is used at the time of the factory inspection of the IC. During normal operation, make the $\overline{\text{TEST}}$ an N.C. (no connection).

CHAPTER 3 CPU, ROM, RAM

3.1 CPU

The E0C62T3 employs the 4-bit core CPU E0C6200A for the CPU, so that register configuration, instructions and so forth are virtually identical to those in other family processors using the E0C6200A.
Refer to "E0C6200/6200A Core CPU Manual" for details about the E0C6200A.
Note the following points with regard to the E0C62T3:

(1) The SLEEP operation is not provided, so the SLP instruction cannot be used.

(2) Because the ROM capacity is 3,072 words, bank bits are unnecessary and PCB and NBP are not used.

(3) RAM is set up to five pages, so the three low-order bits are valid for the page portion (XP, YP) of the index register that specifies addresses. (The most high-order bit is ignored.)

3.2 ROM

The built-in ROM, a mask ROM for loading the program, has a capacity of 3,072 steps, 12 bits each. The program area is 12 pages (0–11), each of 256 steps (00H–FFH). After initial reset, the program beginning address is page 1, step 00H. The interrupt vector is allocated to page 1, steps 02H–0DH.

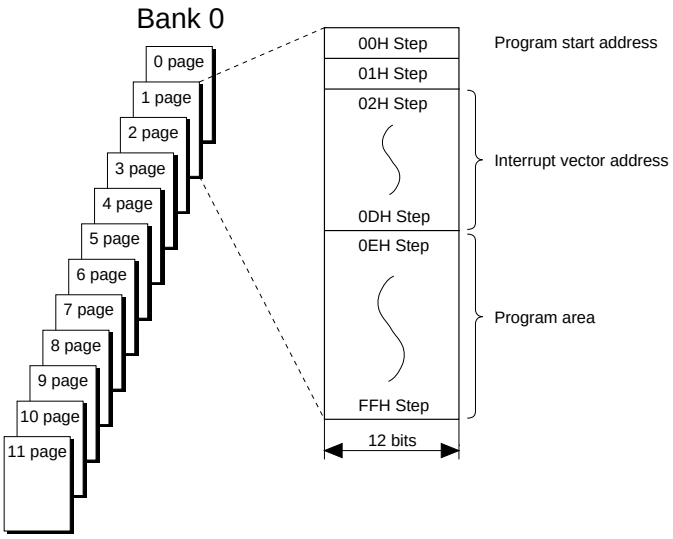


Fig. 3.2.1
ROM configuration

3.3 RAM

The RAM, a data memory storing a variety of data, has a capacity of 640 words, each of four bits. When programming, keep the following points in mind.

(1) Part of the data memory can be used as stack area when subroutine calls and saving registers, so be careful not to overlap the data area and stack area.

(2) Subroutine calls and interrupts take up three words of the stack area.

(3) The data memory 000H–00FH is for the register pointers (RP), and is the addressable memory register area.

CHAPTER 4 PERIPHERAL CIRCUITS AND OPERATION

Peripheral circuits (timer, I/O, and so on) of the E0C62T3 are memory mapped, and interfaced with the CPU. Thus, all the peripheral circuits can be controlled by using the memory operation command to access the I/O memory in the memory map.
The following sections describe how the peripheral circuits operation.

4.1 Memory Map

Data memory of the E0C62T3 has an address space of 731 words, of which 48 words are allocated to display memory and 43 words to I/O memory.
Figures 4.1.1(a)–(b) present the overall memory maps of the E0C62T3, and Tables 4.1.1(a)–(i) the peripheral circuits' (I/O space) memory maps.
In the E0C62T3 the same I/O memory has been laid out for each page 0C0H–0EBH and the same display memory for 080H–0AFH. As a result, the I/O memory and display memory can be accessed without changing over the data memory page. The same result is obtained for I/O memory and display memory changes and for readable/writable address references, no matter on what page it is done.

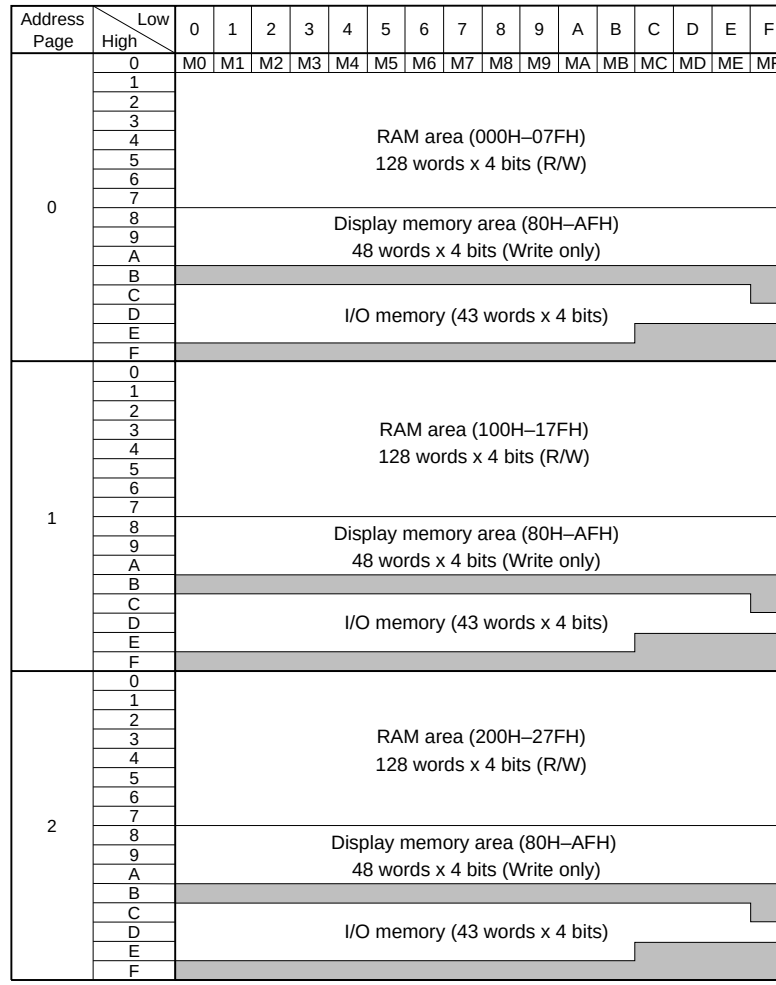


Fig. 4.1.1(a)
Memory map

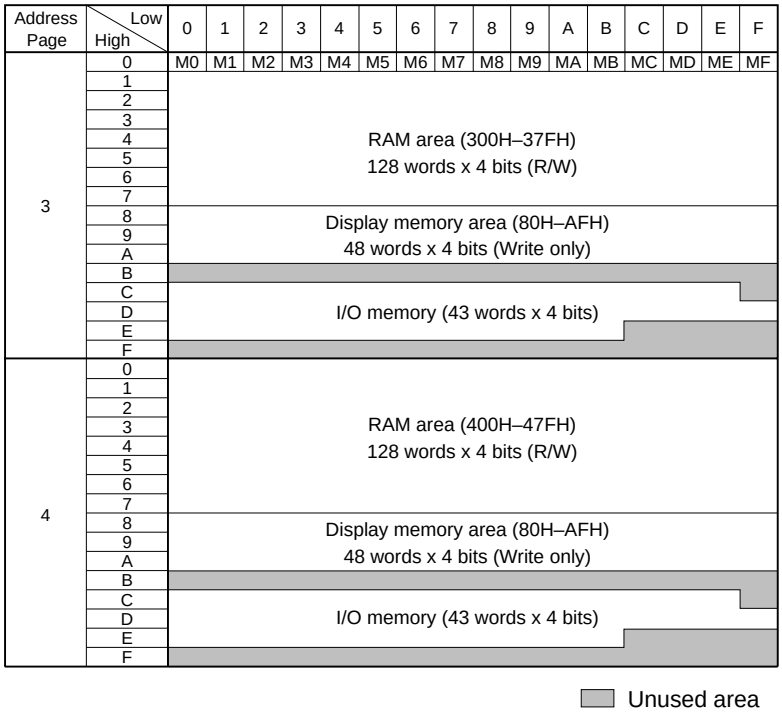


Fig. 4.1.1(b)
Memory map

Note: *Memory is not mounted in unused area within the memory map and in memory area not indicated in this chapter. For this reason, normal operation cannot be assured for programs that have been prepared with access to these areas.*

Table 4.1.1(a) I/O memory map (C0H–C4H)

Address *6	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
C0H	0	0	0	IK22	0	– *2			Unused *5
	R				0	– *2			Unused *5
					0	– *2			Unused *5
					IK22	0	Yes	No	Interrupt factor flag (K22) Clear to 0 after read out
C1H	0	0	0	IK2	0	– *2			Unused *5
	R				0	– *2			Unused *5
					0	– *2			Unused *5
					IK2	0	Yes	No	Interrupt factor flag (K20, K21) Clear to 0 after read out
C2H	0	0	0	IK1	0	– *2			Unused *5
	R				0	– *2			Unused *5
					0	– *2			Unused *5
					IK1	0	Yes	No	Interrupt factor flag (K10 ~ K13) Clear to 0 after read out
C3H	0	0	0	IK0	0	– *2			Unused *5
	R				0	– *2			Unused *5
					0	– *2			Unused *5
					IK0	0	Yes	No	Interrupt factor flag (K00 ~ K03) Clear to 0 after read out
C4H	IT1	IT2	IT16	IT32	IT1	0	Yes	No	Interrupt factor flag (clock timer 1 Hz) Clear to 0 after read out
	R				IT2	0	Yes	No	Interrupt factor flag (clock timer 2 Hz) Clear to 0 after read out
					IT16	0	Yes	No	Interrupt factor flag (clock timer 16 Hz) Clear to 0 after read out
					IT32	0	Yes	No	Interrupt factor flag (clock timer 32 Hz) Clear to 0 after read out

*1 Initial value at initial reset
*2 Not set in the circuit
*3 Undefined
*4 Inhibit state (output port will be set to "1")
*5 Constantly "0" when being read
*6 Page switching in I/O memory is not necessary

Table 4.1.1(b) I/O memory map (C5H–C9H)

Address *6	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
C5H	0	0	0	ID	0	– *2			Unused *5
	R				0	– *2			Unused *5
					0	– *2			Unused *5
					ID	0	Yes	No	Interrupt factor flag (dialing) Clear to 0 after read out
C6H	0	0	SIK21	SIK20	0	– *2			Unused *5
	R		R/W		0	– *2			Unused *5
					SIK21	0	Enable	Disable	Interrupt selection register (K21)
					SIK20	0	Enable	Disable	Interrupt selection register (K20)
C7H	SIK13	SIK12	SIK11	SIK10	SIK13	0	Enable	Disable	Interrupt selection register (K13)
	R/W				SIK12	0	Enable	Disable	Interrupt selection register (K12)
					SIK11	0	Enable	Disable	Interrupt selection register (K11)
					SIK10	0	Enable	Disable	Interrupt selection register (K10)
C8H	SIK03	SIK02	SIK01	SIK00	SIK03	0	Enable	Disable	Interrupt selection register (K03)
	R/W				SIK02	0	Enable	Disable	Interrupt selection register (K02)
					SIK01	0	Enable	Disable	Interrupt selection register (K01)
					SIK00	0	Enable	Disable	Interrupt selection register (K00)
C9H	0	K22	K21	K20	0	– *2			Unused *5
	R				K22	– *2	High	Low	Input port (K20 ~ K22)
					K21	– *2	High	Low	
					K20	– *2	High	Low	

*1 Initial value at initial reset
*2 Not set in the circuit
*3 Undefined
*4 Inhibit state (output port will be set to "1")
*5 Constantly "0" when being read
*6 Page switching in I/O memory is not necessary

Table 4.1.1(c) I/O memory map (CAH–CEH)

Address *6	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
CAH	K13	K12	K11	K10	K13	– *2	High	Low	Input port (K10 ~ K13)
	R				K12	– *2	High	Low	
					K11	– *2	High	Low	
					K10	– *2	High	Low	
CBH	K03	K02	K01	K00	K03	– *2	High	Low	Input port (K00 ~ K03)
	R				K02	– *2	High	Low	
					K01	– *2	High	Low	
					K00	– *2	High	Low	
CCH	0	DFK22	DFK21	DFK20	0	– *2			Unused *5
	R	R/W			DFK22	1	↓	↑	Input comparison register (K20 ~ K22)
					DFK21	1	↓	↑	
					DFK20	1	↓	↑	
CDH	DFK13	DFK12	DFK11	DFK10	DFK13	1	↓	↑	Input comparison register (K10 ~ K13)
	R/W				DFK12	1	↓	↑	
					DFK11	1	↓	↑	
					DFK10	1	↓	↑	
CEH	DFK03	DFK02	DFK01	DFK00	DFK03	1	↓	↑	Input comparison register (K00 ~ K03)
	R/W				DFK02	1	↓	↑	
					DFK01	1	↓	↑	
					DFK00	1	↓	↑	

*1 Initial value at initial reset
*2 Not set in the circuit
*3 Undefined
*4 Inhibit state (output port will be set to "1")
*5 Constantly "0" when being read
*6 Page switching in I/O memory is not necessary

Table 4.1.1(d) I/O memory map (CFH–D3H)

Address *6	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
CFH									Unused
D0H	EIK22	EIK2	EIK1	EIK0	EIK22	0	Enable	Mask	Interrupt mask register (K22)
	R/W				EIK2	0	Enable	Mask	Interrupt mask register (K20, K21)
					EIK1	0	Enable	Mask	Interrupt mask register (K10 ~ K13)
					EIK0	0	Enable	Mask	Interrupt mask register (K00 ~ K03)
D1H	EIT1	EIT2	EIT16	EIT32	EIT1	0	Enable	Mask	Interrupt mask register (clcok timer 1 Hz)
	R/W				EIT2	0	Enable	Mask	Interrupt mask register (clock timer 2 Hz)
					EIT16	0	Enable	Mask	Interrupt mask register (clock timer 16 Hz)
					EIT32	0	Enable	Mask	Interrupt mask register (clock timer 32 Hz)
D2H	0	0	0	EID	0	– *2			Unused *5
	R			R/W	0	– *2			Unused *5
					0	– *2			Unused *5
					EID	0	Enable	Mask	Interrupt mask register (dialing)
D3H	R13	R12	R11	R10	R13	0	High	Low	Output port (R13)
	HFO				HFO	– *4	– *4	ON	Handfree output (HFO)
	HFO	HDO	BZ	$\overline{BZ}$	R12	0	High	Low	Output port (R12)
					HDO	– *4	– *4	ON	Hold-line output (HDO)
	R/W				R11	0	High	Low	Output port (R11)
					BZ	– *4	– *4	ON	Buzzer output (BZ)
					R10	0	High	Low	Output port (R10)
					$\overline{BZ}$	– *4	– *4	ON	Buzzer inverted output ($\overline{BZ}$)

*1 Initial value at initial reset
*2 Not set in the circuit
*3 Undefined
*4 Inhibit state (output port will be set to "1")
*5 Constantly "0" when being read
*6 Page switching in I/O memory is not necessary

Table 4.1.1(e) I/O memory map (D4H–D8H)

Address *6	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
D4H	R03	R02	R01	R00	R03	0	High	Low	Output port (R00 ~ R03)
	R/W				R02	0	High	Low	
					R01	0	High	Low	
					R00	0	High	Low	
D5H	IOC3	IOC2	IOC1	IOC0	IOC3	0	Output	Input	I/O control register
	R/W				IOC2	0	Output	Input	
					IOC1	0	Output	Input	
					IOC0	0	Output	Input	
D6H	PUP3	PUP2	PUP1	PUP0	PUP3	0	ON	OFF	Pull up control register
	R/W				PUP2	0	ON	OFF	
					PUP1	0	ON	OFF	
					PUP0	0	ON	OFF	
D7H	P03	P02	P01	P00	P03	1	High	Low	I/O port
	R/W				P02	1	High	Low	
					P01	1	High	Low	
					P00	1	High	Low	
D8H	0	0	CLKCHG	OSCC	0	– *2			Unused *5
	R		R/W		0	– *2			Unused *5
					CLKCHG	0	OSC3	OSC1	CPU system clock switch
					OSCC	0	ON	OFF	OSC3 oscillation ON/OFF

*1 Initial value at initial reset
*2 Not set in the circuit
*3 Undefined
*4 Inhibit state (output port will be set to "1")
*5 Constantly "0" when being read
*6 Page switching in I/O memory is not necessary

Table 4.1.1(f) I/O memory map (D9H–DDH)

Address *6	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
D9H	0	0	0	TMRST	0	– *2			Unused *5
	R			W	0	– *2			Unused *5
					0	– *2			Unused *5
					TMRST	– *2	Reset	Invalid	Clock timer reset *5
DAH	TM3	TM2	TM1	TM0	TM3	– *3			Clock timer data (low-order) 16 Hz
	R				TM2	– *3			Clock timer data (low-order) 32 Hz
					TM1	– *3			Clock timer data (low-order) 64 Hz
					TM0	– *3			Clock timer data (low-order) 128 Hz
DBH	TM7	TM6	TM5	TM4	TM7	– *3			Clock timer data (high-order) 1 Hz
	R				TM6	– *3			Clock timer data (high-order) 2 Hz
					TM5	– *3			Clock timer data (high-order) 4 Hz
					TM4	– *3			Clock timer data (high-order) 8 Hz
DCH	WDON	WDRST	WD1	WD0	WDON	0	ON	OFF	Watchdog timer ON/OFF
	R/W	W	R		WDRST	Reset	Reset	Invalid	Watchdog timer reset *5
					WD1	0			Watchdog timer data 1/4 Hz
					WD0	0			Watchdog timer data 1/2 Hz
DDH	BZR11	BZR10	0	BZFQ	BZR11	0	Buzzer	DC	R11 port output selection
	R/W		R	R/W	BZR10	0	Buzzer (inverted)	DC	R10 port output selection
					0	– *2			Unused *5
					BZFQ	0	2 kHz	4 kHz	Buzzer frequency selection

*1 Initial value at initial reset
*2 Not set in the circuit
*3 Undefined
*4 Inhibit state (output port will be set to "1")
*5 Constantly "0" when being read
*6 Page switching in I/O memory is not necessary

Table 4.1.1(g) I/O memory map (DEH–E2H)

Address *6	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
DEH	LDTY1	LDTY0	0	LCDON	LDTY1	0			LCD drive duty selection 0 : 1/4, 1 : 1/3, 2 : 1/2, 3 : 1/1
	R/W		R	R/W	LDTY0	0			
					0	– *2			Unused *5
					LCDON	0	ON	OFF	LCD display control (LCD display all off)
DFH	0	0	SVDDT	SVDON	0	– *2			Unused *5
	R			R/W	0	– *2			Unused *5
					SVDDT	0	Supply voltage Low	Supply voltage Normal	Supply votage detector data
					SVDON	0	ON	OFF	SVD circuit ON/OFF
E0H	TPS	0	MB	DRS	TPS	0	PULSE	TONE	Tone / pulse mode selection
	R/W	R	R/W		0	– *2			Unused *5
					MB	0	33.3:66.6	40:60	Make : Break ratio selection
					DRS	0	20 pps	10 pps	Dialing pulse rate selection
E1H	PTS3	PTS2	PTS1	PTS0	PTS3	0			Pause time selection 0 : Use inhibited 8 : 8 sec 1 : 1 sec 9 : 9 sec 2 : 2 sec A : 10 sec 3 : 3 sec B : 11 sec 4 : 4 sec C : 12 sec 5 : 5 sec D : 13 sec 6 : 6 sec E : 14 sec 7 : 7 sec F : 15 sec
	R/W				PTS2	1			
					PTS1	0			
	Default value : 4 seconds				PTS0	0			
E2H	FTS3	FTS2	FTS1	FTS0	FTS3	0			Flash time selection 0 : Use inhibited 8 : 750 ms 1 : 94 ms 9 : 844 ms 2 : 188 ms A : 938 ms 3 : 281 ms B : 1031 ms 4 : 375 ms C : 1125 ms 5 : 469 ms D : 1219 ms 6 : 563 ms E : 1313 ms 7 : 656 ms F : 1406 ms
	R/W				FTS2	1			
					FTS1	1			
	Default value : 563 ms				FTS0	0			

*1 Initial value at initial reset
*2 Not set in the circuit
*3 Undefined
*4 Inhibit state (output port will be set to "1")
*5 Constantly "0" when being read
*6 Page switching in I/O memory is not necessary

Table 4.1.1(h) I/O memory map (E3H–E7H)

Address *6	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
E3H	0	HOLD	PAUSE	FLASH	0	– *2			Unused *5
	R	R/W	W		HOLD	0	On	Off	Hold-line function
					PAUSE	0	Yes	No	Pause function *5
					FLASH	0	Yes	No	Flash function *5
E4H	HF	0	0	0	HF	0	Yes	No	Hand free
	R/W	R			0	– *2			Unused *5
					0	– *2			Unused *5
					0	– *2			Unused *5
E5H	IDP3	IDP2	IDP1	IDP0	IDP3	1			Inter-digit pause selection for dial pulse 0 : Use inhibited 8 : 750 ms 1 : 94 ms 9 : 844 ms 2 : 188 ms A : 938 ms 3 : 281 ms B : 1031 ms 4 : 375 ms C : 1125 ms 5 : 469 ms D : 1219 ms 6 : 563 ms E : 1313 ms 7 : 656 ms F : 1406 ms
	R/W				IDP2	0			
	Default value : 750 ms				IDP1	0			
					IDP0	0			
E6H	0	0	SINR	SINC	0	– *2			Unused *5
	R		R/W		0	– *2			Unused *5
					SINR	1	Enable	Disable	DTMF row frequency output enable
					SINC	1	Enable	Disable	DTMF column frequency output enable
E7H	TCD3	TCD2	TCD1	TCD0	TCD3	0			Telephone code for dialing TCD DTMF DP TCD DTMF DP 0 : (R_1C_4) Use inhibited 8 : (R_3C_2) 8 1 : (R_1C_1) 1 9 : (R_3C_3) 9 2 : (R_1C_2) 2 A : (R_4C_2) 10 3 : (R_1C_3) 3 B : (R_4C_3) 11 4 : (R_2C_1) 4 C : (R_4C_1) 12 5 : (R_2C_2) 5 D : (R_2C_4) 13 6 : (R_2C_3) 6 E : (R_4C_4) 14 7 : (R_3C_1) 7 F : (R_3C_4) 15
	R/W				TCD2	0			
					TCD1	0			
					TCD0	0			

*1 Initial value at initial reset
*2 Not set in the circuit
*3 Undefined
*4 Inhibit state (output port will be set to "1")
*5 Constantly "0" when being read
*6 Page switching in I/O memory is not necessary

Table 4.1.1(i) I/O memory map (E8H–EBH)

Address *6	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
E8H	0	0	CRMUT	CTMUT	0	– *2			Unused *5
	R		R/W		0	– *2			Unused *5
					CRMUT	1	Receive mute output	0	Receive mute control
					CTMUT	1	Transmit mute output	0	Transmit mute control
E9H	0	0	0	HSON	0	– *2			Unused *5
	R			R/W	0	– *2			Unused *5
					0	– *2			
					HSON	0	Hook Off	Hook On	Hook switch ON/OFF
EAH	CHFO	CHDO	0	0	CHFO	0	Handfree output	DC	R13 output selection (R13 data register has to be "0")
	R/W		R		CHDO	0	Hold output	DC	R12 output selection (R12 data register has to be "0")
					0	– *2			Unused *5
					0	– *2			Unused *5
EBH	CTO	0	0	0	CTO	0	Continuous tone output ON	Continuous tone output OFF	Tone duration time control
	R/W	R			0	– *2			Unused *5
					0	– *2			Unused *5
					0	– *2			Unused *5
									Unused

*1 Initial value at initial reset
*2 Not set in the circuit
*3 Undefined
*4 Inhibit state (output port will be set to "1")
*5 Constantly "0" when being read
*6 Page switching in I/O memory is not necessary

4.2 Watchdog Timer

Configuration of watchdog timer

The E0C62T3 incorporates a watchdog timer as the source oscillator for OSC1 (clock timer 1 Hz signal). The watchdog timer can be controlled by WDON register. The watchdog timer has to be turned on when it is being used.
When the watchdog timer is used, it must be reset cyclically by the software. If reset is not executed in at least 3 seconds, the initial reset signal is output automatically for the CPU.
Figure 4.2.1 is the block diagram of the watchdog timer.

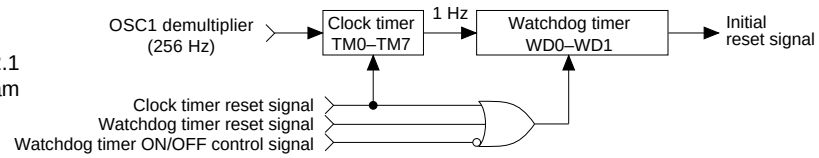


Fig. 4.2.1
Watchdog timer block diagram

The watchdog timer, configured of a two-bit binary counter (WD0–WD1), generates the initial reset signal internally by overflow of the WD1 (1/4 Hz).
Watchdog timer reset processing in the program's main routine enables detection of program overrun, such as when the main routine's watchdog timer processing is bypassed. Ordinarily this routine is incorporated where periodic processing takes place, just as for the timer interrupt routine.
The watchdog timer can also be reset by the resetting of the clock timer.
The watchdog timer operates in the HALT mode. If the HALT status continues for 3 or 4 seconds, the initial reset signal restarts operation.

Control of watchdog timer

Table 4.2.1 lists the watchdog timer's control bits and their addresses.

Table 4.2.1 Control bits of watchdog timer

Address *6	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
D9H	0	0	0	TMRST	0	– *2			Unused *5
	R			W	0	– *2			Unused *5
					0	– *2			Unused *5
					TMRST	– *2	Reset	Invalid	Clock timer reset *5
DCH	WDON	WDRST	WD1	WD0	WDON	0	ON	OFF	Watchdog timer ON/OFF
	R/W	W	R		WDRST	Reset	Reset	Invalid	Watchdog timer reset *5
					WD1	0			Watchdog timer data 1/4 Hz
					WD0	0			Watchdog timer data 1/2 Hz

*1 Initial value at initial reset
*2 Not set in the circuit
*3 Undefined
*4 Inhibit state (Output port will be set to "1")
*5 Constantly "0" when being read
*6 Page switching in I/O memory is not necessary

TMRST: Clock timer reset (D9H•D0)

This is the bit for resetting the clock timer and the watchdog timer.

When "1" is written: Clock timer and watchdog timer are reset
When "0" is written: No operation
Reading: Always "0"

When "1" is written to TMRST, the clock timer and the watchdog timer are reset, and the operation restarts immediately after this.
When "0" is written to TMRST, no operation results.
This bit is dedicated for writing, and is always "0" for reading.

WDON: Watchdog timer ON/OFF (DCH•D3)

This bit is used to turn the watchdog timer ON/OFF.

When "1" is written: ON
When "0" is written: OFF
Reading: Valid

At initial reset, WDON is set to "0" and the watchdog timer is turned OFF. When watchdog timer is being used, it has to be turned ON, firstly.

WDRST: Watchdog timer reset (DCH•D2)

This is the bit for resetting the watchdog timer.

When "1" is written: Watchdog timer is reset
When "0" is written: No operation
Reading: Always "0"

When "1" is written to WDRST, the watchdog timer is reset, and the operation restarts immediately after this. When "0" is written to WDRST, no operation results.
This bit is dedicated for writing, and is always "0" for reading.

Programming note

When the watchdog timer is being used, the software must reset it within 3-second cycles, and timer data (WD0 and WD1) cannot be used for timer applications.

4.3 Oscillation Circuit

Configuration of oscillation circuit

The E0C62T3 has two oscillation circuits (OSC1 and OSC3). OSC1 is a crystal oscillation circuit that supplies the operating clock the CPU and peripheral circuits. OSC3 is either a crystal or ceramic oscillation circuit that supplies the operating clock the CPU and DTMF circuit. When processing with the E0C62T3 requires high-speed operation, the CPU source clock can be switched from OSC1 to OSC3.
Figure 4.3.1 is the block diagram of this oscillation system.

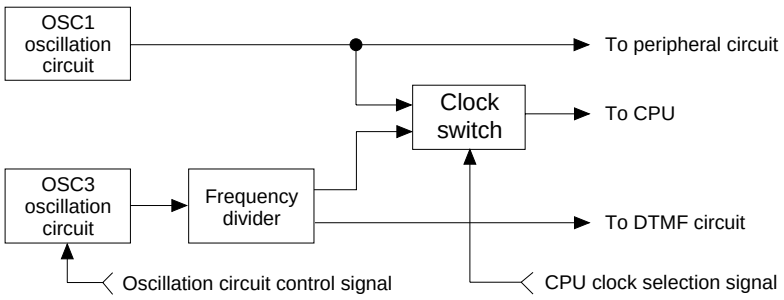


Fig. 4.3.1
Oscillation system

Selection of either OSC1 or OSC3 for the CPU's operating clock can be made through the software.

OSC1 oscillation circuit

The E0C62T3 has a built-in crystal oscillation circuit (OSC1 oscillation circuit). As an external element, the OSC1 oscillation circuit generates the operating clock for the CPU and peripheral circuitry by connecting the crystal oscillator (Typ. 32.768 kHz) and trimmer capacitor (5–25 pF).
Figure 4.3.2 is the block diagram of the OSC1 oscillation circuit.

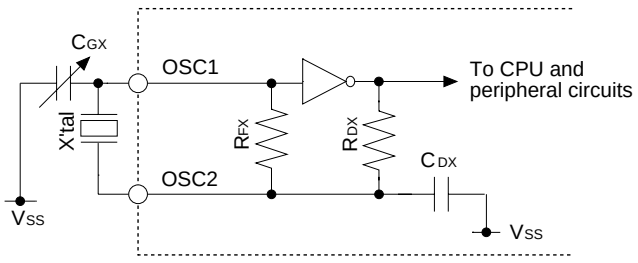


Fig. 4.3.2
OSC1 oscillation circuit

As Figure 4.3.2 indicates, the crystal oscillation circuit can be configured simply by connecting the crystal oscillator (X'tal) between terminals OSC1 and OSC2 to the trimmer capacitor (C_{GX}) between terminals OSC1 and V_{SS}.

OSC3 oscillation circuit

The E0C62T3 has twin clock specification. The mask option enables selection of either the crystal or ceramic oscillation circuit (OSC3 oscillation circuit) as the CPU's sub-clock and DTMF's operating clock.
Figure 4.3.3 is the block diagram of the OSC3 oscillation circuit.

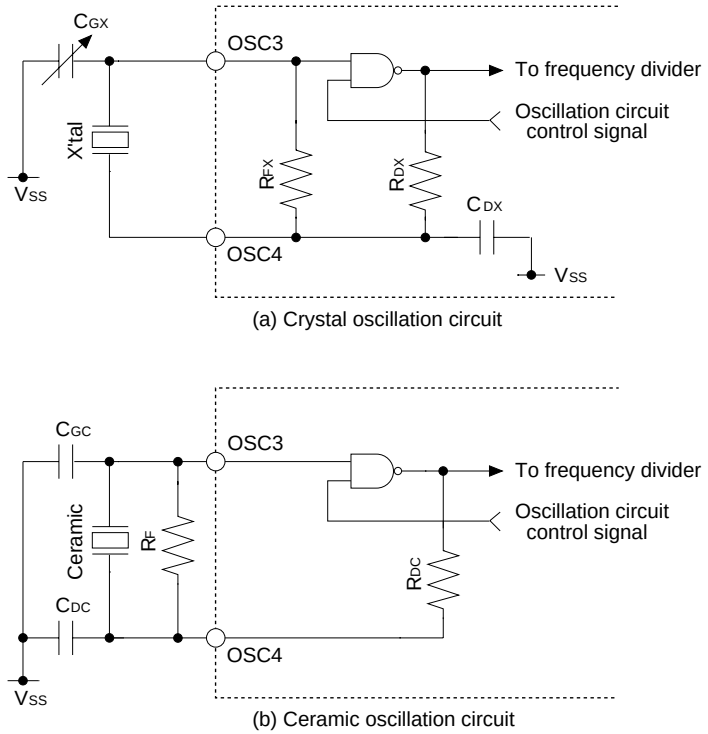


Fig. 4.3.3
OSC3 oscillation circuit

As Figure 4.3.3(a) indicates, the crystal oscillation circuit can be configured simply by connecting the crystal oscillator (Typ. 3.579545 MHz) between terminals OSC3 and OSC4 to the trimmer capacitor (CGX) between terminals OSC3 and VSS.
When ceramic oscillation is selected, the ceramic oscillation circuit can be configured by connecting the ceramic oscillator (Typ. 3.579545 MHz) and feedback resistor (RF) between terminals OSC3 and OSC4 to the two capacitors (CGC and CDC) located between terminals OSC3 and OSC4 and VSS. To lower current consumption of the OSC3 oscillation circuit, oscillation can be stopped through the software.

Control of oscillation circuit

Table 4.3.1 lists the control bits and their addresses for the oscillation circuit.

Table 4.3.1 Control bits of oscillation circuit

Address *6	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
D8H	0	0	CLKCHG	OSCC	0	– *2			Unused *5
	R		R/W		0	– *2			Unused *5
					CLKCHG	0	OSC3	OSC1	CPU system clock switch
					OSCC	0	ON	OFF	OSC3 oscillation ON/OFF

*1 Initial value at initial reset
*2 Not set in the circuit
*3 Undefined
*4 Inhibit state (output port will be set to "1")
*5 Constantly "0" when being read
*6 Page switching in I/O memory is not necessary

OSCC: OSC3 oscillation control (D8H•D0)

Controls oscillation ON/OFF for the OSC3 oscillation circuit.

When "1" is written: The OSC3 oscillation ON
When "0" is written: The OSC3 oscillation OFF
Reading: Valid

When it is necessary to activate DTMF generator or to operate the CPU at high speed, set OSCC to "1". At other times, set it to "0" to lessen the current consumption.
When "Not Use" is selected for the mask option of the OSC3 oscillation circuit, keep OSCC set to "0".
At initial reset, OSCC is set to "0".

CLKCHG: The CPU's clock switch (D8H•D1)

The CPU's operation clock is selected with this register.

When "1" is written: OSC3 clock is selected
When "0" is written: OSC1 clock is selected
Reading: Valid

When the CPU clock is to be OSC3, set CLKCHG to "1"; for OSC1, set CLKCHG to "0".
At initial reset, CLKCHG is set to "0".

Clock frequency and instruction execution time

Table 4.3.2 shows the instruction execution time according to each frequency of the system clock.

Table 4.3.2
Clock frequency and instruction execution time

Clock frequency	Instruction execution time (µsec)		
	5-clock instruction	7-clock instruction	12-clock instruction
OSC1: 32.768 kHz	152.6	213.6	366.2
OSC3: 3.58 MHz	11.1	15.6	26.7

Programming notes

(1) It takes at least 5 msec from the time the OSC3 oscillation circuit goes ON until the oscillation stabilizes. Consequently, when switching the CPU operation clock from OSC1 to OSC3, do this after a minimum of 5 msec have elapsed since the OSC3 oscillation went ON.
Further, the oscillation stabilization time varies depending on the external oscillator characteristics and conditions of use, so allow ample margin when setting the wait time.

(2) When switching the clock form OSC3 to OSC1, use a separate instruction for switching the OSC3 oscillation OFF. An error in the CPU operation can result if this processing is performed at the same time by the one instruction.

4.4 Input Ports (K00–K03, K10–K13, K20–K22)

Configuration of input ports

The E0C62T3 has two 4 bits and one 3 bits general-purpose input ports. Each of the input port terminals (K00–K03, K10–K13, K20–K22) provides internal pull up resistor. Pull up resistor can be selected for each bit with the mask option.
Figure 4.4.1 shows the configuration of input port.

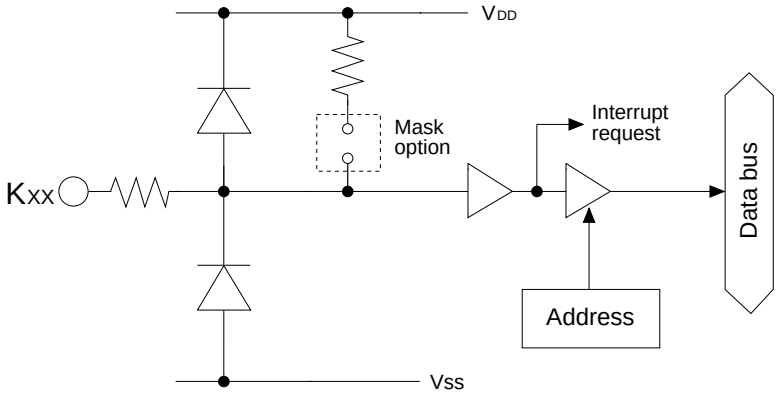


Fig. 4.4.1
Configuration of input port

Selection of "With pull up resistor" with the mask option suits input from the push switch, key matrix, and so forth. When "Gate direct" is selected, the port can be used for slide switch input and interfacing with other LSIs.

Interrupt function

All 11 bits of the input ports (K00–K03, K10–K13, K20–K22) provide the interrupt function and are divided into four interrupt systems. The conditions for issuing an interrupt can be set by the software. Further, whether to mask the interrupt function can be selected individually for all 11 bits by the software.

(1) K00–K03, K10–K13 and K20–K21 interrupts

Figure 4.4.2 shows the configuration of K00–K03, K10–K13 and K20–K21 interrupts circuit.

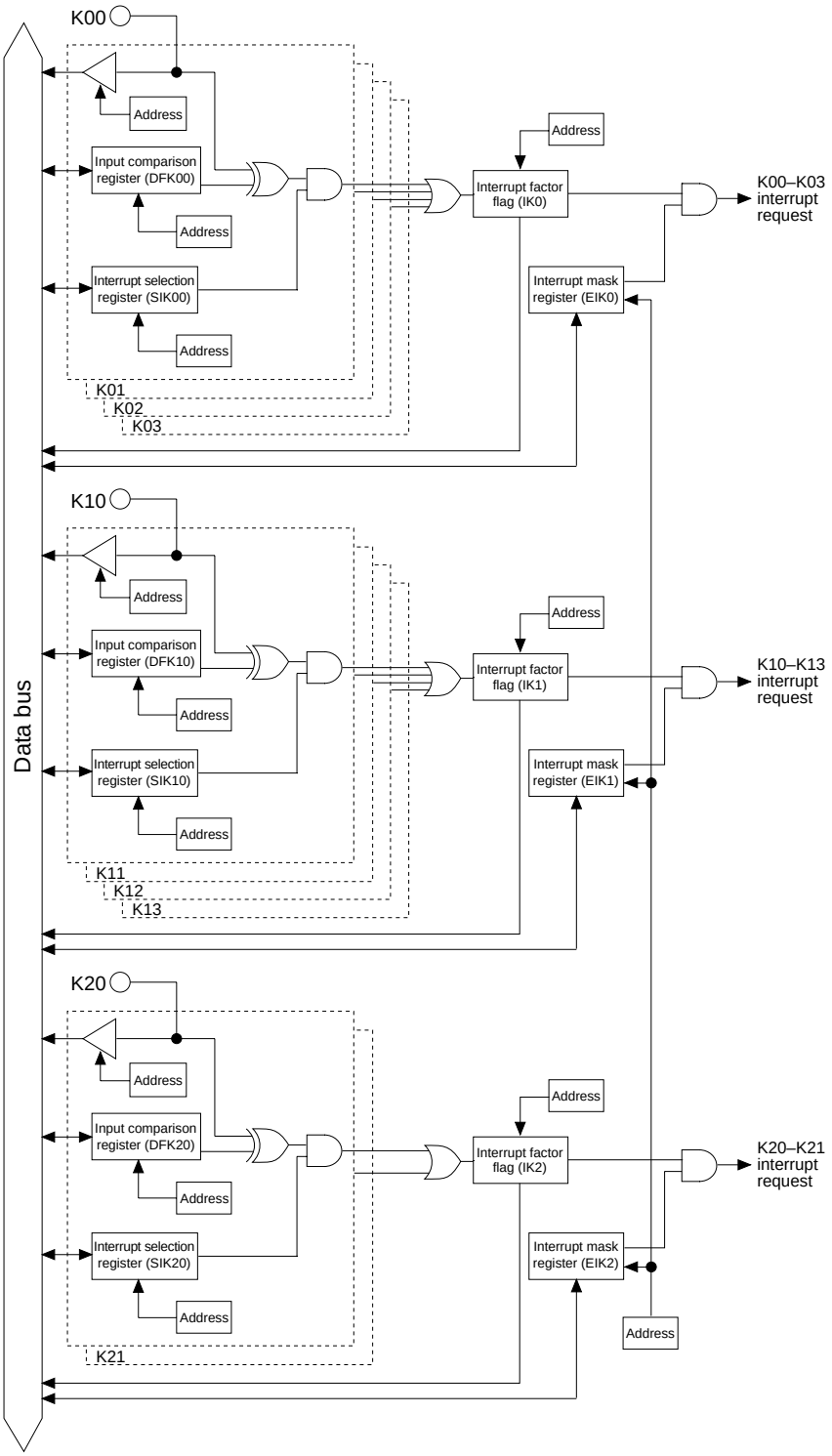


Fig. 4.4.2
Input interrupt circuit configuration (K00–K03, K10–K13, K20–K21)

The interrupt selection register (SIK) and input comparison register (DFK) are individually set for the input ports K00–K03, K10–K13 and K20–K21, and can specify the terminal for generating interrupt and interrupt timing.
The interrupt selection register (SIK) select what input terminal of input port to use for the interrupt. Writing "1" into an interrupt selection register incorporates that input port into the interrupt generation conditions. The changing the input port where the interrupt selection register has been set to "0" does not affect the generation of the interrupt.
The input interrupt timing can select that the interrupt be generated at the rising edge of the input or that it be generated at the falling edge according to the set value of the input comparison register (DFK).
By setting these two conditions, the interrupt for input ports are generated when an input port in which an interrupt has been enabled by the input selection register and the content of the input comparison register have been changed from matching to no matching.
The interrupt mask register (EIK) enables the interrupt mask to be selected for K00–K03, K10–K13, K20–K21 and K22.
When the interrupt is generated, the interrupt factor flag (IK) is set to "1".
Figure 4.4.3 shows an example of an interrupt for K00–K03.

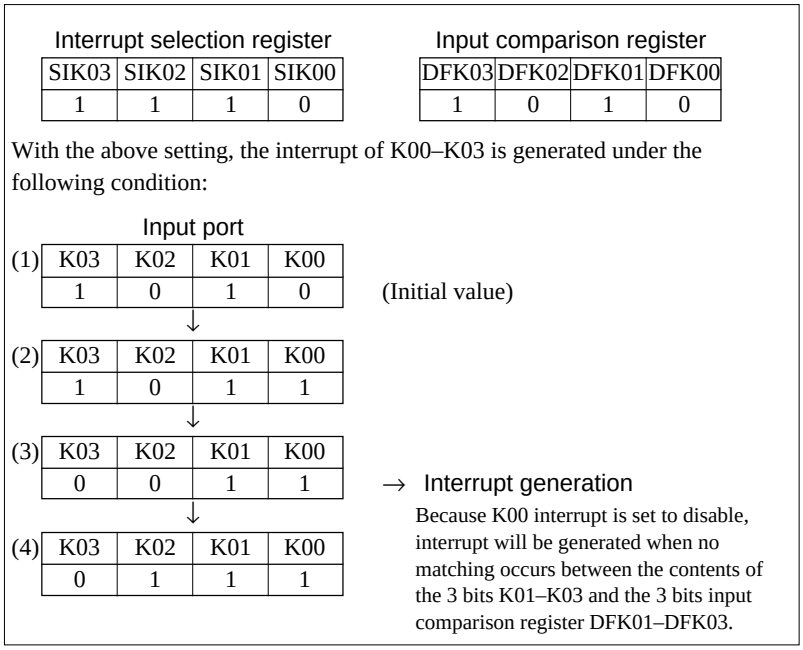


Fig. 4.4.3
Example of interrupt of K00–K03

K00 interrupt is disabled by the interrupt selection register (SIK00), so that an interrupt does not occur at (2). At (3), K03 changes to "0"; the data of the terminal that is interrupt enabled no longer matches the data of the input comparison register, so that interrupt occurs. As already explained, the condition for the interrupt to occur is the change in the port data and contents of the input comparison register from matching to no matching. Hence, in (4), when the no matching status changes to another no matching status, an interrupt does not occur. Further, terminals that have been masked for interrupt do not affect the conditions for interrupt generation.

(2) K22 interrupt

Figure 4.4.4 shows the configuration of K22 interrupt circuit.

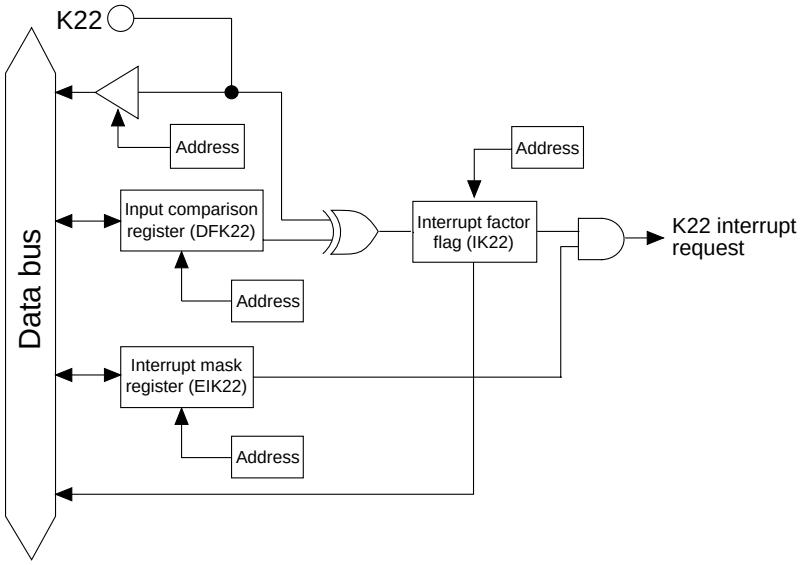


Fig. 4.4.4
Input interrupt circuit configuration (K22)

The input port K22 can generate interrupts for systems other then K00–K03, K10–K13 and K20–K21. The input comparison register (DFK22) is also set to the K22 port and can specify the timing for generating an interrupt. The interrupt generated timing is also the same as for K00–K03, K10–K13 and K20–K21, and when the content of the K22 input and the input comparison register changes from matching to no matching an interrupt is generated.
The interrupt mask register (EIK22) enables the interrupt mask to be selected for K22.
When the interrupt is generated, the interrupt factor flag (IK22) is set to "1".

Mask option

Internal pull up resistor can be selected for each of the 11 bits of the input ports (K00–K03, K10–K13, K20–K22) with the input port mask option.
When you have selected "Gate direct", take care that the floating status does not occur for the input. Select "With pull up resistor" for input ports that are not being used.

Control of input ports

Tables 4.4.1(a), (b) and (c) list the input ports control bits and their addresses.

Table 4.4.1(a) Input port control bits (1)

Address *6	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
C0H	0	0	0	IK22	0	– *2			Unused *5
	R				0	– *2			Unused *5
					0	– *2			Unused *5
					IK22	0	Yes	No	Interrupt factor flag (K22) Clear to 0 after read out
C1H	0	0	0	IK2	0	– *2			Unused *5
	R				0	– *2			Unused *5
					0	– *2			Unused *5
					IK2	0	Yes	No	Interrupt factor flag (K20, K21) Clear to 0 after read out
C2H	0	0	0	IK1	0	– *2			Unused *5
	R				0	– *2			Unused *5
					0	– *2			Unused *5
					IK1	0	Yes	No	Interrupt factor flag (K10 ~ K13) Clear to 0 after read out
C3H	0	0	0	IK0	0	– *2			Unused *5
	R				0	– *2			Unused *5
					0	– *2			Unused *5
					IK0	0	Yes	No	Interrupt factor flag (K00 ~ K03) Clear to 0 after read out
C6H	0	0	SIK21	SIK20	0	– *2			Unused *5
	R		R/W		0	– *2			Unused *5
					SIK21	0	Enable	Disable	Interrupt selection register (K21)
					SIK20	0	Enable	Disable	Interrupt selection register (K20)

*1 Initial value at initial reset
*2 Not set in the circuit
*3 Undefined
*4 Inhibit state (output port will be set to "1")
*5 Constantly "0" when being read
*6 Page switching in I/O memory is not necessary

Table 4.4.1(b) Input port control bits (2)

Address *6	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
C7H	SIK13	SIK12	SIK11	SIK10	SIK13	0	Enable	Disable	Interrupt selection register (K13)
	R/W				SIK12	0	Enable	Disable	Interrupt selection register (K12)
					SIK11	0	Enable	Disable	Interrupt selection register (K11)
					SIK10	0	Enable	Disable	Interrupt selection register (K10)
C8H	SIK03	SIK02	SIK01	SIK00	SIK03	0	Enable	Disable	Interrupt selection register (K03)
	R/W				SIK02	0	Enable	Disable	Interrupt selection register (K02)
					SIK01	0	Enable	Disable	Interrupt selection register (K01)
					SIK00	0	Enable	Disable	Interrupt selection register (K00)
C9H	0	K22	K21	K20	0	– *2			Unused *5
	R				K22	– *2	High	Low	Input port (K20 ~ K22)
					K21	– *2	High	Low	
					K20	– *2	High	Low	
CAH	K13	K12	K11	K10	K13	– *2	High	Low	
	R				K12	– *2	High	Low	Input port (K10 ~ K13)
					K11	– *2	High	Low	
					K10	– *2	High	Low	
CBH	K03	K02	K01	K00	K03	– *2	High	Low	
	R				K02	– *2	High	Low	Input port (K00 ~ K03)
					K01	– *2	High	Low	
					K00	– *2	High	Low	

*1 Initial value at initial reset
*2 Not set in the circuit
*3 Undefined
*4 Inhibit state (output port will be set to "1")
*5 Constantly "0" when being read
*6 Page switching in I/O memory is not necessary

Table 4.4.1(c) Input port control bits (3)

Address *6	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
CCH	0	DFK22	DFK21	DFK20	0	– *2			Unused *5
	R	R/W			DFK22	1	↓	↑	
					DFK21	1	↓	↑	Input comparison register (K20 ~ K22)
					DFK20	1	↓	↑	
CDH	DFK13	DFK12	DFK11	DFK10	DFK13	1	↓	↑	
	R/W				DFK12	1	↓	↑	
					DFK11	1	↓	↑	Input comparison register (K10 ~ K13)
					DFK10	1	↓	↑	
CEH	DFK03	DFK02	DFK01	DFK00	DFK03	1	↓	↑	
	R/W				DFK02	1	↓	↑	
					DFK01	1	↓	↑	Input comparison register (K00 ~ K03)
					DFK00	1	↓	↑	
D0H	EIK22	EIK2	EIK1	EIK0	EIK22	0	Enable	Mask	Interrupt mask register (K22)
	R/W				EIK2	0	Enable	Mask	Interrupt mask register (K20, K21)
					EIK1	0	Enable	Mask	Interrupt mask register (K10 ~ K13)
					EIK0	0	Enable	Mask	Interrupt mask register (K00 ~ K03)

*1 Initial value at initial reset
*2 Not set in the circuit
*3 Undefined
*4 Inhibit state (output port will be set to "1")
*5 Constantly "0" when being read
*6 Page switching in I/O memory is not necessary

IK22, IK2, IK1, IK0:
Interrupt factor flags
(C0H•D0, C1H•D0, C2H•D0,
C3H•D0)

These flags indicate the occurrence of input interrupt.

When "1" is read: Interrupt has occurred
When "0" is read: Interrupt has not occurred
Writing: Invalid

The interrupt factor flags IK0, IK1, IK2 and IK22 are associated with K00–K03, K10–K13, K20–K21 and K22, respectively. From the status of these flags, the software can decide whether an input interrupt has occurred.
Reading of interrupt factor flags is available at EI, but be careful in the following cases.
If the interrupt mask register value corresponding to the interrupt factor flags to be read is set to "1", an interrupt request will be generated by the interrupt factor flags set timing, or an interrupt request will not be generated.
These flags are reset when the software reads them.
At initial reset, these flags are set to "0".

SIK21–SIK20:
SIK13–SIK10:
SIK03–SIK00:
Interrupt selection registers
(C6H•D1, D0, C7H, C8H)

Selects the port to be used for the K00–K03, K10–K13 and K20–K21 input interrupts.

When "1" is written: Enable
When "0" is written: Disable
Reading: Valid

Enables the interrupt for the input ports (K00–K03, K10–K13, K20–K21) for which "1" has been written into the interrupt selection register (SIK). The input port set for "0" does not affect the interrupt generation condition.
At initial reset, these registers are set to "0".

K22–K20:
K13–K10:
K03–K00:
Input port data
(C9H•D2–D0, CAH, CBH)

Input data of the input port terminals can be read with these registers.

When "1" is read: High level
When "0" is read: Low level
Writing: Invalid

The reading is "1" when the terminal voltage of the 11 bits of the input ports (K00–K03, K10–K13, K20–K22) goes high (V_{DD}), and "0" when the voltage goes low (V_{SS}).
These bits are dedicated for reading, so writing cannot be done.

DFK22–DFK20:
DFK13–DFK10:
DFK03–DFK00:
Input comparison registers
(CCH•D2–D0, CDH, CEH)

Interrupt conditions for terminals K00–K03, K10–K13 and K20–K22 can be set with these registers.

When "1" is written: Falling edge
When "0" is written: Rising edge
Reading: Valid

The interrupt conditions can be set for the rising or falling edge of input for each of the 11 bits, through the input comparison registers (DFK).
Comparison is done only with the ports that are enabled by the interrupt among input terminals by means of the SIK register.
At initial reset, these registers are set to "0".

EIK22, EIK2, EIK1, EIK0:
Interrupt mask registers
(D0H)

Masking the interrupt of the input port can be selected with these registers.

When "1" is written: Enable
When "0" is written: Mask
Reading: Valid

With these registers, masking of the input port can be selected for each of the four systems (K00–K03, K10–K13, K20–K21, K22).
Writing to the interrupt mask registers can be done only in the DI status (interrupt flag = "0").
At initial reset, these registers are all set to "0".

Programming notes

(1) When input ports are changed from low to high by pull up resistor, the rise of the waveform is delayed on account of the time constant of the pull up resistor and input gate capacitance. Hence, when fetching input ports, set an appropriate wait time.
Particular care needs to be taken of the key scan during key matrix configuration.
Make this waiting time the amount of time or more calculated by the following expression.
$10 \times C \times R$
C: terminal capacitance 5 pF + parasitic capacitance ? pF
R: pull up resistance 300 kΩ

(2) Reading of interrupt factor flags is available at EI, but be careful in the following cases.
If the interrupt mask register value corresponding to the interrupt factor flags to be read is set to "1", an interrupt request will be generated by the interrupt factor flags set timing, or an interrupt request will not be generated.

(3) Write the interrupt mask register (EIK) only in the DI status (interrupt flag = "0"). Writing during EI status (interrupt flag = "1") will cause malfunction.

4.5 Output Ports (R00–R03, R10–R13)

Configuration of output ports

The E0C62T3 has two 4 bits general output ports.
Output specifications of the output ports can be selected individually with the mask option. Two kinds of output specifications are available: complementary output and Nch open drain output.
Further, R10–R13 of the output port to be used as special output port by the software setting.
Figure 4.5.1 shows the configuration of the output port.

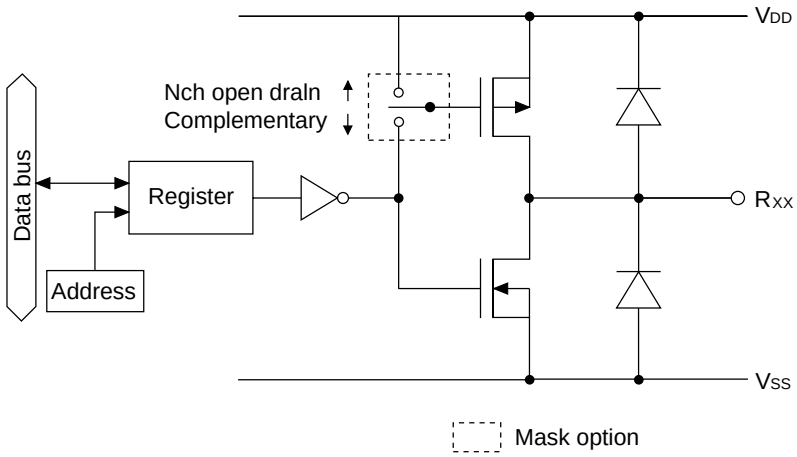


Fig. 4.5.1
Configuration of output port

Mask option

Output specifications of the output ports can be selected with the mask option.
Output specifications for the output ports enable selection of either complementary output or Nch open drain output for each of the eight bits.
However, even when Nch open drain output is selected, voltage exceeding source voltage must not be applied to the output port.

Special output

In addition to the regular DC output, special output can be selected as shown in Table 4.5.1 with the software. Figure 4.5.2 shows the structure of the output ports R10–R13.

Table 4.5.1
Special output

Terminal	Special output	Output selection register
R10	$\overline{BZ}$	BZR10
R11	BZ	BZR11
R12	HDO	CHDO
R13	HFO	CHFO

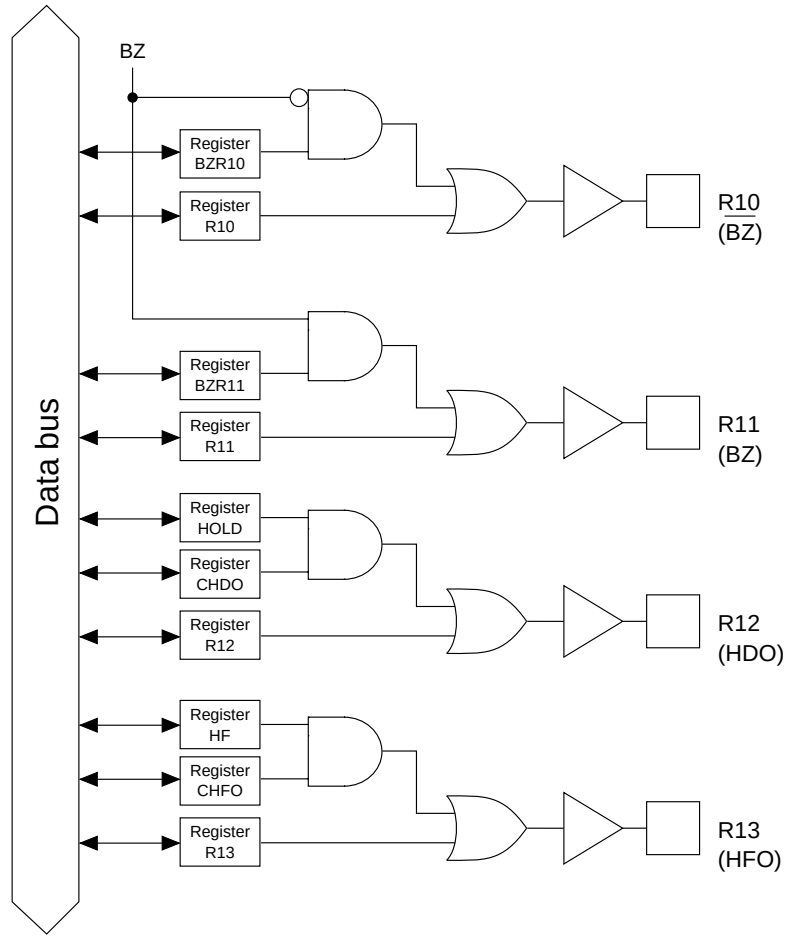
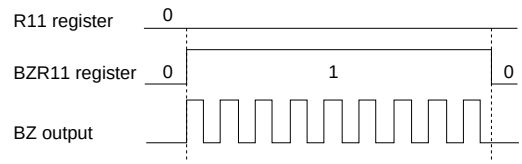


Fig. 4.5.2
Structure of the
output ports R10–R13

• BZ and $\overline{BZ}$ (R11 and R10) BZ and $\overline{BZ}$ are the buzzer signal output for driving the piezoelectric buzzer.
By setting the register BZR11 to "1", R11 terminal is set to BZ (buzzer signal) output port and by setting the register BZR10 to "1", R10 terminal is set to $\overline{BZ}$ (buzzer inverted signal) output port.
When BZR10 and BZR11 are set to "0", R10 terminal and R11 terminal become the regular DC output ports.
When the buzzer output and the buzzer inverted output are selected, ON/OFF of the buzzer outputs can be controlled by the BZR10/R10 and BZR11/R11 registers, respectively.
Figures 4.5.3(a) and (b) show the output waveform of BZ and $\overline{BZ}$.
The buzzer frequency may be selected as 2 kHz or 4 kHz by setting of the BZFQ register.

Note: *The BZ and $\overline{BZ}$ output signals could generate hazards during ON/OFF switching.*



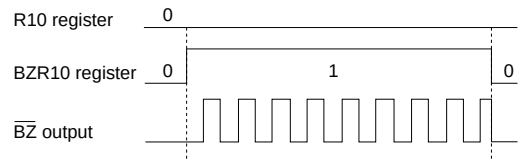
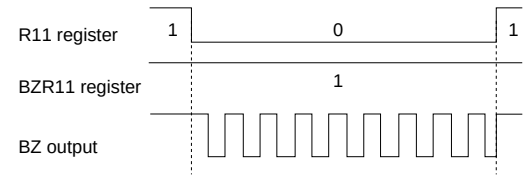


Fig. 4.5.3(a)
Output waveform of BZ and $\overline{BZ}$



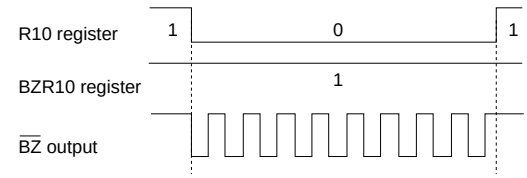


Fig. 4.5.3(b)
Output waveform of BZ and $\overline{BZ}$

• HDO (R12) HDO is hold-line signal output for telephone function.
By setting the register CHDO (EAH•D2) to "1", R12 terminal is set to HDO (Hold-line output) output port. At meanwhile, R12 register (D3H•D2) must be set to "0"; otherwise R12 terminal is set to high level (V_{DD}). When CHDO is set to "0", R12 terminal becomes the regular DC output port.
When the HDO output is selected, the R12 terminal outputs the data which is written in the register HOLD (E3H•D2).
See Section 4.10, "Telephone Function" for detail of HDO.

• HFO (R13) HFO is handfree signal output for telephone function.
By setting the register CHFO (EAH•D3) to "1", R13 terminal is set to HFO (Handfree output) output port. At meantime, R13 register (D3H•D3) must be set to "0"; otherwise R13 terminal is set to high level (V_{DD}). When CHFO is set to "0", R13 terminal becomes the regular DC output port.
When the HFO output is selected, the R13 terminal outputs the data which is written in the register HF (E4H•D3).
See Section 4.10, "Telephone Function" for detail of HFO.

Control of output ports

Tables 4.5.2(a) and (b) list the output ports' control bits and their addresses.

Table 4.5.2(a) Control bits of output ports (1)

Address *6	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
D3H	R13	R12	R11	R10	R13	0	High	Low	Output port (R13)
					HFO		– *4	ON	Handfree output (HFO)
	HFO	HDO	BZ	$\overline{BZ}$	R12	0	High	Low	Output port (R12)
					HDO		– *4	ON	Hold-line output (HDO)
	R/W				R11	0	High	Low	Output port (R11)
					BZ		– *4	ON	Buzzer output (BZ)
					R10	0	High	Low	Output port (R10)
					$\overline{BZ}$		– *4	ON	Buzzer inverted output ($\overline{BZ}$)
D4H	R03	R02	R01	R00	R03	0	High	Low	Output port (R00 ~ R03)
	R/W				R02	0	High	Low	
					R01	0	High	Low	
					R00	0	High	Low	
DDH	BZR11	BZR10	0	BZFQ	BZR11	0	Buzzer	DC	R11 port output selection
	R/W		R	R/W	BZR10	0	Buzzer (inverted)	DC	R10 port output selection
					0	– *2			Unused *5
					BZFQ	0	2 kHz	4 kHz	Buzzer frequency selection
E3H	0	HOLD	PAUSE	FLASH	0	– *2			Unused *5
	R	R/W	W		HOLD	0	On	Off	Hold – line function
					PAUSE	0	Yes	No	Pause function *5
					FLASH	0	Yes	No	Flash function *5
E4H	HF	0	0	0	HF	0	Yes	No	Hand free
	R/W	R			0	– *2			Unused *5
					0	– *2			Unused *5
					0	– *2			Unused *5

*1 Initial value at initial reset
*2 Not set in the circuit
*3 Undefined
*4 Inhibit state (output port will be set to "1")
*5 Constantly "0" when being read
*6 Page switching in I/O memory is not necessary

Table 4.5.2(b) Control bits of output ports (2)

Address *6	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
EAH	CHFO	CHDO	0	0	CHFO	0	Handfree output	DC	R13 output selection (R13 data register has to be "0")
	R/W		R		CHDO	0	Hold output	DC	R12 output selection (R12 data register has to be "0")
					0	– *2			Unused *5
					0	– *2			Unused *5

*1 Initial value at initial reset
*2 Not set in the circuit
*3 Undefined
*4 Inhibit state (output port will be set to "1")
*5 Constantly "0" when being read
*6 Page switching in I/O memory is not necessary

R10–R13 (when DC output): Output port data (D3H)

Sets the output data for the output ports.

When "1" is written: High output
When "0" is written: Low output
Reading: Valid

The output port terminals output the data written in the corresponding registers (R10–R13) without changing it. When "1" is written in the register, the output port terminal goes high (V_{DD}), and when "0" is written, the output port terminal goes low (V_{SS}). At initial reset, R10–R13 are set to "0".

R13 (when HFO is selected): Special output port data (D3H•D3)

Controls the HFO (Handfree Output) output and acts as HFO output terminal.

When "1" is written: High level (DC) output
When "0" is written: Handfree signal output
Reading: Valid

R13 terminal can be used as HFO signal output terminal, by writing "1" into register CHFO (EAH•D3), "0" into register R13 (D3H•D3).
When HFO output is selected, the R13 terminal outputs the data which is written in the register HF (E4H•D3).
At initial reset, this register is set to "0".

R12 (when HDO is selected): Special output port data (D3H•D2)

Controls the HDO (Hold-Line Output) output and acts as HDO output terminal.

When "1" is written: High level (DC) output
When "0" is written: Hold-line signal output
Reading: Valid

R12 terminal can be used as HDO signal output terminal, by writing "1" into register CHDO (EAH•D2), "0" into register R12 (D3H•D2).
When HDO output is selected, the R12 terminal outputs the data which is written in the register HOLD (E3H•D2).
At initial reset, this register is set to "0".

R10, R11 (when $\overline{BZ}$ and BZ output is selected): Special output port data (D3H•D0, D1)

These bits control the output of the buzzer signals (BZ, $\overline{BZ}$).

When "1" is written: High level (DC) output
When "0" is written: Buzzer signals output
Reading: Valid

BZ (buzzer signal) output is controlled by writing data to BZR11/R11, and $\overline{BZ}$ (buzzer inverted signal) output is controlled by writing data to BZR10/R10.
At initial reset, R10 and R11 are set to "0".

R00–R03: Output port data (D4H)

Sets the output data for the output ports.

When "1" is written: High output
When "0" is written: Low output
Reading: Valid

The output port terminals output the data written in the corresponding registers (R00–R03) without changing it. When "1" is written in the register, the output port terminal goes high (V_{DD}), and when "0" is written, the output port terminal goes low (V_{SS}).
At initial reset, R00–R03 are set to "0".

BZR10, BZR11: R10, R11 output selection register (DDH•D2, D3)

Selects the output type for the R10 and R11 terminals.

When "1" is written: Buzzer signal output
When "0" is written: DC output
Reading: Valid

By setting the register BZR11 to "1", R11 is set to BZ (buzzer signal) output port and by setting the register BZR10 to "1", R10 is set to $\overline{BZ}$ (buzzer inverted signal) output port. When BZR10 and BZR11 are set to "0", R10 and R11 become the regular DC output ports.
When the buzzer output and the buzzer inverted output are selected, ON/OFF of the buzzer outputs can be controlled by the R10 and R11 registers, respectively.
At initial reset, these register are set to "0".

BZFQ:
Buzzer frequency selection register
(DDH•D0)

Selects the frequency of the buzzer signal.

When "1" is written: 2 kHz
When "0" is written: 4 kHz
Reading: Valid

When "1" is written to register BZFQ, the frequency of the buzzer signal is set in 2 kHz, and in 4 kHz when "0" is written.
At initial reset, this register is set to "0".

HOLD:
Hold-line function
(E3H•D2)

Executes the hold function ON/OFF and outputs data from register HOLD to R12 terminal.

When "1" is written: ON (High level output on R12 terminal)
When "0" is written: OFF (Low level output on R12 terminal)
Reading: Valid

HDO (Hold-Line Output) is output terminal for hold-line function.
When HDO output is selected, the R12 terminal outputs the data which is written in the register HOLD (E3H•D2).
When R12 terminal is used as HDO output port, the register CHDO (EAH•D2) must be written "1" and register R12 (D3H•D2) must be written "0".
When HOLD (E3H•D2) register is turned ON, $\overline{\text{TMUTE}}$ terminal goes low level (V_{SS}) and HDO (R12) terminal goes high level (V_{DD}).
When HOLD register is turned OFF, $\overline{\text{TMUTE}}$ terminal goes high level (V_{DD}) and HDO (R12) terminal goes low level (V_{SS}).
Hold-line function is a toggle selection and it does not generate interrupt.
At initial reset, this register is set to "0".

HF:
Handfree
(E4H•D3)

Executes the handfree function ON/OFF and outputs data from register HF to HFO (R13) terminal.

When "1" is written: ON (High level output on R13 terminal)
When "0" is written: OFF (Low level output on R13 terminal)
Reading: Valid

HFO (HandFree Output) is output terminal for handfree function.
When HFO output is selected, the R13 terminal outputs the data which is written in the register HF (E4H•D3).
When R13 terminal is used as HFO output port, the register CHFO (EAH•D3) must be written "1" and register R13 (D3H•D3) must be written "0".
Handfree function is a toggle selection and it does not generate interrupt.
At initial reset, this register is set to "0".

CHFO:
R13 output selection register
(EAH•D3)

Selects the output type for the R13 terminal.

When "1" is written: Handfree signal output
When "0" is written: DC output
Reading: Valid

By setting the register CHFO to "1", R13 is set to HFO (HandFree Output) output port. When CHFO is set to "0", R13 becomes the regular DC output port.
See Section 4.10, "Telephone Function".
At initial reset, this register is set to "0".

CHDO:
R12 output selection register
(EAH•D2)

Selects the output type for the R12 terminal.

When "1" is written: Hold-line signal output
When "0" is written: DC output
Reading: Valid

By setting the register CHDO to "1", R12 is set to HDO (Hold-Line Output) output port. When CHDO is set to "0", R12 becomes the regular DC output port.
See Section 4.10, "Telephone Function".
At initial reset, this register is set to "0".

Programming notes

(1) When output ports (R10–R13) are selected as special output, the corresponding output port data (R10–R13) must be set to "0".

(2) When BZ and $\overline{BZ}$ are selected, a hazard may be observed in the output waveform when the data of control registers (BZR11 and BZR10) change.

4.6 I/O Ports (P00–P03)

Configuration of I/O port

The E0C62T3 has a 4 bits general-purpose I/O port.
Figure 4.6.1 shows the configuration of I/O port.
The each bit of the I/O port P00–P03 can be set to either input mode or output mode, individually. Modes can be set by writing data to the I/O control register.
During input mode, the pull up resistors can be controlled through the software by writing data into the pull up control register.

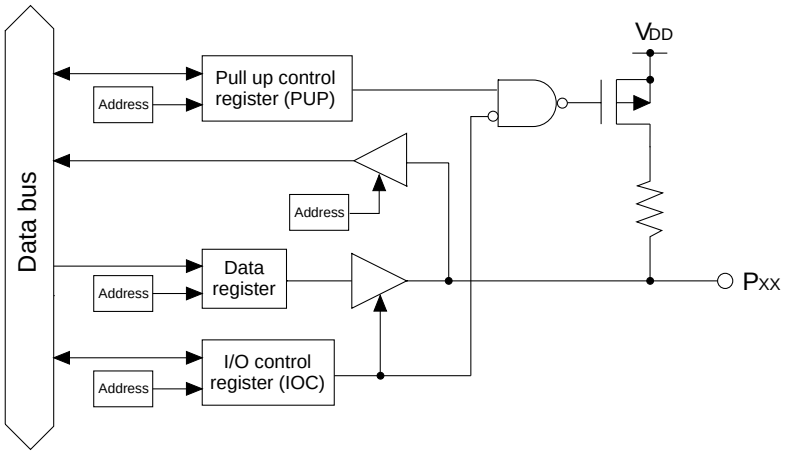


Fig. 4.6.1
Configuration of I/O port

I/O control registers and input/output mode

Input or output mode can be set for the each bit of I/O port P00–P03 by writing data into the corresponding I/O control register IOC0, IOC1, IOC2 and IOC3.

To set the input mode, "0" is written to the I/O control register. When an I/O port is set to input mode, it becomes high impedance status and works as an input port.
However, when the pull up explained in the following section has been set by software, the input line is pulled up only during this input mode.

The output mode is set when "1" is written to the I/O control register. When an I/O port set to output mode works as an output port, it outputs a high level (V_{DD}) when the port output data is "1", and a low level (V_{SS}) when the port output data is "0".

If perform the read out in each mode; when output mode, the register value is read out, and when input mode, the port value is read out.

At initial reset, the I/O control registers are set to "0", and the I/O port enters the input mode.

Pull up during input mode

A pull up resistor that operates during the input mode is built into the I/O port of the E0C62T3. Software can set the use or non-use of this pull up. The pull up resistor becomes effective by writing "1" into the pull up control registers PUP0, PUP1, PUP2 and PUP3 that correspond to each bit of P00–P03, and the input line is pulled up during the input mode. When "0" has been written, no pull up is done.
At initial reset, the pull up control registers are set to "0".

Mask option

Output specifications during the output mode (IOC = "1") can be selected with the mask option.
Output specifications for the I/O port (P00–P03) enable selection of either complementary output or Nch open drain output for each of the 4 bits.
However, even when Nch open drain output is selected, voltage exceeding source voltage must not be applied to the output port.

Control of I/O port

Table 4.6.1 lists the I/O port's control bits and their addresses.

Table 4.6.1 Control bits of I/O port

Address *6	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
D5H	IOC3	IOC2	IOC1	IOC0	IOC3	0	Output	Input	I/O control register
	R/W				IOC2	0	Output	Input	
					IOC1	0	Output	Input	
					IOC0	0	Output	Input	
D6H	PUP3	PUP2	PUP1	PUP0	PUP3	0	ON	OFF	Pull up control register
	R/W				PUP2	0	ON	OFF	
					PUP1	0	ON	OFF	
					PUP0	0	ON	OFF	
D7H	P03	P02	P01	P00	P03	1	High	Low	I/O port
	R/W				P02	1	High	Low	
					P01	1	High	Low	
					P00	1	High	Low	

*1 Initial value at initial reset
*2 Not set in the circuit
*3 Undefined
*4 Inhibit state (output port will be set to "1")
*5 Constantly "0" when being read
*6 Page switching in I/O memory is not necessary

IOC0, IOC1, IOC2, IOC3: I/O control register (D5H)

The input and output modes of the I/O port can be set with these registers.

When "1" is written: Output mode
When "0" is written: Input mode
Reading: Valid

The input and output modes of the I/O port is set in each bit. IOC0, IOC1, IOC2 and IOC3 set the mode for P00, P01, P02 and P03, respectively.
Writing "1" to the I/O control register makes the corresponding bit of I/O port enter the output mode, and writing "0" induces the input mode.
At initial reset, these registers are set to "0", so the I/O port is in the input mode.

PUP0, PUP1, PUP2, PUP3: Pull up control register (D6H)

The pull up during the input mode can be set with these registers.

When "1" is written: Pull up ON
When "0" is written: Pull up OFF
Reading: Valid

The built-in pull up resistor which is turned ON during input mode is set to enable in each bit. PUP0, PUP1, PUP2 and PUP3 set the pull up for P00, P01, P02 and P03, respectively.
By writing "1" to the pull up control register, the corresponding bit of I/O port is pulled up (during input mode), while writing "0" turns the pull up function OFF.
At initial reset, these registers are set to "0", so the pull up function is set to OFF.

P00–P03: I/O port data (D7H)

I/O port data can be read and output data can be set through this port.

• ***When writing data***

When "1" is written: High level
When "0" is written: Low level

When an I/O port is set to the output mode, the written data is output unchanged from the I/O port terminal. When "1" is written as the port data, the port terminal goes high (V_{DD}), and when "0" is written, the level goes low (V_{SS}).
Port data can be written also in the input mode.

• ***When reading data out***

When "1" is read: High level
When "0" is read: Low level

The terminal voltage level of the I/O port is read out. When the I/O port is in the input mode the voltage level being input to the port terminal can be read out; in the output mode the register value can be read. When the terminal voltage is high (V_{DD}) the port data that can be read is "1", and when the terminal voltage is low (V_{SS}) the data is "0".
When PUP register is set to "1", the built-in pull up resistor goes ON during input mode, so that the I/O port terminal is pulled up. Internal pull up resistors are only ON during input mode, but the gate floating has not occur even during output mode.

Programming note

When in the input mode, I/O port is changed from low to high by pull up resistor, the rise of the waveform is delayed on account of the time constant of the pull up resistor and input gate capacitance. Hence, when fetching input ports, set an appropriate wait time.
Particular care needs to be taken of the key scan during key matrix configuration.
Make this waiting time the amount of time or more calculated by the following expression.
10 x C x R
C: terminal capacitance 5 pF + parasitic capacitance ? pF
R: pull up resistance 300 kΩ

4.7 LCD Driver (COM0–COM3, SEG0–SEG31)

Configuration of LCD driver

The E0C62T3 has four common terminals (COM0–COM3) and 32 segment terminals (SEG0–SEG31), so that it can drive an LCD with a maximum of 128 (32 × 4) segments.
The power for driving the LCD is generated by the CPU internal circuit so that there is no need to apply power especially from outside.
The driving method is 1/4 duty dynamic drive depending on the four types of potential, V_{SS}, V_{C1}, V_{C2} and V_{C3}. In addition to the 1/4 duty, 1/3, 1/2 and 1/1 drive duty can be selected through the software. The frame frequency is 32 Hz for 1/4, 1/2 and 1/1 duty, and 42.7 Hz for 1/3 duty (f_{OSC1} = 32,768 Hz).
LCD display ON/OFF may be controlled by the software.
Figures 4.7.1–4.7.3 show the drive waveform for 1/4 duty, 1/3 duty and 1/2 duty.

Note: *"f_{OSC1}" indicates the oscillation frequency of the OSC1 oscillation circuit.*

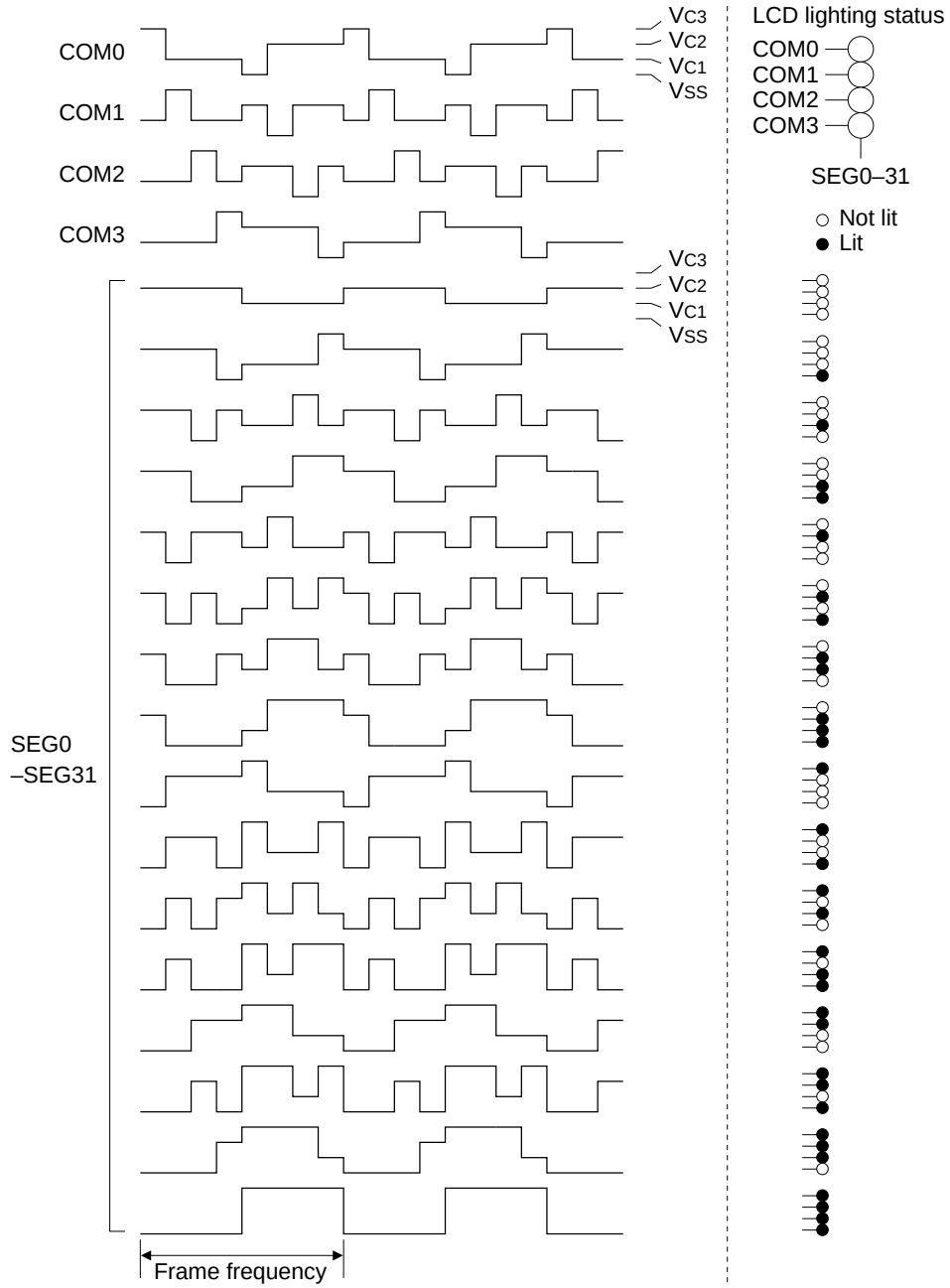


Fig. 4.7.1
Drive waveform
for 1/4 duty

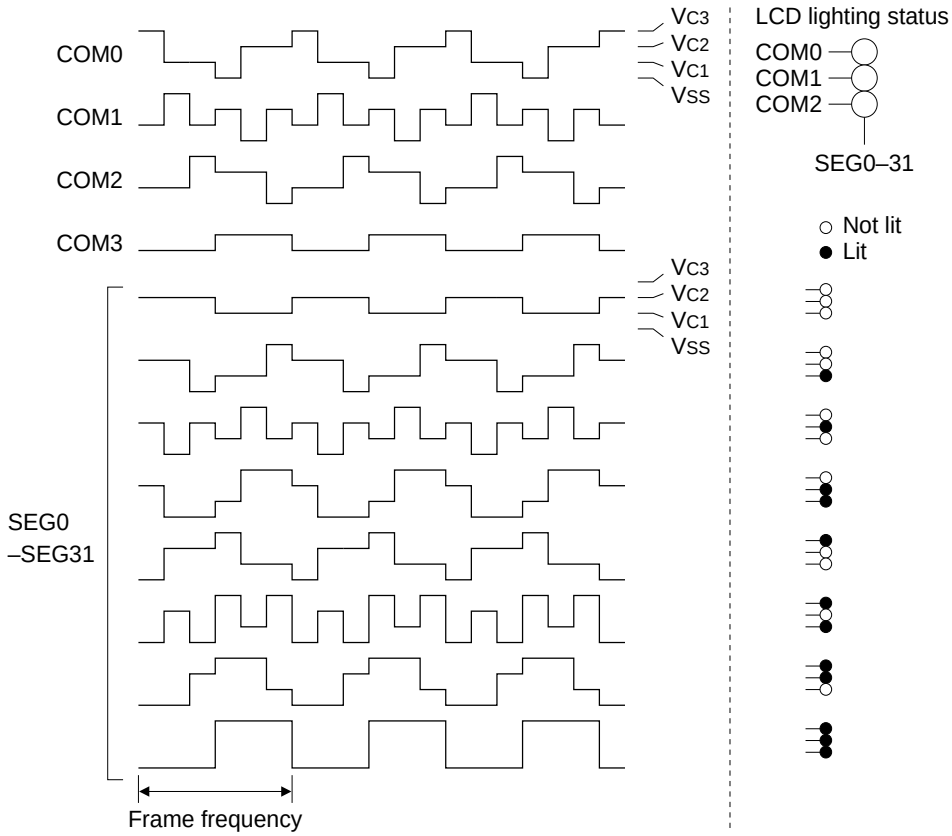


Fig. 4.7.2
Drive waveform
for 1/3 duty

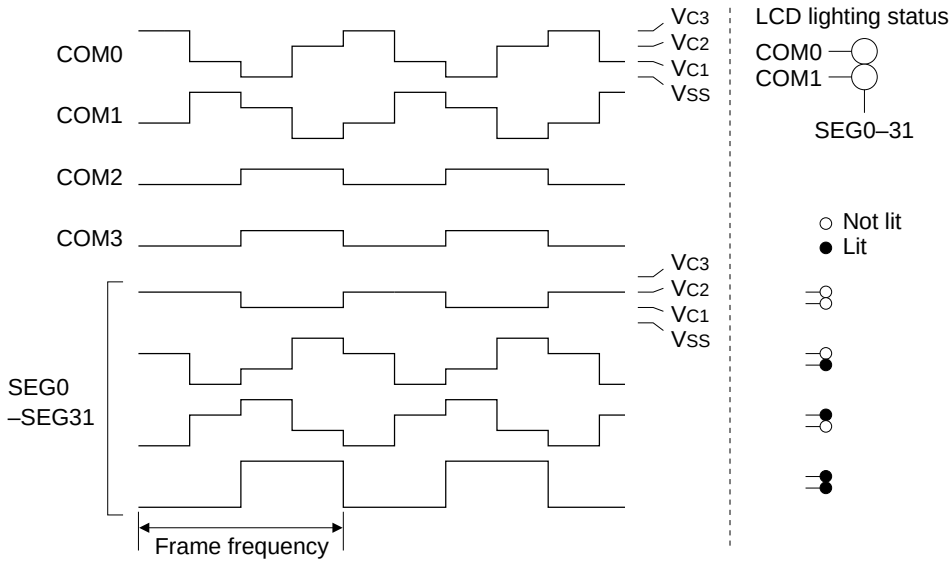


Fig. 4.7.3
Drive waveform
for 1/2 duty

LCD display ON/OFF control and duty switching

(1) Display ON/OFF control

In the E0C62T3, ON/OFF of the LCD display can be controlled by LCDON register.
At initial reset, LCDON is set to "0", and the LCD display is set to the OFF status. In this time, the COM terminal and the SEG terminal goes to V_{C1} level.
To set the LCD display ON, write "1" to register LCDON.

(2) Switching of drive duty

By settings of registers LDTY0 and LDTY1, the LCD drive duty can be selected from among 4 types, 1/4, 1/3, 1/2, 1/1 duty. Table 4.7.1 shows the LCD drive duty setting.

Table 4.7.1
LCD drive duty setting

LDTY1	LDTY0	Duty	Terminals used in common	Maximum number of segments	Frame frequency
0	0	1/4	COM0–COM3	128 (32 × 4)	f_{OSC1}/1,024 (32 Hz)
0	1	1/3	COM0–COM2	96 (32 × 3)	f_{OSC1}/768 (42.7 Hz)
1	0	1/2	COM0, COM1	64 (32 × 2)	f_{OSC1}/1,024 (32 Hz)
1	1	1/1	COM0	32 (32 × 1)	f_{OSC1}/1,024 (32 Hz)

* In case of f_{OSC1} = 32,768 Hz

Basically you should select the drive duty with the smallest drive segment number (for example, 1/3 duty for 80 segments and 1/2 duty for 40 segments) from among the drive duties permitting driving of the segment number of the LCD panel.

(3) Cadence adjustment of oscillation frequency

By using the 1/1 duty drive waveform, it enables easy adjustment (cadence adjustment) of the oscillation frequency of the OSC1 oscillation circuit (crystal oscillation circuit).

Note: *For cadence adjustment, set the segment data so that all the LCDs light.*

Figure 4.7.4 shows the drive waveform for 1/1 duty.

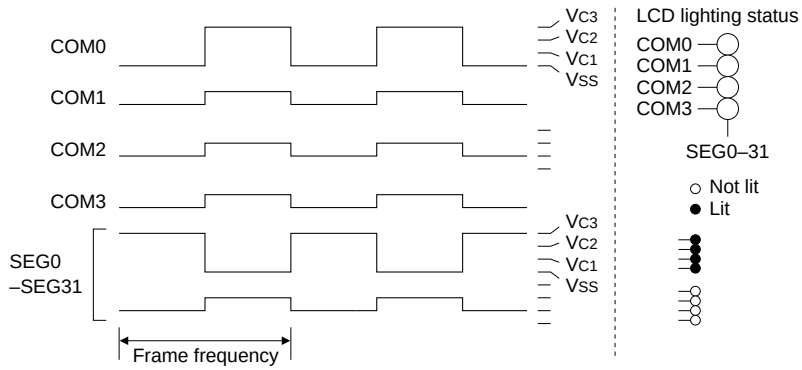


Fig. 4.7.4
Drive waveform for 1/1 duty

Mask option (segment allocation)

(1) Segment allocation

The LCD driver has a segment decoder built-in, and the data bit of the optional address in the display memory area (80H–AFH) can be allocated to the optional segment. This makes design easy by increasing the degree of freedom with which the liquid crystal panel can be designed.
The allocated segment displays when the bit for the display memory is set to "1", and goes out when bit is set to "0".

Figure 4.7.5 shows an example of the relationship between the LCD segments (on the panel) and the display memory for the case of 1/3 duty.

Address	Data			
	D3	D2	D1	D0
9AH	d	c	b	a
9BH	p	g	f	e
9CH	d'	c'	b'	a'
9DH	p'	g'	f'	e'

Display memory allocation

	Common 0	Common 1	Common 2
SEG10	9A, D0 (a)	9B, D1 (f)	9B, D0 (e)
SEG11	9A, D1 (b)	9B, D2 (g)	9A, D3 (d)
SEG12	9D, D1 (f')	9A, D2 (c)	9B, D3 (p)

Pin address allocation

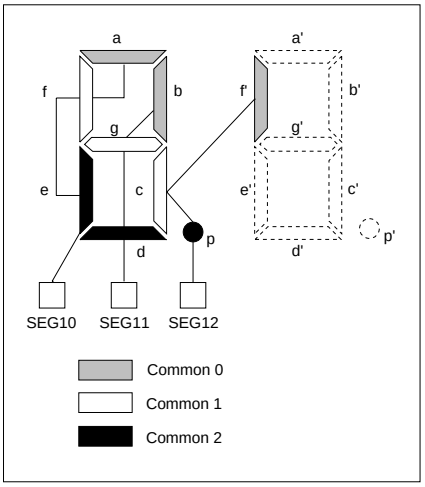


Fig. 4.7.5
Segment allocation

(2) Output specification

① The segment terminals (SEG0–SEG31) are selected with the mask option in pairs for either segment signal output or DC output (V_{DD} and V_{SS} binary output).
When DC output is selected, the data corresponding to COM0 of each segment terminal is output.

② When DC output is selected, either complementary output or Nch open drain output can be selected for each terminal with the mask option.

Note: *The terminal pairs are the combination of SEG2*n and SEG2*n + 1 (where n is an integer from 0 to 15).*

Control of LCD driver

Table 4.7.2 shows the LCD driver's control bits and their addresses. Figure 4.7.6 shows the display memory map.

Table 4.7.2 LCD driver control bits

Address *6	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
DEH	LDTY1	LDTY0	0	LCDON	LDTY1	0			LCD drive duty selection 0 : 1/4, 1 : 1/3, 2 : 1/2, 3 : 1/1
	R/W		R	R/W	LDTY0	0			
					0	– *2			Unused *5
					LCDON	0	ON	OFF	LCD display control (LCD display all off)

*1 Initial value at initial reset
*2 Not set in the circuit
*3 Undefined
*4 Inhibit state (output port will be set to "1")
*5 Constantly "0" when being read
*6 Page switching in I/O memory is not necessary

Address Page *1	Low / High	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0–4	8	Display memory area (80H–AFH) 48 words x 4 bits (Write only)															
	9																
	A																

*1 Page switching in display memory is not necessary

Fig. 4.7.6 Display memory map

LCDON: Display control (DEH•D0)

Controls the LCD display

When "1" is written: Display ON
When "0" is written: Display OFF
Reading: Valid

By writing "1" to LCDON, the LCD display goes ON, and goes OFF when "0" is written. The LCD display OFF setting does not affect the contents of the display memory.
At initial reset, this register is set to "0".

LDTY1, LDTY0: LCD drive duty selection (DEH•D3, D2)

Sets the LCD drive duty as shown in Table 4.7.3.

Table 4.7.3 LCD drive duty setting

LDTY1	LDTY0	Duty	Terminals used in common	Maximum number of segments	Frame frequency
0	0	1/4	COM0–COM3	128 (32 × 4)	fOSC1/1,024 (32 Hz)
0	1	1/3	COM0–COM2	96 (32 × 3)	fOSC1/768 (42.7 Hz)
1	0	1/2	COM0, COM1	64 (32 × 2)	fOSC1/1,024 (32 Hz)
1	1	1/1	COM0	32 (32 × 1)	fOSC1/1,024 (32 Hz)

* In case of fOSC1 = 32,768 Hz

At initial reset, these registers are set to "0".

Display memory (80H–AFH)

The LCD segments are lit or turned off depending on this data.

When "1" is written: Lit
When "0" is written: Not lit
Reading: Invalid

By writing data into the display memory allocated to the LCD segment (on the panel), the segment can be lit or put out.
At initial reset, the contents of the display memory for COM0 is set to "1", and COM1–COM3 are undefined. Accordingly, when DC output is selected, the output level at initial reset goes high (VDD).

Programming notes

(1) The contents of the display memory are undefined until the area is initialized (through, for instance, memory clear processing by the CPU). Initialize the display memory by executing initial processing.

(2) Since the display memory area is write-only, display data cannot be rewritten by arithmetic operations (such as AND, OR, ADD, SUB).

4.8 Clock Timer

Configuration of clock timer

The E0C62T3 has a built-in clock timer as the source oscillator for OSC1 (crystal oscillator). The clock timer is configured of a 8-bit binary counter that serves as the input clock, a 256 Hz signal output by the OSC1 oscillation circuit. Timer data (128–16 Hz and 8–1 Hz) can be read out by the software.
Figure 4.8.1 is the block diagram for the clock timer.

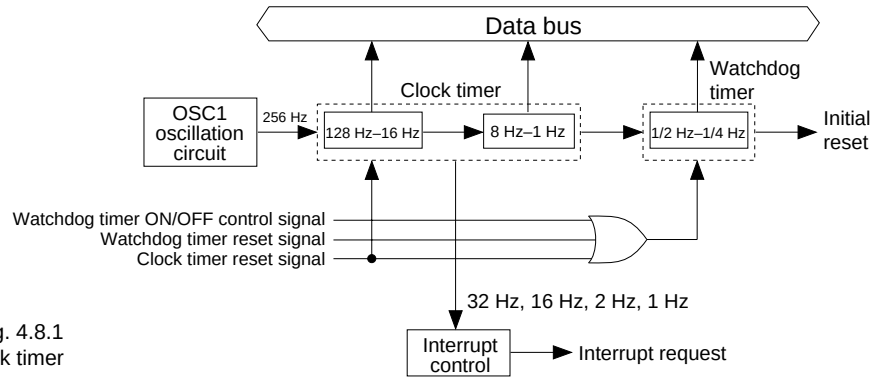


Fig. 4.8.1
Block diagram for the clock timer

Ordinarily, this clock timer is used for all types of timing functions such as clocks.

Data reading and hold function

The 8 bits timer data are allocated to the address DAH and DBH.

DAH	D0: TM0 (128 Hz)	D1: TM1 (64 Hz)	D2: TM2 (32 Hz)	D3: TM3 (16 Hz)
DBH	D0: TM4 (8 Hz)	D1: TM5 (4 Hz)	D2: TM6 (2 Hz)	D3: TM7 (1 Hz)

Since the clock timer data has been allocated to two addresses, a carry is generated from the low-order data within the count (TM0–TM3: 128–16 Hz) to the high-order data (TM4–TM7: 8–1 Hz). When this carry is generated between the reading of the low-order data and the high-order data, a content combining the two does not become the correct value (the low-order data is read as FFH and the high-order data becomes the value that is counted up 1 from that point).
The high-order data hold function in the E0C62T3 is designed to operate to avoid this. This function temporarily stops the counting up of the high-order data (by carry from the low-order data) at the point where the low-order data has been read and consequently the time during which the high-order data is held is the shorter of the two indicated here following.

1. Period until it reads the high-order data.
2. 0.48–1.5 msec (varies due to the timing of the reading)

Note: *When the high-order data has previously been read, since the low-order data is not held, you should be sure to first read from the low-order data.*

Interrupt function

The clock timer can cause interrupts at the falling edge of 32 Hz, 16 Hz, 2 Hz and 1 Hz signals. Software can set whether to mask any of these frequencies.
Figure 4.8.2 is the timing chart of the clock timer.

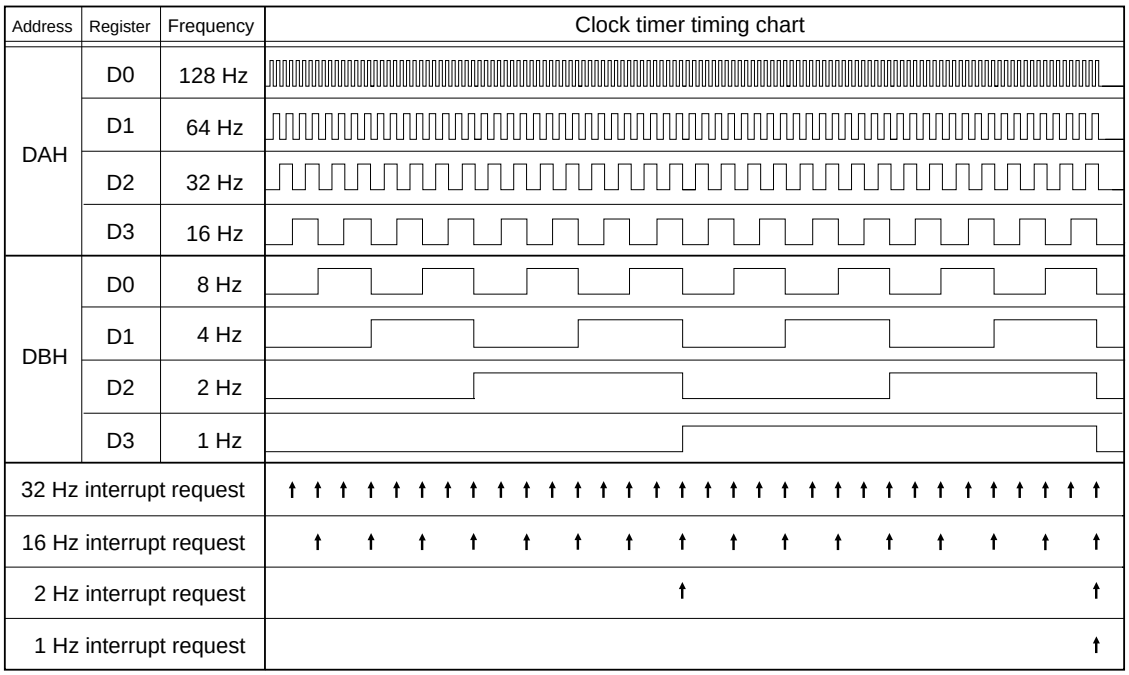


Fig. 4.8.2 Timing chart of clock timer

As shown in Figure 4.8.2, interrupt is generated at the falling edge of the frequencies (32 Hz, 16 Hz, 2 Hz, 1 Hz). At this time, the corresponding interrupt factor flag (IT32, IT16, IT2, IT1) is set to "1". Selection of whether to mask the separate interrupts can be made with the interrupt mask registers (EIT32, EIT16, EIT2, EIT1). However, regardless of the interrupt mask register setting, the interrupt factor flag is set to "1" at the falling edge of the corresponding signal.

Note: • *Reading of interrupt factor flags is available at EI, but be careful in the following cases.*
If the interrupt mask register value corresponding to the interrupt factor flags to be read is set to "1", an interrupt request will be generated by the interrupt factor flags set timing, or an interrupt request will not be generated. Be very careful when interrupt factor flags are in the same address.

• *Write the interrupt mask register only in the DI status (interrupt flag = "0"). Writing during EI status (interrupt flag = "1") will cause malfunction.*

Control of clock timer

Table 4.8.1 shows the clock timer control bits and their addresses.

Table 4.8.1 Control bits of clock timer

Address *6	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
C4H	IT1	IT2	IT16	IT32	IT1	0	Yes	No	Interrupt factor flag (clock timer 1 Hz) Clear to 0 after read out
	R				IT2	0	Yes	No	Interrupt factor flag (clock timer 2 Hz) Clear to 0 after read out
					IT16	0	Yes	No	Interrupt factor flag (clock timer 16 Hz) Clear to 0 after read out
					IT32	0	Yes	No	Interrupt factor flag (clock timer 32 Hz) Clear to 0 after read out
D1H	EIT1	EIT2	EIT16	EIT32	EIT1	0	Enable	Mask	Interrupt mask register (clcok timer 1 Hz)
	R/W				EIT2	0	Enable	Mask	Interrupt mask register (clock timer 2 Hz)
					EIT16	0	Enable	Mask	Interrupt mask register (clock timer 16 Hz)
					EIT32	0	Enable	Mask	Interrupt mask register (clock timer 32 Hz)
D9H	0	0	0	TMRST	0	– *2			Unused *5
	R			W	0	– *2			Unused *5
					0	– *2			Unused *5
					TMRST	– *2	Reset	Invalid	Clock timer reset *5
DAH	TM3	TM2	TM1	TM0	TM3	– *3			Clock timer data (low-order) 16 Hz
	R				TM2	– *3			Clock timer data (low-order) 32 Hz
					TM1	– *3			Clock timer data (low-order) 64 Hz
					TM0	– *3			Clock timer data (low-order) 128 Hz
DBH	TM7	TM6	TM5	TM4	TM7	– *3			Clock timer data (high-order) 1 Hz
	R				TM6	– *3			Clock timer data (high-order) 2 Hz
					TM5	– *3			Clock timer data (high-order) 4 Hz
					TM4	– *3			Clock timer data (high-order) 8 Hz

*1 Initial value at initial reset
*2 Not set in the circuit
*3 Undefined
*4 Inhibit state (output port will be set to "1")
*5 Constantly "0" when being read
*6 Page switching in I/O memory is not necessary

IT32, IT16, IT2, IT1: Interrupt factor flag (C4H)

These flags indicate the status of the clock timer interrupt.

When "1" is read: Interrupt has occurred
When "0" is read: Interrupt has not occurred
Writing: Invalid

The interrupt factor flags (IT32, IT16, IT2, IT1) correspond to the clock timer interrupts of the respective frequencies (32 Hz, 16 Hz, 2 Hz, 1 Hz). The software can judge from these flags whether there is a clock timer interrupt. However, even if the interrupt is masked, the flags are set to "1" at the falling edge of the signal.
These flags can be reset through being read out by the software.
Reading of interrupt factor flags is available at EI, but be careful in the following cases.
If the interrupt mask register value corresponding to the interrupt factor flags to be read is set to "1", an interrupt request will be generated by the interrupt factor flags set timing, or an interrupt request will not be generated. Be very careful when interrupt factor flags are in the same address.
At initial reset, these flags are set to "0".

EIT32, EIT16, EIT2, EIT1: Interrupt mask register (D1H)

These registers are used to select whether to mask the clock timer interrupt.

When "1" is written: Enabled
When "0" is written: Masked
Reading: Valid

The interrupt mask registers (EIT32, EIT16, EIT2, EIT1) are used to select whether to mask the interrupt to the separate frequencies (32 Hz, 16 Hz, 2 Hz, 1 Hz).
Writing to the interrupt mask registers can be done only in the DI status (interrupt flag = "0").
At initial reset, these registers are all set to "0".

TMRST: Clock timer reset (D9H•D0)

This bit resets the clock timer.

When "1" is written: Clock timer reset
When "0" is written: No operation
Reading: Always "0"

The clock timer is reset by writing "1" to TMRST. The clock timer starts immediately after this. No operation results when "0" is written to TMRST.
TMRST also resets the watchdog timer.
This bit is write-only, and so is always "0" at reading.

TM0–TM7: Timer data (DAH, DBH)

The 128 Hz–1 Hz timer data of the clock timer can be read out with these registers. These eight bits are read only, and writing operations are invalid.
At initial reset, the timer data is initialized to "00H".

Programming notes

(1) Be sure to data reading in the order of low-order data (TM0–TM3) then high-order data (TM4–TM7).

(2) When the clock timer has been reset, the interrupt factor flag (IT) may sometimes be set to "1". Consequently, perform flag reading (reset the flag) as necessary at reset.

(3) When the clock timer has been reset, the watchdog timer is also reset. (If watchdog timer is ON, WDON = "1")

(4) Reading of interrupt factor flags is available at EI, but be careful in the following cases.
If the interrupt mask register value corresponding to the interrupt factor flags to be read is set to "1", an interrupt request will be generated by the interrupt factor flags set timing, or an interrupt request will not be generated. Be very careful when interrupt factor flags are in the same address.

(5) Write the interrupt mask register (EIT) only in the DI status (interrupt flag = "0"). Writing during EI status (interrupt flag = "1") will cause malfunction.

4.9 SVD (Supply Voltage Detection) Circuit

Configuration of SVD circuit

The E0C62T3 has a built-in SVD (supply voltage detection) circuit, so that the software can find when the source voltage lowers. Turning the SVD circuit ON/OFF can be controlled through the software.
Figure 4.9.1 shows the configuration of the SVD circuit.

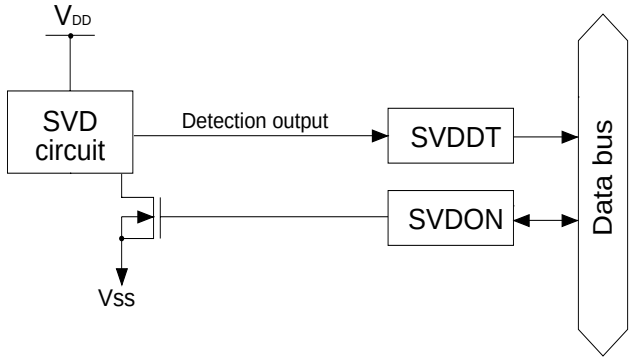


Fig. 4.9.1
Configuration of the SVD circuit

SVD operation

The SVD circuit compares the detecting voltage level of the SVD circuit (1.8 V) with the supply voltage (VDD–VSS) and sets its results into the SVDDT latch. By reading the data of this SVDDT latch, it can be determined by means of software whether the supply voltage is normal or has dropped.

When SVDON is set to "1", source voltage detection by the SVD circuit is executed. As soon as SVDON is reset to "0", the result is loaded to in the SVDDT register and SVD circuit goes OFF.
To obtain a stable SVD detection result, the SVD circuit must be on for at least l00 µsec. So, to obtain the SVD detection result, follow the programming sequence below.

① Set SVDON to "1"
② Maintain for 100 µsec minimum
③ Set SVDON to "0"
④ Read SVDDT

However, when fOSC1 is selected for CPU system clock, the instruction cycles are long enough, so there is no need to worry about maintaining 100 µsec for SVDON = "1" in the software.
When SVD is on, the IC draws a large current, so keep SVD off unless it is.

Control of SVD circuit

Table 4.9.1 shows the control bits and their addresses for the SVD circuit.

Table 4.9.1 Control bits for SVD circuit

Address *6	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
DFH	0	0	SVDDT	SVDON	0	– *2			Unused *5
	R			R/W	0	– *2			Unused *5
					SVDDT	0	Supply voltage Low	Supply voltage Normal	Supply votage detector data
					SVDON	0	ON	OFF	SVD circuit ON/OFF

*1 Initial value at initial reset
*2 Not set in the circuit
*3 Undefined
*4 Inhibit state (output port will be set to "1")
*5 Constantly "0" when being read
*6 Page switching in I/O memory is not necessary

SVDON: SVD ON/OFF (DFH•D0)

Turns the SVD circuit ON and OFF.

When "1" is written: SVD circuit ON
When "0" is written: SVD circuit OFF
Reading: Valid

When SVDON is set to "1", source voltage detection by the SVD circuit is executed. As soon as SVDON is reset to "0", the result is loaded to in the SVDDT register. To obtain a stable SVD detection result, the SVD circuit must be on for at least l00 µsec.
At initial reset, this register is set to "0".

SVDDT: SVD data (DFH•D1)

This is the result of supply voltage detection.

When "0" is read: Supply voltage (V_{DD}–V_{SS}) ≥ 1.8 V
When "1" is read: Supply voltage (V_{DD}–V_{SS}) < 1.8 V
Writing: Invalid

The result of supply voltage detection at time of SVDON is set to "0" can be read from this register.
At initial reset, SVDDT is set to "0".

Programming notes

(1) To obtain a stable SVD detection result, the SVD circuit must be on for at least l00 µsec. So, to obtain the SVD detection result, follow the programming sequence below.

① Set SVDON to "1"
② Maintain for 100 µsec minimum
③ Set SVDON to "0"
④ Read SVDDT

However, when fOSC1 is selected for CPU system clock, the instruction cycles are long enough, so there is no need to worry about maintaining 100 µsec for SVDON = "1" in the software.

(2) The SVD circuit should normally be turned OFF as the consumption current of the IC becomes large when it is ON.

4.10 Telephone Function

Configuration of telephone function

The E0C62T3 has a telephone function built-in. This function includes about DTMF (Dual Tone Multi-Frequency), DP (Dialing pulse), Pause, Flash, Hold-line, Mute control, Hook switch control and Handfree.
The configuration of the telephone function is shown in Figure 4.10.1. First of all, the CPU reads or writes these functions through data bus. And the control registers transmit the instructions of CPU to each blocks.
According to the instructions, telephone timing generator will generate the timing to associated circuits. And mute generator perform mute function to the associated output terminals ($\overline{\text{RMUTE}}$ and $\overline{\text{TMUTE}}$).
When telephone function operates at DTMF mode, DTMF generator use a 3.58 MHz oscillator as source clock to generate the tone signal (signal tone or dual tone) and outputs tone signal to TONE terminal.
When telephone function works at DP mode, DP generator use a 32 kHz oscillator as source clock to produce the dialing pulses and outputs pulses signal to $\overline{\text{DP}}$ terminal.
CPU will be informed by the interrupt circuit when the function (DTMF, DP, Pause, Flash) is over.
Input port K22, it is better to be used as $\overline{\text{HS}}$ (Hook-Switch) terminal. Because K22 has the highest interrupt priority.
Output port R12 and R13 can be selected as the output terminals or HFO and HDO terminals through the software.
See Section 4.5, "Output Ports".

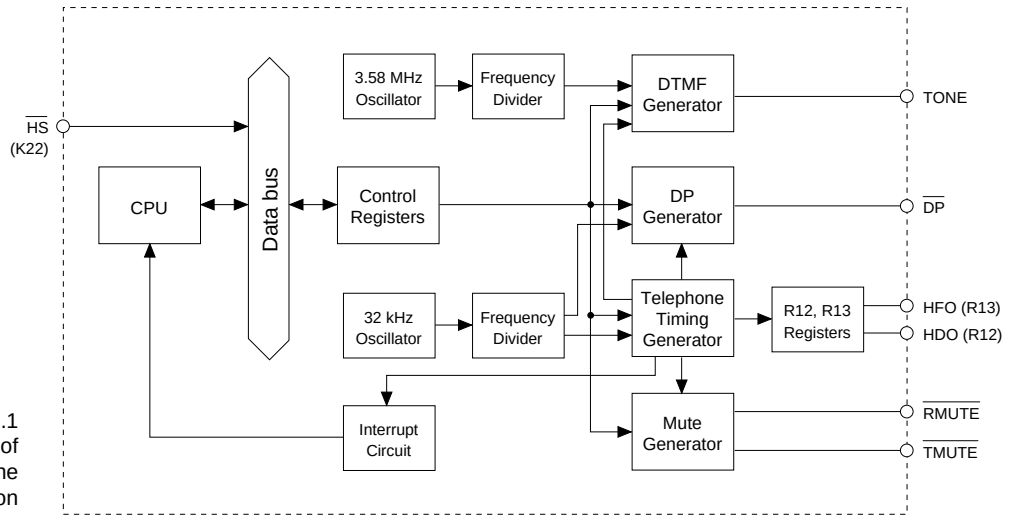


Fig. 4.10.1 Configuration of telephone function

Mask option

Output specifications for the $\overline{DP}$, $\overline{RMUTE}$ and $\overline{TMUTE}$ are selected with the mask option in pairs of either complementary output or Nch open drain output.

Output specifications for the HDO and HFO are selected with the mask option in pairs of either complementary output or Nch open drain output. See Section 4.5, "Output Ports".

However, even when Nch open drain output is selected, voltage exceeding source voltage must not be applied to the output port.

Operation of telephone function

To realize the operation of the telephone function, dialing procedure is the most important concept. This procedure contains three steps: (1) setting, (2) executing and (3) interrupt.

(1) Setting

Every function has its control registers. It is necessary to set the appropriate control registers before execution.
Table 4.10.1 lists the relations of functions and control registers.

Table 4.10.1
Control registers and default setting

Functions	Control registers	Default setting
DTMF	TPS (E0H•D3) SINC, SINR (E6H)	Tone mode Dual tone
DP	TPS (E0H•D3) MB (E0H•D1) DRS (E0H•D0) IDP3–IDP0 (E5H)	Tone mode 40 : 60 10 pps 750 ms
PAUSE	PTS3–PTS0 (E1H)	4 sec
FLASH	FTS3–FTS0 (E2H)	563 ms

See "Control of telephone function".

(2) Executing

After setting, writing the corresponding control register to start the execution.
Table 4.10.2 lists control registers for executing.

Table 4.10.2
Control registers and executing function

Functions	Control registers	Executing function
DTMF	TCD3–TCD0 (E7H) CTO (EBH•D3) HSON (E9H•D0)	Dialing tone Continuous tone output ON/OFF Hook switch ON/OFF
DP	TCD3–TCD0 (E7H) HSON (E9H•D0)	Dialing pulse Hook switch ON/OFF
Pause	PAUSE (E3H•D1)	Pause
Flash	FLASH (E3H•D0)	Flash
Hold-line	HOLD (E3H•D2)	Hold-line
Handfree	HF (E4H•D3)	Handfree

See "Control of telephone function".

Hook switch control (HSON), continuous tone output (CTO), hold-line (HOLD) and handfree (HF) are toggle selection. These functions don't generate interrupts.

HSON must be turned ON before executing the telephone function.

Dialing number (TCD), Pause (PAUSE) and Flash (FLASH) will be executed immediately when the corresponding control registers are written. These function will generate interrupts after it is finished.

For handfree function, R13 port can be used as HFO (handfree output) signal output terminal.
The register CHFO (EAH•D3) can control the R13 port as HFO or DC output terminal.
When HFO output is selected, R13 terminal outputs the data which is written in the register HF (E4H•D3). See Section 4.5, "Output Ports".

(3) Interrupt

After executing cycle has been finished, the CPU will be informed by an interrupt.
The register ID (C5H•D0) has to be clear "0", before start next executing cycle.
By reading register ID to check the executing function has been finished or not. The register ID will be clear to "0" after read out.
Interrupt mask register EID (D2H•D0) can be selected to mask or enable interrupt.
See "Telephone function and interrupt".

Figure 4.10.2 is an example of dialing pulse.

When it is at the setting step. It can be selected as DP mode, M/B ratio = 40:60, dialing rate = 10 pps, by writing "1000" into address E0H. To write data into IDP (E5H), PTS (E1H) and FTS (E2H) can set inter-digit pause time, pause time and flash time, respectively. If IDP, PTS and FTS do not change, they will use default value.

When it is during executing step.
To write "0001" into address E9H, enable the dialing function. At the same time, $\overline{DP}$ terminal will be pulled to high level (V_{DD}). By writing "0101" into TCD, it will start the dialing pulse function and outputs the five pulses at $\overline{DP}$ terminal. $\overline{TMUTE}$ and $\overline{RMUTE}$ terminals are also concurrently activated.

After pulse sending has been finished, it will generate an interrupt. Next operation can be started from executing step, but ID has to be cleared to "0" before next operation.

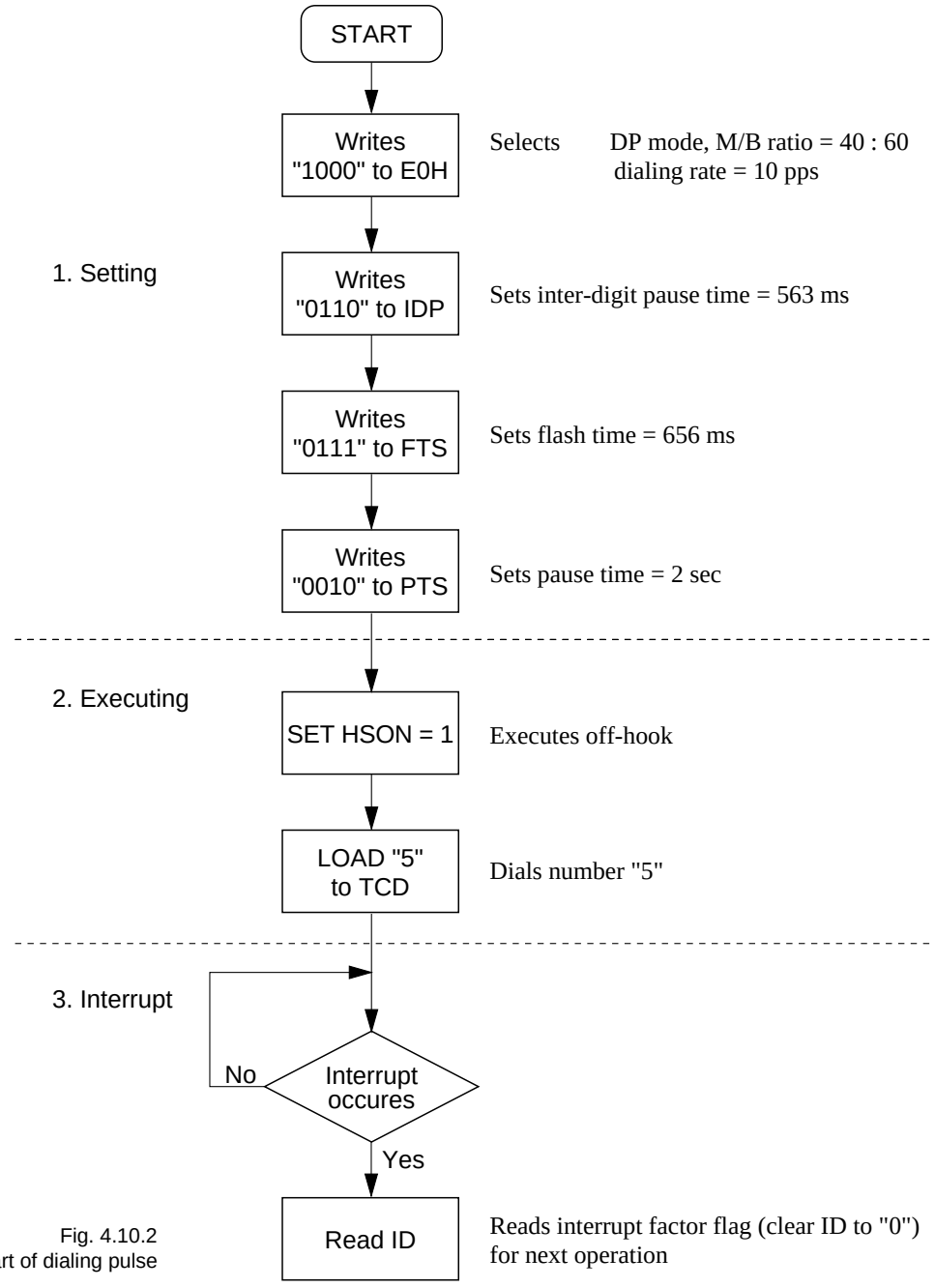


Fig. 4.10.2
Flow chart of dialing pulse

Dialing tone

The operation of dialing tone, which uses different composition of frequencies to represent the dialing number and transmits it, is activated by TCD3–TCD0 (E7H) and tone duration time is controlled by register CTO (EBH•D3).
A complete dialing tone cycle is including tone duration time (minimum 94 msec) and tone inter-digit pause time (94 msec). When dialing tone is over, CPU will be informed by an interrupt.

DTMF (Dual Tone Multi-Frequency) is used to generate a compound frequency or single frequency. DTMF generator can compose two kind of frequency to represent the dialing number.
Tone frequency, which is generated from DTMF generator, are classified into two groups. One is the Column group (high group), the other is the Row group (low group).

Table 4.10.3 lists the comparisons of Standard vs Actual tone frequency.

Table 4.10.3
Standard vs Actual tone frequency

	Tone output frequency (Hz)		Error (%) *
	Standard	Actual	
ROW1	697	701.32	+0.62
ROW2	770	771.45	+0.19
ROW3	852	857.17	+0.61
ROW4	941	935.10	–0.63
COL1	1209	1215.88	+0.57
COL2	1336	1331.68	–0.32
COL3	1477	1471.85	–0.35
COL4	1633	1645.01	+0.74

* Error (%) does not include oscillator drift

Figure 4.10.3 is the block diagram of DTMF generator.

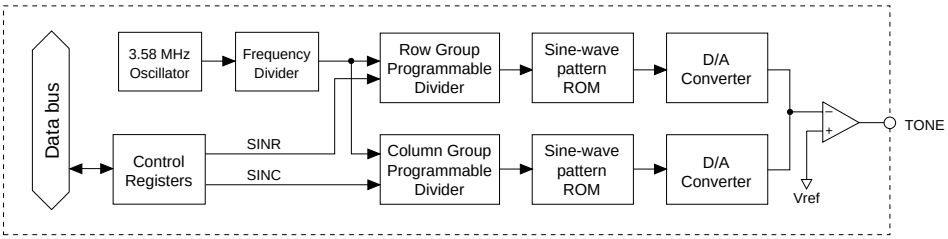


Fig. 4.10.3
Block diagram of DTMF generator

In Figure 4.10.3, 3.58 MHz oscillator is used as source clock for DTMF generator (it has to be turned on before activated DTMF generator). Programmable divider is controlled by registers SINR (E6H•D1) and SINC (E6H•D0) to select the tone output as single tone (Row or Column) or dual tone output.
Sine-wave ROM and D/A converter are used to convert the data, which comes from programmable divider, to generate a tone waveform. The dual tone signal is composed with an addition of two frequencies and each signal is selected from different group.

When uses dialing tone, it is needed to understand the relations of control registers and I/O terminals. There are explained as below.

The dialing tone signal is output on TONE terminal. At standby state, the terminal TONE is VSS level.

The terminals $\overline{\text{RMUTE}}$ and $\overline{\text{TMUTE}}$ are used for mute, and both terminals can be controlled by the registers CRMUT (E8H•D1) and CTMUT (E8H•D0).

The register HSON (E9H•D0) is used to set HOOK state. By writing data into register HSON can set HOOK-ON or HOOK-OFF status. When HSON is set to HOOK-OFF state, terminal $\overline{\text{DP}}$ will go high level (VDD).
The default setting of HSON is HOOK-ON (HSON = "0").

The Tone/Pulse (T/P) mode is software-selectable to be either tone or pulse mode. By writing data into register TPS (E0H•D3) can select tone or pulse mode.
The default setting of T/P is tone mode (TPS = "0").

The registers of SINR (E6H•D1) and SINC (E6H•D0) are used for selecting tone output frequencies.
The default selection is dual tone output.
Table 4.10.4 lists the selection of tone output.

Table 4.10.4
Selection of tone output

Control registers		Tone output
SINR	SINC	
0	0	DC level : $\frac{1}{2}$ (VDD–VSS)
0	1	Column frequencies
1	0	Row frequencies
1	1	Dual tone output

By writing code into registers TCD (E7H), a dialing tone cycle has being started and outputs tone at TONE terminal. The tone frequencies and code has a relationship.
Table 4.10.5 lists the relationship of code and tone frequencies.

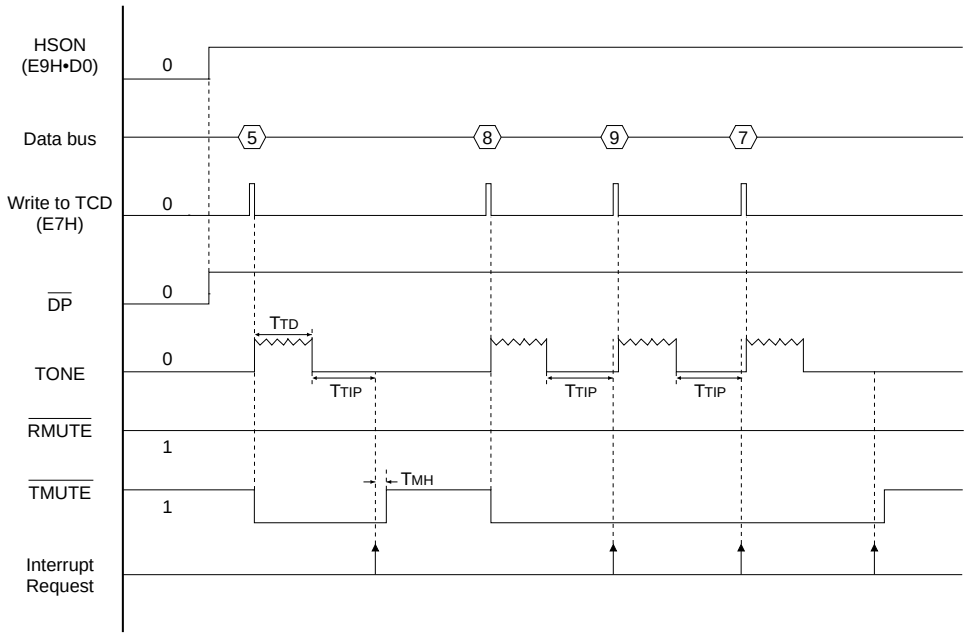
Table 4.10.5
Relationship of code and tone frequencies

TCD's code				Tone frequencies	Key's symbol	TCD's code				Tone frequencies	Key's symbol
D3	D2	D1	D0			D3	D2	D1	D0		
0	0	0	0	(ROW1, COL4)		1	0	0	0	(ROW3, COL2)	"8"
0	0	0	1	(ROW1, COL1)	"1"	1	0	0	1	(ROW3, COL3)	"9"
0	0	1	0	(ROW1, COL2)	"2"	1	0	1	0	(ROW4, COL2)	"0"
0	0	1	1	(ROW1, COL3)	"3"	1	0	1	1	(ROW4, COL3)	"#"
0	1	0	0	(ROW2, COL1)	"4"	1	1	0	0	(ROW4, COL1)	"*"
0	1	0	1	(ROW2, COL2)	"5"	1	1	0	1	(ROW2, COL4)	
0	1	1	0	(ROW2, COL3)	"6"	1	1	1	0	(ROW4, COL4)	
0	1	1	1	(ROW3, COL1)	"7"	1	1	1	1	(ROW3, COL4)	

At initial reset, these registers (TCD) are set to "0".

The register CTO (EBH•D3) is used to decide the tone duration time. The minimum value of tone duration time is 94 msec.
When CTO is set to "0", tone duration time will be output with the minimum time (94 msec).
When CTO is set to "1", tone duration time will be output until the CTO is changed to "0". If the period (CTO is changed from "1" to "0"), which is controlled by CTO, is less than 94 msec. The duration time will be prolonged to 94 msec.

Figure 4.10.4 is the timing diagram of dialing tone.
The DTMF generator produces the dialing tone on terminal TONE. At the same time, $\overline{\text{TMUTE}}$ terminal will go low level (VSS) during the tone duration time and tone inter-digit pause time periods. $\overline{\text{TMUTE}}$ terminal will be continuously kept on low level (VSS), if next dialing number is coming within Tmh (4 msec). Otherwise, they will go high level (VDD) after passed a period of time Tmh (4 msec).



TTD : Tone duration time
TTIP : Tone inter-digit pause time
TMH : Mute hold time

Fig. 4.10.4
Timing diagram of dialing tone

Dialing pulse (DP)

The operation of dialing pulse, which uses pulse numbers to represent the dialing number, is activated by writing data into registers TCD3–TCD0 (E7H). A complete dialing pulse cycle includes dialing number period and inter-digit pause time period. When dialing pulse cycle is finished, CPU will be informed by an interrupt.

Figure 4.10.5 is the block diagram of the DP generator.

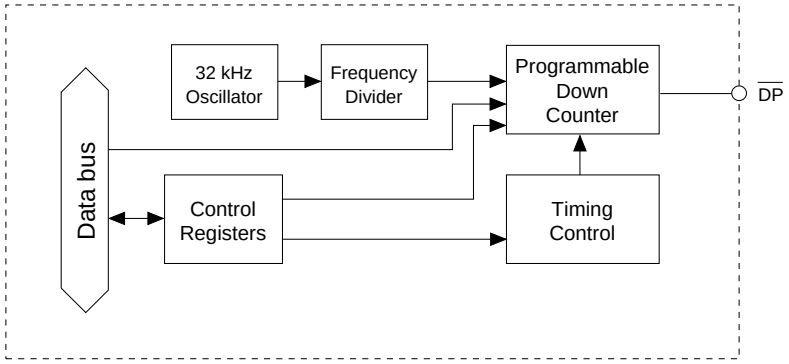


Fig. 4.10.5
Block diagram of DP generator

The CPU can select Tone/Pulse mode, Make/Break ratio and dialing pulse rate by writing data into control registers (E0H) TPS, MB and DRS, respectively.
32 kHz oscillator is used to generate the dialing pulses through the frequency divider, programmable down counter and timing control. Basically, the dialing number will be loaded into programmable down counter. Then, the programmable down counter will produce pulses to $\overline{DP}$ terminal until the counter is equal to zero.
The dialing pulse signal is output on $\overline{DP}$ terminal.
At initial, terminal $\overline{DP}$ is low level (V_{SS}) and number dialing can not be executed.

When uses dialing pulse, it is needed to understand the relations of control registers and I/O terminals. There are explained as below.

When the control register HSON (E9H•D0) is set to "HOOK-OFF" state, terminal $\overline{DP}$ will go high level (V_{DD}) and number dialing can be executed.

The terminals $\overline{TMUTE}$ and $\overline{RMUTE}$ are used for mute, and both terminals can be controlled by registers CTMUT (E8H•D0) and CRMUT (E8H•D1).

The Tone/Pulse (T/P) mode is software-selectable to be either Tone or Pulse mode. By writing data into register TPS (E0H•D3) can select Tone or Pulse mode.
The default setting of T/P is Tone mode. So it is needed to set TPS = "1", during DP mode.

The Make/Break ratio (M/B) is software-selectable to be either 40/60 or 33.3/66.6. By writing data into register MB (E0H•D1) can select 40/60 or 33.3/66.6. During dialing number period, the "Make" is before the "Break".
The default value of M/B is 40/60 (MB = "0").

The dialing pulse rate (DR) is software-selectable to be either 10 or 20 pps (pulse per second). By writing data into register DRS (E0H•D0) can select 10 or 20 pps.
The default value of DR is 10 pps (DRS = "0").

When dialing number at DP mode, it need to give an inter-digit pause time (IDP) between two numbers. The value of IDP can be selected from 94 msec to 1406 msec by writing data into registers IDP3–IDP0 (E5H).
The default value of IDP is 750 msec.

By writing code into registers TCD (E7H), a dialing pulse cycle has being started and outputs pulses at $\overline{DP}$ terminal.
The count of pulse has a relationship with code.
Table 4.10.6 lists the relationship of code and pulse's counts.

Table 4.10.6
Relationship of code and pulse's counts

TCD's code				Counts of pulse (pulses)	TCD's code				Counts of pulse (pulses)
D3	D2	D1	D0		D3	D2	D1	D0	
0	0	0	0	Use inhibited *	1	0	0	0	8
0	0	0	1	1	1	0	0	1	9
0	0	1	0	2	1	0	1	0	10
0	0	1	1	3	1	0	1	1	11
0	1	0	0	4	1	1	0	0	12
0	1	0	1	5	1	1	0	1	13
0	1	1	0	6	1	1	1	0	14
0	1	1	1	7	1	1	1	1	15

* If software program writes a code of "0H" into TCD register, it will cause a malfunction.

At initial reset, these registers (TCD) are set to "0".

Figure 4.10.6 is the timing diagram of DP function.
When DP generator produces the dialing pulse, Make period is before Break period and outputs pulses on $\overline{DP}$ terminal.
At the same time, $\overline{RMUTE}$ and $\overline{TMUTE}$ terminals will go low level (V_{SS}) during the dialing pulses and inter-digit pause time. Both terminal ($\overline{RMUTE}$ and $\overline{TMUTE}$) will be continuously kept on low level, if next dialing number is coming within Tmh (4 msec). Otherwise, they ($\overline{RMUTE}$ and $\overline{TMUTE}$) will go high level (V_{DD}) after passed a period of time Tmh (4 msec).

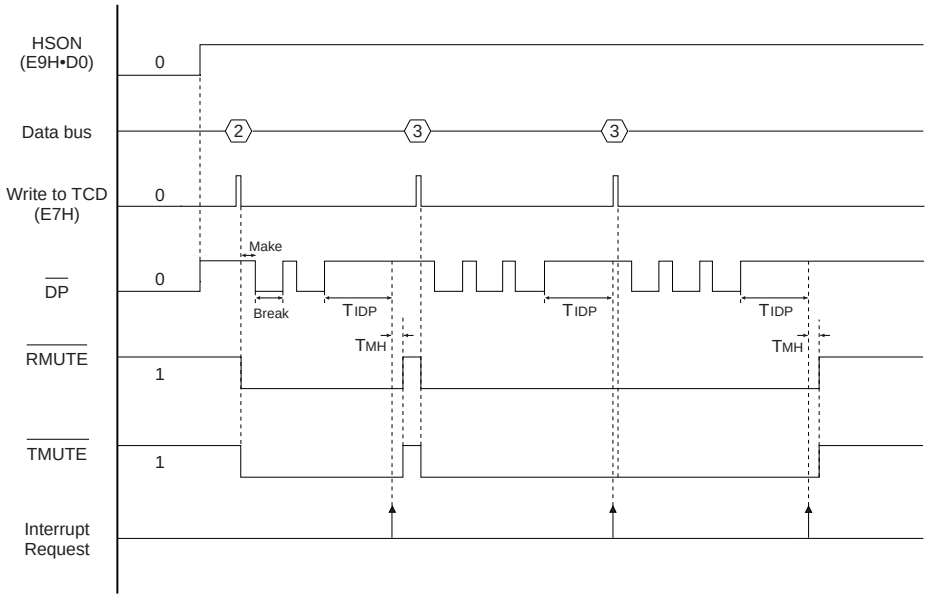


Fig. 4.10.6
Timing diagram of
DP function

T_{IDP} : Inter-digit pause time
T_{MH} : Mute hold time

Pause

The pause operation, which causes a pre-determined period of pause time in data transmission, is activated by writing "1" into the control register PAUSE (E3H•D1). When the pause operation is finished, CPU will be informed by an interrupt and the control register PAUSE is cleared to "0", automatically.

Pause time can be selected by the control registers PTS3–PTS0 (E1H) through CPU. The value of Pause Time is from 1 sec to 15 sec.
Table 4.10.7 lists pause times.

Table 4.10.7
Selection of pause times

PTS				Pause time (sec)	PTS				Pause time (sec)
D3	D2	D1	D0		D3	D2	D1	D0	
0	0	0	0	Use inhibited *	1	0	0	0	8
0	0	0	1	1	1	0	0	1	9
0	0	1	0	2	1	0	1	0	10
0	0	1	1	3	1	0	1	1	11
0	1	0	0	4	1	1	0	0	12
0	1	0	1	5	1	1	0	1	13
0	1	1	0	6	1	1	1	0	14
0	1	1	1	7	1	1	1	1	15

* If software program writes a code of "0H" into PTS register, it will cause a malfunction.

Figure 4.10.7 and Figure 4.10.8 show the timing diagram of pause function at DP (Dialing Pulse) and DTMF (Dual Tone Multi-Frequency) mode, respectively.

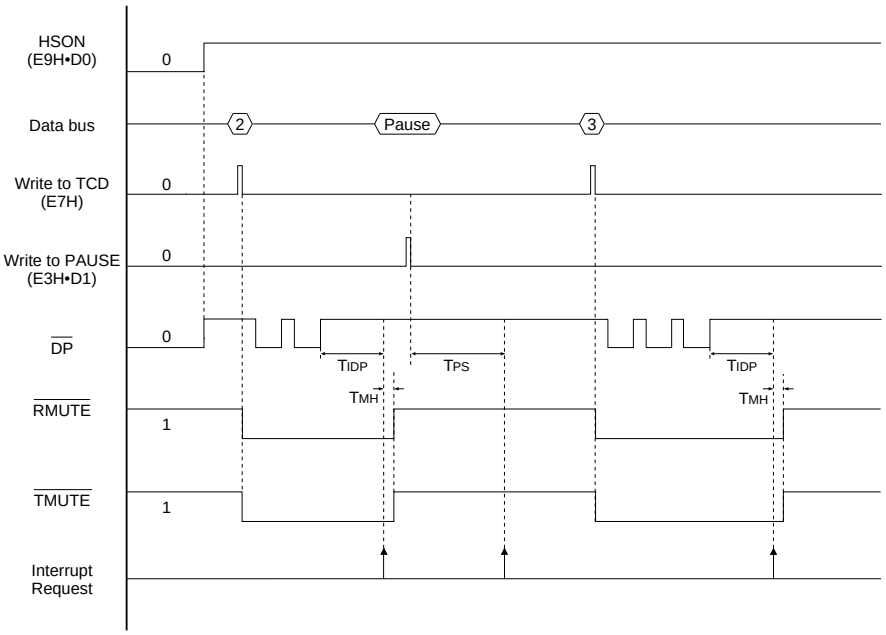


Fig. 4.10.7
Timing diagram
of pause function
at DP mode

T_{IDP} : Inter-digit pause time
T_{MH} : Mute hold time
T_{PS} : pause time

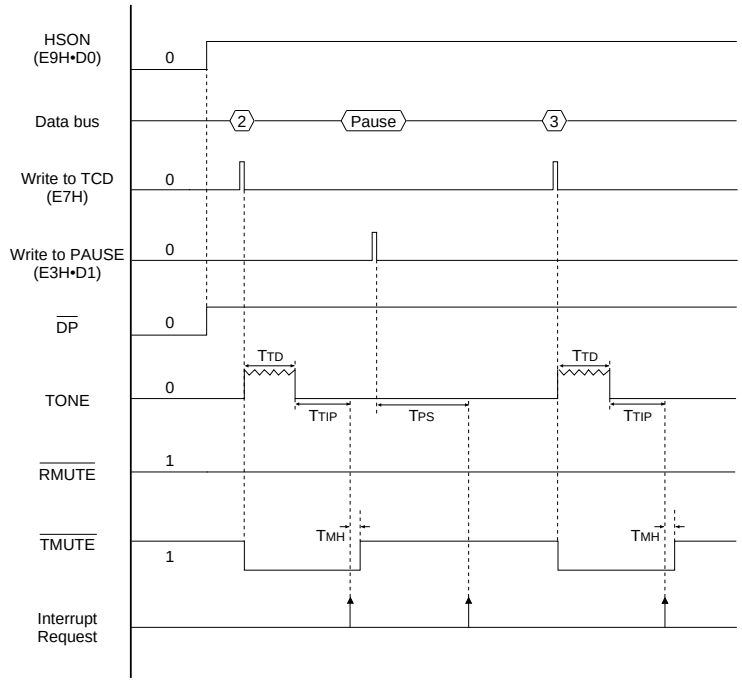


Fig. 4.10.8
Timing diagram
of pause function
at DTMF mode

T_{TD} : Tone duration time
T_{TIP} : Tone inter-digit pause time
T_{MH} : Mute hold time
T_{PS} : pause time

Flash

The flash operation, which restores the device to the on-hook state for a pre-determined period of time, is activated by writing "1" into the control register FLASH (E3H•D0). A complete flash function cycle is including flash time period and flash pause time period. When the flash function cycle is finished, CPU will be informed by an interrupt and the control register FLASH is cleared to "0", automatically.

Flash time can be selected by the control registers FTS3–FTS0 (E2H) through CPU. The range of flash time period is from 94 msec to 1406 msec and flash pause time period is fixed to 938 msec. Table 4.10.8 lists the flash times.

Table 4.10.8
Selection of flash times

FTS				Flash time (ms)	FTS				Flash time (ms)
D3	D2	D1	D0		D3	D2	D1	D0	
0	0	0	0	Use inhibited *	1	0	0	0	750
0	0	0	1	94	1	0	0	1	844
0	0	1	0	188	1	0	1	0	938
0	0	1	1	281	1	0	1	1	1031
0	1	0	0	375	1	1	0	0	1125
0	1	0	1	469	1	1	0	1	1219
0	1	1	0	563	1	1	1	0	1313
0	1	1	1	656	1	1	1	1	1406

* If software program writes a code of "0H" into FTS register, it will cause a malfunction.

Figure 4.10.9 is the timing diagram of flash function.
When executing flash function, the $\overline{DP}$ terminal goes low level (Vss) during the flash time period. $\overline{RMUTE}$ and $\overline{TMUTE}$ terminals go low level (Vss) during the flash time and flash pause time periods. Following the flash time period, there is a 938 msec Flash Pause Time before further data is transmitted.

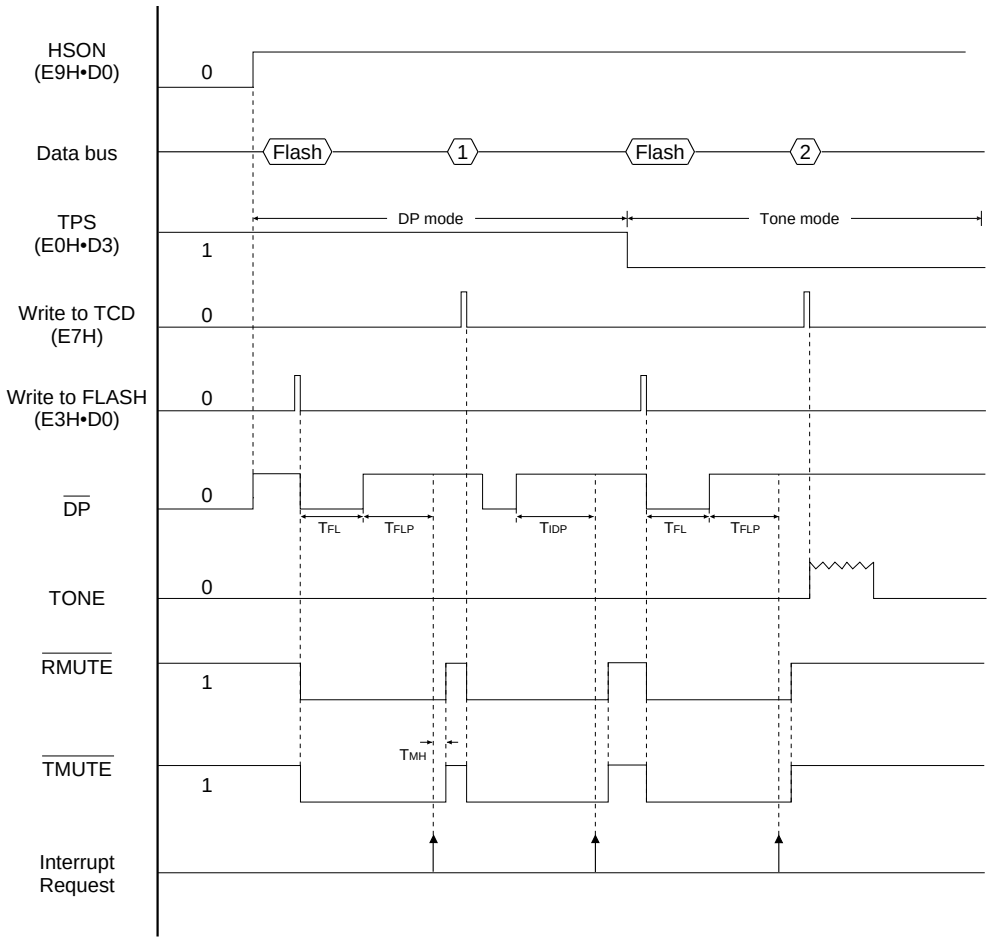


Fig. 4.10.9
Timing diagram of flash function

T_{FL} : Flash time
T_{FLP} : Flash pause time
T_{IDP} : Inter-digit pause time
T_{MH} : Mute hold time

Hold-line

The hold-line operation, which is used to keep current telephone communication, is turned ON/OFF by writing "1"/"0" into control register HOLD (E3H•D2).

HDO (Hold-Line Output) is output terminal for hold-line function. R12 terminal can be selected for HDO output terminal by setting the register CHDO (EAH•D2) to "1". At the same time, R12 register (D3H•D2) must be set to "0", otherwise R12 terminal goes high level (V_{DD}).
See Section 4.5, "Output Ports".

When the HDO output is selected, the R12 terminal outputs the data which is written in the register HOLD (E3H•D2).

Figure 4.10.10 shows the timing diagram of hold-line function. When register HOLD (E3H•D2) is turned ON, $\overline{TMUTE}$ terminal goes low level (V_{SS}) and HDO (R12) terminal goes high level (V_{DD}). When register HOLD (E3H•D2) is turned OFF, $\overline{TMUTE}$ goes high level (V_{DD}) and HDO (R12) terminal goes low level (V_{SS}).

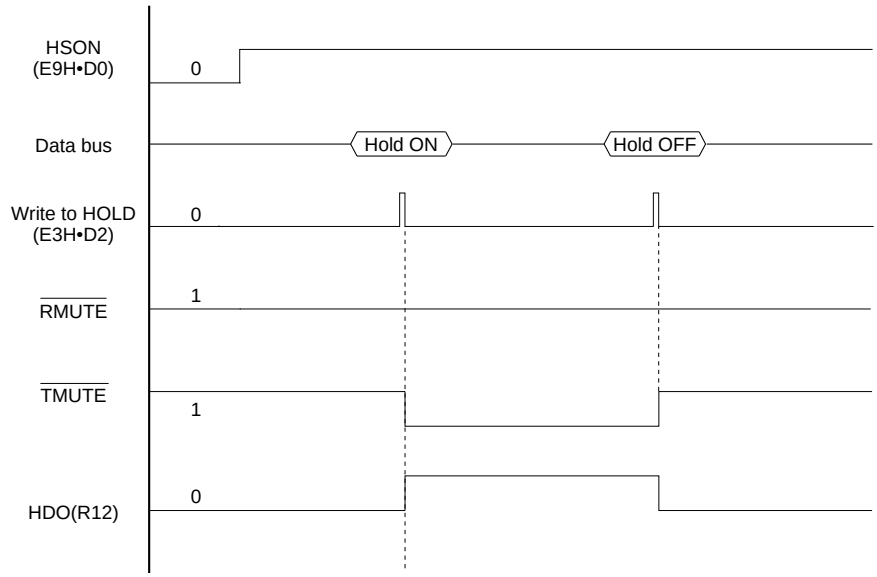


Fig. 4.10.10
Timing diagram of hold-line function

Telephone function and interrupt

There are three kinds of telephone function can generate interrupt. Which are number dialing, pause, and flash.

(1) Number dialing has two modes.

a. ***DTMF mode***
This mode will wait a period of time that contains the tone duration period (minimum 94 msec) and tone inter-digit pause period (94 msec), then generates an interrupt.
See Figure 4.10.4, "Timing diagram of dialing tone".

b. ***DP mode***
This mode will wait a period of time that contains the dialing number period and inter-digit pause period, then generates an interrupt.
See Figure 4.10.6, "Timing diagram of DP function".

(2) Pause function will wait a period of pause time (software-selectable: 1 sec to 15 sec), then generates an interrupt.
See Figure 4.10.7, "Timing diagram of pause function at DP mode", and Figure 4.10.8, "Timing diagram of pause function at DTMF mode".

(3) Flash function will wait a period of flash time (software-selectable: 94 msec to 1406 msec), then generates an interrupt.
See Figure 4.10.9, "Timing diagram of flash function".

The register ID (C5H•D0) is set by an interrupt of telephone function. By reading register ID, can check the executing cycle has been finished or not.
The register ID has to be clear "0", before starts next executing cycle.
Interrupt mask register EID (D2H•D0) can be selected to mask or enable interrupt.

Control of telephone function

Tables 4.10.9(a)–(d) list the telephone function's control bits and their address.

Table 4.10.9(a) Control bits of telephone function

Address *6	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
C5H	0	0	0	ID	0	– *2			Unused *5
	R				0	– *2			Unused *5
					0	– *2			Unused *5
					ID	0	Yes	No	Interrupt factor flag (dialing) Clear to 0 after read out
D2H	0	0	0	EID	0	– *2			Unused *5
	R			R/W	0	– *2			Unused *5
					0	– *2			Unused *5
					EID	0	Enable	Mask	Interrupt mask register (dialing)
D3H	R13	R12	R11	R10	R13	0	High	Low	Output port (R13)
					HFO		– *4	ON	Handfree output (HFO)
	HFO	HDO	BZ	$\overline{BZ}$	R12	0	High	Low	Output port (R12)
					HDO		– *4	ON	Hold-line output (HDO)
	R/W				R11	0	High	Low	Output port (R11)
					BZ		– *4	ON	Buzzer output (BZ)
					R10	0	High	Low	Output port (R10)
					$\overline{BZ}$		– *4	ON	Buzzer inverted output ($\overline{BZ}$)
D8H	0	0	CLKCHG	OSCC	0	– *2			Unused *5
	R		R/W		0	– *2			Unused *5
					CLKCHG	0	OSC3	OSC1	CPU system clock switch
					OSCC	0	ON	OFF	OSC3 oscillation ON/OFF
E0H	TPS	0	MB	DRS	TPS	0	PULSE	TONE	Tone / pulse mode selection
	R/W	R	R/W		0	– *2			Unused *5
					MB	0	33.3:66.6	40:60	Make : Break ratio selection
					DRS	0	20 pps	10 pps	Dialing pulse rate selection

*1 Initial value at initial reset
*2 Not set in the circuit
*3 Undefined
*4 Inhibit state (output port will be set to "1")
*5 Constantly "0" when being read
*6 Page switching in I/O memory is not necessary

Table 4.10.9(b) Control bits of telephone function

Address *6	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
E1H	PTS3	PTS2	PTS1	PTS0	PTS3	0			Pause time selection 0 : Use inhibited 8 : 8 sec 1 : 1 sec 9 : 9 sec 2 : 2 sec A : 10 sec 3 : 3 sec B : 11 sec 4 : 4 sec C : 12 sec 5 : 5 sec D : 13 sec 6 : 6 sec E : 14 sec 7 : 7 sec F : 15 sec
	R/W				PTS2	1			
					PTS1	0			
	Default value : 4 seconds				PTS0	0			
E2H	FTS3	FTS2	FTS1	FTS0	FTS3	0			Flash time selection 0 : Use inhibited 8 : 750 ms 1 : 94 ms 9 : 844 ms 2 : 188 ms A : 938 ms 3 : 281 ms B : 1031 ms 4 : 375 ms C : 1125 ms 5 : 469 ms D : 1219 ms 6 : 563 ms E : 1313 ms 7 : 656 ms F : 1406 ms
	R/W				FTS2	1			
					FTS1	1			
	Default value : 563 ms				FTS0	0			
E3H	0	HOLD	PAUSE	FLASH	0	– *2			Unused *5
	R	R/W	W		HOLD	0	On	Off	Hold-line function
					PAUSE	0	Yes	No	Pause function *5
					FLASH	0	Yes	No	Flash function *5
E4H	HF	0	0	0	HF	0	Yes	No	Hand free
	R/W	R			0	– *2			Unused *5
					0	– *2			Unused *5
					0	– *2			Unused *5
E5H	IDP3	IDP2	IDP1	IDP0	IDP3	1			Inter-digit pause selection for dial pulse 0 : Use inhibited 8 : 750 ms 1 : 94 ms 9 : 844 ms 2 : 188 ms A : 938 ms 3 : 281 ms B : 1031 ms 4 : 375 ms C : 1125 ms 5 : 469 ms D : 1219 ms 6 : 563 ms E : 1313 ms 7 : 656 ms F : 1406 ms
	R/W				IDP2	0			
					IDP1	0			
	Default value : 750 ms				IDP0	0			

*1 Initial value at initial reset
*2 Not set in the circuit
*3 Undefined
*4 Inhibit state (output port will be set to "1")
*5 Constantly "0" when being read
*6 Page switching in I/O memory is not necessary

Table 4.10.9(c) Control bits of telephone function

Address *6	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
E6H	0	0	SINR	SINC	0	– *2			Unused *5
	R		R/W		0	– *2			Unused *5
					SINR	1	Enable	Disable	DTMF row frequency output enable
					SINC	1	Enable	Disable	DTMF column frequency output enable
E7H	TCD3	TCD2	TCD1	TCD0	TCD3	0			Telephone code for dialing TCD DTMF DP TCD DTMF DP 0 : (R_1C_4) Use inhibited 8 : (R_3C_2) 8 1 : (R_1C_1) 1 9 : (R_3C_3) 9 2 : (R_1C_2) 2 A : (R_4C_2) 10 3 : (R_1C_3) 3 B : (R_4C_3) 11 4 : (R_2C_1) 4 C : (R_4C_1) 12 5 : (R_2C_2) 5 D : (R_2C_4) 13 6 : (R_2C_3) 6 E : (R_4C_4) 14 7 : (R_3C_1) 7 F : (R_3C_4) 15
	R/W				TCD2	0			
					TCD1	0			
					TCD0	0			
E8H	0	0	CRMUT	CTMUT	0	– *2			Unused *5
	R		R/W		0	– *2			Unused *5
					CRMUT	1	Receive mute output	0	Receive mute control
					CTMUT	1	Transmit mute output	0	Transmit mute control
E9H	0	0	0	HSON	0	– *2			Unused *5
	R			R/W	0	– *2			Unused *5
					0	– *2			
					HSON	0	Hook Off	Hook On	Hook switch ON/OFF
EAH	CHFO	CHDO	0	0	CHFO	0	Handfree output	DC	R13 output selection (R13 data register has to be "0")
	R/W		R		CHDO	0	Hold output	DC	R12 output selection (R12 data register has to be "0")
					0	– *2			Unused *5
					0	– *2			Unused *5

*1 Initial value at initial reset
*2 Not set in the circuit
*3 Undefined
*4 Inhibit state (output port will be set to "1")
*5 Constantly "0" when being read
*6 Page switching in I/O memory is not necessary

Table 4.10.9(d) Control bits of telephone function

Address *6	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
EBH	CTO	0	0	0	CTO	0	Continuous tone output ON	Continuous tone output OFF	Tone duration time control
	R/W	R			0	– *2			Unused *5
					0	– *2			Unused *5
					0	– *2			Unused *5

*1 Initial value at initial reset
*2 Not set in the circuit
*3 Undefined
*4 Inhibit state (output port will be set to "1")
*5 Constantly "0" when being read
*6 Page switching in I/O memory is not necessary

ID: Interrupt factor flag (dialing) (C5H•D0)

This flag indicates the status of the dialing interrupt, that is for dialing number, pause and flash function.

When "1" is read: Interrupt has occurred
When "0" is read: Interrupt has not occurred
Writing: Invalid

After executing a dialing function (dialing number, pause, flash), it needs to read the ID (C5H•D0). Otherwise, the next dialing function can not be executed.
The software can judge from this flag whether there is a dialing interrupt. However, even if the interrupt is masked, the flag is set to "1" at the falling edge of the signal.
This flag can be reset through being read out by the software.
Reading of interrupt factor flag is available at EI, but be careful in the following cases.
If the interrupt mask register value corresponding to the interrupt factor flag to be read is set to "1", an interrupt request will be generated by the interrupt factor flag set timing.
At initial reset, this flag is set to "0".

EID: Interrupt mask register (dialing) (D2H•D0)

This register is used to select whether to mask the dialing interrupt.

When "1" is written: Enabled
When "0" is written: Masked
Reading: Valid

Writing to the interrupt mask register can be done only in the DI status (interrupt flag = "0").
At initial reset, this register is set to "0".

R13:
(When HFO is selected)
Special output port data
(D3H•D3)

Controls the HFO (HandFree Output) output and acts as HFO output terminal.

When "1" is written: High level (DC) output
When "0" is written: Handfree signal output
Reading: Valid

R13 terminal can be used as HFO signal output terminal, by writing "1" into register CHFO (EAH•D3), "0" into register R13 (D3H•D3).
When HFO output is selected, the R13 terminal outputs the data which is written in the register HF (E4H•D3).
At initial reset, this register is set to "0".

R12:
(When HDO is selected)
Special output port data
(D3H•D2)

Controls the HDO (Hold-Line Output) output and acts as HDO output terminal.

When "1" is written: High level (DC) output
When "0" is written: Hold-line signal output
Reading: Valid

R12 terminal can be used as HDO signal output terminal, by writing "1" into register CHDO (EAH•D2), "0" into register R12 (D3H•D2).
When HDO output is selected, the R12 terminal outputs the data which is written in the register HOLD (E3H•D2).
At initial reset, this register is set to "0".

OSCC:
OSC3 oscillation control
(D8H•D0)

Controls oscillation ON/OFF for the OSC3 oscillation circuit.

When "1" is written: The OSC3 oscillation ON
When "0" is written: The OSC3 oscillation OFF
Reading: Valid

When it is necessary to activate DTMF generator or to operate the CPU at high speed, set OSCC to "1". At other times, set it to "0" to lessen the current consumption. When "Not Use" is selected for the mask option of the OSC3 oscillation circuit, keep OSCC set to "0".
At initial reset, OSCC is set to "0".

TPS:
Tone/Pulse mode selection
(E0H•D3)

Selects the dialing mode to dual tone multi-frequency mode or dialing pulse mode.

When "1" is written: Pulse mode
When "0" is written: Tone mode
Reading: Valid

At initial reset, this register is set to "0".

MB:
Make/Break ratio selection
(E0H•D1)

Selects the Make/Break ratio for dialing pulse mode.

When "1" is written: 33.3/66.6
When "0" is written: 40.0/60.0
Reading: Valid

When DP generator produces the dialing pulse, "Make" period is before "Break" period.
At initial reset, this register is set to "0".

DRS:
Dialing pulse rate selection
(E0H•D0)

Selects the dialing pulse rate for dialing pulse mode.

When "1" is written: 20 pps (pulses per second)
When "0" is written: 10 pps (pulses per second)
Reading: Valid

At initial reset, this register is set to "0".

PTS0–PTS3:
Pause time selection
(E1H)

These registers are used to select pause time.
Table 4.10.10 lists the pause times.

Table 4.10.10
Selection of pause times

PTS				Pause time (sec)	PTS				Pause time (sec)
D3	D2	D1	D0		D3	D2	D1	D0	
0	0	0	0	Use inhibited *	1	0	0	0	8
0	0	0	1	1	1	0	0	1	9
0	0	1	0	2	1	0	1	0	10
0	0	1	1	3	1	0	1	1	11
0	1	0	0	4	1	1	0	0	12
0	1	0	1	5	1	1	0	1	13
0	1	1	0	6	1	1	1	0	14
0	1	1	1	7	1	1	1	1	15

* If software program writes a code of "0H" into PTS register, it will cause a malfunction.

At initial reset, the pause time is set to 4 seconds.

FTS0–FTS3:
Flash time selection
(E2H)

These registers are used to select flash time.
Table 4.10.11 lists the flash times.

Table 4.10.11
Selection of flash times

FTS				Flash time (ms)	FTS				Flash time (ms)
D3	D2	D1	D0		D3	D2	D1	D0	
0	0	0	0	Use inhibited *	1	0	0	0	750
0	0	0	1	94	1	0	0	1	844
0	0	1	0	188	1	0	1	0	938
0	0	1	1	281	1	0	1	1	1031
0	1	0	0	375	1	1	0	0	1125
0	1	0	1	469	1	1	0	1	1219
0	1	1	0	563	1	1	1	0	1313
0	1	1	1	656	1	1	1	1	1406

* If software program writes a code of "0H" into FTS register, it will cause a malfunction.

At initial reset, the flash time is set to 563 msec.

HOLD: Hold-line function (E3H•D2)

Executes the hold function ON/OFF and outputs data from register HOLD to R12 terminal.

When "1" is written: ON (High level output on R12 terminal)
When "0" is written: OFF (Low level output on R12 terminal)
Reading: Valid

HDO (Hold-Line Output) is output terminal for hold-line function. When HDO output is selected, the R12 terminal outputs the data which is written in the register HOLD (E3H•D2).
When R12 terminal is used as HDO output port. The register CHDO (EAH•D2) must be written "1" and register R12 (D3H•D2) must be written "0".
When HOLD (E3H•D2) register is turned ON, $\overline{\text{TMUTE}}$ terminal goes low level (VSS) and HDO (R12) terminal goes high level (VDD).
When HOLD register is turned OFF, $\overline{\text{TMUTE}}$ terminal goes high level (VDD) and HDO (R12) terminal goes low level (VSS).
Hold-line function is a toggle selection and it does not generate interrupt. At initial reset, this register is set to "0".

PAUSE: Pause function (E3H•D1)

Executes the pause function.

When "1" is written: Execute pause function
When "0" is written: No operation
Reading: Always "0"

By writing "1" into register PAUSE (E3H•D1), can start the execution of pause function.
When the operation of pause function has been finished, CPU will be informed by an interrupt and register PAUSE is cleared to "0", automatically.
When pause function is executing, $\overline{\text{DP}}$ terminal will output a predetermined pause time.
At initial reset, this register is set to "0".

FLASH: Flash function (E3H•D0)

Executes the flash function.

When "1" is written: Execute flash function
When "0" is written: No operation
Reading: Always "0"

By writing "1" into register FLASH (E3H•D0), can start the execution of flash function.
When the operation of flash function has been finished, CPU will be informed by an interrupt and register FLASH is cleared to "0", automatically.
When flash function is executing, $\overline{\text{DP}}$ terminal goes low level (VSS) during the flash time period. $\overline{\text{RMUTE}}$ and $\overline{\text{TMUTE}}$ terminals go low level (VSS) during the flash time and flash pause time periods.
At initial reset, this register is set to "0".

HF: Handfree (E4H•D3)

Executes the handfree function ON/OFF and outputs data from register HF to HFO (R13) terminal.

When "1" is written: ON (High level output on R13 terminal)
When "0" is written: OFF (Low level output on R13 terminal)
Reading: Valid

HFO (HandFree Output) is output terminal for handfree function. When HFO output is selected, the R13 terminal outputs the data which is written in the register HF (E4H•D3).
When R13 terminal is used as HFO output port. The register CHFO (EAH•D3) must be written "1" and register R13 (D3H•D3) must be written "0".
Handfree function is a toggle selection and it does not generate interrupt.
At initial reset, this register is set to "0".

IDP0–IDP3: Inter-digit pause time selection (E5H)

These registers are used to select inter-digit pause time for dialing pulse mode.
Table 4.10.12 lists the inter-digit pause times.

Table 4.10.12 Selection of inter-digit pause times

IDP				Inter-digit pause (ms)	IDP				Inter-digit pause (ms)
D3	D2	D1	D0		D3	D2	D1	D0	
0	0	0	0	Use inhibited *	1	0	0	0	750
0	0	0	1	94	1	0	0	1	844
0	0	1	0	188	1	0	1	0	938
0	0	1	1	281	1	0	1	1	1031
0	1	0	0	375	1	1	0	0	1125
0	1	0	1	469	1	1	0	1	1219
0	1	1	0	563	1	1	1	0	1313
0	1	1	1	656	1	1	1	1	1406

* If software program writes a code of "0H" into IDP, it will cause a malfunction.

A complete dialing pulse cycle includes a dialing number period and following an inter-digit pause time period.
At initial reset, the inter-digit pause time is set to 750 msec.

SINR: DTMF row frequencies output enable (E6H•D1)

Selects DTMF row frequencies output enable or disable.

When "1" is written: Enabled
When "0" is written: Disabled
Reading: Valid

See "Register SINC (E6H•D0)".
At initial reset, this register is set to "1".

SINC: DTMF column frequencies output enable (E6H•D0)

Selects DTMF column frequencies output enable or disable.

When "1" is written: Enabled
When "0" is written: Disabled
Reading: Valid

SINR and SINC can be composed to control tone output as DC level, single tone (Row or Column) and dual tone output. The default selection is dual tone output.
At initial reset, these registers are set to "1".

Table 4.10.13(a) lists the selection of tone output.

Table 4.10.13(a) Selection of tone output

Control registers		Tone output
SINR	SINC	
0	0	DC level : $\frac{1}{2}$ (V_{DD}–V_{SS})
0	1	Column frequencies
1	0	Row frequencies
1	1	Dual tone output

When single tone is selected, by writing code into registers TCD (E7H), the terminal of TONE will output relative frequency. Tables 4.10.13(b) and (c) list the relationship of code and frequency.

Table 4.10.13(b) Relationship of TCD's code and column frequency

TCD's code				Column frequency (Hz) *		TCD's code				Column frequency (Hz) *	
D3	D2	D1	D0			D3	D2	D1	D0		
0	0	0	0	COL4 :	1645.01	1	0	0	0	COL2 :	1331.68
0	0	0	1	COL1 :	1215.88	1	0	0	1	COL3 :	1471.85
0	0	1	0	COL2 :	1331.68	1	0	1	0	COL2 :	1331.68
0	0	1	1	COL3 :	1471.85	1	0	1	1	COL3 :	1471.85
0	1	0	0	COL1 :	1215.88	1	1	0	0	COL1 :	1215.88
0	1	0	1	COL2 :	1331.68	1	1	0	1	COL4 :	1645.01
0	1	1	0	COL3 :	1471.85	1	1	1	0	COL4 :	1645.01
0	1	1	1	COL1 :	1215.88	1	1	1	1	COL4 :	1645.01

* It does not include oscillator drift

Table 4.10.13(c) Relationship of TCD's code and row frequency

TCD's code				Row frequency (Hz) *		TCD's code				Row frequency (Hz) *	
D3	D2	D1	D0			D3	D2	D1	D0		
0	0	0	0	ROW1 :	701.32	1	0	0	0	ROW3 :	857.17
0	0	0	1	ROW1 :	701.32	1	0	0	1	ROW3 :	857.17
0	0	1	0	ROW1 :	701.32	1	0	1	0	ROW4 :	935.10
0	0	1	1	ROW1 :	701.32	1	0	1	1	ROW4 :	935.10
0	1	0	0	ROW2 :	771.45	1	1	0	0	ROW4 :	935.10
0	1	0	1	ROW2 :	771.45	1	1	0	1	ROW2 :	771.45
0	1	1	0	ROW2 :	771.45	1	1	1	0	ROW4 :	935.10
0	1	1	1	ROW3 :	857.17	1	1	1	1	ROW3 :	857.17

* It does not include oscillator drift

TCD0–TCD3:
Telephone code for dialing
(E7H)

Telephone code for dialing.
By writing code into registers TCD (E7H), starts the dialing number cycle and outputs signal to appropriate terminals. When dialing number cycle is finished, CPU will be informed by an interrupt. Depending the status of register TPS (E0H•D3), TCD is separated into two mode DP mode (TPS = "1") and DTMF mode (TPS = "0").

(1) DP mode

By writing code into registers TCD (E7H), a dialing pulse cycle has being started and outputs pulses at $\overline{DP}$ terminal. The counts of pulse has a relationship with code.
Table 4.10.14 lists the relationship of code and pulse's counts.

Table 4.10.14
Relationship of code and pulse's count

TCD's code				Counts of pulse (pulses)	TCD's code				Counts of pulse (pulses)
D3	D2	D1	D0		D3	D2	D1	D0	
0	0	0	0	Use inhibited *	1	0	0	0	8
0	0	0	1	1	1	0	0	1	9
0	0	1	0	2	1	0	1	0	10
0	0	1	1	3	1	0	1	1	11
0	1	0	0	4	1	1	0	0	12
0	1	0	1	5	1	1	0	1	13
0	1	1	0	6	1	1	1	0	14
0	1	1	1	7	1	1	1	1	15

* If software program writes a code of "0H" into TCD register, it will cause a malfunction.

At initial reset, these registers (TCD) are set to "0".

(2) DTMF mode

By writing code into registers TCD (E7H), a dialing tone cycle has being started and outputs tone signal at TONE terminal. The tone frequencies and code has a relationship.
Table 4.10.15 lists the relationship of code and tone frequencies.

Table 4.10.15
Relationship of code and tone frequencies

TCD's code				Tone frequencies	Key's symbol	TCD's code				Tone frequencies	Key's symbol
D3	D2	D1	D0			D3	D2	D1	D0		
0	0	0	0	(ROW1, COL4)		1	0	0	0	(ROW3, COL2)	"8"
0	0	0	1	(ROW1, COL1)	"1"	1	0	0	1	(ROW3, COL3)	"9"
0	0	1	0	(ROW1, COL2)	"2"	1	0	1	0	(ROW4, COL2)	"0"
0	0	1	1	(ROW1, COL3)	"3"	1	0	1	1	(ROW4, COL3)	"#"
0	1	0	0	(ROW2, COL1)	"4"	1	1	0	0	(ROW4, COL1)	"*"
0	1	0	1	(ROW2, COL2)	"5"	1	1	0	1	(ROW2, COL4)	
0	1	1	0	(ROW2, COL3)	"6"	1	1	1	0	(ROW4, COL4)	
0	1	1	1	(ROW3, COL1)	"7"	1	1	1	1	(ROW3, COL4)	

At initial reset, these registers (TCD) are set to "0".

CRMUT:
Receive mute control
(E8H•D1)

Controls the receive mute.

When "1" is written: Receive mute output
When "0" is written: Low level output on $\overline{\text{RMUTE}}$ terminal
Reading: Valid

The receive mute signal is output on terminal $\overline{\text{RMUTE}}$ and terminal $\overline{\text{RMUTE}}$ can be controlled by register CRMUT.
By writing the register CRMUT to "0", terminal $\overline{\text{RMUTE}}$ is set to low level (VSS), forever.
When the register CRMUT is written to "1", the output terminal of $\overline{\text{RMUTE}}$ will be controlled by telephone function (Terminal $\overline{\text{RMUTE}}$ will go low level (Vss) during dialing pulse cycle or flash function cycle).
At initial reset, this register is set to "1".

CTMUT:
Transmit mute control
(E8H•D0)

Controls the transmit mute.

When "1" is written: Transmit mute output
When "0" is written: Low level output on $\overline{\text{TMUTE}}$ terminal
Reading: Valid

The transmit mute signal is output on terminal $\overline{\text{TMUTE}}$ and terminal $\overline{\text{TMUTE}}$ can be controlled by register CTMUT.
By writing the register CTMUT to "0", terminal $\overline{\text{TMUTE}}$ is set to low level (VSS), forever.
When the register CTMUT is written to "1", the output terminal of $\overline{\text{TMUTE}}$ will be controlled by telephone function (Terminal $\overline{\text{TMUTE}}$ will go low level (Vss) during dialing pulse cycle, flash function cycle, dialing tone cycle or hold-line function).
At initial reset, this register is set to "1".

HSON:
Hook switch ON/OFF
(E9H•D0)

Controls the hook switch ON/OFF.

When "1" is written: Hook off
When "0" is written: Hook on
Reading: Valid

When the register HSON is set to "1", $\overline{\text{DP}}$ terminal will be pulled to high level (VDD), immediately.
At initial reset, this register is set to "0".

CHFO:
R13 output selection register
(EAH•D3)

Selects the output type for the R13 terminal.

When "1" is written: Handfree signal output
When "0" is written: DC output
Reading: Valid

By setting the register CHFO to "1", R13 is set to HFO (HandFree Output) output port. When CHFO is set to "0", R13 becomes the regular DC output port.
See Section 4.5, "Output Ports".
At initial reset, this register is set to "0".

CHDO:
R12 output selection register
(EAH•D2)

Selects the output type for the R12 terminal.

When "1" is written: Hold-line signal output
When "0" is written: DC output
Reading: Valid

By setting the register CHDO to "1", R12 is set to HDO (Hold-Line Output) output port. When CHDO is set to "0", R12 becomes the regular DC output port.
See Section 4.5, "Output Ports".
At initial reset, this register is set to "0".

CTO:
Continuous output tone selection
(EBH•D3)

Selects the tone duration time to be continuous output or not.

When "1" is written: Continuous
When "0" is written: Uncontinuous
Reading: Valid

The register CTO (EBH•D3) is used to decide the tone duration time. The minimum value of tone duration time is 94 msec.
When CTO is set to "0", tone duration time will be output with the minimum time (94 msec).
When CTO is set to "1", tone duration time will be output until the CTO is changed to "0". If the period (CTO is changed from "1" to "0"), which is controlled by CTO, is less than 94 msec. The duration time will be prolonged to 94 msec.
At initial reset, this register is set to "0".

Programming notes

(1) When uses the DTMF, it is necessary to turn ON the 3.58 MHz oscillator. This function needs big current. Therefore, using DTMF dialing at off-hook or handfree status is the best.

(2) Reading of interrupt factor flags is available at EI, but be careful in the following cases.
If the interrupt mask register value corresponding to the interrupt factor flags to be read is set to "1", an interrupt request will be generated by the interrupt factor flags set timing, or an interrupt request will not be generated.

(3) Write the interrupt mask register (EID) only in the DI status (interrupt flag = "0"). Writing during EI status (interrupt flag = "1") will cause malfunction.

(4) If software program writes a code of "0H" into TCD register in pulse mode, IDP, FTS or PTS registers, it will cause a malfunction.

(5) Because pause function control register (E3H•D1) and flash function control register (E3H•D0) are write-only, software cannot use ALU instructions (AND, OR ...) on E3H resisters while dialing a pause or flash function cycle.

4.11 Interrupt and HALT

<Interrupt types>

The E0C62T3 provides the following interrupt settings, each of which is maskable.

External interrupt: • Input interrupt (4 systems)

Internal interrupt: • Timer interrupt (1 system)
• Dialing interrupt (1 system)

To authorize interrupt, the interrupt flag must be set to "1" (EI) and the necessary related interrupt mask registers must be set to "1" (enable).
When an interrupt occurs the interrupt flag is automatically reset to "0" (DI), and interrupts after that are inhibited.
Figure 4.11.1 shows the configuration of the interrupt circuit.

<HALT>

The E0C62T3 has HALT function. The function can considerably reduce the current consumption, when it is used.

The CPU enters the HALT status when the HALT instruction is executed.
In the HALT status, the operation of the CPU is stopped. However, the oscillation circuit operates. Reactivating the CPU from the HALT status is done by generating an interrupt request. When it does not reactivate upon an interrupt request, the watchdog timer (watchdog timer must be in "ON" status) will cause it to restart from the initial reset status.

Refer to the "E0C6200/6200A Core CPU Manual" for transition to the HALT status and timing of its cancellation.

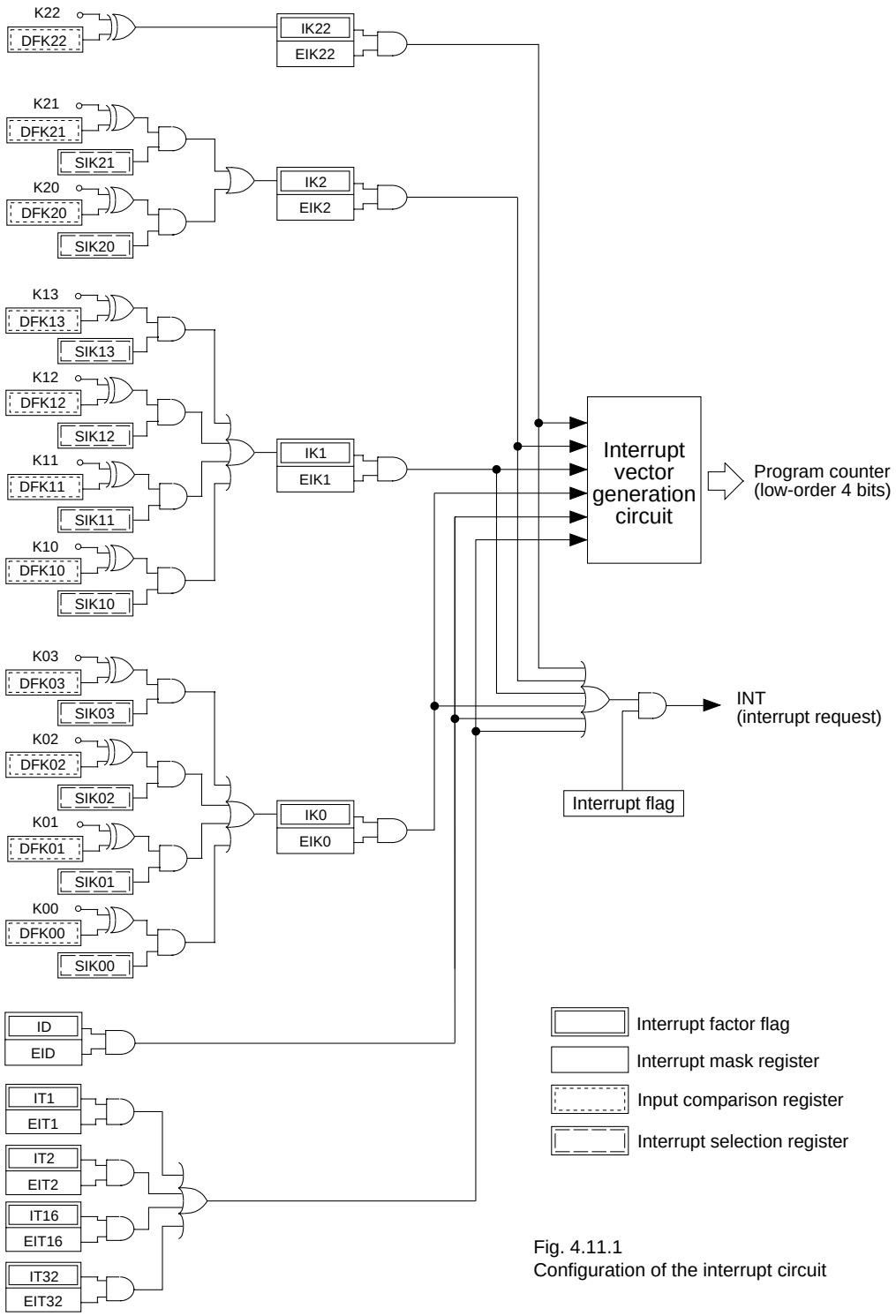


Fig. 4.11.1
Configuration of the interrupt circuit

Interrupt factor

Table 4.11.1 shows the factors for generating interrupt requests.

The interrupt flags are set to "1" depending on the corresponding interrupt factors.
The CPU operation is interrupted when any of the conditions below set an interrupt factor flag to "1".

- The corresponding mask register is "1" (enabled)
- The interrupt flag is "1" (EI)

The interrupt factor flag is a read-only register, but can be reset to "0" when the register data is read out.
At initial reset, the interrupt factor flags are reset to "0".

Table 4.11.1
Interrupt factors

Interrupt factor	Interrupt factor flag
Input data (K22) rising or falling edge	IK22 (C0H•D0)
Input data (K20, K21) rising or falling edge	IK2 (C1H•D0)
Input data (K10–K13) rising or falling edge	IK1 (C2H•D0)
Input data (K00–K03) rising or falling edge	IK0 (C3H•D0)
Clock timer 1 Hz falling edge	IT1 (C4H•D3)
Clock timer 2 Hz falling edge	IT2 (C4•D2)
Clock timer 16 Hz falling edge	IT16 (C4H•D1)
Clock timer 32 Hz falling edge	IT32 (C4H•D0)
Dialing cycle completion	ID (C5H•D0)

Note: *Reading of interrupt factor flags is available at EI, but be careful in the following cases.*
If the interrupt mask register value corresponding to the interrupt factor flags to be read is set to "1", an interrupt request will be generated by the interrupt factor flags set timing, or an interrupt request will not be generated. Be very careful when interrupt factor flags are in the same address.

Interrupt mask

The interrupt factor flags can be masked by the corresponding interrupt mask registers.
The interrupt mask registers are read/write registers. They are enabled (interrupt authorized) when "1" is written to them, and masked (interrupt inhibited) when "0" is written to them.
At initial reset, the interrupt mask register is set to "0".
Table 4.11.2 shows the correspondence between interrupt mask registers and interrupt factor flags.

Table 4.11.2
Interrupt mask registers and interrupt factor flags

Interrupt mask register	Interrupt factor flag
EIK22 (D0H•D3)	IK22 (C0H•D0)
EIK2 (D0H•D2)	IK2 (C1H•D0)
EIK1 (D0H•D1)	IK1 (C2H•D0)
EIK0 (D0H•D0)	IK0 (C3H•D0)
EIT1 (D1H•D3)	IT1 (C4H•D3)
EIT2 (D1H•D2)	IT2 (C4H•D2)
EIT16 (D1H•D1)	IT16 (C4H•D1)
EIT32 (D1H•D0)	IT32 (C4H•D0)
EID (D2H•D0)	ID (C5H•D0)

Note: *Write the interrupt mask register only in the DI status (interrupt flag = "0"). Writing during EI status (interrupt flag = "1") will cause malfunction.*

Interrupt vector

When an interrupt request is input to the CPU, the CPU begins interrupt processing. After the program being executed is terminated, the interrupt processing is executed in the following order.

① The address data (value of program counter) of the program to be executed next is saved in the stack area (RAM).

② The interrupt request causes the value of the interrupt vector (page 1, 02H–0DH) to be set in the program counter.

③ The program at the specified address is executed (execution of interrupt processing routine by software).

Table 4.11.3 shows the correspondence of interrupt requests and interrupt vectors.

Note: *The processing in ① and ② above take 12 cycles of the CPU system clock.*

Table 4.11.3
Interrupt request and interrupt vectors

Interrupt vector	Interrupt request	Priority
102H	Clock timer	Low
104H	Dialing cycle completion	↑
106H	K00–K03 input	
108H	K10–K13 input	
10AH	K20–K21 input	↓
10CH	K22 input	High

The four low-order bits of the program counter are indirectly addressed through the interrupt request.

Control of interrupt

Tables 4.11.4(a)–(c) show the interrupt control bits and their addresses.

Table 4.11.4(a) Control bits of interrupt (1)

Address *6	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
C0H	0	0	0	IK22	0	– *2			Unused *5
	R				0	– *2			Unused *5
					0	– *2			Unused *5
					IK22	0	Yes	No	Interrupt factor flag (K22) Clear to 0 after read out
C1H	0	0	0	IK2	0	– *2			Unused *5
	R				0	– *2			Unused *5
					0	– *2			Unused *5
					IK2	0	Yes	No	Interrupt factor flag (K20, K21) Clear to 0 after read out
C2H	0	0	0	IK1	0	– *2			Unused *5
	R				0	– *2			Unused *5
					0	– *2			Unused *5
					IK1	0	Yes	No	Interrupt factor flag (K10 ~ K13) Clear to 0 after read out
C3H	0	0	0	IK0	0	– *2			Unused *5
	R				0	– *2			Unused *5
					0	– *2			Unused *5
					IK0	0	Yes	No	Interrupt factor flag (K00 ~ K03) Clear to 0 after read out
C4H	IT1	IT2	IT16	IT32	IT1	0	Yes	No	Interrupt factor flag (clock timer 1 Hz) Clear to 0 after read out
	R				IT2	0	Yes	No	Interrupt factor flag (clock timer 2 Hz) Clear to 0 after read out
					IT16	0	Yes	No	Interrupt factor flag (clock timer 16 Hz) Clear to 0 after read out
					IT32	0	Yes	No	Interrupt factor flag (clock timer 32 Hz) Clear to 0 after read out

*1 Initial value at initial reset
*2 Not set in the circuit
*3 Undefined
*4 Inhibit state (output port will be set to "1")
*5 Constantly "0" when being read
*6 Page switching in I/O memory is not necessary

Table 4.11.4(b) Control bits of interrupt (2)

Address *6	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
C5H	0	0	0	ID	0	– *2			Unused *5
	R				0	– *2			Unused *5
					0	– *2			Unused *5
					ID	0	Yes	No	Interrupt factor flag (dialing) Clear to 0 after read out
C6H	0	0	SIK21	SIK20	0	– *2			Unused *5
	R		R/W		0	– *2			Unused *5
					SIK21	0	Enable	Disable	Interrupt selection register (K21)
					SIK20	0	Enable	Disable	Interrupt selection register (K20)
C7H	SIK13	SIK12	SIK11	SIK10	SIK13	0	Enable	Disable	Interrupt selection register (K13)
	R/W				SIK12	0	Enable	Disable	Interrupt selection register (K12)
					SIK11	0	Enable	Disable	Interrupt selection register (K11)
					SIK10	0	Enable	Disable	Interrupt selection register (K10)
C8H	SIK03	SIK02	SIK01	SIK00	SIK03	0	Enable	Disable	Interrupt selection register (K03)
	R/W				SIK02	0	Enable	Disable	Interrupt selection register (K02)
					SIK01	0	Enable	Disable	Interrupt selection register (K01)
					SIK00	0	Enable	Disable	Interrupt selection register (K00)
CCH	0	DFK22	DFK21	DFK20	0	– *2			Unused *5
	R	R/W			DFK22	1	↓	↑	
					DFK21	1	↓	↑	Input comparison register (K20 ~ K22)
					DFK20	1	↓	↑	

*1 Initial value at initial reset
*2 Not set in the circuit
*3 Undefined
*4 Inhibit state (output port will be set to "1")
*5 Constantly "0" when being read
*6 Page switching in I/O memory is not necessary

Table 4.11.4(c) Control bits of interrupt (3)

Address *6	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
CDH	DFK13	DFK12	DFK11	DFK10	DFK13	1	↓	↑	
	R/W				DFK12	1	↓	↑	
					DFK11	1	↓	↑	Input comparison register (K10 ~ K13)
					DFK10	1	↓	↑	
CEH	DFK03	DFK02	DFK01	DFK00	DFK03	1	↓	↑	
	R/W				DFK02	1	↓	↑	
					DFK01	1	↓	↑	Input comparison register (K00 ~ K03)
					DFK00	1	↓	↑	
D0H	EIK22	EIK2	EIK1	EIK0	EIK22	0	Enable	Mask	Interrupt mask register (K22)
	R/W				EIK2	0	Enable	Mask	Interrupt mask register (K20, K21)
					EIK1	0	Enable	Mask	Interrupt mask register (K10 ~ K13)
					EIK0	0	Enable	Mask	Interrupt mask register (K00 ~ K03)
D1H	EIT1	EIT2	EIT16	EIT32	EIT1	0	Enable	Mask	Interrupt mask register (clcok timer 1 Hz)
	R/W				EIT2	0	Enable	Mask	Interrupt mask register (clock timer 2 Hz)
					EIT16	0	Enable	Mask	Interrupt mask register (clock timer 16 Hz)
					EIT32	0	Enable	Mask	Interrupt mask register (clxok timer 32 Hz)
D2H	0	0	0	EID	0	– *2			Unused *5
	R			R/W	0	– *2			Unused *5
					0	– *2			Unused *5
					EID	0	Enable	Mask	Interrupt mask register (dialing)

*1 Initial value at initial reset
*2 Not set in the circuit
*3 Undefined
*4 Inhibit state (output port will be set to "1")
*5 Constantly "0" when being read
*6 Page switching in I/O memory is not necessary

IK22: Interrupt factor flag (C0H•D0)
DFK22: Input comparison register (CCH•D2)
EIK22: Interrupt mask register (D0H•D3)
See Section 4.4, "Input Ports".

IK2: Interrupt factor flag (C1H•D0)
SIK20, SIK21: Interrupt selection register (C6H•D0, D1)
DFK20, DFK21: Input comparison register (CCH•D0, D1)
EIK2: Interrupt mask register (D0H•D2)
See Section 4.4, "Input Ports".

IK1: Interrupt factor flag (C2H•D0)
SIK10–SIK13: Interrupt selection register (C7H)
DFK10–DFK13: Input comparison register (CDH)
EIK1: Interrupt mask register (D0H•D1)
See Section 4.4, "Input Ports".

IK0: Interrupt factor flag (C3H•D0)
SIK00–SIK03: Interrupt selection register (C8H)
DFK00–DFK03: Input comparison register (CEH)
EIK0: Interrupt mask register (D0H•D0)
See Section 4.4, "Input Ports".

IT32, IT16, IT2, IT1: Interrupt factor flag (C4H)
EIT32, EIT16, EIT2, EIT1: Interrupt mask register (D1H)
See Section 4.8, "Clock Timer".

ID: Interrupt factor flag (C5H•D0)
EID: Interrupt mask register (D2H•D0)
See Section 4.10, "Telephone Function".

Programming notes

(1) The interrupt factor flags are set when the timing condition is established, even if the interrupt mask registers are set to "0".

(2) Reading of interrupt factor flags is available at EI, but be careful in the following cases.
If the interrupt mask register value corresponding to the interrupt factor flags to be read is set to "1", an interrupt request will be generated by the interrupt factor flags set timing, or an interrupt request will not be generated. Be very careful when interrupt factor flags are in the same address.

(3) Write the interrupt mask register only in the DI status (interrupt flag = "0"). Writing during EI status (interrupt flag = "1") will cause malfunction.

CHAPTER 5 SUMMARY OF NOTES

5.1 Notes for Low Current Consumption

The E0C62T3 contains control registers for each of the circuits so that current consumption can be lowered. These control registers lower the current consumption through programs that operate the circuits at the minimum levels.
The following text explains the circuits that can control operation and their control registers. Refer to these when putting programs together.

Table 5.1.1
Circuits and control registers

Circuits (and items)	Control registers	Order of consumed current
CPU	HALT instruction	See electrical characteristics (chapter 7)
CPU operating frequency	CLKCHG, OSCC	See electrical characteristics (chapter 7)
SVD circuit	SVDON	Several tens µA

Below are the circuit statuses at initial reset.

CPU: Operating status

CPU operating frequency: Low speed (CLKCHG = "0"),
OSC3 oscillation circuit OFF status (OSCC = "0")

SVD circuit: OFF status (SVDON = "0")

Also, be careful about panel selection because the current consumption can differ by the order of several µA on account of the LCD panel characteristics.

5.2 Summary of Notes by Function

Here, the cautionary notes are summed up by function category. Keep these notes well in mind when programming.

Memory

Memory is not mounted in unused area within the memory map and in memory area not indicated in this manual. For this reason, normal operation cannot be assured for programs that have been prepared with access to these areas.

Watchdog timer

When the watchdog timer is being used, the software must reset it within 3-second cycles, and timer data (WD0 and WD1) cannot be used for timer applications.

Oscillation circuit

(1) It takes at least 5 msec from the time the OSC3 oscillation circuit goes ON until the oscillation stabilizes. Consequently, when switching the CPU operation clock from OSC1 to OSC3, do this after a minimum of 5 msec have elapsed since the OSC3 oscillation went ON.
Further, the oscillation stabilization time varies depending on the external oscillator characteristics and conditions of use, so allow ample margin when setting the wait time.

(2) When switching the clock form OSC3 to OSC1, use a separate instruction for switching the OSC3 oscillation OFF. An error in the CPU operation can result if this processing is performed at the same time by the one instruction.

Input ports

When input ports are changed from low to high by pull up resistor, the rise of the waveform is delayed on account of the time constant of the pull up resistor and input gate capacitance. Hence, when fetching input ports, set an appropriate wait time.
Particular care needs to be taken of the key scan during key matrix configuration.
Make this waiting time the amount of time or more calculated by the following expression.

$10 \times C \times R$

C: terminal capacitance 5 pF + parasitic capacitance ? pF
R: pull up resistance 300 kΩ

Output ports

(1) When output ports (R10–R13) are selected as special output, the corresponding output port data (R10–R13) must be set to "0".

(2) When BZ and $\overline{BZ}$ are selected, a hazard may be observed in the output waveform when the data of control registers (BZR11 and BZR10) change.

I/O ports

When in the input mode, I/O port is changed from low to high by pull up resistor, the rise of the waveform is delayed on account of the time constant of the pull up resistor and input gate capacitance. Hence, when fetching input ports, set an appropriate wait time. Particular care needs to be taken of the key scan during key matrix configuration.
Make this waiting time the amount of time or more calculated by the following expression.

$10 \times C \times R$

C: terminal capacitance 5 pF + parasitic capacitance ? pF
R: pull up resistance 300 kΩ

LCD driver

(1) The contents of the display memory are undefined until the area is initialized (through, for instance, memory clear processing by the CPU). Initialize the display memory by executing initial processing.

(2) Since the display memory area is write-only, display data cannot be rewritten by arithmetic operations (such as AND, OR, ADD, SUB).

Clock timer

(1) Be sure to data reading in the order of low-order data (TM0–TM3) then high-order data (TM4–TM7).

(2) When the clock timer has been reset, the interrupt factor flag (IT) may sometimes be set to "1". Consequently, perform flag reading (reset the flag) as necessary at reset.

(3) When the clock timer has been reset, the watchdog timer is also reset. (If watchdog timer is ON, WDON = "1")

SVD circuit

(1) To obtain a stable SVD detection result, the SVD circuit must be on for at least l00 µsec. So, to obtain the SVD detection result, follow the programming sequence below.

① Set SVDON to "1"
② Maintain for 100 µsec minimum
③ Set SVDON to "0"
④ Read SVDDT

However, when f_{OSC1} is selected for CPU system clock, the instruction cycles are long enough, so there is no need to worry about maintaining 100 µsec for SVDON = "1" in the software.

(2) The SVD circuit should normally be turned OFF as the consumption current of the IC becomes large when it is ON.

Telephone function

(1) When uses the DTMF, it is necessary to turn ON the 3.58 MHz oscillator. This function needs big current. Therefore, using DTMF dialing at off-hook or handfree status is the best.

(2) If software program writes a code of "0H" into TCD register in pulse mode, IDP, FTS or PTS registers, it will cause a malfunction.

(3) Because pause function control register (E3H•D1) and flash function control register (E3H•D0) are write-only, software cannot use ALU instructions (AND, OR ...) on E3H resisters while dialing a pause or flash function cycle.

Interrupt and HALT

(1) The interrupt factor flags are set when the timing condition is established, even if the interrupt mask registers are set to "0".

(2) Reading of interrupt factor flags is available at EI, but be careful in the following cases.
If the interrupt mask register value corresponding to the interrupt factor flags to be read is set to "1", an interrupt request will be generated by the interrupt factor flags set timing, or an interrupt request will not be generated. Be very careful when interrupt factor flags are in the same address.

(3) Write the interrupt mask register only in the DI status (interrupt flag = "0"). Writing during EI status (interrupt flag = "1") will cause malfunction.

CHAPTER 6 DIAGRAM OF TYPICAL APPLICATION

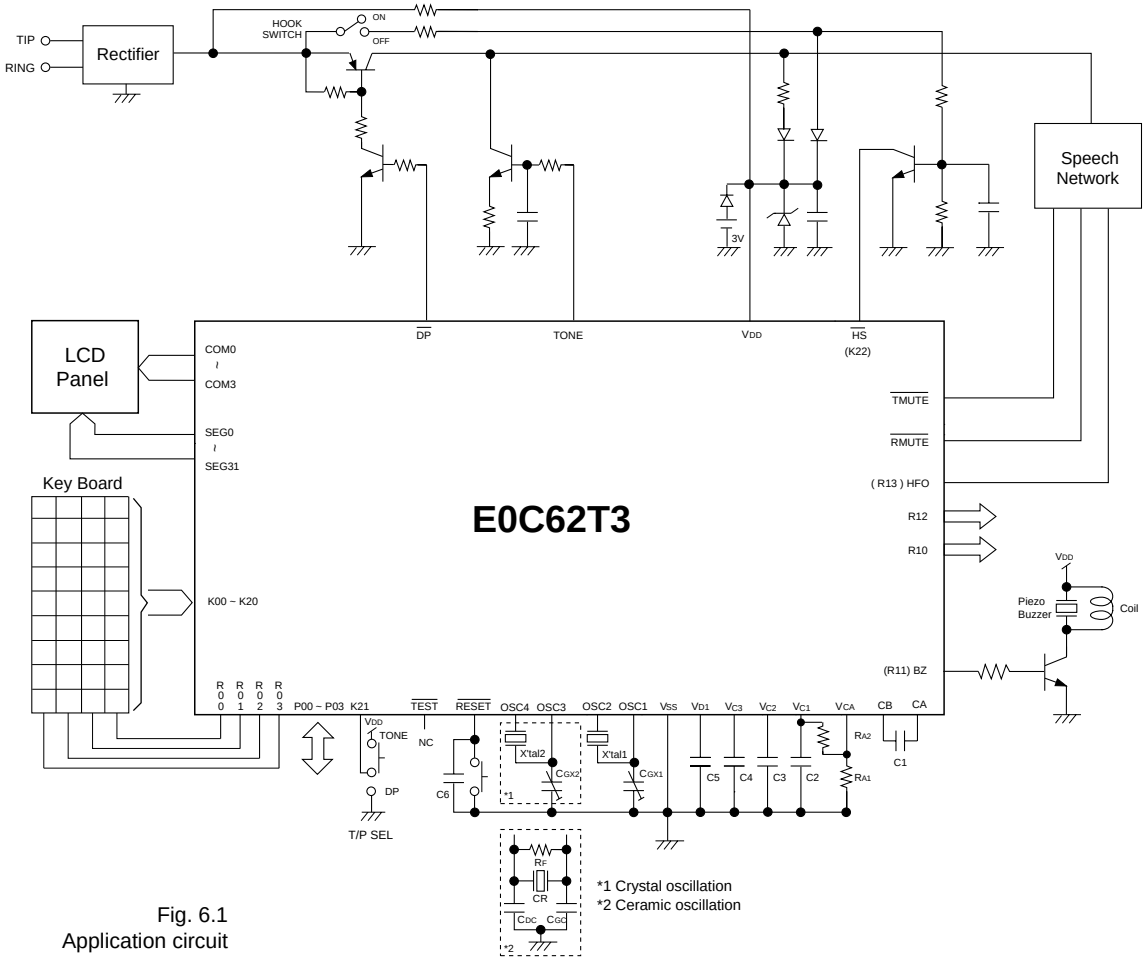


Fig. 6.1
Application circuit

Table 6.1
Components

X'tal1	Crystal oscillator	32,768 Hz CI (MAX)=35 kΩ
C_{GX1}	Trimmer capacitor	5–25 pF
X'tal2	Crystal oscillator	3.579545 MHz
C_{GX2}	Trimmer capacitor	5–25 pF
CR	Ceramic oscillator	3.579545 MHz
R_F	Feedback resistor	1 MΩ
C_{GC}	Gate capacitor	30 pF
C_{DC}	Drain capacitor	30 pF
R_{A1}	Resistance for LCD drive voltage adjustment	2 MΩ (V_{C1} = 1.5 V)
R_{A2}	Resistance for LCD drive voltage adjustment	1 MΩ (V_{C1} = 1.5V)
C_1–C_6	Capacitor	0.1 µF

Note: *The above table is simply an example, and is not guaranteed to work.*

• When the piezoelectric buzzer is driven directly

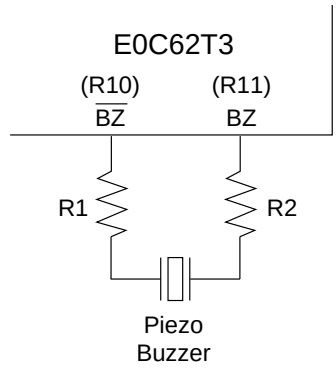


Fig. 6.2
Connection of directly driving buzzer

R1	Protection resistance	100 Ω
R2	Protection resistance	100 Ω

CHAPTER 7 ELECTRICAL CHARACTERISTICS

7.1 Absolute Maximum Rating

(V_{SS} = 0 V)

Item	Symbol	Rated value	Unit
Power voltage	V_{DD}	-0.5 to 7.0	V
Input voltage (1)	V_I	-0.5 to V_{DD} + 0.3	V
Input voltage (2)	V_{IOSC}	-0.5 to V_{D1} + 0.3	V
Permissible total output current *1	ΣI_{VDD}	10	mA
Operating temperature	Topr	-20 to 70	°C
Storage temperature	Tstg	-65 to 150	°C
Soldering temperature / Time	Tsol	260°C, 10sec (lead section)	–
Allowable dissipation *2	P_D	250	mW

*1 The permissible total output current is the sum total of the current (average current) that simultaneously flows from the output pins (or is drawn in).

*2 For plastic package (QFP5-80pin, QFP14-80pin)

7.2 Recommended Operating Conditions

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Power voltage	V_{DD}	V_{SS} = 0 V, OSC1 = 32 kHz, OSC3 = stop	1.6	3.0	5.5	V
		V_{SS} = 0 V When DTMF is used	2.5		5.5	V
Oscillation frequency (1)	f_{OSC1}			32,768		Hz
Oscillation frequency (2)	f_{OSC3}			3.579545		MHz

7.3 DC Characteristics

If no special requirement

V_{DD} = 3 V, V_{SS} = 0 V, f_{OSC1} = 32.768 kHz, Ta = 25°C, V_{D1}, V_{C1}, V_{C2} and V_{C3} are internal voltage,

C1–C5 = 0.1 µF

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
High level input voltage (1)	V_{IH1}		K00–K03, K10–K13 K20–K22, P00–P03	0.8·V_{DD}		V_{DD}	V
High level input voltage (2)	V_{IH2}		$\overline{RESET}$, $\overline{TEST}$	0.9·V_{DD}		V_{DD}	V
Low level input voltage (1)	V_{IL1}		K00–K03, K10–K13 K20–K22, P00–P03	0		0.2·V_{DD}	V
Low level input voltage (2)	V_{IL2}		$\overline{RESET}$, $\overline{TEST}$	0		0.1·V_{DD}	V
High level input current (1)	I_{IH1}	V_{IH} = 3.0 V Without pull up resistor	K00–K03, K10–K13 K20–K22, P00–P03	0		0.5	µA
High level input current (2)	I_{IH2}	V_{IH} = 3.0 V With pull up resistor	K00–K03, K10–K13 K20–K22, P00–P03 $\overline{RESET}$, $\overline{TEST}$			0.5	µA
Low level input current (1)	I_{IL1}	V_{IL} = V_{SS} Without pull up resistor	K00–K03, K10–K13 K20–K22, P00–P03 $\overline{RESET}$, $\overline{TEST}$	-0.5		0	µA
Low level input current (2)	I_{IL2}	V_{IL} = V_{SS} With pull up resistor	K00–K03, K10–K13 K20–K22, P00–P03 $\overline{RESET}$, $\overline{TEST}$	-20	-10	-5	µA
High level output current (1)	I_{OH1}	V_{OH1} = 0.9·V_{DD}	R00–R03, R10–R13 P00–P03			-1	mA
High level output current (2)	I_{OH2}	V_{OH2} = 0.9·V_{DD}	$\overline{DP}$, $\overline{TMUTE}$, $\overline{RMUTE}$			-1	mA
Low level output current (1)	I_{OL1}	V_{OL1} = 0.1·V_{DD}	R00–R03, R10–R13 P00–P03	3			mA
Low level output current (2)	I_{OL2}	V_{OL2} = 0.1·V_{DD}	$\overline{DP}$, $\overline{TMUTE}$, $\overline{RMUTE}$	3			mA
Common output current	I_{OH3}	V_{OH3} = V_{C3} - 0.05 V	COM0~3			-3	µA
	I_{OL3}	V_{OL3} = V_{SS} + 0.05 V		3			µA
Segment output current (during LCD output)	I_{OH4}	V_{OH4} = V_{C3} - 0.05 V	SEG0~31			-3	µA
	I_{OL4}	V_{OL4} = V_{SS} + 0.05 V		3			µA
Segment output current (during DC output)	I_{OH5}	V_{OH5} = 0.9·V_{DD}	SEG0~31			-300	µA
	I_{OL5}	V_{OL5} = 0.1·V_{DD}		300			µA

7.4 Analog Characteristics and Consumed Current

If no special requirement

V_{DD} = 3 V, V_{SS} = 0 V, f_{OSC1} = 32.768 kHz, f_{OSC3} = 3.579545 MHz (crystal), C_G = 25 pF, Ta = 25°C, V_{D1}, V_{C1}, V_{C2} and V_{C3} are internal voltage, C1–C5 = 0.1 µF

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
LCD drive voltage	V_{C1}	V_{CA} = V_{C1} Connect 1MΩ load resistor between V_{SS} and V_{C1} (without panel load)		0.95	1.05	1.15	V
	V_{C2}	Connect 2MΩ load resistor between V_{SS} and V_{C2} (without panel load)		$2 \cdot V_{C1}$ x 0.9		$2 \cdot V_{C1}$ + 0.1	V
	V_{C3}	Connect 3MΩ load resistor between V_{SS} and V_{C3} (without panel load)		$3 \cdot V_{C1}$ x 0.9		$3 \cdot V_{C1}$ + 0.1	V
SVD voltage	V_{SVD}			1.65	1.8	1.95	V
SVD circuit response time	t_{SVD}					100	µS
Power current consumption	I_{OP}	During HALT (32 kHz)	Without panel load		2	5	µA
		During execution (32 kHz) *1			5	12	µA
		During execution (3.58 MHz) *1			200	500	µA
		During execution (3.58 MHz) *2			1.3	4	mA

*1 The SVD and DTMF generator are OFF status.

*2 The DTMF generator is ON status. The SVD is OFF status.

7.5 Oscillation Characteristics

The oscillation characteristics change depending on the conditions (components used, board pattern, etc.). Use the following characteristics as reference values.

OSC1 crystal oscillation circuit

If no special requirement

V_{DD} = 3 V, V_{SS} = 0 V, Crystal: C-002R (CI = 35 kΩ), C_G = 25 pF, C_D = built-in, Ta = 25°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start voltage	Vsta	tsta ≤ 3 sec	1.6			V
Oscillation stop voltage	Vstp	tstp ≤ 10 sec	1.6			V
Built-in capacitance (drain)	C_D	Including the parasitic capacitance inside the IC		18.5		pF
Frequency/voltage deviation	f/V	V_{DD} = 2 to 5.5 V			5	ppm
Frequency/IC deviation	f/IC		-10		10	ppm
Frequency adjustment range	f/C_G	C_G = 5 to 25 pF	35			ppm
Harmonic oscillation start voltage	Vhho	C_G = 5 pF			5.5	V
Permitted leak resistance *	Rleak	Between OSC1 and V_{SS}	200			MΩ

* The shielding plate for OSC1 and OSC2 should be connected to V_{SS}.

OSC3 crystal oscillation circuit

If no special requirement

V_{DD} = 3 V, V_{SS} = 0 V, Crystal: CA-301, C_G = 5 pF, C_D = built-in, Ta = 25°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start voltage	Vsta	tsta ≤ 30 msec	1.6			V
Oscillation stop voltage	Vstp	tstp ≤ 10 sec	1.6			V
Built-in capacitance (drain)	C_D	Including the parasitic capacitance inside the IC		14		pF
Frequency/voltage deviation	f/V	V_{DD} = 2 to 5.5 V			5	ppm
Frequency/IC deviation	f/IC		-10		10	ppm
Frequency adjustment range	f/C_G	C_G = 5 to 55 pF		35		ppm
Harmonic oscillation start voltage	Vhho	C_G = 5 pF			5.5	V
Permitted leak resistance	Rleak	Between OSC3 and V_{DD}, V_{SS}	200			MΩ

OSC3 ceramic oscillation circuit

If no special requirement

V_{DD} = 3 V, V_{SS} = 0 V, Ceramic oscillator: 3.579545 MHz, C_{GC} = C_{DC} = 30 pF, R_F = 1 MΩ, Ta = 25°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start voltage	Vsta		2.0			V
Oscillation start time	tsta				3	ms
Oscillation stop voltage	Vstp		2.0			V

7.6 Telephone Function Characteristics

If no special requirement

V_{DD} = 3 V, V_{SS} = 0 V, f_{OSC1} = 32.768 kHz, f_{OSC3} = 3.579545 MHz, Ta = 25°C, V_{D1}, V_{C1}, V_{C2} and V_{C3} are internal voltage, C1–C5 = 0.1 µF

Item	Symbol	Condition					Min.	Typ.	Max.	Unit
Flash time	t_{FL}		FTS3	FTS2	FTS1	FTS0		–		ms
			0	0	0	1		94		
			0	0	1	0		188		
			0	0	1	1		281		
			0	1	0	0		375		
			0	1	0	1		469		
			0	1	1	0		563		
			0	1	1	1		656		
			1	0	0	0		750		
			1	0	0	1		844		
			1	0	1	0		938		
			1	0	1	1		1031		
			1	1	0	0		1125		
			1	1	0	1		1219		
			1	1	1	0		1313		
			1	1	1	1		1406		
Flash pause time	t_{FLP}							938		ms
Pause time	t_{PS}		PTS3	PTS2	PTS1	PTS0		–		sec
			0	0	0	1		1		
			0	0	1	0		2		
			0	0	1	1		3		
			0	1	0	0		4		
			0	1	0	1		5		
			0	1	1	0		6		
			0	1	1	1		7		
			1	0	0	0		8		
			1	0	0	1		9		
			1	0	1	0		10		
			1	0	1	1		11		
			1	1	0	0		12		
			1	1	0	1		13		
			1	1	1	0		14		
			1	1	1	1		15		
Mute hold-time	t_{MH}						–	4	–	ms
Inter-digit pause time	t_{IDP}		IDP3	IDP2	IDP1	IDP0		–		ms
			0	0	0	1		94		
			0	0	1	0		188		
			0	0	1	1		281		
			0	1	0	0		375		
			0	1	0	1		469		
			0	1	1	0		563		
			0	1	1	1		656		
			1	0	0	0		750		
			1	0	0	1		844		
			1	0	1	0		938		
			1	0	1	1		1031		
			1	1	0	0		1125		
			1	1	0	1		1219		
			1	1	1	0		1313		
			1	1	1	1		1406		

If no special requirement

V_{DD} = 3 V, V_{SS} = 0 V, f_{OSC1} = 32.768 kHz, f_{OSC3} = 3.579545 MHz, Ta = 25°C, V_{D1}, V_{C1}, V_{C2} and V_{C3} are internal voltage, C1–C5 = 0.1 µF

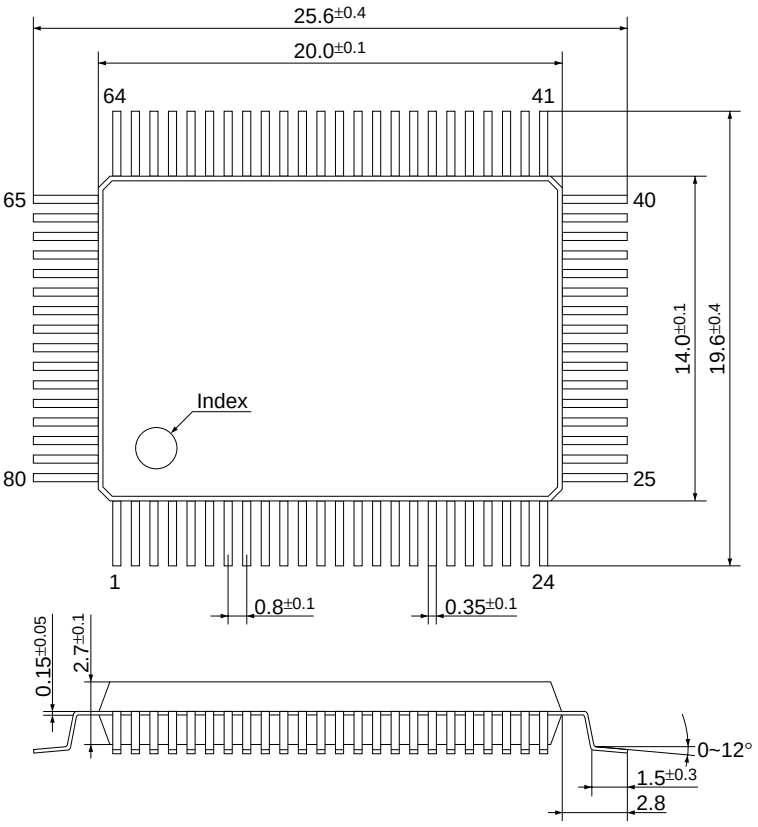
Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Make/Break ratio	M/B	Software–selected	–	1/2 2/3	–	–
Dialing pulse rate	DR	Software–selected	–	10 20	–	pps
Make time	t_M	10 pps, M/B = 1/2	–	33.2	–	ms
		20 pps, M/B = 1/2	–	16.6	–	
		10 pps, M/B = 2/3	–	39.1	–	
		20 pps, M/B = 2/3	–	19.5	–	
Break time	t_B	10 pps, M/B = 1/2	–	66.4	–	ms
		20 pps, M/B = 1/2	–	33.2	–	
		10 pps, M/B = 2/3	–	58.6	–	
		20 pps, M/B = 2/3	–	29.3	–	
Tone output DC level	V_{TDC}		–	0.5(V_{DD}-V_{SS})	–	V
Single Row tone output amplitude	V_R	V_{DD} = 3 V, R_L = 10 kΩ	–	92	–	mVrms
		V_{DD} = 5.5 V, R_L = 10 kΩ	–	168	–	mVrms
Single Column tone output amplitude	V_C	V_{DD} = 3 V, R_L = 10 kΩ	–	122	–	mVrms
		V_{DD} = 5.5 V, R_L = 10 kΩ	–	224	–	mVrms
Tone output voltage ratio	dB_{CR}	V_{DD} = 3 V, R_L = 10 kΩ	–	2.5	–	dB
		V_{DD} = 5.5 V, R_L = 10 kΩ	–	2.5	–	dB
Tone load impedance	R_{TL}	V_{DD} = 2 to 5.5 V	7	–	–	kΩ
Total harmonic distortion	THD	V_{DD} = 2 to 5.5 V, R_L = 10 kΩ	–	–	6	%
Tone output frequency	f_{ROW1}		–	701.32	–	Hz
	f_{ROW2}		–	771.45	–	
	f_{ROW3}		–	857.17	–	
	f_{ROW4}		–	935.10	–	
	f_{COL1}		–	1215.88	–	
	f_{COL2}		–	1331.68	–	
	f_{COL3}		–	1471.85	–	
	f_{COL4}		–	1645.01	–	
Tone duration time	t_{TD}		94	–	–	ms
Tone inter-digit pause	t_{TIP}		–	94	–	ms
Maximum dial rate	t_T	t_{TD} + t_{TIP}	188	–	–	ms

CHAPTER 8 PACKAGE

8.1 Plastic Package

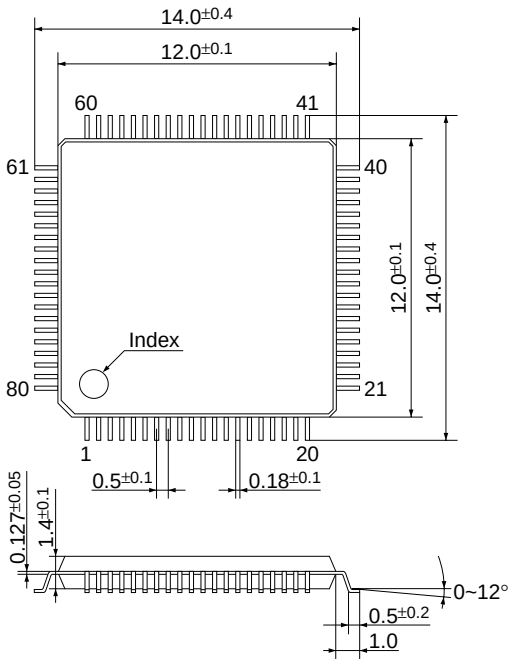
QFP5-80pin

(Unit: mm)



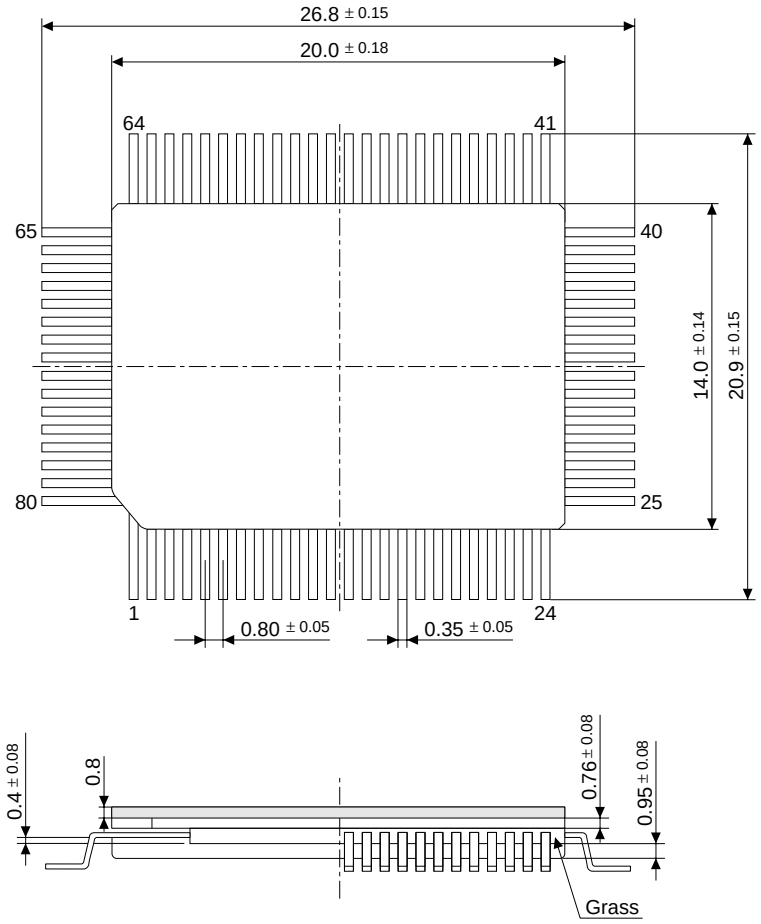
QFP14-80pin

(Unit: mm)



8.2 Ceramic Package for Test Samples

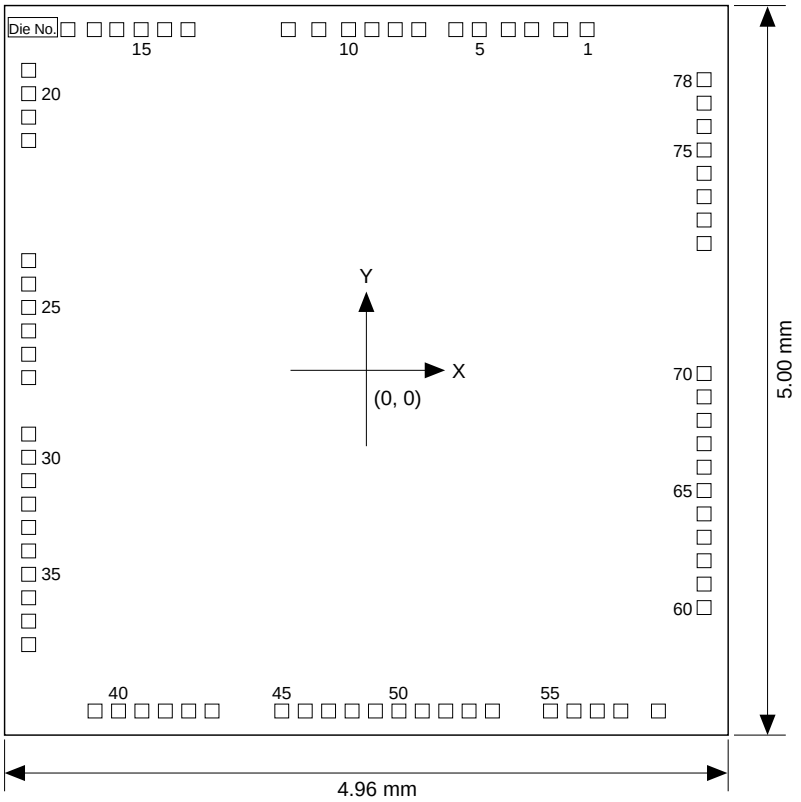
(Unit: mm)



Note: *The ceramic package is fixed in this form regardless selecting of the plastic package form.*

CHAPTER 9 PAD LAYOUT

9.1 Diagram of Pad Layout



Chip thickness: 400 µm
Pad opening: 95 µm

9.2 Pad Coordinates

PAD		Coordinates		PAD		Coordinates	
No.	Name	X [μm]	Y [μm]	No.	Name	X [μm]	Y [μm]
1	$\overline{\text{RESET}}$	1,513	2,335	40	SEG17	-1,699	-2,335
2	V_{DD}	1,332	2,335	41	SEG18	-1,539	-2,335
3	$\overline{\text{RMUTE}}$	1,133	2,335	42	SEG19	-1,378	-2,335
4	$\overline{\text{TMUTE}}$	973	2,335	43	SEG20	-1,218	-2,335
5	$\overline{\text{DP}}$	774	2,335	44	SEG21	-1,058	-2,335
6	V_{SS}	613	2,335	45	SEG22	-580	-2,335
7	OSC1	359	2,335	46	SEG23	-419	-2,335
8	OSC2	198	2,335	47	SEG24	-259	-2,335
9	OSC3	38	2,335	48	SEG25	-98	-2,335
10	OSC4	-122	2,335	49	SEG26	62	-2,335
11	V_{D1}	-326	2,335	50	SEG27	223	-2,335
12	TONE	-535	2,335	51	SEG28	383	-2,335
13	CA	-1,223	2,335	52	SEG29	544	-2,335
14	CB	-1,383	2,335	53	SEG30	704	-2,335
15	V_{C1}	-1,544	2,335	54	SEG31	864	-2,335
16	V_{CA}	-1,711	2,335	55	P00	1,262	-2,335
17	V_{C3}	-1,865	2,335	56	P01	1,423	-2,335
18	V_{C2}	-2,046	2,335	57	P02	1,583	-2,335
19	COM0	-2,315	2,056	58	P03	1,744	-2,335
20	COM1	-2,315	1,896	59	$\overline{\text{TEST}}$	2,002	-2,335
21	COM2	-2,315	1,735	60	K00	2,315	-1,626
22	COM3	-2,315	1,575	61	K01	2,315	-1,465
23	SEG0	-2,315	752	62	K02	2,315	-1,305
24	SEG1	-2,315	591	63	K03	2,315	-1,144
25	SEG2	-2,315	431	64	K10	2,315	-984
26	SEG3	-2,315	270	65	K11	2,315	-824
27	SEG4	-2,315	110	66	K12	2,315	-664
28	SEG5	-2,315	-50	67	K13	2,315	-503
29	SEG6	-2,315	-437	68	K20	2,315	-343
30	SEG7	-2,315	-596	69	K21	2,315	-182
31	SEG8	-2,315	-756	70	K22	2,315	-22
32	SEG9	-2,315	-917	71	R00	2,315	869
33	SEG10	-2,315	-1,077	72	R01	2,315	1,030
34	SEG11	-2,315	-1,238	73	R02	2,315	1,190
35	SEG12	-2,315	-1,398	74	R03	2,315	1,350
36	SEG13	-2,315	-1,559	75	R10	2,315	1,510
37	SEG14	-2,315	-1,719	76	R11	2,315	1,671
38	SEG15	-2,315	-1,880	77	R12	2,315	1,831
39	SEG16	-1,860	-2,335	78	R13	2,315	1,992

II. E0C62T3 Technical Software

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CHAPTER 1 INTRODUCTION

The E0C62T3 is a single-chip microcomputer made up of the 4-bit core CPU E0C6200A, ROM (3,072 words, 12 bits to a word), RAM (640 words, 4 bits to a word), LCD driver, watchdog timer, time base counter, SVD circuit and DTMF/DP generator.
The E0C62T3 can be applied to telephone set which has feature as DTMF/DP switchable, repertory dial, ON/OFF hook dial, etc.

CHAPTER 2 BLOCK DIAGRAM

The E0C62T3 block diagram is shown in Figure 2.1.

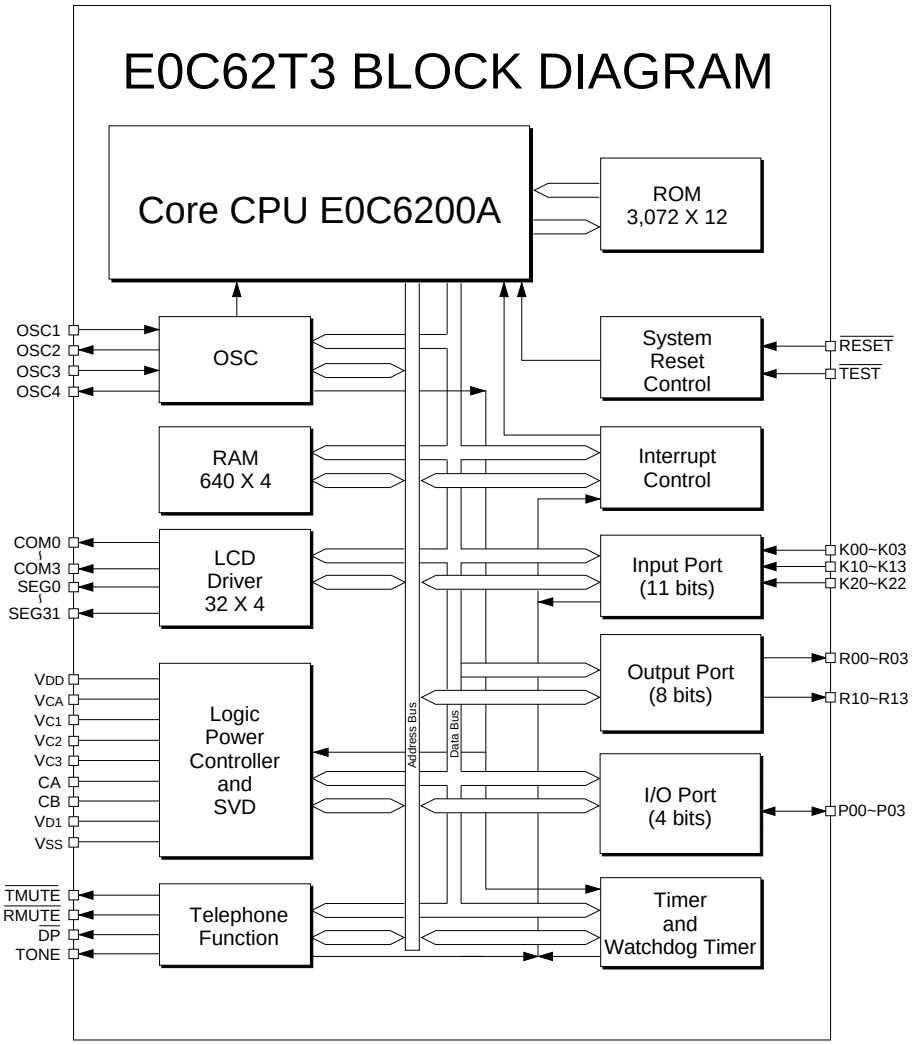


Fig. 2.1
E0C62T3 block
diagram

CHAPTER 3 PROGRAM MEMORY (ROM)

3.1 Configuration of the ROM

E0C62T3 is built-in with 3,072 steps × 12 bits mask ROM for program storage.
The program area is 12 pages (0–11), each 256 steps (00H–FFH). After initial reset, the program beginning address is page 1, step 00H. The interrupt vector is allocated to page 1, steps 02H–0DH. The configuration of the ROM is as shown in Figure 3.1.1.

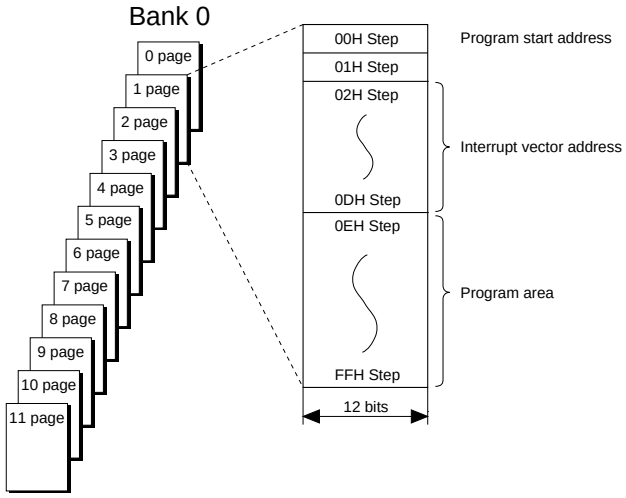


Fig. 3.1.1
Configuration of the ROM

3.2 Interrupt Vector

The interrupt vector and interrupt request correspondence is shown in Table 3.2.1.

Table 3.2.1
Interrupt request and interrupt vector

Interrupt vector (PCP and PCS)	Interrupt request	Priority
102H	Clock timer interrupt	Low
104H	Dialing cycle completion interrupt	↑
106H	Input (K00–K03) interrupt	
108H	Input (K10–K13) interrupt	
10AH	Input (K20–K21) interrupt	↓
10CH	Input (K22) interrupt	High

When multiple interrupts simultaneously occur, the high priority vector address is set to the program counter.

CHAPTER 4 DATA MEMORY

4.1 Configuration of the Data Memory

The data memory consist of 640 words RAM, and I/O memory which controls the peripheral circuit.

Figures 4.1.1(a) and (b) show the configuration of the data memory.

When you make your program, please take note of the following:

(1) Since the stack area is taken from the RAM area, take care that destruction of stack data due to data writing does not occur. Sub-routine calls or interrupts consume 3 words of the stack area.

(2) RAM address 000H–00FH are memory register areas that are addressed with register pointer RP.

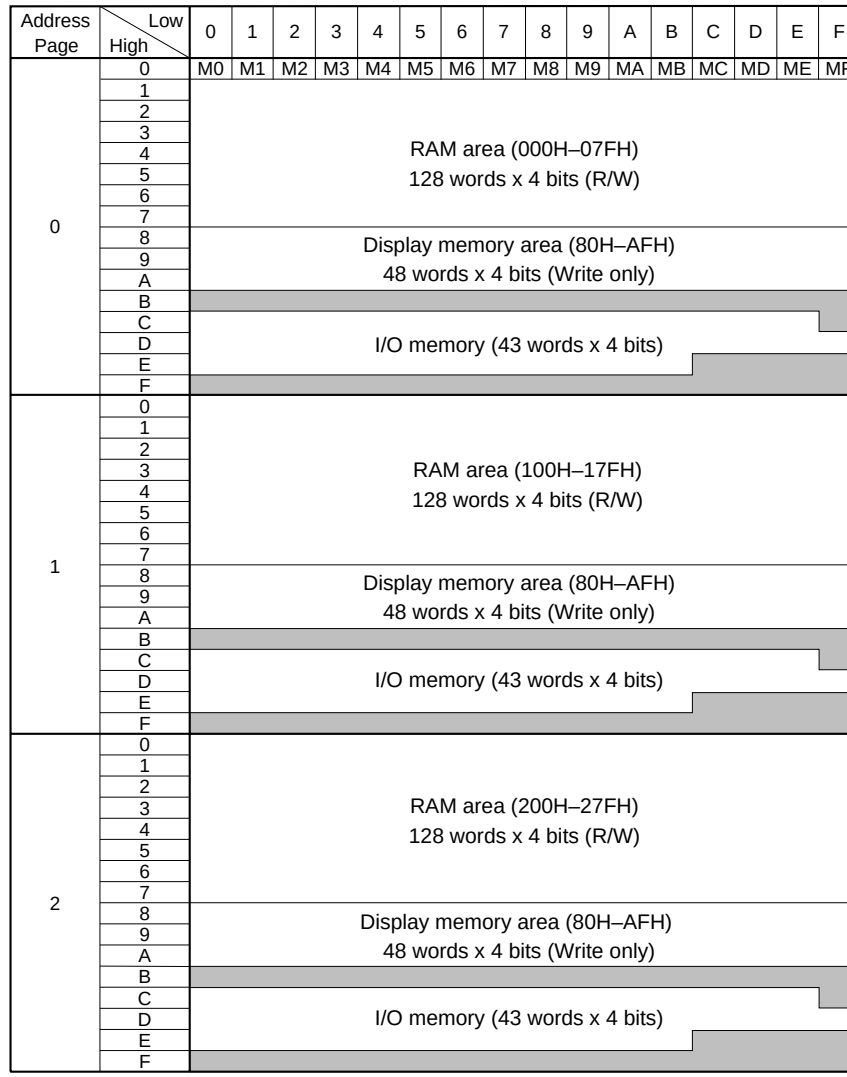


Fig. 4.1.1(a)
Data memory map

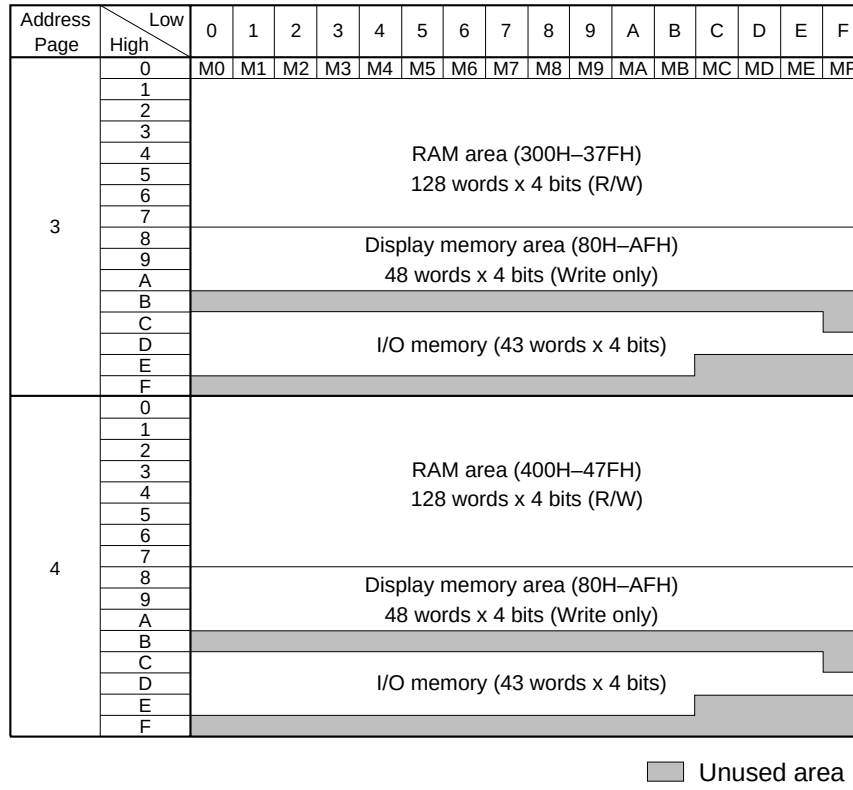


Fig. 4.1.1(b)
Data memory map

Note: *Memory is not mounted in unused area within the memory map and in memory area not indicated in this chapter. For this reason, normal operation cannot be assured for programs that have been prepared with access to these areas.*

4.2 Detail Map of the I/O Memory

Tables 4.2.1(a)–(i) show the detail map of the I/O memory.

Table 4.2.1(a) I/O memory map (C0H–C4H)

Address *6	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
C0H	0	0	0	IK22	0	– *2			Unused *5
	R				0	– *2			Unused *5
					0	– *2			Unused *5
					IK22	0	Yes	No	Interrupt factor flag (K22) Clear to 0 after read out
C1H	0	0	0	IK2	0	– *2			Unused *5
	R				0	– *2			Unused *5
					0	– *2			Unused *5
					IK2	0	Yes	No	Interrupt factor flag (K20, K21) Clear to 0 after read out
C2H	0	0	0	IK1	0	– *2			Unused *5
	R				0	– *2			Unused *5
					0	– *2			Unused *5
					IK1	0	Yes	No	Interrupt factor flag (K10 ~ K13) Clear to 0 after read out
C3H	0	0	0	IK0	0	– *2			Unused *5
	R				0	– *2			Unused *5
					0	– *2			Unused *5
					IK0	0	Yes	No	Interrupt factor flag (K00 ~ K03) Clear to 0 after read out
C4H	IT1	IT2	IT16	IT32	IT1	0	Yes	No	Interrupt factor flag (clock timer 1 Hz) Clear to 0 after read out
	R				IT2	0	Yes	No	Interrupt factor flag (clock timer 2 Hz) Clear to 0 after read out
					IT16	0	Yes	No	Interrupt factor flag (clock timer 16 Hz) Clear to 0 after read out
					IT32	0	Yes	No	Interrupt factor flag (clock timer 32 Hz) Clear to 0 after read out

*1 Initial value at initial reset
*2 Not set in the circuit
*3 Undefined
*4 Inhibit state (output port will be set to "1")
*5 Constantly "0" when being read
*6 Page switching in I/O memory is not necessary

Table 4.2.1(b) I/O memory map (C5H–C9H)

Address *6	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
C5H	0	0	0	ID	0	– *2			Unused *5
	R				0	– *2			Unused *5
					0	– *2			Unused *5
					ID	0	Yes	No	Interrupt factor flag (dialing) Clear to 0 after read out
C6H	0	0	SIK21	SIK20	0	– *2			Unused *5
	R		R/W		0	– *2			Unused *5
					SIK21	0	Enable	Disable	Interrupt selection register (K21)
					SIK20	0	Enable	Disable	Interrupt selection register (K20)
C7H	SIK13	SIK12	SIK11	SIK10	SIK13	0	Enable	Disable	Interrupt selection register (K13)
	R/W				SIK12	0	Enable	Disable	Interrupt selection register (K12)
					SIK11	0	Enable	Disable	Interrupt selection register (K11)
					SIK10	0	Enable	Disable	Interrupt selection register (K10)
C8H	SIK03	SIK02	SIK01	SIK00	SIK03	0	Enable	Disable	Interrupt selection register (K03)
	R/W				SIK02	0	Enable	Disable	Interrupt selection register (K02)
					SIK01	0	Enable	Disable	Interrupt selection register (K01)
					SIK00	0	Enable	Disable	Interrupt selection register (K00)
C9H	0	K22	K21	K20	0	– *2			Unused *5
	R				K22	– *2	High	Low	Input port (K20 ~ K22)
					K21	– *2	High	Low	
					K20	– *2	High	Low	

*1 Initial value at initial reset
*2 Not set in the circuit
*3 Undefined
*4 Inhibit state (output port will be set to "1")
*5 Constantly "0" when being read
*6 Page switching in I/O memory is not necessary

Table 4.2.1(c) I/O memory map (CAH–CEH)

Address *6	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
CAH	K13	K12	K11	K10	K13	– *2	High	Low	Input port (K10 ~ K13)
	R				K12	– *2	High	Low	
					K11	– *2	High	Low	
					K10	– *2	High	Low	
CBH	K03	K02	K01	K00	K03	– *2	High	Low	Input port (K00 ~ K03)
	R				K02	– *2	High	Low	
					K01	– *2	High	Low	
					K00	– *2	High	Low	
CCH	0	DFK22	DFK21	DFK20	0	– *2			Unused *5
	R	R/W			DFK22	1	↓	↑	Input comparison register (K20 ~ K22)
					DFK21	1	↓	↑	
					DFK20	1	↓	↑	
CDH	DFK13	DFK12	DFK11	DFK10	DFK13	1	↓	↑	Input comparison register (K10 ~ K13)
	R/W				DFK12	1	↓	↑	
					DFK11	1	↓	↑	
					DFK10	1	↓	↑	
CEH	DFK03	DFK02	DFK01	DFK00	DFK03	1	↓	↑	Input comparison register (K00 ~ K03)
	R/W				DFK02	1	↓	↑	
					DFK01	1	↓	↑	
					DFK00	1	↓	↑	

*1 Initial value at initial reset
*2 Not set in the circuit
*3 Undefined
*4 Inhibit state (output port will be set to "1")
*5 Constantly "0" when being read
*6 Page switching in I/O memory is not necessary

Table 4.2.1(d) I/O memory map (CFH–D3H)

Address *6	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
CFH									Unused
D0H	EIK22	EIK2	EIK1	EIK0	EIK22	0	Enable	Mask	Interrupt mask register (K22)
	R/W				EIK2	0	Enable	Mask	Interrupt mask register (K20, K21)
					EIK1	0	Enable	Mask	Interrupt mask register (K10 ~ K13)
					EIK0	0	Enable	Mask	Interrupt mask register (K00 ~ K03)
D1H	EIT1	EIT2	EIT16	EIT32	EIT1	0	Enable	Mask	Interrupt mask register (clcok timer 1 Hz)
	R/W				EIT2	0	Enable	Mask	Interrupt mask register (clock timer 2 Hz)
					EIT16	0	Enable	Mask	Interrupt mask register (clock timer 16 Hz)
					EIT32	0	Enable	Mask	Interrupt mask register (clock timer 32 Hz)
D2H	0	0	0	EID	0	– *2			Unused *5
	R			R/W	0	– *2			Unused *5
					0	– *2			Unused *5
					EID	0	Enable	Mask	Interrupt mask register (dialing)
D3H	R13	R12	R11	R10	R13	0	High	Low	Output port (R13)
	HFO	HDO	BZ	$\overline{BZ}$	HFO	– *4	– *4	ON	Handfree output (HFO)
					R12	0	High	Low	Output port (R12)
					HDO	– *4	– *4	ON	Hold-line output (HDO)
					R11	0	High	Low	Output port (R11)
					BZ	– *4	– *4	ON	Buzzer output (BZ)
	R/W				R10	0	High	Low	Output port (R10)
					$\overline{BZ}$	– *4	– *4	ON	Buzzer inverted output ($\overline{BZ}$)

*1 Initial value at initial reset
*2 Not set in the circuit
*3 Undefined
*4 Inhibit state (output port will be set to "1")
*5 Constantly "0" when being read
*6 Page switching in I/O memory is not necessary

Table 4.2.1(e) I/O memory map (D4H–D8H)

Address *6	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
D4H	R03	R02	R01	R00	R03	0	High	Low	Output port (R00 ~ R03)
	R/W				R02	0	High	Low	
					R01	0	High	Low	
					R00	0	High	Low	
D5H	IOC3	IOC2	IOC1	IOC0	IOC3	0	Output	Input	I/O control register
	R/W				IOC2	0	Output	Input	
					IOC1	0	Output	Input	
					IOC0	0	Output	Input	
D6H	PUP3	PUP2	PUP1	PUP0	PUP3	0	ON	OFF	Pull up control register
	R/W				PUP2	0	ON	OFF	
					PUP1	0	ON	OFF	
					PUP0	0	ON	OFF	
D7H	P03	P02	P01	P00	P03	1	High	Low	I/O port
	R/W				P02	1	High	Low	
					P01	1	High	Low	
					P00	1	High	Low	
D8H	0	0	CLKCHG	OSCC	0	– *2			Unused *5
	R		R/W		0	– *2			Unused *5
					CLKCHG	0	OSC3	OSC1	CPU system clock switch
					OSCC	0	ON	OFF	OSC3 oscillation ON/OFF

*1 Initial value at initial reset
*2 Not set in the circuit
*3 Undefined
*4 Inhibit state (output port will be set to "1")
*5 Constantly "0" when being read
*6 Page switching in I/O memory is not necessary

Table 4.2.1(f) I/O memory map (D9H–DDH)

Address *6	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
D9H	0	0	0	TMRST	0	– *2			Unused *5
	R			W	0	– *2			Unused *5
					0	– *2			Unused *5
					TMRST	– *2	Reset	Invalid	Clock timer reset *5
DAH	TM3	TM2	TM1	TM0	TM3	– *3			Clock timer data (low-order) 16 Hz
	R				TM2	– *3			Clock timer data (low-order) 32 Hz
					TM1	– *3			Clock timer data (low-order) 64 Hz
					TM0	– *3			Clock timer data (low-order) 128 Hz
DBH	TM7	TM6	TM5	TM4	TM7	– *3			Clock timer data (high-order) 1 Hz
	R				TM6	– *3			Clock timer data (high-order) 2 Hz
					TM5	– *3			Clock timer data (high-order) 4 Hz
					TM4	– *3			Clock timer data (high-order) 8 Hz
DCH	WDON	WDRST	WD1	WD0	WDON	0	ON	OFF	Watchdog timer ON/OFF
	R/W	W	R		WDRST	Reset	Reset	Invalid	Watchdog timer reset *5
					WD1	0			Watchdog timer data 1/4 Hz
					WD0	0			Watchdog timer data 1/2 Hz
DDH	BZR11	BZR10	0	BZFQ	BZR11	0	Buzzer	DC	R11 port output selection
	R/W		R	R/W	BZR10	0	Buzzer (inverted)	DC	R10 port output selection
					0	– *2			Unused *5
					BZFQ	0	2 kHz	4 kHz	Buzzer frequency selection

*1 Initial value at initial reset
*2 Not set in the circuit
*3 Undefined
*4 Inhibit state (output port will be set to "1")
*5 Constantly "0" when being read
*6 Page switching in I/O memory is not necessary

Table 4.2.1(g) I/O memory map (DEH–E2H)

Address *6	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
DEH	LDTY1	LDTY0	0	LCDON	LDTY1	0			LCD drive duty selection 0 : 1/4, 1 : 1/3, 2 : 1/2, 3 : 1/1
	R/W		R	R/W	LDTY0	0			
					0	– *2			Unused *5
					LCDON	0	ON	OFF	LCD display control (LCD display all off)
DFH	0	0	SVDDT	SVDON	0	– *2			Unused *5
	R			R/W	0	– *2			Unused *5
					SVDDT	0	Supply voltage Low	Supply voltage Normal	Supply votage detector data
					SVDON	0	ON	OFF	SVD circuit ON/OFF
E0H	TPS	0	MB	DRS	TPS	0	PULSE	TONE	Tone / pulse mode selection
	R/W	R	R/W		0	– *2			Unused *5
					MB	0	33.3:66.6	40:60	Make : Break ratio selection
					DRS	0	20 pps	10 pps	Dialing pulse rate selection
E1H	PTS3	PTS2	PTS1	PTS0	PTS3	0			Pause time selection 0 : Use inhibited 8 : 8 sec 1 : 1 sec 9 : 9 sec 2 : 2 sec A : 10 sec 3 : 3 sec B : 11 sec 4 : 4 sec C : 12 sec 5 : 5 sec D : 13 sec 6 : 6 sec E : 14 sec 7 : 7 sec F : 15 sec
	R/W				PTS2	1			
					PTS1	0			
	Default value : 4 seconds				PTS0	0			
E2H	FTS3	FTS2	FTS1	FTS0	FTS3	0			Flash time selection 0 : Use inhibited 8 : 750 ms 1 : 94 ms 9 : 844 ms 2 : 188 ms A : 938 ms 3 : 281 ms B : 1031 ms 4 : 375 ms C : 1125 ms 5 : 469 ms D : 1219 ms 6 : 563 ms E : 1313 ms 7 : 656 ms F : 1406 ms
	R/W				FTS2	1			
					FTS1	1			
	Default value : 563 ms				FTS0	0			

*1 Initial value at initial reset
*2 Not set in the circuit
*3 Undefined
*4 Inhibit state (output port will be set to "1")
*5 Constantly "0" when being read
*6 Page switching in I/O memory is not necessary

Table 4.2.1(h) I/O memory map (E3H–E7H)

Address *6	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
E3H	0	HOLD	PAUSE	FLASH	0	– *2			Unused *5
	R	R/W	W		HOLD	0	On	Off	Hold-line function
					PAUSE	0	Yes	No	Pause function *5
					FLASH	0	Yes	No	Flash function *5
E4H	HF	0	0	0	HF	0	Yes	No	Hand free
	R/W	R			0	– *2			Unused *5
					0	– *2			Unused *5
					0	– *2			Unused *5
E5H	IDP3	IDP2	IDP1	IDP0	IDP3	1			Inter-digit pause selection for dial pulse 0 : Use inhibited 8 : 750 ms 1 : 94 ms 9 : 844 ms 2 : 188 ms A : 938 ms 3 : 281 ms B : 1031 ms 4 : 375 ms C : 1125 ms 5 : 469 ms D : 1219 ms 6 : 563 ms E : 1313 ms 7 : 656 ms F : 1406 ms
	R/W				IDP2	0			
	Default value : 750 ms				IDP1	0			
					IDP0	0			
E6H	0	0	SINR	SINC	0	– *2			Unused *5
	R		R/W		0	– *2			Unused *5
					SINR	1	Enable	Disable	DTMF row frequency output enable
					SINC	1	Enable	Disable	DTMF column frequency output enable
E7H	TCD3	TCD2	TCD1	TCD0	TCD3	0			Telephone code for dialing TCD DTMF DP TCD DTMF DP 0 : (R_1C_4) Use inhibited 8 : (R_3C_2) 8 1 : (R_1C_1) 1 9 : (R_3C_3) 9 2 : (R_1C_2) 2 A : (R_4C_2) 10 3 : (R_1C_3) 3 B : (R_4C_3) 11 4 : (R_2C_1) 4 C : (R_4C_1) 12 5 : (R_2C_2) 5 D : (R_2C_4) 13 6 : (R_2C_3) 6 E : (R_4C_4) 14 7 : (R_3C_1) 7 F : (R_3C_4) 15
	R/W				TCD2	0			
					TCD1	0			
					TCD0	0			

*1 Initial value at initial reset
*2 Not set in the circuit
*3 Undefined
*4 Inhibit state (output port will be set to "1")
*5 Constantly "0" when being read
*6 Page switching in I/O memory is not necessary

Table 4.2.1(i) I/O memory map (E8H–EBH)

Address *6	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
E8H	0	0	CRMUT	CTMUT	0	– *2			Unused *5
	R		R/W		0	– *2			Unused *5
					CRMUT	1	Receive mute output	0	Receive mute control
					CTMUT	1	Transmit mute output	0	Transmit mute control
E9H	0	0	0	HSON	0	– *2			Unused *5
	R			R/W	0	– *2			Unused *5
					0	– *2			
					HSON	0	Hook Off	Hook On	Hook switch ON/OFF
EAH	CHFO	CHDO	0	0	CHFO	0	Handfree output	DC	R13 output selection (R13 data register has to be "0")
	R/W		R		CHDO	0	Hold output	DC	R12 output selection (R12 data register has to be "0")
					0	– *2			Unused *5
					0	– *2			Unused *5
EBH	CTO	0	0	0	CTO	0	Continuous tone output ON	Continuous tone output OFF	Tone duration time control
	R/W	R			0	– *2			Unused *5
					0	– *2			Unused *5
					0	– *2			Unused *5
									Unused

*1 Initial value at initial reset
*2 Not set in the circuit
*3 Undefined
*4 Inhibit state (output port will be set to "1")
*5 Constantly "0" when being read
*6 Page switching in I/O memory is not necessary

CHAPTER 5 INITIAL RESET

5.1 Initialized Status

The CPU core and peripheral circuits are initialized by initial resetting as follows:

Table 5.1.1
Initialized status

CPU core			
Name	Symbol	Number of bits	Setting value
Program counter step	PCS	8	00H
Program counter page	PCP	4	1H
New page pointer	NPP	4	1H
Stack pointer	SP	8	Undefined
Index register IX	IX	11	Undefined
Index register IY	IY	11	Undefined
Register pointer	RP	4	Undefined
General-purpose register A	A	4	Undefined
General-purpose register B	B	4	Undefined
Interrupt flag	I	1	0
Decimal flag	D	1	0
Zero flag	Z	1	Undefined
Carry flag	C	1	Undefined

Peripheral circuits		
Name	Number of bits	Setting value
RAM	640 x 4	Undefined
Display memory	32 x 4	Undefined
Other peripheral circuits	–	*1

*1 See Tables 4.2.1(a)–(i)

Note: *Undefined values must be defined by the program.*

5.2 Example Program for the System Initialization

Following program shows the example of the procedure for system initialization.

```
Label    Mnemonic/operand    Comment
;*
;* INITIAL RESET PROGRAM
;*
       ORG    100H
;
       JP     INIT
;
       ORG    110H
;
INIT:
;* INITIALIZE CPU CORE AT THE BEGINNING
;
       RST    F,0000B    ;CLEAR IDZC FLAGS
;
       LD     A,08H      ;SET STACK POINTER TO 080H
       LD     SPH,A
       LD     A,00H
       LD     SPL,A
;
;* CLEAR DATA MEMORY
;
       LD     A,0
CLL0:
       LD     XP,A
       LD     X,00H      ;CLEAR RAMS
CLL1   LBPX   MX,0H      ;
       CP     XH,8       ;CONTINUE TILL 080H
       JP     C,CLL1
       ADD    A,1
       CP     A,5
       JP     C,CLL0
;
;* INITIALIZE PERIPHERAL CIRCUITS
;
RSTCM:
       LD     X,0D9H     ;RESET CLOCK TIMER
       OR     MX,0001B
;      :
```

5.3 Programming Note for the System Initialization

In some of initial registers and initial data memory area, the initial value is undefined after reset. Set them proper initial values by the program, as necessary.

CHAPTER 6 PERIPHERAL CIRCUITS

6.1 Watchdog Timer

I/O data memory of the watchdog timer

The control registers of the watchdog timer is shown in Table 6.1.1.

Table 6.1.1 Control registers of watchdog timer

Address *6	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
D9H	0	0	0	TMRST	0	– *2			Unused *5
	R			W	0	– *2			Unused *5
					0	– *2			Unused *5
					TMRST	– *2	Reset	Invalid	Clock timer reset *5
DCH	WDON	WDRST	WD1	WD0	WDON	0	ON	OFF	Watchdog timer ON/OFF
	R/W	W	R		WDRST	Reset	Reset	Invalid	Watchdog timer reset *5
					WD1	0			Watchdog timer data 1/4 Hz
					WD0	0			Watchdog timer data 1/2 Hz

*1 Initial value at initial reset
*2 Not set in the circuit
*3 Undefined
*4 Inhibit state (output port will be set to "1")
*5 Constantly "0" when being read
*6 Page switching in I/O memory is not necessary

Control of the watchdog timer

The watchdog timer can be turned ON or OFF by writing "1" or "0" to WDON.

The watchdog timer must be reset cyclically by the software if the WDON is "1". If reset is not executed in at least 3 or 4 seconds, the initial reset signal is output automatically for the CPU.

When "1" is written to WDRST, the watchdog timer is reset, and the operation restarts immediately after this. When "0" is written to WDRST, no operation results.
When "1" is written to TMRST, the watchdog timer is reset, same as the case of WDRST.

The watchdog timer operates in the halt mode. If the halt status continues for 3 seconds, the initial reset signal restarts operation.

Example program for the watchdog timer

Following program shows the reset procedure for watchdog timer.

```
Label    Mnemonic/operand    Comment
;*
;* RESET WATCHDOG TIMER
;*
ZWDOG   EQU    0DCH      ;WATCHDOG ADDRESS
WDON    EQU    1000B     ;WATCHDOG ON/OFF BIT
WDRST   EQU    0100B     ;WATCHDOG RESET BIT
;
;*
;* AT INITIAL ROUTINE SET WATCHDOG TIMER ON
;*
INIT:
;       :
        LD     X,ZWDOG   ;SET WATCHDOG ADDRESS
        OR     MX,WDON   ;SET WATCHDOG ON
;       :
;
;*
;* AT MAIN ROUTINE RESET THE WATCHDOG TIMER WITHIN 3 SECONDS
;*
MAIN:
;       :
        LD     X,ZWDOG   ;SET WATCHDOG ADDRESS
        OR     MX,WDRST  ;RESET WATCHDOG TIMER
;       :
        JP     MAIN
;
```

Programming notes

(1) The watchdog timer must reset within 3-second cycles by the software. In this case, timer data (WD1 and WD0) cannot be used for timer applications.

(2) When clock timer resetting (TMRST←"1") is performed, the watchdog timer is also reset.

6.2 OSC3

E0C62T3 has two built-in oscillation circuits (OSC1 and OSC3).

I/O data memory of the OSC3

The control registers of the OSC3 are shown in Table 6.2.1.

Table 6.2.1 Control registers of OSC3

Address *6	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
D8H	0	0	CLKCHG	OSCC	0	– *2			Unused *5
	R		R/W		0	– *2			Unused *5
					CLKCHG	0	OSC3	OSC1	CPU system clock switch
					OSCC	0	ON	OFF	OSC3 oscillation ON/OFF

*1 Initial value at initial reset
*2 Not set in the circuit
*3 Undefined
*4 Inhibit state (output port will be set to "1")
*5 Constantly "0" when being read
*6 Page switching in I/O memory is not necessary

Control of the OSC3

When processing of the E0C62T3 requires high-speed operations, the CPU's operating clock should be switched from OSC1 to OSC3.

When the E0C62T3's CPU clock is to be OSC3, first set OSCC to "1" (OSC3 oscillation goes ON), and then, after about 5 msec, set CLKCHG to "1" (switching from OSC1 to OSC3).
When switching the clock from OSC3 to OSC1, first set CLKCHG to "0", and then set OSCC to "0". In this case, use a separate instruction for switching the clock and OSC3 OFF.
When DTMF is used, OSC3 also should be turned on firstly, but no need change CPU clock to OSC3.

Example program for the OSC3

Following program shows the oscillation clock controlling procedure.

```
Label    Mnemonic/operand   Comment
;*
;* OSC3 CLOCK CONTROL
;*
ZOSCC  EQU    0D8H      ;CPU CLOCK CONTROL
CLKCHG EQU    0010B     ;CPU SYSTEM CLOCK SWITCH
OSCC   EQU    0001B     ;OSC3 OSCILLATION ON/OFF
;
OS3:
;* CHANGE CLOCK FREQUENCY FROM OSC1 TO OSC3
       LD     X,ZOSCC   ;SET OSC3 ON
       OR     MX,OSCC
;
       LD     A,0EH     ;WAIT 5mS
OS3DLP:
       ADD    A,0FH
       JP     NZ,OS3DLP
;
       OR     MX,CLKCHG ;CHANGE CLOCK TO OSC3
       RET
;
OS1:
;* CHANGE CLOCK FREQUENCY FROM OSC3 TO OSC1
       LD     X,ZOSCC   ;CHANGE CLOCK TO OSC1
       AND    MX,(NOT CLKCHG) AND 0FH
;
       AND    MX,(NOT OSCC) AND 0FH
                        ;SET OSC3 TO OFF
       RET
;
```

Programming notes

(1) It takes at least 5 msec from the time the OSC3 oscillation circuit goes ON until the oscillation stabilizes. Consequently, when switching the CPU operation clock from OSC1 to OSC3, do this after a minimum of 5 msec have elapsed since the OSC3 oscillation went ON.
Further, the oscillation stabilization time varies depending on the external oscillator characteristics and conditions of use, so allow ample margin when setting the wait time.

(2) When switching the clock from OSC3 to OSC1, use a separate instruction for switching the OSC3 oscillation OFF. An error in the CPU operation can result if this processing is performed at the same time by the one instruction.

(3) To lessen current consumption, keep OSC3 oscillation OFF except when the CPU must be run at high speed, or when DTMF is used.

6.3 Input Ports (K00–K03, K10–K13, K20–K22)

I/O data memory of the input ports

The control registers of the input ports are shown in Tables 6.3.1(a)–(c).

Table 6.3.1(a) Control registers of input ports

Address *6	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
C0H	0	0	0	IK22	0	– *2			Unused *5
	R				0	– *2			Unused *5
					0	– *2			Unused *5
					IK22	0	Yes	No	Interrupt factor flag (K22) Clear to 0 after read out
C1H	0	0	0	IK2	0	– *2			Unused *5
	R				0	– *2			Unused *5
					0	– *2			Unused *5
					IK2	0	Yes	No	Interrupt factor flag (K20, K21) Clear to 0 after read out
C2H	0	0	0	IK1	0	– *2			Unused *5
	R				0	– *2			Unused *5
					0	– *2			Unused *5
					IK1	0	Yes	No	Interrupt factor flag (K10 ~ K13) Clear to 0 after read out
C3H	0	0	0	IK0	0	– *2			Unused *5
	R				0	– *2			Unused *5
					0	– *2			Unused *5
					IK0	0	Yes	No	Interrupt factor flag (K00 ~ K03) Clear to 0 after read out
C6H	0	0	SIK21	SIK20	0	– *2			Unused *5
	R		R/W		0	– *2			Unused *5
					SIK21	0	Enable	Disable	Interrupt selection register (K21)
					SIK20	0	Enable	Disable	Interrupt selection register (K20)

*1 Initial value at initial reset
*2 Not set in the circuit
*3 Undefined
*4 Inhibit state (output port will be set to "1")
*5 Constantly "0" when being read
*6 Page switching in I/O memory is not necessary

Table 6.3.1(b) Control registers of input ports

Address *6	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
C7H	SIK13	SIK12	SIK11	SIK10	SIK13	0	Enable	Disable	Interrupt selection register (K13)
	R/W				SIK12	0	Enable	Disable	Interrupt selection register (K12)
					SIK11	0	Enable	Disable	Interrupt selection register (K11)
					SIK10	0	Enable	Disable	Interrupt selection register (K10)
C8H	SIK03	SIK02	SIK01	SIK00	SIK03	0	Enable	Disable	Interrupt selection register (K03)
	R/W				SIK02	0	Enable	Disable	Interrupt selection register (K02)
					SIK01	0	Enable	Disable	Interrupt selection register (K01)
					SIK00	0	Enable	Disable	Interrupt selection register (K00)
C9H	0	K22	K21	K20	0	– *2			Unused *5
	R				K22	– *2	High	Low	Input port (K20 ~ K22)
					K21	– *2	High	Low	
					K20	– *2	High	Low	
CAH	K13	K12	K11	K10	K13	– *2	High	Low	
	R				K12	– *2	High	Low	Input port (K10 ~ K13)
					K11	– *2	High	Low	
					K10	– *2	High	Low	
CBH	K03	K02	K01	K00	K03	– *2	High	Low	
	R				K02	– *2	High	Low	Input port (K00 ~ K03)
					K01	– *2	High	Low	
					K00	– *2	High	Low	

*1 Initial value at initial reset
*2 Not set in the circuit
*3 Undefined
*4 Inhibit state (output port will be set to "1")
*5 Constantly "0" when being read
*6 Page switching in I/O memory is not necessary

Table 6.3.1(c) Control registers of input ports

Address *6	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
CCH	0	DFK22	DFK21	DFK20	0	– *2			Unused *5
	R	R/W			DFK22	1	↓	↑	
					DFK21	1	↓	↑	Input comparison register (K20 ~ K22)
					DFK20	1	↓	↑	
CDH	DFK13	DFK12	DFK11	DFK10	DFK13	1	↓	↑	
	R/W				DFK12	1	↓	↑	
					DFK11	1	↓	↑	Input comparison register (K10 ~ K13)
					DFK10	1	↓	↑	
CEH	DFK03	DFK02	DFK01	DFK00	DFK03	1	↓	↑	
	R/W				DFK02	1	↓	↑	
					DFK01	1	↓	↑	Input comparison register (K00 ~ K03)
					DFK00	1	↓	↑	
D0H	EIK22	EIK2	EIK1	EIK0	EIK22	0	Enable	Mask	Interrupt mask register (K22)
	R/W				EIK2	0	Enable	Mask	Interrupt mask register (K20, K21)
					EIK1	0	Enable	Mask	Interrupt mask register (K10 ~ K13)
					EIK0	0	Enable	Mask	Interrupt mask register (K00 ~ K03)

*1 Initial value at initial reset
*2 Not set in the circuit
*3 Undefined
*4 Inhibit state (output port will be set to "1")
*5 Constantly "0" when being read
*6 Page switching in I/O memory is not necessary

Control of the input ports

Reading of input data

Input data of the input port terminal may be read out with registers K00–K03, K10–K13 and K20–K22. The terminal voltage of 11 bits input ports are each reading as "1" and "0" at high (V_{DD}) level and low (V_{SS}) level, respectively.

Input interrupt (K00–K03)

The input interrupt timing of K00–K03 can be set to generate interrupt at the rising edge or falling edge of the input by the setting of input comparison registers DFK00–DFK03. When DFK register is set to "1", the falling edge of the input becomes an interrupt generating condition, the rising edge when set to "0". Moreover, the interrupt mask can be set with the interrupt mask register EIK0. And each K00–K03 inputs interrupt can be selected by the interrupt selection registers SIK00–SIK03. So if you want enable interrupt, for example K03, set EIK0 and SIK03 to "1". However, if the interrupt of any one of K00–K03 is enabled, interrupt will be generated when the content change from matched to no matched with the input comparison register.
When interrupt is generated, the interrupt factor flag IK0 is set to "1".
Figure 6.3.1 shows an example of an interrupt for K00–K03.

Input interrupt (K10–K13)

The input interrupt timing of K10–K13 can be set to generate interrupt at the rising edge or falling edge of the input by the setting of input comparison registers DFK10–DFK13. When DFK register is set to "1", the falling edge of the input becomes an interrupt generating condition, the rising edge when set to "0". Moreover, the interrupt mask can be set with the interrupt mask register EIK1. And each K10–K13 inputs interrupt can be selected by the interrupt selection registers SIK10–SIK13. So if you want enable interrupt, for example K13, set EIK1 and SIK13 to "1". However, if the interrupt of any one of K10–K13 is enabled, interrupt will be generated when the content change from matched to no matched with the input comparison register.
When interrupt is generated, the interrupt factor flag IK1 is set to "1".
Figure 6.3.2 shows an example of an interrupt for K10–K13.

Input interrupt (K20–K21)

The input interrupt timing of K20–K21 can be set to generate interrupt at the rising edge or falling edge of the input by the setting of input comparison registers DFK20–DFK21. When DFK register is set to "1", the falling edge of the input becomes an interrupt generating condition, the rising edge when set to "0". Moreover, the interrupt mask can be set with the interrupt mask register EIK2. And each K20–K21 inputs interrupt can be selected by the interrupt selection registers SIK20–SIK21. So if you want enable interrupt, for example K20, set EIK2 and SIK20 to "1". However, if the interrupt of any one of K20–K21 is enabled, interrupt will be generated when the content change from matched to no matched with the input comparison register.
When interrupt is generated, the interrupt factor flag IK2 is set to "1".
Figure 6.3.3 shows an example of an interrupt for K20–K21.

Input interrupt (K22)

The input interrupt timing of K22 can be set to generate interrupt at the rising edge or falling edge of the input by the setting of input comparison registers DFK22. When DFK22 register is set to "1", the falling edge of the input becomes an interrupt generating condition, the rising edge when set to "0".
The interrupt mask can be selected with the interrupt mask register EIK22. When interrupt is generated, the interrupt factor flag IK22 is set to "1".
Figure 6.3.4 shows an example of an interrupt for K22.

Interrupt mask register

EIK0
1

Interrupt selection register

SIK03	SIK02	SIK01	SIK00
1	1	1	0

Input comparison register

DFK03	DFK02	DFK01	DFK00
1	0	1	0

With the above setting, the interrupt of K00–K03 is generated under the following condition :

Input ports

(1)

K03	K02	K01	K00
1	0	1	0

(Initial value)

↓

(2)

K03	K02	K01	K00
1	0	1	1

↓

(3)

K03	K02	K01	K00
0	0	1	1

→ Interrupt generation
Because K00 is masked, interrupt will be generated when no matching occurs between the contents of the 3 bits K01–K03 and the 3 bits input comparison registers DFK01–DFK03.

Fig. 6.3.1
Example of an interrupt for K00–K03

Interrupt mask register

EIK1
1

Interrupt selection register

SIK13	SIK12	SIK11	SIK10
1	1	0	1

Input comparison register

DFK13	DFK12	DFK11	DFK10
1	0	1	1

With the above setting, the interrupt of K10–K13 is generated under the following condition :

Input ports

(1)

K13	K12	K11	K10
1	0	1	1

(Initial value)

↓

(2)

K13	K12	K11	K10
1	0	0	1

↓

(3)

K13	K12	K11	K10
1	0	0	0

→ Interrupt generation
Because K11 is masked, interrupt will be generated when no matching occurs between the contents of the 3 bits (K13, K12, K10) and the 3 bits input comparison registers (DFK13, DFK12, DFK10).

Fig. 6.3.2
Example of an interrupt for K10–K13

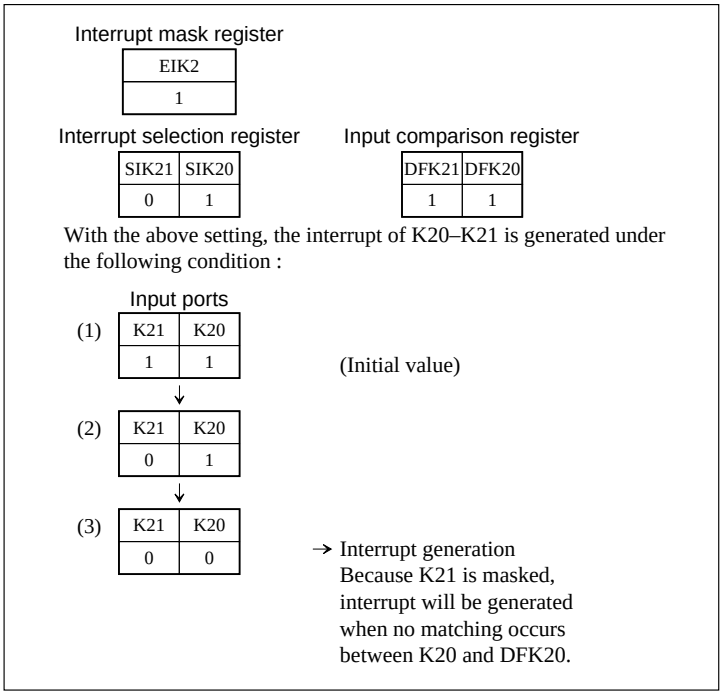


Fig. 6.3.3
Example of an interrupt for K20–K21

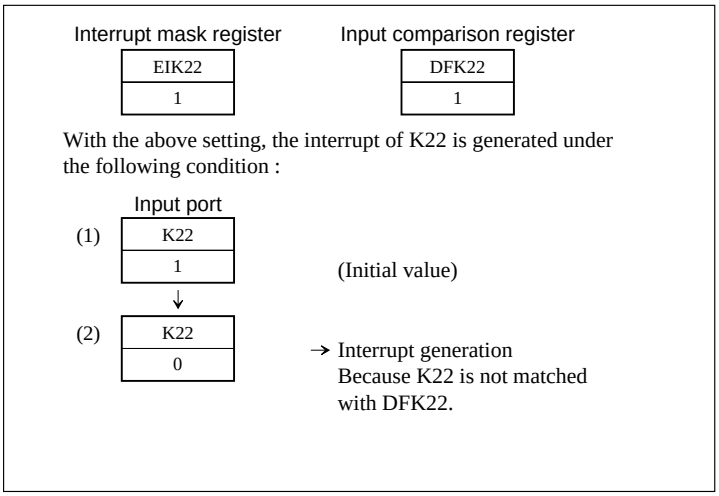


Fig. 6.3.4
Example of an interrupt for K22

Example program for the input ports

Following program shows the input ports controlling procedure.

```
Label   Mnemonic/operand   Comment
;*
;* INPUT PORT
;*
ZIK22   EQU    0C0H      ;K22     INTERRUPT FACTOR FLAG
ZIK2    EQU    0C1H      ;K20-K21 INTERRUPT FACTOR FLAG
ZIK1    EQU    0C2H      ;K10-K13 INTERRUPT FACTOR FLAG
ZIK0    EQU    0C3H      ;K00-K03 INTERRUPT FACTOR FLAG
ZSIK2   EQU    0C6H      ;K20-K21 INTERRUPT SELECTION REGISTER
ZSIK1   EQU    0C7H      ;K10-K13 INTERRUPT SELECTION REGISTER
ZSIK0   EQU    0C8H      ;K00-K03 INTERRUPT SELECTION REGISTER
ZK2     EQU    0C9H      ;K20-K22 INPUT PORT
ZK1     EQU    0CAH      ;K10-K13 INPUT PORT
ZK0     EQU    0CBH      ;K00-K03 INPUT PORT
ZDFK2   EQU    0CCH      ;K20-K22 INPUT COMPARISON REGISTER
ZDFK1   EQU    0CDH      ;K10-K13 INPUT COMPARISON REGISTER
ZDFK0   EQU    0CEH      ;K00-K03 INPUT COMPARISON REGISTER
ZEIK    EQU    0D0H      ;K22,K20-K21,K1,K0
                         ;INTERRUPT MASK REGISTER
;
        ORG    106H
        JP     K0INT     ;K0 INTERRUPT ROUTINE
;
        ORG    108H
        JP     K1INT     ;K1 INTERRUPT ROUTINE
;
        ORG    10AH
        JP     K2INT     ;K2 INTERRUPT ROUTINE
;
        ORG    10CH
        JP     K22INT    ;K22 INTERRUPT ROUTINE
;
INITK:
;* INPUT PORT K0, K1, K20-K21 & K22 INITIAL ROUTINE
;
        LD     X,ZK2     ;INITIALIZE FOR INPUT COMPARISON
        LD     Y,ZDFK2   ; REGISTERS
        LDPY   MY,MX     ;DFK2 <- K2
        INC    X
        LDPY   MY,MX     ;DFK1 <- K1
        INC    X
        LDPY   MY,MX     ;DFK0 <- K0
;
        DI
        LD     X,ZEIK
        LD     MX,1111B  ;ENABLE K0,K1,K20-K21,K22 INPUT INTERRUPT
        LD     X,ZSIK2
        LDPX   MX,03H    ;SELECT K20,K21 INTERRUPT
        LDPX   MX,0FH    ;SELECT K10,K11,K12,K13 INTERRUPT
        LD     MX,0FH    ;SELECT K00,K01,K02,K03 INTERRUPT
;
        LD     X,ZIK22   ;RESET INTERRUPT FACTOR FLAG
        LDPX   A,MX      ;RESET IK22 INTERRUPT FACTOR FLAG
        LDPX   A,MX      ;RESET IK2 INTERRUPT FACTOR FLAG
        LDPX   A,MX      ;RESET IK1 INTERRUPT FACTOR FLAG
        LD     A,MX      ;RESET IK0 INTERRUPT FACTOR FLAG
        EI
        RET
```

```
;
K0INT:
;* K0 INTERRUPT SERVICE ROUTINE
       LD     X,ZIK0    ;READ INTERRUPT FACTOR FLAG
       LD     A,MX
;      :
;      :
       LD     X,ZK0     ;STORE INPUT COMPARISON REGISTER
       LD     Y,ZDFK0
       LD     MY,MX
       EI
       RET
;
K1INT:
;* K1 INTERRUPT SERVICE ROUTINE
       LD     X,ZIK1    ;READ INTERRUPT FACTOR FLAG
       LD     A,MX
;      :
;      :
       LD     X,ZK1     ;STORE INPUT COMPARISON REGISTER
       LD     Y,ZDFK1
       LD     MY,MX
       EI
       RET
;
K2INT:
;* K2 INTERRUPT SERVICE ROUTINE
       LD     X,ZIK2    ;READ INTERRUPT FACTOR FLAG
       LD     A,MX
;      :
;      :
       LD     X,ZK2     ;STORE INPUT COMPARISON REGISTER
       LD     Y,ZDFK2
       LD     MY,MX
       EI
       RET
;
K22INT:
;* K22 INTERRUPT SERVICE ROUTINE
       LD     X,ZIK22   ;READ INTERRUPT FACTOR FLAG
       LD     A,MX
;      :
;      :
       LD     X,ZK2     ;STORE INPUT COMPARISON REGISTER
       LD     Y,ZDFK2
       LD     MY,MX
       EI
       RET
;
```

Programming notes

(1) When input ports are changed from low to high by pull up resistor, the rise of the waveform is delayed on account of the time constant of the pull up resistor and input gate capacitance. Hence, when fetching input ports, set an appropriate wait time.
Particular care needs to be taken of the key scan during key matrix configuration. Aim for a wait time of about 1 msec.

(2) When an interrupt occurs, for example, a key been pressed, software must has the debounce routine, to insure the input port interrupt stable, then to read out the interrupt flag for resetting interrupt flag. If no debounce routine, the input might interrupt many times.

(3) Read the interrupt factor flag in the DI status (interrupt flag = "0"). Reading of interrupt factor flag is available at EI, but be careful in the following cases.
If the interrupt mask register value corresponding to the interrupt factor flags to be read is set to "1", an interrupt request will be generated by the interrupt factor flags set timing, or an interrupt request will not be generated. Be very careful when interrupt factor flags are in the same address.

(4) Writing to the interrupt mask registers can be done only in the DI status (interrupt flag = "0").
Writing during EI status (interrupt flag = "1") will cause malfunction.

6.4 Output Ports (R00–R03, R10–R13)

I/O data memory of the output ports

The control registers of the output ports are shown in Tables 6.4.1(a) and (b).

Table 6.4.1(a) Control registers of output ports

Address *6	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
D3H	R13	R12	R11	R10	R13	0	High	Low	Output port (R13)
					HFO		– *4	ON	Handfree output (HFO)
	HFO	HDO	BZ	$\overline{BZ}$	R12	0	High	Low	Output port (R12)
					HDO		– *4	ON	Hold-line output (HDO)
	R/W				R11	0	High	Low	Output port (R11)
					BZ		– *4	ON	Buzzer output (BZ)
					R10	0	High	Low	Output port (R10)
					$\overline{BZ}$		– *4	ON	Buzzer inverted output ($\overline{BZ}$)
D4H	R03	R02	R01	R00	R03	0	High	Low	Output port (R00 ~ R03)
	R/W				R02	0	High	Low	
					R01	0	High	Low	
					R00	0	High	Low	
DDH	BZR11	BZR10	0	BZFQ	BZR11	0	Buzzer	DC	R11 port output selection
	R/W		R	R/W	BZR10	0	Buzzer (inverted)	DC	R10 port output selection
					0	– *2			Unused *5
					BZFQ	0	2 kHz	4 kHz	Buzzer frequency selection
E3H	0	HOLD	PAUSE	FLASH	0	– *2			Unused *5
	R	R/W	W		HOLD	0	On	Off	Hold – line function
					PAUSE	0	Yes	No	Pause function *5
					FLASH	0	Yes	No	Flash function *5
E4H	HF	0	0	0	HF	0	Yes	No	Hand free
	R/W	R			0	– *2			Unused *5
					0	– *2			Unused *5
					0	– *2			Unused *5

*1 Initial value at initial reset
*2 Not set in the circuit
*3 Undefined
*4 Inhibit state (output port will be set to "1")
*5 Constantly "0" when being read
*6 Page switching in I/O memory is not necessary

Table 6.4.1(b) Control registers of output ports

Address *6	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
EAH	CHFO	CHDO	0	0	CHFO	0	Handfree output	DC	R13 output selection (R13 data register has to be "0")
	R/W		R		CHDO	0	Hold output	DC	R12 output selection (R12 data register has to be "0")
					0	– *2			Unused *5
					0	– *2			Unused *5

*1 Initial value at initial reset
*2 Not set in the circuit
*3 Undefined
*4 Inhibit state (output port will be set to "1")
*5 Constantly "0" when being read
*6 Page switching in I/O memory is not necessary

Control of the general output ports

The E0C62T3 has 8 bits (R00–R03, R10–R13) general output ports built-in.
Output port terminals will generate the data written into the corresponding registers (R00–R03, R10–R13) as it is. The output port terminal goes high (V_{DD}) when "1" is written to the register, and goes low (V_{SS}) when "0" is written. The output ports R00–R03 and R10–R13 are initialized to low level (V_{SS}) after an initial reset. The output ports (R00–R03, R10–R13) can also be read, and output control is possible using the bit operation instruction (AND, OR, etc.).

The output ports R10–R13 are all software programmable for special use output ports as shown in the later of this section. So please set the following registers to "0" when want to use R10–R13 as general output ports.

for R10 port: set BZR10 (DDH•D2) to "0".
for R11 port: set BZR11 (DDH•D3) to "0".
for R12 port: set CHDO (EAH•D2) to "0".
for R13 port: set CHFO (EAH•D3) to "0".

At initial reset, R10–R13 output ports are set to general output ports.

Example program for the general output ports

Following program shows the output ports controlling procedure in ordinary DC output case.

Bit-unit operation of R00–R03 output ports

```
Label    Mnemonic/operand    Comment
;*
;* R00-R03 OUTOUT PORTS
;*
;* BIT-UNIT OPERATION OF R00-R03 OUTPUT PORTS
;
ZR0     EQU    0D4H       ;R0 OUTPUT PORT
;
        LD     Y,ZR0      ;SET OUTPUT PORT ADDRESS
        OR     MY,0010B   ;SET R01 TO "1"
        AND    MY,1011B   ;SET R02 TO "0"
;
```

The three instruction steps above cause the output port to be set, as shown in Figure 6.4.1.

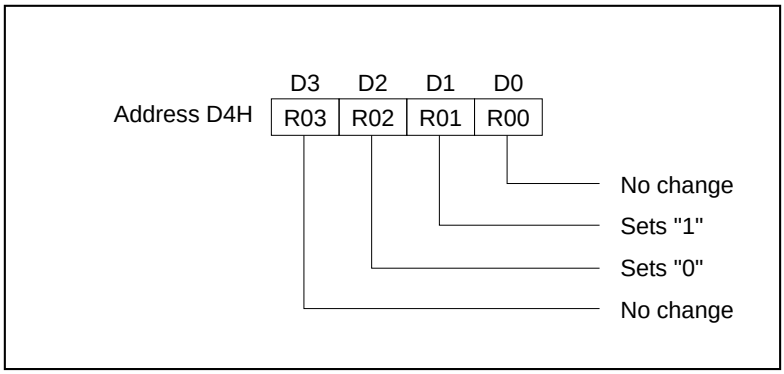


Fig. 6.4.1
Bit-unit operation of R00–R03 output ports

Loading B register data into R10–R13

```
Label     Mnemonic/operand    Comment
;*
;* R10-R13 OUTOUT PORTS
;*
;* LOADING DATA OF B REGISTER TO R10-R13
;
ZR1     EQU    0D3H       ;R1 OUTPUT PORT
ZBZCTL  EQU    0DDH       ;BUZZER CONTROL REGISTER
BZR11   EQU    1000B      ;R11 PORT SELECTION
BZR10   EQU    0100B      ;R10 PORT SELECTION
ZCHFO   EQU    0EAH       ;HANDFREE & HOLD OUTPUT CONTROL REGISTER
CHFO    EQU    1000B      ;R13 PORT SELECTION
CHDO    EQU    0100B      ;R12 PORT SELECTION
;
        LD     X,ZBZCTL   ;DISABLE BUZZER OUTPUT TO R10 & R11
        AND    MX,(NOT BZR11 AND NOT BZR10) AND 0FH
        LD     X,ZCHFO    ;DISABLE HANDFREE
                          ;& HOLD OUTPUT TO R12 & R13
        AND    MX,(NOT CHFO AND NOT CHDO) AND 0FH
;
        LD     X,ZR1      ;SET OUTPUT PORT ADDRESS
        LD     MX,B       ;OUTPUT B REGISTER TO R1 PORT
;
```

As shown in Figure 6.4.2, the above program loads the data of the B register into the output ports.

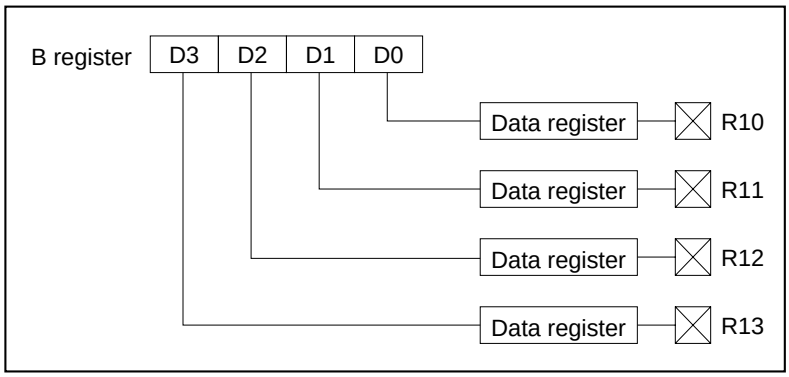


Fig. 6.4.2
Correspondence between output ports (R10–R13) and B register

Control of the special use output ports

In addition to the regular DC output, special output can be selected by software program for output ports (R10–R13), as shown in Table 6.4.2.

Table 6.4.2
Special output

Terminal	Special output	Output selection register
R10	$\overline{BZ}$	BZR10
R11	BZ	BZR11
R12	HDO	CHDO
R13	HFO	CHFO

Figure 6.4.3 shows the structure of output ports (R10–R13).

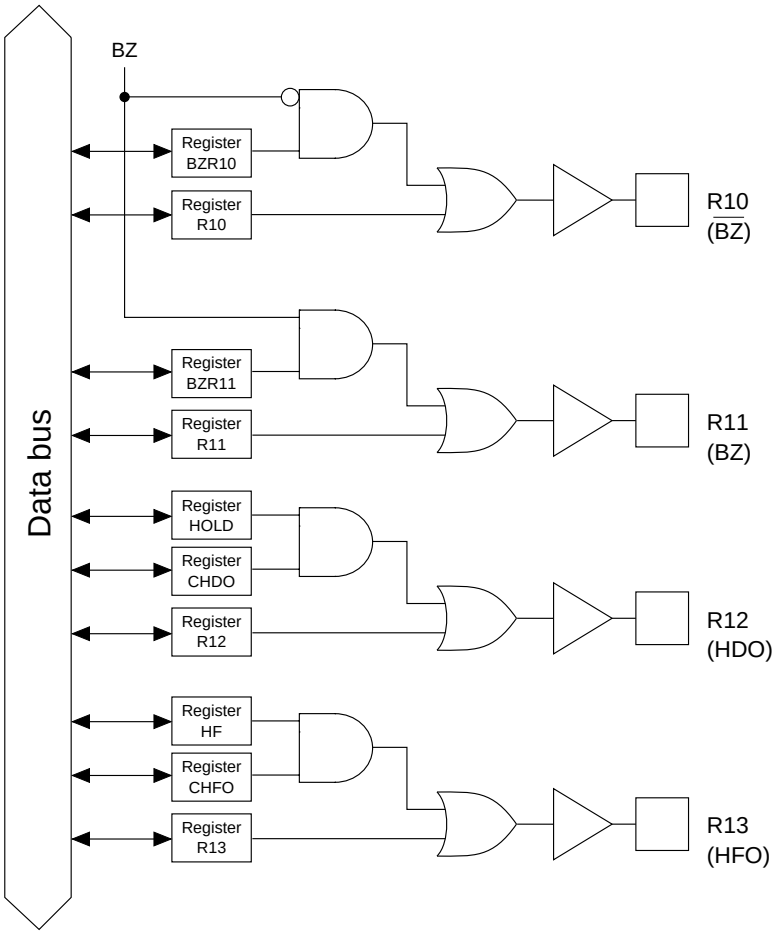


Fig. 6.4.3
Structure of output ports (R10–R13)

Buzzer output (R10 and R11)

The R10/R11 terminal can be controlled to generate $\overline{BZ}$ (buzzer inverted) output/BZ (buzzer) output. By writing R10 register and BZR10 register, software program can control the $\overline{BZ}$ output to R10 terminal. By writing R11 register and BZR11 register, software program can control the BZ output to R11 terminal.
There are two methods can be used for output the buzzer frequency.

method 1:
BZR10 and BZR11 is to select R10 and R11 for $\overline{BZ}$ (buzzer inverted) output and BZ (buzzer) output, respectively. So when you want to use R10 or R11 as buzzer inverted output or buzzer output, set BZR10 or BZR11 to "1" first.
When "0" is set on R11, buzzer signal is generated from R11 terminal. When "1" is set on R11, R11 terminal output goes high (V_{DD}). The R10 control way is the same with R11. But the R10 is output the buzzer inverted signal to the terminal.

method 2:
Writes R10/R11 register to "0", firstly. Then writes BZR10/BZR11 register to "1", the $\overline{BZ}$/BZ output to R10/R11 terminal.
When writing BZR10/BZR11 register to "0", the R10/R11 terminal will go to low level (V_{SS}).

The buzzer frequency may be selected as 2 kHz or 4 kHz by software. When BZFQ (DDH•D0) is set to "0", the frequency of the buzzer signal is set in 4 kHz, and in 2 kHz when "1" is set.

Hold output (R12)

HDO is hold-line signal output for telephone function.
By setting the register CHDO (EAH•D2) to "1", R12 terminal is set to HDO (Hold-line output) output port. At meanwhile, R12 register (D3H•D2) must be set to "0"; otherwise R12 terminal is set to high level (V_{DD}). When CHDO is set to "0", R12 terminal becomes the regular DC output port.
When the HDO output is selected, the R12 terminal outputs the data which is written in the register HOLD (E3H•D2).
See Section 6.9, "Telephone Function" for detail of HDO.

Handfree output (R13)

HFO is handfree signal output for telephone function.
By setting the register CHFO (EAH•D3) to "1", R13 terminal is set to HFO (Handfree output) output port. At meantime, R13 register (D3H•D3) must be set to "0"; otherwise R13 terminal is set to high level (V_{DD}). When CHFO is set to "0", R13 terminal becomes the regular DC output port.
When the HFO output is selected, the R13 terminal outputs the data which is written in the register HF (E4H•D3).
See Section 6.9, "Telephone Function" for detail of HFO.

Example program for the special use output ports

Following program shows the special use output ports controlling procedure.

```
Label    Mnemonic/operand   Comment
;*
;* SPECIAL USE R10-R13 OUTOUT PORT
;*
;
ZR1    EQU    0D3H      ;R1 OUTPUT PORT
ZBZCTL EQU    0DDH      ;BUZZER CONTROL REGISTER
BZR11  EQU    1000B     ;R11 PORT SELECTION
BZR10  EQU    0100B     ;R10 PORT SELECTION
BZFQ   EQU    0001B     ;BUZZER FREQUENCY SELECTION
ZHOLD  EQU    0E3H      ;HOLD, PAUSE, FLASH OUTPUT CONTROL
                        ; ADDRESS
ZHF    EQU    0E4H      ;HANDFREE OUTPUT CONTROL ADDRESS
ZCHFO  EQU    0EAH      ;R13 & R12 TERMINALS SELECTION ADDRESS
;
;*
;* BUZZER OUTPUT
;*
       LD     X,ZR1     ;R10 & R11 BOTH MUST SET TO "0" FOR
       AND    MX,1100B  ; BUZZER OUTPUT
;
       LD     X,ZBZCTL  ;TURN ON R10 & R11 AS BUZZER OUTPUT,
       LD     MX,1100B  ; AND SET FREQUENCY = 4 KHz
;      :
;      :
       LD     X,ZBZCTL  ;TURN OFF R10 & R11 BUZZER OUTPUT
       AND    MX,0011B  ;
;*
;* HOLD-LINE FUNCTION
;*
       LD     X,ZR1     ;R12 MUST SET TO "0"
       AND    MX,1011B  ; FOR HOLD-LINE FUNCTION
;
       LD     X,ZCHFO   ;SET R12 TERMINAL AS HOLD-LINE OUTPUT
       OR     MX,0100B
;
       LD     X,ZHOLD   ;SET HOLD CONTROL ADDRESS
       OR     MX,0100B  ;EXECUTING HOLD-LINE FUNCTION
;      :
;      :
       LD     X,ZHOLD   ;SET HOLD CONTROL ADDRESS
       AND    MX,1011B  ;CANCELLING HOLD-LINE FUNCTION
;
;*
;* HANDFREE FUNCTION
;*
       LD     X,ZR1     ;R13 MUST SET TO "0"
       AND    MX,0111B  ; FOR HANDFREE FUNCTION
;
       LD     X,ZCHFO   ;SET R13 TERMINAL AS HANDFREE OUTPUT
       OR     MX,1000B
```

```
;
        LD      X,ZHF       ;SET HANDFREE OUTPUT CONTROL ADDRESS
        OR      MX,1000B    ;SET HFO (R13) TERMINAL TO VDD
;       :
;       :
        LD      X,ZHF       ;SET HANDFREE OUTPUT CONTROL ADDRESS
        AND     MX,0111B    ;SET HFO TERMINAL TO VSS
;
```

Programming notes

(1) When BZ and $\overline{BZ}$ output are selected by software, a hazard may be observed in the output waveform when the data of the output register changes.

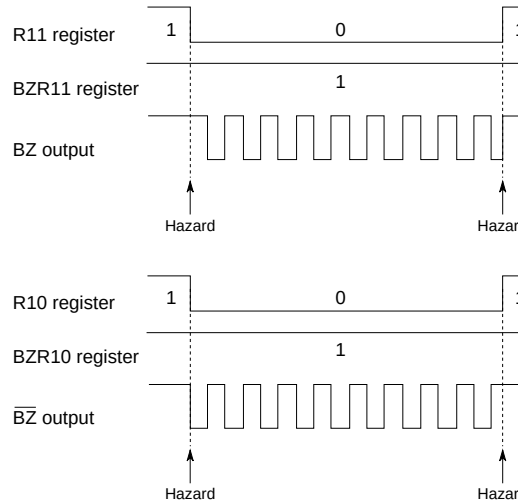


Fig. 6.4.4
Output waveform

(2) When R10 terminal is used for general output port, set BZR10 register to "0". When R10 terminal is used for $\overline{BZ}$ output port, set R10 register to "0".

(3) When R11 terminal is used for general output port, set BZR11 register to "0". When R11 terminal is used for BZ output port, set R11 register to "0".

(4) When R12 terminal is used for general output port, set CHDO register to "0". When R12 terminal is used for HOLD output port, set R12 register to "0".

(5) When R13 terminal is used for general output port, set CHFO register to "0". When R13 terminal is used for HANDFREE output port, set R13 register to "0".

6.5 I/O Ports (P00–P03)

I/O data memory of the I/O port

The control registers of the I/O port are shown in Table 6.5.1.

Table 6.5.1 Control registers of I/O port

Address *6	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
D5H	IOC3	IOC2	IOC1	IOC0	IOC3	0	Output	Input	I/O control register
	R/W				IOC2	0	Output	Input	
					IOC1	0	Output	Input	
					IOC0	0	Output	Input	
D6H	PUP3	PUP2	PUP1	PUP0	PUP3	0	ON	OFF	Pull up control register
	R/W				PUP2	0	ON	OFF	
					PUP1	0	ON	OFF	
					PUP0	0	ON	OFF	
D7H	P03	P02	P01	P00	P03	1	High	Low	I/O port
	R/W				P02	1	High	Low	
					P01	1	High	Low	
					P00	1	High	Low	

*1 Initial value at initial reset
*2 Not set in the circuit
*3 Undefined
*4 Inhibit state (output port will be set to "1")
*5 Constantly "0" when being read
*6 Page switching in I/O memory is not necessary

Control of the I/O port

The E0C62T3 contains 4 bits general I/O port.
Each terminal of the I/O port can be used as input or output port individually, according to the I/O control registers IOC3–IOC0 (D5H). When the I/O control register is "0", the I/O port is set as input port, and when it is "1", the I/O port is set as output port.
Each terminal of the I/O port can be operated with connecting or unconnecting pull-up resistor by software while in the input mode. These 4 pull-up resistors are controlled by pull-up control registers PUP3–PUP0 (D6H).

How to set as input

Set "0" in the I/O port control register IOC0 (IOC1 for P01, IOC2 for P02, IOC3 for P03) and the I/O port P00 is set as an input port.
The state of the I/O port P00–P03 are decided by the address D7H. (In the input mode, the port level is read directly.)
The P00–P03 I/O port can be pull up by software in each bit. Set "1" in the I/O pull up control register PUP0 (PUP1 for P01, PUP2 for P02, PUP3 for P03) and the pull-up resistor will directly connect to P00 internally.

How to set as output

Set "1" in the I/O port control register IOC0 (IOC1 for P01, IOC2 for P02, IOC3 for P03) and the I/O port P00 is set as an output port.
In the output mode, the I/O port terminals are decided by P00–P03 (D7H) registers. These registers can be set regardless the each bit of the I/O port is in the input mode or output mode.

If perform the read-out I/O port in each mode; when output mode, the register value is read out, and when input mode, the port value (input voltage level) is read out.

After an initial reset, I/O port is set as input port and without pull-up resistor.

Example program for the I/O port

Following program shows the I/O port controlling procedure.

```
Label    Mnemonic/operand    Comment
;*
;* I/O PORT
;*
;
ZIOC    EQU    0D5H      ;I/O PORT CONTROL REGISTER
IOC3    EQU    1000B     ;P03 PORT CONTROL BIT
IOC2    EQU    0100B     ;P02 PORT CONTROL BIT
IOC1    EQU    0010B     ;P01 PORT CONTROL BIT
IOC0    EQU    0001B     ;P00 PORT CONTROL BIT
;
ZPUP    EQU    0D6H      ;I/O PORT PULL-UP CONTROL REGISTER
PUP3    EQU    1000B     ;P03 PULL-UP CONTROL BIT
PUP2    EQU    0100B     ;P02 PULL-UP CONTROL BIT
PUP1    EQU    0010B     ;P01 PULL-UP CONTROL BIT
PUP0    EQU    0001B     ;P00 PULL-UP CONTROL BIT
;
ZP0     EQU    0D7H      ;I/O PORT P00-P03
P03     EQU    1000B     ;P03
P02     EQU    0100B     ;P02
P01     EQU    0010B     ;P01
P00     EQU    0001B     ;P00
;
```

```
;*
;* SET P00 & P01 AS INPUT WITH PULL-UP RESISTOR
;* AND READ P00 & P01 INTO A REG.
;*
       LD     X,ZIOC    ;SET P00 & P01 AS INPUT
       AND    MX,(NOT (IOC0 OR IOC1)) AND 0FH
;
       LD     X,ZPUP    ;CONNECTING PULL-UP RESISTORS
                        ; TO P00 & P01
       OR     MX,PUP0 OR PUP1
;
       LD     X,ZP0     ;READ IN P00 & P01 INTO Areg's D0 & D1
       LD     A,MX
       AND    A,P00 OR P01 ;MASK P02 & P03 PORT REGISTER'S DATA
;
;*
;* SET P02 & P03 AS OUTPUT
;* AND OUTPUT B REGISTER TO P02-P03 TERMINALS
;*
       LD     X,ZIOC    ;SET P02 & P03 AS OUTPUT
       OR     MX,IOC2 OR IOC3
;
       LD     X,ZP0     ;SET I/O PORT ADDRESS
       LD     MX,B      ;LOAD B TO I/O PORT REGISTER
                        ;ONLY P02 & P03 TERMINALS CAN OUTPUT DATA
;
```

Programming note

When in the input mode, I/O port is changed from low to high by pull up resistor, the rise of the waveform is delayed on account of the time constant of the pull up resistor and input gate capacitance. Hence, when fetching input port, set an appropriate wait time.

6.6 LCD Driver

I/O data memory of the LCD driver

The control registers of the LCD driver are shown in Table 6.6.1.

Table 6.6.1 Control registers of LCD driver

Address *6	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
DEH	LDTY1	LDTY0	0	LCDON	LDTY1	0			LCD drive duty selection 0 : 1/4, 1 : 1/3, 2 : 1/2, 3 : 1/1
	R/W		R	R/W	LDTY0	0			
					0	– *2			Unused *5
					LCDON	0	ON	OFF	LCD display control (LCD display all off)

*1 Initial value at initial reset
*2 Not set in the circuit
*3 Undefined
*4 Inhibit state (output port will be set to "1")
*5 Constantly "0" when being read
*6 Page switching in I/O memory is not necessary

Address Page *1	Low / High	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0–4	8	Display memory area (80H–AFH) 48 words x 4 bits (Write only)															
	9																
	A																

*1 Page switching in display memory is not necessary

Fig. 6.6.1 Display memory map

Control of the LCD driver

The E0C62T3 contains 192 bits of display memory in addresses 80H to AFH of the data memory.
It's LCD common can be software programmable for 4 COM, 3 COM, 2 COM or 1 COM. So each display memory can be assigned to any 128 bits of the 192 bits for the LCD driver (32 SEG × 4 COM), 96 bits of 192 bits (32 SEG × 3 COM), 64 bits of 192 bits (32 SEG × 2 COM), or 32 bits of the 192 bits (32 SEG × 1 COM) by using a segment mask option. The remaining 64 bits, 96 bits, 128 bits or 160 bits of display memory are not connected to the LCD driver, and are not output even when data is written. An LCD segment is on with "1" set in the display memory, and off with "0" set in the display memory. Note that the display memory is a write-only RAM.

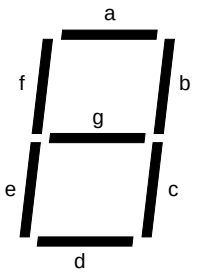
- LCD drive duty selection is control by registers LDTY1 and LDTY0 (DEH•D3, D2).

Table 6.6.2
LCD drive duty selection

LDTY1	LDTY0	LCD drive duty
0	0	1/4 (dynamic)
0	1	1/3 (dynamic)
1	0	1/2 (dynamic)
1	1	1/1 (dynamic)

- LCD display ON/OFF is controlled by register LCDON (DEH•D0).
  Set LCDON to "1" to turn on LCD.
  Set LCDON to "0" to turn off LCD.

Figure 6.6.2 is an example of the 7-segment LCD assignment.



Address	Register			
	D3	D2	D1	D0
090H	d	c	b	a
091H		g	f	e

Fig. 6.6.2
7-segment LCD assignment

In the assignment shown in Figure 6.6.2, the 7-segment display pattern is controlled by writing data to display memory addresses 90H and 91H.

Example program for the LCD driver

LCD common control and display ON/OFF

```
Label    Mnemonic/operand    Comment
;*
;* LCD DRIVER
;*
;* TURN ON LCD AND USE 4 COMMONS
;
ZLCDC  EQU    0DEH       ;LCD CONTROL REGISTER
;
       LD     X,ZLCDC    ;SET LCD CONTROL REGISTER ADDRESS
       LD     MX,0001B   ;SET DUTY AS 1/4 (4 COMMONS)
                         ;SET LCD DISPLAY ON
;
```

Displaying 7-segment

The LCD display routine using the assignment of Figure 6.6.2 can be programmed as follows.

```
Label     Mnemonic/operand    Comment
;*
;* LCD DRIVER
;*
;* SEVEN SEGMENT CHARACTER GENERATOR
;
        ORG    000H
        RETD   3FH        ;0 IS DISPLAYED
        RETD   06H        ;1 IS DISPLAYED
        RETD   5BH        ;2 IS DISPLAYED
        RETD   4FH        ;3 IS DISPLAYED
        RETD   66H        ;4 IS DISPLAYED
        RETD   6DH        ;5 IS DISPLAYED
        RETD   7DH        ;6 IS DISPLAYED
        RETD   07H        ;7 IS DISPLAYED
        RETD   7FH        ;8 IS DISPLAYED
        RETD   6FH        ;9 IS DISPLAYED
;
SEVENS:
        LD     B,0        ;PREPARE B AS 0 FOR JUMP
        LD     X,090H     ;SET LCD DISPLAY MEMORY ADDRESS
        JPBA              ;JUMP TO TABLE
;
```

When the above routine is called (by the CALL or CALZ instruction) with any number from "0" to "9" set in the A register for the assignment of Figure 6.6.3, seven segments are displayed according to the contents of the A register.

Fig. 6.6.3
Data set in A register and display patterns

A register	Display	A register	Display	A register	Display	A register	Display	A register	Display
0		2		4		6		8	
1		3		5		7		9	

The RETD instruction can be used to write data to the display memory only if it is addressed using the X register. (Addressing using the Y register is invalid.)

Note that the stack pointer must be set to a proper value before the CALL (CALZ) instruction is executed.

Bit-unit operation of the display memory

Address	Data			
	D3	D2	D1	D0
90H			▲	●

▲ : SEG - A
● : SEG - B

Fig. 6.6.4
Example of segment assignment

```
Label    Mnemonic/operand   Comment
;*
;* LCD DRIVER
;*
;* BIT UNIT OPERATION
;
SEGBUF EQU    00H        ;DISPLAY MEMORY BUFFER
;
       LD     X,SEGBUF   ;SET ADDRESS DISPLAY MEMORY BUFFER
       LD     Y,90H      ;SET ADDRESS DISPLAY MEMORY
       LD     MX,3       ;SET BUFFER DATA
       LD     MY,MX      ;SET SEGMENT A, B ON ( ○, △ )
       AND    MX,1110B   ;CHANGE BUFFER DATA
       LD     MY,MX      ;SET SEGMENT A OFF ( ○, ▲ )
       AND    MX,1101B   ;CHANGE BUFFER DATA
       LD     MY,MX      ;SET SEGMENT B OFF ( ●, ▲ )
;
```

For manipulation of the display memory in bit-units for the assignment of Figure 6.6.4, a buffer must be provided in RAM to hold data. Note that, since the display memory is write-only, data cannot be changed directly using an ALU instruction (for example, AND or OR).

After manipulating the data in the buffer, write it into the corresponding display memory using the transfer command.

Programming notes

(1) The contents of the display memory are undefined until the area is initialized (through, for instance, memory clear processing by the CPU). Initialize the display memory by executing initial processing.

(2) Since the display memory area is write-only, display data cannot be rewritten by arithmetic operations (such as AND, OR, ADD, SUB).

6.7 Clock Timer

I/O data memory of the clock timer

The control registers of the clock timer are shown in Table 6.7.1.

Table 6.7.1 Control registers of clock timer

Address *6	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
C4H	IT1	IT2	IT16	IT32	IT1	0	Yes	No	Interrupt factor flag (clock timer 1 Hz) Clear to 0 after read out
	R				IT2	0	Yes	No	Interrupt factor flag (clock timer 2 Hz) Clear to 0 after read out
					IT16	0	Yes	No	Interrupt factor flag (clock timer 16 Hz) Clear to 0 after read out
					IT32	0	Yes	No	Interrupt factor flag (clock timer 32 Hz) Clear to 0 after read out
D1H	EIT1	EIT2	EIT16	EIT32	EIT1	0	Enable	Mask	Interrupt mask register (clcok timer 1 Hz)
	R/W				EIT2	0	Enable	Mask	Interrupt mask register (clock timer 2 Hz)
					EIT16	0	Enable	Mask	Interrupt mask register (clock timer 16 Hz)
					EIT32	0	Enable	Mask	Interrupt mask register (clock timer 32 Hz)
D9H	0	0	0	TMRST	0	– *2			Unused *5
	R			W	0	– *2			Unused *5
					0	– *2			Unused *5
					TMRST	– *2	Reset	Invalid	Clock timer reset *5
DAH	TM3	TM2	TM1	TM0	TM3	– *3			Clock timer data (low-order) 16 Hz
	R				TM2	– *3			Clock timer data (low-order) 32 Hz
					TM1	– *3			Clock timer data (low-order) 64 Hz
					TM0	– *3			Clock timer data (low-order) 128 Hz
DBH	TM7	TM6	TM5	TM4	TM7	– *3			Clock timer data (high-order) 1 Hz
	R				TM6	– *3			Clock timer data (high-order) 2 Hz
					TM5	– *3			Clock timer data (high-order) 4 Hz
					TM4	– *3			Clock timer data (high-order) 8 Hz

*1 Initial value at initial reset
*2 Not set in the circuit
*3 Undefined
*4 Inhibit state (output port will be set to "1")
*5 Constantly "0" when being read
*6 Page switching in I/O memory is not necessary

Control of the clock timer

E0C62T3 has a clock timer with OSC1 (crystal oscillation) as basic oscillation built-in.

Clock timer data

The 128–1 Hz timer data of the clock timer can be read out with TM0–TM7 registers (DAH and DBH).

Clock timer reset

By writing "1" on TMRST (D9H•D0), the clock timer is reset and all timer data are set to "0".

Timer interrupt

The clock timer interrupt is generated at the falling edge of the frequencies (32 Hz, 16 Hz, 2 Hz and 1 Hz). At this time, the corresponding interrupt factor flag (IT32, IT16, IT2 and IT1) is set to "1". Selection of whether to mask the separate interrupts can be made with the interrupt mask registers (EIT32, EIT16, EIT2 and EIT1). However, regardless of the interrupt mask register setting, the interrupt factor flag is set to "1" at the falling edge of the corresponding signal.

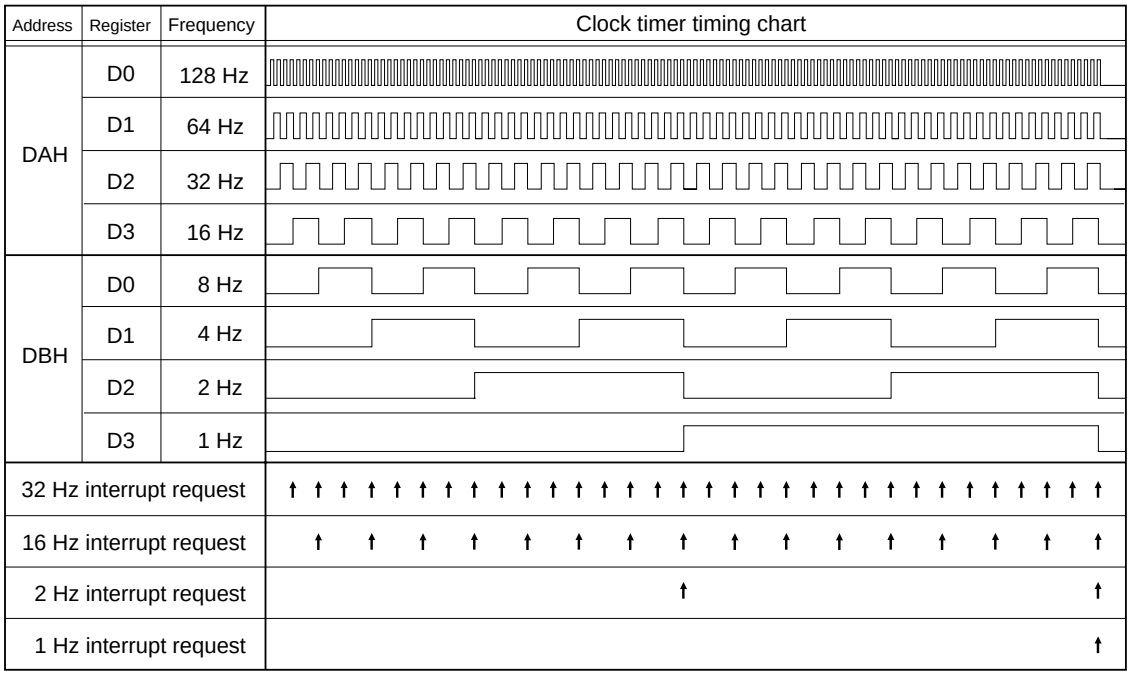


Fig. 6.7.1 Timing chart of clock timer

Example program for the clock timer

Following program shows the clock timer controlling procedure.

```
Label    Mnemonic/operand    Comment
;*
;* CLOCK TIMER
;*
ZIT     EQU    0C4H       ;CLOCK TIMER INTERRUPT FACTOR FLAG
ZEIT    EQU    0D1H       ;CLOCK TIMER INTERRUPT MASK REGISTER
ZTMRST  EQU    0D9H       ;CLOCK TIMER RESET
ZTML    EQU    0DAH       ;CLOCK TIMER DATA LOW
ZTMH    EQU    0DBH       ;CLOCK TIMER DATA HIGH
;
        ORG    102H
        JP     TMINIT     ;TIMER INTERRUPT ROUTINE
;
TMINIT:
        LD     X,ZTMRST   ;RESET CLOCK TIMER
        OR     MX,0001B
;
        DI
        LD     X,ZIT      ;RESET IT FLAGS
        LD     A,MX
;
        LD     X,ZEIT     ;SET ADDRESS TO TIMER MASK REGISTER
        LD     MX,0100B   ;ENABLE TIMER 2 Hz INTERRUPT
        EI
        RET

;
;* CLOCK TIMER INTERRUPT
TMINT:
        LD     X,ZIT      ;LOAD TIMER INTERRUPT FLAG TO B REGISTER
        LD     B,MX
;       :
;       DO THE PROCEDURE FOR 2 Hz INTERRUPT SERVICE
;       :
        EI
        RET
;
;*
;* READ TIMER DATA TO (B,A) REGISTERS
;*
READTM:
        LD     X,ZTML     ;SET TO TIMER DATA ADDRESS
        LDPX   A,MX       ;READ TIMER LOW INTO A REGISTER
        LD     B,MX       ;READ TIMER HIGH INTO B REGISTER
        RET
;
```

Programming notes

(1) Clock timer data is not reset at initial reset. It can be reset by software, writing "1" to TMRST.

(2) When the clock timer has been reset, the interrupt factor flag (IT) may sometimes be set to "1". Consequently, perform flag read (reset the flag) as necessary at reset.

(3) When reading both timer data, TMH (DBH) and TML (DAH), after reading TML, TMH should be read within 0.5 msec, otherwise, the hardware can not guarantee the readout is correct.

(4) Be sure that writing to the interrupt mask register is done with the interrupt in the DI status (interrupt flag = "0"). Writing to the interrupt mask register while in the EI status (interrupt flag = "1") may cause malfunction.

(5) Read the interrupt factor flag in the DI status (interrupt flag = "0"). Reading of interrupt factor flag is available at EI, but be careful in the following cases.
If the interrupt mask register value corresponding to the interrupt factor flags to be read is set to "1", an interrupt request will be generated by the interrupt factor flags set timing, or an interrupt request will not be generated. Be very careful when interrupt factor flags are in the same address.

6.8 SVD (Supply Voltage Detection) Circuit

I/O data memory of the SVD circuit

The control registers of the SVD circuit are shown in Table 6.8.1.

Table 6.8.1 Control registers of SVD circuit

Address *6	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
DFH	0	0	SVDDT	SVDON	0	– *2			Unused *5
	R			R/W	0	– *2			Unused *5
					SVDDT	0	Supply voltage Low	Supply voltage Normal	Supply votage detector data
					SVDON	0	ON	OFF	SVD circuit ON/OFF

*1 Initial value at initial reset
*2 Not set in the circuit
*3 Undefined
*4 Inhibit state (output port will be set to "1")
*5 Constantly "0" when being read
*6 Page switching in I/O memory is not necessary

Control of the SVD circuit

The E0C62T3 has a built-in SVD (supply voltage detection) circuit which allows detection of power voltage drop through software. Turning the SVD operation on and off can be controlled through the software (SVDON: DFH•D0). Because the IC consumes a large amount of current during SVD operation, it is recommended that the SVD operation be kept OFF unless it is otherwise necessary. The SVD criteria voltage is 1.8 V.

When SVDON is set to "1", SVD detection is executed. As soon as SVDON is set to "0" the detection result is loaded to the SVDDT register. To obtain a stable result, the SVD circuit must be set to ON with at least 100 µsec. Hence, to obtain the SVD detection result, follow the programming sequence below.

1. Set SVDON to "1" (ON)
2. Maintain at least 100 µsec minimum
3. Set SVDON to "0" (OFF)
4. Read out SVDDT

However, when a crystal oscillation clock (fosc1) is selected for CPU system clock, the instruction cycle are long enough, so that there is no need for concern about maintaining 100 µsec for the SVDON = "1" with the software.

Example program for the SVD circuit

Following program shows the SVD controlling procedure.

```
Label    Mnemonic/operand   Comment
;*
;* SVD (CPU CLOCK IS OSC1)
;*
ZSVDC  EQU    0DFH      ;SVD CONTROL REGISTER
;
SVDCHK:
       LD     X,ZSVDC
;
       OR     MX,0001B  ;START CHECK SUPPLY VOLTAGE
       AND    MX,1110B  ;TURN OFF SVD
;
       LD     A,MX      ;READ SVD DATA INTO A REGISTER'S BIT 1
       RET
;
```

Programming notes

(1) The SVD circuit should normally be turned OFF (SVDON = "0") as the consumption current of the IC becomes large when it is ON (SVDON = "1").

(2) To obtain a stable result, the SVD circuit must be set to ON with at least 100 µsec. Hence, to obtain the SVD detection result, follow the programming sequence below.

1. Set SVDON to "1" (ON)
2. Maintain at least 100 µsec minimum
3. Set SVDON to "0" (OFF)
4. Read out SVDDT

However, when a crystal oscillation clock (fosc1) is selected for CPU system clock, the instruction cycle are long enough, so that there is no need for concern about maintaining 100 µsec for the SVDON = "1" with the software.

6.9 Telephone Function

I/O data memory of the telephone function

The control registers of the telephone function are shown in Tables 6.9.1(a)–(d).

Table 6.9.1(a) Control registers of telephone function

Address *6	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
C5H	0	0	0	ID	0	– *2			Unused *5
	R				0	– *2			Unused *5
					0	– *2			Unused *5
					ID	0	Yes	No	Interrupt factor flag (dialing) Clear to 0 after read out
D2H	0	0	0	EID	0	– *2			Unused *5
	R			R/W	0	– *2			Unused *5
					0	– *2			Unused *5
					EID	0	Enable	Mask	Interrupt mask register (dialing)
D3H	R13	R12	R11	R10	R13	0	High	Low	Output port (R13)
	HFO	HDO	BZ	$\overline{BZ}$	HFO		– *4	ON	Handfree output (HFO)
					R12	0	High	Low	Output port (R12)
					HDO		– *4	ON	Hold-line output (HDO)
					R11	0	High	Low	Output port (R11)
	R/W				BZ		– *4	ON	Buzzer output (BZ)
					R10	0	High	Low	Output port (R10)
					$\overline{BZ}$		– *4	ON	Buzzer inverted output ($\overline{BZ}$)
D8H	0	0	CLKCHG	OSCC	0	– *2			Unused *5
	R		R/W		0	– *2			Unused *5
					CLKCHG	0	OSC3	OSC1	CPU system clock switch
					OSCC	0	ON	OFF	OSC3 oscillation ON/OFF
E0H	TPS	0	MB	DRS	TPS	0	PULSE	TONE	Tone / pulse mode selection
	R/W	R	R/W		0	– *2			Unused *5
					MB	0	33.3:66.6	40:60	Make : Break ratio selection
					DRS	0	20 pps	10 pps	Dialing pulse rate selection

*1 Initial value at initial reset
*2 Not set in the circuit
*3 Undefined
*4 Inhibit state (output port will be set to "1")
*5 Constantly "0" when being read
*6 Page switching in I/O memory is not necessary

Table 6.9.1(b) Control registers of telephone function

Address *6	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
E1H	PTS3	PTS2	PTS1	PTS0	PTS3	0			Pause time selection 0 : Use inhibited 8 : 8 sec 1 : 1 sec 9 : 9 sec 2 : 2 sec A : 10 sec 3 : 3 sec B : 11 sec 4 : 4 sec C : 12 sec 5 : 5 sec D : 13 sec 6 : 6 sec E : 14 sec 7 : 7 sec F : 15 sec
	R/W				PTS2	1			
					PTS1	0			
	Default value : 4 seconds				PTS0	0			
E2H	FTS3	FTS2	FTS1	FTS0	FTS3	0			Flash time selection 0 : Use inhibited 8 : 750 ms 1 : 94 ms 9 : 844 ms 2 : 188 ms A : 938 ms 3 : 281 ms B : 1031 ms 4 : 375 ms C : 1125 ms 5 : 469 ms D : 1219 ms 6 : 563 ms E : 1313 ms 7 : 656 ms F : 1406 ms
	R/W				FTS2	1			
					FTS1	1			
	Default value : 563 ms				FTS0	0			
E3H	0	HOLD	PAUSE	FLASH	0	– *2			Unused *5
	R	R/W	W		HOLD	0	On	Off	Hold-line function
					PAUSE	0	Yes	No	Pause function *5
					FLASH	0	Yes	No	Flash function *5
E4H	HF	0	0	0	HF	0	Yes	No	Hand free
	R/W	R			0	– *2			Unused *5
					0	– *2			Unused *5
					0	– *2			Unused *5
E5H	IDP3	IDP2	IDP1	IDP0	IDP3	1			Inter-digit pause selection for dial pulse 0 : Use inhibited 8 : 750 ms 1 : 94 ms 9 : 844 ms 2 : 188 ms A : 938 ms 3 : 281 ms B : 1031 ms 4 : 375 ms C : 1125 ms 5 : 469 ms D : 1219 ms 6 : 563 ms E : 1313 ms 7 : 656 ms F : 1406 ms
	R/W				IDP2	0			
					IDP1	0			
	Default value : 750 ms				IDP0	0			

*1 Initial value at initial reset
*2 Not set in the circuit
*3 Undefined
*4 Inhibit state (output port will be set to "1")
*5 Constantly "0" when being read
*6 Page switching in I/O memory is not necessary

Table 6.9.1(c) Control registers of telephone function

Address *6	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
E6H	0	0	SINR	SINC	0	– *2			Unused *5
	R		R/W		0	– *2			Unused *5
					SINR	1	Enable	Disable	DTMF row frequency output enable
					SINC	1	Enable	Disable	DTMF column frequency output enable
E7H	TCD3	TCD2	TCD1	TCD0	TCD3	0			Telephone code for dialing TCD DTMF DP TCD DTMF DP 0 : (R_1C_4) Use inhibited 8 : (R_3C_2) 8 1 : (R_1C_1) 1 9 : (R_3C_3) 9 2 : (R_1C_2) 2 A : (R_4C_2) 10 3 : (R_1C_3) 3 B : (R_4C_3) 11 4 : (R_2C_1) 4 C : (R_4C_1) 12 5 : (R_2C_2) 5 D : (R_2C_4) 13 6 : (R_2C_3) 6 E : (R_4C_4) 14 7 : (R_3C_1) 7 F : (R_3C_4) 15
	R/W				TCD2	0			
					TCD1	0			
					TCD0	0			
E8H	0	0	CRMUT	CTMUT	0	– *2			Unused *5
	R		R/W		0	– *2			Unused *5
					CRMUT	1	Receive mute output	0	Receive mute control
					CTMUT	1	Transmit mute output	0	Transmit mute control
E9H	0	0	0	HSON	0	– *2			Unused *5
	R			R/W	0	– *2			Unused *5
					0	– *2			
					HSON	0	Hook Off	Hook On	Hook switch ON/OFF
EAH	CHFO	CHDO	0	0	CHFO	0	Handfree output	DC	R13 output selection (R13 data register has to be "0")
	R/W		R		CHDO	0	Hold output	DC	R12 output selection (R12 data register has to be "0")
					0	– *2			Unused *5
					0	– *2			Unused *5

*1 Initial value at initial reset
*2 Not set in the circuit
*3 Undefined
*4 Inhibit state (output port will be set to "1")
*5 Constantly "0" when being read
*6 Page switching in I/O memory is not necessary

Table 6.9.1(d) Control registers of telephone function

Address *6	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
EBH	CTO	0	0	0	CTO	0	Continuous tone output ON	Continuous tone output OFF	Tone duration time control
	R/W	R			0	– *2			Unused *5
					0	– *2			Unused *5
					0	– *2			Unused *5

*1 Initial value at initial reset
*2 Not set in the circuit
*3 Undefined
*4 Inhibit state (output port will be set to "1")
*5 Constantly "0" when being read
*6 Page switching in I/O memory is not necessary

Features of the telephone function

The E0C62T3 has a built-in telephone function.
It includes the following functions:

(1) Hook switch control
(2) Mute function
(3) Dialing tone (DTMF)
(4) Dialing pulse (DP)
(5) Pause function
(6) Flash function
(7) Hold-line
(8) Handfree

Tone/Pulse selection

Before dialing a number, software program should select DP or DTMF mode by writing TPS register. When writing TPS (E0H•D3) to "1", it will be dialed in DP mode. When writing TPS to "0", it will be dialed in DTMF mode.
At initial reset, TPS is set to "0" (DTMF mode).

Interrupt

The telephone function also provides an interrupt when each of the following condition occurs:

- End of a dialing number cycle by DP mode.
- End of a dialing number cycle by DTMF mode.
- End of a pause function dialing cycle.
- End of a flash function dialing cycle.

At the end of each above cycle, the interrupt factor flag ID (C5H•D0) will be set to "1". For activating next dialing function, software program should perform a reading of ID register in order to clear it. Otherwise, the next dialing (dialing number by DP or DTMF, dialing a pause function or flash function) can not be executed.

The telephone dialing interrupt can be enabled or masked by writing interrupt mask register EID (D2H•D0). When writing "1" to EID register, the dialing interrupt is enabled. When writing "0" to EID register, the dialing interrupt is masked.

Control of the hook switch

The hook switch control register HSON (E9H•D0) is to set the telephone in OFF-HOOK state or ON-HOOK state.
When writing "1" to HSON register, the telephone will become OFF-HOOK state ($\overline{DP}$ terminal goes high level).
When writing "0" to HSON, telephone will become ON-HOOK state ($\overline{DP}$ terminal goes low level).
Before using the telephone, software program should set HSON to "1" for OFF-HOOK state.
At initial reset, HSON is set to "0".

Example program for the hook switch control

Following program shows the hook switch controlling procedure.

```
Label    Mnemonic/operand    Comment
;*
;* HOOK SWITCH CONTROL
;*
ZHSON   EQU    0E9H       ;HOOK SWITCH REGISTER
;
;*
;* SET TO OFF-HOOK STATE
;*
        LD     X,ZHSON
        LD     MX,1
;       :
;       :
;*
;* SET TO ON-HOOK STATE
;*
        LD     X,ZHSON
        LD     MX,0
;       :
;       :
;
```

Control of the mute function

There are two terminals ($\overline{\text{RMUTE}}$ and $\overline{\text{TMUTE}}$) for telephone mute function. The $\overline{\text{RMUTE}}$ terminal is used for receiving mute; the $\overline{\text{TMUTE}}$ terminal is used for transmitting mute.
Software program can force $\overline{\text{RMUTE}}$ terminal to low level (V_{SS}) by writing "0" to CRMUT register (E8H•D1). When writing "1" to CRMUT register, the $\overline{\text{RMUTE}}$ terminal can be controlled by telephone function (during dialing pulse cycle or flash function cycle, it will go to low level).

Software program can force $\overline{\text{TMUTE}}$ terminal to low level (V_{SS}) by writing "0" to CTMUT register (E8H•D0). When writing "1" to CTMUT register, the $\overline{\text{TMUTE}}$ terminal can be controlled by telephone function (during dialing pulse cycle, flash function cycle, dialing tone cycle or hold-line function).

At initial reset, both of CTMUT and CRMUT registers are set to "1".

Example program for the mute function

Following program shows the mute function controlling procedure.

```
Label   Mnemonic/operand   Comment
;*
;* MUTE FUNCTION
;*
ZMUT    EQU    0E8H       ;MUTE CONTROL ADDRESS
CRMUT   EQU    0010B      ;RECEIVE MUTE CONTROL BIT
CTMUT   EQU    0001B      ;TRANSMIT MUTE CONTROL BIT
;
        LD     X,ZMUT     ;SET /RMUTE TERMINAL TO LOW LEVEL
        AND    MX,(NOT CRMUT) AND 0FH
;       :
;       :
        LD     X,ZMUT     ;SET /TMUTE TERMINAL TO LOW LEVEL
        AND    MX,(NOT CTMUT) AND 0FH
;       :
;       :
        LD     X,ZMUT     ;SET /RMUTE & /TMUTE TERMINALS CONTROLLED
                          ;BY TELEPHONE FUNCTION
        OR     MX,(CRMUT OR CTMUT)
;       :
;       :
;
```

Control of the dialing tone (DTMF)

For dialing a number in tone mode, software program should give appropriate values for the following registers.

(1) TPS (E0H•D3): Tone/Pulse mode selection register
Writes "0" to TPS for selecting dialing tone mode.

(2) EID (D2H•D0): Interrupt mask register
Writes "1" to EID for enable dialing interrupt.
Writes "0" to EID for mask dialing interrupt.

(3) SINR (E6H•D1) and SINC (E6H•D0):
DTMF row and column frequency output enable register
The signal of DTMF, it includes two frequencies, row and column frequencies. On the output of DTMF, the row frequency can be controlled by SINR and the column frequency can be controlled by SINC. The SINR and SINC registers can be arranged to control DTMF's output as DC level, single tone or dual tone output.
Table 6.9.2 lists the selection of tone output.

Table 6.9.2
Selection of tone output

Control registers		Tone output
SINR	SINC	
0	0	DC level : $\frac{1}{2}$ (V_{DD}–V_{SS})
0	1	Column frequencies
1	0	Row frequencies
1	1	Dual tone output

The default selection is dual tone output.
At initial reset, these registers are set to "1".

(4) CTO (EBH•D3): Tone duration time control register
A complete dialing tone cycle includes tone duration time period and tone inter-digit pause time period.
When finishing this cycle, it will generate an interrupt.
The tone inter-digit pause time is always fixed to 94 msec.
The tone duration time is controlled by CTO register.
The minimum value of tone duration time is 94 msec.
When CTO is set to "0", tone duration time will be output with the minimum time (94 msec).
When CTO is set to "1", tone duration time will be output until the CTO is changed to "0". If the period (CTO is changed from "1" to "0"), which is controlled by CTO, is less than 94 msec. The duration time will be prolonged to 94 msec.
At initial reset, this register is set to "0".

(5) OSCC (D8H•D0): OSC3 oscillation ON/OFF control register
Because the DTMF's frequencies are based on 3.58 MHz frequency, so before output DTMF's signal, software program should turn on OSC3 oscillator. By writing "1" to OSCC register, and waiting about 5 msec, the OSC3 will be turned on and stable.

After setting the above registers, then software program can start dialing a digit in tone mode by writing a code into telephone code register TCD (E7H). Table 6.9.3(a) shows the dual tone frequencies related to the TCD register when both SINR and SINC registers are set to "1" (dual tone mode).
Table 6.9.3(b) shows the single column frequency related to the TCD register when SINC register is set to "1" and SINR register is set to "0".
Table 6.9.3(c) shows the single row frequency related to the TCD register when SINR register is set to "1" and SINC register is set to "0".

Table 6.9.3(a) Relationship of code and tone frequencies

TCD's code				Tone frequencies	Key's symbol	TCD's code				Tone frequencies	Key's symbol
D3	D2	D1	D0			D3	D2	D1	D0		
0	0	0	0	(ROW1, COL4)		1	0	0	0	(ROW3, COL2)	"8"
0	0	0	1	(ROW1, COL1)	"1"	1	0	0	1	(ROW3, COL3)	"9"
0	0	1	0	(ROW1, COL2)	"2"	1	0	1	0	(ROW4, COL2)	"0"
0	0	1	1	(ROW1, COL3)	"3"	1	0	1	1	(ROW4, COL3)	"#"
0	1	0	0	(ROW2, COL1)	"4"	1	1	0	0	(ROW4, COL1)	"*"
0	1	0	1	(ROW2, COL2)	"5"	1	1	0	1	(ROW2, COL4)	
0	1	1	0	(ROW2, COL3)	"6"	1	1	1	0	(ROW4, COL4)	
0	1	1	1	(ROW3, COL1)	"7"	1	1	1	1	(ROW3, COL4)	

Table 6.9.3(b) Relationship of TCD's code and column frequency

TCD's code				Column frequency	TCD's code				Column frequency
D3	D2	D1	D0		D3	D2	D1	D0	
0	0	0	0	COL4	1	0	0	0	COL2
0	0	0	1	COL1	1	0	0	1	COL3
0	0	1	0	COL2	1	0	1	0	COL2
0	0	1	1	COL3	1	0	1	1	COL3
0	1	0	0	COL1	1	1	0	0	COL1
0	1	0	1	COL2	1	1	0	1	COL4
0	1	1	0	COL3	1	1	1	0	COL4
0	1	1	1	COL1	1	1	1	1	COL4

Table 6.9.3(c) Relationship of TCD's code and row frequency

TCD's code				Row frequency	TCD's code				Row frequency
D3	D2	D1	D0		D3	D2	D1	D0	
0	0	0	0	ROW1	1	0	0	0	ROW3
0	0	0	1	ROW1	1	0	0	1	ROW3
0	0	1	0	ROW1	1	0	1	0	ROW4
0	0	1	1	ROW1	1	0	1	1	ROW4
0	1	0	0	ROW2	1	1	0	0	ROW4
0	1	0	1	ROW2	1	1	0	1	ROW2
0	1	1	0	ROW2	1	1	1	0	ROW4
0	1	1	1	ROW3	1	1	1	1	ROW3

When writing a code to TCD, TONE terminal will output DTMF's signal. $\overline{\text{TMUTE}}$ terminal will go to low level (Vss) during tone duration time period and tone inter-digit pause time period. $\overline{\text{TMUTE}}$ terminal will be continuously kept on low level about 4 msec from the end of the tone inter-digit pause time period. The purpose of the extra 4 msec is for the $\overline{\text{TMUTE}}$ terminal remain low level if next number is dialed within 4 msec.

When completing tone dialing cycle, the interrupt factor flag ID (C5H•D0) will be set to "1". For activating next dialing function, software program should perform a reading of ID register in order to clear it. Otherwise, the next dialing (dialing number by DP or DTMF, dialing a pause function or flash function) can not be executed.

Example program for the dialing tone

Following program shows the dialing tone controlling procedure.

```
Label    Mnemonic/operand   Comment
;*
;* DIALING DTMF EXAMPLE
;*
ZID     EQU    0C5H      ;DIALING INTERRUPT FACTOR FLAG
ZEID    EQU    0D2H      ;DIALING INTERRUPT MASK REGISTER
ZOSCC   EQU    0D8H      ;CPU CLOCK CONTROL
ZTPS    EQU    0E0H      ;TONE/PULSE SELECTION ADDRESS
ZSIN    EQU    0E6H      ;DTMF ROW, COLUMN FREQ. CONTROL REGISTERS
ZTCD    EQU    0E7H      ;TELEPHONE CODE DIALING REGISTER
ZHSON   EQU    0E9H      ;HOOK SWITCH CONTROL REGISTER
ZCTO    EQU    0EBH      ;CONTINUOUS TONE OUTPUT CONTROL REGISTER
;
        ORG    104H
        JP     DILINT    ;DIALING INTERRUPT VECTOR ADDRESS
;*
;* USING INTERRUPT AND FIX TONE OUTPUT DURATION
;*
        DI
        LD     X,ZID     ;CLEAR NULL INTERRUPT FLAG
        LD     A,MX
        LD     X,ZEID    ;ENABLE DIALING INTERRUPT
        LD     MX,1H
        EI
;
        LD     X,ZTPS    ;SET TO TONE MODE
        LD     MX,0
        LD     X,ZSIN    ;SET TO DUAL TONE
        LD     MX,0011B
        LD     X,ZHSON   ;TURN ON HOOK SWITCH
        LD     MX,1
        LD     X,ZCTO    ;SET NO CONTINUOUS TONE OUTPUT
        LD     MX,0      ;(FIX TONE OUTPUT DURATION)
        CALL   OSC3ON    ;TURN ON OSC3
;
```

```
        LD      X,ZTCD    ;DIALING CODE "3"
        LD      MX,3
        HALT              ;CPU HALT AND WAITING DIALING INTERRUPT
        LD      X,ZTCD    ;DIALING CODE "9"
        LD      MX,9
        HALT              ;CPU HALT AND WAITING DIALING INTERRUPT
;       :
;       :
;       :
DILINT:
        LD      X,ZID     ;READING INTERRUPT FACTOR FLAG
        LD      A,MX
        EI
        RET
;*
;* USING POLLING AND CONTINUOUS OUTPUT (WITH SINGLE ROW FREQUENCY)
;*
        LD      X,ZEID    ;DISABLE DIALING INTERRUPT
        LD      MX,0
;
        LD      X,ZTPS    ;SET TO TONE MODE
        LD      MX,0
        LD      X,ZSIN    ;SET TO SINGLE ROW TONE
        LD      MX,0010B
        LD      X,ZHSON   ;TURN ON HOOK SWITCH
        LD      MX,1
        CALL    OSC3ON    ;TURN ON OSC3
;
        LD      X,ZCTO    ;SET TO CONTINUOUS TONE OUTPUT
        LD      MX,1000B
        LD      X,ZTCD    ;DIALING CODE "6"
        LD      MX,6
;       :
;       (SOME PROCEDURE OR WAITING KEY RELEASE)
;       :
        LD      X,ZCTO    ;TURN OFF CONTINUOUS TONE OUTPUT
        LD      MX,0
;
        LD      X,ZID     ;WAITING ID = 1
WAIT1:
        FAN     MX,0001B  ;(IT ALSO CLEAR ID TO "0" WHEN ID IS "1")
        JP      Z,WAIT1
;
        LD      X,ZCTO    ;SET TO CONTINUOUS TONE OUTPUT
        LD      MX,1000B
        LD      X,ZTCD    ;DIALING ANOTHER CODE "8"
        LD      MX,8
;       :
;       (SOME PROCEDURE OR WAITING KEY RELEASE)
;       :
        LD      X,ZCTO    ;TURN OFF CONTINUOUS TONE OUTPUT
        LD      MX,0
;
        LD      X,ZID     ;WAITING ID = 1
```

```
WAIT2:
        FAN     MX,0001B  ;(IT ALSO CLEAR ID TO "0" WHEN ID IS "1")
        JP      Z,WAIT2
;       :
;       :
;*
;* TURN ON OSC3
;*
OSC3ON:
        LD      X,Z0SCC   ;SET OSC3 ON
        OR      MX,0001B
;
        LD      A,0EH     ;WAIT 5mS
OS3DLP:
        ADD     A,0FH
        JP      NZ,OS3DLP
;
        RET
;
```

Control of the dialing pulse (DP)

For dialing a number in pulse mode, software program should give appropriate values for the following registers.

(1) TPS (E0H•D3): Tone/Pulse mode selection register
Writes "1" to TPS for selecting dialing pulse mode.

(2) EID (D2H•D0): Interrupt mask register
Writes "1" to EID for enable dialing interrupt
Writes "0" to EID for mask dialing interrupt

(3) MB (E0H•D1): Make:Break ratio selection register
When writing "1" to MB, the ratio will be set to 33.3:66.6.
When writing "0" to MB, the ratio will be set to 40:60.
At initial reset, it is set to 40:60 ratio.

(4) DRS (E0H•D0): Dialing pulse rate selection register
When writing "1" to DRS, it will be set to 20 pps (pulse per second).
When writing "0" to DRS, it will be set to 10 pps.
At initial reset, it is set to 10 pps.

(5) IDP (E5H): Inter-digit pause time selection registers
A complete dialing pulse cycle includes dialing number period and inter-digit pause time period. When finishing this cycle, it will generate an interrupt. The inter-digit pause time is selected by IDP registers as shown in Table 6.9.4.

Table 6.9.4
Selection of inter-digit pause time

IDP				Inter-digit pause (ms)	IDP				Inter-digit pause (ms)
D3	D2	D1	D0		D3	D2	D1	D0	
0	0	0	0	Use inhibited *	1	0	0	0	750
0	0	0	1	94	1	0	0	1	844
0	0	1	0	188	1	0	1	0	938
0	0	1	1	281	1	0	1	1	1031
0	1	0	0	375	1	1	0	0	1125
0	1	0	1	469	1	1	0	1	1219
0	1	1	0	563	1	1	1	0	1313
0	1	1	1	656	1	1	1	1	1406

* If software program writes a code of "0H" into IDP, it will cause a malfunction.

After setting the above registers, then software program can start to dial a number in pulse mode by writing a code into telephone code register TCD (E7H). Table 6.9.5 shows the counts of pulse related to the TCD register.

Table 6.9.5
Relationship of code and pulse's count

TCD's code				Counts of pulse (pulses)	TCD's code				Counts of pulse (pulses)
D3	D2	D1	D0		D3	D2	D1	D0	
0	0	0	0	Use inhibited *	1	0	0	0	8
0	0	0	1	1	1	0	0	1	9
0	0	1	0	2	1	0	1	0	10
0	0	1	1	3	1	0	1	1	11
0	1	0	0	4	1	1	0	0	12
0	1	0	1	5	1	1	0	1	13
0	1	1	0	6	1	1	1	0	14
0	1	1	1	7	1	1	1	1	15

* If software program writes a code of "0H" into TCD register, it will cause a malfunction.

When writing a code into TCD register, $\overline{DP}$ terminal will output dialing pulses (make period is before break period). $\overline{RMUTE}$ and $\overline{TMUTE}$ terminals will go to low level (Vss) during dialing number period and inter-digit pause time period. Both terminals ($\overline{RMUTE}$ and $\overline{TMUTE}$) will be continuously kept on low level about 4 msec from the end of the inter-digit pause time period. The purpose of the extra 4 msec is for the $\overline{TMUTE}$ and $\overline{RMUTE}$ terminals to remain low level if next number is dialed within 4 msec.

When completing the dialing pulse cycle, the interrupt factor flag ID (C5H•D0) will be set to "1". For activating next dialing function, software program should perform a reading of ID register in order to clear it. Otherwise, the next dialing (dialing number by DP or DTMF, dialing a pause function or flash function) can not be executed.

Example program for the dialing pulse

Following program shows the dialing pulse controlling procedure.

```
Label    Mnemonic/operand    Comment
;*
;* DIALING PULSE EXAMPLE
;*
ZID     EQU    0C5H      ;DIALING INTERRUPT FACTOR FLAG
ZEID    EQU    0D2H      ;DIALING INTERRUPT MASK REGISTER
ZTPS    EQU    0E0H      ;TONE/PULSE, MB, DRS SELECTIONS ADDRESS
ZIDP    EQU    0E5H      ;INTER-DIGIT PAUSE SELECTION REGISTER
ZTCD    EQU    0E7H      ;TELEPHONE CODE DIALING REGISTER
ZHSON   EQU    0E9H      ;HOOK SWITCH CONTROL REGISTER
;
        LD     X,ZEID    ;DISABLE DIALING INTERRUPT
        LD     MX,0
;
        LD     X,ZTPS    ;SET TO PAUSE MODE
        LD     MX,1000B  ;SET MB IS 40:60
                         ;SET DIALING PULSE RATE IS 10 PPS
        LD     X,ZIDP    ;SET INTER-DIGIT PAUSE IS 750 mS
        LD     MX,8H
        LD     X,ZHSON   ;TURN ON FOOK SWITCH
        LD     MX,1
;
        LD     X,ZTCD    ;DIALING CODE "6"
        LD     MX,6
;       :
        LD     X,ZID     ;WAITING ID = 1
WAIT1:
        FAN    MX,0001B  ;(IT ALSO CLEAR ID TO "0" WHEN ID IS "1")
        JP     Z,WAIT1
;       :
;       :
;
```

Control of the pause function

For starting a pause function, software program should give appropriate values for the following registers.

(1) EID (D2H•D0): Interrupt mask register
Writes "1" to EID for enable dialing interrupt
Writes "0" to EID for mask dialing interrupt

(2) PTS (E1H): Pause time selection registers
The time interval of pause function can be set by software program from 1 second to 15 seconds as shown in Table 6.9.6.

Table 6.9.6
Selection of pause time

PTS				Pause time (sec)	PTS				Pause time (sec)
D3	D2	D1	D0		D3	D2	D1	D0	
0	0	0	0	Use inhibited *	1	0	0	0	8
0	0	0	1	1	1	0	0	1	9
0	0	1	0	2	1	0	1	0	10
0	0	1	1	3	1	0	1	1	11
0	1	0	0	4	1	1	0	0	12
0	1	0	1	5	1	1	0	1	13
0	1	1	0	6	1	1	1	0	14
0	1	1	1	7	1	1	1	1	15

* If software program writes a code of "0H" into PTS register, it will cause a malfunction.

At initial reset, the pause time is set to 4 seconds.

After writing the above registers, the software program can start dialing a pause function by writing "1" to PAUSE register (E3H•D1).

When writing "1" to PAUSE, it will pause a few seconds which is set by PTS register. During the pause time it will not affect any hardware terminals.

When completing the pause function, the interrupt factor flag ID (C5H•D0) will be set to "1". For activating next dialing function, software program should perform a reading of ID register in order to clear it. Otherwise, the next dialing (dialing number by DP or DTMF, dialing a pause function or flash function) can not be executed.

Example program for the pause function

Following program shows the pause function controlling procedure.

```
Label    Mnemonic/operand   Comment
;*
;* PAUSE TIME FUNCTION (USING INTERRUPT)
;*
ZID     EQU    0C5H       ;DIALING INTERRUPT FACTOR FLAG
ZEID    EQU    0D2H       ;DIALING INTERRUPT MASK REGISTER
ZPTS    EQU    0E1H       ;PAUSE TIME SELECTION REGISTER
ZHOLD   EQU    0E3H       ;HOLD, PAUSE, FLASH OUTPUT CONTROL
                          ; ADDRESS
;
        ORG    104H
        JP     DILINT     ;DIALING INTERRUPT VACTOR ADDRESS
;
        DI
        LD     X,ZID      ;CLEAR NULL INTERRUPT FLAG
        LD     A,MX
        LD     X,ZEID     ;ENABLE DIALING INTERRUPT
        LD     MX,1H
        EI
;
        LD     X,ZPTS     ;SET PAUSE TIME SELECTION ADDRESS
        LD     MX,6       ;SET PAUSE TIME = 6 SECONDS
;
        LD     X,ZHOLD    ;SET PAUSE CONTROL ADDRESS
        LD     MX,0010B   ;STARTING PAUSE FUNCTION
;
        HALT              ;CPU HALT AND WAITING DIALING INTERRUPT
;       :
;       :
;
;*
;* DIALING INTERRUPT SERVICE ROUTINE
;*
DILINT:
        LD     X,ZID      ;READING INTERRUPT FACTOR FLAG
        LD     A,MX
        EI
        RET
;
```

Control of the flash function

For starting a flash function, software program should give appropriate values for the following register.

(1) EID (D2H•D0): Interrupt mask register
Writes "1" to EID for enable dialing interrupt
Writes "0" to EID for mask dialing interrupt

(2) FTS (E2H): Flash time selection registers
The time interval of flash time can be set by software program from 94 msec to 1406 msec as shown in Table 6.9.7.

Table 6.9.7
Selection of flash times

FTS				Flash time (ms)	FTS				Flash time (ms)
D3	D2	D1	D0		D3	D2	D1	D0	
0	0	0	0	Use inhibited *	1	0	0	0	750
0	0	0	1	94	1	0	0	1	844
0	0	1	0	188	1	0	1	0	938
0	0	1	1	281	1	0	1	1	1031
0	1	0	0	375	1	1	0	0	1125
0	1	0	1	469	1	1	0	1	1219
0	1	1	0	563	1	1	1	0	1313
0	1	1	1	656	1	1	1	1	1406

* If software program writes a code of "0H" into FTS register, it will cause a malfunction.

At initial reset, the flash time is set to 563 msec.

After setting the above registers, the software program can start dialing a flash function by writing "1" to FLASH register (E3H•D0). When writing "1" to FLASH, $\overline{DP}$ terminal will go to low level (V_{SS}) for a few hundreds milliseconds which is set by FTS register. $\overline{RMUTE}$ and $\overline{TMUTE}$ terminals will go to low level during the flash time and flash pause time periods. Both terminals ($\overline{RMUTE}$ and $\overline{TMUTE}$) will be continuously kept on low level about 4 msec from the end of flash pause time period. The purpose of the extra 4 msec is for the $\overline{TMUTE}$ and $\overline{RMUTE}$ terminals to remain low level if next number is dialed within 4 msec.

When completing the flash function, the interrupt factor flag ID (C5H•D0) will be set to "1". For activating next dialing function, software program should perform a reading of ID register in order to clear it. Otherwise, the next dialing (dialing number by DP or DTMF, dialing a pause function or flash function) cannot be executed.

Example program for the flash function

Following program shows the flash function controlling procedure.

```
Label   Mnemonic/operand   Comment
;*
;* FLASH TIME FUNCTION (USING INTERRUPT)
;*
ZID     EQU    0C5H       ;DIALING INTERRUPT FACTOR FLAG
ZEID    EQU    0D2H       ;DIALING INTERRUPT MASK REGISTER
ZFTS    EQU    0E2H       ;FLASH TIME SELECTION REGISTER
ZHOLD   EQU    0E3H       ;HOLD, PAUSE, FLASH OUTPUT CONTROL
                          ; ADDRESS
ZHSON   EQU    0E9H       ;HOOK SWITCH CONTROL REGISTER
;
        ORG    104H
        JP     DILINT     ;DIALING INTERRUPT VACTOR ADDRESS
;
        DI
        LD     X,ZID      ;CLEAR NULL INTERRUPT FLAG
        LD     A,MX
        LD     X,ZEID     ;ENABLE DIALING INTERRUPT
        LD     MX,1H
        EI
;
        LD     X,ZHSON    ;TURN ON HOOK SWITCH
        LD     MX,1
;
        LD     X,ZFTS     ;SET FLASH TIME SELECTION ADDRESS
        LD     MX,8       ;SET FLASH TIME = 750 mS
;
        LD     X,ZHOLD    ;SET FLASH CONTROL ADDRESS
        LD     MX,0001B   ;STARTING FLASH FUNCTION
;
        HALT              ;CPU HALT AND WAITING DIALING INTERRUPT
;       :
;       :
;
;*
;* DIALING INTERRUPT SERVICE ROUTINE
;*
DILINT:
        LD     X,ZID      ;READING INTERRUPT FACTOR FLAG
        LD     A,MX
        EI
        RET
;
```

Control of the hold-line function

The E0C62T3 also has a built-in telephone hold-line function. Software program can set R12 terminal to hold-line output (HDO) terminal by writing "1" to CHDO register (EAH•D2) and writing "0" to R12 register.
When R12 terminal is used as HDO output, it outputs the data which is written in the register HOLD (E3H•D2).

When HOLD (E3H•D2) register is turned ON, $\overline{\text{TMUTE}}$ terminal goes low level (VSS) and HDO (R12) terminal goes high level (VDD).
When HOLD register is turned OFF, $\overline{\text{TMUTE}}$ terminal goes high level (VDD) and HDO (R12) terminal goes low level (VSS).
Hold-line function is a toggle selection and it does not generate interrupt.
At initial reset, this register is set to "0".

Example program for the hold-line function

Following program shows the hold-line function controlling procedure.

```
Label    Mnemonic/operand   Comment
;*
;* HOLD-LINE FUNCTION
;*
ZR1    EQU    0D3H      ;R10-R13 REGISTERS ADDRESS
ZHOLD  EQU    0E3H      ;HOLD, PAUSE, FLASH OUTPUT CONTROL
                        ; ADDRESS
ZCHFO  EQU    0EAH      ;R13 & R12 TERMINALS SELECTION ADDRESS
;
       LD     X,ZR1     ;R12 MUST SET TO "0" FOR HOLD-LINE
       AND    MX,1011B  ; FUNCTION
;
       LD     X,ZCHFO   ;SET R12 TERMINAL AS HOLD-LINE OUTPUT
       OR     MX,0100B
;
       LD     X,ZHOLD   ;SET HOLD CONTROL ADDRESS
       LD     MX,0100B  ;EXECUTING HOLD-LINE FUNCTION
;      :
;      :
       LD     X,ZHOLD   ;SET HOLD CONTROL ADDRESS
       LD     MX,0000B  ;CANCELLING HOLD-LINE FUNCTION
;
```

Control of the handfree function

For handfree function, R13 terminal can be used as HFO (handfree output) signal output terminal. Software program can set R13 terminal to HFO output by writing "1" to CHFO register (EAH•D3) and writing "0" to R13 register.
When R13 terminal is used as HFO output, it outputs the data which is written in the register HF (E4H•D3).
When writing "1" to HF register, the HFO (R13) terminal output high level (V_{DD}).
When writing "0" to HF register, then HFO (R13) terminal output low level (V_{SS}).

Example program for the handfree function

Following program shows the handfree function controlling procedure.

```
Label   Mnemonic/operand   Comment
;*
;* HANDFREE FUNCTION
;*
ZR1     EQU    0D3H       ;R10-R13 REGISTERS ADDRESS
ZHF     EQU    0E4H       ;HANDFREE OUTPUT CONTROL ADDRESS
ZCHFO   EQU    0EAH       ;R13 & R12 TERMINALS SELECTION ADDRESS
;
        LD     X,ZR1      ;R13 MUST SET TO "0" FOR HANDFREE
        AND    MX,0111B   ;  FUNCTION
;
        LD     X,ZCHFO    ;SET R13 TERMINAL AS HANDFREE OUTPUT
        OR     MX,1000B
;
        LD     X,ZHF      ;SET HANDFREE CONTROL ADDRESS
        OR     MX,1000B   ;SET HFO (R13) TERMINAL TO VDD
;       :
;       :
        LD     X,ZHF      ;SET HANDFREE CONTROL ADDRESS
        AND    MX,0111B   ;SET HFO TERMINAL TO VSS
;
```

Programming notes

(1) When uses the DTMF, it is necessary to turn ON the 3.58 MHz oscillator. This function needs big current. Therefore, using DTMF dialing at off-hook or handfree status is the best.

(2) Read the interrupt factor flag in the DI status (interrupt flag = "0"). Reading of interrupt factor flag is available at EI, but be careful in the following cases.
If the interrupt mask register value corresponding to the interrupt factor flags to be read is set to "1", an interrupt request will be generated by the interrupt factor flags set timing, or an interrupt request will not be generated. Be very careful when interrupt factor flags are in the same address.

(3) Be sure that writing to the interrupt mask register is done with the interrupt in the DI status (interrupt flag = "0"). Writing to the interrupt mask register while in the EI status (interrupt flag = "1") may cause malfunction.

(4) Before using the telephone, software program should set HSON (E9H•D0) register to "1" for OFF-HOOK state ($\overline{DP}$ terminal goes high level).

(5) If software program writes a code of "0H" into TCD register in pulse mode, IDP, FTS or PTS registers, it will cause a malfunction.

(6) Because pause function control register (E3H•D1) and flash function control register (E3H•D0) are write-only, software cannot use ALU instructions (AND, OR ...) on E3H resisters while dialing a pause or flash function cycle.

6.10 Interrupt

Interrupt vector, factor flag, and mask register

When an interrupt request is issued to the CPU, the CPU starts interrupt processing.
Interrupt processing is accomplished by the following steps after the instruction being executed is completed.

① The address (value of the program counter) of the program which should be run next is saved in the stack area (RAM).

② The vector address (1 page 02H–0DH) for each interrupt request is set to the program counter.

③ Branch instruction written to the vector is effected (branch to software interrupt processing routine).

Note: *Time equivalent to 12 cycles of CPU system clock is required for steps ① and ②.*

The interrupt request and interrupt vector correspondence is shown in Table 6.10.1.

Table 6.10.1
Interrupt request and interrupt vectors

Interrupt vector	Interrupt request	Priority
102H	Clock timer	Low
104H	Dialing cycle completion	↑
106H	K00–K03 input	
108H	K10–K13 input	
10AH	K20–K21 input	↓
10CH	K22 input	High

When multiple interrupts simultaneously occur, the high priority vector address is set to the program counter.

The interrupt factor flags and interrupt mask registers correspondence are shown in Table 6.10.2.
The configuration of the interrupt circuit is shown in Figure 6.10.1.

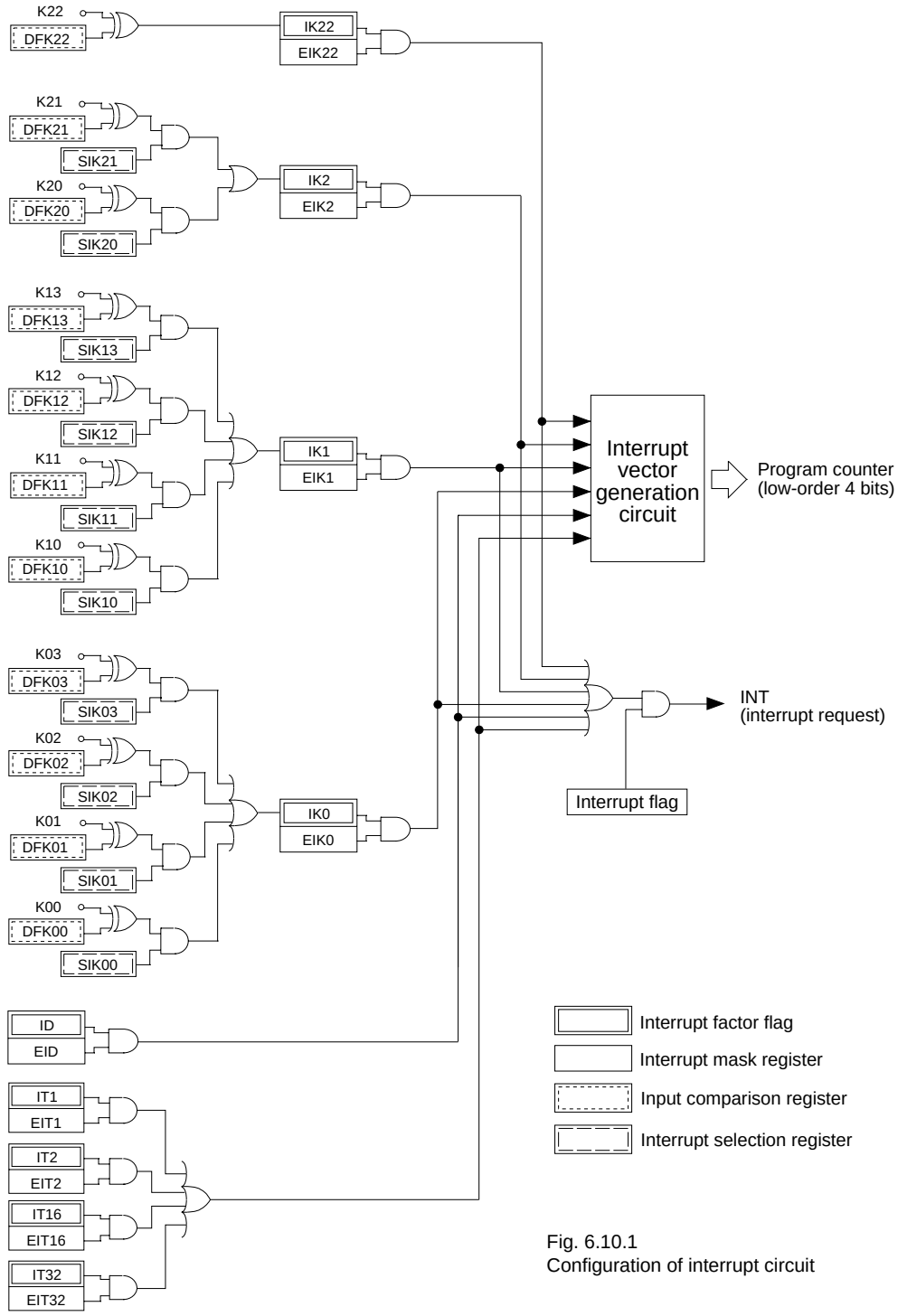


Fig. 6.10.1
Configuration of interrupt circuit

Table 6.10.2
Interrupt flags and interrupt mask registers

Interrupt factor	Interrupt factor flag	Interrupt mask register
Falling edge of clock timer (1 Hz)	IT1(C4H•D3)	EIT1(D1H•D3)
Falling edge of clock timer (2 Hz)	IT2(C4H•D2)	EIT2(D1H•D2)
Falling edge of clock timer (16 Hz)	IT16(C4H•D1)	EIT16(D1H•D1)
Falling edge of clock timer (32 Hz)	IT32(C4H•D0)	EIT32(D1H•D0)
Dialing cycle completion	ID(C5H•D0)	EID(D2H•D0)
No matching between input ports (K00–K03) and input comparison registers (DFK00–DFK03)	IK0(C3H•D0)	EIK0(D0H•D0) SIK00(C8H•D0) SIK01(C8H•D1) SIK02(C8H•D2) SIK03(C8H•D3)
No matching between input ports (K10–K13) and input comparison registers (DFK10–DFK13)	IK1(C2H•D0)	EIK1(D0H•D1) SIK10(C7H•D0) SIK11(C7H•D1) SIK12(C7H•D2) SIK13(C7H•D3)
No matching between input ports (K20–K21) and input comparison registers (DFK20–DFK21)	IK2(C1H•D0)	EIK2(D0H•D2) SIK20(C6H•D0) SIK21(C6H•D1)
No matching between input ports (K22) and input comparison registers (DFK22)	IK22(C0H•D0)	EIK22(D0H•D3)

Example program for the interrupt

Following program shows the interrupt procedure.

```
Label   Mnemonic/operand   Comment
;*
;* INTERRUPT
;*
ZIK22   EQU    0C0H      ;K22 INTERRUPT FACTOR FLAG ADDRESS
IK22    EQU    0001B     ;K22 INTERRUPT FACTOR FLAG BIT
;
ZIK2    EQU    0C1H      ;K20-K21 INTERRUPT FACTOR FLAG ADDRESS
IK2     EQU    0001B     ;K20-K21 INTERRUPT FACTOR FLAG BIT
;
ZIK1    EQU    0C2H      ;K10-K13 INTERRUPT FACTOR FLAG ADDRESS
IK1     EQU    0001B     ;K10-K13 INTERRUPT FACTOR FLAG BIT
;
ZIK0    EQU    0C3H      ;K00-K03 INTERRUPT FACTOR FLAG ADDRESS
IK0     EQU    0001B     ;K00-K03 INTERRUPT FACTOR FLAG BIT
;
ZIT     EQU    0C4H      ;TIMER INTERRUPT FACTOR FLAG ADDRESS
IT1     EQU    1000B     ;1 Hz INTERRUPT FACTOR FLAG BIT
IT2     EQU    0100B     ;2 Hz INTERRUPT FACTOR FLAG BIT
IT16    EQU    0010B     ;16 Hz INTERRUPT FACTOR FLAG BIT
IT32    EQU    0001B     ;32 Hz INTERRUPT FACTOR FLAG BIT
;
ZID     EQU    0C5H      ;DIALING INTERRUPT FACTOR FLAG ADDRESS
ID      EQU    0001B     ;DIALING INTERRUPT FACTOR FLAG BIT
```

```
;
ZWDOG  EQU    0DCH      ;WATCHDOG ADDRESS
WDON   EQU    1000B     ;WATCHDOG ON/OFF BIT
WDRST  EQU    0100B     ;WATCHDOG RESET BIT
;
       ORG    102H
       JP     TMINT     ;TIMER (6th PRIORITY)
;
       ORG    104H
       JP     DILINT    ;DIALING (5th PRIORITY)
;
       ORG    106H
       JP     K0INT     ;K0 (4th PRIORITY)
;
       ORG    108H
       JP     K1INT     ;K1 (3rd PRIORITY)
;
       ORG    10AH
       JP     K2INT     ;K2 (2nd PRIORITY)
;
       ORG    10CH
       JP     K22INT    ;K22 (1st PRIORITY)
;
;* APPLICATION MAIN ROUTINE
MAIN:
       DI
;      :
;  (ENABLE TIMER, DIALING, K00-K03 INPUT,
;   K10-K13 INPUT, K20-K21 INPUT, K22 INPUT)
;  (DIALING A NUMBER FOR TRIGGER DIALING INTERRUPT)
;      :
       LD     X,ZWDOG   ;TURN ON WATCHDOG TIMER
       LD     MX,WDON
       EI
MAIN1:
       HALT
       JP     MAIN1
;
;* CLOCK TIMER INTERRUPT
TMINT:
       LD     X,ZIT     ;LOAD TIMER INTERRUPT FLAG TO B REGISTER
       LD     B,MX
CHKT32:
       FAN    B,IT32    ;CHECK TIMER 32 Hz INTERRUPT FLAG
       JP     Z,CHKT16  ;NO, THEN JUMP
       CALL   SERT32    ;TIMER 32 Hz SERVICE ROUTINE
CHKT16:
       FAN    B,IT16    ;CHECK TIMER 16 Hz INTERRUPT FLAG
       JP     Z,CHKT2   ;NO, THEN JUMP
       CALL   SERT16    ;TIMER 16 Hz SERVICE ROUTINE
CHKT2:
       FAN    B,IT2     ;CHECK TIMER 2 Hz INTERRUPT FLAG
       JP     Z,CHKT1   ;NO, THEN JUMP
       CALL   SERT2     ;TIMER 2 Hz SERVICE ROUTINE
```

```
CHKT1:
       FAN    B,IT1     ;CHECK TIMER 1 Hz INTERRUPT FLAG
       JP     Z,INTEND  ;NO, THEN JUMP
       CALL   SERT1     ;TIMER 1 Hz SERVICE ROUTINE
;
       LD     X,ZWDOG   ;RESET WATCHDOG
                        ; IN EVERY ONE 1 HZ INTERRUPT
       OR     MX,WDON
INTEND:                 ;END OF INTERRUPT
       EI
       RET
;
;* DIALING INTERRUPT SERVICE ROUTINE
DILINT:
       LD     X,ZID
       FAN    MX,ID
       JP     Z,INTEND
       CALL   SERDIL
       JP     INTEND
;
;* K0 INTERRUPT SERVICE ROUTINE
K0INT:
       LD     X,ZIK0
       FAN    MX,IK0    ;CHECK K0 INTERRUPT FLAG
       JP     Z,INTEND  ;NO, THEN JUMP
       CALL   SERK0     ;K0 SERVICE ROUTINE
       JP     INTEND
;
;* K1 INTERRUPT SERVICE ROUTINE
K1INT:
       LD     X,ZIK1
       FAN    MX,IK1    ;CHECK K1 INTERRUPT FLAG
       JP     Z,INTEND  ;NO, THEN JUMP
       CALL   SERK1     ;K1 SERVICE ROUTINE
       JP     INTEND
;
;* K20-K21 INTERRUPT SERVICE ROUTINE
K2INT:
       LD     X,ZIK2
       FAN    MX,IK2    ;CHECK K2 INTERRUPT FLAG
       JP     Z,INTEND  ;NO, THEN JUMP
       CALL   SERK2     ;K2 SERVICE ROUTINE
       JP     INTEND
;
;* K22 INTERRUPT SERVICE ROUTINE
K22INT:
       LD     X,ZIK22
       FAN    MX,IK22   ;CHECK K22 INTERRUPT FLAG
       JP     Z,INTEND  ;NO, THEN JUMP
       CALL   SERK22    ;K22 SERVICE ROUTINE
       JP     INTEND

;
```

```
SERT32:
;       :
;       DO THE TIMER 32 Hz INTERRUPT
;       SERVICE ROUTINE HERE
;       :
        RET

;
SERT16:
;       :
;       DO THE TIMER 16 Hz INTERRUPT
;       SERVICE ROUTINE HERE
;       :
        RET
;

SERT2:
;       :
;       DO THE TIMER 2 Hz INTERRUPT
;       SERVICE ROUTINE HERE
;       :
        RET
;

SERT1:
;       :
;       DO THE TIMER 1 Hz INTERRUPT
;       SERVICE ROUTINE HERE
;       :
        RET
;

SERDIL:
;       :
;       DO THE DIALING INTERRUPT
;       SERVICE ROUTINE HERE
;       :
        RET
;

SERK0:
;       :
;       DO THE INPUT K0 INTERRUPT
;       SERVICE ROUTINE HERE
;       :
        RET
;

SERK1:
;       :
;       DO THE INPUT K1 INTERRUPT
;       SERVICE ROUTINE HERE
;       :
        RET
;
```

```
SERK2:
;       :
;       DO THE INPUT K2 INTERRUPT
;       SERVICE ROUTINE HERE
;       :
        RET
;

SERK22:
;       :
;       DO THE INPUT K22 INTERRUPT
;       SERVICE ROUTINE HERE
;       :
        RET
;
```

Programming notes

(1) The interrupt factor flag is set when the interrupt conditions are established, regardless of the setting of the interrupt mask register.

(2) Read the interrupt factor flag in the DI status (interrupt flag = "0"). Reading of interrupt factor flag is available at EI, but be careful in the following cases.
If the interrupt mask register value corresponding to the interrupt factor flags to be read is set to "1", an interrupt request will be generated by the interrupt factor flags set timing, or an interrupt request will not be generated. Be very careful when interrupt factor flags are in the same address.

(3) Be sure that writing to the interrupt mask register is done with the interrupt in the DI status (interrupt flag = "0"). Writing to the interrupt mask register while in the EI status (interrupt flag = "1") may cause malfunction.

(4) When multiple interrupts simultaneously occur, the high priority vector address is set to the program counter.

CHAPTER 7 SUMMARY OF NOTES

7.1 Notes for Low Current Consumption

The E0C62T3 contains control registers for each of the circuits so that current consumption can be lowered. These control registers lower the current consumption through programs that operate the circuits at the minimum levels.
The following text explains the circuits that can control operation and their control registers. Refer to these when putting programs together.

Table 7.1.1 Circuits and control registers

Circuits (and items)	Control registers	Order of consumed current
CPU	HALT instruction	See electrical characteristics (*)
CPU operating frequency	CLKCHG, OSCC	See electrical characteristics (*)
SVD circuit	SVDON	Several tens µA

* "E0C62T3 Technical Hardware", Chapter 7

Below are the circuit statuses at initial reset.

CPU: Operating status

CPU operating frequency: Low speed side (CLKCHG = "0"),
OSC3 oscillation circuit OFF status (OSCC = "0")

SVD circuit: OFF status (SVDON = "0")

7.2 Summary of Notes by Function

Here, the cautionary notes are summed up by function category. Keep these notes well in mind when programming.

System initialization

In some of initial registers and initial data memory area, the initial value is undefined after reset. Set them proper initial values by the program, as necessary.

Memory

Memory is not mounted in unused area within the memory map and in memory area not indicated in this manual. For this reason, normal operation cannot be assured for programs that have been prepared with access to these areas.

Watchdog timer

(1) The watchdog timer must reset within 3-second cycles by the software. In this case, timer data (WD1 and WD0) cannot be used for timer applications.

(2) When clock timer resetting (TMRST ← "1") is performed, the watchdog timer is also reset.

Oscillation circuit

(1) It takes at least 5 msec from the time the OSC3 oscillation circuit goes ON until the oscillation stabilizes. Consequently, when switching the CPU operation clock from OSC1 to OSC3, do this after a minimum of 5 msec have elapsed since the OSC3 oscillation went ON.
Further, the oscillation stabilization time varies depending on the external oscillator characteristics and conditions of use, so allow ample margin when setting the wait time.

(2) When switching the clock from OSC3 to OSC1, use a separate instruction for switching the OSC3 oscillation OFF. An error in the CPU operation can result if this processing is performed at the same time by the one instruction.

(3) To lessen current consumption, keep OSC3 oscillation OFF except when the CPU must be run at high speed, or when DTMF is used.

Input ports

(1) When input ports are changed from low to high by pull up resistor, the rise of the waveform is delayed on account of the time constant of the pull up resistor and input gate capacitance. Hence, when fetching input ports, set an appropriate wait time.
Particular care needs to be taken of the key scan during key matrix configuration. Aim for a wait time of about 1 msec.

(2) When an interrupt occurs, for example, a key been pressed, software must has the debounce routine, to insure the input port interrupt stable, then to read out the interrupt flag for resetting interrupt flag. If no debounce routine, the input might interrupt many times.

Output ports

(1) When BZ and $\overline{BZ}$ output are selected by software, a hazard may be observed in the output waveform when the data of the output register changes.

(2) When R10 terminal is used for general output port, set BZR10 register to "0". When R10 terminal is used for $\overline{BZ}$ output port, set R10 register to "0".

(3) When R11 terminal is used for general output port, set BZR11 register to "0". When R11 terminal is used for BZ output port, set R11 register to "0".

(4) When R12 terminal is used for general output port, set CHDO register to "0". When R12 terminal is used for HOLD output port, set R12 register to "0".

(5) When R13 terminal is used for general output port, set CHFO register to "0". When R13 terminal is used for HANDFREE output port, set R13 register to "0".

I/O ports

When in the input mode, I/O port is changed from low to high by pull up resistor, the rise of the waveform is delayed on account of the time constant of the pull up resistor and input gate capacitance. Hence, when fetching input port, set an appropriate wait time.

LCD driver

(1) The contents of the display memory are undefined until the area is initialized (through, for instance, memory clear processing by the CPU). Initialize the display memory by executing initial processing.

(2) Since the display memory area is write-only, display data cannot be rewritten by arithmetic operations (such as AND, OR, ADD, SUB).

Clock timer

(1) Clock timer data is not reset at initial reset. It can be reset by software, writing "1" to TMRST.

(2) When the clock timer has been reset, the interrupt factor flag (IT) may sometimes be set to "1". Consequently, perform flag read (reset the flag) as necessary at reset.

(3) When reading both timer data, TMH (DBH) and TML (DAH), after reading TML, TMH should be read within 0.5 msec, otherwise, the hardware can not guarantee the readout is correct.

SVD (Supply voltage detection) circuit

(1) The SVD circuit should normally be turned OFF (SVDON = "0") as the consumption current of the IC becomes large when it is ON (SVDON = "1").

(2) To obtain a stable result, the SVD circuit must be set to ON with at least 100 µsec. Hence, to obtain the SVD detection result, follow the programming sequence below.

1. Set SVDON to "1" (ON)
2. Maintain at least 100 µsec minimum
3. Set SVDON to "0" (OFF)
4. Read out SVDDT

However, when a crystal oscillation clock (fosc1) is selected for CPU system clock, the instruction cycle are long enough, so that there is no need for concern about maintaining 100 µsec for the SVDON = "1" with the software.

Telephone function

(1) When uses the DTMF, it is necessary to turn ON the 3.58 MHz oscillator. This function needs big current. Therefore, using DTMF dialing at off-hook or handfree status is the best.

(2) Before using the telephone, software program should set HSON (E9H•D0) register to "1" for OFF-HOOK state ($\overline{DP}$ terminal goes high level).

(3) If software program writes a code of "0H" into TCD register in pulse mode, IDP, FTS or PTS registers, it will cause a malfunction.

(4) Because pause function control register (E3H•D1) and flash function control register (E3H•D0) are write-only, software cannot use ALU instructions (AND, OR ...) on E3H resisters while dialing a pause or flash function cycle.

Interrupt

(1) The interrupt factor flag is set when the interrupt conditions are established, regardless of the setting of the interrupt mask register.

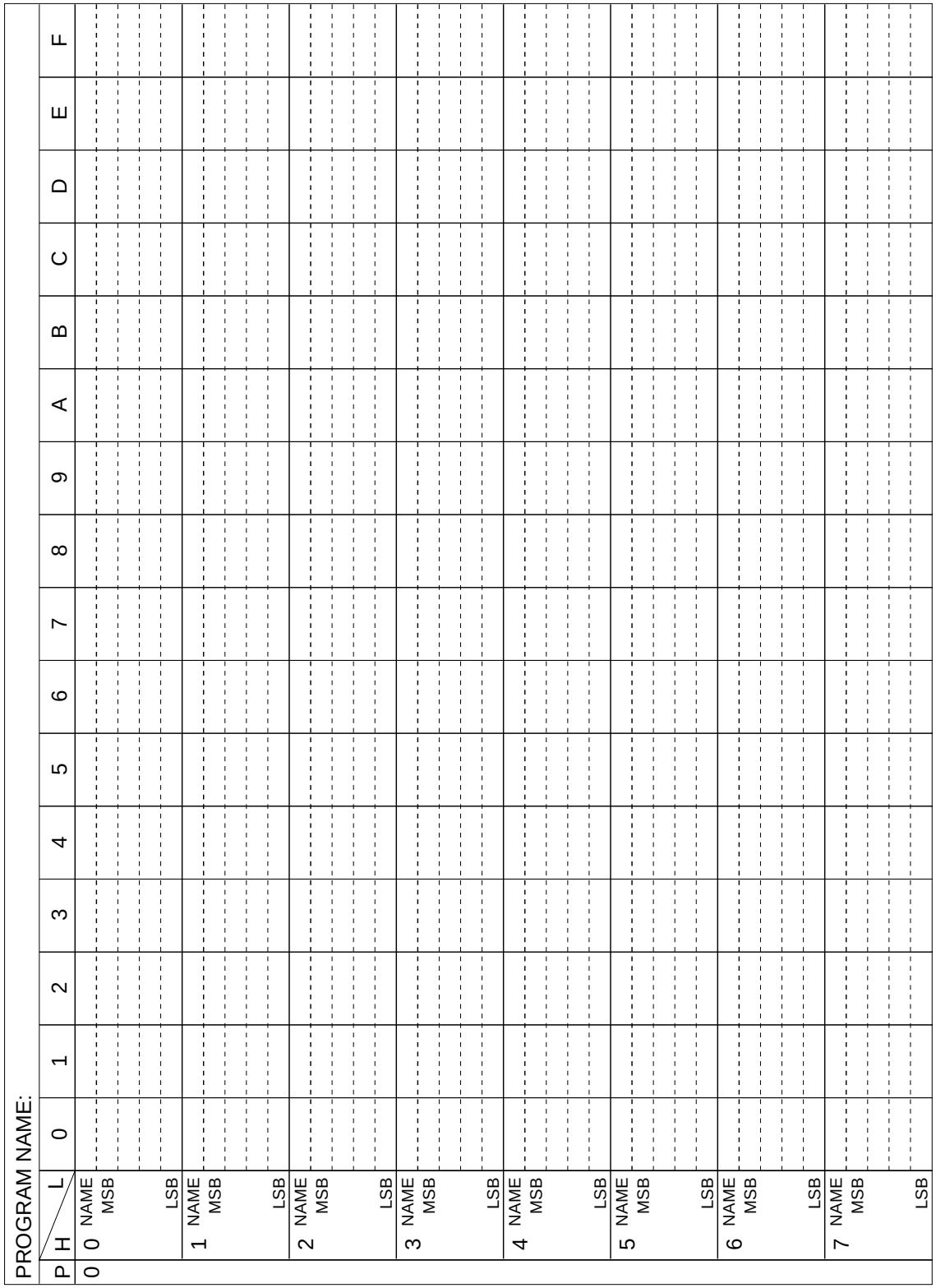
(2) Read the interrupt factor flag in the DI status (interrupt flag = "0"). Reading of interrupt factor flag is available at EI, but be careful in the following cases.
If the interrupt mask register value corresponding to the interrupt factor flags to be read is set to "1", an interrupt request will be generated by the interrupt factor flags set timing, or an interrupt request will not be generated. Be very careful when interrupt factor flags are in the same address.

(3) Be sure that writing to the interrupt mask register is done with the interrupt in the DI status (interrupt flag = "0"). Writing to the interrupt mask register while in the EI status (interrupt flag = "1") may cause malfunction.

(4) When multiple interrupts simultaneously occur, the high priority vector address is set to the program counter.

APPENDIX A E0C62T3 DATA MEMORY (RAM) MAP

RAM map - 1 (000H–07FH)



RAM map - 2 (100H–17FH)

PROGRAM NAME:

P	H \ L	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
1	0	NAME MSB															LSB
	1	NAME MSB															LSB
	2	NAME MSB															LSB
	3	NAME MSB															LSB
	4	NAME MSB															LSB
	5	NAME MSB															LSB
	6	NAME MSB															LSB
	7	NAME MSB															LSB

RAM map - 3 (200H–27FH)

PROGRAM NAME:

P	H \ L	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
2	0	NAME MSB															
		LSB															
	1	NAME MSB															
		LSB															
	2	NAME MSB															
		LSB															
	3	NAME MSB															
		LSB															
	4	NAME MSB															
		LSB															
	5	NAME MSB															
		LSB															
	6	NAME MSB															
		LSB															
	7	NAME MSB															
		LSB															

RAM map - 4 (300H–37FH)

PROGRAM NAME:

P H \ L	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
3 0	NAME MSB LSB															
1	NAME MSB LSB															
2	NAME MSB LSB															
3	NAME MSB LSB															
4	NAME MSB LSB															
5	NAME MSB LSB															
6	NAME MSB LSB															
7	NAME MSB LSB															

RAM map - 5 (400H–47FH)

PROGRAM NAME:

P	H \ L	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
4	0	NAME MSB															LSB
	1	NAME MSB															LSB
	2	NAME MSB															LSB
	3	NAME MSB															LSB
	4	NAME MSB															LSB
	5	NAME MSB															LSB
	6	NAME MSB															LSB
	7	NAME MSB															LSB

Display memory (80H–AFH), I/O memory (C0H–EFH)

PROGRAM NAME:

P	H \ L	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	8 NAME																
	MSB																
1																	
2																	
	LSB																
3	9 NAME																
	MSB																
4																	
	LSB																
	A NAME																
	MSB																
	LSB																
	C NAME	ZIK22	ZIK2	ZIK1	ZIK0	ZIT	ZID	ZSIK2	ZSIK1	ZSIK0	ZK2	ZK1	ZK0	ZDFK2	ZDFK1	ZDFK0	–
	MSB	0	0	0	0	IT1	0	0	SIK13	SIK03	0	K13	K03	0	DFK13	DFK03	–
		0	0	0	0	IT2	0	0	SIK12	SIK02	K22	K12	K02	DFK22	DFK12	DFK02	–
		0	0	0	0	IT16	0	SIK21	SIK11	SIK01	K21	K11	K01	DFK21	DFK11	DFK01	–
	LSB	IK22	IK2	IK1	IK0	IT32	ID	SIK20	SIK10	SIK00	K20	K10	K00	DFK20	DFK10	DFK00	–
	D NAME	ZEIK	ZEIT	ZEID	ZR1	ZR0	ZIOC	ZPUP	ZP0	ZOSCC	ZTMRST	ZTML	ZTMH	ZWDOG	ZBZCTL	ZLCDC	ZSVDC
	MSB	EIK22	EIT1	0	R13	R03	IOC3	PUP3	P03	0	0	TM3	TM7	WDON	BZR11	LDTY1	0
		EIK2	EIT2	0	R12	R02	IOC2	PUP2	P02	0	0	TM2	TM6	WDRST	BZR10	LDTY0	0
		EIK1	EIT16	0	R11	R01	IOC1	PUP1	P01	CLKCHG	0	TM1	TM5	WD1	0	0	SVDDT
	LSB	EIK0	EIT32	EID	R10	R00	IOC0	PUP0	P00	OSCC	TMRST	TM0	TM4	WD0	BZFQ	LCDON	SVDON
	E NAME	ZTPS	ZPTS	ZFTS	ZHOLD	ZHF	ZIDP	ZSIN	ZTCD	ZMUT	ZHSON	ZCHFO	ZCTO	–	–	–	–
	MSB	TPS	PTS3	FTS3	0	HF	IDP3	0	TCD3	0	0	CHFO	CTO	–	–	–	–
		0	PTS2	FTS2	HOLD	0	IDP2	0	TCD2	0	0	CHDO	0	–	–	–	–
		MB	PTS1	FTS1	PAUSE	0	IDP1	SINR	TCD1	CRMUT	0	0	0	–	–	–	–
	LSB	DRS	PTS0	FTS0	FLASH	0	IDP0	SINC	TCD0	CTMUT	HSON	0	0	–	–	–	–

APPENDIX B E0C62T3 INSTRUCTION SET

Instruction set - 1

Classification	Mnemonic	Operand	Operation Code												Flag				Clock	Operation
			B	A	9	8	7	6	5	4	3	2	1	0	I	D	Z	C		
Branch instructions	PSET	p	1	1	1	0	0	1	0	p4	p3	p2	p1	p0					5	NBP ← p4, NPP ← p3~p0
	JP	s	0	0	0	0	s7	s6	s5	s4	s3	s2	s1	s0					5	PCB ← NBP, PCP ← NPP, PCS ← s7~s0
		C, s	0	0	1	0	s7	s6	s5	s4	s3	s2	s1	s0					5	PCB ← NBP, PCP ← NPP, PCS ← s7~s0 if C=1
		NC, s	0	0	1	1	s7	s6	s5	s4	s3	s2	s1	s0					5	PCB ← NBP, PCP ← NPP, PCS ← s7~s0 if C=0
		Z, s	0	1	1	0	s7	s6	s5	s4	s3	s2	s1	s0					5	PCB ← NBP, PCP ← NPP, PCS ← s7~s0 if Z=1
		NZ, s	0	1	1	1	s7	s6	s5	s4	s3	s2	s1	s0					5	PCB ← NBP, PCP ← NPP, PCS ← s7~s0 if Z=0
	JPBA		1	1	1	1	1	1	1	0	1	0	0	0					5	PCB ← NBP, PCP ← NPP, PCSH ← B, PCSL ← A
	CALL	s	0	1	0	0	s7	s6	s5	s4	s3	s2	s1	s0					7	M(SP-1) ← PCP, M(SP-2) ← PCSH, M(SP-3) ← PCSL+1 SP ← SP-3, PCP ← NPP, PCS ← s7~s0
	CALZ	s	0	1	0	1	s7	s6	s5	s4	s3	s2	s1	s0					7	M(SP-1) ← PCP, M(SP-2) ← PCSH, M(SP-3) ← PCSL+1 SP ← SP-3, PCP ← 0, PCS ← s7~s0
	RET		1	1	1	1	1	1	0	1	1	1	1	1					7	PCSL ← M(SP), PCSH ← M(SP+1), PCP ← M(SP+2) SP ← SP+3
	RETS		1	1	1	1	1	1	0	1	1	1	1	0					12	PCSL ← M(SP), PCSH ← M(SP+1), PCP ← M(SP+2) SP ← SP+3, PC ← PC+1
	RETD	*l*	0	0	0	1	*l*7	*l*6	*l*5	*l*4	*l*3	*l*2	*l*1	*l*0					12	PCSL ← M(SP), PCSH ← M(SP+1), PCP ← M(SP+2) SP ← SP+3, M(X) ← *l*3~*l*0, M(X+1) ← *l*7~*l*4, X ← X+2
System control instructions	NOP5		1	1	1	1	1	1	1	1	1	0	1	1					5	No operation (5 clock cycles)
	NOP7		1	1	1	1	1	1	1	1	1	1	1	1					7	No operation (7 clock cycles)
	HALT		1	1	1	1	1	1	1	1	1	0	0	0					5	Halt (stop clock)
Index operation instructions	INC	X	1	1	1	0	1	1	1	0	0	0	0	0					5	X ← X+1
		Y	1	1	1	0	1	1	1	1	0	0	0	0					5	Y ← Y+1
	LD	X, x	1	0	1	1	x7	x6	x5	x4	x3	x2	x1	x0					5	XH ← x7~x4, XL ← x3~x0
		Y, y	1	0	0	0	y7	y6	y5	y4	y3	y2	y1	y0					5	YH ← y7~y4, YL ← y3~y0
		XP, r	1	1	1	0	1	0	0	0	0	0	r1	r0					5	XP ← r
		XH, r	1	1	1	0	1	0	0	0	0	1	r1	r0					5	XH ← r
		XL, r	1	1	1	0	1	0	0	0	1	0	r1	r0					5	XL ← r
		YP, r	1	1	1	0	1	0	0	1	0	0	r1	r0					5	YP ← r
		YH, r	1	1	1	0	1	0	0	1	0	1	r1	r0					5	YH ← r
		YL, r	1	1	1	0	1	0	0	1	1	0	r1	r0					5	YL ← r
		r, XP	1	1	1	0	1	0	1	0	0	0	r1	r0					5	r ← XP
		r, XH	1	1	1	0	1	0	1	0	0	1	r1	r0					5	r ← XH
		r, XL	1	1	1	0	1	0	1	0	1	0	r1	r0					5	r ← XL
		r, YP	1	1	1	0	1	0	1	1	0	0	r1	r0					5	r ← YP
		r, YH	1	1	1	0	1	0	1	1	0	1	r1	r0					5	r ← YH
		r, YL	1	1	1	0	1	0	1	1	1	0	r1	r0					5	r ← YL
	ADC	XH, i	1	0	1	0	0	0	0	0	i3	i2	i1	i0			↕	↕	7	XH ← XH+i3~i0+C
		XL, i	1	0	1	0	0	0	0	1	i3	i2	i1	i0			↕	↕	7	XL ← XL+i3~i0+C
		YH, i	1	0	1	0	0	0	1	0	i3	i2	i1	i0			↕	↕	7	YH ← YH+i3~i0+C
		YL, i	1	0	1	0	0	0	1	1	i3	i2	i1	i0			↕	↕	7	YL ← YL+i3~i0+C

Instruction set - 2

Classification	Mnemonic	Operand	Operation Code												Flag				Clock	Operation
			B	A	9	8	7	6	5	4	3	2	1	0	I	D	Z	C		
Index operation instructions	CP	XH, i	1	0	1	0	0	1	0	0	i3	i2	i1	i0			↕	↕	7	XH-i3~i0
		XL, i	1	0	1	0	0	1	0	1	i3	i2	i1	i0			↕	↕	7	XL-i3~i0
		YH, i	1	0	1	0	0	1	1	0	i3	i2	i1	i0			↕	↕	7	YH-i3~i0
		YL, i	1	0	1	0	0	1	1	1	i3	i2	i1	i0			↕	↕	7	YL-i3~i0
Data transfer instructions	LD	r, i	1	1	1	0	0	0	r1	r0	i3	i2	i1	i0					5	r←i3~i0
		r, q	1	1	1	0	1	1	0	0	r1	r0	q1	q0					5	r←q
		A, Mn	1	1	1	1	1	0	1	0	n3	n2	n1	n0					5	A←M(n3~n0)
		B, Mn	1	1	1	1	1	0	1	1	n3	n2	n1	n0					5	B←M(n3~n0)
		Mn, A	1	1	1	1	1	0	0	0	n3	n2	n1	n0					5	M(n3~n0)←A
		Mn, B	1	1	1	1	1	0	0	1	n3	n2	n1	n0					5	M(n3~n0)←B
	LDPX	MX, i	1	1	1	0	0	1	1	0	i3	i2	i1	i0					5	M(X)←i3~i0, X←X+1
		r, q	1	1	1	0	1	1	1	0	r1	r0	q1	q0					5	r←q, X←X+1
	LDPY	MY, i	1	1	1	0	0	1	1	1	i3	i2	i1	i0					5	M(Y)←i3~i0, Y←Y+1
		r, q	1	1	1	0	1	1	1	1	r1	r0	q1	q0					5	r←q, Y←Y+1
	LBPX	MX, *l*	1	0	0	1	*l*7	*l*6	*l*5	*l*4	*l*3	*l*2	*l*1	*l*0					5	M(X)←*l*3~*l*0, M(X+1)←*l*7~*l*4, X←X+2
Flag operation instructions	SET	F, i	1	1	1	1	0	1	0	0	i3	i2	i1	i0	↑	↑	↑	↑	7	F←F∨i3~i0
	RST	F, i	1	1	1	1	0	1	0	1	i3	i2	i1	i0	↓	↓	↓	↓	7	F←F∧i3~i0
	SCF		1	1	1	1	0	1	0	0	0	0	0	1				↑	7	C←1
	RCF		1	1	1	1	0	1	0	1	1	1	1	0				↓	7	C←0
	SZF		1	1	1	1	0	1	0	0	0	0	1	0			↑		7	Z←1
	RZF		1	1	1	1	0	1	0	1	1	1	0	1			↓		7	Z←0
	SDF		1	1	1	1	0	1	0	0	0	1	0	0		↑			7	D←1 (Decimal Adjuster ON)
	RDF		1	1	1	1	0	1	0	1	1	0	1	1		↓			7	D←0 (Decimal Adjuster OFF)
	EI		1	1	1	1	0	1	0	0	1	0	0	0	↑				7	I←1 (Enables Interrupt)
	DI		1	1	1	1	0	1	0	1	0	1	1	1	↓				7	I←0 (Disables Interrupt)
Stack operation instructions	INC	SP	1	1	1	1	1	1	0	1	1	0	1	1					5	SP←SP+1
	DEC	SP	1	1	1	1	1	1	0	0	1	0	1	1					5	SP←SP-1
	PUSH	r	1	1	1	1	1	1	0	0	0	0	r1	r0					5	SP←SP-1, M(SP)←r
		XP	1	1	1	1	1	1	0	0	0	1	0	0					5	SP←SP-1, M(SP)←XP
		XH	1	1	1	1	1	1	0	0	0	1	0	1					5	SP←SP-1, M(SP)←XH
		XL	1	1	1	1	1	1	0	0	0	1	1	0					5	SP←SP-1, M(SP)←XL
		YP	1	1	1	1	1	1	0	0	0	1	1	1					5	SP←SP-1, M(SP)←YP
		YH	1	1	1	1	1	1	0	0	1	0	0	0					5	SP←SP-1, M(SP)←YH
		YL	1	1	1	1	1	1	0	0	1	0	0	1					5	SP←SP-1, M(SP)←YL
		F	1	1	1	1	1	1	0	0	1	0	1	0					5	SP←SP-1, M(SP)←F
	POP	r	1	1	1	1	1	1	0	1	0	0	r1	r0					5	r←M(SP), SP←SP+1
		XP	1	1	1	1	1	1	0	1	0	1	0	0					5	XP←M(SP), SP←SP+1
		XH	1	1	1	1	1	1	0	1	0	1	0	1					5	XH←M(SP), SP←SP+1
		XL	1	1	1	1	1	1	0	1	0	1	1	0					5	XL←M(SP), SP←SP+1
		YP	1	1	1	1	1	1	0	1	0	1	1	1					5	YP←M(SP), SP←SP+1

Instruction set - 3

Classification	Mnemonic	Operand	Operation Code												Flag				Clock	Operation
			B	A	9	8	7	6	5	4	3	2	1	0	I	D	Z	C		
Stack operation instructions	POP	YH	1	1	1	1	1	1	0	1	1	0	0	0					5	YH← M(SP), SP← SP+1
		YL	1	1	1	1	1	1	0	1	1	0	0	1					5	YL← M(SP), SP← SP+1
		F	1	1	1	1	1	1	0	1	1	0	1	0	↕	↕	↕	↕	5	F← M(SP), SP← SP+1
	LD	SPH, r	1	1	1	1	1	1	1	0	0	0	r1	r0					5	SPH← r
		SPL, r	1	1	1	1	1	1	1	1	0	0	r1	r0					5	SPL ← r
		r, SPH	1	1	1	1	1	1	1	0	0	1	r1	r0					5	r← SPH
		r, SPL	1	1	1	1	1	1	1	1	0	1	r1	r0					5	r← SPL
Arithmetic instructions	ADD	r, i	1	1	0	0	0	0	r1	r0	i3	i2	i1	i0	★	↕	↕		7	r← r+i3~i0
		r, q	1	0	1	0	1	0	0	0	r1	r0	q1	q0	★	↕	↕		7	r← r+q
	ADC	r, i	1	1	0	0	0	1	r1	r0	i3	i2	i1	i0	★	↕	↕		7	r← r+i3~i0+C
		r, q	1	0	1	0	1	0	0	1	r1	r0	q1	q0	★	↕	↕		7	r← r+q+C
	SUB	r, q	1	0	1	0	1	0	1	0	r1	r0	q1	q0	★	↕	↕		7	r← r-q
	SBC	r, i	1	1	0	1	0	1	r1	r0	i3	i2	i1	i0	★	↕	↕		7	r← r-i3~i0-C
		r, q	1	0	1	0	1	0	1	1	r1	r0	q1	q0	★	↕	↕		7	r← r-q-C
	AND	r, i	1	1	0	0	1	0	r1	r0	i3	i2	i1	i0		↕			7	r← r∧ i3~i0
		r, q	1	0	1	0	1	1	0	0	r1	r0	q1	q0		↕			7	r← r∧ q
	OR	r, i	1	1	0	0	1	1	r1	r0	i3	i2	i1	i0		↕			7	r← r∨i3~i0
		r, q	1	0	1	0	1	1	0	1	r1	r0	q1	q0		↕			7	r← r∨q
	XOR	r, i	1	1	0	1	0	0	r1	r0	i3	i2	i1	i0		↕			7	r← r∀i3~i0
		r, q	1	0	1	0	1	1	1	0	r1	r0	q1	q0		↕			7	r← r∀q
	CP	r, i	1	1	0	1	1	1	r1	r0	i3	i2	i1	i0		↕	↕		7	r-i3~i0
		r, q	1	1	1	1	0	0	0	0	r1	r0	q1	q0		↕	↕		7	r-q
	FAN	r, i	1	1	0	1	1	0	r1	r0	i3	i2	i1	i0		↕			7	r∧i3~i0
		r, q	1	1	1	1	0	0	0	1	r1	r0	q1	q0		↕			7	r∧q
	RLC	r	1	0	1	0	1	1	1	1	r1	r0	r1	r0		↕	↕		7	d3 ← d2, d2 ← d1, d1 ← d0, d0 ← C, C← d3
	RRC	r	1	1	1	0	1	0	0	0	1	1	r1	r0		↕	↕		5	d3 ← C, d2 ← d3, d1 ← d2, d0 ← d1, C← d0
	INC	Mn	1	1	1	1	0	1	1	0	n3	n2	n1	n0		↕	↕		7	M(n3~n0) ← M(n3~n0)+1
	DEC	Mn	1	1	1	1	0	1	1	1	n3	n2	n1	n0		↕	↕		7	M(n3~n0) ← M(n3~n0)-1
	ACPX	MX, r	1	1	1	1	0	0	1	0	1	0	r1	r0	★	↕	↕		7	M(X) ← M(X)+r+C, X ← X+1
	ACPY	MY, r	1	1	1	1	0	0	1	0	1	1	r1	r0	★	↕	↕		7	M(Y) ← M(Y)+r+C, Y ← Y+1
	SCPX	MX, r	1	1	1	1	0	0	1	1	1	0	r1	r0	★	↕	↕		7	M(X) ← M(X)-r-C, X ← X+1
	SCPY	MY, r	1	1	1	1	0	0	1	1	1	1	r1	r0	★	↕	↕		7	M(Y) ← M(Y)-r-C, Y ← Y+1
	NOT	r	1	1	0	1	0	0	r1	r0	1	1	1	1		↕			7	r← $\overline{r}$

Abbreviations used in the explanations have the following meanings.

Symbols associated with registers and memory

A ..... A register
B ..... B register
X ..... XHL register (low order eight bits of index register IX)
Y ..... YHL register (low order eight bits of index register IY)
XH ..... XH register (high order four bits of XHL register)
XL ..... XL register (low order four bits of XHL register)
YH ..... YH register (high order four bits of YHL register)
YL ..... YL register (low order four bits of YHL register)
XP ..... XP register (high order four bits of index register IX)
YP ..... YP register (high order four bits of index register IY)
SP ..... Stack pointer SP
SPH ..... High-order four bits of stack pointer SP
SPL ..... Low-order four bits of stack pointer SP
MX, M(X) .... Data memory whose address is specified with index register IX
MY, M(Y)..... Data memory whose address is specified with index register IY
Mn, M(n) .... Data memory address 000H–00FH (address specified with immediate data n of 00H–0FH)
M(SP) ..... Data memory whose address is specified with stack pointer SP
r, q ..... Two-bit register code
r, q is two-bit immediate data; according to the contents of these bits, they indicate registers A, B, and MX and MY (data memory whose addresses are specified with index registers IX and IY)

r		q		Registers specified
r1	r0	q1	q0	
0	0	0	0	A
0	1	0	1	B
1	0	1	0	MX
1	1	1	1	MY

Symbols associated with program counter

NBP ..... New bank pointer
NPP ..... New page pointer
PCB ..... Program counter bank
PCP ..... Program counter page
PCS ..... Program counter step
PCSH .... Four high order bits of PCS
PCSL ..... Four low order bits of PCS

Symbols associated with flags

F ..... Flag register (I, D, Z, C)
C ..... Carry flag
Z ..... Zero flag
D ..... Decimal flag
I ..... Interrupt flag
↓ ..... Flag reset
↑ ..... Flag set
↕ ..... Flag set or reset

Associated with immediate data

p ..... Five-bit immediate data or label 00H–1FH
s ..... Eight-bit immediate data or label 00H–0FFH
l ..... Eight-bit immediate data 00H–0FFH
i ..... Four-bit immediate data 00H–0FH

Associated with arithmetic and other operations

+ ..... Add
- ..... Subtract
∧ ..... Logical AND
∨ ..... Logical OR
∀ ..... Exclusive-OR
★ ..... Add-subtract instruction for decimal operation when the D flag is set

APPENDIX C PSEUDO-INSTRUCTION TABLE OF THE CROSS ASSEMBLER

Item No.	Pseudo-instruction	Meaning	Example of Use
1	EQU (Equation)	To allocate data to label	`ABC EQU 9` `BCD EQU ABC+1`
2	ORG (Origin)	To define location counter	`ORG 100H` `ORG 256`
3	SET (Set)	To allocate data to label (data can be changed)	`ABC SET 0001H` `ABC SET 0002H`
4	DW (Define Word)	To define ROM data	`ABC DW 'AB'` `BCD DW 0FFBH`
5	PAGE (Page)	To define boundary of page	`PAGE 1H` `PAGE 3`
6	SECTION (Section)	To define boundary of section	`SECTION`
7	END (End)	To terminate assembly	`END`

8	MACRO
	(Macro)
		To define macro	`CHECK MACRO DATA`
			`LOCAL LOOP`
			`LOOP CP MX,DATA`
			`JP NZ,LOOP`
			`ENDM`
			
			`CHECK 1`

9	LOCAL (Local)	To make local specification of label during macro definition	
10	ENDM (End Macro)	To end macro definition	

APPENDIX D COMMAND TABLE OF ICE6200

ICE6200 command table - 1

Item No.	Function	Command Format	Outline of Operation
1	Assemble	#A,a ↵	Assemble command mnemonic code and store at address "a"
2	Disassemble	#L,a1,a2 ↵	Contents of addresses a1 to a2 are disassembled and displayed
3	Dump	#DP,a1,a2 ↵	Contents of program area a1 to a2 are displayed
		#DD,a1,a2 ↵	Content of data area a1 to a2 are displayed
4	Fill	#FP,a1,a2,d ↵	Data d is set in addresses a1 to a2 (program area)
		#FD,a1,a2,d ↵	Data d is set in addresses a1 to a2 (data area)
5	Set Run Mode	#G,a ↵	Program is executed from the "a" address
		#TIM ↵	Execution time and step counter selection
		#OTF ↵	On-the-fly display selection
6	Trace	#T,a,n ↵	Executes program while displaying results of step instruction from "a" address
		#U,a,n ↵	Displays only the final step of #T,a,n
7	Break	#BA,a ↵	Sets Break at program address "a"
		#BAR,a ↵	Breakpoint is canceled
		#BD ↵	Break condition is set for data RAM
		#BDR ↵	Breakpoint is canceled
		#BR ↵	Break condition is set for EVA62XXCPU internal registers
		#BRR ↵	Breakpoint is canceled
		#BM ↵	Combined break conditions set for program data RAM address and registers
		#BMR ↵	Cancel combined break conditions for program data ROM address and registers
		#BRES ↵	All break conditions canceled
		#BC ↵	Break condition displayed
		#BE ↵	Enter break enable mode
		#BSYN ↵	Enter break disable mode
		#BT ↵	Set break stop/trace modes
		#BRKSEL,REM ↵	Set BA condition clear/remain modes
8	Move	#MP,a1,a2,a3 ↵	Contents of program area addresses a1 to a2 are moved to addresses a3 and after
		#MD,a1,a2,a3 ↵	Contents of data area addresses a1 to a2 are moved to addresses a3 and after
9	Data Set	#SP,a ↵	Data from program area address "a" are written to memory
		#SD,a ↵	Data from data area address "a" are written to memory
10	Change CPU Internal Registers	#DR ↵	Display EVA62XXCPU internal registers
		#SR ↵	Set EVA62XXCPU internal registers
		#I ↵	Reset EVA62XXCPU
		#DXY ↵	Display X, Y, MX and MY
		#SXY ↵	Set data for X and Y display and MX, MY

ICE6200 command table - 2

Item No.	Function	Command Format	Outline of Operation
11	History	#H,p1,p2 ↵	Display history data for pointer 1 and pointer 2
		#HB ↵	Display upstream history data
		#HG ↵	Display 21 line history data
		#HP ↵	Display history pointer
		#HPS,a ↵	Set history pointer
		#HC,S/C/E ↵	Sets up the history information acquisition before (S), before/after (C) and after (E)
		#HA,a1,a2 ↵	Sets up the history information acquisition from program area a1 to a2
		#HAR,a1,a2 ↵	Sets up the prohibition of the history information acquisition from program area a1 to a2
		#HAD ↵	Indicates history acquisition program area
		#HS,a ↵	Retrieves and indicates the history information which executed a program address "a"
		#HSW,a ↵ #HSR,a ↵	Retrieves and indicates the history information which wrote or read the data area address "a"
12	File	#RF,file ↵	Move program file to memory
		#RFD,file ↵	Move data file to memory
		#VF,file ↵	Compare program file and contents of memory
		#VFD,file ↵	Compare data file and contents of memory
		#WF,file ↵	Save contents of memory to program file
		#WFD,file ↵	Save contents of memory to data file
		#CL,file ↵	Load ICE6200 set condition from file
		#CS,file ↵	Save ICE6200 set condition to file
13	Coverage	#CVD ↵	Indicates coverage information
		#CVR ↵	Clears coverage information
14	ROM Access	#RP ↵	Move contents of ROM to program memory
		#VP ↵	Compare contents of ROM with contents of program memory
		#ROM ↵	Set ROM type
15	Terminate ICE	#Q ↵	Terminate ICE and return to operating system control
16	Command Display	#HELP ↵	Display ICE6200 instruction
17	Self Diagnosis	#CHK ↵	Report results of ICE6200 self diagnostic test

↵ means press the RETURN key.

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