MF842-03

EPSON

CMOS 4-BIT SINGLE CHIP MICROCOMPUTER

E0C6S37 TECHNICAL MANUAL

E0C6S37 Technical Hardware

E0C6S37 Technical Software

ENERGY SAVING EPSON

SEIKO EPSON CORPORATION

PREFACE

This manual is individualy described about the hardware and the software of the E0C6S37.

I. E0C6S37 Technical Hardware

This part explains the function of the E0C6S37, the circuit configurations, and details the controlling method.

II. E0C6S37 Technical Software

This part explains the programming method of the E0C6S37.

I. E0C6S37 Technical Hardware

CONTENTS

CHAPTER 1 INTRODUCTION

Each member of the E0C6S37 Series of single chip microcomputers feature a 4-bit E0C6200A core CPU, 1,024 words of ROM (12 bits per word), 80 words of RAM (4 bits per word), an LCD driver, 4 bits for input ports (K00–K03), 4 bits for output ports (R00–R03), one 4-bit I/O port (P00–P03) and two timer (clock timer and stopwatch timer).

Because of their low voltage operation and low power consumption, the E0C6S37 Series are ideal for a wide range of applications.

1.1 Configuration

The E0C6S37 Series are configured as follows, depending on the supply voltage.

Table 1.1.1 Configuration of the E0C6S37 Series

Model	Supply Voltage	Supply Voltage Range	Oscillation Circuits
E0C6S37	3.0 V	1.8–3.6 V	Crystal or CR
E0C6SL37	1.5 V	0.9–2.0 V	Crystal or CR
E0C6SB37	3.0 V	0.9–3.6 V	Crystal or CR

1.2 Features

Built-in oscillation circuit	Crystal or CR oscillation circuit, 32.768 kHz (typ.)	
Instruction set	100 instructions	
ROM capacity	1,024 words ×12 bits	
RAM capacity (data RAM)	80 words × 4 bits	
Input port	4 bits (Supplementary pull-down resistors may be used)	
Output port	4 bits (Piezo buzzer and programmable frequency output can be driven directry by mask option)	
Input/output port	4 bits	
LCD driver	26 segments × 4, 3 or 2 common duty	
Timer	2 systems: clock timer/stopwatch timer	
Supply voltage detection circuit (SVD)	1.2 V / 2.4 V	
Interrupts:		
External interrupt	Input port interrupt	1 system
Internal interrupt	Timer interrupt	2 systems
Supply voltage	1.5 V (0.9–2.0 V)	E0C6SL37
	3.0 V (1.8–3.6 V)	E0C6S37
	3.0 V (0.9–3.6 V)	E0C6SB37
Current consumption (typ.)	1.0 µA (Crystal oscillation CLK = 32.768 kHz, when halted) 2.5 µA (Crystal oscillation CLK = 32.768 kHz, when executing)	
Supply form	QFP6-60pin (plastic) or chip	

1.3 Block Diagram

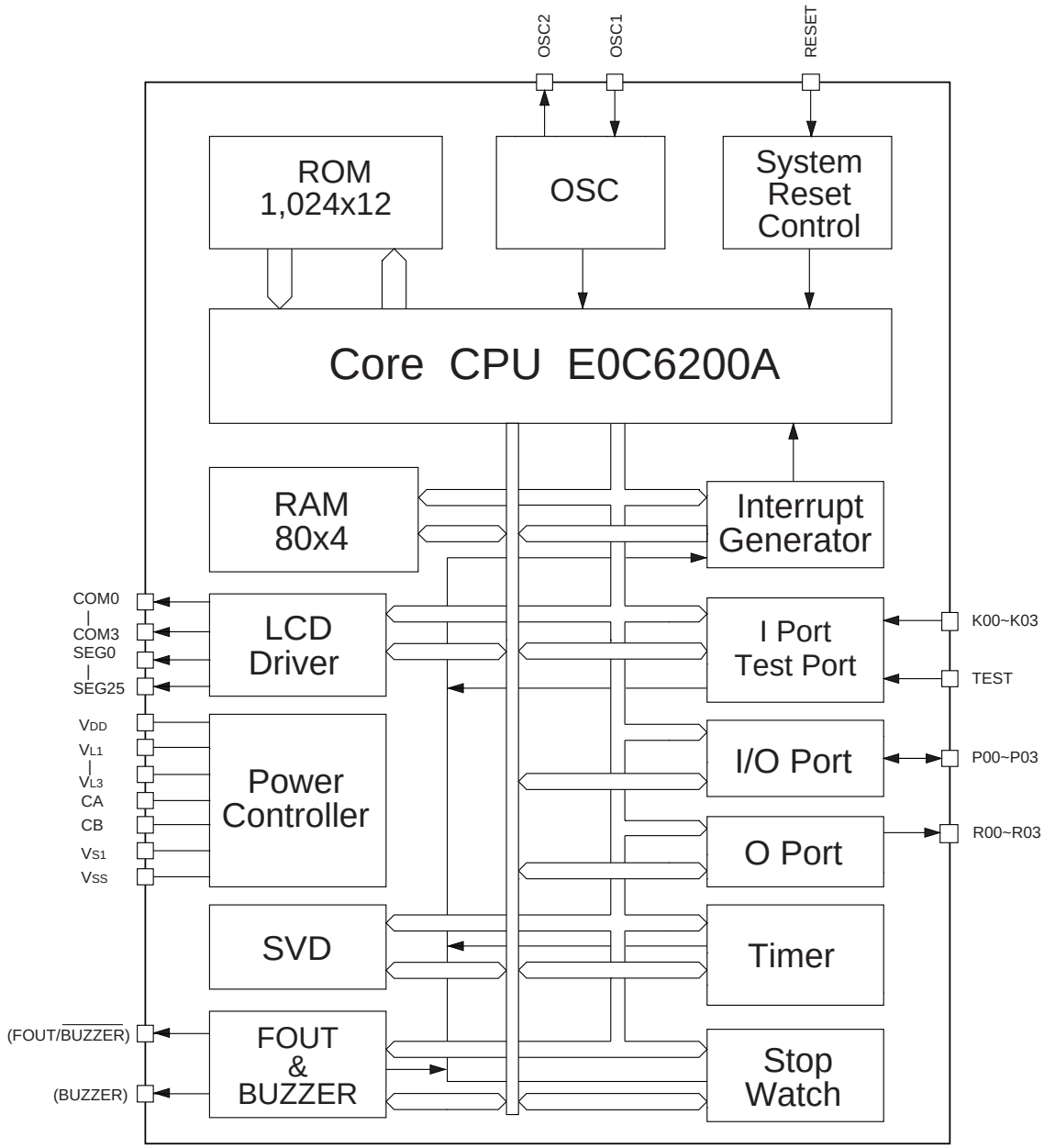
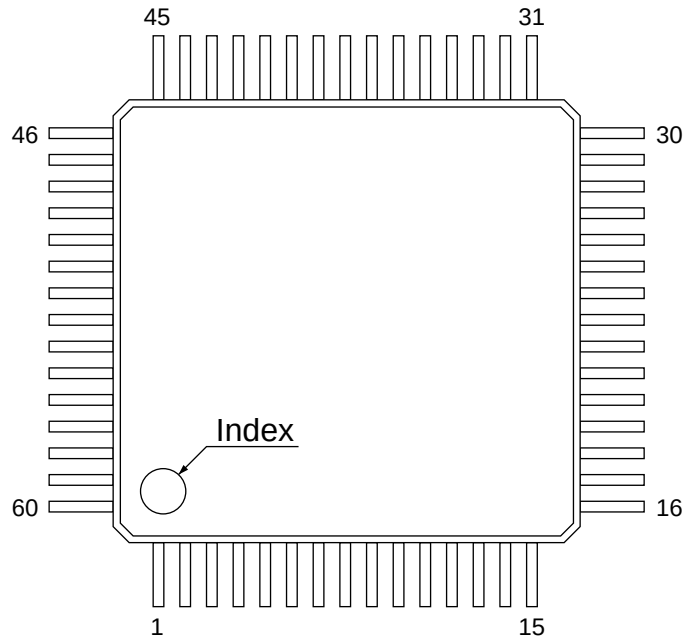


Fig. 1.3.1
Block diagram

1.4 Pin Layout Diagram

QFP6-60pin



Pin No	Pin Name	Pin No	Pin Name	Pin No	Pin Name	Pin No	Pin Name
1	OSC1	16	COM2	31	TEST	46	P01
2	OSC2	17	COM3	32	SEG13	47	P02
3	N.C.	18	SEG0	33	SEG14	48	P03
4	V_{S1}	19	SEG1	34	SEG15	49	RESET
5	N.C.	20	SEG2	35	SEG16	50	K00
6	CA	21	SEG3	36	SEG17	51	K01
7	CB	22	SEG4	37	SEG18	52	K02
8	N.C.	23	SEG5	38	SEG19	53	K03
9	N.C.	24	SEG6	39	SEG20	54	R00
10	N.C.	25	SEG7	40	SEG21	55	R01
11	V_{L1}	26	SEG8	41	SEG22	56	R02
12	V_{L2}	27	SEG9	42	SEG23	57	R03
13	V_{L3}	28	SEG10	43	SEG24	58	N.C.
14	COM0	29	SEG11	44	SEG25	59	V_{SS}
15	COM1	30	SEG12	45	P00	60	V_{DD}

Fig. 1.4.1
Pin assignment

N.C. = No Connection

1.5 Pin Description

Table 1.5.1 Pin description

Terminal Name	Pin No.	Input/Output	Function
V_{DD}	60	(I)	Power source (+) terminal
V_{SS}	59	(I)	Power source (-) terminal
V_{S1}	4	O	Oscillation and internal logic system regulated voltage output terminal
V_{L1}	11	O	LCD system regulated voltage output terminal (approx. -1.05 V) / LCD system reducer output terminal ($V_{L2} \times 1/2$)
V_{L2}	12	O	LCD system booster output terminal ($V_{L1} \times 2$) / LCD system booster output terminal (approx. -2.10 V)
V_{L3}	13	O	LCD system booster output terminal ($V_{L1} \times 3$) / LCD system booster output terminal ($V_{L2} \times 3/2$)
CA–CB	6, 7	–	Booster capacitor connecting terminal
OSC1	1	I	Crystal or CR oscillation input terminal
OSC2	2	O	Crystal or CR oscillation output terminal
K00–K03	50–53	I	Input terminal
P00–P03	45–48	I/O	I/O terminal
R00–R03	54–57	O	Output terminal
SEG0–25	18–30 32–44	O	LCD segment output terminal (convertible to DC output terminal by mask option)
COM0–3	14–17	O	LCD common output terminal
RESET	49	I	Initial setting input terminal
TEST	31	I	Test input terminal

CHAPTER 2 POWER SUPPLY AND INITIAL RESET

2.1 Power Supply

With a single external power supply (*1) supplied to V_{DD} through V_{SS}, the E0C6S37 Series generate the necessary internal voltages with the regulated voltage circuit (<V_{S1}> for oscillators and internal circuit, <V_{L1} or V_{L2}> for LCDs) and the voltage booster/reducer (<V_{L2}, V_{L3} or V_{L1}, V_{L3}> for LCDs).

The E0C6S37 generates <V_{L2}> with the regulated voltage circuit and <V_{L1}, V_{L3}> with the voltage booster/reducer. The E0C6SL37 and the E0C6SB37 generate <V_{L1}> with the regulated voltage circuit and <V_{L2}, V_{L3}> with the voltage booster. The voltage <V_{S1}> for the internal circuit that is generated by the regulated voltage circuit is -1.2 V (V_{DD} standard).

Figure 2.1.1 shows the power supply configuration of the E0C6S37. Figure 2.1.2 shows the power supply configuration of the E0C6SL37 and the E0C6SB37.

*1 Supply voltage: E0C6S37, E0C6SB37...3 V
E0C6SL37...1.5 V

Note - External loads cannot be driven by the output voltage of the regulated voltage circuit and the voltage booster/reducer.

- See Chapter 6, "ELECTRICAL CHARACTERISTICS", for voltage values.

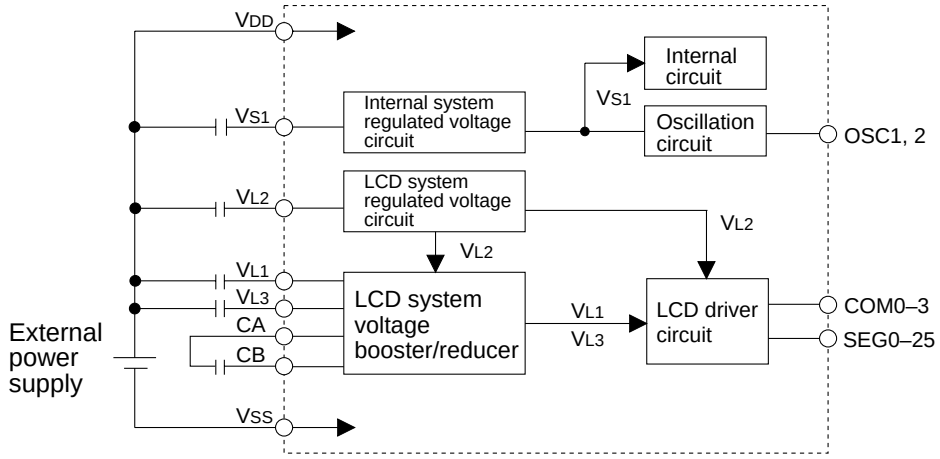


Fig. 2.1.1 Configuration of E0C6S37 power supply system
(when LCD system regulated voltage circuit is used)

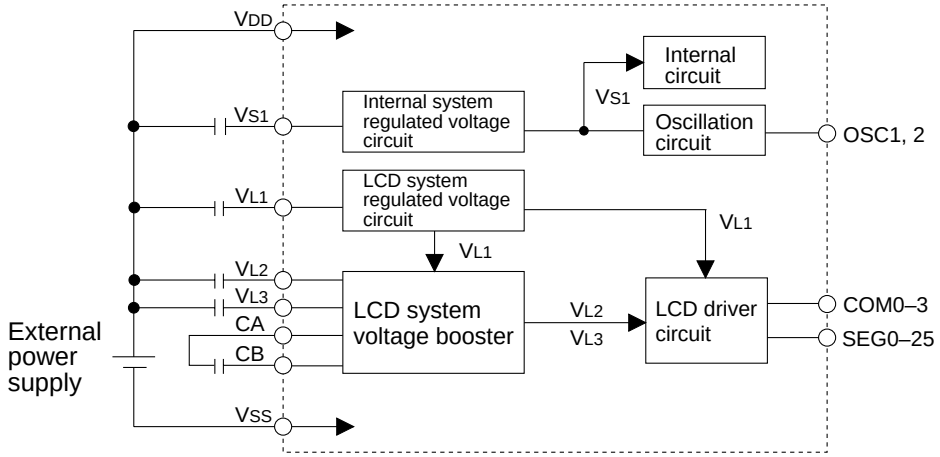


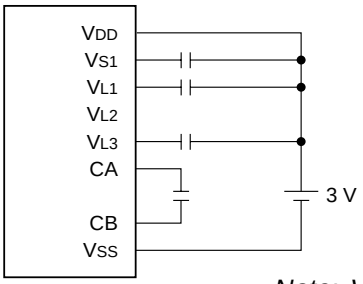
Fig. 2.1.2 Configuration of E0C6SL37/E0C6SB37 power supply system
(when LCD system regulated voltage circuit is used)

The LCD system regulated voltage circuit use can be prohibited by setting the mask option. In this case, external elements can be minimized because the external capacitors for the LCD system regulated voltage circuit are not necessary. However when the LCD system regulated voltage circuit is not used, the display quality of the LCD panel, when the supply voltage fluctuates (drops), is inferior to when the LCD system regulated voltage circuit is used. The E0C6SB37 always uses the the LCD system regulated voltage circuit, therefore the external capacitors are required.
Figure 2.1.3 shows the external elements when the the LCD system regulated voltage circuit is not used.

• **E0C6S37**

4.5 V LCD panel

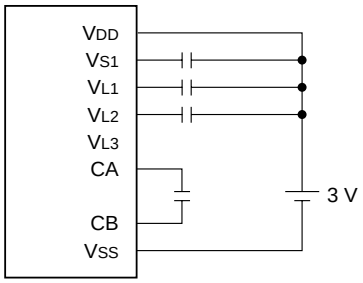
1/4, 1/3, 1/2 duty, 1/3 bias



Note: V_{L2} is shorted to V_{SS} inside the IC.

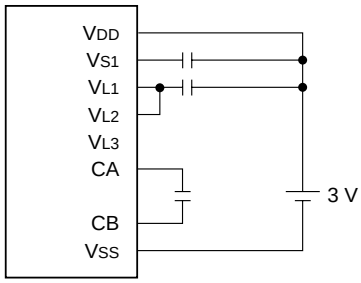
3 V LCD panel

1/4, 1/3, 1/2 duty, 1/3 bias



3 V LCD panel

1/4, 1/3, 1/2 duty, 1/2 bias

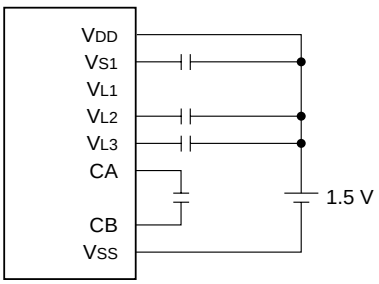


Note: V_{L3} is shorted to V_{SS} inside the IC.

• **E0C6SL37**

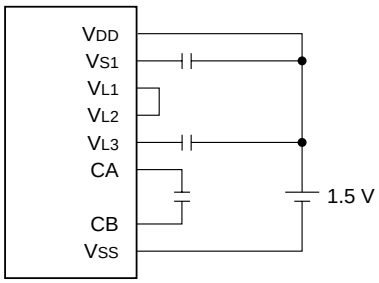
4.5 V LCD panel

1/4, 1/3, 1/2 duty, 1/3 bias



3 V LCD panel

1/4, 1/3, 1/2 duty, 1/2 bias



Note: V_{L1} is shorted to V_{SS} inside the IC.

Fig. 2.1.3 External elements when LCD system regulated voltage circuit is not used

2.2 Initial Reset

To initialize the E0C6S37 Series circuits, an initial reset must be executed. There are three ways of doing this.

(1) Initial reset by the oscillation detection circuit (Note)
(2) External initial reset via the RESET pin
(3) External initial reset by simultaneous high input to pins K00–K03 (depending on mask option)

Figure 2.2.1 shows the configuration of the initial reset circuit.

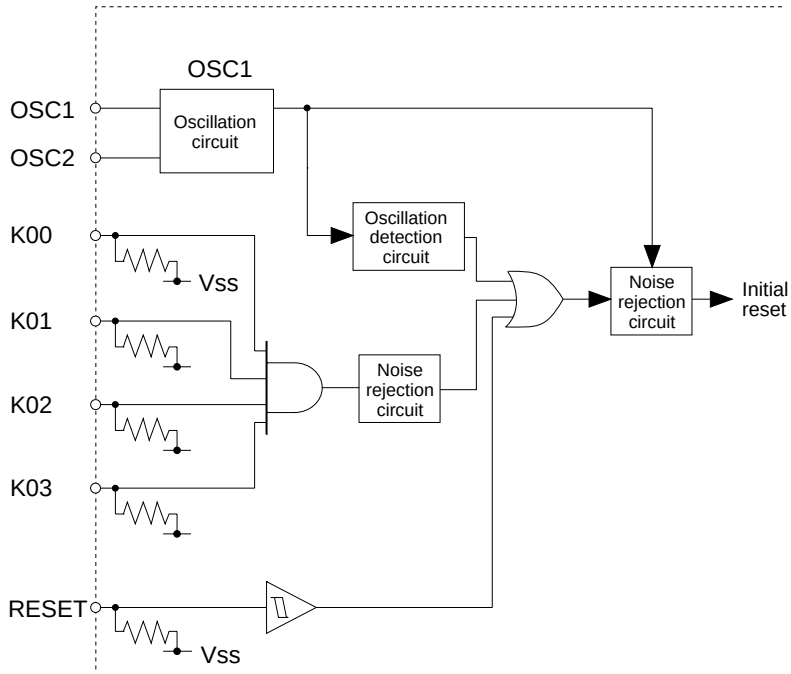


Fig. 2.2.1
Configuration of initial reset circuit

Note *Be sure to use reset function (2) or (3) at power-on because the initial reset function by the oscillation detection circuit (1) may not operate normally depending on the power-on procedure.*

Oscillation detection circuit

The oscillation detection circuit outputs the initial reset signal at power-on until the crystal oscillation circuit starts oscillating, or when the crystal oscillation circuit stops oscillating for some reason.
However, use the following reset functions at power-on because the initial reset function by the oscillation detection circuit may not operate normally depending on the power-on procedure.

Reset pin (RESET)

An initial reset can be invoked externally by making the reset pin high. This high level must be maintained for at least 5 ms (when oscillating frequency, fosc = 32 kHz), because the initial reset circuit contains a noise rejection circuit. When the reset pin goes low the CPU begins to operate.

Simultaneous high input to input ports (K00–K03)

Another way of invoking an initial reset externally is to input a high signal simultaneously to the input ports (K00–K03) selected with the mask option. The specified input port pins must be kept high for at least 4 sec (when oscillating frequency fosc = 32 kHz), because of the noise rejection circuit. Table 2.2.1 shows the combinations of input ports (K00–K03) that can be selected with the mask option.

Table 2.2.1
Input port combinations

A	Not used
B	K00*K01
C	K00*K01*K02
D	K00*K01*K02*K03

When, for instance, mask option D (K00*K01*K02*K03) is selected, an initial reset is executed when the signals input to the four ports K00–K03 are all high at the same time.

If you use this function, make sure that the specified ports do not go high at the same time during normal operation.

Internal register following initialization

An initial reset initializes the CPU as shown in the table below.

Table 2.2.2 Initial values

CPU Core			
Name	Signal	Number of Bits	Setting Value
Program counter step	PCS	8	00H
Program counter page	PCP	4	1H
New page pointer	NPP	4	1H
Stack pointer	SP	8	Undefined
Index register X	X	8	Undefined
Index register Y	Y	8	Undefined
Register pointer	RP	4	Undefined
General register A	A	4	Undefined
General register B	B	4	Undefined
Interrupt flag	I	1	0
Decimal flag	D	1	0
Zero flag	Z	1	Undefined
Carry flag	C	1	Undefined

Peripheral Circuits		
Name	Number of Bits	Setting Value
RAM	80 × 4	Undefined
Display memory	26 × 4	Undefined
Other peripheral circuit	–	*1

*1: See section 4.1, "Memory Map"

2.3 Test Pin (TEST)

This pin is used when IC is inspected for shipment.
During normal operation connect it to VSS.

CHAPTER 3 CPU, ROM, RAM

3.1 CPU

The E0C6S37 Series employs the E0C6200A core CPU, so that register configuration, instructions, and so forth are virtually identical to those in other processors in the family using the E0C6200A. Refer to the "E0C6200A Core CPU Manual" for details of the E0C6200A.

Note the following points with regard to the E0C6S37 Series:

(1) The SLEEP operation is not provided, so the SLP instruction cannot be used.

(2) Because the ROM capacity is 1,024 words, 12 bits per word, bank bits are unnecessary, and PCB and NBP are not used.

(3) The RAM page is set to 0 only, so the page part (XP, YP) of the index register that specifies addresses is invalid.

PUSH	XP	PUSH	YP
POP	XP	POP	YP
LD	XP,r	LD	YP,r
LD	r,XP	LD	r,YP

3.2 ROM

The built-in ROM, a mask ROM for the program, has a capacity of 1,024 × 12-bit steps. The program area is 4 pages (0–3), each consisting of 256 steps (00H–FFH). After an initial reset, the program start address is page 1, step 00H. The interrupt vector is allocated to page l, steps 01H–07H.

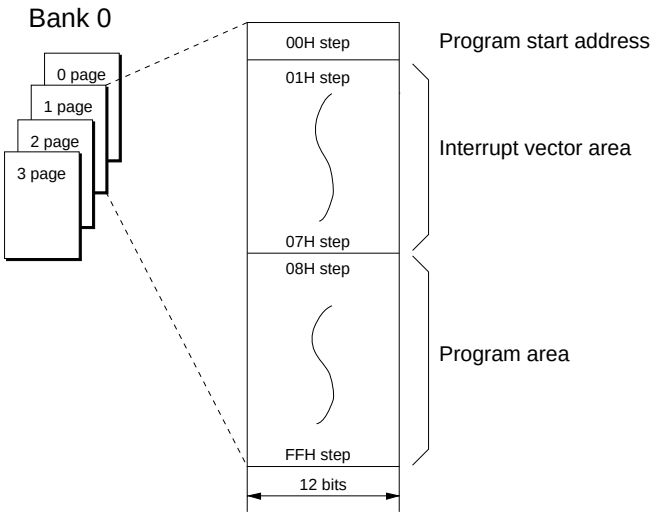


Fig. 3.2.1
ROM configuration

3.3 RAM

The RAM, a data memory for storing a variety of data, has a capacity of 80 words, 4-bit words. When programming, keep the following points in mind:

(1) Part of the data memory is used as stack area when saving subroutine return addresses and registers, so be careful not to overlap the data area and stack area.

(2) Subroutine calls and interrupts take up three words on the stack.

(3) Data memory 000H–00FH is the memory area pointed by the register pointer (RP).

CHAPTER 4 PERIPHERAL CIRCUITS AND OPERATION

Peripheral circuits (timer, I/O, and so on) of the E0C6S37 Series are memory mapped. Thus, all the peripheral circuits can be controlled by using memory operations to access the I/O memory. The following sections describe how the peripheral circuits operate.

4.1 Memory Map

The data memory of the E0C6S37 Series has an address space of 154 words, of which 32 words are allocated to display memory and 26 words, to I/O memory. Figure 4.1.1 show the overall memory map for the E0C6S37 Series, and Tables 4.1.1(a)–(e), the memory maps for the peripheral circuits (I/O space).

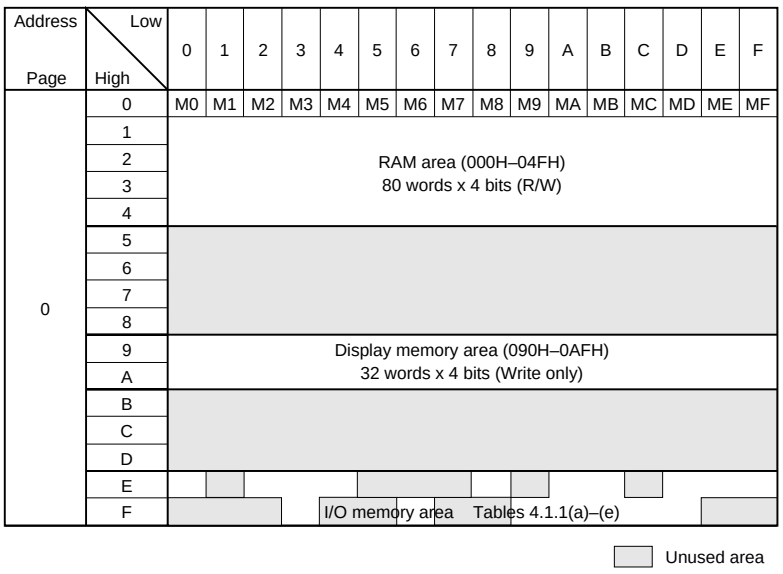


Fig. 4.1.1
Memory map

Note *Memory is not mounted in unused area within the memory map and in memory area not indicated in this chapter. For this reason, normal operation cannot be assured for programs that have been prepared with access to these areas.*

Table 4.1.1(a) I/O memory map

Address	Register D3	D2	D1	D0	Name	SR *1	1	0	Comment
0E0H	K03	K02	K01	K00	K03	– *2	High	Low	Input port (K00–K03)
	R				K02	– *2	High	Low	
					K01	– *2	High	Low	
					K00	– *2	High	Low	
0E2H	SWL3	SWL2	SWL1	SWL0	SWL3	0			MSB
	R				SWL2	0			Stopwatch timer 1/100 sec (BCD)
					SWL1	0			
					SWL0	0			LSB
0E3H	SWH3	SWH2	SWH1	SWH0	SWH3	0			MSB
	R				SWH2	0			Stopwatch timer 1/10 sec (BCD)
					SWH1	0			
					SWH0	0			LSB
0E4H	TM3	TM2	TM1	TM0	TM3	–	High	Low	Timer data (clock timer 2 Hz)
	R				TM2	–	High	Low	Timer data (clock timer 4 Hz)
					TM1	–	High	Low	Timer data (clock timer 8 Hz)
					TM0	–	High	Low	Timer data (clock timer 16 Hz)

* 1 Initial value following initial reset
* 2 Not set in the circuit
* 3 Undefined
* 4 Reset (0) immediately after being read
* 5 Constantly 0 when being read
* 6 Refer to main manual

Table 4.1.1(b) I/O memory map

Address	Register								Comment
	D3	D2	D1	D0	Name	SR *1	1	0	
0E8H	EIK03	EIK02	EIK01	EIK00	EIK03	0	Enable	Mask	Interrupt mask register (K03)
	R/W				EIK02	0	Enable	Mask	Interrupt mask register (K02)
					EIK01	0	Enable	Mask	Interrupt mask register (K01)
					EIK00	0	Enable	Mask	Interrupt mask register (K00)
0EAH	0	0	EISW1	EISW0	0 *5				
	R		R/W		0 *5				
					EISW1	0	Enable	Mask	Interrupt mask register (stopwatch 1 Hz)
					EISW0	0	Enable	Mask	Interrupt mask register (stopwatch 10 Hz)
0EBH	0	EIT2	EIT8	EIT32	0 *5				
	R	R/W			EIT2	0	Enable	Mask	Interrupt mask register (clock timer 2 Hz)
					EIT8	0	Enable	Mask	Interrupt mask register (clock timer 8 Hz)
					EIT32	0	Enable	Mask	Interrupt mask register (clock timer 32 Hz)
0EDH	0	0	0	IK0	0 *5				
	R				0 *5				
					0 *5				
					IK0 *4	0	Yes	No	Interrupt factor flag (K00–K03)

* 1 Initial value following initial reset
* 2 Not set in the circuit
* 3 Undefined
* 4 Reset (0) immediately after being read
* 5 Constantly 0 when being read
* 6 Refer to main manual

Table 4.1.1(c) I/O memory map

Address	Register D3	D2	D1	D0	Name	SR *1	1	0	Comment
0EEH	0	0	ISW1	ISW0	0 *5				
	R				0 *5				
					ISW1 *4	0	Yes	No	Interrupt factor flag (stopwatch 1 Hz)
					ISW0 *4	0	Yes	No	Interrupt factor flag (stopwatch 10 Hz)
0EFH	0	IT2	IT8	IT32	0 *5				
	R				IT2 *4	0	Yes	No	Interrupt factor flag (clock timer 2 Hz)
					IT8 *4	0	Yes	No	Interrupt factor flag (clock timer 8 Hz)
					IT32 *4	0	Yes	No	Interrupt factor flag (clock timer 32 Hz)
0F3H	R03	R02	R01 / BUZZER	R00 / FOUT	R03	0	High	Low	R03 output port data
	R/W				R02	0	High	Low	R02 output port data
					R01	0	High	Low	R01 output port data
					BUZZER	0	ON	OFF	Buzzer ON/OFF control register
					R00	0	High	Low	R00 output port data
					FOUT	0	ON	OFF	Frequency output ON/OFF control register
0F6H	P03	P02	P01	P00	P03	*2	High	Low	I/O port (P00–P03)
	R/W				P02	*2	High	Low	
					P01	*2	High	Low	
					P00	0 *2	High	Low	

* 1 Initial value following initial reset
* 2 Not set in the circuit
* 3 Undefined
* 4 Reset (0) immediately after being read
* 5 Constantly 0 when being read
* 6 Refer to main manual

Table 4.1.1(d) I/O memory map

Address	Register								Comment
	D3	D2	D1	D0	Name	SR *1	1	0	
0F9H	0	TMRST	SWRUN	SWRST	0 *5				
	R	W	R/W	W	TMRST	Reset	Reset	–	Clock timer reset
					SWRUN	0	Run	Stop	Stopwatch timer RUN/STOP
					SWRST *5	Reset	Reset	–	Stopwatch timer reset
0FAH	HLMOD	0	SVDDT	SVDON	HLMOD	0	Heavy load	Normal load	Heavy load protection mode register
	R/W	R		R/W	0 *5				
					SVDDT	0	Supply voltage low	Supply voltage normal	Supply voltage detection data
					SVDON	0	ON	OFF	Supply voltage detection ON/OFF
0FBH	CSDC	0	0	0	CSDC	0	Static	Dynamic	LCD drive switch
	R/W	R			0 *5				
					0 *5				
					0 *5				
0FCH	0	0	0	IOC	0 *5				
	R			R/W	0 *5				
					0 *5				
					IOC	0	Output	Input	I/O port P00–P03 Input/Output

* 1 Initial value following initial reset
* 2 Not set in the circuit
* 3 Undefined
* 4 Reset (0) immediately after being read
* 5 Constantly 0 when being read
* 6 Refer to main manual

Table 4.1.1(e) I/O memory map

Address	Register								Comment
	D3	D2	D1	D0	Name	SR *1	1	0	
0FDH	XBZR	0	XFOUT1	XFOUT0	XBZR	0	2 kHz	4 kHz	Buzzer frequency control
	R/W	R	R/W		0 *5				
					XFOUT1	0	High	Low	FOUT frequency control: XFOUT1(0), XFOUT0(0) -> F1 XFOUT1(0), XFOUT0(1) -> F2 XFOUT1(1), XFOUT0(0) -> F3 XFOUT1(1), XFOUT0(1) -> F4
					XFOUT0	0	High	Low	

* 1 Initial value following initial reset
* 2 Not set in the circuit
* 3 Undefined
* 4 Reset (0) immediately after being read
* 5 Constantly 0 when being read
* 6 Refer to main manual

4.2 Oscillation Circuit

Crystal oscillation circuit

The E0C6S37 Series have a built-in crystal oscillation circuit. This circuit generates the operating clock for the CPU and peripheral circuit on connection to an external crystal oscillator (typ. 32.768 kHz) and trimmer capacitor (5–25 pF).
Figure 4.2.1 is the block diagram of the crystal oscillation circuit.

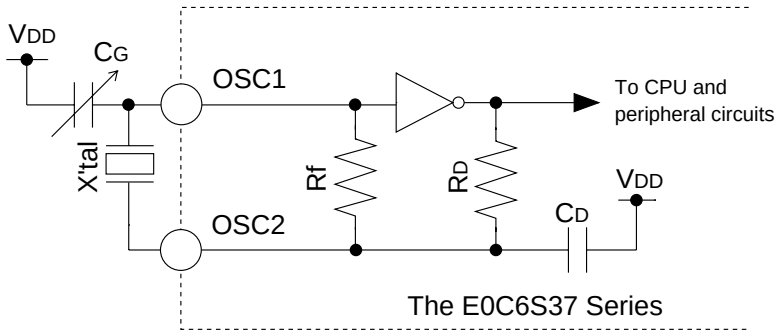


Fig. 4.2.1
Crystal oscillation circuit

As Figure 4.2.1 indicates, the crystal oscillation circuit can be configured simply by connecting the crystal oscillator (X'tal) between the OSC1 and OSC2 pins and the trimmer capacitor (C_G) between the OSC1 and V_{DD} pins.

Note *The OSC1 and OSC2 terminals on the board should be shielded with the V_{DD} (+ side).*

CR oscillation circuit

For the E0C6S37 Series, CR oscillation circuit (typ. 65 kHz) may also be selected by a mask option. Figure 4.2.2 is the block diagram of the CR oscillation circuit.

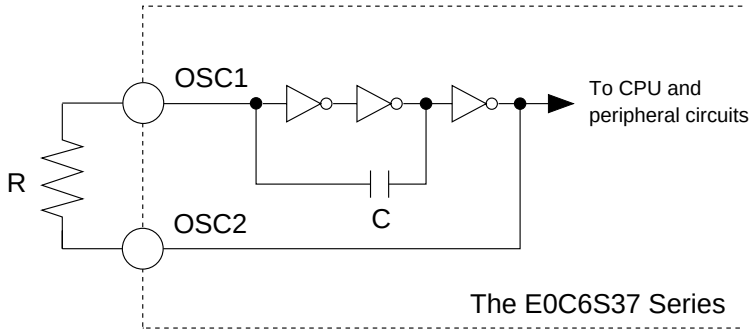


Fig. 4.2.2
CR oscillation circuit

As Figure 4.2.2 indicates, the CR oscillation circuit can be configured simply by connecting the register (R) between pins OSC1 and OSC2 since capacity (C) is built-in.
See Chapter 6, "ELECTRICAL CHARACTERISTICS" for R value.

4.3 Input Port (K00–K03)

Configuration of input port

The E0C6S37 Series have a 4-bit general-purpose input port. Each of the input port pins (K00–K03) has an internal pull-down resistance. The pull-down resistance can be selected for each bit with the mask option.
Figure 4.3.1 shows the configuration of input port.

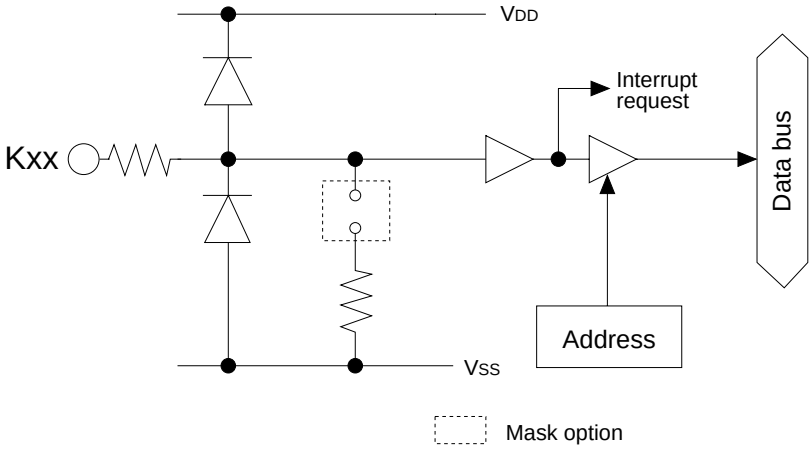


Fig. 4.3.1
Configuration of input port

Selecting "pull-down resistance enabled" with the mask option allows input from a push button, key matrix, and so forth. When "pull-down resistance disabled" is selected, the port can be used for slide switch input and interfacing with other LSIs.

Interrupt function

All four input port bits (K00–K03) provide the interrupt function. The conditions for issuing an interrupt can be set by the software for the four bits. Also, whether to mask the interrupt function can be selected individually for all four bits by the software. Figure 4.3.2 shows the configuration of K00–K03.

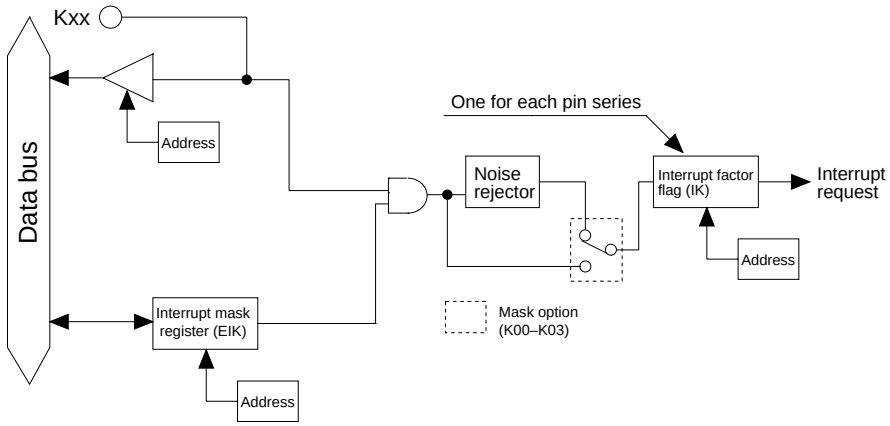
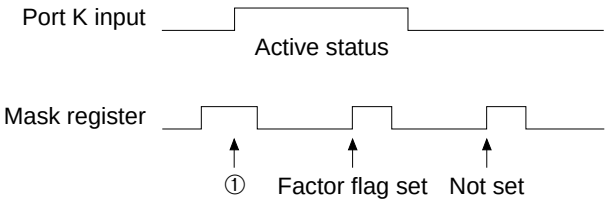


Fig. 4.3.2
Input interrupt circuit configuration (K00–K03)

The interrupt mask registers (EIK00–EIK03) enable the interrupt mask to be selected individually for K00–K03. An interrupt occurs when the input value which are not masked change and the interrupt factor flag (IK0) is set to 1.

Input interrupt programing related precautions



When the content of the mask register is rewritten, while the port K input is in the active status. The input interrupt factor flag is set at ①.

Fig. 4.3.3
Input interrupt timing

When using an input interrupt, if you rewrite the content of the mask register, when the value of the input terminal which becomes the interrupt input is in the active status (input terminal = high status), the factor flag for input interrupt may be set.
For example, a factor flag is set with the timing of ① shown in Figure 4.3.3. However, when clearing the content of the mask register with the input terminal kept in the high status and then setting it, the factor flag of the input interrupt is again set at the timing that has been set.

Consequently, when the input terminal is in the active status (high status), do not rewrite the mask register (clearing, then setting the mask register), so that a factor flag will only set at the rising edge in this case. When clearing, then setting the mask register, set the mask register, when the input terminal is not in the active status (low status).

Mask option

The contents that can be selected with the input port mask option are as follows:

(1) An internal pull-down resistance can be selected for each of the four bits of the input ports (K00–K03). Having selected "pull-down resistance disabled", take care that the input does not float. Select "pull-down resistance enabled" for input ports that are not being used.

(2) The input interrupt circuit contains a noise rejection circuit to prevent interrupts form occurring through noise. The mask option enables selection of the noise rejection circuit for each separate pin series. When "use" is selected, a maximum delay of 0.5 ms (fosc = 32 kHz) occurs from the time an interrupt condition is established until the interrupt factor flag (IK) is set to 1.

Control of input port

Table 4.3.1 list the input port control bits and their addresses.

Table 4.3.1 Input port control bits

Address	Register D3	D2	D1	D0	Name	SR	1	0	Comment
0E0H	K03	K02	K01	K00	K03	–	High	Low	Input port (K00–K03)
	R				K02	–	High	Low	
					K01	–	High	Low	
					K00	–	High	Low	
0E8H	EIK03	EIK02	EIK01	EIK00	EIK03	0	Enable	Mask	Interrupt mask register (K03)
	R/W				EIK02	0	Enable	Mask	Interrupt mask register (K02)
					EIK01	0	Enable	Mask	Interrupt mask register (K01)
					EIK00	0	Enable	Mask	Interrupt mask register (K00)
0EDH	0	0	0	IK0	0				
	R				0				
					0				
					IK0	0	Yes	No	Interrupt factor flag (K00–K03)

K00–K03 Input port data (0E0H)

The input data of the input port pins can be read with these registers.

When 1 is read: High level
When 0 is read: Low level
Writing: Invalid

The value read is 1 when the pin voltage of the four bits of the input port (K00–K03) goes high (V_{DD}), and 0 when the voltage goes low (V_{SS}). These bits are reading, so writing cannot be done.

EIK00–EIK03 Interrupt mask registers (0E8H)

Masking the interrupt of the input port pins can be done with these registers.

When 1 is written: Enable
When 0 is written: Mask
Reading: Valid

With these registers, masking of the input port bits can be done for each of the four bits. After an initial reset, these registers are all set to 0.

IK0 Interrupt factor flag (0EDH)

This flag indicates the occurrence of an input interrupt.

When 1 is read: Interrupt has occurred
When 0 is read: Interrupt has not occurred
Writing: Invalid

The interrupt factor flag IK0 is associated with K00–K03. From the status of this flag, the software can decide whether an input interrupt has occurred.
This flag is reset when the software has read it.
Reading of interrupt factor flag is available at EI, but be careful in the following cases.
If the interrupt mask register value corresponding to the interrupt factor flag to be read is set to 1, an interrupt request will be generated by the interrupt factor flag set timing, or an interrupt request will not be generated.
After an initial reset, this flag is set to 0.

4.4 Output Port (R00–R03)

Configuration of output port

The E0C6S37 Series have a 4-bit general output port (R00–R03).
Output specification of the output port can be selected in a bit unit with the mask option. Two kinds of output specifications are available: complementary output and Pch open drain output. Also, the mask option enables the output ports R00 and R01 to be used as special output ports.
Figure 4.4.1 shows the configuration of the output port.

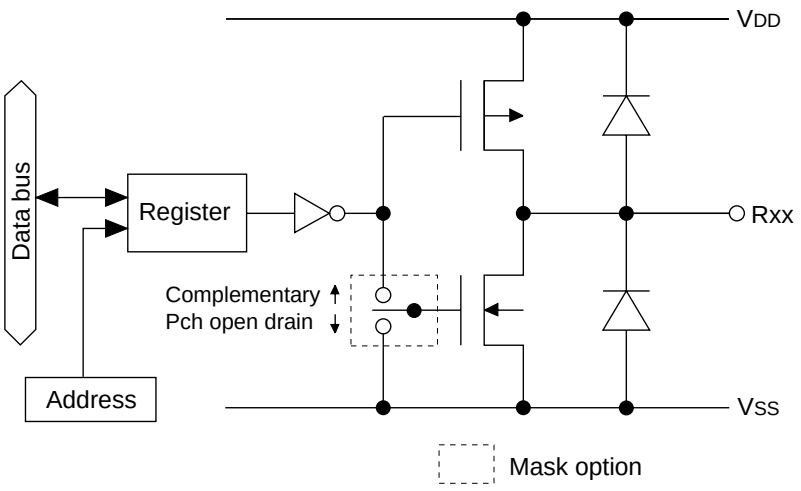


Fig. 4.4.1
Configuration of output port

Mask option

The mask option enables the following output port selection.

(1) Output specification of output port

The output specifications for the output port (R00–R03) may be either complementary output or Pch open drain output for each of the four bits. However, even when Pch open drain output is selected, a voltage exceeding the source voltage must not be applied to the output port.

(2) Special output

In addition to the regular DC output, special output can be selected for output ports R00 and R01, as shown in Table 4.4.1. Figure 4.4.2 shows the structure of output ports R00–R03.

Table 4.4.1
Special output

Pin Name	When Special Output is Selected
R00	FOUT or $\overline{\text{BUZZER}}$
R01	BUZZER

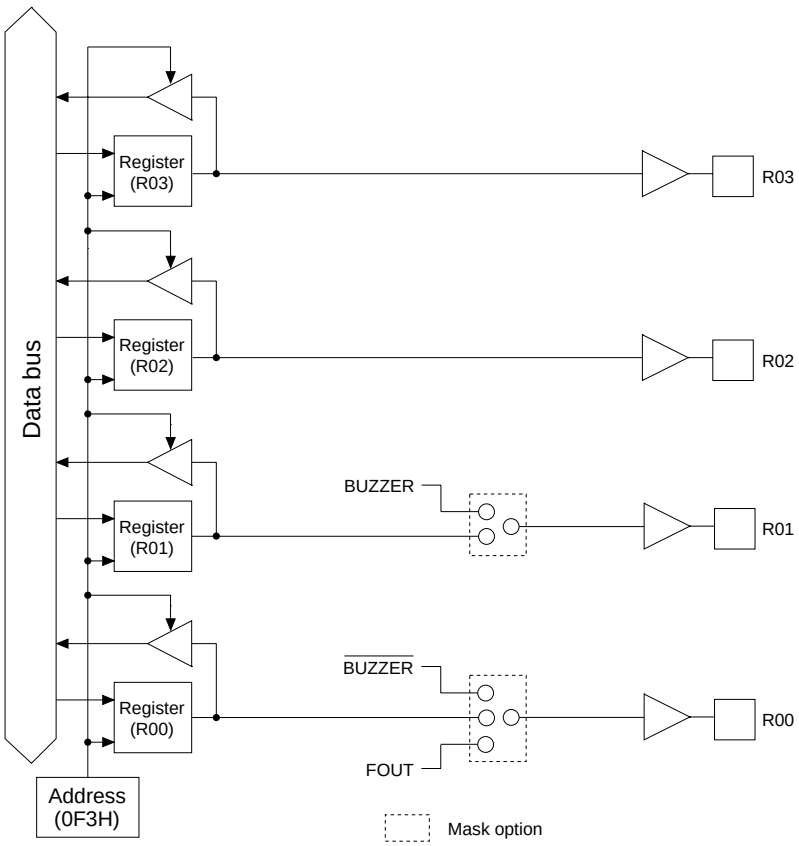


Fig. 4.4.2
Structure of output ports R00–R03

FOUT (R00) When output port R00 is set for FOUT output, this port will generate fosc (CPU operating clock frequency) or clock frequency divided into fosc. Clock frequency may be selected individually for F1–F4, from among 5 types by mask option; one among F1–F4 is selected by software and used. The types of frequency which may be selected are shown in Table 4.4.2.

Table 4.4.2
FOUT clock frequency

Mask Option Sets	Clock Frequency (Hz) fosc = 32.768 kHz			
	F1	F2	F3	F4
	(D1,D0)=(0,0)	(D1,D0)=(0,1)	(D1,D0)=(1,0)	(D1,D0)=(1,1)
Set 1	256 (fosc/128)	512 (fosc/64)	1,024 (fosc/32)	2,048 (fosc/16)
Set 2	512 (fosc/64)	1,024 (fosc/32)	2,048 (fosc/16)	4,096 (fosc/8)
Set 3	1,024 (fosc/32)	2,048 (fosc/16)	4,096 (fosc/8)	8,192 (fosc/4)
Set 4	2,048 (fosc/16)	4,096 (fosc/8)	8,192 (fosc/4)	16,384 (fosc/2)
Set 5	4,096 (fosc/8)	8,192 (fosc/4)	16,384 (fosc/2)	32,768 (fosc/1)

(D1, D0) = (XFOUT1, XFOUT0)

Note *A hazard may occur when the FOUT signal is turned on or off.*

BUZZER, $\overline{\text{BUZZER}}$ (R01, R00) Output ports R01 and R00 may be set to BUZZER output and $\overline{\text{BUZZER}}$ output (BUZZER reverse output), respectively, allowing for direct driving of the piezo-electric buzzer. $\overline{\text{BUZZER}}$ output (R00) may only be set if R01 is set to BUZZER output. In such case, whether ON/OFF of the $\overline{\text{BUZZER}}$ output is done through R00 register or is controlled through R01 simultaneously with BUZZER output is also selected by mask option.
The frequency of buzzer output may be selected by software to be either 2 kHz or 4 kHz.

Control of output port

Table 4.4.3 lists the output port control bits and their addresses.

Table 4.4.3 Control bits of output port

Address	Register D3	D2	D1	D0	Name	SR	1	0	Comment
0F3H	R03	R02	R01 / BUZZER	R00 / FOUT	R03	0	High	Low	R03 output port data
	R/W				R02	0	High	Low	R02 output port data
					R01	0	High	Low	R01 output port data
					BUZZER	0	ON	OFF	Buzzer ON/OFF control register
					R00	0	High	Low	R00 output port data
					FOUT	0	ON	OFF	Frequency output ON/OFF control register
0FDH	XBZR	0	XFOUT1	XFOUT0	XBZR	0	2 kHz	4 kHz	Buzzer frequency control
	R/W	R	R/W		0				
					XFOUT1	0	High	Low	FOUT frequency control: XFOUT1(0), XFOUT0(0) -> F1 XFOUT1(0), XFOUT0(1) -> F2 XFOUT1(1), XFOUT0(0) -> F3 XFOUT1(1), XFOUT0(1) -> F4
					XFOUT0	0	High	Low	

R00–R03 Output port data (0F3H)

Sets the output data for the output ports.

When 1 is written: High output
When 0 is written: Low output
Reading: Valid

The output port pins output the data written to the corresponding registers (R00–R03) without changing it. When 1 is written to the register, the output port pin goes high (V_{DD}), and when 0 is written, the output port pin goes low (V_{SS}). After an initial reset, all the registers are set to 0.

R00 (when FOUT is selected)

Special output port data (0F3H D0)
Controls the FOUT (clock) output.

When 1 is written:	Clock output
When 0 is written:	Low level (DC) output
Reading:	Valid

FOUT output can be controlled by writing data to R00. After an initial reset, this register is set to 0.

Figure 4.4.3 shows the output waveform for FOUT output.

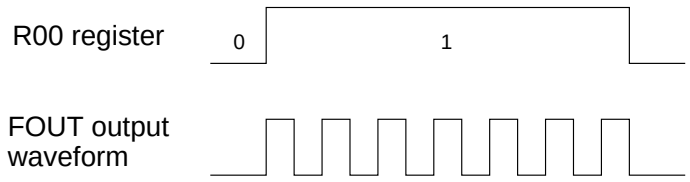


Fig. 4.4.3
FOUT output waveform

XFOUT0, XFOUT1

FOUT frequency control (0FDH D0, 0FDH D1)
Selects the output frequency when R00 port is set for FOUT output.

Table 4.4.4
FOUT frequency selection

XFOUT1	XFOUT0	Frequency Selection
0	0	F1
0	1	F2
1	0	F3
1	1	F4

After an initial reset, these registers are set to 0.

R00, R01 (when $\overline{\text{BUZZER}}$ and BUZZER is selected)

Special output port data (0F3H D0, 0F3H D1)
Controls the buzzer output.

When 1 is written:	Buzzer output
When 0 is written:	Low level (DC) output
Reading:	Valid

$\overline{\text{BUZZER}}$ and BUZZER output can be controlled by writing data to R00 and R01.
When $\overline{\text{BUZZER}}$ output by R01 register control is selected by mask option, BUZZER output and $\overline{\text{BUZZER}}$ output can be controlled simultaneously by writing data to R01 register.
After an initial reset, these registers are set to 0.

Figure 4.4.4 shows the output waveform for buzzer output.

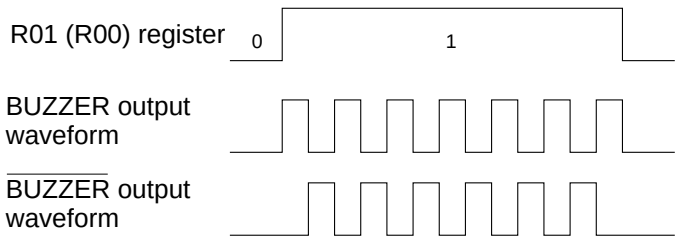


Fig. 4.4.4
Buzzer output waveform

XBZR

Buzzer frequency control (0FDH D3)
Selects the frequency of the buzzer signal.

When 1 is written:	2 kHz
When 0 is written:	4 kHz
Reading:	Valid

When R00 and R01 port is set to buzzer output, the frequency of the buzzer signal can be selected by this register.
When 1 is written to this register, the frequency is set in 2 kHz, and in 4 kHz when 0 is written.
After an initial reset, this register is set to 0.

4.5 I/O Port (P00–P03)

Configuration of I/O port

The E0C6S37 Series have a 4-bit general-purpose I/O port. Figure 4.5.1 shows the configuration of the I/O port. The four bits of the I/O port P00–P03 can be set to either input mode or output mode. The mode can be set by writing data to the I/O control register (IOC).

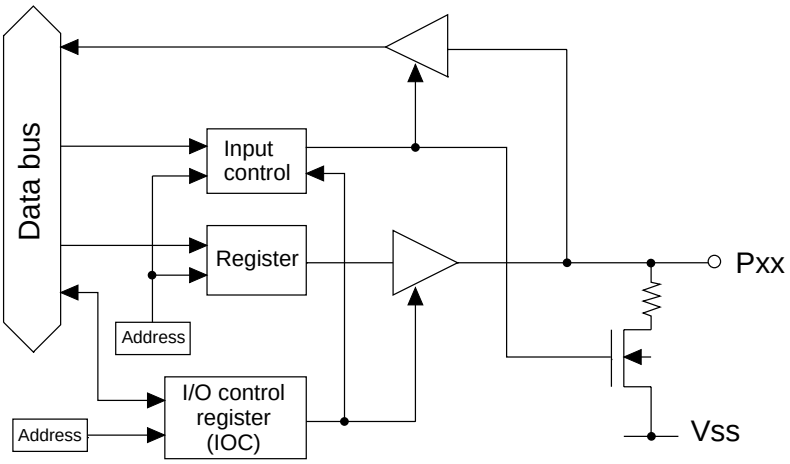


Fig. 4.5.1
Configuration of I/O port

I/O control register and I/O mode

Input or output mode can be set for the four bits of I/O port P00–P03 by writing data into I/O control register IOC.
To set the input mode, 0 is written to the I/O control register. When an I/O port is set to input mode, its impedance becomes high and it works as an input port. However, the input line is pulled down when input data is read.

The output mode is set when 1 is written to the I/O control register (IOC). When an I/O port set to output mode works as an output port, it outputs a high signal (V_{DD}) when the port output data is 1, and a low signal (V_{SS}) when the port output data is 0.
After an initial reset, the I/O control register is set to 0, and the I/O port enters the input mode.

Mask option

The output specification during output mode (IOC = 1) of the I/O port can be set with the mask option for either complementary output or Pch open drain output. This setting can be performed for each bit of the I/O port. However, when Pch open drain output has been selected, voltage in excess of the supply voltage must not be applied to the port.

Control of I/O port

Table 4.5.1 lists the I/O port control bits and their addresses.

Table 4.5.1 I/O port control bits

Address	Register D3	D2	D1	D0	Name	SR	1	0	Comment
0F6H	P03	P02	P01	P00	P03	–	High	Low	I/O port (P00–P03)
	R/W				P02	–	High	Low	
					P01	–	High	Low	
					P00	–	High	Low	
0FCH	0	0	0	IOC	0				
	R			R/W	0				
					0				
					IOC	0	Output	Input	I/O port P00–P03 Input/Output

P00–P03 I/O port data (0F6H)

I/O port data can be read and output data can be written through the port.

• When writing data

When 1 is written: High level
When 0 is written: Low level

When an I/O port is set to the output mode, the written data is output from the I/O port pin unchanged. When 1 is written as the port data, the port pin goes high (V_{DD}), and when 0 is written, the level goes low (V_{SS}). Port data can also be written in the input mode.

• When reading data

When 1 is read: High level
When 0 is read: Low level

The pin voltage level of the I/O port is read. When the I/O port is in the input mode the voltage level being input to the port pin can be read; in the output mode the output voltage level can be read. When the pin voltage is high (V_{DD}) the port data read is 1, and when the pin voltage is low (V_{SS}) the data is 0. Also, the built-in pull-down resistance functions during reading, so the I/O port pin is pulled down.

Note - *When the I/O port is set to the output mode and a low-impedance load is connected to the port pin, the data written to the register may differ from the data read.*

- *When the I/O port is set to the input mode and a low-level voltage (Vss) is input by the built-in pull-down resistance, an erroneous input results if the time constant of the capacitive load of the input line and the built- in pull-down resistance load is greater than the read-out time. When the input data is being read, the time that the input line is pulled down is equivalent to 0.5 cycles of the CPU system clock. Hence, the electric potential of the pins must settle within 0.5 cycles. If this condition cannot be met, some measure must be devised, such as arranging a pull-down resistance externally, or performing multiple read-outs.*

IOC I/O control register (0FCH D0)

The input or output I/O port mode can be set with this register.

When 1 is written:	Output mode
When 0 is written:	Input mode
Reading:	Valid

The input or output mode of the I/O port is set in units of four bits. For instance, IOC sets the mode for P00–P03. Writing 1 to the I/O control register makes the I/O port enter the output mode, and writing 0, the input mode. After an initial reset, the IOC register is set to 0, so the I/O port is in the input mode.

4.6 LCD Driver (COM0–COM3, SEG0–SEG25)

Configuration of LCD driver

The E0C6S37 Series have four common pins and 26 (SEG0–SEG25) segment pins, so that an LCD with a maximum of 104 (26 × 4) segments can be driven. The power for driving the LCD is generated by the CPU internal circuit, so there is no need to supply power externally.
The driving method is 1/4 duty (or 1/3, 1/2 duty by mask option) dynamic drive, adopting the four types of potential (1/3 bias), V_{DD}, V_{L1}, V_{L2} and V_{L3}. Moreover, the 1/2 bias dynamic drive that uses three types of potential, V_{DD}, V_{L1} = V_{L2} and V_{L3}, can be selected by setting the mask option (drive duty can also be selected from 1/4, 1/3 or 1/2). 1/2 bias drive is effective when the LCD system regulated voltage circuit is not used. The V_{L1} terminal and the V_{L2} terminal should be connected outside of the IC.
The frame frequency is 32 Hz for 1/4 duty and 1/2 duty, and 42.7 Hz for 1/3 duty (in the case of fosc = 32.768 kHz).
Figure 4.6.1 shows the drive waveform for 1/4 duty (1/3 bias), Figure 4.6.2 shows the drive waveform for 1/3 duty (1/3 bias), Figure 4.6.3 shows the drive waveform for 1/2 duty (1/3 bias), Figure 4.6.4 shows the drive waveform for 1/4 duty (1/2 bias), Figure 4.6.5 shows the drive waveform for 1/3 duty (1/2 bias) and Figure 4.6.6 shows the drive waveform for 1/2 duty (1/2 bias).

Note *fosc indicates the oscillation frequency of the oscillation circuit.*

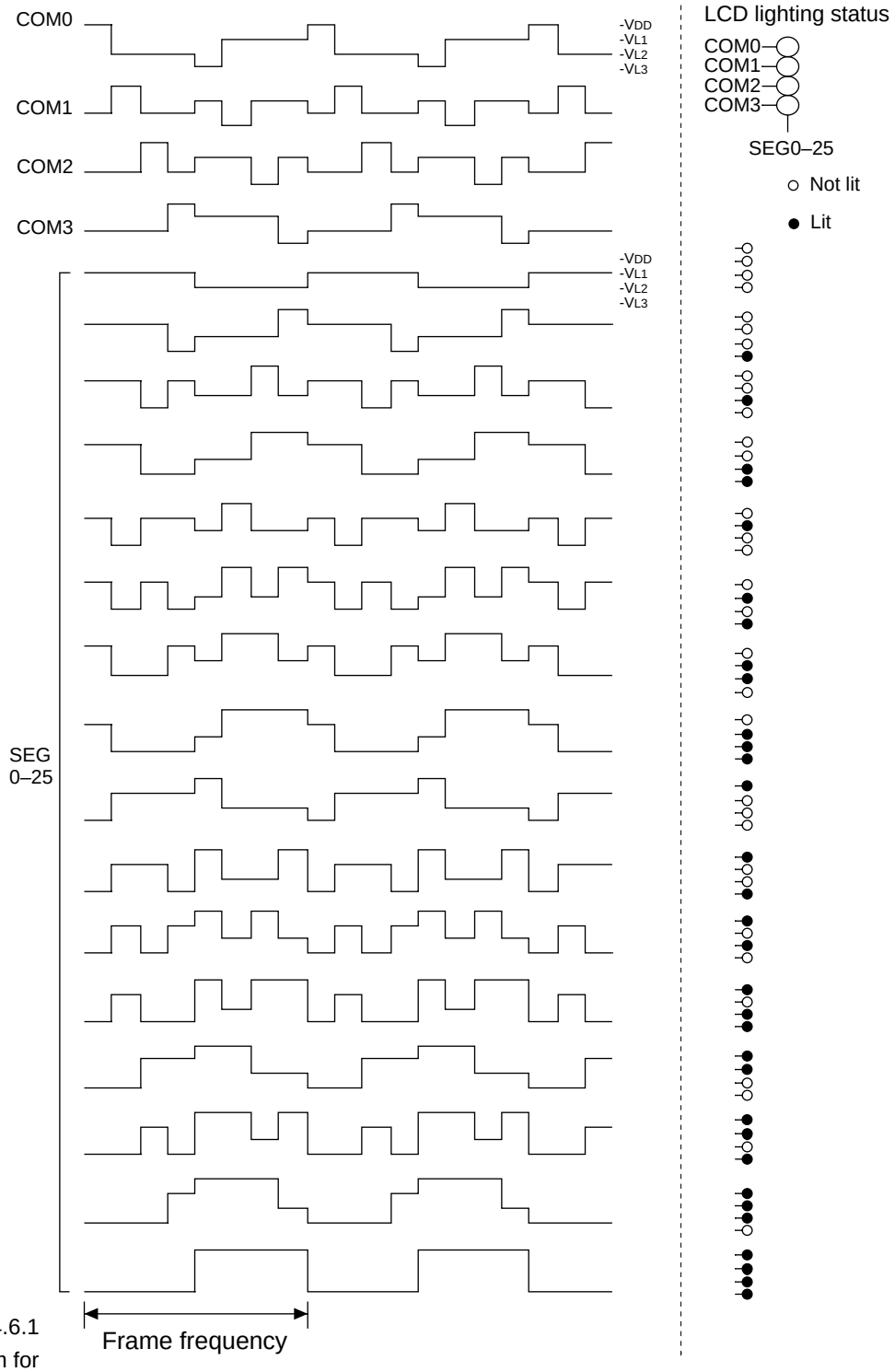


Fig. 4.6.1
Drive waveform for
1/4 duty (1/3 bias)

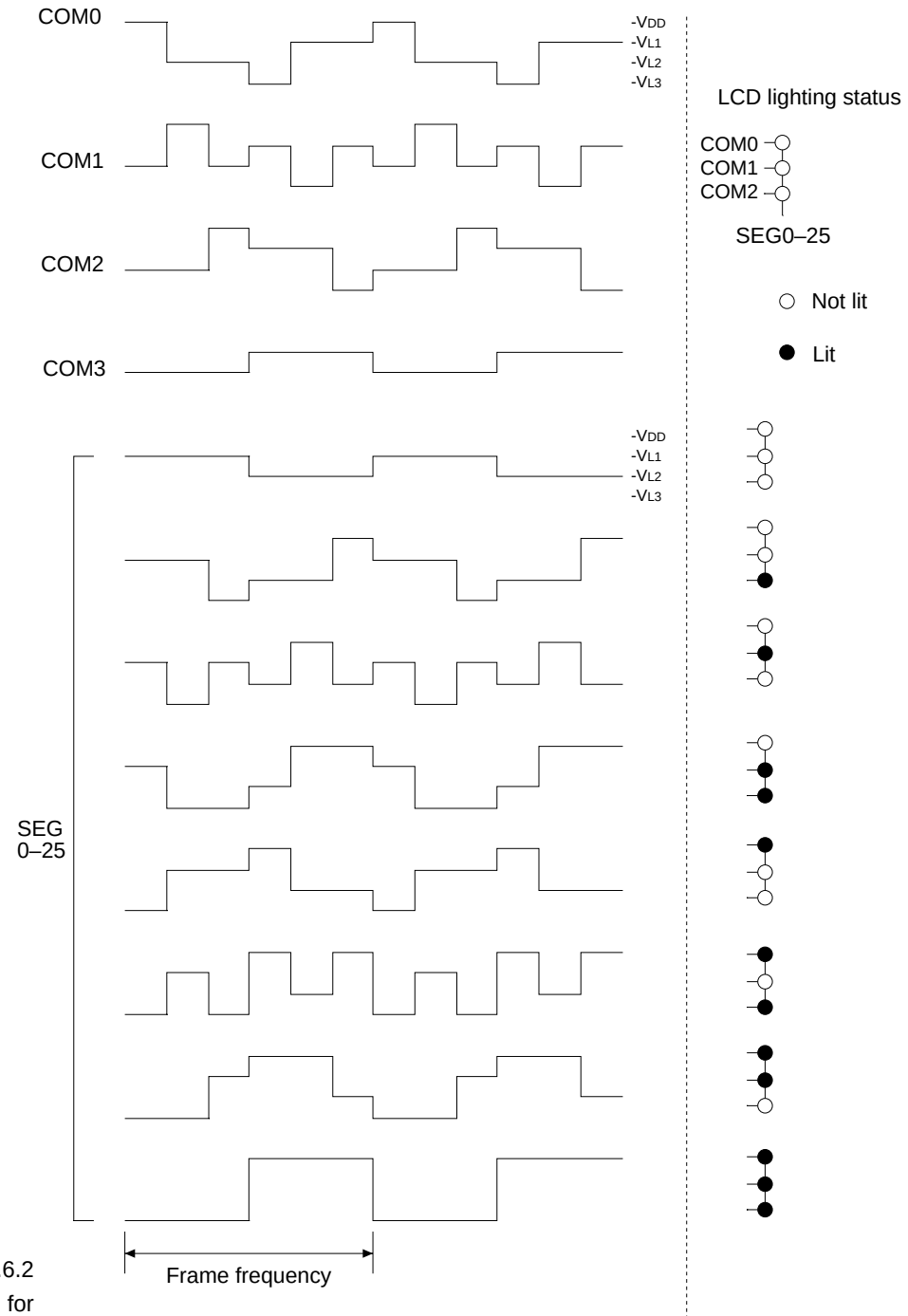


Fig. 4.6.2
Drive waveform for
1/3 duty (1/3 bias)

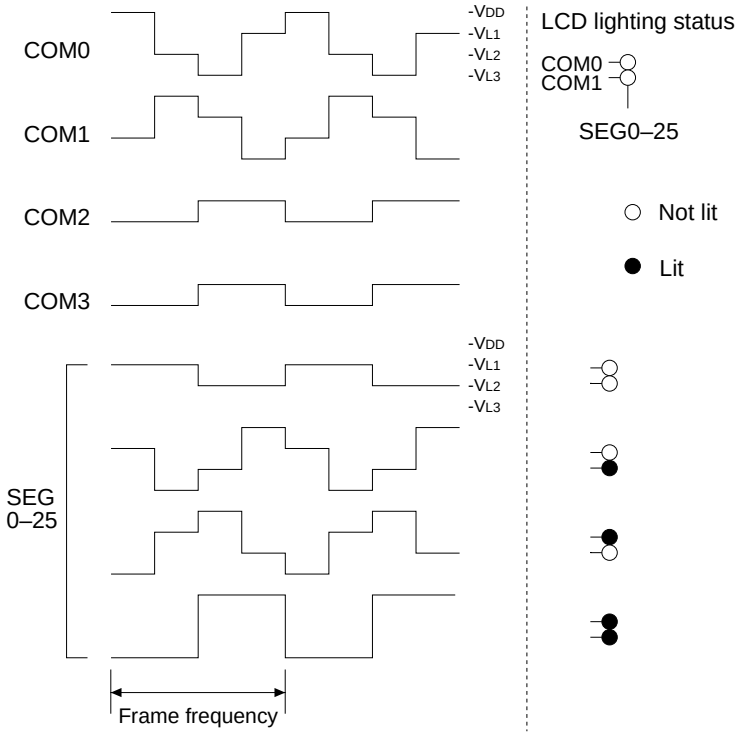


Fig. 4.6.3
Drive waveform for
1/2 duty (1/3 bias)

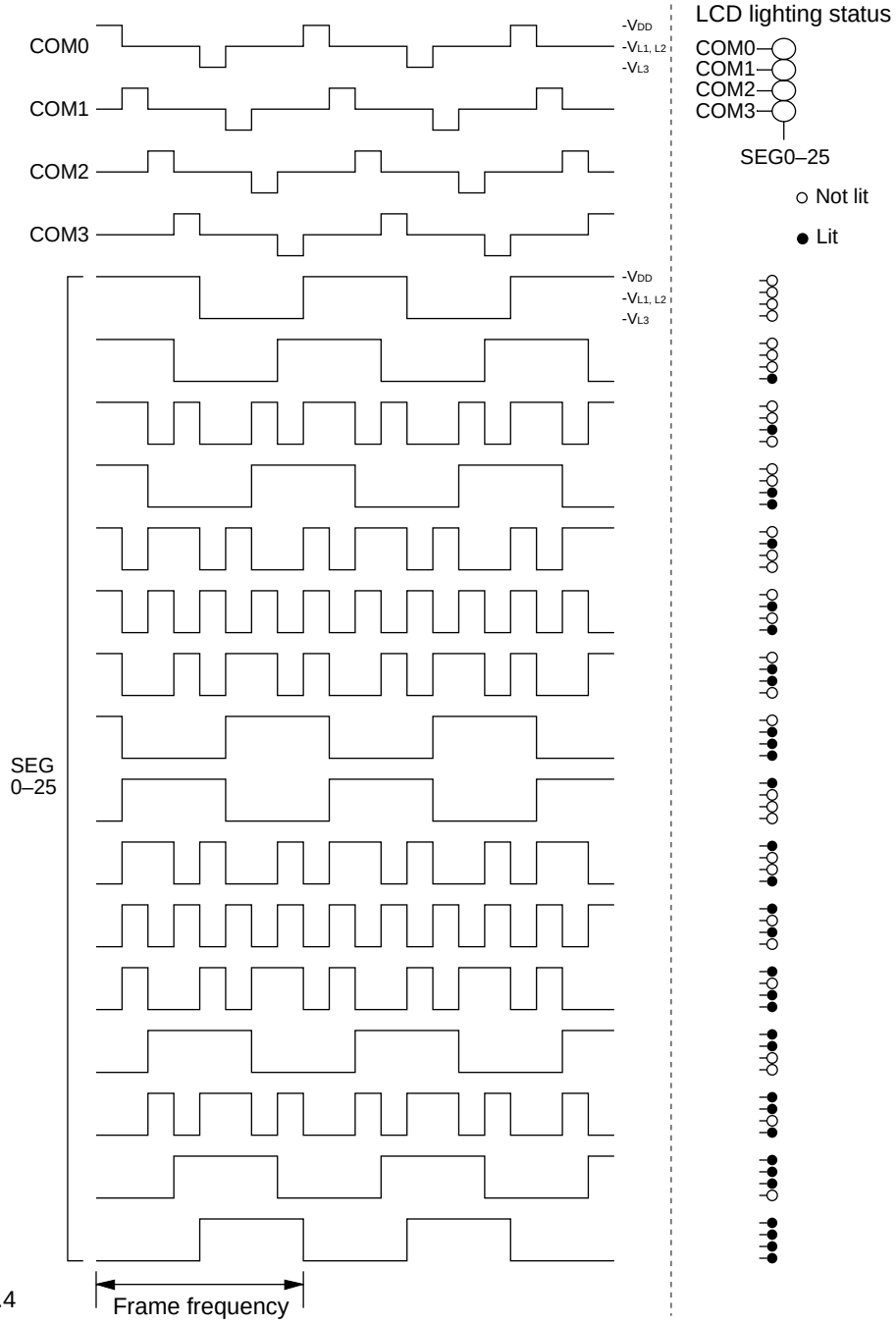


Fig. 4.6.4
Drive waveform for
1/4 duty (1/2 bias)

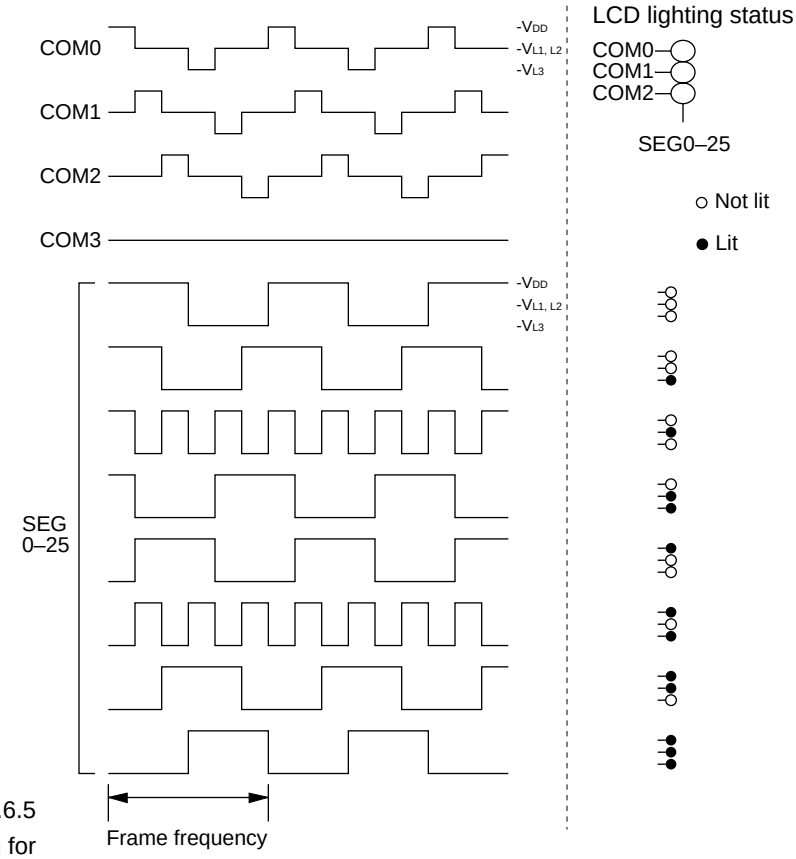


Fig. 4.6.5
Drive waveform for
1/3 duty (1/2 bias)

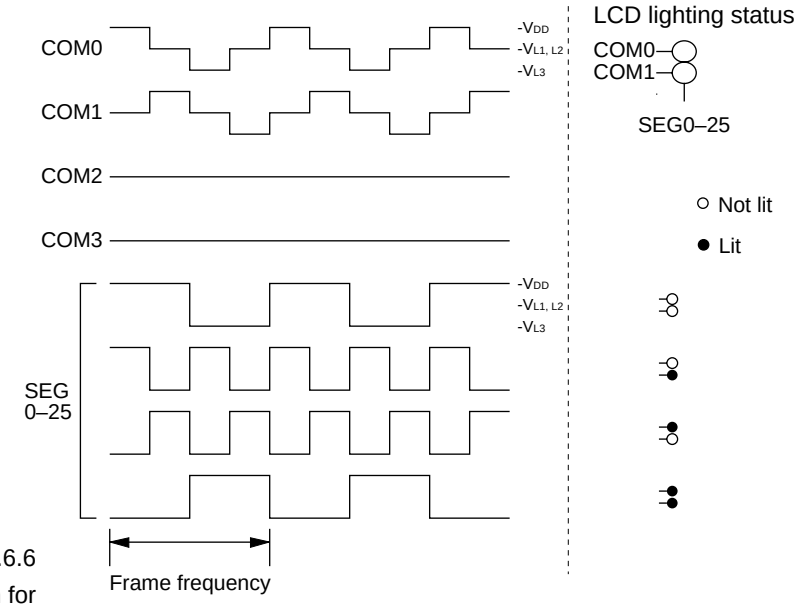


Fig. 4.6.6
Drive waveform for
1/2 duty (1/2 bias)

Cadence adjustment of oscillation frequency

In the E0C6S37 Series, the LCD drive duty can be set to 1/1 duty by software. This function enables easy adjustment (cadence adjustment) of the oscillation frequency of the OSC circuit.

The procedure to set to 1/1 duty drive is as follows:

① Write 1 to the CSDC register at address 0FBH D3.

② Write the same value to all registers corresponding to COMs 0 through 3 of the display memory.

The frame frequency is 32 Hz (f_{OSC1}/1,024, when f_{OSC1} = 32.768 kHz).

Note
- *Even when l/3 or 1/2 duty is selected by the mask option, the display data corresponding to all COM are valid during 1/1 duty driving. Hence, for 1/1 duty drive, set the same value for all display memory corresponding to COMs 0 through 3.*
- *For cadence adjustment, set the display data corresponding to COMs 0 through 3, so that all the LCD segments go on.*

Figure 4.6.7 shows the 1/1 duty drive waveform (1/3 bias).
Figure 4.6.8 shows the 1/1 duty drive waveform (1/2 bias).

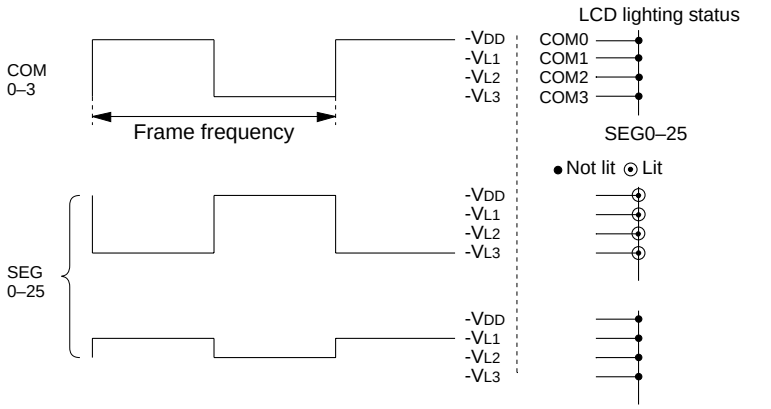


Fig. 4.6.7
1/1 duty drive waveform
(1/3 bias)

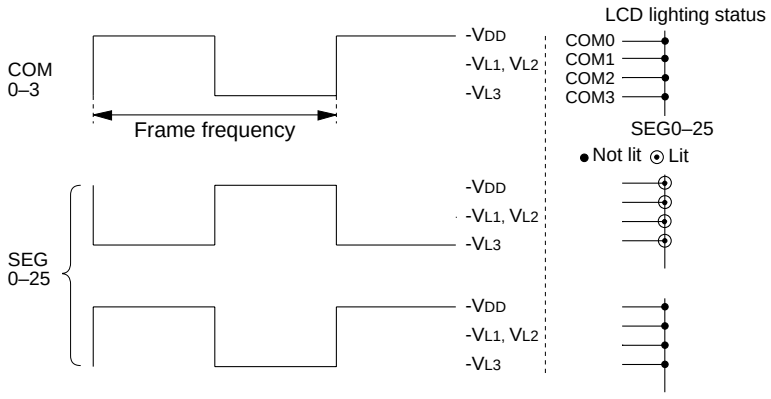


Fig. 4.6.8
1/1 duty drive waveform
(1/2 bias)

Mask option (segment allocation)

(1) Segment allocation

As shown in Figure 4.l.1, the E0C6S37 Series display data is decided by the display data written to the display memory (write-only) at address 090H–0AFH.

The address and bits of the display memory can be made to correspond to the segment pins (SEG0–SEG25) in any combination through mask option. This simplifies design by increasing the degree of freedom with which the liquid crystal panel can be designed.

Figure 4.6.9 shows an example of the relationship between the LCD segments (on the panel) and the display memory in the case of 1/3 duty.

Address	Data			
	D3	D2	D1	D0
09AH	d	c	b	a
09BH	p	g	f	e
09CH	d'	c'	b'	a'
09DH	p'	g'	f'	e'

Display data memory allocation

	Common 0	Common 1	Common 2
SEG10	9A, D0 (a)	9B, D1 (f)	9B, D0 (e)
SEG11	9A, D1 (b)	9B, D2 (g)	9A, D3 (d)
SEG12	9D, D1 (f')	9A, D2 (c)	9B, D3 (p)

Pin address allocation

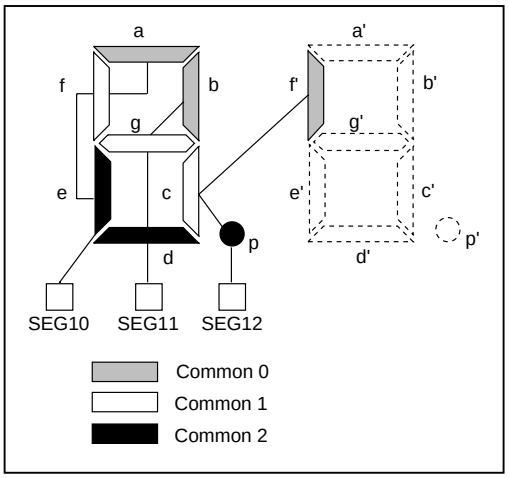


Fig. 4.6.9
Segment allocation

(2) Drive duty

According to the mask option, either 1/4, 1/3 or 1/2 duty can be selected as the LCD drive duty.
Table 4.6.1 shows the differences in the number of segments according to the selected duty.

Table 4.6.1 Differences according to selected duty

Duty	Pins Used in Common	Maximum Number of Segments	Frame Frequency (when fosc = 32 kHz)
1/4	COM0–3	104 (26 × 4)	32 Hz
1/3	COM0–2	78 (26 × 3)	42.7 Hz
1/2	COM0–1	52 (26 × 2)	32 Hz

(3) Output specification

① The segment pins (SEG0–SEG25) are selected by mask option in pairs for either segment signal output or DC output (V_{DD} and V_{SS} binary output). When DC output is selected, the data corresponding to COM0 of each segment pin is output.

② When DC output is selected, either complementary output or Pch open drain output can be selected for each pin by mask option.

Note *The pin pairs are the combination of SEG (2*n) and SEG (2*n + 1) (where n is an integer from 0 to 12).*

(4) Drive bias

For the drive bias of the E0C6S37 or the E0C6SL37, either 1/3 bias or 1/2 bias can be selected by the mask option. When using the LCD system regulated voltage circuit, it is fixed at 1/3 bias.
The E0C6SB37 can only use 1/3 bias.

Control of LCD driver

Table 4.6.2 shows the control bits of the LCD driver and their addresses. Figure 4.6.10 shows the display memory map.

Table 4.6.2 Control bits of LCD driver

Address	Register								Comment
	D3	D2	D1	D0	Name	SR	1	0	
0FBH	CSDC	0	0	0	CSDC	0	Static	Dynamic	LCD drive switch
	R/W	R			0				
					0				
					0				

Fig. 4.6.10 Display memory map

Address	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
090	Display memory (Write only) 32 words x 4 bits															
0A0																

CSDC LCD drive switch (0FBH D3)

The LCD drive format can be selected with this switch.

When 1 is written: Static drive
When 0 is written: Dynamic drive
Reading: Valid

After an initial reset, dynamic drive (CSDC = 0) is selected.

Display memory (090H–0AFH)

The LCD segments are turned on or off according to this data.

When 1 is written: On
When 0 is written: Off
Reading: Invalid

By writing data into the display memory allocated to the LCD segment (on the panel), the segment can be turned on or off. After an initial reset, the contents of the display memory are undefined.

4.7 Clock Timer

Configuration of clock timer

The E0C6S37 Series have a built-in clock timer driven by the source oscillator. The clock timer is configured as a seven-bit binary counter that serves as a frequency divider taking a 256 Hz source clock from the dividing circuit. The four high-order bits (16 Hz–2 Hz) can be read by the software.
Figure 4.7.1 is the block diagram of the clock timer.

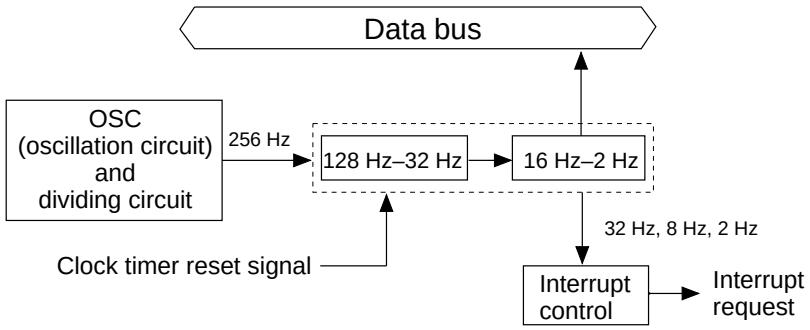


Fig. 4.7.1
Block diagram of clock timer

Normally, this clock timer is used for all kinds of timing purpose, such as clocks.

Interrupt function

The clock timer can interrupt on the falling edge of the 32 Hz, 8 Hz, and 2 Hz signals. The software can mask any of these interrupt signals.
Figure 4.7.2 is the timing chart of the clock timer.

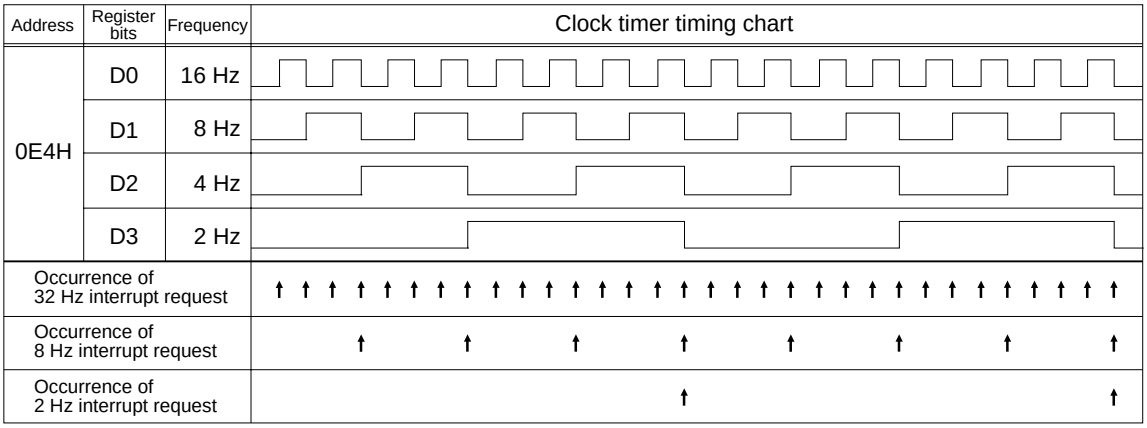


Fig. 4.7.2 Timing chart of the clock timer

As shown in Figure 4.7.2, an interrupt is generated on the falling edge of the 32 Hz, 8 Hz, and 2 Hz frequencies. When this happens, the corresponding interrupt event flag (IT32, IT8, IT2) is set to 1. Masking the separate interrupts can be done with the interrupt mask register (EIT32, EIT8, EIT2). However, regardless of the interrupt mask register setting, the interrupt event flags will be set to 1 on the falling edge of their corresponding signal (e.g. the falling edge of the 2 Hz signal sets the 2 Hz interrupt factor flag to 1).

Note *Write to the interrupt mask register (EIT32, EIT8, EIT2) and read the interrupt factor flags (IT32, IT8, IT2) only in the DI status (interrupt flag = 0). Otherwise, it causes malfunction.*

Control of clock timer

Table 4.7.1 shows the clock timer control bits and their addresses.

Table 4.7.1 Control bits of clock timer

Address	Register D3	D2	D1	D0	Name	SR	1	0	Comment
0E4H	TM3	TM2	TM1	TM0	TM3	–	High	Low	Timer data (clock timer 2 Hz)
	R				TM2	–	High	Low	Timer data (clock timer 4 Hz)
					TM1	–	High	Low	Timer data (clock timer 8 Hz)
					TM0	–	High	Low	Timer data (clock timer 16 Hz)
0EBH	0	EIT2	EIT8	EIT32	0				
	R	R/W			EIT2	0	Enable	Mask	Interrupt mask register (clock timer 2 Hz)
					EIT8	0	Enable	Mask	Interrupt mask register (clock timer 8 Hz)
					EIT32	0	Enable	Mask	Interrupt mask register (clock timer 32 Hz)
0EFH	0	IT2	IT8	IT32	0				
	R				IT2	0	Yes	No	Interrupt factor flag (clock timer 2 Hz)
					IT8	0	Yes	No	Interrupt factor flag (clock timer 8 Hz)
					IT32	0	Yes	No	Interrupt factor flag (clock timer 32 Hz)
0F9H	0	TMRST	SWRUN	SWRST	0				
	R	W	R/W	W	TMRST	Reset	Reset	–	Clock timer reset
					SWRUN	0	Run	Stop	Stopwatch timer RUN/STOP
					SWRST	Reset	Reset	–	Stopwatch timer reset

TM0–TM3 Timer data (0E4H)

The l6 Hz to 2 Hz timer data of the clock timer can be read from this register. These four bits are read-only, and write operations are invalid.

After an initial reset, the timer data is initialized to 0H.

EIT32, EIT8, EIT2 Interrupt mask registers (0EBH D0–D2)

These registers are used to mask the clock timer interrupt.

When 1 is written:	Enabled
When 0 is written:	Masked
Reading:	Valid

The interrupt mask register bits (EIT32, EIT8, EIT2) mask the corresponding interrupt frequencies (32 Hz, 8 Hz, 2 Hz). After an initial reset, these registers are all set to 0.

IT32, IT8, IT2 Interrupt factor flags (0EFH D0–D2)

These flags indicate the status of the clock timer interrupt.

When 1 is read:	Interrupt has occurred
When 0 is read:	Interrupt has not occurred
Writing:	Invalid

The interrupt factor flags (IT32, IT8, IT2) correspond to the clock timer interrupts (32 Hz, 8 Hz, 2 Hz). The software can determine from these flags whether there is a clock timer interrupt. However, even if the interrupt is masked, the flags are set to 1 on the falling edge of the signal. These flags can be reset when the register is read by the software. Reading of interrupt factor flags is available at EI, but be careful in the following cases.

If the interrupt mask register value corresponding to the interrupt factor flags to be read is set to 1, an interrupt request will be generated by the interrupt factor flags set timing, or an interrupt request will not be generated. Be very careful when interrupt factor flags are in the same address.

After an initial reset, these flags are set to 0.

TMRST Clock timer reset (0F9H D2)

This bit resets the clock timer.

When 1 is written:	Clock timer reset
When 0 is written:	No operation
Reading:	Always 0

The clock timer is reset by writing 1 to TMRST. The clock timer starts immediately after this. No operation results when 0 is written to TMRST.

This bit is write-only, and so is always 0 when read.

4.8 Stopwatch Timer

Configuration of stopwatch timer

The E0C6S37 Series incorporate a 1/100 sec and 1/10 sec stopwatch timer. The stopwatch timer is configured as a two-stage, four-bit BCD timer serving as the clock source for an approximately 100 Hz signal (obtained by approximately dividing the 256 Hz signal output from the dividing circuit). Data can be read out four bits at a time by the software. Figure 4.8.1 is the block diagram of the stopwatch timer.

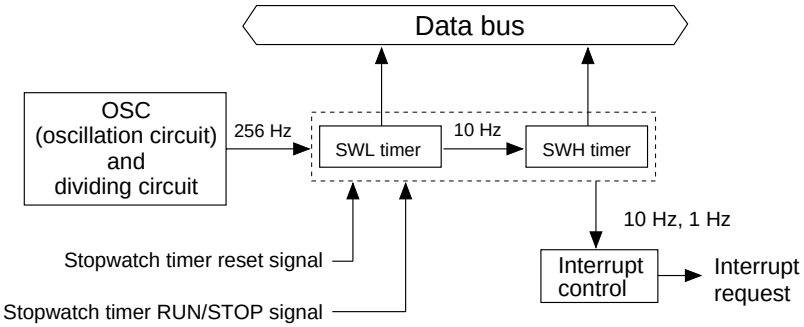


Fig. 4.8.1
Block diagram of stopwatch timer

The stopwatch timer can be used separately from the clock timer. In particular, digital stopwatch functions can be easily realized by software.

Count-up pattern

The stopwatch timer is configured as two four-bit BCD timers, SWL and SWH. The SWL timer, at the stage preceding the stopwatch timer, has an approximate l00 Hz signal as its input clock. It counts up every 1/100 sec and generates an approximate 10 Hz signal. The SWH timer has an approximate 10 Hz signal generated by the SWL timer for its input clock. It counts up every 1/10 sec and generates a 1 Hz signal.

Figure 4.8.2 shows the count-up pattern of the stopwatch timer.

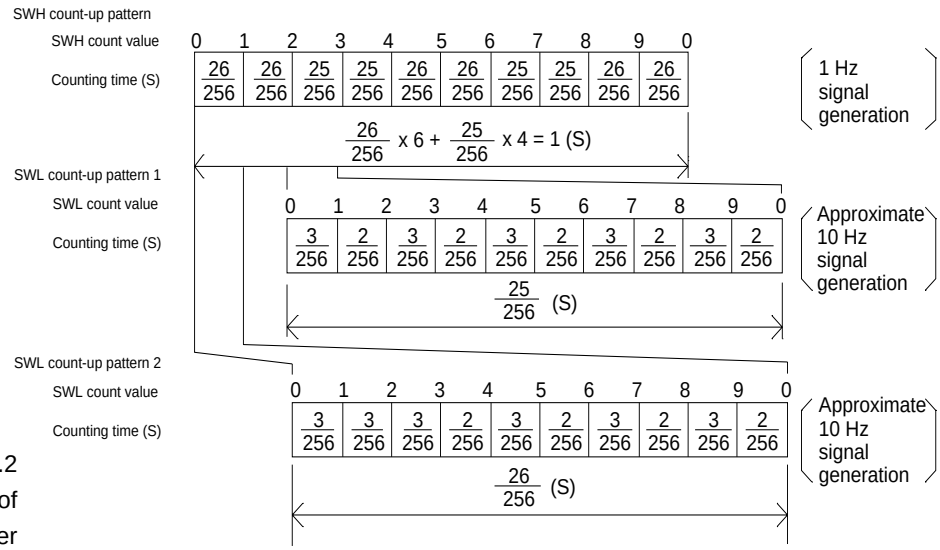


Fig. 4.8.2
Count-up pattern of stopwatch timer

SWL generates an approximate 10 Hz signal from the 256 Hz based signal. The count-up intervals are 2/256 sec and 3/256 sec, so that two final patterns are generated: a 25/256 sec interval and a 26/256 sec interval. Consequently, the count-up intervals are 2/256 sec and 3/256 sec, which do not amount to an accurate 1/100 sec. SWH counts the approximate 10 Hz signals generated by the 25/256 sec and 26/256 sec intervals in the ratio of 4:6 to generate a l Hz signal. The count-up intervals are 25/256 sec and 26/256 sec, which do not amount to an accurate 1/10 sec.

Interrupt function

The 10 Hz (approximate 10 Hz) and 1 Hz interrupts can be generated by the overflow of the SWL and SWH stopwatch timers, respectively. Also, software can separately mask the frequencies as described earlier.
Figure 4.8.3 is the timing chart for the stopwatch timer.

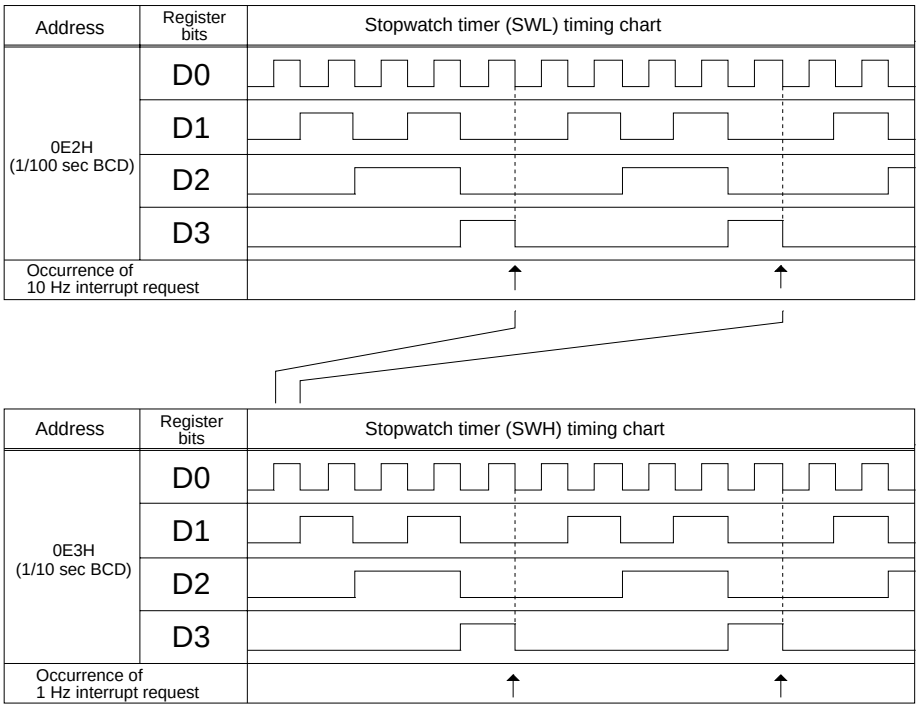


Fig. 4.8.3
Timing chart for stopwatch timer

As shown in Figure 4.8.3, the interrupts are generated by the overflow of the respective timers (9 changing to 0). Also when this happens, the corresponding interrupt factor flags (ISW0, ISW1) are set to 1. The respective interrupts can be masked separately with the interrupt mask registers (EISW0, EISW1). However, regardless of the setting of the interrupt mask registers, the interrupt factor flags are set to 1 by the overflow of the corresponding timers.

Note *Write to the interrupt mask registers (EISW0, EISW1) and read the interrupt factor flags (ISW0, ISW1) only in the DI status (interrupt flag = 0). Otherwise, it causes malfunction.*

Control of stopwatch timer

Table 4.8.1 shows the stopwatch timer control bits and their addresses.

Table 4.8.1 Stopwatch timer control bits

Address	Register D3	D2	D1	D0	Name	SR	1	0	Comment
0E2H	SWL3	SWL2	SWL1	SWL0	SWL3	0			MSB
	R				SWL2	0			Stopwatch timer 1/100 sec (BCD)
					SWL1	0			
					SWL0	0			LSB
0E3H	SWH3	SWH2	SWH1	SWH0	SWH3	0			MSB
	R				SWH2	0			Stopwatch timer 1/10 sec (BCD)
					SWH1	0			
					SWH0	0			LSB
0EAH	0	0	EISW1	EISW0	0				
	R		R/W		0				
					EISW1	0	Enable	Mask	Interrupt mask register (stopwatch 1 Hz)
					EISW0	0	Enable	Mask	Interrupt mask register (stopwatch 10 Hz)
0EEH	0	0	ISW1	ISW0	0				
	R				0				
					ISW1	0	Yes	No	Interrupt factor flag (stopwatch 1 Hz)
					ISW0	0	Yes	No	Interrupt factor flag (stopwatch 10 Hz)
0F9H	0	TMRST	SWRUN	SWRST	0				
	R	W	R/W	W	TMRST	Reset	Reset	–	Clock timer reset
					SWRUN	0	Run	Stop	Stopwatch timer RUN/STOP
					SWRST	Reset	Reset	–	Stopwatch timer reset

SWL0–SWL3 1/100 sec stopwatch timer (0E2H)

Data (BCD) of the 1/100 sec column of the stopwatch timer can be read. These four bits are read-only, and cannot be written to.

After an initial reset, the timer data is set to 0H.

SWH0–SWH3 1/10 sec stopwatch timer (0E3H)

Data (BCD) of the 1/10 sec column of the stopwatch timer can be read. These four bits are read-only, and cannot be written to.

After an initial reset, the timer data is set to 0H.

EISW0, EISW1 Interrupt mask register (0EAH D0 and D1)

These registers mask the stopwatch timer interrupt.

When 1 is written:	Enabled
When 0 is written:	Masked
Reading:	Valid

The interrupt mask register bits (EISW0, EISW1) are used to mask the 10 Hz and 1 Hz interrupts, respectively.

After an initial reset, these registers are both set to 0.

ISW0, ISW1 Interrupt factor flags (0EEH D0 and D1)

These flags indicate the status of the stopwatch timer interrupt.

When 1 is read:	Interrupt has occurred
When 0 is read:	Interrupt has not occurred
Writing:	Invalid

The interrupt factor flags (ISW0, ISW1) correspond to the 10 Hz and 1 Hz interrupts, respectively. With these flags, the software can determine whether a stopwatch timer interrupt has occurred. However, regardless of the interrupt mask register setting, these flags are set to 1 by the timer overflow.

They are reset when the register is read by the software. Reading of interrupt factor flags is available at EI, but be careful in the following cases.

If the interrupt mask register value corresponding to the interrupt factor flags to be read is set to 1, an interrupt request will be generated by the interrupt factor flags set timing, or an interrupt request will not be generated.

Be very careful when interrupt factor flags are in the same address.
After an initial reset, these flags are set to 0.

SWRST Stopwatch timer reset (0F9H D0)

This bit resets the stopwatch timer.

When 1 is written:	Stopwatch timer reset
When 0 is written:	No operation
Reading:	Always 0

The stopwatch timer is reset when 1 is written to SWRST. When the stopwatch timer is reset while running, operation restarts immediately. Also, while stopped, the reset data is maintained.
This bit is write-only, and is always 0 when read.

SWRUN Stopwatch timer run/stop (0F9H D1)

This bit controls run/stop of the stopwatch timer.

When 1 is written:	Run
When 0 is written:	Stop
Reading:	Valid

The stopwatch timer runs when 1 is written to SWRUN, and stops when 0 is written.
When stopped, the timer data is maintained until the timer next Run or is reset. Also, when the timer runs after being stopped, the data that was maintained can be used to resume the count.
If the timer data is read while running, a correct read may be impossible because of the carry from the low-order bit (SWL) to the high-order bit (SWH). This occurs if reading has extended over the SWL and SWH bits when the carry occurs. To prevent this, read after stopping, and then continue running. Also, the stopped duration must be within 976 μs (256 Hz, 1/4 cycle).
After an initial reset, this register is set to 0.

4.9 Supply Voltage Detection (SVD) Circuit and Heavy Load Protection Function

Configuration of SVD circuit and heavy load protection function

The E0C6S37 Series have a built-in supply voltage detection (SVD) circuit and a heavy load protection function. Figure 4.9.1 shows the configuration of the circuit.

SVD circuit

The SVD circuit monitors the conditions of the supply voltage (battery voltage), and software can check whether the supply voltage has dropped below the detecting voltage level of the SVD circuit: 2.4 V for the E0C6S37 (supply voltage is 3.0 V), or l.2 V for the E0C6SL37 (1.5 V) and the E0C6SB37 (3.0 V). Registers SVDON (SVD control on/off) and SVDDT (SVD data) are used for the SVD circuit. The software can turn SVD operation on and off. When SVD is on, the IC draws a large current, so keep SVD off unless it is.
Since supply voltage detection is automatically performed by the hardware every 2 Hz (0.5 sec) when the heavy load protection function operates, do not permit the operation of the SVD circuit by the software in order to minimize power current consumption.

Heavy load protection function

Note that the heavy load protection function on the E0C6SL37/E0C6SB37 are different from the E0C6S37.

(1) In case of E0C6SL37/E0C6SB37

The E0C6SL37/E0C6SB37 have the heavy load protection function for when the battery load becomes heavy and the source voltage drops, such as when an external buzzer sounds or an external lamp lights. The state where the heavy load protection function is in effect is called the heavy load protection mode. In this mode, operation with a lower voltage than normal is possible. The normal mode changes to the heavy load protection mode in the following two cases:

① When the software changes the mode to the heavy load protection mode (HLMOD = 1)

② When supply voltage drop (SVDDT = 1) in the SVD circuit is detected, the mode will automatically shift to the heavy load protection mode until the supply voltage is recovered (SVTDT = 0)

In the heavy load protection mode, the internally regulated voltage is generated by the liquid crystal driver source output V_{L2} so as to operate the internal circuit. Consequently, more current is consumed in the heavy load protection mode than in the normal mode. Unless it is necessary, be careful not to set the heavy load protection mode with the software. Also, to reduce current consumption, do not set the SVDON to ON in the heavy load protection mode.

Note that in E0C6SL37/E0C6SB37, the range of operating voltage differs during CR oscillation and during crystal oscillation.

(2) In case of E0C6S37

The E0C6S37 has the heavy load protection function for when the battery load becomes heavy and the source voltage changes, such as when an external buzzer sounds or an external lamp lights. The state where the heavy load protection function is in effect is called the heavy load protection mode. Compared with the normal operation mode, this mode can reduce the output voltage variation of the constant voltage or voltage booster/reducer of the LCD system.
The normal mode changes to the heavy load protection mode in the following case:

- When the software changes the mode to the heavy load protection mode (HLMOD = 1)

The heavy load protection mode switches the constant voltage circuit of the LCD system to the high-stability mode from the low current consumption mode. Consequently, more current is consumed in the heavy load protection mode than in the normal mode. Unless it is necessary, be careful not to set the heavy load protection mode with the software.

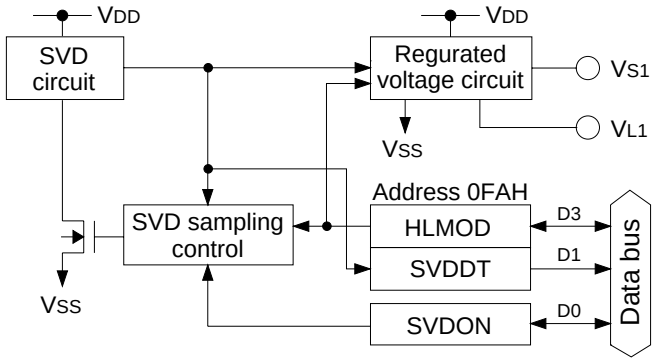


Fig. 4.9.1
Configuration of SVD and heavy load protection circuits

Operation of SVD detection timing

The following explains the timing when the SVD circuit writes the result of supply voltage detection to the SVDDT register.
The result of supply voltage detection is written to the SVDDT register by the SVD circuit, and this data can be read by the software to determine the supply voltage.
There are two methods, explained below, for executing the detection by the SVD circuit.

(1) Sampling with HLMOD set to 1

When HLMOD is set to 1 and SVD sampling is executed, the detection results can be written to the SVDDT register with the following timing:

Immediately after sampling with the 2 Hz cycle output by the oscillation circuit while HLMOD = 1 (sampling time is 122 µs in the case of fosc = 32.768 kHz).

Consequently, after HLMOD has been set to 1, the new detection result is written in a 2 Hz.

(2) Sampling with SVDON set to 1

When SVDON is set to 1, SVD detection is executed. As soon as SVDON is reset to 0, the result is loaded to in the SVDDT register. To obtain a stable SVD detection result, the SVD circuit must be on for at least l00 µs. So, to obtain the SVD detection result, follow the programming sequence below.

① Set SVDON to 1
② Maintain for 100 µs minimum
③ Set SVDON to 0
④ Read SVDDT

However, at 32 kHz for the E0C6S37, E0C6SL37 and E0C6SB37, the instruction cycles are long enough, so there is no need to worry about maintaining 100 µs for SVDON = 1 in the software.

Notice that even if the SVD circuit detects a drop in the supply voltage (l.2 V/2.4 V or less) and invokes the heavy load protection mode, this will be the same as when the software invokes the heavy load protection mode, in that the SVD circuit will be sampled with a timing synchronized to the 2 Hz output from the prescaler. If the SVD circuit detects a voltage drop and enters the heavy load protection mode, it will return to the normal mode once the supply voltage recovers and the SVD circuit determines that the supply voltage is l.2 V/2.4 V or more.

Operation of heavy load protection function

The E0C6S37 Series have a heavy load protection function for when the battery load becomes heavy and the supply voltage drops, such as when a melody is played or an external lamp lights. This functions works in the heavy load protection mode.

(1) In cace of E0C6SL37/E0C6SB37

The normal mode changes to the heavy load protection mode in the following two cases:

① When the software changes the mode to the heavy load protection mode

② When the SVD circuit detects a supply voltage less than l.2 V, in which case the mode is automatically changed to the heavy load protection mode

(2) In case of E0C6S37

The normal mode changes to the heavy load protection mode in the following case:

- When the software changes the mode to the heavy load protection mode (HLMOD = 1)

Based on the operation of the SVD circuit and the heavy load protection function, the E0C6SL37/E0C6SB37 obtains an operation supply voltage as low as 0.9 V. See the electrical characteristics for the precision of voltage detection by the SVD circuit.

In the heavy load protection mode, the internally regulated voltage is generated by the liquid crystal driver supply output, V_{L2}, in order to operate the internal circuit (E0C6SL37/E0C6SB37). Consequently, more current is consumed in the heavy load protection mode than in the normal mode. Unless necessary, do not select the heavy load protection mode with the software.

Note *Activation of the SVD circuit by software in the heavy load protection mode causes a malfunction. Avoid such activation if possible.*

Control of SVD circuit and heavy load protection function

Table 4.9.1 shows the control bits and their addresses for the SVD circuit and the heavy load protection function.

Table 4.9.1 Control bits for SVD circuit and heavy load protection function

Address	Register								Comment
	D3	D2	D1	D0	Name	SR	1	0	
0FAH	HLMOD	0	SVDDT	SVDON	HLMOD	0	Heavy load	Normal load	Heavy load protection mode register
	R/W	R		R/W	0				
					SVDDT	0	Supply voltage low	Supply voltage normal	Supply voltage detection data
					SVDON	0	ON	OFF	Supply voltage detection ON/OFF

HLMOD Heavy load protection mode on/off (0FAH D3)

When 1 is written: Heavy load protection mode on
When 0 is written: Heavy load protection mode off
Reading: Valid

When HLMOD is set to 1, the IC enters the heavy load protection mode, and sampling control is executed for the time the SVD circuit is on. The sampling timing is as follows:

Sampling in cycles of 2 Hz output by the oscillation circuit while HLMOD = 1 (sampling time is 122 µs in the case of fosc = 32.768 kHz).

When SVD sampling is done with HLMOD set to 1, the results are written to the SVDDT register with the as following timing:

Immediately on completion of sampling in cycles of 2 Hz output by the oscillation circuit while HLMOD = 1.

Consequently, after HLMOD is set to 1, the new detected result is written in 2 Hz.
In the heavy load protection mode, the consumed current becomes larger. Unless necessary, do not select the heavy load protection mode with the software.

SVDON SVD control on/off (0FAH D0)

When 0 is written: SVD detection off
When 1 is written: SVD detection on
Reading: Valid

When this bit is written, the SVD detection on/off operation is controlled. Large current is drawn during SVD detection, so keep SVD detection off except when necessary. When SVDON is set to 1, SVD detection is executed. As soon as SVDON is reset to 0, the detected result is loaded into the SVDDT register.

SVDDT SVD data (0FAH D1)

When 0 is read: Supply voltage ≥ Criteria voltage
When 1 is read: Supply voltage < Criteria voltage

When SVDDT is 1, the E0C6S37 enters the heavy load protection mode. In this mode, the detection operation of the SVD circuit is sampled in 2 Hz cycles and the respective detection results are written to the SVDDT register.

4.10 Interrupt and HALT

The E0C6S37 Series provide the following interrupt settings, each of which is maskable.

External interrupt:	Input interrupt (one)
Internal interrupt:	Timer interrupt (one)
	Stopwatch interrupt (one)

To enable interrupts, the interrupt flag must be set to 1 (EI) and the necessary related interrupt mask registers must be set to 1 (enable). When an interrupt occurs, the interrupt flag is automatically reset to 0 (DI) and interrupts after that are inhibited.
When a HALT instruction is input, the CPU operating clock stops and the CPU enters the halt state. The CPU is reactivated from the halt state when an interrupt request occurs.
Figure 4.10.1 shows the configuration of the interrupt circuit.

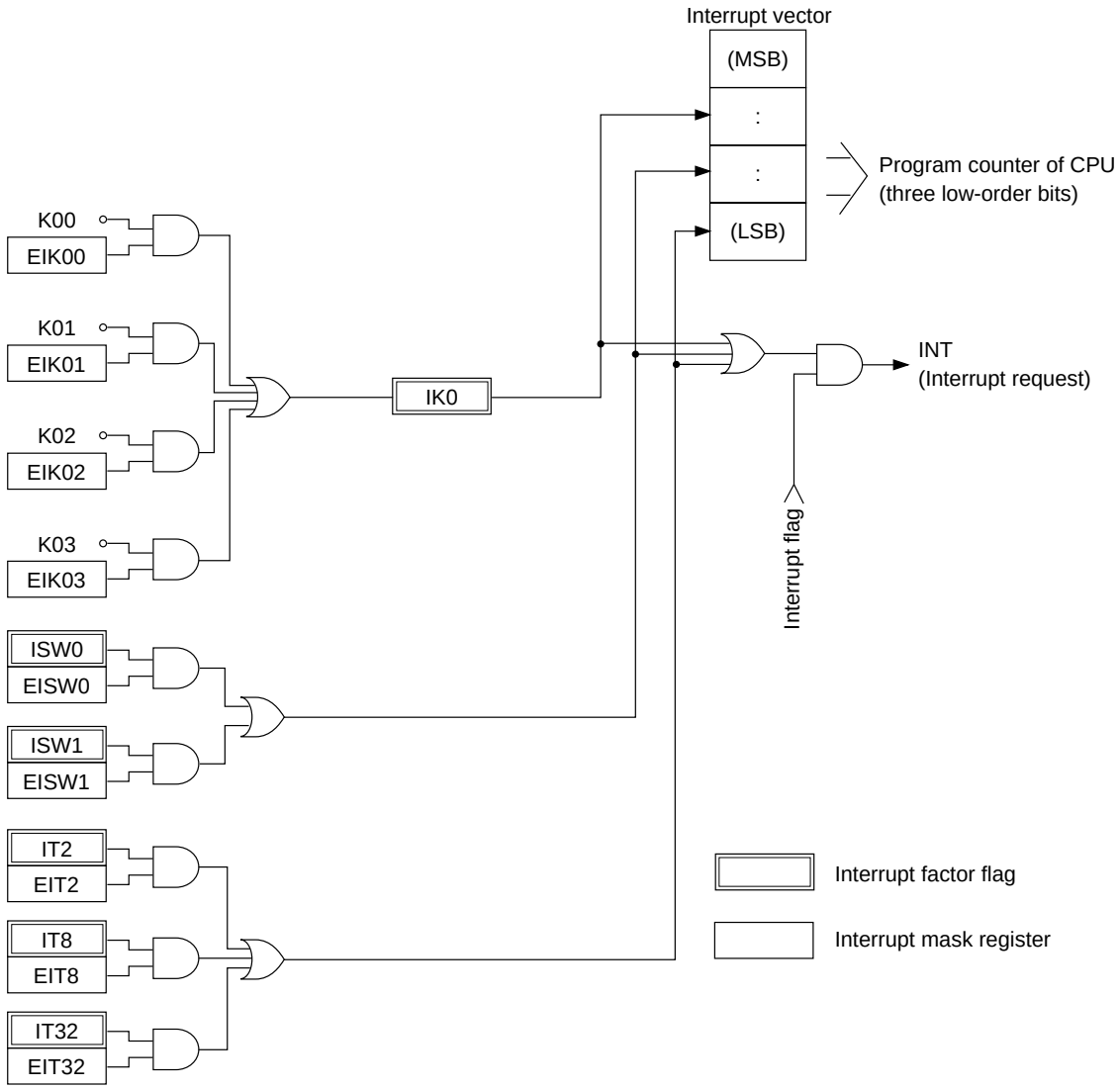


Fig. 4.10.1 Configuration of interrupt circuit

Interrupt factors

Table 4.10.1 shows the factors that generate interrupt requests.

The interrupt factor flags are set to 1 depending on the corresponding interrupt factors.

The CPU is interrupted when the following two conditions occur and an interrupt factor flag is set to 1.

- The corresponding mask register is 1 (enabled)
- The interrupt flag is 1 (EI)

The interrupt factor flag is a read-only register, but can be reset to 0 when the register data is read.
After an initial reset, the interrupt factor flags are reset to 0.

Note *Reading of interrupt factor flags is available at EI, but be careful in the following cases.*
If the interrupt mask register value corresponding to the interrupt factor flags to be read is set to 1, an interrupt request will be generated by the interrupt factor flags set timing, or an interrupt request will not be generated. Be very careful when interrupt factor flags are in the same address.

Table 4.10.1 Interrupt factors

Interrupt Factor	Interrupt Factor Flag	
Colck timer 2 Hz falling edge	IT2	(0EFH D2)
Colck timer 8 Hz falling edge	IT8	(0EFH D1)
Colck timer 32 Hz falling edge	IT32	(0EFH D0)
Stopwatch timer 1 Hz falling edge	ISW1	(0EEH D1)
Stopwatch timer 10 Hz falling edge	ISW0	(0EEH D0)
Input data (K00–K03) rising edge	IK0	(0EDH D0)

Specific masks and factor flags for interrupt

The interrupt factor flags can be masked by the corresponding interrupt mask registers. The interrupt mask registers are read/write registers. They are enabled (interrupt enabled) when 1 is written to them, and masked (interrupt disabled) when 0 is written to them. After an initial reset, the interrupt mask register is set to 0.
Table 4.10.2 shows the correspondence between interrupt mask registers and interrupt factor flags.

Table 4.10.2
Interrupt mask registers and interrupt factor flags

Interrupt Mask Register		Interrupt Factor Flag	
EIT2	(0EBH D2)	IT2	(0EFH D2)
EIT8	(0EBH D1)	IT8	(0EFH D1)
EIT32	(0EBH D0)	IT32	(0EFH D0)
EISW1	(0EAH D1)	ISW1	(0EEH D1)
EISW0	(0EAH D0)	ISW0	(0EEH D0)
EIK03*	(0E8H D3)	IK0	(0EDH D0)
EIK02*	(0E8H D2)		
EIK01*	(0E8H D1)		
EIK00*	(0E8H D0)		

* There is an interrupt mask register for each input port pin.

Interrupt vectors

When an interrupt request is input to the CPU, the CPU begins interrupt processing. After the program being executed is suspended, interrupt processing is executed in the following order:

① The address data (value of the program counter) of the program step to be executed next is saved on the stack (RAM).

② The interrupt request causes the value of the interrupt vector (page 1, 01H–07H) to be loaded into the program counter.

③ The program at the specified address is executed (execution of interrupt processing routine).

Note *The processing in steps 1 and 2, above, takes 12 cycles of the CPU system clock.*

Control of interrupt

Tables 4.10.3 (a) and (b) shows the interrupt control bits and their addresses.

Table 4.10.3 (a) Interrupt control bits (1)

Address	Register								Comment
	D3	D2	D1	D0	Name	SR	1	0	
0E8H	EIK03	EIK02	EIK01	EIK00	EIK03	0	Enable	Mask	Interrupt mask register (K03)
	R/W				EIK02	0	Enable	Mask	Interrupt mask register (K02)
					EIK01	0	Enable	Mask	Interrupt mask register (K01)
					EIK00	0	Enable	Mask	Interrupt mask register (K00)
0EAH	0	0	EISW1	EISW0	0				
	R		R/W		0				
					EISW1	0	Enable	Mask	Interrupt mask register (stopwatch 1 Hz)
					EISW0	0	Enable	Mask	Interrupt mask register (stopwatch 10 Hz)
0EBH	0	EIT2	EIT8	EIT32	0				
	R	R/W			EIT2	0	Enable	Mask	Interrupt mask register (clock timer 2 Hz)
					EIT8	0	Enable	Mask	Interrupt mask register (clock timer 8 Hz)
					EIT32	0	Enable	Mask	Interrupt mask register (clock timer 32 Hz)
0EDH	0	0	0	IK0	0				
	R				0				
					0				
					IK0	0	Yes	No	Interrupt factor flag (K00–K03)

Table 4.10.3 (b) Interrupt control bits (2)

Address	Register								Comment
	D3	D2	D1	D0	Name	SR	1	0	
0EEH	0	0	ISW1	ISW0	0				
	R				0				
					ISW1	0	Yes	No	Interrupt factor flag (stopwatch 1 Hz)
					ISW0	0	Yes	No	Interrupt factor flag (stopwatch 10 Hz)
0EFH	0	IT2	IT8	IT32	0				
	R				IT2	0	Yes	No	Interrupt factor flag (clock timer 2 Hz)
					IT8	0	Yes	No	Interrupt factor flag (clock timer 8 Hz)
					IT32	0	Yes	No	Interrupt factor flag (clock timer 32 Hz)

EIT32, EIT8, EIT2 Interrupt mask registers (0EBH D0–D2)

IT32, IT8, IT2 Interrupt factor flags (0EFH D0–D2)

See 4.7, "Clock Timer".

EISW0, EISW1 Interrupt mask registers (0EAH D0–D1)

ISW0, ISW1 Interrupt factor flags (0EEH D0–D1)

See 4.8, "Stopwatch Timer".

EIK00–EIK03 Interrupt mask registers (0E8H)

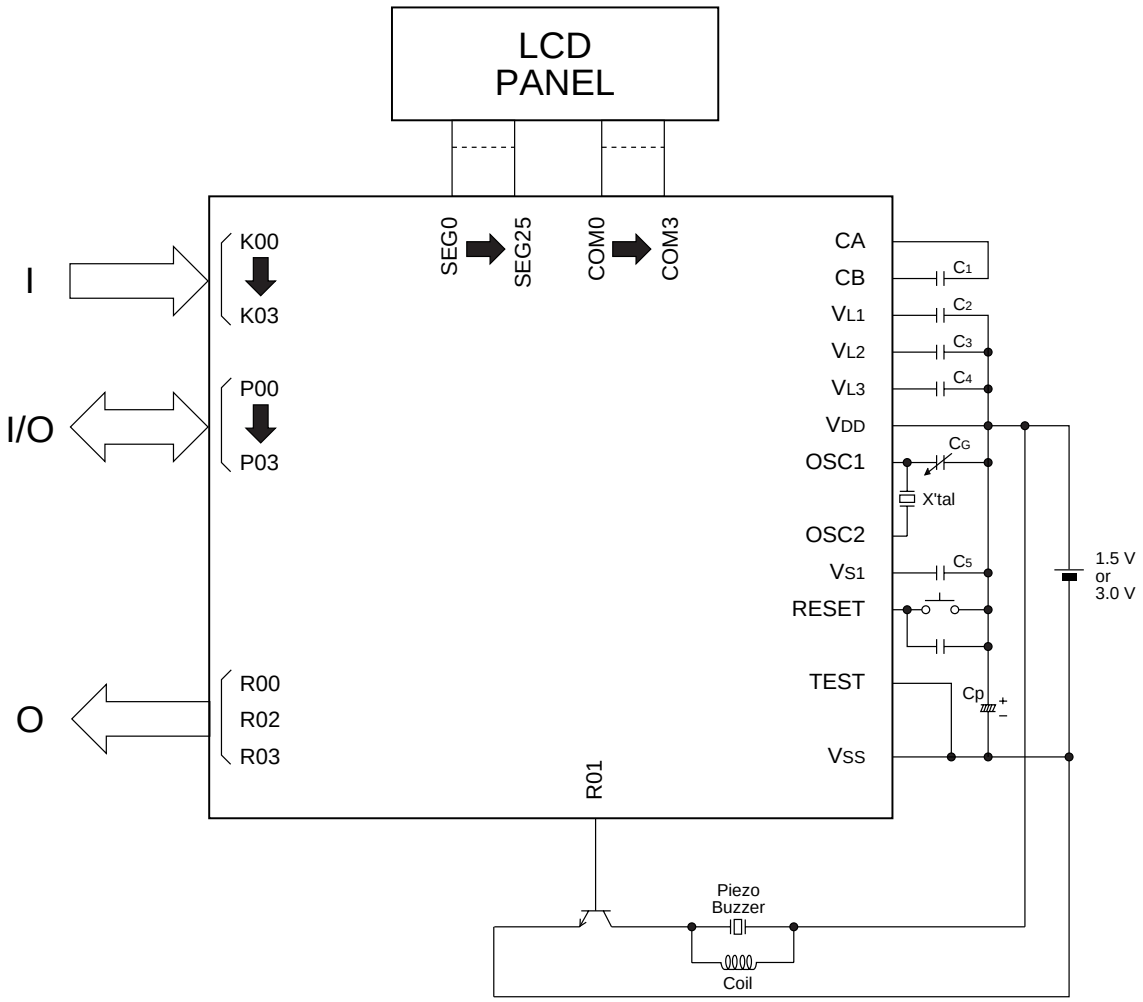
IK0 Interrupt factor flag (0EDH D0)

See 4.3, "Input Port".

CHAPTER 5 BASIC EXTERNAL WIRING DIAGRAM

(1) Piezo Buzzer Single Terminal Driving

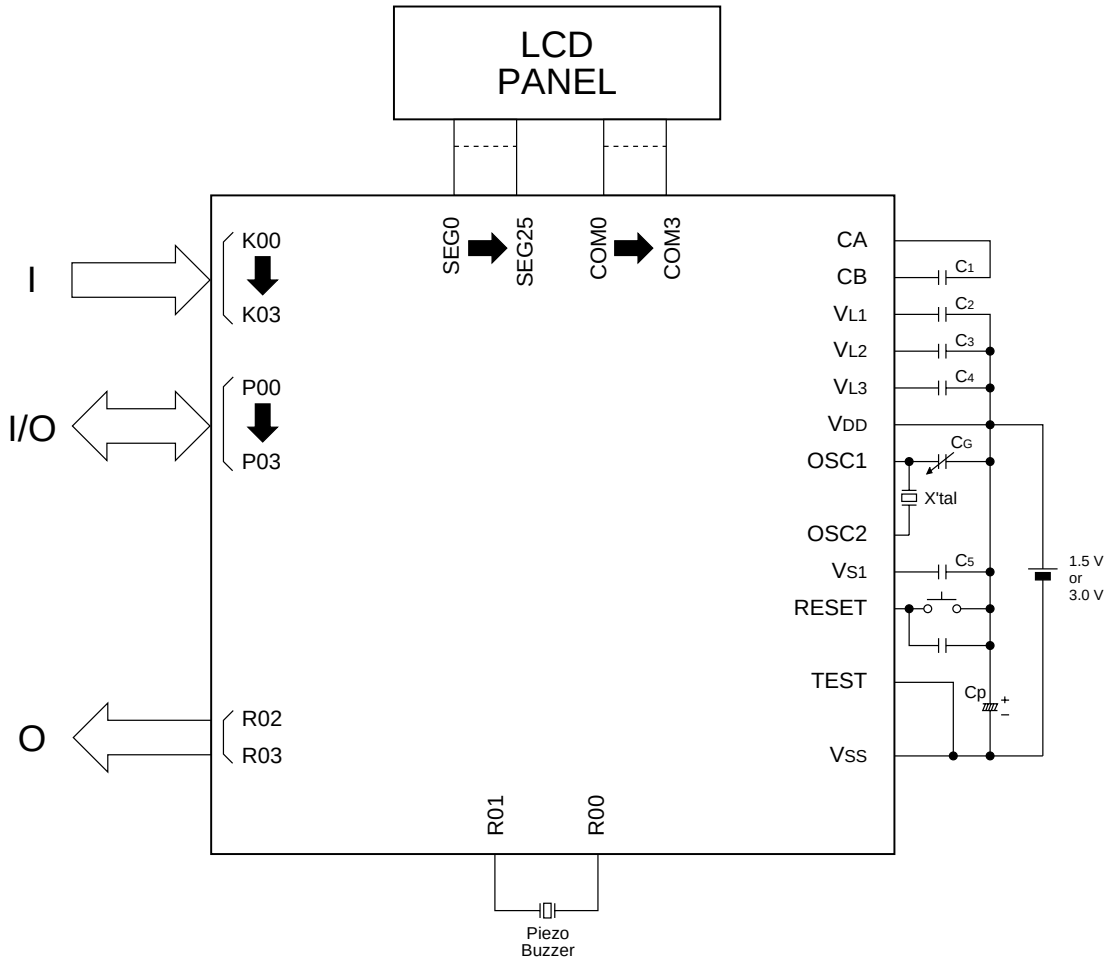
(When LCD system regulated voltage circuit is used)



X'tal	Crystal oscillator	32.768 kHz CI(MAX) = 35 kΩ
C_G	Trimmer capacitor	5–25 pF
C_1–C_5	Capacitor	0.1 µF
Cp	Capacitor	3.3 µF

(2) Piezo Buzzer Direct Driving

(When LCD system regulated voltage circuit is used)



X'tal	Crystal oscillator	32.768 kHz CI(MAX) = 35 kΩ
C_G	Trimmer capacitor	5–25 pF
C_1–C_5	Capacitor	0.1 µF
Cp	Capacitor	3.3 µF

CHAPTER 6 ELECTRICAL CHARACTERISTICS

6.1 Absolute Maximum Rating

(V_{DD}=0V)

Item	Symbol	Rated Value	Unit
Power voltage	V_{SS}	-5.0 to 0.5	V
Input voltage (1)	V_I	Vss-0.3 to 0.5	V
Input voltage (2)	V_{IOSC}	Vss-0.3 to 0.5	V
Permissible total output current *1	$\sum I_{VSS}$	10	mA
Operating temperature	Topr	-20 to 70	°C
Storage temperature	Tstg	-65 to 150	°C
Soldering temperature / Time	Tsol	260°C, 10sec (lead section)	–
Allowable dissipation *2	P_D	250	mW

∗1 The permissible total output current is the sum total of the current (average current) that simultaneously flows from the output pins (or is draw in).

∗2 In case of QFP6-60pin plastic package

6.2 Recommended Operating Conditions

E0C6S37

(Ta=-20 to 70°C)

Item	Symbol	Condition	Min	Typ	Max	Unit
Power voltage	V_{SS}	V_{DD}=0V	-3.6	-3.0	-1.8	V
Oscillation frequency	f_{OSC1}	Crystal oscillation		32.768		kHz
	f_{OSC2}	CR oscillation, R=470kΩ	50	65	80	kHz
Booster capacitor	C1		0.1			µF
Capacitor between V_{DD} and V_{L1}	C2		0.1			µF
Capacitor between V_{DD} and V_{L2}	C3		0.1			µF
Capacitor between V_{DD} and V_{L3}	C4		0.1			µF
Capacitor between V_{DD} and V_{S1}	C5		0.1			µF

E0C6SL37

(Ta=-20 to 70°C)

Item	Symbol	Condition	Min	Typ	Max	Unit
Power voltage	V_{SS}	V_{DD}=0V *3	-2.0	-1.5	-1.1	V
		V_{DD}=0V With software control *1	-2.0	-1.5	-0.9 *2	V
Oscillation frequency	f_{OSC1}	Crystal oscillation		32.768		kHz
	f_{OSC2}	CR oscillation, R=470kΩ	50	65	80	kHz
Booster capacitor	C1		0.1			µF
Capacitor between V_{DD} and V_{L1}	C2		0.1			µF
Capacitor between V_{DD} and V_{L2}	C3		0.1			µF
Capacitor between V_{DD} and V_{L3}	C4		0.1			µF
Capacitor between V_{DD} and V_{S1}	C5		0.1			µF

*1 When the heavy load protection mode is set by software and the SVD circuit is turned OFF. Cannot be operated when the CR oscillation circuit is used. (For details, refer to Section 4.9).

*2 The voltage which can be displayed on the LCD panel will differ according to the characteristics of the LCD panel.

*3 When there is no software control during CR oscillation or crystal oscillation.

E0C6SB37

(Ta=-20 to 70°C)

Item	Symbol	Condition	Min	Typ	Max	Unit
Power voltage	V_{SS}	V_{DD}=0V *3	-3.6	-1.5	-1.1	V
		V_{DD}=0V With software control *1	-3.6	-1.5	-0.9 *2	V
Oscillation frequency	f_{OSC1}	Crystal oscillation		32.768		kHz
	f_{OSC2}	CR oscillation, R=470kΩ	50	65	80	kHz
Booster capacitor	C1		0.1			µF
Capacitor between V_{DD} and V_{L1}	C2		0.1			µF
Capacitor between V_{DD} and V_{L2}	C3		0.1			µF
Capacitor between V_{DD} and V_{L3}	C4		0.1			µF
Capacitor between V_{DD} and V_{S1}	C5		0.1			µF

*1 When the heavy load protection mode is set by software and the SVD circuit is turned OFF. Cannot be operated when the CR oscillation circuit is used. (For details, refer to Section 4.9).

*2 The voltage which can be displayed on the LCD panel will differ according to the characteristics of the LCD panel.

*3 When there is no software control during CR oscillation or crystal oscillation.

6.3 DC Characteristics

E0C6S37/E0C6SB37

Unless otherwise specified

V_{DD}=0 V, V_{SS}=-3.0 V, fosc=32.768 kHz, Ta=25°C, V_{S1}, V_{L1}, V_{L2} and V_{L3} are internal voltages, and C1=C2=C3=C4=C5=0.1 µF

Item	Symbol	Condition		Min	Typ	Max	Unit
High level input voltage (1)	V_{IH1}		K00–K03, P00–P03	0.2•Vss		0	V
High level input voltage (2)	V_{IH2}		RESET	0.15•Vss		0	V
Low level input voltage (1)	V_{IL1}		K00–K03, P00–P03	Vss		0.8•Vss	V
Low level input voltage (2)	V_{IL2}		RESET	Vss		0.85•Vss	V
High level input current (1)	I_{IH1}	V_{IH1}=0V Without pull down resistor	K00–K03, P00–P03	0		0.5	µA
High level input current (2)	I_{IH2}	V_{IH2}=0V With pull down resistor	K00–K03	10		40	µA
High level input current (3)	I_{IH3}	V_{IH3}=0V With pull down resistor	P00–P03, RESET	30		100	µA
Low level input current	I_{IL}	V_{IL}=V_{SS}	K00–K03, P00–P03, RESET, TEST	-0.5		0	µA
High level output current (1)	I_{OH1}	V_{OH1}=0.1•V_{SS}	R02, R03, P00–P03			-1.0	mA
High level output current (2)	I_{OH2}	V_{OH2}=0.1•V_{SS} (built-in protection resistance)	R00, R01			-1.0	mA
Low level output current (1)	I_{OL1}	V_{OL1}=0.9•V_{SS}	R02, R03, P00–P03	3.0			mA
Low level output current (2)	I_{OL2}	V_{OL2}=0.9•V_{SS} (built-in protection resistance)	R00, R01	3.0			mA
Common output current	I_{OH3}	V_{OH3}=-0.05V	COM0–COM3			-3	µA
	I_{OL3}	V_{OL3}=V_{L3}+0.05V		3			µA
Segment output current (during LCD output)	I_{OH4}	V_{OH4}=-0.05V	SEG0–SEG25			-3	µA
	I_{OL4}	V_{OL4}=V_{L3}+0.05V		3			µA
Segment output current (during DC output)	I_{OH5}	V_{OH5}=0.1•V_{SS}	SEG0–SEG25			-300	µA
	I_{OL5}	V_{OL5}=0.9•V_{SS}		300			µA

E0C6SL37

Unless otherwise specified

V_{DD}=0 V, V_{SS}=-1.5 V, fosc=32.768 kHz, Ta=25°C, V_{S1}, V_{L1}, V_{L2} and V_{L3} are internal voltages, and C1=C2=C3=C4=C5=0.1 µF

Item	Symbol	Condition		Min	Typ	Max	Unit
High level input voltage (1)	V_{IH1}		K00–K03, P00–P03	0.2•Vss		0	V
High level input voltage (2)	V_{IH2}		RESET	0.15•Vss		0	V
Low level input voltage (1)	V_{IL1}		K00–K03, P00–P03	Vss		0.8•Vss	V
Low level input voltage (2)	V_{IL2}		RESET	Vss		0.85•Vss	V
High level input current (1)	I_{IH1}	V_{IH1}=0V Without pull down resistor	K00–K03, P00–P03	0		0.5	µA
High level input current (2)	I_{IH2}	V_{IH2}=0V With pull down resistor	K00–K03	5.0		20	µA
High level input current (3)	I_{IH3}	V_{IH3}=0V With pull down resistor	P00–P03, RESET	9.0		100	µA
Low level input current	I_{IL}	V_{IL}=V_{SS}	K00–K03, P00–P03, RESET, TEST	-0.5		0	µA
High level output current (1)	I_{OH1}	V_{OH1}=0.1•V_{SS}	R02, R03, P00–P03			-200	µA
High level output current (2)	I_{OH2}	V_{OH2}=0.1•V_{SS} (built-in protection resistance)	R00, R01			-200	µA
Low level output current (1)	I_{OL1}	V_{OL1}=0.9•V_{SS}	R02, R03, P00–P03	700			µA
Low level output current (2)	I_{OL2}	V_{OL2}=0.9•V_{SS} (built-in protection resistance)	R00, R01	700			µA
Common output current	I_{OH3}	V_{OH3}=-0.05V	COM0–COM3			-3	µA
	I_{OL3}	V_{OL3}=V_{L3}+0.05V		3			µA
Segment output current (during LCD output)	I_{OH4}	V_{OH4}=-0.05V	SEG0–SEG25			-3	µA
	I_{OL4}	V_{OL4}=V_{L3}+0.05V		3			µA
Segment output current (during DC output)	I_{OH5}	V_{OH5}=0.1•V_{SS}	SEG0–SEG25			-100	µA
	I_{OL5}	V_{OL5}=0.9•V_{SS}		130			µA

6.4 Analog Circuit Characteristics and Power Current Consumption

E0C6S37 (Normal Operating Mode)

Unless otherwise specified

V_{DD}=0 V, V_{SS}=-3.0 V, fosc=32.768 kHz (crystal oscillation), Ta=25°C, C_G=25 pF, V_{S1}, V_{L1}, V_{L2} and V_{L3} are internal voltages, and C1=C2=C3=C4=C5=0.1 µF

Item	Symbol	Condition		Min	Typ	Max	Unit
Internal voltage	V_{L1}	Connect 1MΩ load resistor between V_{DD} and V_{L1} (without panel load)		1/2•V_{L2} -0.1		1/2•V_{L2} ×0.9	V
	V_{L2}	Connect 1MΩ load resistor between V_{DD} and V_{L2} (without panel load)		-2.25	-2.10	-1.95	V
	V_{L3}	Connect 1MΩ load resistor between V_{DD} and V_{L3} (without panel load)		3/2•V_{L2} -0.1		3/2•V_{L2} ×0.9	V
SVD voltage	V_{SVD}			-2.55	-2.40	-2.25	V
SVD circuit response time	t_{SVD}					100	µs
Power current consumption	I_{OP}	During HALT	Without panel load		1.0	2.5	µA
		During execution *1			2.5	5.0	µA

*1 The SVD circuit is turned OFF.

E0C6S37 (Heavy Load Protection Mode)

Unless otherwise specified

V_{DD}=0 V, V_{SS}=-3.0 V, fosc=32.768 kHz (crystal oscillation), Ta=25°C, C_G=25 pF, V_{S1}, V_{L1}, V_{L2} and V_{L3} are internal voltages, and C1=C2=C3=C4=C5=0.1 µF

Item	Symbol	Condition		Min	Typ	Max	Unit
Internal voltage	V_{L1}	Connect 1MΩ load resistor between V_{DD} and V_{L1} (without panel load)		1/2•V_{L2} -0.1		1/2•V_{L2} ×0.85	V
	V_{L2}	Connect 1MΩ load resistor between V_{DD} and V_{L2} (without panel load)		-2.25	-2.10	-1.95	V
	V_{L3}	Connect 1MΩ load resistor between V_{DD} and V_{L3} (without panel load)		3/2•V_{L2} -0.1		3/2•V_{L2} ×0.85	V
SVD voltage	V_{SVD}			-2.55	-2.40	-2.25	V
SVD circuit response time	t_{SVD}					100	µs
Power current consumption	I_{OP}	During HALT	Without panel load		2.0	5.5	µA
		During execution *1			5.5	10.0	µA

*1 The SVD circuit is turned OFF.

E0C6SL37 (Normal Operating Mode)

Unless otherwise specified

VDD=0 V, VSS=-1.5 V, fosc=32.768 kHz (crystal oscillation), Ta=25°C, CG=25 pF, VS1, VL1, VL2 and VL3 are internal voltages, and C1=C2=C3=C4=C5=0.1 µF

Item	Symbol	Condition		Min	Typ	Max	Unit
Internal voltage	V_{L1}	Connect 1MΩ load resistor between V_{DD} and V_{L1} (without panel load)		-1.15	-1.05	-0.95	V
	V_{L2}	Connect 1MΩ load resistor between V_{DD} and V_{L2} (without panel load)		2•V_{L1} -0.1		2•V_{L1} × 0.9	V
	V_{L3}	Connect 1MΩ load resistor between V_{DD} and V_{L3} (without panel load)		3•V_{L1} -0.1		3•V_{L1} × 0.9	V
SVD voltage	V_{SVD}			-1.30	-1.20	-1.10	V
SVD circuit response time	t_{SVD}					100	µs
Power current consumption	I_{OP}	During HALT	Without panel load		1.0	2.5	µA
		During execution *1			2.5	5.0	µA

*1 The SVD circuit is turned OFF.

E0C6SL37 (Heavy Load Protection Mode)

Unless otherwise specified

VDD=0 V, VSS=-1.5 V, fosc=32.768 kHz (crystal oscillation), Ta=25°C, CG=25 pF, VS1, VL1, VL2 and VL3 are internal voltages, and C1=C2=C3=C4=C5=0.1 µF

Item	Symbol	Condition		Min	Typ	Max	Unit
Internal voltage	V_{L1}	Connect 1MΩ load resistor between V_{DD} and V_{L1} (without panel load)		-1.15	-1.05	-0.95	V
	V_{L2}	Connect 1MΩ load resistor between V_{DD} and V_{L2} (without panel load)		2•V_{L1} -0.1		2•V_{L1} × 0.85	V
	V_{L3}	Connect 1MΩ load resistor between V_{DD} and V_{L3} (without panel load)		3•V_{L1} -0.1		3•V_{L1} × 0.85	V
SVD voltage	V_{SVD}			-1.30	-1.20	-1.10	V
SVD circuit response time	t_{SVD}					100	µs
Power current consumption	I_{OP}	During HALT	Without panel load		2.0	5.5	µA
		During execution *1			5.5	10.0	µA

*1 The SVD circuit is turned OFF.

E0C6SB37 (Normal Operating Mode)

Unless otherwise specified

V_{DD}=0 V, V_{SS}=-3.0 V, fosc=32.768 kHz (crystal oscillation), Ta=25°C, C_G=25 pF,
V_{S1}, V_{L1}, V_{L2} and V_{L3} are internal voltages, and C1=C2=C3=C4=C5=0.1 µF

Item	Symbol	Condition		Min	Typ	Max	Unit
Internal voltage	V_{L1}	Connect 1MΩ load resistor between V_{DD} and V_{L1} (without panel load)		-1.15	-1.05	-0.95	V
	V_{L2}	Connect 1MΩ load resistor between V_{DD} and V_{L2} (without panel load)		2•V_{L1} -0.1		2•V_{L1} ×0.9	V
	V_{L3}	Connect 1MΩ load resistor between V_{DD} and V_{L3} (without panel load)		3•V_{L1} -0.1		3•V_{L1} ×0.9	V
SVD voltage	V_{SVD}			-1.30	-1.20	-1.10	V
SVD circuit response time	t_{SVD}					100	µs
Power current consumption	I_{OP}	During HALT	Without panel load		1.0	2.5	µA
		During execution *1			2.5	5.0	µA

*1 The SVD circuit is turned OFF.

E0C6SB37 (Heavy Load Protection Mode)

Unless otherwise specified

V_{DD}=0 V, V_{SS}=-3.0 V, fosc=32.768 kHz (crystal oscillation), Ta=25°C, C_G=25 pF,
V_{S1}, V_{L1}, V_{L2} and V_{L3} are internal voltages, and C1=C2=C3=C4=C5=0.1 µF

Item	Symbol	Condition		Min	Typ	Max	Unit
Internal voltage	V_{L1}	Connect 1MΩ load resistor between V_{DD} and V_{L1} (without panel load)		-1.15	-1.05	-0.95	V
	V_{L2}	Connect 1MΩ load resistor between V_{DD} and V_{L2} (without panel load)		2•V_{L1} -0.1		2•V_{L1} ×0.85	V
	V_{L3}	Connect 1MΩ load resistor between V_{DD} and V_{L3} (without panel load)		3•V_{L1} -0.1		3•V_{L1} ×0.85	V
SVD voltage	V_{SVD}			-1.30	-1.20	-1.10	V
SVD circuit response time	t_{SVD}					100	µs
Power current consumption	I_{OP}	During HALT	Without panel load		2.0	5.5	µA
		During execution *1			5.5	10.0	µA

*1 The SVD circuit is turned OFF.

E0C6S37 (CR, Normal Operating Mode)

Unless otherwise specified

V_{DD}=0 V, V_{SS}=-3.0 V, fosc=65 kHz, Ta=25°C, C_G=25 pF, V_{S1}, V_{L1}, V_{L2} and V_{L3} are internal voltages, and C1=C2=C3=C4=C5=0.1 µF, Recommended external resistance for CR oscillation=470 kΩ

Item	Symbol	Condition		Min	Typ	Max	Unit
Internal voltage	V_{L1}	Connect 1MΩ load resistor between V_{DD} and V_{L1} (without panel load)		1/2•V_{L2} -0.1		1/2•V_{L2} × 0.9	V
	V_{L2}	Connect 1MΩ load resistor between V_{DD} and V_{L2} (without panel load)		-2.25	-2.10	-1.95	V
	V_{L3}	Connect 1MΩ load resistor between V_{DD} and V_{L3} (without panel load)		3/2•V_{L2} -0.1		3/2•V_{L2} × 0.9	V
SVD voltage	V_{SVD}			-2.55	-2.40	-2.25	V
SVD circuit response time	t_{SVD}					100	µs
Power current consumption	I_{OP}	During HALT	Without panel load		8.0	15.0	µA
		During execution *1			15.0	20.0	µA

*1 The SVD circuit is turned OFF.

E0C6S37 (CR, Heavy Load Protection Mode)

Unless otherwise specified

V_{DD}=0 V, V_{SS}=-3.0 V, fosc=65 kHz, Ta=25°C, C_G=25 pF, V_{S1}, V_{L1}, V_{L2} and V_{L3} are internal voltages, and C1=C2=C3=C4=C5=0.1 µF, Recommended external resistance for CR oscillation=470 kΩ

Item	Symbol	Condition		Min	Typ	Max	Unit
Internal voltage	V_{L1}	Connect 1MΩ load resistor between V_{DD} and V_{L1} (without panel load)		1/2•V_{L2} -0.1		1/2•V_{L2} × 0.85	V
	V_{L2}	Connect 1MΩ load resistor between V_{DD} and V_{L2} (without panel load)		-2.25	-2.10	-1.95	V
	V_{L3}	Connect 1MΩ load resistor between V_{DD} and V_{L3} (without panel load)		3/2•V_{L1} -0.1		3/2•V_{L1} × 0.85	V
SVD voltage	V_{SVD}			-2.55	-2.40	-2.25	V
SVD circuit response time	t_{SVD}					100	µs
Power current consumption	I_{OP}	During HALT	Without panel load		16.0	30.0	µA
		During execution *1			30.0	40.0	µA

*1 The SVD circuit is turned OFF.

E0C6SL37 (CR, Normal Operating Mode)

Unless otherwise specified

VDD=0 V, VSS=-1.5 V, fosc=65 kHz, Ta=25°C, CG=25 pF, VS1, VL1, VL2 and VL3 are internal voltages, and C1=C2=C3=C4=C5=0.1 µF, Recommended external resistance for CR oscillation=470 kΩ

Item	Symbol	Condition		Min	Typ	Max	Unit
Internal voltage	V_{L1}	Connect 1MΩ load resistor between V_{DD} and V_{L1} (without panel load)		-1.15	-1.05	-0.95	V
	V_{L2}	Connect 1MΩ load resistor between V_{DD} and V_{L2} (without panel load)		2•V_{L1} -0.1		2•V_{L1} ×0.9	V
	V_{L3}	Connect 1MΩ load resistor between V_{DD} and V_{L3} (without panel load)		3•V_{L1} -0.1		3•V_{L1} ×0.9	V
SVD voltage	V_{SVD}			-1.30	-1.20	-1.10	V
SVD circuit response time	t_{SVD}					100	µs
Power current consumption	I_{OP}	During HALT	Without panel load		8.0	15.0	µA
		During execution *1			15.0	20.0	µA

*1 The SVD circuit is turned OFF.

E0C6SL37 (CR, Heavy Load Protection Mode)

Unless otherwise specified

VDD=0 V, VSS=-1.5 V, fosc=65 kHz, Ta=25°C, CG=25 pF, VS1, VL1, VL2 and VL3 are internal voltages, and C1=C2=C3=C4=C5=0.1 µF, Recommended external resistance for CR oscillation=470 kΩ

Item	Symbol	Condition		Min	Typ	Max	Unit
Internal voltage	V_{L1}	Connect 1MΩ load resistor between V_{DD} and V_{L1} (without panel load)		-1.15	-1.05	-0.95	V
	V_{L2}	Connect 1MΩ load resistor between V_{DD} and V_{L2} (without panel load)		2•V_{L1} -0.1		2•V_{L1} ×0.85	V
	V_{L3}	Connect 1MΩ load resistor between V_{DD} and V_{L3} (without panel load)		3•V_{L1} -0.1		3•V_{L1} ×0.85	V
SVD voltage	V_{SVD}			-1.30	-1.20	-1.10	V
SVD circuit response time	t_{SVD}					100	µs
Power current consumption	I_{OP}	During HALT	Without panel load		16.0	30.0	µA
		During execution *1			30.0	40.0	µA

*1 The SVD circuit is turned OFF.

E0C6SB37 (CR, Normal Operating Mode)

Unless otherwise specified

VDD=0 V, VSS=-3.0 V, fosc=65 kHz, Ta=25°C, CG=25 pF, VS1, VL1, VL2 and VL3 are internal voltages, and C1=C2=C3=C4=C5=0.1 µF, Recommended external resistance for CR oscillation=470 kΩ

Item	Symbol	Condition		Min	Typ	Max	Unit
Internal voltage	V_{L1}	Connect 1MΩ load resistor between V_{DD} and V_{L1} (without panel load)		-1.15	-1.05	-0.95	V
	V_{L2}	Connect 1MΩ load resistor between V_{DD} and V_{L2} (without panel load)		2•V_{L1} -0.1		2•V_{L1} ×0.9	V
	V_{L3}	Connect 1MΩ load resistor between V_{DD} and V_{L3} (without panel load)		3•V_{L1} -0.1		3•V_{L1} ×0.9	V
SVD voltage	V_{SVD}			-1.30	-1.20	-1.10	V
SVD circuit response time	t_{SVD}					100	µs
Power current consumption	I_{OP}	During HALT	Without panel load		8.0	15.0	µA
		During execution *1			15.0	20.0	µA

*1 The SVD circuit is turned OFF.

E0C6SB37 (CR, Heavy Load Protection Mode)

Unless otherwise specified

VDD=0 V, VSS=-3.0 V, fosc=65 kHz, Ta=25°C, CG=25 pF, VS1, VL1, VL2 and VL3 are internal voltages, and C1=C2=C3=C4=C5=0.1 µF, Recommended external resistance for CR oscillation=470 kΩ

Item	Symbol	Condition		Min	Typ	Max	Unit
Internal voltage	V_{L1}	Connect 1MΩ load resistor between V_{DD} and V_{L1} (without panel load)		-1.15	-1.05	-0.95	V
	V_{L2}	Connect 1MΩ load resistor between V_{DD} and V_{L2} (without panel load)		2•V_{L1} -0.1		2•V_{L1} ×0.85	V
	V_{L3}	Connect 1MΩ load resistor between V_{DD} and V_{L3} (without panel load)		3•V_{L1} -0.1		3•V_{L1} ×0.85	V
SVD voltage	V_{SVD}			-1.30	-1.20	-1.10	V
SVD circuit response time	t_{SVD}					100	µs
Power current consumption	I_{OP}	During HALT	Without panel load		16.0	30.0	µA
		During execution *1			30.0	40.0	µA

*1 The SVD circuit is turned OFF.

6.5 Oscillation Characteristics

Oscillation characteristics will vary according to different conditions. Use the following characteristics are as reference values.

E0C6S37

Unless otherwise specified

VDD=0 V, VSS=-3.0 V, Crystal : C-002R (CI=35 kΩ), CG=25 pF, CD=built-in, Ta=25°C

Item	Symbol	Condition	Min	Typ	Max	Unit
Oscillation start voltage	Vsta (Vss)	tsta≤5sec	-1.8			V
Oscillation stop voltage	Vstp (Vss)	tstp≤10sec	-1.8			V
Built-in capacity (drain)	CD	Including the parasitic capacity inside the IC		20		pF
Frequency voltage deviation	f/V	Vss=-1.8 to -3.6V			5	ppm
Frequency IC deviation	f/IC		-10		10	ppm
Frequency adjustment range	f/CG	CG=5–25pF	40			ppm
Higher harmonic oscillation start voltage	Vhho (Vss)	CG=5pF			-3.6	V
Allowable leak resistance	Rleak	Between OSC1 and VDD	200			MΩ

E0C6SL37

Unless otherwise specified

VDD=0 V, VSS=-1.5 V, Crystal : C-002R (CI=35 kΩ), CG=25 pF, CD=built-in, Ta=25°C

Item	Symbol	Condition	Min	Typ	Max	Unit
Oscillation start voltage	Vsta (Vss)	tsta≤5sec	-1.1			V
Oscillation stop voltage	Vstp (Vss)	tstp≤10sec	-1.1 (-0.9)*1			V
Built-in capacity (drain)	CD	Including the parasitic capacity inside the IC		20		pF
Frequency voltage deviation	f/V	Vss=-1.1 to -2.0V (-0.9)*1			5	ppm
Frequency IC deviation	f/IC		-10		10	ppm
Frequency adjustment range	f/CG	CG=5–25pF	40			ppm
Higher harmonic oscillation start voltage	Vhho (Vss)	CG=5pF			-2.0	V
Allowable leak resistance	Rleak	Between OSC1 and VDD	200			MΩ

*1 Items enclosed in parentheses ( ) are those used when operating at heavy load protection mode.

E0C6SB37

Unless otherwise specified

V_{DD}=0 V, V_{SS}=-3.0 V, Crystal : C-002R (CI=35 kΩ), C_G=25 pF, C_D=built-in, Ta=25°C

Item	Symbol	Condition	Min	Typ	Max	Unit
Oscillation start voltage	Vsta (Vss)	tsta≤5sec	-1.1			V
Oscillation stop voltage	Vstp (Vss)	tstp≤10sec	-1.1 (-0.9)*1			V
Built-in capacity (drain)	C_D	Including the parasitic capacity inside the IC		20		pF
Frequency voltage deviation	f/V	Vss=-1.1 to -3.6V (-0.9)*1			5	ppm
Frequency IC deviation	f/I_C		-10		10	ppm
Frequency adjustment range	f/C_G	C_G=5–25pF	40			ppm
Higher harmonic oscillation start voltage	V_{hho} (Vss)	C_G=5pF			-3.6	V
Allowable leak resistance	R_{leak}	Between OSC1 and V_{DD}	200			MΩ

*1 Items enclosed in parentheses ( ) are those used when operating at heavy load protection mode.

E0C6S37 (CR)

Unless otherwise specified

V_{DD}=0 V, V_{SS}=-3.0 V, R_{CR}=470 kΩ, Ta=25°C

Item	Symbol	Condition	Min	Typ	Max	Unit
Oscillation frequency dispersion	fosc		-20	65kHz	20	%
Oscillation start voltage	Vsta		-1.8			V
Oscillation start time	tsta	Vss=-1.8 to -3.6V		3		ms
Oscillation stop voltage	Vstp		-1.8			V

E0C6SL37 (CR)

Unless otherwise specified

V_{DD}=0 V, V_{SS}=-1.5 V, R_{CR}=470 kΩ, Ta=25°C

Item	Symbol	Condition	Min	Typ	Max	Unit
Oscillation frequency dispersion	fosc		-20	65kHz	20	%
Oscillation start voltage	Vsta		-1.1			V
Oscillation start time	tsta	Vss=-1.1 to -2.0V		3		ms
Oscillation stop voltage	Vstp		-1.1			V

E0C6SB37 (CR)

Unless otherwise specified

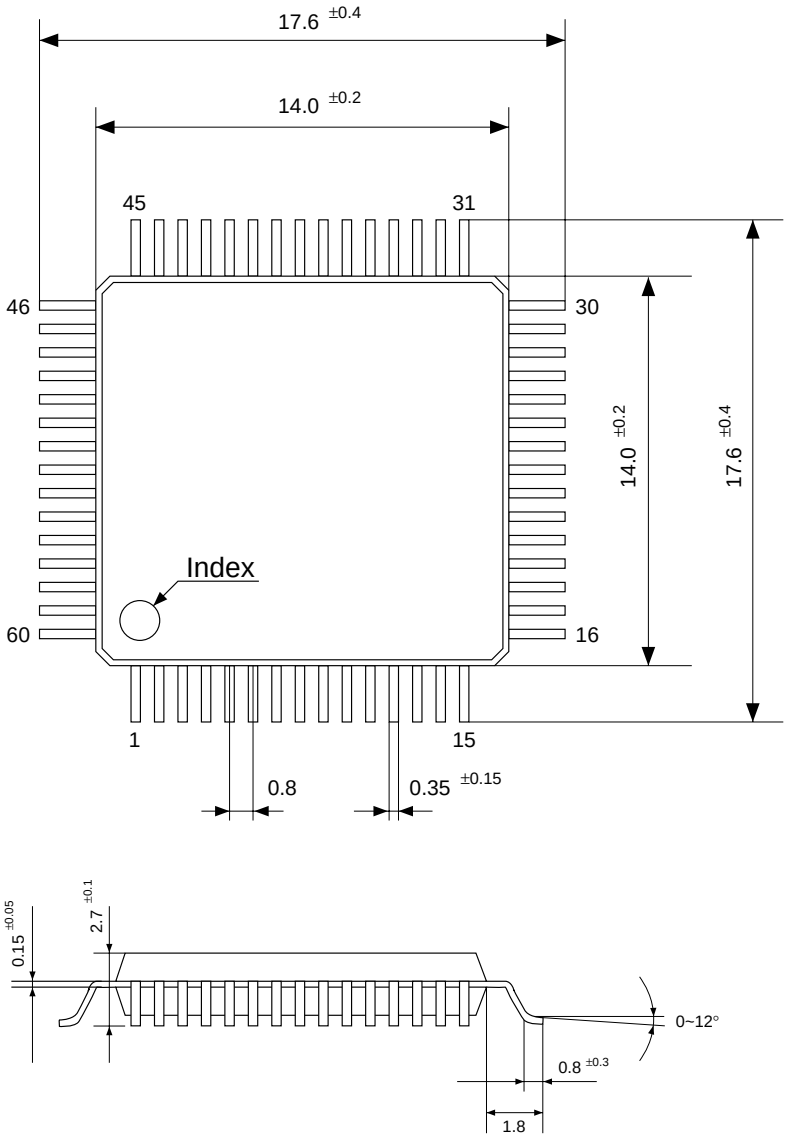
V_{DD}=0 V, V_{SS}=-3.0 V, R_{CR}=470 kΩ, Ta=25°C

Item	Symbol	Condition	Min	Typ	Max	Unit
Oscillation frequency dispersion	fosc		-20	65kHz	20	%
Oscillation start voltage	Vsta		-1.1			V
Oscillation start time	tsta	Vss=-1.1 to -3.6V		3		ms
Oscillation stop voltage	Vstp		-1.1			V

CHAPTER 7 PACKAGE

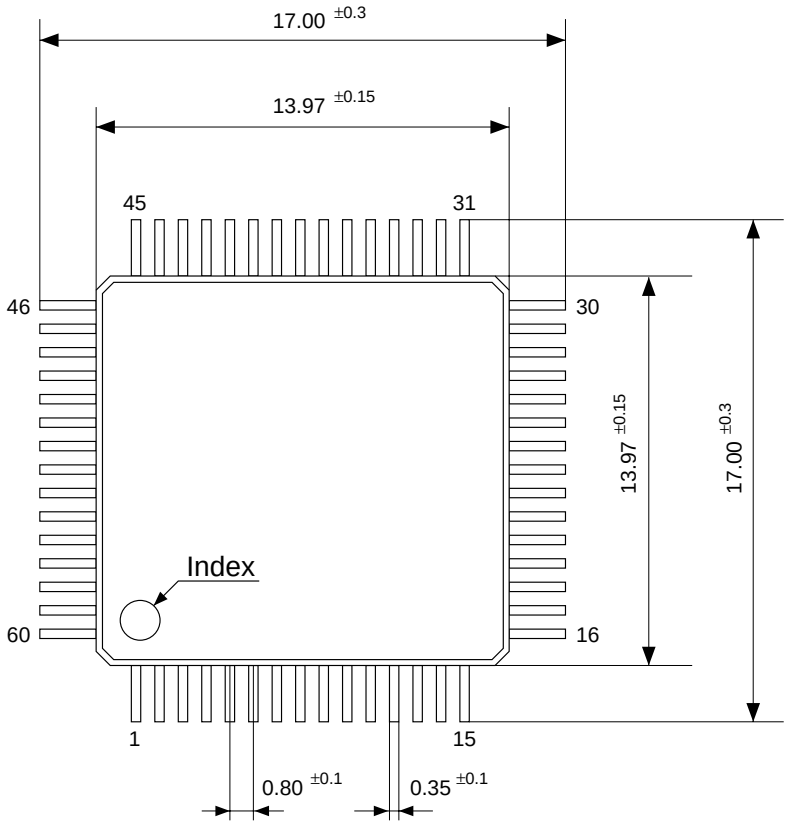
7.1 Plastic Package

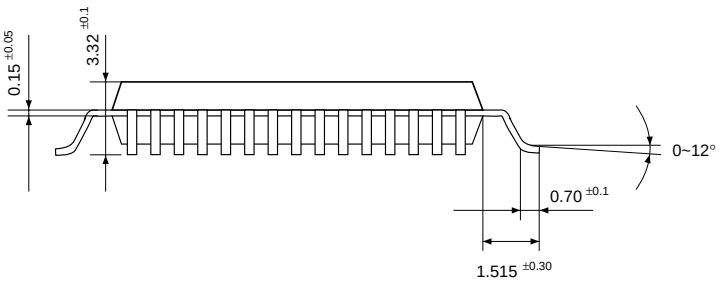
QFP6-60pin



7.2 Ceramic Package for Test Samples

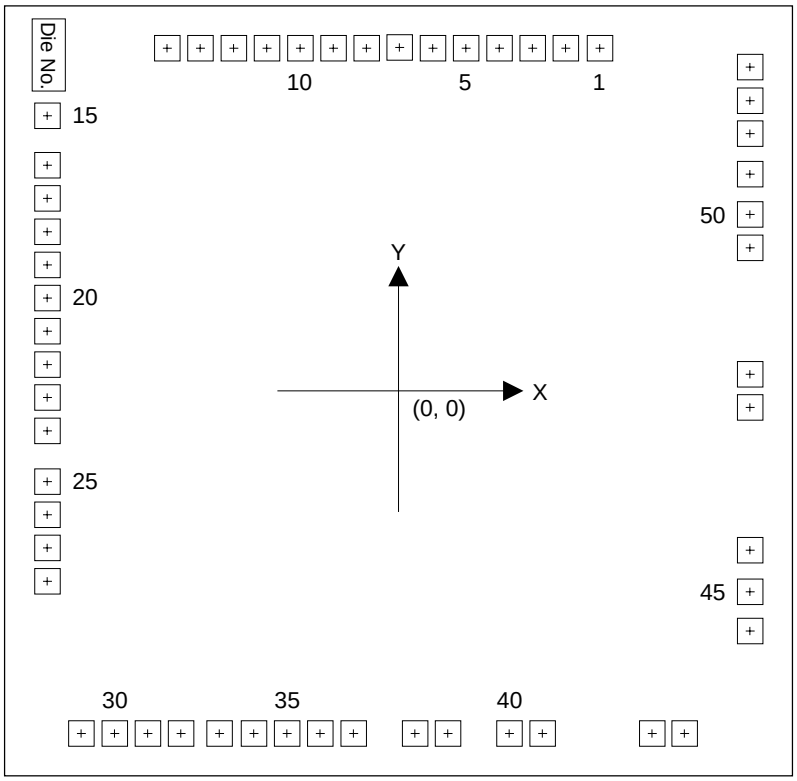
QFP6-60pin





CHAPTER 8 PAD LAYOUT

8.1 Diagram of Pad Layout



Chip size: 3,090 µm (X) x 3,020 µm (Y)

8.2 Pad Coordinates

Pad No	Pad Name	X	Y	Pad No	Pad Name	X	Y
1	COM3	789	1,344	28	SEG25	-1,378	-747
2	SEG0	655	1,344	29	P00	-1,245	-1,344
3	SEG1	525	1,344	30	P01	-1,114	-1,344
4	SEG2	395	1,344	31	P02	-984	-1,344
5	SEG3	264	1,344	32	P03	-854	-1,344
6	SEG4	134	1,344	33	RESET	-703	-1,344
7	SEG5	3	1,344	34	K00	-568	-1,344
8	SEG6	-126	1,344	35	K01	-438	-1,344
9	SEG7	-256	1,344	36	K02	-308	-1,344
10	SEG8	-386	1,344	37	K03	-177	-1,344
11	SEG9	-517	1,344	38	R00	64	-1,344
12	SEG10	-647	1,344	39	R01	193	-1,344
13	SEG11	-778	1,344	40	R02	434	-1,344
14	SEG12	-908	1,344	41	R03	564	-1,344
15	TEST	-1,378	1,079	42	V_{SS}	994	-1,344
16	SEG13	-1,378	885	43	V_{DD}	1,121	-1,344
17	SEG14	-1,378	755	44	OSC1	1,378	-942
18	SEG15	-1,378	624	45	OSC2	1,378	-789
19	SEG16	-1,378	494	46	V_{S1}	1,378	-625
20	SEG17	-1,378	364	47	CA	1,378	-65
21	SEG18	-1,378	234	48	CB	1,378	65
22	SEG19	-1,378	103	49	V_{L1}	1,378	561
23	SEG20	-1,378	-26	50	V_{L2}	1,378	692
24	SEG21	-1,378	-157	51	V_{L3}	1,378	850
25	SEG22	-1,378	-356	52	COM0	1,378	1,009
26	SEG23	-1,378	-486	53	COM1	1,378	1,138
27	SEG24	-1,378	-616	54	COM2	1,378	1,270

(Unit: µm)

II. E0C6S37 Technical Software

CONTENTS

CHAPTER 1 CONFIGURATION

1.1 E0C6S37 Block Diagram

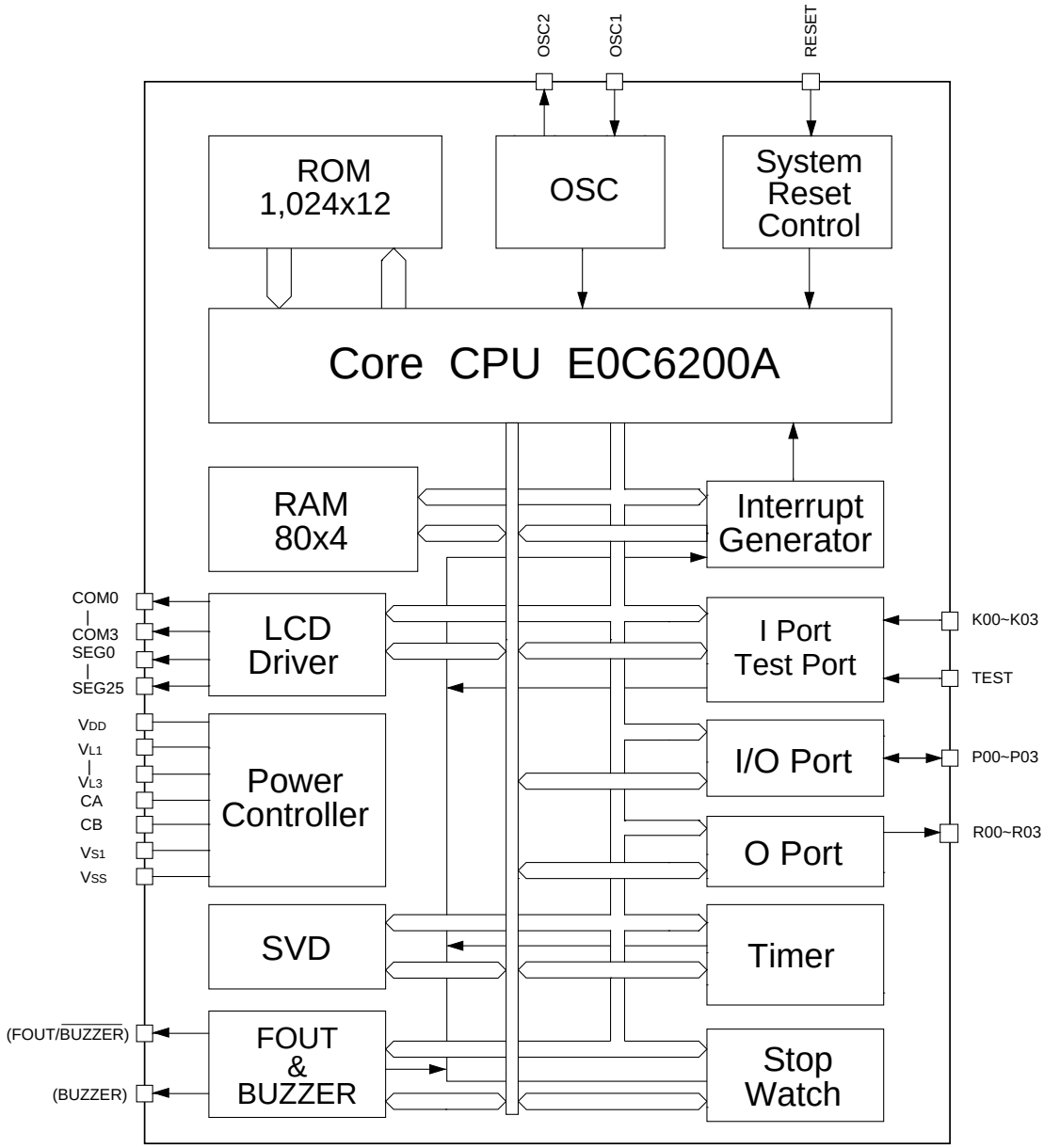


Fig. 1.1.1
E0C6S37 block diagram

1.2 ROM Map

The E0C6S37 has a built-in mask ROM with a capacity of 1,024 steps × 12 bits for program storage. The configuration of the ROM is shown in Figure 1.2.1.

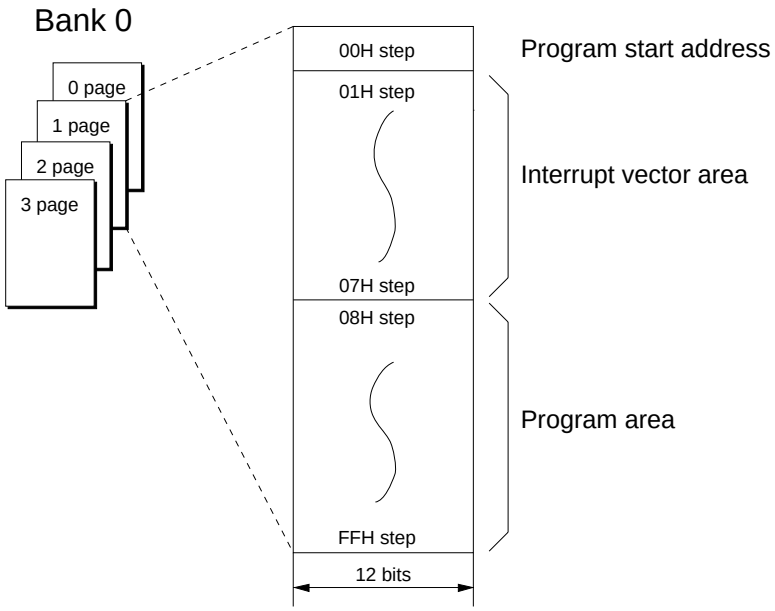


Fig. 1.2.1
Configuration of built-in ROM

1.3 Interrupt Vectors

When an interrupt request is received by the CPU, the CPU initiates the following interrupt processing after completing the instruction being executed.

(1) The address of the next instruction to be executed (the value of the program counter) is saved on the stack (RAM).

(2) The interrupt vector address corresponding to the interrupt request is loaded into the program counter.

(3) The branch instruction written in the vector is executed to branch to the software interrupt processing routine.

Note Steps 1 and 2 require 12 cycles of the CPU system clock.

The interrupt vectors are shown in Table 1.3.1.

Table 1.3.1
Interrupt requests and vectors

Page	Step	Interrupt Vector
1	00H	Initial reset
	01H	Clock timer interrupt
	02H	Stopwatch interrupt
	03H	Clock timer interrupt and stopwatch interrupt
	04H	Input (K00–K03) interrupt
	05H	Input interrupt and clock timer interrupt
	06H	Input interrupt and stopwatch interrupt
	07H	Generation of all interrupt

Addesses (start address of interrupt processing routines) to jump to are written into the addresses available for interrupt vector allocation.

1.4 Data Memory Map

The E0C6S37 built-in RAM has 80 words of data memory, 32 words of display memory for the LCD, and I/O memory for controlling the peripheral circuit. When writing programs, note the following:

(1) Since the stack area is in the data memory area, take care not to overwrite the stack with data. Subroutine calls or interrupts use 3 words on the stack.

(2) Data memory addresses 000H–00FH are memory register areas that are addressed with register pointer RP.

Address Page	Low / High	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	0	M0	M1	M2	M3	M4	M5	M6	M7	M8	M9	MA	MB	MC	MD	ME	MF
	1	RAM (80 words x 4 bits) R/W															
	2																
	3																
	4																
	5	Unused area															
	6																
	7																
	8																
	9	Display memory															
	A																
	B	Unused area															
	C																
	D																
	E	I/O memory															
	F																

Fig. 1.4.1
Data memory map

Note *Memory is not mounted in unused area within the memory map and in memory area not indicated in this chapter. For this reason, normal operation cannot be assured for programs that have been prepared with access to these areas.*

Table 1.4.1(a) I/O memory map 1

Address	Register D3	D2	D1	D0	Name	SR *1	1	0	Comment
0E0H	K03	K02	K01	K00	K03	– *2	High	Low	Input port (K00–K03)
	R				K02	– *2	High	Low	
					K01	– *2	High	Low	
					K00	– *2	High	Low	
0E2H	SWL3	SWL2	SWL1	SWL0	SWL3	0			MSB
	R				SWL2	0			Stopwatch timer 1/100 sec (BCD)
					SWL1	0			
					SWL0	0			LSB
0E3H	SWH3	SWH2	SWH1	SWH0	SWH3	0			MSB
	R				SWH2	0			Stopwatch timer 1/10 sec (BCD)
					SWH1	0			
					SWH0	0			LSB
0E4H	TM3	TM2	TM1	TM0	TM3	–	High	Low	Timer data (clock timer 2 Hz)
	R				TM2	–	High	Low	Timer data (clock timer 4 Hz)
					TM1	–	High	Low	Timer data (clock timer 8 Hz)
					TM0	–	High	Low	Timer data (clock timer 16 Hz)

*1 Initial value following initial reset
*2 Not set in the circuit
*3 Undefined
*4 Reset (0) immediately after being read
*5 Always 0 when being read
*6 Refer to main manual

Table 1.4.1(b) I/O memory map 2

Address	Register								Comment
	D3	D2	D1	D0	Name	SR *1	1	0	
0E8H	EIK03	EIK02	EIK01	EIK00	EIK03	0	Enable	Mask	Interrupt mask register (K03)
	R/W				EIK02	0	Enable	Mask	Interrupt mask register (K02)
					EIK01	0	Enable	Mask	Interrupt mask register (K01)
					EIK00	0	Enable	Mask	Interrupt mask register (K00)
0EAH	0	0	EISW1	EISW0	0 *5				
	R		R/W		0 *5				
					EISW1	0	Enable	Mask	Interrupt mask register (stopwatch 1 Hz)
					EISW0	0	Enable	Mask	Interrupt mask register (stopwatch 10 Hz)
0EBH	0	EIT2	EIT8	EIT32	0 *5				
	R	R/W			EIT2	0	Enable	Mask	Interrupt mask register (clock timer 2 Hz)
					EIT8	0	Enable	Mask	Interrupt mask register (clock timer 8 Hz)
					EIT32	0	Enable	Mask	Interrupt mask register (clock timer 32 Hz)
0EDH	0	0	0	IK0	0 *5				
	R				0 *5				
					0 *5				
					IK0 *4	0	Yes	No	Interrupt factor flag (K00–K03)

*1 Initial value following initial reset
*2 Not set in the circuit
*3 Undefined
*4 Reset (0) immediately after being read
*5 Always 0 when being read
*6 Refer to main manual

Table 1.4.1(c) I/O memory map 3

Address	Register								Comment
	D3	D2	D1	D0	Name	SR *1	1	0	
0EEH	0	0	ISW1	ISW0	0 *5				
	R				0 *5				
					ISW1 *4	0	Yes	No	Interrupt factor flag (stopwatch 1 Hz)
					ISW0 *4	0	Yes	No	Interrupt factor flag (stopwatch 10 Hz)
0EFH	0	IT2	IT8	IT32	0 *5				
	R				IT2 *4	0	Yes	No	Interrupt factor flag (clock timer 2 Hz)
					IT8 *4	0	Yes	No	Interrupt factor flag (clock timer 8 Hz)
					IT32 *4	0	Yes	No	Interrupt factor flag (clock timer 32 Hz)
0F3H	R03	R02	R01 / BUZZER	R00 / FOUT	R03	0	High	Low	R03 output port data
	R/W				R02	0	High	Low	R02 output port data
					R01	0	High	Low	R01 output port data
					BUZZER	0	ON	OFF	Buzzer ON/OFF control register
					R00	0	High	Low	R00 output port data
					FOUT	0	ON	OFF	Frequency output ON/OFF control register
0F6H	P03	P02	P01	P00	P03	– *2	High	Low	I/O port (P00–P03)
	R/W				P02	– *2	High	Low	
					P01	– *2	High	Low	
					P00	– *2	High	Low	

*1 Initial value following initial reset

*2 Not set in the circuit

*3 Undefined

*4 Reset (0) immediately after being read

*5 Always 0 when being read

*6 Refer to main manual

Table 1.4.1(d) I/O memory map 4

Address	Register								Comment
	D3	D2	D1	D0	Name	SR *1	1	0	
0F9H	0	TMRST	SWRUN	SWRST	0 *5				
	R	W	R/W	W	TMRST	Reset	Reset	–	Clock timer reset
					SWRUN	0	Run	Stop	Stopwatch timer RUN/STOP
					SWRST *5	Reset	Reset	–	Stopwatch timer reset
0FAH	HLMOD	0	SVDDT	SVDON	HLMOD	0	Heavy load	Normal load	Heavy load protection mode register
	R/W	R		R/W	0 *5				
					SVDDT	0	Supply voltage low	Supply voltage normal	Supply voltage detection data
					SVDON	0	ON	OFF	Supply voltage detection ON/OFF
0FBH	CSDC	0	0	0	CSDC	0	Static	Dynamic	LCD drive switch
	R/W	R			0 *5				
					0 *5				
					0 *5				
0FCH	0	0	0	IOC	0 *5				
	R			R/W	0 *5				
					0 *5				
					IOC	0	Output	Input	I/O port P00–P03 Input/Output

*1 Initial value following initial reset
*2 Not set in the circuit
*3 Undefined
*4 Reset (0) immediately after being read
*5 Always 0 when being read
*6 Refer to main manual

Table 1.4.1(e) I/O memory map 5

Address	Register								Comment
	D3	D2	D1	D0	Name	SR *1	1	0	
0FDH	XBZR	0	XFOUT1	XFOUT0	XBZR	0	2 kHz	4 kHz	Buzzer frequency control
	R/W	R	R/W		0 *5				
					XFOUT1	0	High	Low	FOUT frequency control: XFOUT1(0), XFOUT0(0) -> F1 XFOUT1(0), XFOUT0(1) -> F2 XFOUT1(1), XFOUT0(0) -> F3 XFOUT1(1), XFOUT0(1) -> F4
					XFOUT0	0	High	Low	

*1 Initial value following initial reset

*2 Not set in the circuit

*3 Undefined

*4 Reset (0) immediately after being read

*5 Always 0 when being read

*6 Refer to main manual

CHAPTER 2 INITIAL RESET

2.1 Internal Register Status on Initial Reset

Following an initial reset, the internal registers and internal data memory area are initialized to the values shown in Tables 2.1.1 and 2.1.2.

Table 2.1.1
Initial values of internal registers

Internal Register		Bit Length	Initial Value Following Reset
Program counter step	PCS	8	00H
Program counter page	PCP	4	1H
New page pointer	NPP	4	1H
Stack pointer	SP	8	Undefined
Index register	X	8	Undefined
Index register	Y	8	Undefined
Register pointer	RP	4	Undefined
General register	A	4	Undefined
General register	B	4	Undefined
Interrupt flag	I	1	0
Decimal flag	D	1	0
Zero flag	Z	1	Undefined
Carry flag	C	1	Undefined

Table 2.1.2
Initial values of internal data memory area

Internal Data Memory Area	Bit Length	Initial Value Following Reset	Address
RAM data	4 × 80	Undefined	000H–05FH
Display memory	4 × 26	Undefined	090H–0AFH
Internal I/O register	See Tables 1.4.1(a)–1.4.1(e)		0E0H–0FDH

After an initial reset, the program counter page (PCP) is initialized to 1H, and the program counter step (PCS), to 00H. This is why the program is executed from step 00H of the first page.

The initial values of some internal registers and internal data memory area locations are undefined after a reset. Set them as necessary to the proper initial values in the program.

The peripheral I/O functions (memory-mapped I/O) are assigned to internal data memory area addresses 0E0H to 0FDH. Each address represents a 4-bit internal I/O register, allowing access to the peripheral functions in 1-word (4-bit) read/write units.

2.2 Initialize Program Example

The following is a program that clears the RAM and LCD, resets the flags, registers, timer, and stopwatch timer, and sets the stack pointer immediately after resetting the system.

```
Label   Mnemonic/operand        Comment
        ORG     100H
        JP      INIT            ;Jump to "INIT"
;
        ORG     110H
INIT    RST     F,0011B         ;Interrupt mask, decimal
                                ;adjustment off
;
        LD      X,0             ;┐
RAMCLR  LDPX    MX,0            ;│
        CP      XH,5H           ;│ Clear RAM (00H–4FH)
        JP      NZ,RAMCLR       ;│
        LD      X,90H           ;┘
LCDCLR  LDPX    MX,0            ;┐
        CP      XM,0BH          ;│ Clear LCD (90H–AFH)
        JP      NZ,LCDCLR       ;┘
;
        LD      A,0             ;┐
        LD      B,4             ;│
        LD      SPL,A           ;│ Set stack pointer to 40H
        LD      SPH,B           ;┘
;
        LD      X,0F9H          ;┐ Reset timer and stopwatch
        OR      MX,0101B        ;┘ timer
;
        LD      X,0EBH          ;┐
        OR      MX,0111B        ;┘ Enable timer interrupt
;
        LD      X,0EBH          ;┐ Enable input interrupt
        OR      MX,1111B        ;┘ (K03–K00)
```

```
;
        LD      X,0             ;┐
        LD      Y,0             ;
        LD      A,0             ;  Reset register flags
        LD      B,0             ;
        RST     F,0             ;┘
        EI                      ;Enable interrupt
```

The above program is a basic initialization program for the E0C6S37. The setting data are all initialized as shown in Table 2.1.1 by executing this program. When using this program, add setting items necessary for each specific application. (Figure 2.2.1 is the flow chart for this program.)

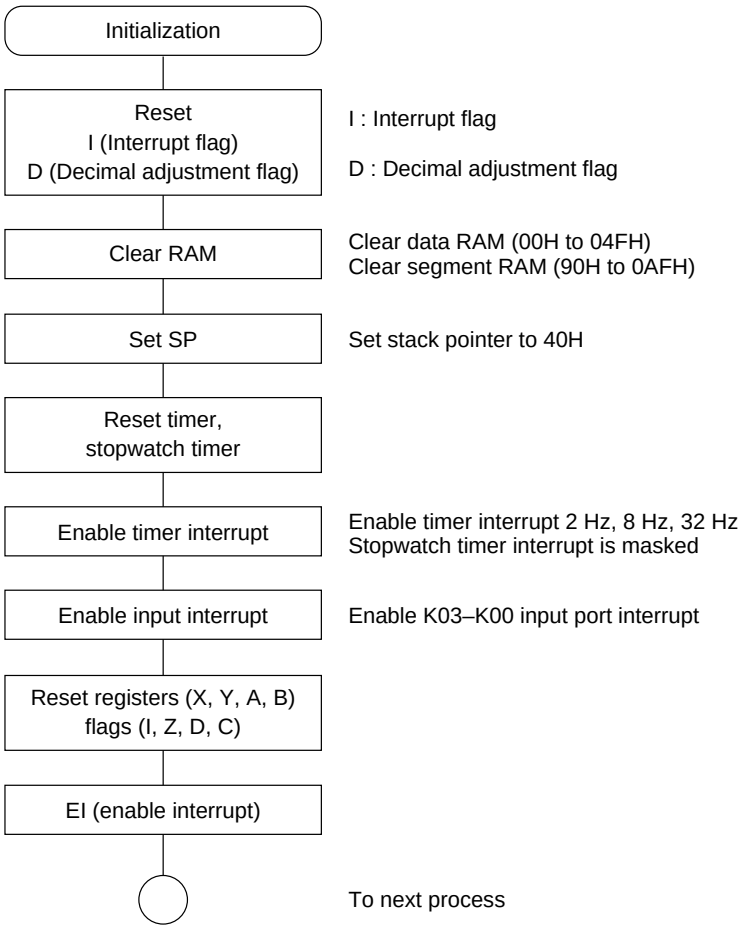


Fig. 2.2.1
Flow chart of the initialization program

CHAPTER 3 PERIPHERAL CIRCUITS

Details on how to control the E0C6S37 peripheral circuit is given in this chapter.

3.1 Input Port

Input port memory map

Table 3.1.1 I/O memory map

Address	Register D3	D2	D1	D0	Name	SR *1	1	0	Comment
0E0H	K03	K02	K01	K00	K03	– *2	High	Low	Input port (K00–K03)
	R				K02	– *2	High	Low	
					K01	– *2	High	Low	
					K00	– *2	High	Low	
0E8H	EIK03	EIK02	EIK01	EIK00	EIK03	0	Enable	Mask	Interrupt mask register (K03)
	R/W				EIK02	0	Enable	Mask	Interrupt mask register (K02)
					EIK01	0	Enable	Mask	Interrupt mask register (K01)
					EIK00	0	Enable	Mask	Interrupt mask register (K00)
0EDH	0	0	0	IK0	0 *5				
	R				0 *5				
					0 *5				
					IK0 *4	0	Yes	No	Interrupt factor flag (K00–K03)

*1 Initial value following initial reset
*2 Not set in the circuit
*3 Undefined
*4 Reset (0) immediately after being read
*5 Always 0 when being read
*6 Refer to main manual

Control of the input port

The E0C6S37 has one 4-bit input port (K00–K03). Input port data can be read as a 4-bit unit (K00–K03).

The state of the input ports can be obtained by reading the data (bits D3, D2, D1, D0) of address 0E0H. The input ports can be used to send an interrupt request to the CPU via the input interrupt condition flag. See Section 3.9 "Interrupt and Halt", for details.

Examples of input port control program

• Loading K00–K03 into the A register

```
Label   Mnemonic/operand          Comment
        LD      Y,0E0H           ;Set address of port
        LD      A,MY             ;A register ← K00–K03
```

As shown in Figure 3.1.1, the two instruction steps above load the data of the input port into the A register.

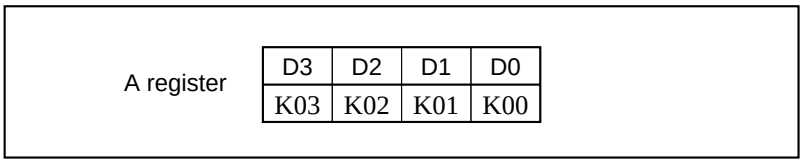


Fig. 3.1.1
Loading the A register

The data of the input port can be loaded into the B register or MX instead of the A register.

• Bit-unit checking of input ports

```
Label    Mnemonic/operand          Comment
         DI                        ;Disable interrupt
         LD      Y,0E0H            ;Set address of port
INPUT1:  FAN     MY,0010B          ;
         JP      NZ,INPUT1         ;Loop until K01 becomes "0"
INPUT2:  FAN     MY,0010B          ;
         JP      Z,INPUT2          ;Loop until K01 becomes "1"
```

This program loopes until a rising edge is input to input port K01.

The input port can be addressed using the X register instead of the Y register.

Note *When the input port is changed from high level to low level with a pull-down resistor, the signal falls following a certain delay caused by the time constants of the pull-down resistance and the input gate capacitance. It is therefore necessary to observe a proper wait time before the input port data is read.*

3.2 Output Port

Output port memory map

Table 3.2.1 I/O memory map

Address	Register D3	D2	D1	D0	Name	SR *1	1	0	Comment
0F3H	R03	R02	R01 / BUZZER	R00 / FOUT	R03	0	High	Low	R03 output port data
	R/W				R02	0	High	Low	R02 output port data
					R01	0	High	Low	R01 output port data
					BUZZER	0	ON	OFF	Buzzer ON/OFF control register
					R00	0	High	Low	R00 output port data
					FOUT	0	ON	OFF	Frequency output ON/OFF control register

*1 Initial value following initial reset
*2 Not set in the circuit
*3 Undefined
*4 Reset (0) immediately after being read
*5 Always 0 when being read
*6 Refer to main manual

Control of the output port

The E0C6S37 Series have 4 bits for general output ports (R00–R03). R00 and R01 although can be use for special use output port as shown in later of this section. The output port is a read/write register, output pins provide the contents of the register. The states of the output ports (R00–R03) are decided by the data of address 0F3H. Output ports can also be read, and output control is possible using the operation instructions (AND, OR, etc.). The output ports are all initialized to low level (0) after an initial reset.

Examples of output port control program

• Loading B register data into R00–R03

```
Label   Mnemonic/operand        Comment
        LD      Y,0F3H          ;Set address of port
        LD      MY,B            ;R00–R03 ← B register
```

As shown in Figure 3.2.1, the two instruction steps above load the data of the B register into the output ports.

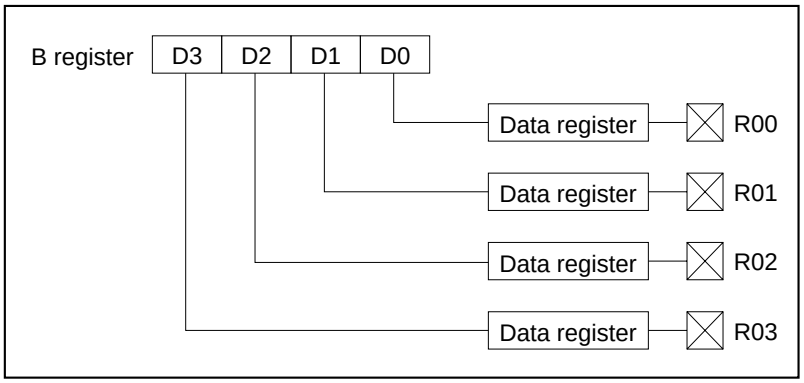


Fig. 3.2.1
Control of the output port

The output data can be taken from the A register, MX, or immediate data instead of the B register.

• Bit-unit operation of output ports

Label	Mnemonic/operand		Comment
	LD	Y,0F3H	;Set address of port
	OR	MY,0010B	;Set R01 to 1
	AND	MY,1011B	;Set R02 to 0

The three instruction steps above cause the output port to be set, as shown in Figure 3.2.2.

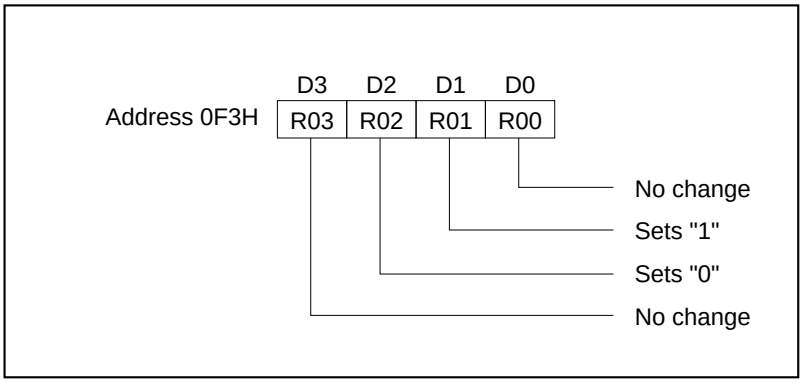


Fig. 3.2.2
Setting of the output port

3.3 Special Use Output Port

Special use output port memory map

Table 3.3.1 I/O memory map

Address	Register D3	Register D2	Register D1	Register D0	Name	SR *1	1	0	Comment
0F3H	R03	R02	R01 / BUZZER	R00 / FOUT	R03	0	High	Low	R03 output port data
	R/W				R02	0	High	Low	R02 output port data
					R01	0	High	Low	R01 output port data
					BUZZER	0	ON	OFF	Buzzer ON/OFF control register
					R00	0	High	Low	R00 output port data
					FOUT	0	ON	OFF	Frequency output ON/OFF control register
0FDH	XBZR	0	XFOUT1	XFOUT0	XBZR	0	2 kHz	4 kHz	Buzzer frequency control
	R/W	R	R/W		0 *5				
					XFOUT1	0	High	Low	FOUT frequency control: XFOUT1(0), XFOUT0(0) -> F1 XFOUT1(0), XFOUT0(1) -> F2
					XFOUT0	0	High	Low	XFOUT1(1), XFOUT0(0) -> F3 XFOUT1(1), XFOUT0(1) -> F4

*1 Initial value following initial reset
*2 Not set in the circuit
*3 Undefined
*4 Reset (0) immediately after being read
*5 Always 0 when being read
*6 Refer to main manual

Control of the special use output port

In addition to the regular DC, special output can be selected for output ports R00 and R01, as shown in Table 3.3.2. Figure 3.3.1 shows the structure of output ports R00–R03.

Table 3.3.2
Special output

Pin Name	When Special Output is Selected
R00	FOUT or $\overline{\text{BUZZER}}$
R01	BUZZER

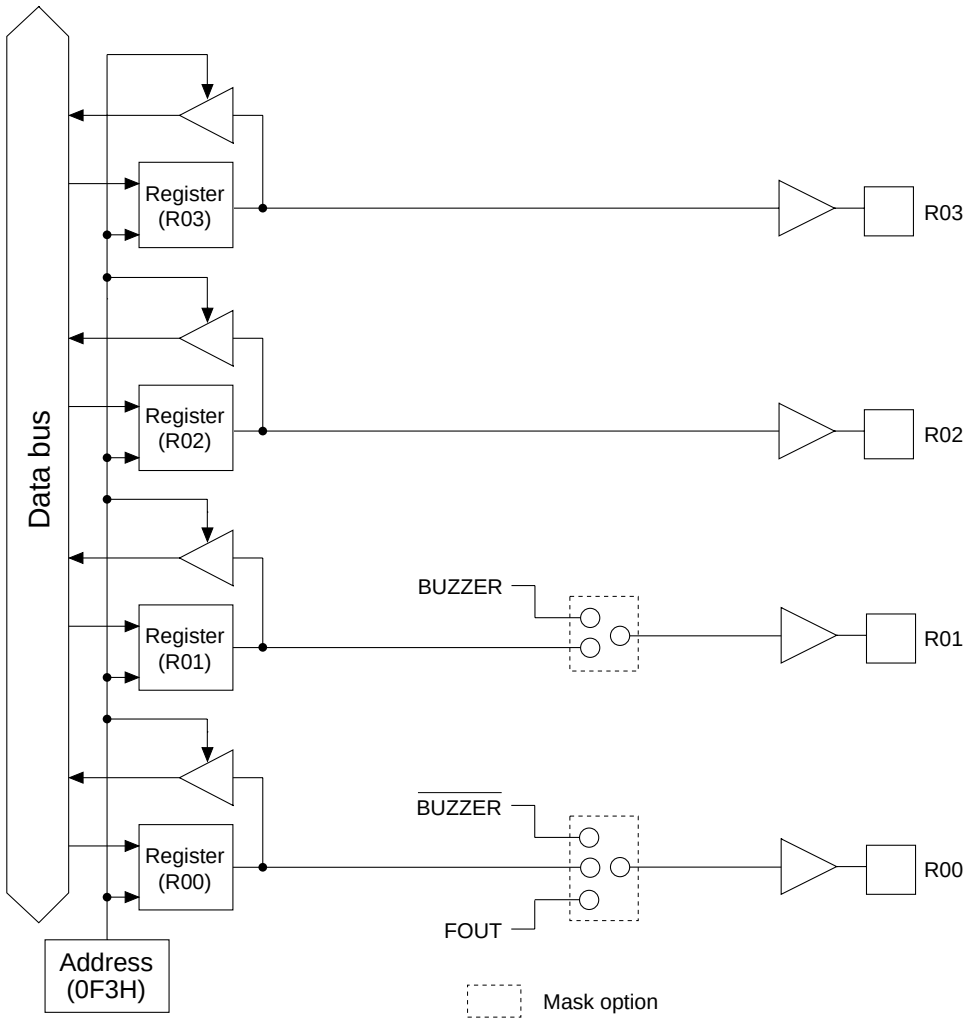


Fig. 3.3.1
Structure of output ports R00–R03

Examples of special use output port control program

• Buzzer driver output (BUZZER)

When output port R01 is set for BUZZER and R00 is set for $\overline{\text{BUZZER}}$, it performs 2,048 Hz or 4,096 Hz selected by register XBZR (0FDH D3).

```
Label   Mnemonic/operand          Comment
        LD      Y,0FDH           ;Set address of BUZZER
                                 ;frequency control register
        LD      MY,1000B         ;Select 2,048 Hz
        LD      Y,0F3H           ;Set address of output port
        OR      MY,0010B         ;Turn on BUZZER
         :       :
        AND     MY,1101B         ;Turn off BUZZER
```

• Internal divided frequency output (FOUT)

When output port R00 is set to FOUT output, fosc or clock frequency divided into fosc is generated. Clock frequency may be selected individually for F1–F4, from among 5 types by mask option; a clock frequency is then selected from 4 types (i.e., F1–F4) through XFOUT0 and XFOUT1 (0FDH D0 and D1) registers and is generated.
The clock frequency types are shown in Table 3.3.3.

Table 3.3.3
Mask option and register selection

Mask Option Sets	Clock Frequency (Hz) fosc = 32.768 kHz			
	F1	F2	F3	F4
	(D1,D0)=(0,0)	(D1,D0)=(0,1)	(D1,D0)=(1,0)	(D1,D0)=(1,1)
Set 1	256 (fosc/128)	512 (fosc/64)	1,024 (fosc/32)	2,048 (fosc/16)
Set 2	512 (fosc/64)	1,024 (fosc/32)	2,048 (fosc/16)	4,096 (fosc/8)
Set 3	1,024 (fosc/32)	2,048 (fosc/16)	4,096 (fosc/8)	8,192 (fosc/4)
Set 4	2,048 (fosc/16)	4,096 (fosc/8)	8,192 (fosc/4)	16,384 (fosc/2)
Set 5	4,096 (fosc/8)	8,192 (fosc/4)	16,384 (fosc/2)	32,768 (fosc/1)

For example mask option is set to Set 4:

```
Label   Mnemonic/operand        Comment
        LD      Y,0FDH          ;Set address of FOUT
                                ;frequency control register
        LD      MY,0011B        ;Select 16,384 Hz
        LD      Y,0F3H          ;Set address of output port
        OR      MY,0001B        ;Turn on FOUT
          :       :
        AND     MY,1110B        ;Turn off FOUT
```

3.4 I/O Port

I/O port memory map

Table 3.4.1 I/O memory map

Address	Register								Comment
	D3	D2	D1	D0	Name	SR *1	1	0	
0F6H	P03	P02	P01	P00	P03	– *2	High	Low	I/O port (P00–P03)
	R/W				P02	– *2	High	Low	
					P01	– *2	High	Low	
					P00	– *2	High	Low	
0FCH	0	0	0	IOC	0 *5				
	R			R/W	0 *5				
					0 *5				
					IOC	0	Output	Input	I/O port P00–P03 Input/Output

*1 Initial value following initial reset
*2 Not set in the circuit
*3 Undefined
*4 Reset (0) immediately after being read
*5 Always 0 when being read
*6 Refer to main manual

Control of the I/O port

The E0C6S37 contains a 4-bit general I/O port (4 bits × 1). This port can be used as an input port or an output port, according to I/O port control register IOC. When IOC is "0", the port is set for input, when it is "1", the port is set for output.

• How to set an input port

Set "0" in the I/O port control register (D0 of address 0FCH), and the I/O port is set as an input port. The state of the I/O port (P00–P03) is decided by the data of address 0F6H. (In the input mode, the port level is read directly.)

• How to set an output port

Set "1" in the I/O port control register, and the I/O port is set as an output port. The state of the I/O port is decided by the data of address 0F6H. This data is held by the register, and can be set regardless of the contents of the I/O control register. (The data can be set whether P00 to P03 ports are input ports or output ports.)

The I/O control registers are cleared to "0" (input/output ports are set as input ports), and the data registers are also cleared to "0" after an initial reset.

Examples of I/O port control program

• Loading P00–P03 input data into A register

```
Label   Mnemonic/operand        Comment
        LD      Y,0FCH          ;Set address of I/O control port
        AND     MY,1110B        ;Set port as input port
        LD      Y,0F6H          ;Set address of port
        LD      A,MY            ;A register ← P00–P03
```

As shown in Figure 3.4.1, the four instruction steps above load the data of the I/O ports into the A register.

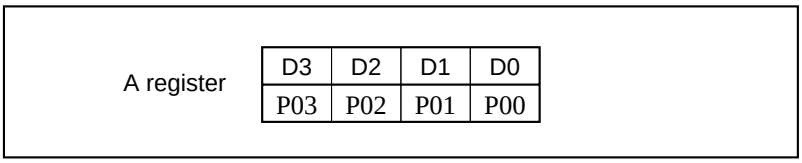


Fig. 3.4.1
Loading into the A register

• Loading P00–P03 output data into A register

Label	Mnemonic/operand		Comment
	LD	Y,0FCH	;Set the address of input/output
			;port control register
	OR	MY,0001B	;Set as output port
	LD	Y,0F6H	;Set the address of port
	LD	A,MY	;A register ← P00–P03

As shown in Figure 3.4.2, the four instruction steps above load the data of the I/O ports into the A register.

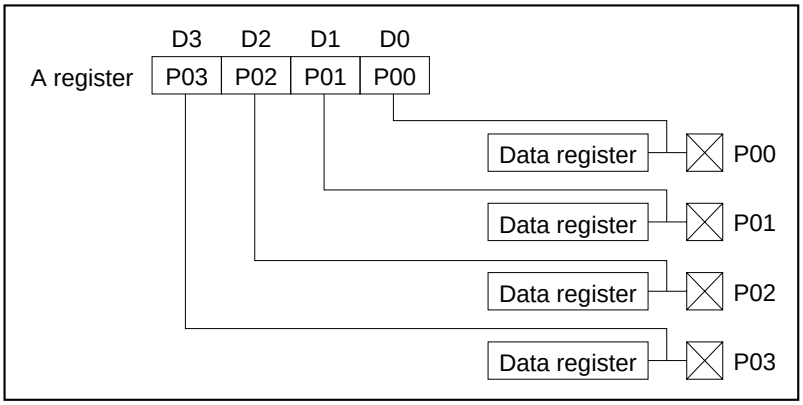


Fig. 3.4.2
Control of I/O port (input)

Data can be loaded from the I/O port into the B register or MX instead of the A register.

• Loading contents of B register into P00–P03

Label	Mnemonic/operand		Comment
	LD	Y,0FCH	;Set the address of input/output
			;port control register
	OR	MY,0001B	;Set port as output port
	LD	Y,0F6H	;Set the address of port
	LD	MY,B	;P00–P03 ← B register

As shown in Figure 3.4.3, the four instruction steps above load the data of the B register into the I/O ports.

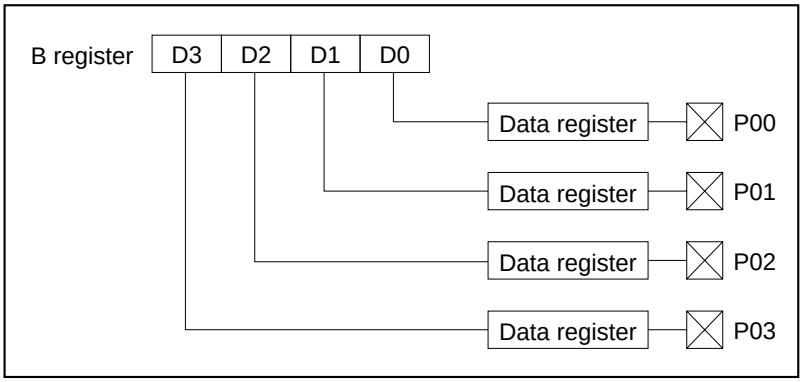


Fig. 3.4.3
Control of the I/O port (output)

The output data can be taken from the A register, MX, or immediate data instead of the B register.

Bit-unit operation for the I/O port is identical to that for the input ports (K00–K03) or output ports (R00–R03).

3.5 LCD Driver

LCD driver memory map

Table 3.5.1 I/O memory map

Address	Register								Comment
	D3	D2	D1	D0	Name	SR *1	1	0	
0FBH	CSDC	0	0	0	CSDC	0	Static	Dynamic	LCD drive switch
	R/W	R			0 *5				
					0 *5				
					0 *5				

*1 Initial value following initial reset
*2 Not set in the circuit
*3 Undefined
*4 Reset (0) immediately after being read
*5 Always 0 when being read
*6 Refer to main manual

Address	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
090 0A0	Display memory (write only) 32 words x 4 bits															

Fig. 3.5.1
Display memory map

Control of the LCD driver

The E0C6S37 contains 128 bits of display memory in addresses 090H to 0AFH of the data memory. Each display memory can be assigned to any 104 bits of the 128 bits for the LCD driver (26 SEG × 4 COM), 78 bits of the 128 bits (26 SEG × 3 COM) or 52 bits of the 128 bits (26 SEG × 2 COM) by using a mask option. The remaining 24 bits, 50 bits or 76 bits of display memory are not connected to the LCD driver, and are not output even when data is written. An LCD segment is on with "1" set in the display memory, and off with "0" set in the display memory. Note that the display memory is a write-only.

• LCD drive control register (CSDC)

The LCD drive control register (CSDC: address 0FBH, D3) can set the 1/1 duty drive. Set "0" in CSDC for 1/4 duty, 1/3 duty or 1/1 duty drive. Set "1" in CSDC and the same value in the registers corresponding to COMs 0 through 3 for 1/1 duty drive.
Figure 3.5.2 shows the 1/1 duty drive waveform (1/3 bias) and Figure 3.5.3 shows an example of the 7-segment LCD assignment.
See page I-44 for the 1/1 duty drive waveform (1/2 bias).

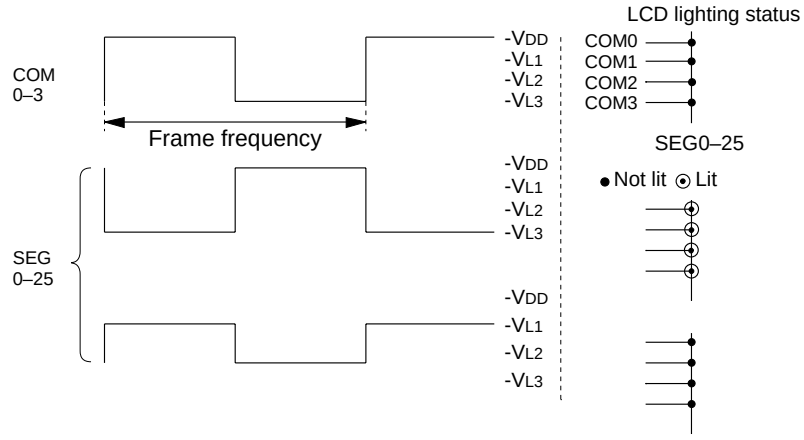
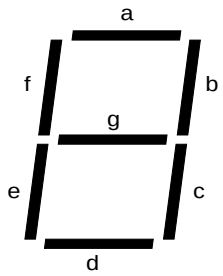


Fig. 3.5.2
1/1 duty drive control
(1/3 bias)



Address	Register			
	D3	D2	D1	D0
090H	d	c	b	a
091H		g	f	e

Fig. 3.5.3
7-segment LCD assignment

In the assignment shown in Figure 3.5.3, the 7-segment display pattern is controlled by writing data to display memory addresses 090H and 091H.

Examples of LCD driver control program

• Displaying 7-segment

The LCD display routine using the assignment of Figure 3.5.3 can be programmed as follows.

```
Label     Mnemonic/operand      Comment
          ORG     000H
          RETD    3FH           ;0 is displayed
          RETD    06H           ;1 is displayed
          RETD    5BH           ;2 is displayed
          RETD    4FH           ;3 is displayed
          RETD    66H           ;4 is displayed
          RETD    6DH           ;5 is displayed
          RETD    7DH           ;6 is displayed
          RETD    27H           ;7 is displayed
          RETD    7FH           ;8 is displayed
          RETD    6FH           ;9 is displayed

SEVENS:   LD      B,0           ;Set the address of jump
          LD      X,090H        ;Set address of display memory
          JPBA
```

When the above routine is called (by the CALL or CALZ instruction) with any number from "0" to "9" set in the A register for the assignment of Figure 3.5.4, seven segments are displayed according to the contents of the A register.

Fig. 3.5.4
Data set in A register and displayed patterns

A resister	Display	A resister	Display	A resister	Display	A resister	Display	A resister	Display
0	0	2	2	4	4	6	6	8	8
1	1	3	3	5	5	7	7	9	9

The RETD instruction can be used to write data to the display memory only if it is addressed using the X register. (Addressing using the Y register is invalid.)

Note that the stack pointer must be set to a proper value before the CALL (CALZ) instruction is executed.

• Bit-unit operation of the display memory

Fig. 3.5.5
Example of segment assignment

Address	Data			
	D3	D2	D1	D0
090H			▲	●

▲ : SEG-A
● : SEG-B

Label	Mnemonic/operand		Comment
	LD	X,SEGBUF	;Set address display
			;memory buffer
	LD	Y,090H	;Set address display memory
	LD	MX,3	;Set buffer data
	LD	MY,MX	;SEG-A, B ON (○, △)
	AND	MX,1110B	;Change buffer data
	LD	MY,MX	;SEG-A OFF (●, △)
	AND	MX,1101B	;Change buffer data
	LD	MY,MX	;SEG-B OFF (●, ▲)

For manipulation of the display memory in bit-units for the assignment of Figure 3.5.5, a buffer must be provided in RAM to hold data. Note that, since the display memory is write-only, data cannot be changed directly using an ALU instruction (for example, AND or OR).

After manipulating the data in the buffer, write it into the corresponding display memory using the transfer command.

3.6 Timer

Timer memory map

Table 3.6.1 I/O memory map

Address	Register D3	D2	D1	D0	Name	SR *1	1	0	Comment
0E4H	TM3	TM2	TM1	TM0	TM3	–	High	Low	Timer data (clock timer 2 Hz)
	R				TM2	–	High	Low	Timer data (clock timer 4 Hz)
					TM1	–	High	Low	Timer data (clock timer 8 Hz)
					TM0	–	High	Low	Timer data (clock timer 16 Hz)
0EBH	0	EIT2	EIT8	EIT32	0 *5				
	R	R/W			EIT2	0	Enable	Mask	Interrupt mask register (clock timer 2 Hz)
					EIT8	0	Enable	Mask	Interrupt mask register (clock timer 8 Hz)
					EIT32	0	Enable	Mask	Interrupt mask register (clock timer 32 Hz)
0EFH	0	IT2	IT8	IT32	0 *5				
	R				IT2 *4	0	Yes	No	Interrupt factor flag (clock timer 2 Hz)
					IT8 *4	0	Yes	No	Interrupt factor flag (clock timer 8 Hz)
					IT32 *4	0	Yes	No	Interrupt factor flag (clock timer 32 Hz)
0F9H	0	TMRST	SWRUN	SWRST	0 *5				
	R	W	R/W	W	TMRST	Reset	Reset	–	Clock timer reset
					SWRUN	0	Run	Stop	Stopwatch timer RUN/STOP
					SWRST *5	Reset	Reset	–	Stopwatch timer reset

*1 Initial value following initial reset
*2 Not set in the circuit
*3 Undefined
*4 Reset (0) immediately after being read
*5 Always 0 when being read
*6 Refer to main manual

Control of the timer

The E0C6S37 contains a timer with a basic oscillation of 32.768 kHz (typical). This timer is a 4-bit binary counter, and the counter data can be read as necessary. The counter data of the 16 Hz clock can be read by reading TM3 to TM0 (address 0E4H, D3 to D0). ("1" to "0" are set in TM3 to TM0, corresponding to the high-low levels of the 2 Hz, 4 Hz, 8 Hz, and 16 Hz 50 % duty waveform. See Figure 3.6.1.) The timer can also interrupt the CPU on the falling edges of the 32 Hz, 8 Hz, and 2 Hz signals. For details, see Section 3.9, "Interrupt and Halt".

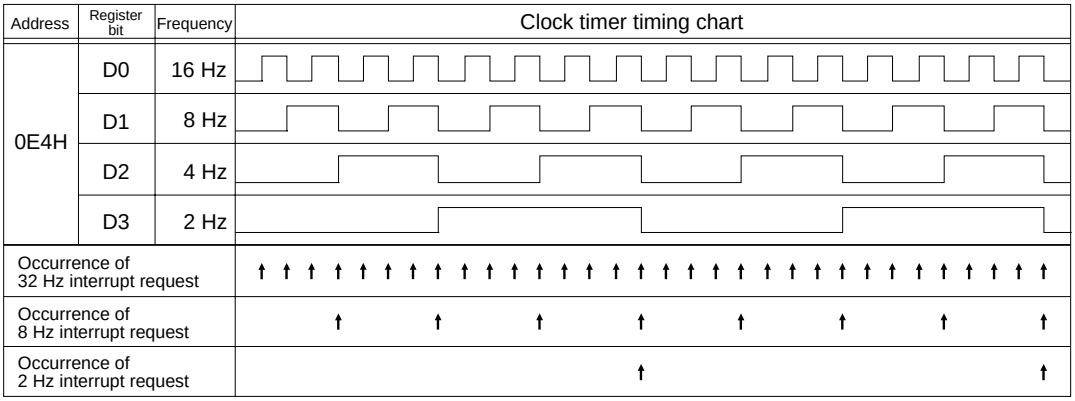


Fig. 3.6.1
Output waveform of timer and interrupt timing

The timer is reset by setting "1" in TMRST (address 0F9H, D2).

Note *The 128 Hz to 2 Hz of the internal divider is initialized by resetting the timer, and 128 Hz to 1 Hz of the internal divider is reset by resetting the stopwatch timer.*

The dividers of the timer and stopwatch timers are individual circuits, so resetting one circuit does not affect the other.

Examples of timer control program

• Initializing the timer

```
Label   Mnemonic/operand        Comment
        LD      Y,0F9H          ;Set address of the timer
                                ;reset register
        OR      MY,0100B        ;Reset the timer
```

The two instruction steps above are used to reset (clear TM0–TM3 to 0) and restart the timer. The TMRST register is cleared to "0" by hardware 1 clock after it is set to "1".

• Loading the timer

```
Label   Mnemonic/operand        Comment
        LD      Y,0E4H          ;Set address of
                                ;the timer data (TM0 to TM3)
        LD      A,MY            ;Load the data of
                                ;TM0 to TM3 into A register
```

As shown in Table 3.6.2, the two instruction steps load the data of TM0 to TM3 into the A register.

Table 3.6.2
Loading the timer data

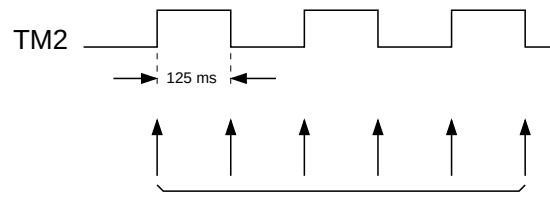
A register	D3	D2	D1	D0
	TM3 (2 Hz)	TM2 (4 Hz)	TM1 (8 Hz)	TM0 (16 Hz)

• Checking timer edge

```
Label      Mnemonic/operand          Comment
           LD      X,TMSTAT          ;Set address of the timer edge counter
           CP      MX,0              ;Check whether the timer edge
                                     ;counter is "0"
           JP      Z,RETURN          ;Jump if "0" (Z-flag is "1")
           LD      Y,0E4H            ;Set address of the timer
           LD      A,MY              ;Read the data of TM0 to TM3
                                     ;into A register
           LD      Y,TMDTBF          ;Set address of the timer data buffer
           XOR     MY,A              ;Did the count on the timer
                                     ;change?
           FAN     MX,0100B          ;Check bit D2 of the timer data buffer
           LD      MY,A              ;Set the data of A register into
                                     ;the timer data buffer
           JP      Z,RETURN          ;Jump, if the Z-flag is "1"
           ADD     MX,0FH            ;Decrement the timer edge counter
;
RETURN:    RET                       ;Return
```

This program takes a subroutine form. It is called at short intervals, and decrements the data at address TMSTAT every 125 ms until the data reaches "0". The timing chart is shown in Figure 3.6.2. The timer can be addressed using the X register instead of the Y register.

Note *TMSTAT and TMDTBF may be any address in RAM and not involve a hardware function.*



Timer edge counter (TMSTAT) decrementing timing

Fig. 3.6.2
Timing of the timer edge counter

3.7 Stopwatch Timer

Stopwatch timer memory map

Table 3.7.1 I/O memory map

Address	Register D3	D2	D1	D0	Name	SR *1	1	0	Comment
0E2H	SWL3	SWL2	SWL1	SWL0	SWL3	0			MSB
	R				SWL2	0			Stopwatch timer 1/100 sec (BCD)
					SWL1	0			
					SWL0	0			LSB
0E3H	SWH3	SWH2	SWH1	SWH0	SWH3	0			MSB
	R				SWH2	0			Stopwatch timer 1/10 sec (BCD)
					SWH1	0			
					SWH0	0			LSB
0EAH	0	0	EISW1	EISW0	0 *5				
	R		R/W		0 *5				
					EISW1	0	Enable	Mask	Interrupt mask register (stopwatch 1 Hz)
					EISW0	0	Enable	Mask	Interrupt mask register (stopwatch 10 Hz)
0EEH	0	0	ISW1	ISW0	0 *5				
	R				0 *5				
					ISW1 *4	0	Yes	No	Interrupt factor flag (stopwatch 1 Hz)
					ISW0 *4	0	Yes	No	Interrupt factor flag (stopwatch 10 Hz)
0F9H	0	TMRST	SWRUN	SWRST	0 *5				
	R	W	R/W	W	TMRST	Reset	Reset	–	Clock timer reset
					SWRUN	0	Run	Stop	Stopwatch timer RUN/STOP
					SWRST *5	Reset	Reset	–	Stopwatch timer reset

*1 Initial value following initial reset
*2 Not set in the circuit
*3 Undefined
*4 Reset (0) immediately after being read
*5 Always 0 when being read
*6 Refer to main manual

Control of the stopwatch timer

The E0C6S37 contains 1/100 sec and 1/10 sec stopwatch timers.

This timer can be loaded in 4-bit units. Starting, stopping, and resetting the timer can be controlled by register.

Figure 3.7.1 shows the operation of the stopwatch timer.

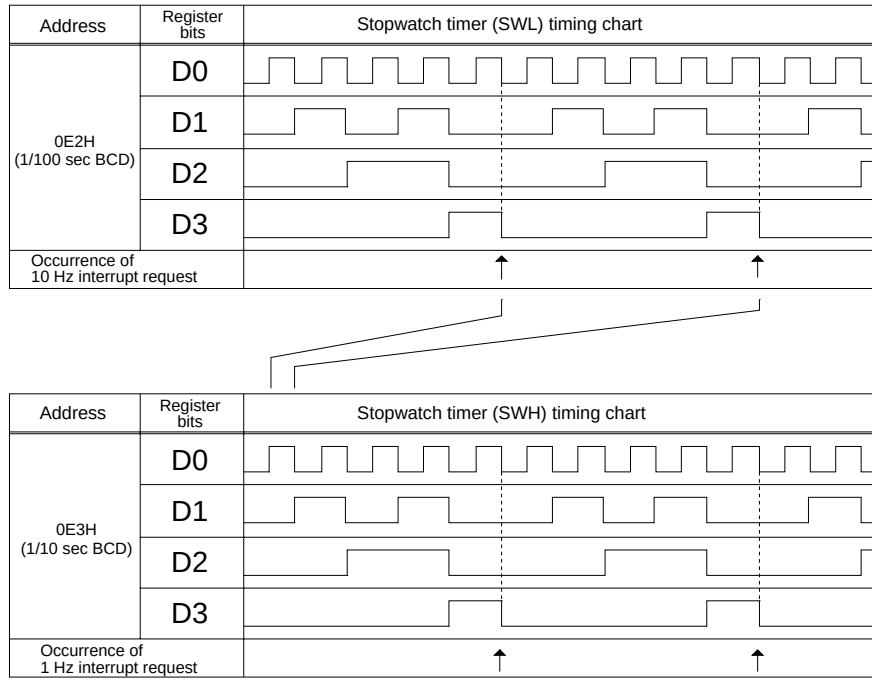


Fig. 3.7.1
Stopwatch timer
operating timing

Examples of stopwatch timer control program

• Initializing the stopwatch timer

Label	Mnemonic/operand		Comment
	LD	Y,0F9H	;Set address of the SWRST register
	OR	MY,0001B	;Reset the stopwatch timer

The two instruction steps above reset the stopwatch timer. (SWL3 to SWL0, SWH3 to SWH0 are all cleared to "0".)

Note *The stopwatch timer is reset by setting "1" in the SWRST register. However, the SWRST register is cleared to "0" by hardware 1 clock after it is set to "1".*

• Starting the stopwatch timer

Label	Mnemonic/operand		Comment
	LD	Y,0F9H	;Set address of SWRUN register
	OR	MY,0010B	;Start the stopwatch timer

The two instruction steps above run the stopwatch timer of SWL0 to SWL3, and SWH0 to SWH3 (addresses 0E2H and 0E3H, respectively).

• Stopping the stopwatch timer

Label	Mnemonic/operand		Comment
	LD	Y,0F9H	;Set address of SWRUN register
	AND	MY,1101B	;Stop the stopwatch timer

The two instruction steps above stop the stopwatch timer of SWL0 to SWL3, and SWH0 to SWH3 (addresses 0E2H and 0E3H, respectively).

• Loading the stopwatch timer

```
Label   Mnemonic/operand          Comment
        LD      Y,0E2H           ;Set address of the SWL of
                                 ;the stopwatch
        LDPY    A,MY             ;Read the data of SWL0 to SWL3
                                 ;into A register
        LD      B,MY             ;Read the data of SWH0 to SWH3
                                 ;into B register
```

The three instruction steps above reads the contents of the stopwatch timer into A register and B register. (Also see Table 3.7.2.)

Table 3.7.2
Data load into A register and B register

	D3	D2	D1	D0
A register	SWL3	SWL2	SWL1	SWL0
B register	SWH3	SWH2	SWH1	SWH0

Note *A read-in error caused by a carry from the SWL is not taken into account in this program. You are recommended to add a handling routine in your application.*

3.8 Supply Voltage Detection (SVD) Circuit and Heavy Load Protection Function

The E0C6S37 Series has built-in supply voltage detection circuit and drop in supply voltage may be detected by controlling the register on the I/O memory. Criteria voltages are as follows:

Model	Criteria Voltage
E0C6S37	2.4 V ± 0.15 V
E0C6SL37	1.2 V ± 0.10 V
E0C6SB37	1.2 V ± 0.10 V

Moreover, when the battery load becomes heavy, such as during external piezo buzzer driving or external lamp lighting, heavy load protection function is built-in in case the supply voltage drops.
E0C6SL37/E0C6SB37 operate at 0.9 V due to the SVD circuit and heavy load protection function.

SVD circuit and heavy load protection function memory map

Table 3.8.1 I/O memory map

Address	Register								Comment
	D3	D2	D1	D0	Name	SR *1	1	0	
0FAH	HLMOD	0	SVDDT	SVDON	HLMOD	0	Heavy load	Normal load	Heavy load protection mode register
	R/W	R		R/W	0 *5				
					SVDDT	0	Supply voltage low	Supply voltage normal	Supply voltage detection data
					SVDON	0	ON	OFF	Supply voltage detection ON/OFF

*1 Initial value following initial reset
*2 Not set in the circuit
*3 Undefined
*4 Reset (0) immediately after being read
*5 Always 0 when being read
*6 Refer to main manual

Control of the SVD circuit

The SVD circuit will turn ON by writing "1" on the SVDON register (address 0FAH, D0, R/W) and supply voltage detection will be performed. By writing "0" on the SVDON register, the detection result is stored in the SVDDT register. However, in order to obtain a stable detection result, it is necessary to turn the SVD circuit ON for at least 100 µs. Accordingly, reading out the detection result from the SVDDT register is performed through the following procedures:

① Set the SVDON register to "1".
② Provide at least 100 µs waiting time.
③ Set the SVDON register to "0".
④ Read-out from the SVDDT register.

Note, however, that when E0C6S37 is to be used with the normal system clock at fosc = 32.768 kHz, there is no need for the waiting time stated in the above procedure ② since 1 instruction cycle will take longer than 100 µs.
Because the power current consumption of the IC becomes large when the SVD circuit is operated, turn the SVD circuit OFF when not in use. The operation timing chart is shown in Figure 3.8.1.

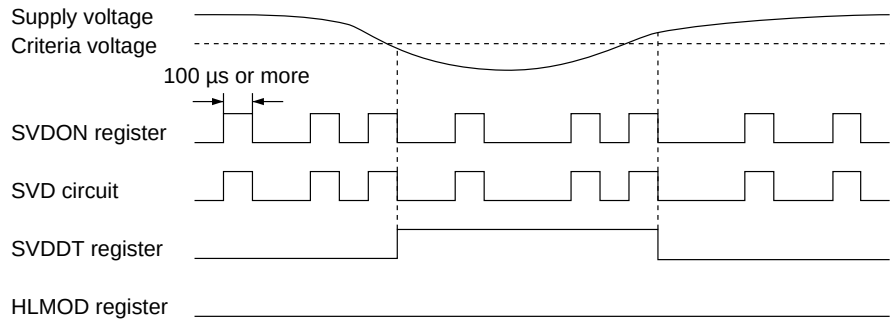


Fig. 3.8.1 Timing chart of supply voltage detection operation through the SVDON register

Example of SVD circuit control program

```
Label   Mnemonic/operand        Comment
        LD      X,0FAH          ;Sets the address of SVDON
        OR      MX,0001B        ;Sets SVDON to "1"
        AND     MX,1110B        ;Sets SVDON to "0"
        LD      A,MX            ;Loads the detection result
                                ;into the A register
```

Heavy load protection function

Note that the heavy load protection function on the E0C6SL37/E0C6SB37 are different from the E0C6S37.

(1) In case of E0C6SL37/E0C6SB37

The E0C6SL37/E0C6SB37 have the heavy load protection function for when the battery load becomes heavy and the source voltage drops, such as when an external buzzer sounds or an external lamp lights. The state where the heavy load protection function is in effect is called the heavy load protection mode. In this mode, operation with a lower voltage than normal is possible. The normal mode changes to the heavy load protection mode in the following two cases:

① When the software changes the mode to the heavy load protection mode (HLMOD = "1")

② When supply voltage drop (SVDDT = "1") in the SVD circuit is detected, the mode will automatically shift to the heavy load protection mode until the supply voltage is recovered (SVTDT = "0")

In the heavy load protection mode, the internally regulated voltage is generated by the liquid crystal driver source output V_{L2} so as to operate the internal circuit. Consequently, more current is consumed in the heavy load protection mode than in the normal mode. Unless it is necessary, be careful not to set the heavy load protection mode with the software. Also, to reduce current consumption, do not set the SVDON to ON in the heavy load protection mode.

(2) In case of E0C6S37

The E0C6S37 has the heavy load protection function for when the battery load becomes heavy and the source voltage changes, such as when an external buzzer sounds or an external lamp lights. The state where the heavy load protection function is in effect is called the heavy load protection mode. Compared with the normal operation mode, this mode can reduce the output voltage variation of the constant voltage or voltage booster/reducer of the LCD system.

The normal mode changes to the heavy load protection mode in the following case:

- When the software changes the mode to the heavy load protection mode (HLMOD = "1")

The heavy load protection mode switches the constant voltage circuit of the LCD system to the high-stability mode from the low current consumption mode. Consequently, more current is consumed in the heavy load protection mode than in the normal mode. Unless it is necessary, be careful not to set the heavy load protection mode with the software.

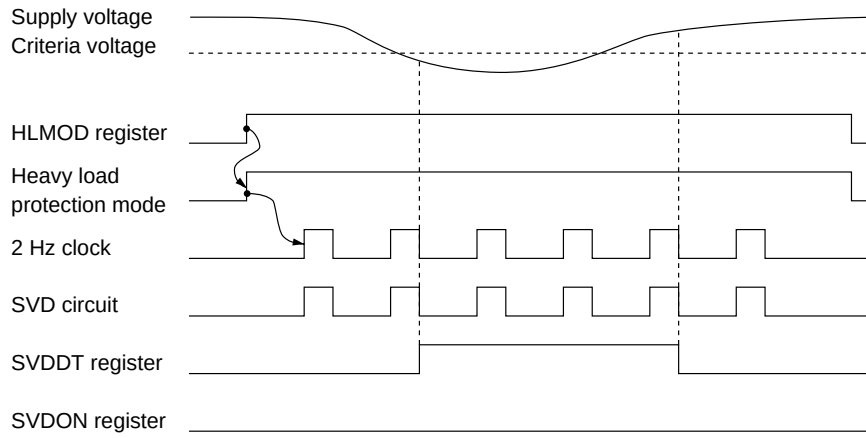


Fig. 3.8.2 Timing chart of supply voltage detection operation through the HLMOD register

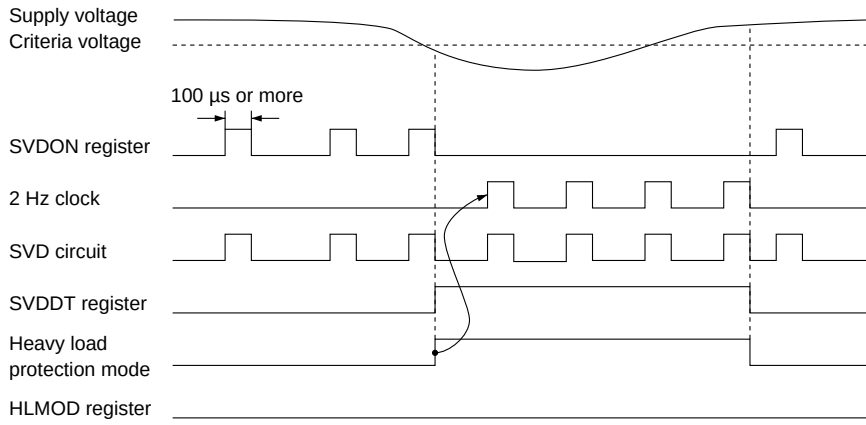


Fig. 3.8.3 Timing chart of heavy load protection function operation through the SVDON register

Examples of heavy load protection function control program

- **Operation through the HLMOD register**

  This is a sample program when lamp is driven with the R00 terminal during performance of heavy load protection.

```
Label   Mnemonic/operand      Comment
        LD      X,0FAH        ;Sets the address of HLMOD
        OR      MX,1000B      ;Sets to the heavy protection mode
        LD      Y,0F3H        ;Sets the address of R0n port
        OR      MY,0001B      ;Turns lamp ON
            :
            :
        LD      Y,0F3H        ;Sets the R0n port address
        AND     MY,1110B      ;Turns the lamp OFF
        CALL    WT1S          ;1 second waiting time (software timer)
        AND     MX,0111B      ;Cancels the heavy load protection mode
```

In the above program, the heavy load protection mode is canceled after 1 sec waiting time provided as the time for the battery voltage to stabilize after the lamp is turned off; however, since this time varies according to the nature of the battery, time setting must be done in accordance with the actual application.

- **Operation through the SVDON register**

```
Label    Mnemonic/operand          Comment
         LD      X,0FAH            ;Sets the HLMOD/SVDDT address
         FAN     MX,1010B          ;Checks the HLMOD/SVDDT bits
         JP      NZ,HLMOD          ;Heavy load protection mode
         OR      MX,0001B          ;Sets the SVDON to "1"
         AND     MX,1110B          ;Sets the SVDON to "0"
         FAN     A,0010B           ;Checks the SVDDT bit
         JP      Z,HLMOD           ;Shifts the mode to
                                   ;the heavy load protection mode
         LD      Y,FLAG
         AND     MY,0              ;Resets the flag to "0"
         RET
;
HLMOD:   LD      Y,FLAG
         OR      MY,1              ;Sets the flag to "1"
         RET
```

The above program operates the heavy load protection function by using the SVDON register. In the normal operation mode, supply voltage detection is done from the SVDON register and when the supply voltage drops below the criteria voltage, the mode shifts to the heavy load protection mode. In the heavy load protection mode, supply voltage detection by the hardware is done every 2 Hz and the detection result is stored in the SVDDT register. Because of this, the SVDDT register will be "1" during the heavy load protection mode. Moreover, in the above program, supply voltage detection by the SVDON is halted during the heavy load protection mode. If the supply voltage become grater than the criteria voltage, the SVDDT register value will become "0" and hence, supply voltage detection through the SVDON register will resume after checking the SVDDT register value. When used as a sub-routine, the above program will enable the user to determine whether the present operation mode is the normal operation mode (flag = "0") or the heavy load protection mode (flag = "1").

The flowchart for the above program is shown in the next page.

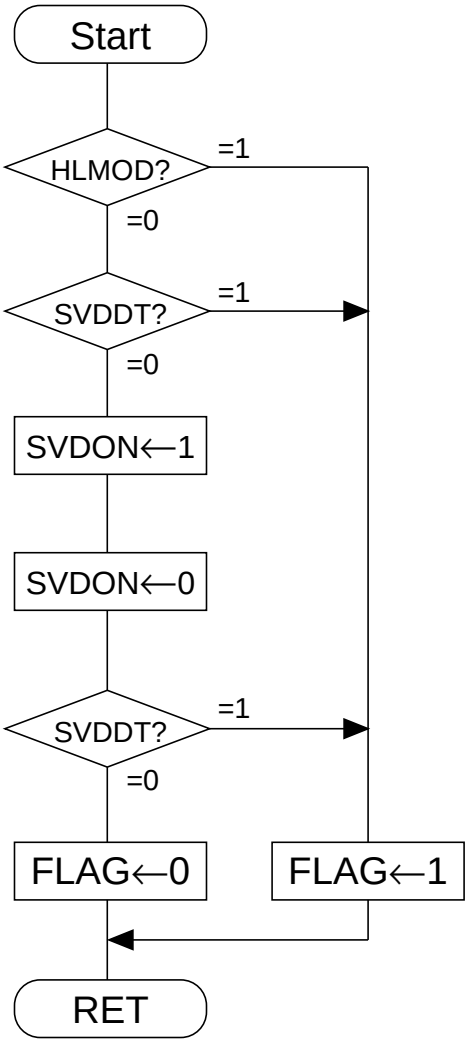


Fig. 3.8.4
Flowchart of operation
through the SVDON register

3.9 Interrupt and Halt

Interrupt memory map

Table 3.9.1(a) I/O memory map

Address	Register D3	D2	D1	D0	Name	SR *1	1	0	Comment
0E8H	EIK03	EIK02	EIK01	EIK00	EIK03	0	Enable	Mask	Interrupt mask register (K03)
	R/W				EIK02	0	Enable	Mask	Interrupt mask register (K02)
					EIK01	0	Enable	Mask	Interrupt mask register (K01)
					EIK00	0	Enable	Mask	Interrupt mask register (K00)
0EAH	0	0	EISW1	EISW0	0 *5				
	R		R/W		0 *5				
					EISW1	0	Enable	Mask	Interrupt mask register (stopwatch 1 Hz)
					EISW0	0	Enable	Mask	Interrupt mask register (stopwatch 10 Hz)
0EBH	0	EIT2	EIT8	EIT32	0 *5				
	R	R/W			EIT2	0	Enable	Mask	Interrupt mask register (clock timer 2 Hz)
					EIT8	0	Enable	Mask	Interrupt mask register (clock timer 8 Hz)
					EIT32	0	Enable	Mask	Interrupt mask register (clock timer 32 Hz)
0EDH	0	0	0	IK0	0 *5				
	R				0 *5				
					0 *5				
					IK0 *4	0	Yes	No	Interrupt factor flag (K00–K03)

*1 Initial value following initial reset
*2 Not set in the circuit
*3 Undefined
*4 Reset (0) immediately after being read
*5 Always 0 when being read
*6 Refer to main manual

Table 3.9.1(b) I/O memory map

Address	Register								Comment
	D3	D2	D1	D0	Name	SR *1	1	0	
0EEH	0	0	ISW1	ISW0	0 *5				
	R				0 *5				
					ISW1 *4	0	Yes	No	Interrupt factor flag (stopwatch 1 Hz)
					ISW0 *4	0	Yes	No	Interrupt factor flag (stopwatch 10 Hz)
0EFH	0	IT2	IT8	IT32	0 *5				
	R				IT2 *4	0	Yes	No	Interrupt factor flag (clock timer 2 Hz)
					IT8 *4	0	Yes	No	Interrupt factor flag (clock timer 8 Hz)
					IT32 *4	0	Yes	No	Interrupt factor flag (clock timer 32 Hz)

*1 Initial value following initial reset
*2 Not set in the circuit
*3 Undefined
*4 Reset (0) immediately after being read
*5 Always 0 when being read
*6 Refer to main manual

Control of interrupts and halt

The E0C6S37 supports four types of a total of 9 interrupts. There are three timer interrupts (2 Hz, 8 Hz, 32 Hz), two stopwatch interrupts (1 Hz, 10 Hz) and four input interrupts (K00–K03).

The 9 interrupts are individually enabled or masked (disabled) by interrupt mask registers. The EI and DI instructions can be used to set or reset the interrupt flag (I), which enables or disables all the interrupts at the same time.

When an interrupt is accepted, the interrupt flag (I) is reset, and cannot accepts any other interrupts (DI state).

Restart from the halt state created by the HALT instruction, is done by interrupt.

• Interrupt factor flags

IK0 This flag is set when any of the K00 to K03 input interrupts occurs. The interrupt factor flag (IK0) is set to "1" when the contents of the input (K00–K03) become "1" and the data of the corresponding interrupt mask register (EIK00–EIK03) is "1".
The contents of the IK0 flag can be loaded by software to determine whether the K00–K03 input interrupts have occured.

The flag is reset when loaded by software. (See Figure 3.9.1.)

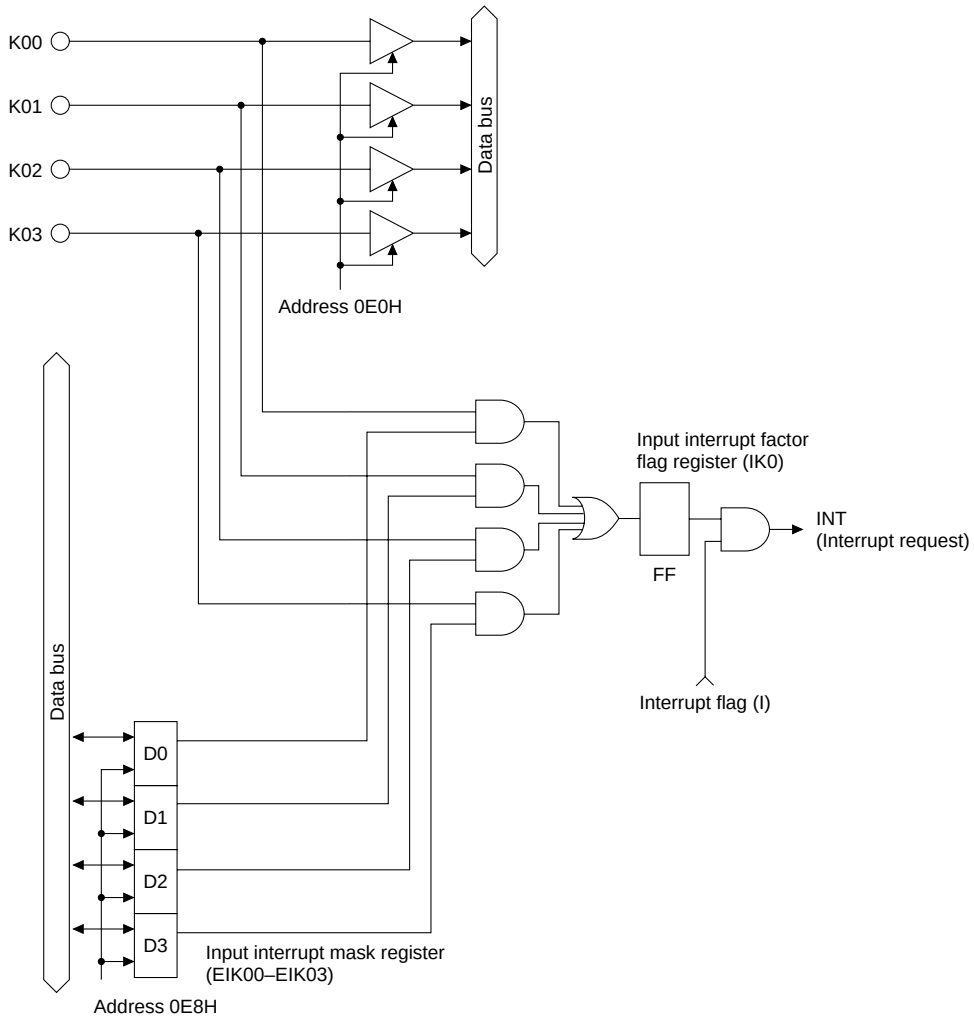


Fig. 3.9.1
K00–K03
Input interrupt circuit

IT32 This flag is set to "1" when a falling edge is detected in the timer TM1 (32 Hz) signal.
The contents of the IT32 flag can be loaded by software to determine whether a 32 Hz timer interrupt has occured.

The flag is reset, when it is loaded by software. (See Figure 3.9.2.)

IT8 This flag is set to "1" when a falling edge is detected in the timer TM1 (8 Hz) signal.
The contents of the IT8 flag can be loaded by software to determine whether an 8 Hz timer interrupt has occured.

The flag is reset, when it is loaded by software. (See Figure 3.9.2.)

IT2 This flag is set to "1" when a falling edge is detected in the timer TM1 (2 Hz) signal.
The contents of the IT2 flag can be loaded by software to determine whether a 2 Hz timer interrupt has occured.

The flag is reset, when it is loaded by software. (See Figure 3.9.2.)

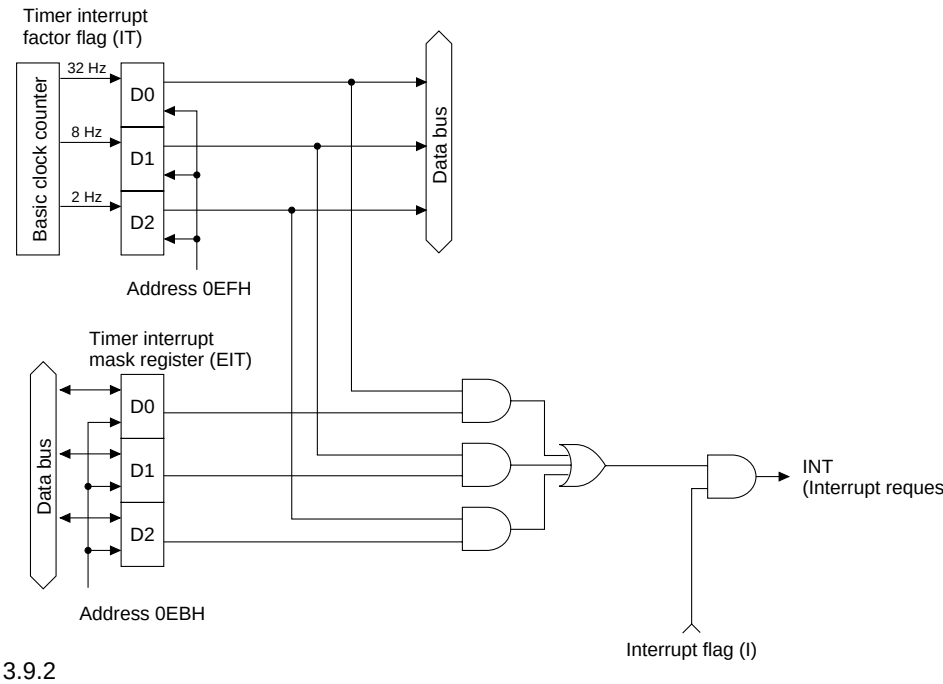


Fig. 3.9.2
Timer interrupt circuit

ISW1 This flag is set to "1" when a falling edge is detected in the stopwatch timer (SWH, 1 Hz).
The contents of the ISW1 flag can be loaded by software to determine whether a 1 Hz stopwatch interrupt has occured.

The flag is reset, when it is loaded by software. (See Figure 3.9.3.)

ISW0 This flag is set to "1" when a falling edge is detected in the stopwatch timer (SWH, 10 Hz).
The contents of the ISW0 flag can be loaded by software to determine whether a 10 Hz stopwatch interrupt has occured.

The flag is reset, when it is loaded by software. (See Figure 3.9.3.)

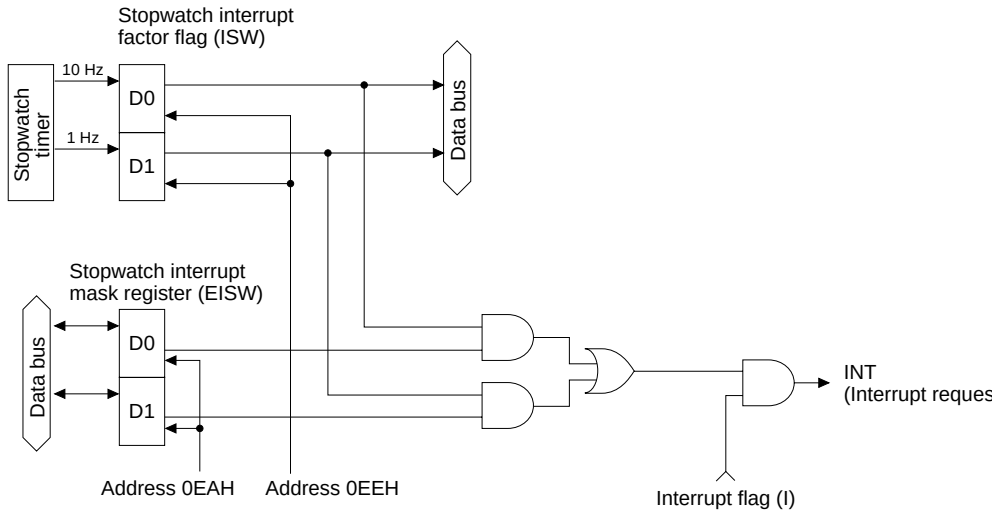


Fig. 3.9.3
Stopwatch interrupt circuit

Note *Reading of interrupt factor flags is available at EI, but be careful in the following cases.*
If the interrupt mask register value corresponding to the interrupt factor flags to be read is set to "1", an interrupt request will be generated by the interrupt factor flags set timing, or an interrupt request will not be generated. Be very careful when interrupt factor flags are in the same address.

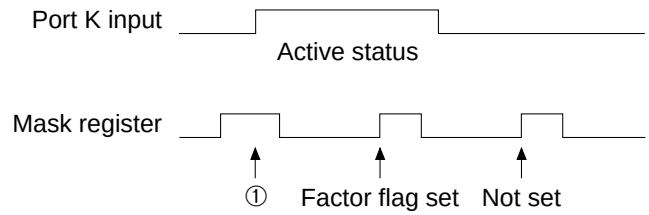
• Interrupt mask registers

The interrupt mask registers are registers that individually specify whether to enable or mask the timer interrupt (2 Hz, 8 Hz, 32 Hz), stopwatch timer interrupt (1 Hz, 10 Hz), or input interrupt (K00–K03).

The following are descriptions of the interrupt mask registers.

EIK00 to EIK03 This register enables or masks the K00–K03 input interrupt. The interrupt condition flag (IK0) is set to "1" when the contents of the input (K00–K03) become "1" and the data of the corresponding interrupt mask register (EIK00–EIK03) is "1". The CPU is interrupted if it is in the EI state (interrupt flag [I] = "1"). (See Figure 3.9.1.)

<Input interrupt programing related precautions>



When the content of the mask register is rewritten, while the port K input is in the active status. The input interrupt factor flag is set at ①.

Fig. 3.9.4
Input interrupt timing

When using an input interrupt, if you rewrite the content of the mask register, when the value of the input terminal which becomes the interrupt input is in the active status (input terminal = high status), the factor flag for input interrupt may be set.
For example, a factor flag is set with the timing of ① shown in Figure 3.9.4. However, when clearing the content of the mask register with the input terminal kept in the high status and then setting it, the factor flag of the input interrupt is again set at the timing that has been set.

Consequently, when the input terminal is in the active status (high status), do not rewrite the mask register (clearing, then setting the mask register), so that a factor flag will only set at the rising edge in this case. When clearing, then setting the mask register, set the mask register, when the input terminal is not in the active status (low status).

EIT32 This register enables or masks the 32 Hz timer interrupt. The CPU is interrupted if it is in the EI state when the interrupt mask register (EIT32) is set to "1" and the interrupt condition flag (IT32) is "1". (See Figure 3.9.2.)

EIT8 This register enables or masks the 8 Hz timer interrupt. The CPU is interrupted if it is in the EI state when the interrupt mask register (EIT8) is set to "1" and the interrupt condition flag (IT8) is "1". (See Figure 3.9.2.)

EIT2 This register enables or masks the 2 Hz timer interrupt. The CPU is intterrupted if it is in the EI state when the interrupt mask register (EIT2) is set to "1" and the interrupt condition flag (IT2) is "1". (See Figure 3.9.2.)

EISW1 This register enables or masks the 1 Hz stopwatch interrupt. The CPU is interrupted if it is in the EI state when the interrupt mask register (EISW1) is set to "1", and also the interrupt condition flag (ISW1) is "1". (See Figure 3.9.3.)

EISW0 This register enables or masks the 10 Hz stopwatch interrupt. The CPU is interrupted if it is in the EI state when the interrupt mask register (EISW0) is set to "1", and the interrupt condition flag (ISW0) is "1". (See Figure 3.9.3.)

• Interrupt vector address

The E0C6S37 interrupt vector address is made up of the low-order 3 bits of the program counter (12 bits), each of which is assigned a specific function as shown in Figure 3.9.5.

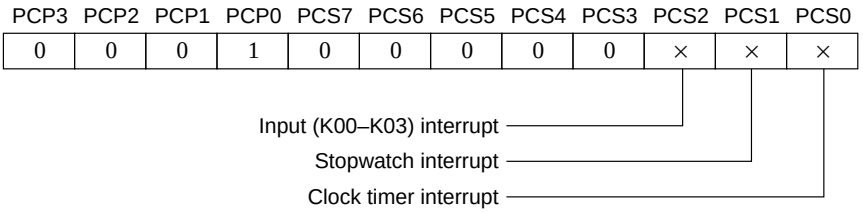


Fig. 3.9.5
Assignment of the interrupt vector address

Note that all of the three timer interrupts have the same vector address, and software must be used to judge whether or not a given timer interrupt has occurred. For instance, when the 32 Hz timer interrupt and the 8 Hz timer interrupt are enabled at the same time, the accepted timer interrupt must be identified by software. (Similarly, the K00–K03 input interrupts and the 10 Hz/1 Hz stopwatch interrupts must be identified by software.)

When an interrupt is generated, the hardware resets the interrupt flag (I) to enter the DI state. Execute the EI instruction as necessary to recover the EI state after interrupt processing.

Set the EI state at the start of the interrupt processing routine to allow nesting of the interrupts.

The interrupt factor flags must always be reset before setting the EI status in the corresponding interrupt processing routine. (The flag is reset when the interrupt condition flag is read by software.)

If the EI instruction is executed without resetting the interrupt factor flag after generating the timer interrupt or the stopwatch timer interrupt, and if the corresponding interrupt mask register is still "1", the same interrupt is generated once more. (See Figure 3.9.6.)

If the EI state is set without resetting the interrupt condition flag after generating the input interrupt (K00–K03), the same interrupt is generated once more. (See Figure 3.9.6.)

The interrupt factor flag must always be read (reset) in the DI state (interrupt flag [I] = "0"). There may be an operation error if read in the EI state.

The timer interrupt factor flags (IT32, IT8, IT2) and the stopwatch interrupt factor flags (ISW1, ISW0) are set whether the corresponding interrupt mask register is set or not.

The input interrupt factor flag (IK0) is allowed to be set in the condition when the corresponding interrupt mask register (EIK00–EIK03) is set to "1" (interrupt is enabled). (See Figure 3.9.6.)

Table 3.9.2 shows the interrupt vector map.

Table 3.9.2
Interrupt vector map

Page	Step	Interrupt vector
1	00H	Initial reset
	01H	Clock timer interrupt
	02H	Stopwatch interrupt
	03H	Clock timer interrupt and stopwatch interrupt
	04H	Input (K00–K03) interrupt
	05H	Input interrupt and clock timer interrupt
	06H	Input interrupt and stopwatch interrupt
	07H	Generation of all interrupt

Addesses (start address of interrupt processing routines) to jump to are written into the addresses available for interrupt vector allocation.

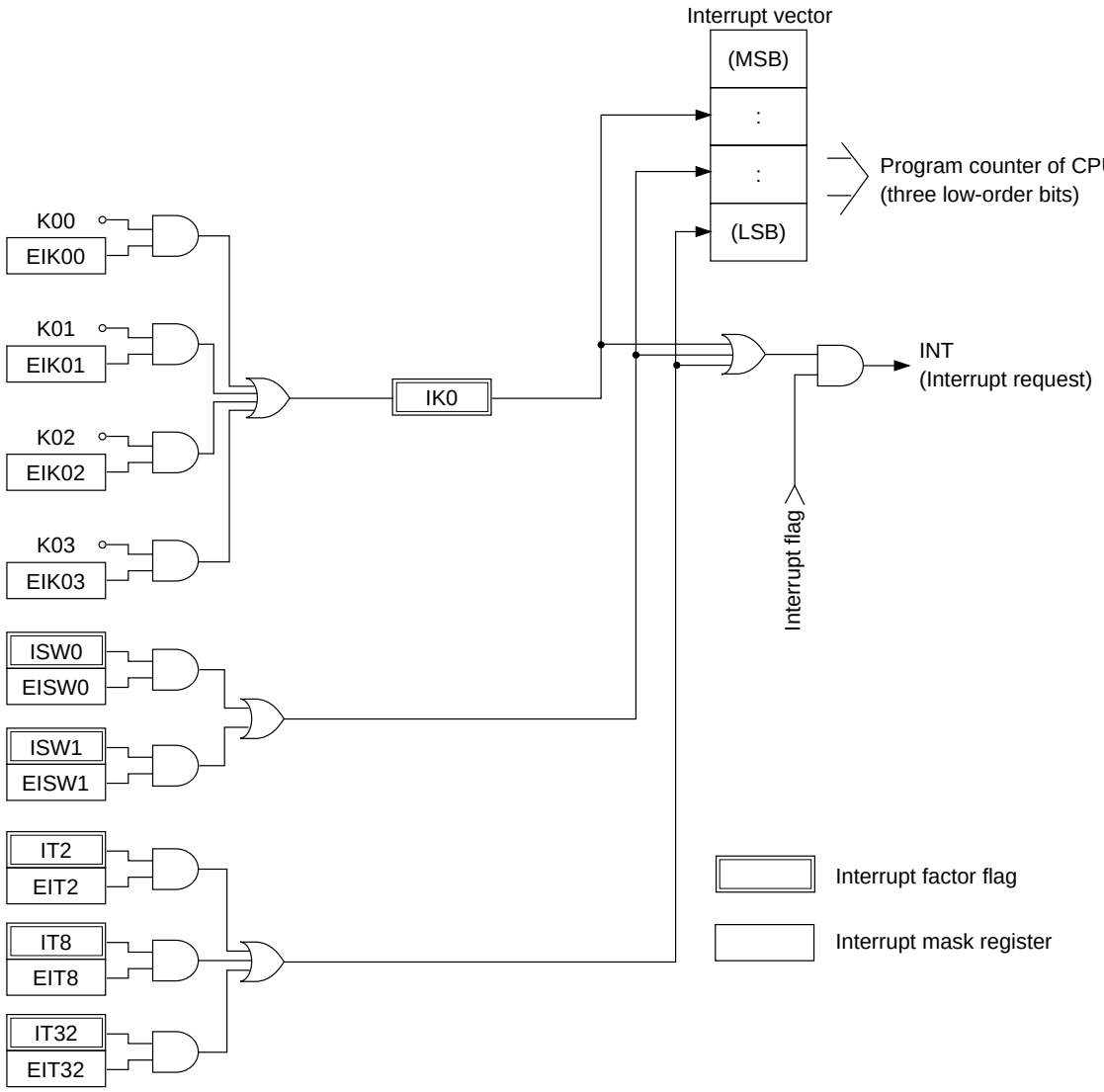


Fig. 3.9.6
Internal interrupt circuit

Examples of interrupt and halt control program

• Restart from halt state by interrupt

Main routine

```
Label   Mnemonic/operand        Comment
        LD      X,0E8H          ;Set address of K00 to K03
                                ;interrupt mask register
        OR      MX,1111B        ;Enable K00 to K03
                                ;input interrupt
;
        LD      X,0EAH          ;Set address of stopwatch
                                ;interrupt mask register
        OR      MX,0011B        ;Enable 1 Hz, 10 Hz stopwatch interrupt
;
        LD      X,0EBH          ;Set address of timer interrupt
                                ;mask register
        OR      MX,0111B        ;Enable timer interrupt
                                ;(32 Hz, 8 Hz, 2 Hz)
MAIN:   EI                      ;Set interrupt flag (EI state is set)
        HALT                    ;Halt mode
        JP      MAIN            ;Jump to MAIN
```

Interruption vector routine

```
Label     Mnemonic/operand     Comment
          ORG     100H
          JP      INIT
          JP      INTR      ;Timer interrupt is generated
          JP      INTR      ;Stopwatch interrupt is generated
          JP      INTR      ;Timer interrupt, stopwatch interrupt
                            ;are generated
          JP      INTR      ;K00 to K03 interrupt is generated
          JP      INTR      ;Timer interrupt, K00 to K03 interrupt
                            ;are generated
          JP      INTR      ;Stopwatch interrupt, K00 to K03 interrupt
                            ;are generated
          JP      INTR      ;Timer interrupt, stopwatch interrupt,
                            ;K00 to K03 interrupt are generated
;
INTR:     LD      X,0EFH    ;Address of timer interrupt factor flag
          LD      Y,TMFSK   ;Address of timer interrupt factor flag buffer
          LD      MY,MX
          FAN     MY,0100B  ;Check 2 Hz timer interrupt
          JP      Z,TI8RQ   ;Jump if not 2 Hz timer interrupt
          CALL    TINT2     ;Call 2 Hz timer interrupt service routine
TI8RQ:
          LD      Y,TMFSK   ;Address of timer factor flag buffer
          FAN     MY,0010B  ;Check 8 Hz timer interrupt
          JP      Z,TI32RQ  ;Jump if not 8 Hz timer interrupt
          CALL    TINT8     ;Call 8 Hz timer interrupt service routine
TI32RQ:
          LD      Y,TMFSK   ;Address of timer factor flag buffer
          FAN     MY,0001B  ;Check 8 Hz timer interrupt
          JP      Z,SW1RQ   ;Jump if not 32 Hz timer interrupt
          CALL    TINT32    ;Call 32 Hz timer interrupt service routine
SW1RQ:
          LD      X,0EEH    ;Address of stopwatch interrupt factor flag
          LD      Y,SWFSK   ;Address of stopwatch interrupt
                            ;factor flag buffer
          FAN     MY,0010B  ;Check 1 Hz stopwatch interrupt
          JP      Z,SW10RQ  ;Jump if not 1 Hz stopwatch interrupt
```

```
        CALL    SW1IN       ;Call 1 Hz stopwatch interrupt service routine
SW10RQ:
        LD      Y,SWFSK     ;Address of stopwatch interrupt
                            ;factor flag buffer
        FAN     MY,0010B    ;Check 10 Hz stopwatch interrupt
        JP      Z,IK0RQ     ;Jump if not 10 Hz stopwatch interrupt
        CALL    SW10IN      ;Call 10 Hz stopwatch interrupt service
                            ;routine
IK0RQ:
        LD      X,0EDH      ;Address of K00 to K03 input interrupt flag
        FAN     MX,0001B    ;Check K00 to K03 input interrupt
        JP      Z,INTEND    ;Jump if not K00 to K03 input interrupt
        CALL    IK0INT      ;Call K00 to K03 input interrupt service
                            ;routine
INTEND:
        EI
        RET
```

The above program is normally used to restart the CPU when in the halt state by interrupt and to return it to the halt state again after the interrupt processing is completed. The processing proceeds by repeating the → halt interrupt → halt → interrupt cycle.

The interrupt factor flag is reset when load by the software.

Thus, when using interrupts which interrupt factor flags are in the same address at the same time, flag check must be done after storing the data. For example, store the 1 word including the factor flag in the RAM. (If check is directly done by the FAN instruction, the factor flags of the same address are all reset.)

Reading of interrupt factor flags is available at EI, but be careful in the following cases.
If the interrupt mask register value corresponding to the interrupt factor flags to be read is set to "1", an interrupt request will be generated by the interrupt factor flags set timing, or an interrupt request will not be generated.

CHAPTER 4 SUMMARY OF PROGRAMMING POINTS

- **Core CPU**

  After the system reset, only the program counter (PC), new page pointer (NPP) and interrupt flag (I) are initialized by the hardware. The other internal circuits whose settings are undefined must be initialized with the program.

- **Power Supply**

  External load driving through the output voltage of constant voltage circuit or voltage booster/reducer is not permitted.

- **Data Memory**

  – Since some portions of the RAM are also used as stack area during sub-routine call or register saving, see to it that the data area and the stack area do not overlap.

  – The stack area consumes 3 words during a sub-routine call or interrupt.

  – Address 00H–0FH in the RAM is the memory register area addressed by the register pointer RP.

  – Memory is not mounted in unused area within the memory map and in memory area not indicated in this manual. For this reason, normal operation cannot be assured for programs that have been prepared with access to these areas.

- **Initial Reset**

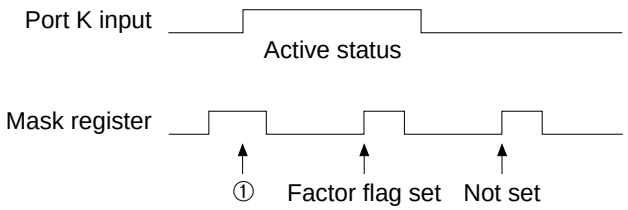
  – Maintain the initial reset circuit at high level for at least 4 seconds (in case of oscillation frequency fosc = 32 kHz) because noise rejector is built-in.

  – When utilizing the simultaneous high input reset function of the input ports (K00–K03), take care not to make the ports specified during normal operation to go high simultaneously.

- **Input Port**

  – When modifying the input port from high level to low level with pull-down resistance, a delay will occur at the rise of the waveform due to time constant of the pull-down resistance and input gate capacities. Provide appropriate waiting time in the program when performing input port reading.

  – Input interrupt programing related precautions



When the content of the mask register is rewritten, while the port K input is in the active status. The input interrupt factor flag is set at ①.

Fig. 4.1
Input interrupt timing

When using an input interrupt, if you rewrite the content of the mask register, when the value of the input terminal which becomes the interrupt input is in the active status (input terminal = high status), the factor flag for input interrupt may be set.
For example, a factor flag is set with the timing of ① shown in Figure 4.1. However, when clearing the content of the mask register with the input terminal kept in the high status and then setting it, the factor flag of the input interrupt is again set at the timing that has been set. Consequently, when the input terminal is in the active status (high status), do not rewrite the mask register (clearing, then setting the mask register), so that a factor flag will only set at the rising edge in this case. When clearing, then setting the mask register, set the mask register, when the input terminal is not in the active status (low status).

- **Output Port**

  The FOUT and BUZZER output signal may produce hazards when the output ports R00 and R01 are turned on or off.

- **I/O Port**
  - When the I/O port is set to the output mode and a low-impedance load is connected to the port pin, the data written to the register may differ from the data read.
  - When the I/O port is set to the input mode and a low-level voltage (VSS) is input by the built-in pull-down resistance, an erroneous input results if the time constant of the capacitive load of the input line and the built-in pull-down resistance load is greater than the read-out time. When the input data is being read, the time that the input line is pulled down is equivalent to 0.5 cycles of the CPU system clock.
    Hence, the electric potential of the pins must settle within 0.5 cycles. If this condition cannot be met, some measure must be devised, such as arranging a pull-down resistance externally, or performing multiple read-outs.

- **LCD Driver**
  - Because the display memory is for writing only, re-writing the contents with computing instructions (e.g., AND, OR, etc.) which come with read-out operations is not possible. To perform bit operations, a buffer to hold the display data is required on the RAM.
  - Even when 1/2 duty is selected, the display data corresponding to COM0, COM3 are valid for static drive. Hence, for static drive set the same value to all display memory corresponding COM0–COM3.
  - Even when 1/3 duty is selected, the display data corresponding to COM3 is valid for static drive. Hence, for static drive set the same value to all display memory corresponding COM0–COM3.
  - For cadence adjustment, set the display data including display data corresponding to COM3.
  - fosc indicates the oscillation frequency of the oscillation circuit.

- **Supply Voltage Detection (SVD) Circuit**

  Since supply voltage detection is automatically performed by the hardware every 2 Hz (0.5 sec) when the heavy load protection function operates, do not permit the operation of the SVD circuit by the software in order to minimize power current consumption.

- **Heavy Load Protection Function**

  In the heavy load protection function (heavy load protection mode flag = "1"), supply voltage detection through the SVDON register is not permitted in order to minimize power current consumption.

- **Interrupt**

  – Re-start from the HALT state is performed by the interrupt. The return address after completion of the interrupt processing in this case will be the address following the HALT instruction.

  – When interrupt occurs, the interrupt flag will be reset by the hardware and it will become DI state. After completion of the interrupt processing, set to the EI state through the software as needed.
  Moreover, the nesting level may be set to be programmable by setting to the EI state at the beginning of the interrupt processing routine.

  – Be sure to reset the interrupt factor flag before setting to the EI state on the interrupt processing routine. The interrupt factor flag is reset by reading through the software. Not resetting the interrupt factor flag and interrupt mask register being "1", will cause the same interrupt to occur again.

  – The interrupt factor flag will be reset by reading through the software. Because of this, when multiple interrupt factor flags are to be assigned to the same address, perform the flag check after the contents of the address has been stored in the RAM. Direct checking with the FAN instruction will cause all the interrupt factor flag to be reset.

  – Reading of interrupt factor flags is available at EI, but be careful in the following cases.
  If the interrupt mask register value corresponding to the interrupt factor flags to be read is set to "1", an interrupt request will be generated by the interrupt factor flags set timing, or an interrupt request will not be generated.

- **Vacant Register and Read/Write**

  Writing data into the addresses where read/write bits and read only bits are mixed in 1 word (4 bits) does not affect the read only bits.

APPENDIX A Table of Instructions

Classification	Mne-monic	Operand	Operation Code												Flag				Clock	Operation
			B	A	9	8	7	6	5	4	3	2	1	0	I	D	Z	C		
Branch instructions	PSET	p	1	1	1	0	0	1	0	p4	p3	p2	p1	p0					5	NBP ← p4, NPP ← p3~p0
	JP	s	0	0	0	0	s7	s6	s5	s4	s3	s2	s1	s0					5	PCB ← NBP, PCP ← NPP, PCS ← s7~s0
		C, s	0	0	1	0	s7	s6	s5	s4	s3	s2	s1	s0					5	PCB ← NBP, PCP ← NPP, PCS ← s7~s0 if C=1
		NC, s	0	0	1	1	s7	s6	s5	s4	s3	s2	s1	s0					5	PCB ← NBP, PCP ← NPP, PCS ← s7~s0 if C=0
		Z, s	0	1	1	0	s7	s6	s5	s4	s3	s2	s1	s0					5	PCB ← NBP, PCP ← NPP, PCS ← s7~s0 if Z=1
		NZ, s	0	1	1	1	s7	s6	s5	s4	s3	s2	s1	s0					5	PCB ← NBP, PCP ← NPP, PCS ← s7~s0 if Z=0
	JPBA		1	1	1	1	1	1	1	0	1	0	0	0					5	PCB ← NBP, PCP ← NPP, PCSH ← B, PCSL ← A
	CALL	s	0	1	0	0	s7	s6	s5	s4	s3	s2	s1	s0					7	M(SP-1) ← PCP, M(SP-2) ← PCSH, M(SP-3) ← PCSL+1 SP ← SP-3, PCP ← NPP, PCS ← s7~s0
	CALZ	s	0	1	0	1	s7	s6	s5	s4	s3	s2	s1	s0					7	M(SP-1) ← PCP, M(SP-2) ← PCSH, M(SP-3) ← PCSL+1 SP ← SP-3, PCP ← 0, PCS ← s7~s0
	RET		1	1	1	1	1	1	0	1	1	1	1	1					7	PCSL ← M(SP), PCSH ← M(SP+1), PCP ← M(SP+2) SP ← SP+3
	RETS		1	1	1	1	1	1	0	1	1	1	1	0					12	PCSL ← M(SP), PCSH ← M(SP+1), PCP ← M(SP+2) SP ← SP+3, PC ← PC+1
	RETD	l	0	0	0	1	l7	l6	l5	l4	l3	l2	l1	l0					12	PCSL ← M(SP), PCSH ← M(SP+1), PCP ← M(SP+2) SP ← SP+3, M(X) ← i3~i0, M(X+1) ← l7~l4, X ← X+2
System control instructions	NOP5		1	1	1	1	1	1	1	1	1	0	1	1					5	No operation (5 clock cycles)
	NOP7		1	1	1	1	1	1	1	1	1	1	1	1					7	No operation (7 clock cycles)
	HALT		1	1	1	1	1	1	1	1	1	0	0	0					5	Halt (stop clock)
Index operation instructions	INC	X	1	1	1	0	1	1	1	0	0	0	0	0					5	X ← X+1
		Y	1	1	1	0	1	1	1	1	0	0	0	0					5	Y ← Y+1
	LD	X, x	1	0	1	1	x7	x6	x5	x4	x3	x2	x1	x0					5	XH ← x7~x4, XL ← x3~x0
		Y, y	1	0	0	0	y7	y6	y5	y4	y3	y2	y1	y0					5	YH ← y7~y4, YL ← y3~y0
		XH, r	1	1	1	0	1	0	0	0	0	1	r1	r0					5	XH ← r
		XL, r	1	1	1	0	1	0	0	0	1	0	r1	r0					5	XL ← r
		YH, r	1	1	1	0	1	0	0	1	0	1	r1	r0					5	YH ← r
		YL, r	1	1	1	0	1	0	0	1	1	0	r1	r0					5	YL ← r
		r, XH	1	1	1	0	1	0	1	0	0	1	r1	r0					5	r ← XH
		r, XL	1	1	1	0	1	0	1	0	1	0	r1	r0					5	r ← XL
		r, YH	1	1	1	0	1	0	1	1	0	1	r1	r0					5	r ← YH
		r, YL	1	1	1	0	1	0	1	1	1	0	r1	r0					5	r ← YL
	ADC	XH, i	1	0	1	0	0	0	0	0	i3	i2	i1	i0			↕	↕	7	XH ← XH+i3~i0+C
		XL, i	1	0	1	0	0	0	0	1	i3	i2	i1	i0			↕	↕	7	XL ← XL+i3~i0+C
		YH, i	1	0	1	0	0	0	1	0	i3	i2	i1	i0			↕	↕	7	YH ← YH+i3~i0+C
		YL, i	1	0	1	0	0	0	1	1	i3	i2	i1	i0			↕	↕	7	YL ← YL+i3~i0+C

Classification	Mnemonic	Operand	Operation Code												Flag				Clock	Operation
			B	A	9	8	7	6	5	4	3	2	1	0	I	D	Z	C		
Index operation instructions	CP	XH, i	1	0	1	0	0	1	0	0	i3	i2	i1	i0			↕	↕	7	XH-i3~i0
		XL, i	1	0	1	0	0	1	0	1	i3	i2	i1	i0			↕	↕	7	XL-i3~i0
		YH, i	1	0	1	0	0	1	1	0	i3	i2	i1	i0			↕	↕	7	YH-i3~i0
		YL, i	1	0	1	0	0	1	1	1	i3	i2	i1	i0			↕	↕	7	YL-i3~i0
Data transfer instructions	LD	r, i	1	1	1	0	0	0	r1	r0	i3	i2	i1	i0					5	r←i3~i0
		r, q	1	1	1	0	1	1	0	0	r1	r0	q1	q0					5	r←q
		A, Mn	1	1	1	1	1	0	1	0	n3	n2	n1	n0					5	A←M(n3~n0)
		B, Mn	1	1	1	1	1	0	1	1	n3	n2	n1	n0					5	B←M(n3~n0)
		Mn, A	1	1	1	1	1	0	0	0	n3	n2	n1	n0					5	M(n3~n0)←A
		Mn, B	1	1	1	1	1	0	0	1	n3	n2	n1	n0					5	M(n3~n0)←B
	LDPX	MX, i	1	1	1	0	0	1	1	0	i3	i2	i1	i0					5	M(X)←i3~i0, X←X+1
		r, q	1	1	1	0	1	1	1	0	r1	r0	q1	q0					5	r←q, X←X+1
	LDPY	MY, i	1	1	1	0	0	1	1	1	i3	i2	i1	i0					5	M(Y)←i3~i0, Y←Y+1
		r, q	1	1	1	0	1	1	1	1	r1	r0	q1	q0					5	r←q, Y←Y+1
	LBPX	MX, l	1	0	0	1	l7	l6	l5	l4	l3	l2	l1	l0					5	M(X)←l3~l0, M(X+1)←l7~l4, X←X+2
Flag operation instructions	SET	F, i	1	1	1	1	0	1	0	0	i3	i2	i1	i0	↑	↑	↑	↑	7	F←F∨i3~i0
	RST	F, i	1	1	1	1	0	1	0	1	i3	i2	i1	i0	↓	↓	↓	↓	7	F←F∧i3~i0
	SCF		1	1	1	1	0	1	0	0	0	0	0	1				↑	7	C←1
	RCF		1	1	1	1	0	1	0	1	1	1	1	0				↓	7	C←0
	SZF		1	1	1	1	0	1	0	0	0	0	1	0			↑		7	Z←1
	RZF		1	1	1	1	0	1	0	1	1	1	0	1			↓		7	Z←0
	SDF		1	1	1	1	0	1	0	0	0	1	0	0		↑			7	D←1 (Decimal Adjuster ON)
	RDF		1	1	1	1	0	1	0	1	1	0	1	1		↓			7	D←0 (Decimal Adjuster OFF)
	EI		1	1	1	1	0	1	0	0	1	0	0	0	↑				7	I ←1 (Enables Interrupt)
	DI		1	1	1	1	0	1	0	1	0	1	1	1	↓				7	I ←0 (Disables Interrupt)
Stack operation instructions	INC	SP	1	1	1	1	1	1	0	1	1	0	1	1					5	SP← SP+1
	DEC	SP	1	1	1	1	1	1	0	0	1	0	1	1					5	SP← SP-1
	PUSH	r	1	1	1	1	1	1	0	0	0	0	r1	r0					5	SP← SP-1, M(SP)←r
		XH	1	1	1	1	1	1	0	0	0	1	0	1					5	SP← SP-1, M(SP)←XH
		XL	1	1	1	1	1	1	0	0	0	1	1	0					5	SP← SP-1, M(SP)←XL
		YH	1	1	1	1	1	1	0	0	1	0	0	0					5	SP← SP-1, M(SP)←YH
		YL	1	1	1	1	1	1	0	0	1	0	0	1					5	SP← SP-1, M(SP)←YL
		F	1	1	1	1	1	1	0	0	1	0	1	0					5	SP← SP-1, M(SP)←F
	POP	r	1	1	1	1	1	1	0	1	0	0	r1	r0					5	r←M(SP), SP←SP+1
		XH	1	1	1	1	1	1	0	1	0	1	0	1					5	XH←M(SP), SP←SP+1
		XL	1	1	1	1	1	1	0	1	0	1	1	0					5	XL←M(SP), SP←SP+1

Classification	Mne-monic	Operand	Operation Code												Flag				Clock	Operation
			B	A	9	8	7	6	5	4	3	2	1	0	I	D	Z	C		
Stack operation instructions	POP	YH	1	1	1	1	1	1	0	1	1	0	0	0					5	YH← M(SP), SP← SP+1
		YL	1	1	1	1	1	1	0	1	1	0	0	1					5	YL ← M(SP), SP ← SP+1
		F	1	1	1	1	1	1	0	1	1	0	1	0	↕	↕	↕	↕	5	F← M(SP), SP ← SP+1
	LD	SPH, r	1	1	1	1	1	1	1	0	0	0	r1	r0					5	SPH← r
		SPL, r	1	1	1	1	1	1	1	1	0	0	r1	r0					5	SPL ← r
		r, SPH	1	1	1	1	1	1	1	0	0	1	r1	r0					5	r← SPH
		r, SPL	1	1	1	1	1	1	1	1	0	1	r1	r0					5	r← SPL
Arithmetic instructions	ADD	r, i	1	1	0	0	0	0	r1	r0	i3	i2	i1	i0	★	↕	↕		7	r← r+i3~i0
		r, q	1	0	1	0	1	0	0	0	r1	r0	q1	q0	★	↕	↕		7	r← r+q
	ADC	r, i	1	1	0	0	0	1	r1	r0	i3	i2	i1	i0	★	↕	↕		7	r← r+i3~i0+C
		r, q	1	0	1	0	1	0	0	1	r1	r0	q1	q0	★	↕	↕		7	r← r+q+C
	SUB	r, q	1	0	1	0	1	0	1	0	r1	r0	q1	q0	★	↕	↕		7	r← r-q
	SBC	r, i	1	1	0	1	0	1	r1	r0	i3	i2	i1	i0	★	↕	↕		7	r← r-i3~i0-C
		r, q	1	0	1	0	1	0	1	1	r1	r0	q1	q0	★	↕	↕		7	r← r-q-C
	AND	r, i	1	1	0	0	1	0	r1	r0	i3	i2	i1	i0		↕			7	r← r∧ i3~i0
		r, q	1	0	1	0	1	1	0	0	r1	r0	q1	q0		↕			7	r← r∧ q
	OR	r, i	1	1	0	0	1	1	r1	r0	i3	i2	i1	i0		↕			7	r← r∨i3~i0
		r, q	1	0	1	0	1	1	0	1	r1	r0	q1	q0		↕			7	r← r∨q
	XOR	r, i	1	1	0	1	0	0	r1	r0	i3	i2	i1	i0		↕			7	r← r∀i3~i0
		r, q	1	0	1	0	1	1	1	0	r1	r0	q1	q0		↕			7	r← r∀q
	CP	r, i	1	1	0	1	1	1	r1	r0	i3	i2	i1	i0		↕	↕		7	r-i3~i0
		r, q	1	1	1	1	0	0	0	0	r1	r0	q1	q0		↕	↕		7	r-q
	FAN	r, i	1	1	0	1	1	0	r1	r0	i3	i2	i1	i0		↕			7	r∧i3~i0
		r, q	1	1	1	1	0	0	0	1	r1	r0	q1	q0		↕			7	r∧q
	RLC	r	1	0	1	0	1	1	1	1	r1	r0	r1	r0		↕	↕		7	d3← d2, d2 ← d1, d1 ← d0, d0 ←C, C← d3
	RRC	r	1	1	1	0	1	0	0	0	1	1	r1	r0		↕	↕		5	d3← C, d2 ← d3, d1 ← d2, d0 ← d1, C← d0
	INC	Mn	1	1	1	1	0	1	1	0	n3	n2	n1	n0		↕	↕		7	M(n3~n0) ← M(n3~n0)+1
	DEC	Mn	1	1	1	1	0	1	1	1	n3	n2	n1	n0		↕	↕		7	M(n3~n0) ← M(n3~n0)-1
	ACPX	MX, r	1	1	1	1	0	0	1	0	1	0	r1	r0	★	↕	↕		7	M(X) ← M(X)+r+C, X ← X+1
	ACPY	MY, r	1	1	1	1	0	0	1	0	1	1	r1	r0	★	↕	↕		7	M(Y) ← M(Y)+r+C, Y ← Y+1
	SCPX	MX, r	1	1	1	1	0	0	1	1	1	0	r1	r0	★	↕	↕		7	M(X) ← M(X)-r-C, X ← X+1
	SCPY	MY, r	1	1	1	1	0	0	1	1	1	1	r1	r0	★	↕	↕		7	M(Y) ← M(Y)-r-C, Y ← Y+1
	NOT	r	1	1	0	1	0	0	r1	r0	1	1	1	1		↕			7	r← $\overline{r}$

Abbreviations used in the explanations have the following meanings.

Symbols associated with registers and memory

A ..... A register
B ..... B register
X ..... XHL register (low order eight bits of index register IX)
Y ..... YHL register (low order eight bits of index register IY)
XH ..... XH register (high order four bits of XHL register)
XL ..... XL register (low order four bits of XHL register)
YH ..... YH register (high order four bits of YHL register)
YL ..... YL register (low order four bits of YHL register)
XP ..... XP register (high order four bits of index register IX)
YP ..... YP register (high order four bits of index register IY)
SP ..... Stack pointer SP
SPH ..... High-order four bits of stack pointer SP
SPL ..... Low-order four bits of stack pointer SP
MX, M(X) .. Data memory whose address is specified with index register IX
MY, M(Y)... Data memory whose address is specified with index register IY
Mn, M(n) .. Data memory address 000H–00FH (address specified with immediate data n of 00H–0FH)
M(SP) ..... Data memory whose address is specified with stack pointer SP
r, q ..... Two-bit register code
r, q is two-bit immediate data; according to the contents of these bits, they indicate registers A, B, and MX and MY (data memory whose addresses are specified with index registers IX and IY)

r		q		Registers specified
r1	r0	q1	q0	
0	0	0	0	A
0	1	0	1	B
1	0	1	0	MX
1	1	1	1	MY

Symbols associated with program counter

NBP ..... New bank pointer
NPP ..... New page pointer
PCB ..... Program counter bank
PCP ..... Program counter page
PCS ..... Program counter step
PCSH .. Four high order bits of PCS
PCSL ... Four low order bits of PCS

Symbols associated with flags

F ..... Flag register (I, D, Z, C)
C ..... Carry flag
Z ..... Zero flag
D ..... Decimal flag
I ..... Interrupt flag
↓ ..... Flag reset
↑ ..... Flag set
↕ ..... Flag set or reset

Associated with immediate data

p ..... Five-bit immediate data or label 00H–1FH
s ..... Eight-bit immediate data or label 00H–0FFH
l ..... Eight-bit immediate data 00H–0FFH
i ..... Four-bit immediate data 00H–0FH

Associated with arithmetic and other operations

+ ..... Add
- ..... Subtract
∧ ..... Logical AND
∨ ..... Logical OR
∀ ..... Exclusive-OR
★ ..... Add-subtract instruction for decimal operation when the D flag is set

APPENDIX B The E0C6S37 I/O Memory Map

ADDRESS	DATA								COMMENT
	D3	D2	D1	D0	NAME	SR	1	0	
E0	K03	K02	K01	K00	K03	–	HIGH	LOW	INPORT DATA K03
	R	R	R	R	K02	–	HIGH	LOW	INPORT DATA K02
					K01	–	HIGH	LOW	INPORT DATA K01
					K00	–	HIGH	LOW	INPORT DATA K00
E2	SWL3	SWL2	SWL1	SWL0	SWL3	0	–	–	STOPWATCH TIMER DATA 3 (1/100) MSB
	R	R	R	R	SWL2	0	–	–	STOPWATCH TIMER DATA 2 (1/100)
					SWL1	0	–	–	STOPWATCH TIMER DATA 1 (1/100)
					SWL0	0	–	–	STOPWATCH TIMER DATA 0 (1/100) LSB
E3	SWH3	SWH2	SWH1	SWH0	SWH3	0	–	–	STOPWATCH TIMER DATA 3 (1/10) MSB
	R	R	R	R	SWH2	0	–	–	STOPWATCH TIMER DATA 2 (1/10)
					SWH1	0	–	–	STOPWATCH TIMER DATA 1 (1/10)
					SWH0	0	–	–	STOPWATCH TIMER DATA 0 (1/10) LSB
E4	TM3	TM2	TM1	TM0	TM3	–	HIGH	LOW	CLOCK TIMER DATA 2 Hz
	R	R	R	R	TM2	–	HIGH	LOW	CLOCK TIMER DATA 4 Hz
					TM1	–	HIGH	LOW	CLOCK TIMER DATA 8 Hz
					TM0	–	HIGH	LOW	CLOCK TIMER DATA 16 Hz
E8	EIK03	EIK02	EIK01	EIK00	EIK03	0	ENABLE	MASK	K03 INTERRUPT MASK REGISTER
	R/W	R/W	R/W	R/W	EIK02	0	ENABLE	MASK	K02 INTERRUPT MASK REGISTER
					EIK01	0	ENABLE	MASK	K01 INTERRUPT MASK REGISTER
					EIK00	0	ENABLE	MASK	K00 INTERRUPT MASK REGISTER
EA	0	0	EISW1	EISW0	0	–	–	–	
	R	R	R/W	R/W	0	–	–	–	
					EISW1	0	ENABLE	MASK	S/W INTERRUPT MASK REGISTER 1 Hz
					EISW0	0	ENABLE	MASK	S/W INTERRUPT MASK REGISTER 10 Hz
EB	0	EIT2	EIT8	EIT32	0	–	–	–	
	R	R/W	R/W	R/W	EIT2	0	ENABLE	MASK	TIMER INTERRUPT MASK REGISTER 2 Hz
					EIT8	0	ENABLE	MASK	TIMER INTERRUPT MASK REGISTER 8 Hz
					EIT32	0	ENABLE	MASK	TIMER INTERRUPT MASK REGISTER 32 Hz
ED	0	0	0	IK0	0	–	–	–	
	R	R	R	R	0	–	–	–	
					0	–	–	–	
					IK0	0	YES	NO	K00–K03 INTERRUPT FACTOR FLAG
EE	0	0	ISW1	ISW0	0	–	–	–	
	R	R	R	R	0	–	–	–	
					ISW1	0	YES	NO	S/W INTERRUPT FACTOR FLAG 1 Hz
					ISW0	0	YES	NO	S/W INTERRUPT FACTOR FLAG 10 Hz
EF	0	IT2	IT8	IT32	0	–	–	–	
	R	R	R	R	IT2	0	YES	NO	TIMER INTERRUPT FACTOR FLAG 2 Hz
					IT8	0	YES	NO	TIMER INTERRUPT FACTOR FLAG 8 Hz
					IT32	0	YES	NO	TIMER INTERRUPT FACTOR FLAG 32 Hz

AD-DRESS	DATA								COMMENT
	D3	D2	D1	D0	NAME	SR	1	0	
F3	R03	R02	R01	R00	R03	0	HIGH	LOW	R03 OUTPUT PORT DATA
			BUZZER	FOUT	R02	0	HIGH	LOW	R02 OUTPUT PORT DATA
	R/W	R/W	R/W	R/W	R01	0	HIGH	LOW	R01 OUTPUT PORT DATA
					BUZZER	0	ON	OFF	BUZZER ON/OFF CONTROL REGISTER
					R00	0	HIGH	LOW	R00 OUTPUT PORT DATA
					FOUT	0	ON	OFF	FREQUENCY OUTPUT ON/OFF CONTROL REGISTER
F6	P03	P02	P01	P00	P03	–	HIGH	LOW	P03 I/O PORT DATA
	R/W	R/W	R/W	R/W	P02	–	HIGH	LOW	P02 I/O PORT DATA
					P01	–	HIGH	LOW	P01 I/O PORT DATA
					P00	–	HIGH	LOW	P00 I/O PORT DATA
F9	0	TMRST	SWRUN	SWRST	0	–	–	–	
	R	W	R/W	W	TMRST	RESET	RESET	–	TIMER RESET
					SWRUN	0	RUN	STOP	STOPWATCH RUN/STOP CONTROL REG.
					SWRST	RESET	RESET	–	STOPWATCH RESET
FA	HLMOD	0	SVDDT	SVDON	HLMOD	0	HEAVY	NORMAL	HEAVY LOAD PROTECTION MODE
	R/W	R	R	R/W	0	–	–	–	
					SVDDT	0	LOW	NORMAL	SVD DATA
					SVDON	0	ON	OFF	SVD ON-OFF CONTROL REGISTER
FB	CSDC	0	0	0	CSDC	0	STATIC	DYNAMIC	LCD DRIVER CONTROL REG.
	R/W	R	R	R	0	–	–	–	
					0	–	–	–	
					0	–	–	–	
FC	0	0	0	IOC	0	–	–	–	
	R	R	R	R/W	0	–	–	–	
					0	–	–	–	
					IOC	0	OUT	IN	I/O IN-OUT CONTROL REG.
FD	XBZR	0	XFOUT1	XFOUT0	XBZR	0	2 kHz	4 kHz	BUZZER FREQUENCY CONTROL
	R/W	R	R/W	R/W	0	–	–	–	
					XFOUT1	0	HIGH	LOW	FOUT FREQUENCY CONTROL:
					XFOUT0	0	HIGH	LOW	XFOUT1(0), XFOUT0(0) -> F1
									XFOUT1(0), XFOUT0(1) -> F2
									XFOUT1(1), XFOUT0(0) -> F3
									XFOUT1(1), XFOUT0(1) -> F4

APPENDIX C Table of the ICE6200 Commands

Item No.	Function	Command Format	Outline of Operation
1	Assemble	#A,a ↵	Assemble command mnemonic code and store at address "a"
2	Disassemble	#L,a1,a2 ↵	Contents of addresses a1 to a2 are disassembled and displayed
3	Dump	#DP,a1,a2 ↵	Contents of program area a1 to a2 are displayed
		#DD,a1,a2 ↵	Content of data area a1 to a2 are displayed
4	Fill	#FP,a1,a2,d ↵	Data d is set in addresses a1 to a2 (program area)
		#FD,a1,a2,d ↵	Data d is set in addresses a1 to a2 (data area)
5	Set Run Mode	#G,a ↵	Program is executed from the "a" address
		#TIM ↵	Execution time and step counter selection
		#OTF ↵	On-the-fly display selection
6	Trace	#T,a,n ↵	Executes program while displaying results of step instruction from "a" address
		#U,a,n ↵	Displays only the final step of #T,a,n
7	Break	#BA,a ↵	Sets Break at program address "a"
		#BAR,a ↵	Breakpoint is canceled
		#BD ↵	Break condition is set for data RAM
		#BDR ↵	Breakpoint is canceled
		#BR ↵	Break condition is set for EVA62XX CPU internal registers
		#BRR ↵	Breakpoint is canceled
		#BM ↵	Combined break conditions set for program data RAM address and registers
		#BMR ↵	Cancel combined break conditions for program data ROM address and registers
		#BRES ↵	All break conditions canceled
		#BC ↵	Break condition displayed
		#BE ↵	Enter break enable mode
		#BSYN ↵	Enter break disable mode
		#BT ↵	Set break stop/trace modes
		#BRKSEL,REM ↵	Set BA condition clear/remain modes
8	Move	#MP,a1,a2,a3 ↵	Contents of program area addresses a1 to a2 are moved to addresses a3 and after
		#MD,a1,a2,a3 ↵	Contents of data area addresses a1 to a2 are moved to addresses a3 and after
9	Data Set	#SP,a ↵	Data from program area address "a" are written to memory
		#SD,a ↵	Data from data area address "a" are written to memory
10	Change CPU Internal Registers	#DR ↵	Display EVA62XX CPU internal registers
		#SR ↵	Set EVA62XX CPU internal registers
		#I ↵	Reset EVA62XX CPU
		#DXY ↵	Display X, Y, MX and MY
		#SXY ↵	Set data for X and Y display and MX, MY

Item No.	Function	Command Format	Outline of Operation
11	History	#H,p1,p2 ↵	Display history data for pointer 1 and pointer 2
		#HB ↵	Display upstream history data
		#HG ↵	Display 21 line history data
		#HP ↵	Display history pointer
		#HPS,a ↵	Set history pointer
		#HC,S/C/E ↵	Sets up the history information acquisition before (S), before/after (C) and after (E)
		#HA,a1,a2 ↵	Sets up the history information acquisition from program area a1 to a2
		#HAR,a1,a2 ↵	Sets up the prohibition of the history information acquisition from program area a1 to a2
		#HAD ↵	Indicates history acquisition program area
		#HS,a ↵	Retrieves and indicates the history information which executed a program address "a"
		#HSW,a ↵ #HSR,a ↵	Retrieves and indicates the history information which wrote or read the data area address "a"
12	File	#RF,file ↵	Move program file to memory
		#RFD,file ↵	Move data file to memory
		#VF,file ↵	Compare program file and contents of memory
		#VFD,file ↵	Compare data file and contents of memory
		#WF,file ↵	Save contents of memory to program file
		#WFD,file ↵	Save contents of memory to data file
		#CL,file ↵	Load ICE6200 set condition from file
		#CS,file ↵	Save ICE6200 set condition to file
13	Coverage	#CVD ↵	Indicates coverage information
		#CVR ↵	Clears coverage information
14	ROM Access	#RP ↵	Move contents of ROM to program memory
		#VP ↵	Compare contents of ROM with contents of program memory
		#ROM ↵	Set ROM type
15	Terminate ICE	#Q ↵	Terminate ICE and return to operating system control
16	Command Display	#HELP ↵	Display ICE6200 instruction
17	Self Diagnosis	#CHK ↵	Report results of ICE6200 self diagnostic test

↵ means press the RETURN key.

APPENDIX D Cross-assembler Pseudo-instruction List

Item No.	Pseudo-instruction	Meaning	Example of Use
1	EQU (Equation)	To allocate data to label	`ABC EQU 9` `BCD EQU ABC+1`
2	ORG (Origin)	To define location counter	`ORG 100H` `ORG 256`
3	SET (Set)	To allocate data to label (data can be changed)	`ABC SET 0001H` `ABC SET 0002H`
4	DW (Define Word)	To define ROM data	`ABC DW 'AB'` `BCD DW 0FFBH`
5	PAGE (Page)	To define boundary of page	`PAGE 1H` `PAGE 3`
6	SECTION (Section)	To define boundary of section	`SECTION`
7	END (End)	To terminate assembly	`END`
8	MACRO (Macro)	To define macro	`CHECK MACRO DATA`

9	LOCAL
	(Local)
		To make local specification of label during macro definition	`LOCAL LOOP`
			`LOOP CP MX,DATA`
			`JP NZ,LOOP`

10	ENDM
	(End Macro)
		To end macro definition	`ENDM`
			
			`CHECK 1`

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