EPSON

E0C5250

CAS + FSK IC

- ITU V.23 & Bell 202 FSK Receiver
- Bellcore "CPE Alerting Signal" Detection
- BT "Idle Tone Alert Signal" Detection
- Low Voltage Operation

■ DESCRIPTION

The CAS + FSK IC Calling Number Identification Receiver IC with Calling Waiting is a CMOS integrated circuit, which provides an interface to various calling information delivery services such as Calling Number Delivery (CND), Calling Name Delivery (CNAM) and Calling Identity on Call Waiting (CIDCW) compatible with the Bellcore GR-30-CORE, British Telecom Calling Line Identification Service (CLIP), the Cable Communications Association's Caller Display Services (CDS). The device also contains a power down circuit, a ring detect circuit, a carrier detect circuit, a synchronous receive data and clock output, 8051 like host interface for easier system implementation.

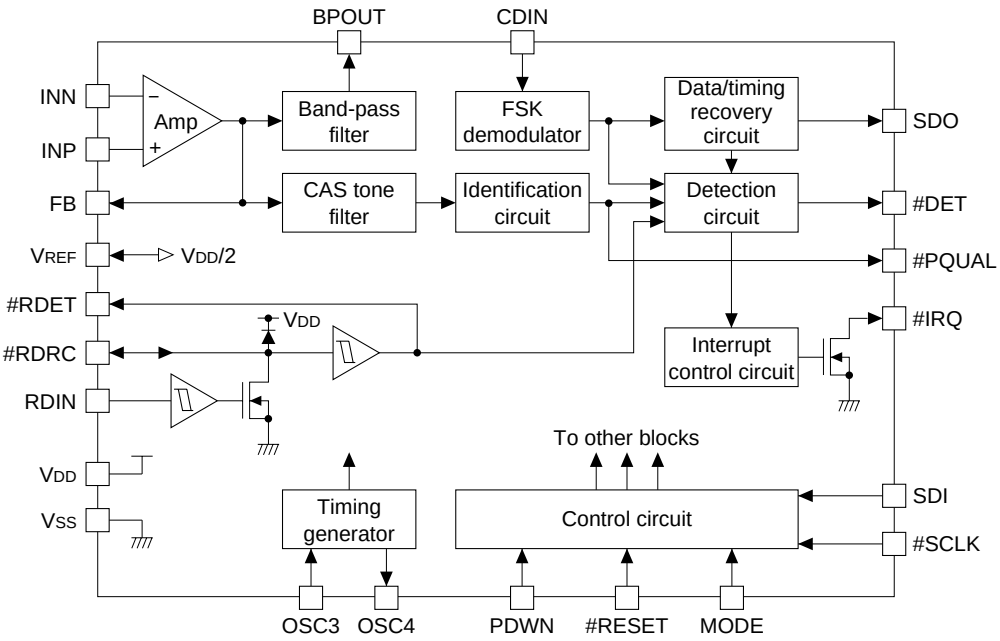
■ FEATURES

- Compatible with Bellcore GR-30-CORE, & SR-TSV-002476, BT SIN227 & SIN242
- Bellcore "CPE Alerting Signal (CAS)" and BT "Idle Tone Alert Signal" detection with programmable filter bandwidth
- ITU V.23 and Bell 202 FSK receiver
- Programmable CD level for each tone
- Ring detect or line reversal detection
- Carrier and ring detection output
- Users 3.579545 MHz crystal or external clock source
- Serial receive data output with clock
- Small pin count and low power consumption
- Power down mode
- Low voltage operation

■ APPLICATIONS

- Calling Number Delivery Service with Call Waiting
- Adjunct Boxes
- Telephone Answering Machines
- Feature Phones
- Fax Machines
- Computer Interface Products

■ BLOCK DIAGRAM



■ PIN DESCRIPTION

Note: The signal and pin names prefixed by # are those of active-low signals and pins.

Pin name	Pin No.	Type	Power-down state	Description
INP	1	Input Analog	Off	Positive input: Non-inverted amp input Connect this pin to the RING side of the twisted-pair telephone line through an input-gain setting resistor and DC-decoupling capacitor. In power-down mode, this pin is disconnected from the internal circuit.
INN	2	Input Analog	Off	Negative input: Inverted amp input Connect this pin to the TIP side of the twisted-pair telephone line through an input-gain setting resistor and DC-decoupling capacitor. In power-down mode, this pin is disconnected from the internal circuit.
FB	3	Output Analog	High-Z	Amp output Connect a feedback resistor to set the gain between this pin and the INN pin. In power-down mode, this pin goes to a high-impedance state.
VREF	4	Output Analog	VDD level	Reference voltage output This pin outputs a voltage that is 1/2 of VDD. Connect this pin to VSS via a 0.1-µF capacitor. In power-down mode, this pin outputs a voltage equal to VDD.
RDIN	5	Schmitt trigger input	Active	Ring detection input For ring detection, attenuate the ring signal before inputting it to this pin. This input circuit remains active even in power-down mode.
#RDRC	6	Open-drain output Schmitt trigger input	Active	Ring detection RC pin Connect an RC network to this pin and set the delay time for ring signal detection. This output circuit remains active even in power-down mode.
#RDET	7	Output	Active	Ring detection output This pin outputs the #RDRC signal after it is passed through a Schmitt trigger buffer. Upon detection of the ring signal, this pin changes to Low level.
PDWN	8	Input	Active	Power-down input This pin must be held at Low level during normal operation. When the pin is set to High level, the E0C5250 is placed in power-down mode. During power-down mode, each pin on the E0C5250 is placed in the state shown in this table.

Pin name	Pin No.	Type	Power-down state	Description
#RESET	9	Input	Active	Reset input All of the internal registers are reset to the default state when the pin is set to Low level. Before any data can be written to the internal registers, this pin must be set to High level.
IMODE	11	Input	Active	Mode selection input: Selects CAS mode or FSK/CPM mode CAS mode is selected by setting this input to High level, so that CAS detection is enabled while FSK function/CPM detection is disabled. Also, in this state, data can be written from the host device to the internal registers using the SDI and #SCLK pins. Note that before writing data to the internal registers, the serial interface must be synchronized to the data write sequence by temporarily setting this pin to Low level. FSK/CPM mode is selected by setting this input to Low level, in which case CAS detection is disabled and FSK function/CPM detection is enabled. In this state, the host device can read out receive data from the SDO pin.
VSS	12	Power supply (-)		Negative power-supply pin Connect this pin to the ground line of the system.
OSC3	13	Input	Off	Crystal oscillator input/external clock input Connect a crystal resonator between this pin and the OSC4 pin and an appropriate capacitance between this pin and the VSS pin. This pin can also be used for external clock input. In power-down mode, this pin is disconnected from the internal circuit.
OSC4	14	Output	High level	Crystal oscillator output Connect a crystal resonator between this pin and the OSC3 pin and an appropriate capacitance between this pin and the VSS pin. When connecting external clock input to the OSC3 pin, leave this pin open. During power-down mode, this pin changes to High level.
#PQUAL	16	Output	High level	Prequalify output The prequalify status of the CAS tone can be monitored from this pin in CAS mode. This pin returns to High level when the CAS tone is not detected.
#DET	17	Output	Active	Detection output During power-down mode, this pin changes to Low level when a ring signal is input or pulled to Low level by the Line Reversal signal. During normal operation in FSK mode, this pin goes to Low level when an FSK signal is input. During normal operation in CPM mode, this pin outputs the input signal in pulse form at the amplitude level of VDD and VSS. By measuring the frequency of the pulse from the host side, the CPM (dial) tone can be identified. During normal operation in CAS mode, this pin goes to Low level when a CAS tone signal is input.
#IRQ	18	Open-drain output	Active	Interrupt request output In power-down mode, this pin changes to Low level when a ring signal is input or pulled to Low level by the Line Reversal signal. During normal operation in FSK mode, this pin changes to Low level when receive data is latched into the internal register and is ready to be read by the host. Then, when the host reads the first bit of the receive data, this pin returns to High level. During normal operation in CPM mode, this pin changes to Low level when a signal with a frequency of 200 Hz or above, such as the dial tone, is input. During normal operation in CAS mode, this pin changes to Low level when the CAS tone is detected. This pin is held at Low level while the CAS tone is being input.
#SCLK	19	Input	Active	Serial clock input When the host writes to the internal register or reads receive data, a clock signal is fed from the host into this pin. The receive data read out by the host is sequentially shifted at falling edges of the clock signal fed to this pin.
SDI	20	Input	Active	Serial data input When the host writes to the internal register, the write data is input from this pin.
SDO	21	Output	High level	Serial data output This pin outputs the receive data read out by the host. When asynchronous mode is selected, data in asynchronous mode is output. When synchronous mode is selected, data is output synchronously with the clock signal fed to the #SCLK pin by the host. In power-down, CPM, or CAS mode, this pin is held at High level.
BPOUT	22	Input Analog	VREF	Capacitor connecting pin Connect a 0.1-µF capacitor between this pin and the CDIN pin.
CDIN	23	Output Analog	High-Z	Capacitor connecting pin Connect a 0.1-µF capacitor between this pin and the BPOUT pin.
VDD	24	Power supply		Positive power supply
N.C.	10,15	Open		Unconnected

■ ELECTRICAL CHARACTERISTICS

● Absolute Maximum Ratings

Parameter	Symbol	Rated value	Unit
Power supply voltage	V_{DD}	-0.5 to 7	V
Input voltage	V_I	-0.3 to V_{DD}+0.3	V
Total output current	ΣI_{VDD}	±10	mA
Power dissipation	P_D	250	mW
Storage temperature	T_{STG}	-65 to 150	°C
Solder temperature	T_{SOL}	255	°C
Soldering time	t_{SOL}	10	Sec
Operating temperature	T_{OPR}	-20 to 70	°C
Electrostatic withstand voltage	V_E	EIAJ test (C=200pF): 150V or more MIL test (C=100pF, R=1.5kΩ): 1200V or more	V

The voltages are referenced to the V_{SS} pin as the ground level.

● Recommended Operating Conditions

Parameter	Symbol	Condition	Unit
Power supply voltage	V_{DD}	2.7 to 5.5	V
Crystal/clock frequency	f_{CLK}	3.579545	MHz
Crystal/clock frequency error	f_{ERR}	±0.01	%

The voltages are referenced to the V_{SS} pin as the ground level.

● DC Characteristics

(Unless otherwise noted: V_{DD}=2.7V to 5.5V, V_{SS}=0V, f_{CLK}=3.579545MHz, Ta=-20 to 70°C)

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit
High level input voltage (1)	V_{IH1}		OSC3,MODE, #SCLK, SDI, PDWN, #RESET,	0.8V_{DD}		V_{DD}	V
High level input voltage (2)	V_{IH2}		RDIN, #RDRC	0.7V_{DD}		V_{DD}	V
Low level input voltage (1)	V_{IL1}		OSC3, MODE, #SCLK, SDI, PDWN, #RESET	0		0.2V_{DD}	V
Low level input voltage (2)	V_{IL2}		RDIN, #RDRC	0		0.3V_{DD}	V
High level input current	I_{IH}	V_{IH}=V_{DD}	RDIN, OSC3, MODE, #SCLK, SDI, PDWN,#RESET, #IRQ #RDRC (RDIN = Low)	0		0.5	µA
Low level input current	I_{IL}	V_{IL}=V_{SS}	RDIN, OSC3, MODE, #SCLK, SDI, PDWN, #RESET, #RDRC, #IRQ	-0.5		0	µA
High level output current	I_{OH}	V_{OH}=0.9V_{DD}	SDO, #DET, #RDET, #PQUAL			-1.5	mA
Low level output current	I_{OL}	V_{OL}=0.1V_{DD}	SDO, #DET, #RDET, #PQUAL, #IRQ, #RDRC	2.5			mA
V_{REF} output voltage	V_{REF}				V_{DD}/2		V
Input impedance	R_{IN}		INP, INN	10			MΩ
	R_{CDIN}		CDIN	140	200	260	kΩ

● Current Consumption

(Unless otherwise noted: V_{DD}=2.7V to 5.5V, V_{SS}=0V, f_{CLK}=3.579545MHz, Ta=-20 to 70°C)

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit
Current consumption	I_{OP}	During power-down (PDWN = High)				1.0	µA
		When operating (no signal input)	V_{DD}=5V		3.0		mA
			V_{DD}=3V		1.8		mA

● Crystal Oscillation Characteristics

(Unless otherwise noted: V_{DD}=2.7V to 5.5V, V_{SS}=0V, C_G=C_D=18pF, Ta=25°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start time	tsta	3.579545MHz oscillator			20	msec

● FSK Demodulation Circuit Characteristics

FSK AC characteristics

(Unless otherwise noted: V_{DD}=5.0/3.0V, V_{SS}=0V, f_{CLK}=3.579545MHz, Ta=-20 to 70°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Transfer rate	T_{RATE}		1188	1200	1212	Baud
Bell 202 mark (logic 1) frequency	f_{B1}		1188	1200	1212	Hz
Bell 202 space (logic 0) frequency	f_{B0}		2178	2200	2222	Hz
ITU-T V.23 mark (logic 1) frequency	f_{V1}		1280	1300	1320	Hz
ITU-T V.23 space (logic 0) frequency	f_{V2}		2068	2100	2132	Hz
SN ratio	SNR		20	–	–	dB
Carrier-detect ON sensitivity *1 (input level at TPI/RING)	CD_{ONFSK}	V_{DD}=5V	-44.9	-42.9	-40.9	dBm
		Input amp gain (G_{AMP})=-5dB	-47.1	-45.1	-43.1	dBV
		V_{DD}=3V	-44.9	-42.9	-40.9	dBm
		Input amp gain (G_{AMP})=-9.4dB	-47.1	-45.1	-43.1	dBV
Carrier-detect OFF sensitivity *1	CD_{OFFFSK}	V_{DD}=5V	-46.9	-44.9	-42.9	dBm
		Input amp gain (G_{AMP})=-5dB	-49.1	-47.1	-45.1	dBV
		V_{DD}=3V	-46.9	-44.9	-42.9	dBm
		Input amp gain (G_{AMP})=-9.4dB	-49.1	-47.1	-45.1	dBV

*1: When the gain in the input amp is set to G_{AMP} (dB), the CD_{ONFSK} and CD_{OFFFSK} values (Typ.) can be calculated from the equation below.

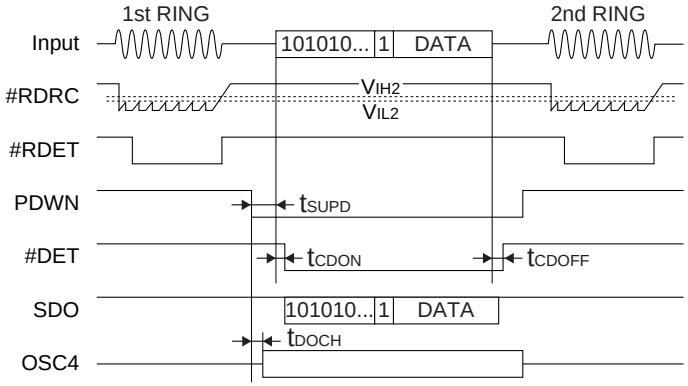
CD_{ONFSK} [dBm] = $-G_{AMP}$ - 47.9 + $20\log(\frac{V_{DD}}{5})$ [dBm], CD_{ONFSK} [dBV] = $-G_{AMP}$ - 50.1 + $20\log(\frac{V_{DD}}{5})$ [dBV]

CD_{OFFFSK} [dBm] = $-G_{AMP}$ - 49.9 + $20\log(\frac{V_{DD}}{5})$ [dBm], CD_{OFFFSK} [dBV] = $-G_{AMP}$ - 52.1 + $20\log(\frac{V_{DD}}{5})$ [dBV]

FSK switching characteristics

(Unless otherwise noted: V_{DD}=5.0/3.0V, V_{SS}=0V, f_{CLK}=3.579545MHz, Ta=-20 to 70°C, C_L=50pF)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
PDWN fall → FSK	t_{SUPD}				20	msec
Carrier detect start time	t_{CDON}		5	10	15	msec
Data end → #DET rise	t_{CDOFF}		5	10	15	msec
PDWN rise → Oscillation start	t_{DOCH}	V_{DD}=5V		7	12	msec
		V_{DD}=3V		10	15	msec



● Dual-Tone (CAS) Detection Circuit Characteristics

CAS AC characteristics

(Unless otherwise noted: V_{DD}=5.0/3.0V, V_{SS}=0V, f_{CLK}=3.579545MHz, Ta=-20 to 70°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Carrier-detect sensitivity *1 (input level at TPI/RING)	CD_{ONTONE}	V_{DD}=5V, Bellcore mode Input amp gain (G_{AMP})=-5dB Tone filter gain=-4dB	-39.8	-35.8	-35.1	dBm
		V_{DD}=5V, BT mode *2 Input amp gain (G_{AMP})=-5dB Tone filter gain=-4dB	-48.0	-44.0	-40.0	dBV
		V_{DD}=3V, BT mode *2 Input amp gain (G_{AMP})=-9.4dB Tone filter gain=-4dB	-39.8	-35.8	-35.1	dBm
		V_{DD}=3V, BT mode *2 Input amp gain (G_{AMP})=-9.4dB Tone filter gain=-4dB	-48.0	-44.0	-40.0	dBV
Low tone frequency	f_{LTONE}	Bellcore (±0.5%)	2119.35	2130	2140.65	Hz
		BT line disconnected	2110	2130	2150	Hz
		BT line connected (±0.6%)	2117.22	2130	2142.78	Hz
High tone frequency	f_{HTONE}	Bellcore (±0.5%)	2736.25	2750	2763.75	Hz
		BT line disconnected	2720	2750	2780	Hz
		BT line connected (±0.6%)	2733.50	2750	2766.50	Hz

*1: When the gain in the input amp is set to G_{AMP} (dB), the CD_{ONTONE} value (Typ.) can be calculated from the equation below.
(When the internal tone filter gain = -4 dB)

$$CD_{ONTONE}\ [dBm] = -G_{AMP} - 40.8 + 20\log(\frac{V_{DD}}{5})\ [dBm],\quad CD_{ONTONE}\ [dBV] = -G_{AMP} - 49 + 20\log(\frac{V_{DD}}{5})\ [dBV]$$

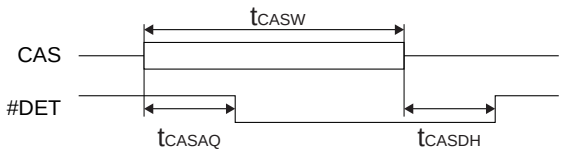
*2: BT mode is selected by setting the mode register (address = 0h) bit 2 to 1. By this setting, the gain in each dual-tone filter is raised +6 dB for adjustment to the British Telecom CD level.

CAS switching characteristics

(Unless otherwise noted: V_{DD}=5.0/3.0V, V_{SS}=0V, f_{CLK}=3.579545MHz, Ta=-20 to 70°C, CL=50pF)

Parameter	Symbol	Min.	Typ.	Max.	Unit
CAS detect capture time	t_{CASAQ}		2.8×(N+2)+16.9		msec
CAS end → #DET rise	t_{CASDH}		2.8×(31-N)+13.1		msec
CAS width	t_{CASW}	75	80	85	msec

$N = TH0 \times 16 + TL3 \times 8 + TL2 \times 4 + TL1 \times 2 + TL0$



● Call Progress Mode (CPM) Detection Circuit Characteristics

CPM AC characteristics

(Unless otherwise noted: V_{DD}=5.0/3.0V, V_{SS}=0V, f_{CLK}=3.579545MHz, Ta=-20 to 70°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Carrier-detect ON sensitivity *1 (input level at TPI/RING)	CD_{ONCPM}	V_{DD}=5V	-44.9	-42.9	-40.9	dBm
		Input amp gain (G_{AMP})=-5dB	-47.1	-45.1	-43.1	dBV
		V_{DD}=3V	-44.9	-42.9	-40.9	dBm
		Input amp gain (G_{AMP})=-9.4dB	-47.1	-45.1	-43.1	dBV
Carrier-detect OFF sensitivity *1	CD_{OFFCPM}	V_{DD}=5V	-46.9	-44.9	-42.9	dBm
		Input amp gain (G_{AMP})=-5dB	-49.1	-47.1	-45.1	dBV
		V_{DD}=3V	-46.9	-44.9	-42.9	dBm
		Input amp gain (G_{AMP})=-9.4dB	-49.1	-47.1	-45.1	dBV

*1: When the gain in the input amp is set to G_{AMP} (dB), the CD_{ONCPM} and CD_{OFFCPM} values (Typ.) can be calculated from the equation below.

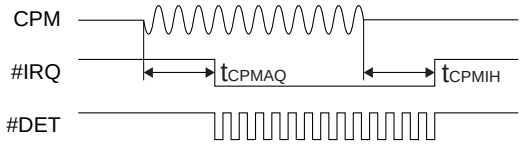
$$CD_{ONCPM}\ [dBm] = -G_{AMP} - 47.9 + 20\log(\frac{V_{DD}}{5})\ [dBm],\quad CD_{ONCPM}\ [dBV] = -G_{AMP} - 50.1 + 20\log(\frac{V_{DD}}{5})\ [dBV]$$

$$CD_{OFFCPM}\ [dBm] = -G_{AMP} - 49.9 + 20\log(\frac{V_{DD}}{5})\ [dBm],\quad CD_{OFFCPM}\ [dBV] = -G_{AMP} - 52.1 + 20\log(\frac{V_{DD}}{5})\ [dBV]$$

CPM switching characteristics

(Unless otherwise noted: V_{DD}=5.0/3.0V, V_{SS}=0V, f_{CLK}=3.579545MHz, Ta=-20 to 70°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
CPM tone-detect capture time	t_{CPMAQ}		25		msec
CPM tone end → #IRQ rise	t_{CPMIH}		30		msec

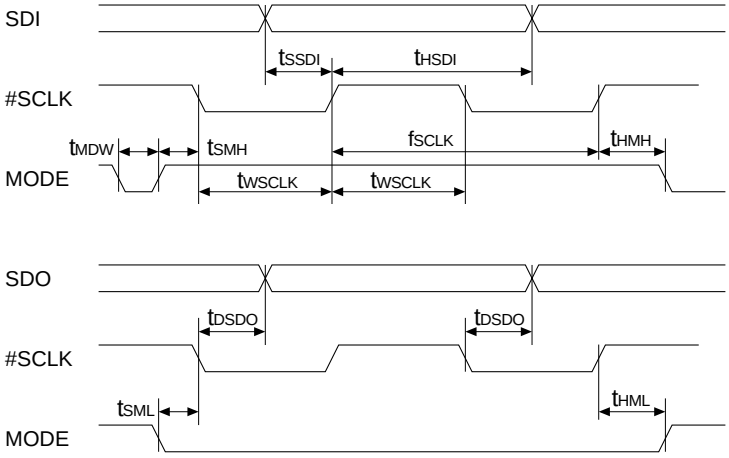


● Serial Interface Circuit Characteristics

Serial interface AC characteristics

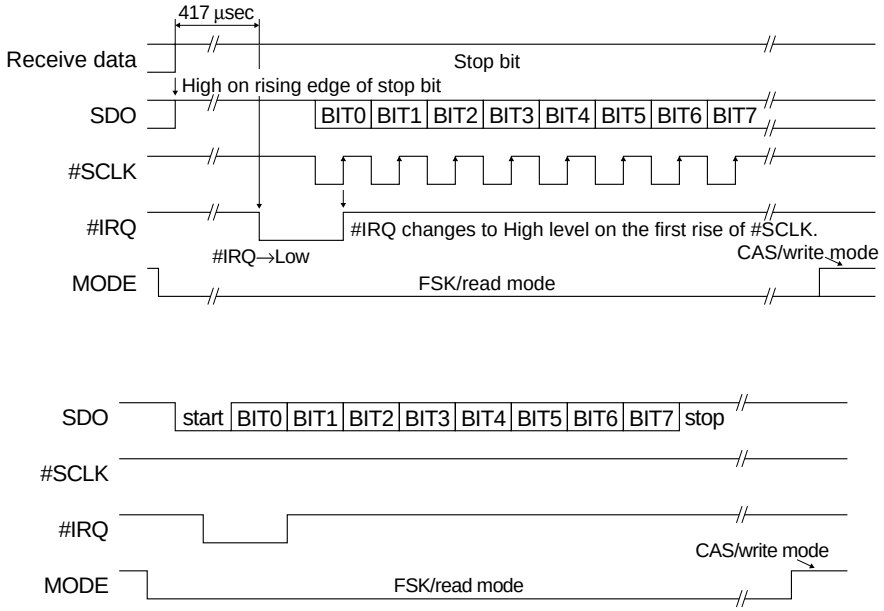
(Unless otherwise noted: V_{DD}=5.0/3.0V, V_{SS}=0V, f_{CLK}=3.579545MHz, Ta=-20 to 70°C, CL=50pF)

Parameter	Symbol	Min.	Typ.	Max.	Unit
#SCLK frequency	f_{SCLK}			1	MHz
#SCLK pulse width	t_{WSCLK}	400			nsec
SDI setup time	t_{SSDI}	250			nsec
SDI hold time	t_{HSDI}	500			nsec
SDO delay time	t_{DSDO}			250	nsec
MODE High setup time	t_{SMH}	1			µsec
MODE High hold time	t_{HMH}	1			µsec
MODE Low setup time	t_{SML}	1			µsec
MODE Low hold time	t_{HML}	1			µsec
MODE Low pulse width	t_{MDW}	1			µsec



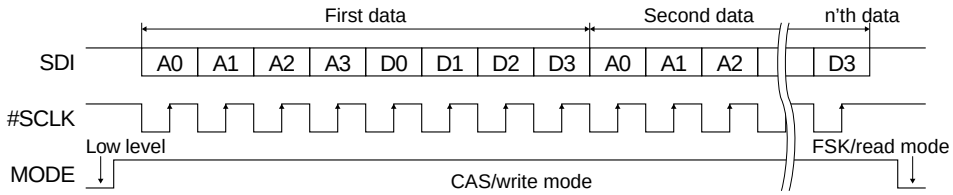
FSK demodulated data read mode

The FSK signal fed to the INP and INN pins is demodulated into 8-bit asynchronous (start-stop) data. The demodulated data is then sampled by the internal 8-bit shift register. When the data has been stored in the shift register, the #IRQ pin changes to Low level, indicating that the data can be read by the host CPU.
If the MODE pin is set to Low level and synchronoμs mode has been selected (MDR[0] = 1), the host CPU reads out the 8-bit data synchronously with the clock signal fed from the host CPU to the #SCLK pin. Figure 5.9.3 shows the timing at which this data is read. Each bit of the 8-bit data is output from the SDO pin synchronously with falling edges of the #SCLK clock signal, beginning with bit 0. The host CPU latches each bit into the internal logic at rising edges of the #SCLK clock signal.
If the MODE pin is set to Low level and asynchronous mode has been set (MDR[0] = 0), the data is output from the SDO pin at a transfer rate of 1,200 baud. The clock signal from the host CPU is unnecessary. The host CPU latches the data synchronously with the start bit.



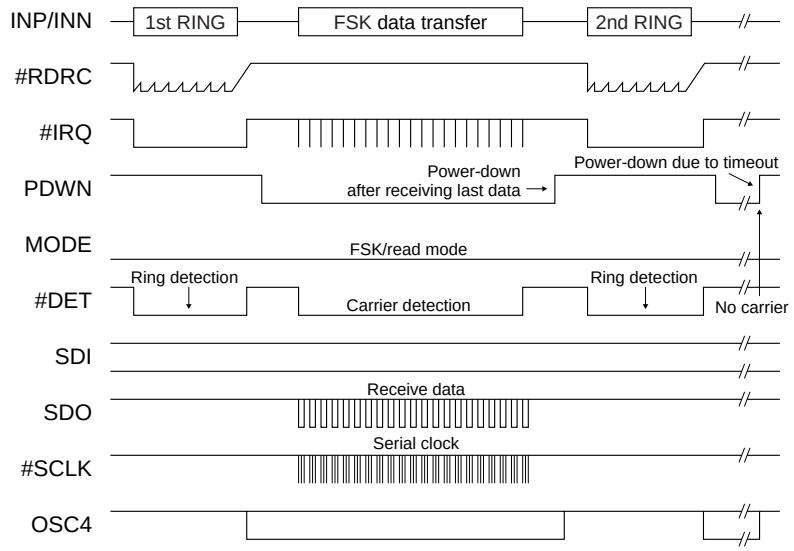
CAS detection circuit control-register write mode

The host CPU can write 4-bit data to the internal registers through the SDI pin in order to set each control bit. The host CPU must temporarily pull the MODE pin to Low level to initialize the write control circuit before it can write data. Then, after releasing the MODE pin back to High level, the host CPU must be held at High level while writing data to the internal register. The data input to the SDI pin is sampled at rising edges of the clock signal fed from the host CPU to the #SCLK pin. The first four bits of data sent from the host CPU are the address A[3:0] of the internal register to be accessed. The subsequent four bits are the data bits D[3:0] to be written to the specified register. The data is input beginning with the LSB.

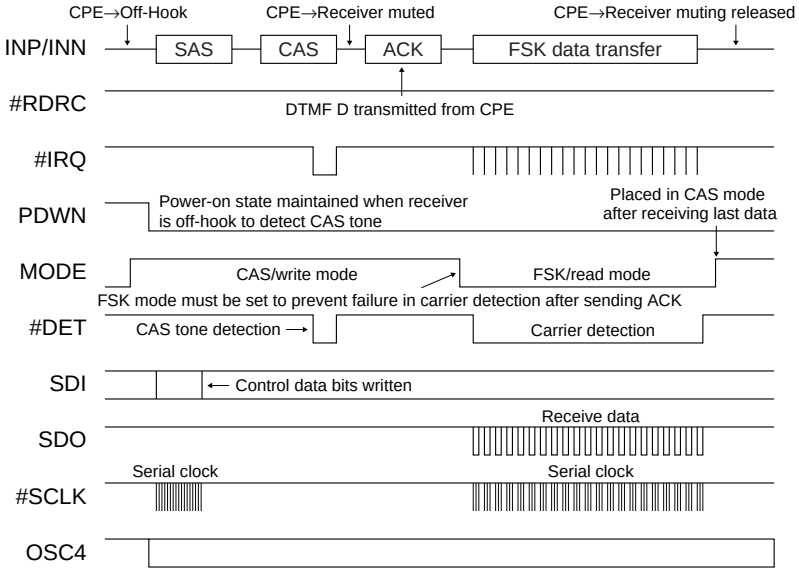


● E0C5250 Timing Chart

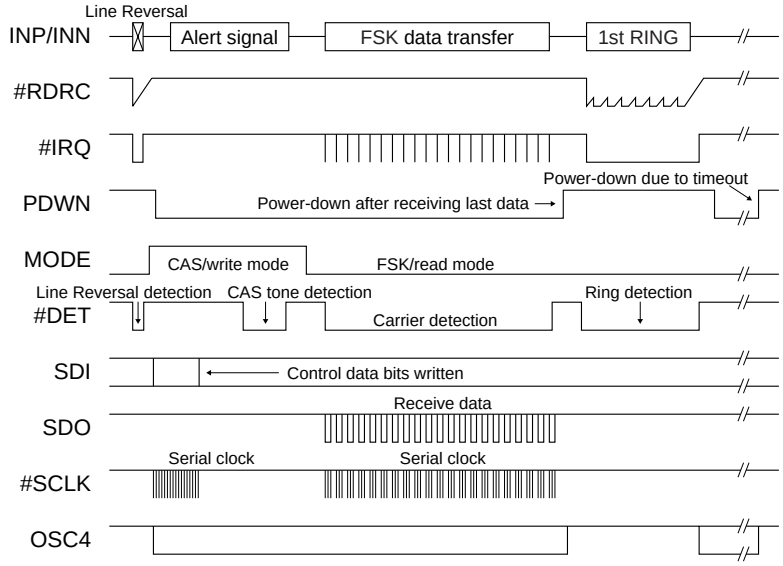
Bellcore on-hook data transfer



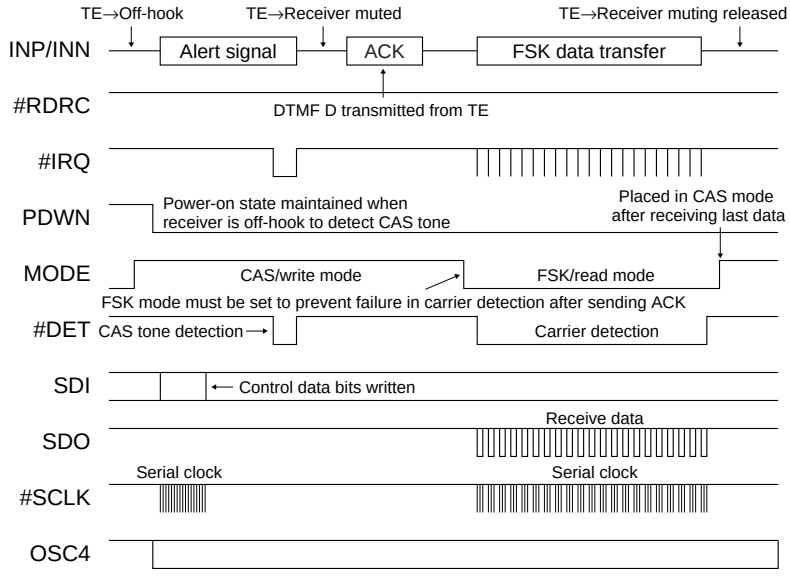
Bellcore off-hook data transfer



BT Idle State CLI service

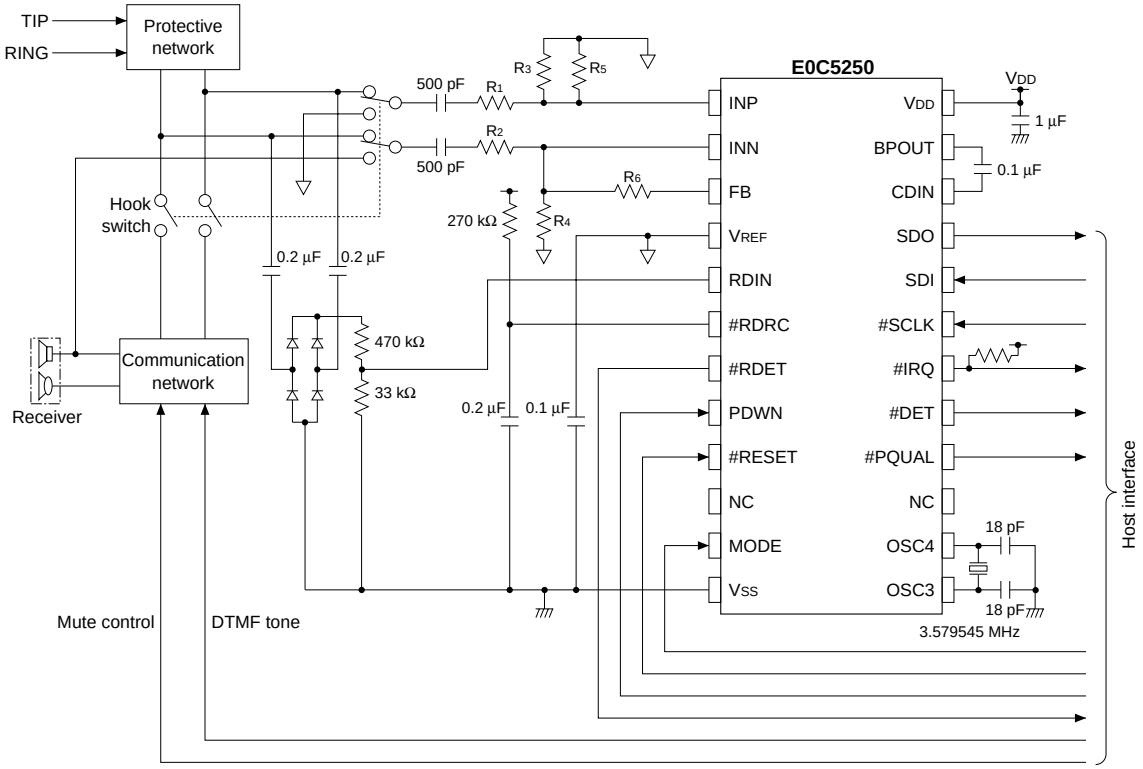


BT Loop State CLI service



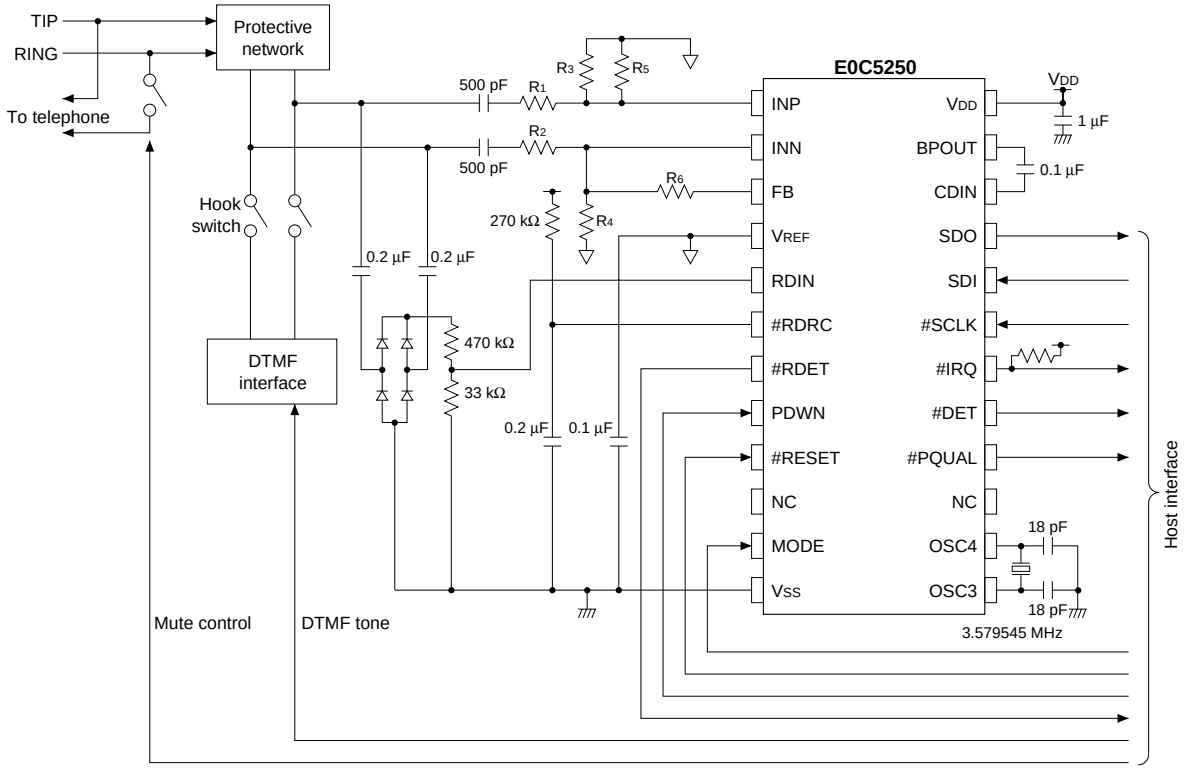
● External Wiring Diagram (Example)

Example of Bellcore-compatible telephone circuit



Note: The above circuit diagram is merely an example, and does not guarantee the operation of the circuit.

Example of Bellcore-compatible auxiliary circuit

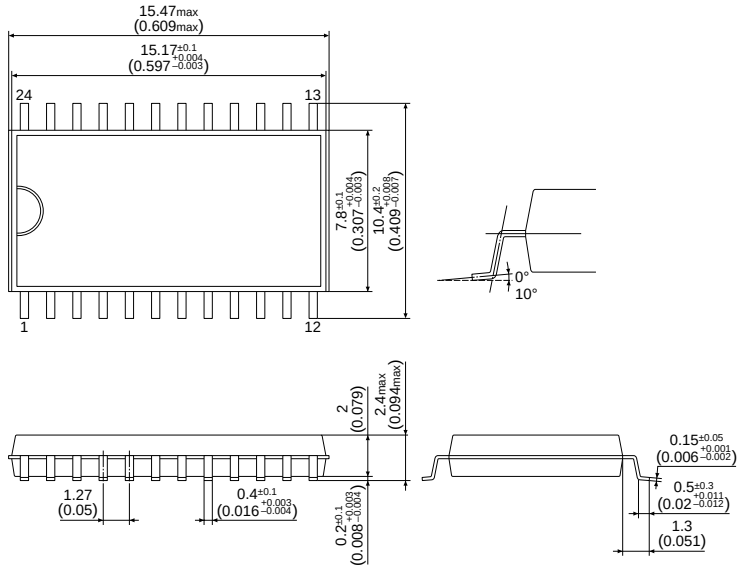


Note: The above circuit diagram is merely an example, and does not guarantee the operation of the circuit.

■ PACKAGE DIMENSIONS

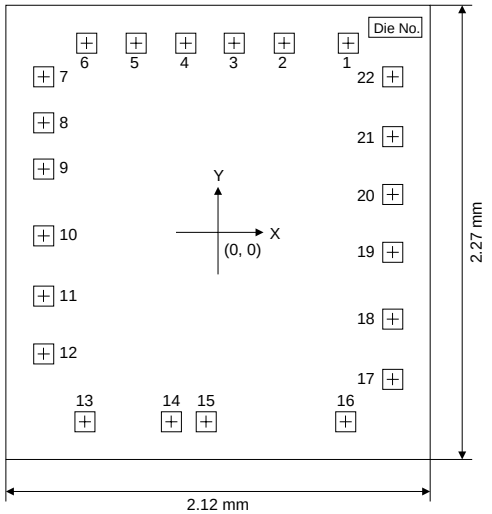
SOP1-24pin Plastic Package

Unit: mm (inch)



■ PAD LAYOUT

● Diagram of Pad Layout



Chip thickness: 400 µm
Pad opening: 100 µm

● Pad Coordinates

(Unit: µm)

Pad No.	Pad name	X coordinate	Y coordinate	Pad No.	Pad name	X coordinate	Y coordinate
1	CDIN	650	946	12	#RESET	-872	-607
2	BPOUT	330	946	13	MODE	-666	-946
3	V_{DD}	80	946	14	V_{SS}	-234	-946
4	INP	-162	946	15	OSC3	-60	-946
5	INN	-410	946	16	OSC4	637	-946
6	FB	-657	946	17	#PQUAL	872	-734
7	V_{REF}	-872	778	18	#DET	872	-433
8	RDIN	-872	548	19	#IRQ	872	-99
9	#RDRC	-872	317	20	#SCLK	872	190
10	#RDET	-872	-17	21	SDI	872	479
11	PDWN	-872	-318	22	SDO	872	778

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