EPSON

E0C63158

4-bit Single Chip Microcomputer

- 4-bit E0C63000 Core CPU
- A/D Converter
- Low Voltage Operation (0.9V min.)
- High Speed Instruction Cycle (2-6CPI)

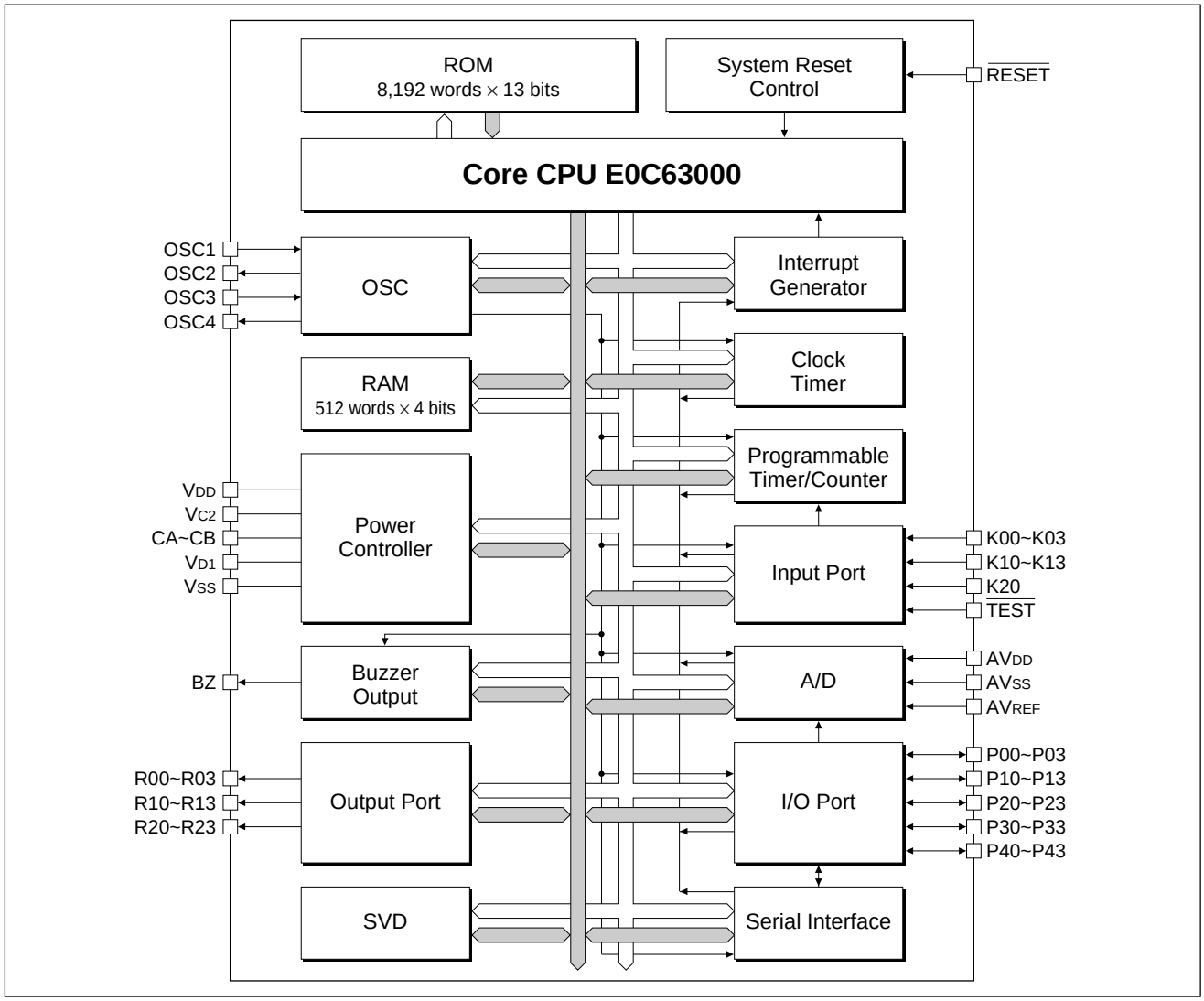
■ DESCRIPTION

The E0C63158 is a microcomputer composed of a CMOS 4-bit core CPU (E0C63000), ROM, RAM, A/D converter and timers. Since the E0C63158 features low voltage and high speed operation and low current consumption, it is suitable for systems that need to be driven with a battery.

■ FEATURES

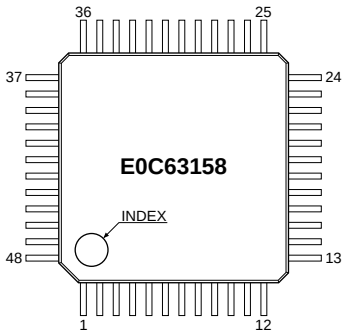
- CMOS LSI 4-bit parallel processing
- Clock ..... 32.768kHz (X'tal or CR oscillation)
  2MHz (CR or Ceramic oscillation)
- Instruction set ..... Basic instruction : 46 types (411 instructions with all)
  Addressing mode : 8 types
- ROM capacity ..... 8,192 words × 13 bits
- RAM capacity ..... 512 words × 4 bits
- Input port ..... 9 bits
- Output port ..... 12 bits
- I/O port ..... 20 bits
- Clock timer ..... 1 ch.
- Programmable timer ..... 8 bits × 2 ch. or 16 bits × 1 ch.
- Watchdog timer ..... Built-in
- Serial interface ..... Synchronous 8 bits
- A/D converter ..... 4 bits (0.9V to 2.7V)
  8 bits (2.7V to 3.6V)
- Supply voltage detection (SVD) circuit ..... From 1.05 to 2.60V
- Operation voltage ..... 0.9 to 3.6V
- Current consumption ..... 2µA (32.768kHz X'tal, 1.5V, HALT)
  4µA (32.768kHz X'tal, 1.5V, RUN)
  900µA (4MHz Ceramic, 3.0V, RUN)
- Package ..... QFP13-64pin, QFP12-48pin, Die form

■ BLOCK DIAGRAM



■ PIN CONFIGURATION

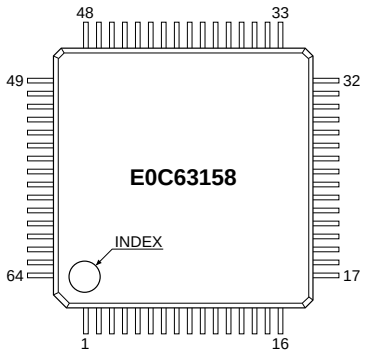
QFP12-48pin



No.	Pin name	No.	Pin name	No.	Pin name	No.	Pin name
1	VSS	13	VC2	25	P10	37	R01
2	OSC1	14	P43	26	P03	38	R00
3	OSC2	15	P42	27	P02	39	BZ
4	VD1	16	P41	28	P01	40	K00
5	OSC3	17	P40	29	P00	41	K01
6	OSC4	18	P23	30	R13	42	K02
7	VDD	19	P22	31	R12	43	K03
8	$\overline{\text{RESET}}$	20	P21	32	R11	44	K10
9	$\overline{\text{TEST}}$	21	P20	33	R10	45	K11
10	AVREF	22	P13	34	R03	46	K12
11	CB	23	P12	35	R02	47	K13
12	CA	24	P11	36	N.C.	48	K20

N.C. : No Connection

QFP13-64pin



No.	Pin name	No.	Pin name	No.	Pin name	No.	Pin name
1	V_{SS}	17	P43	33	P03	49	N.C.
2	OSC1	18	P42	34	P02	50	N.C.
3	OSC2	19	P41	35	P01	51	N.C.
4	V_{D1}	20	P40	36	P00	52	R01
5	OSC3	21	P33	37	R23	53	R00
6	OSC4	22	P32	38	R22	54	BZ
7	V_{DD}	23	P31	39	R21	55	K00
8	$\overline{RESET}$	24	P30	40	R20	56	K01
9	$\overline{TEST}$	25	P23	41	R13	57	K02
10	AV_{DD}	26	P22	42	R12	58	K03
11	AV_{SS}	27	P21	43	R11	59	K10
12	AV_{REF}	28	P20	44	R10	60	K11
13	CB	29	P13	45	R03	61	K12
14	CA	30	P12	46	R02	62	K13
15	V_{C2}	31	P11	47	N.C.	63	K20
16	N.C.	32	P10	48	N.C.	64	N.C.

N.C. : No Connection

■ PIN DESCRIPTION

Pin name	Pin No.		In/Out	Function
	QFP12-48	QFP13-64		
V_{DD}	7	7	–	Power (+) supply pin
V_{SS}	1	1	–	Power (–) supply pin
V_{D1}	4	4	–	Oscillation/internal logic system regulated voltage output pin
V_{C2}	13	15	–	Booster power supply pin
CA, CB	12, 11	14, 13	–	Boosting capacitor connecting pin
OSC1	2	2	I	Crystal or CR oscillation input pin (selected by mask option)
OSC2	3	3	O	Crystal or CR oscillation output pin (selected by mask option)
OSC3	5	5	I	CR or ceramic oscillation input pin (selected by mask option)
OSC4	6	6	O	CR or ceramic oscillation output pin (selected by mask option)
K00–K03	40–43	55–58	I	Input port
K10–K13	44–47	59–62	I	Input port
K20	48	63	I	Input port (key-position detect interrupt port)
P00–P03	29–26	36–33	I/O	I/O port
P10–P13	25–22	32–29	I/O	I/O port (switching to serial I/F input/output is possible by software)
P20–P23	21–18	28–25	I/O	I/O port
P30–P33 *1	–	24–21	I/O	I/O port
P40–P43	17–14	20–17	I/O	I/O port (can be used as A/D converter inputs)
R00	38	53	O	Output port
R01	37	52	O	Output port
R02	35	46	O	Output port (switching to TOUT output is possible by software)
R03	34	45	O	Output port (switching to FOUT output is possible by software)
R10–R13	33–30	44–41	O	Output port
R20–R23 *1	–	40–37	O	Output port
AV_{DD} *2	–	10	–	Power (+) supply pin for A/D converter
AV_{SS} *2	–	11	–	Power (–) supply pin for A/D converter
AV_{REF}	10	12	–	Reference voltage for A/D converter
BZ	39	54	O	Buzzer output pin
$\overline{RESET}$	8	8	I	Initial reset input pin
$\overline{TEST}$	9	9	I	Testing input pin

∗1: P30–P33 and R20–R23 are not available in the QFP12-48pin package.
∗2: In the QFP12-48pin package, AV_{DD} and AV_{SS} are connected with V_{DD} and V_{SS} inside of the IC, respectively.

■ ELECTRICAL CHARACTERISTICS

● Absolute Maximum Ratings

(V_{SS}=0V)

Rating	Symbol	Value	Unit
Supply voltage	V_{DD}	-0.5 to 4.6	V
Input voltage (1)	V_I	-0.5 to V_{DD} + 0.3	V
Input voltage (2)	V_{IOSC}	-0.5 to V_{D1} + 0.3	V
Permissible total output current *1	ΣI_{VDD}	10	mA
Operating temperature	Topr	-20 to 70	°C
Storage temperature	Tstg	-65 to 150	°C
Soldering temperature / time	Tsol	260°C, 10sec (lead section)	–
Permissible dissipation *2	P_D	250	mW

*1: The permissible total output current is the sum total of the current (average current) that simultaneously flows from the output pins (or is draw in).
*2: In case of plastic package (QFP12-48pin, QFP13-64pin).

● Recommended Operating Conditions

(Ta=-20 to 70°C)

Condition	Symbol	Remark		Min.	Typ.	Max.	Unit
Supply voltage	V_{DD}	V_{SS}=0V	Booster mode (OSC3 OFF)	0.9	1.1	1.35	V
			Normal mode (OSC3 OFF)	1.35	3.0	3.6	V
			Normal mode (OSC3 ON)	2.2	3.0	3.6	V
	AV_{DD}	AV_{SS}=0V		0.9	3.0	3.6	V
	AV_{REF}	$AV_{REF} \leq AV_{DD}$		0.9	3.0	3.6	V
Oscillation frequency	f_{OSC1}	Crystal oscillation		–	32.768	–	kHz
		CR oscillation		40	60	80	kHz
	f_{OSC3}	CR oscillation			1800		kHz
		Ceramic oscillation				4100	kHz

● DC Characteristics

(Unless otherwise specified: V_{DD}=1.5V, V_{SS}=0V, f_{OSC1}=32.768kHz, Ta=25°C, V_{D1}/V_{C2} are internal voltage, C_1–C_3=0.2µF)

Characteristic	Symbol	Condition		Min.	Typ.	Max.	Unit
High level input voltage (1)	V_{IH1}		K00–03, K10–13, K20, P00–03 P10–13, P20–23, P30–33, P40–43	0.8·V_{DD}		V_{DD}	V
High level input voltage (2)	V_{IH2}		$\overline{RESET}$, $\overline{TEST}$	0.9·V_{DD}		V_{DD}	V
Low level input voltage (1)	V_{IL1}		K00–03, K10–13, K20, P00–03 P10–13, P20–23, P30–33, P40–43	0		0.2·V_{DD}	V
Low level input voltage (2)	V_{IL2}		$\overline{RESET}$, $\overline{TEST}$	0		0.1·V_{DD}	V
High level input current	I_{IH}	V_{IH}=1.5V	K00–03, K10–13, K20, P00–03 P10–13, P20–23, P30–33, P40–43 $\overline{RESET}$, $\overline{TEST}$	0		0.5	µA
Low level input current (1)	I_{IL1}	V_{IL1}=V_{SS} No Pull-up	K00–03, K10–13, K20, P00–03 P10–13, P20–23, P30–33, P40–43 $\overline{RESET}$, $\overline{TEST}$	-0.5		0	µA
Low level input current (2)	I_{IL2}	V_{IL2}=V_{SS} With Pull-up	K00–03, K10–13, K20, P00–03 P10–13, P20–23, P30–33, P40–43 $\overline{RESET}$, $\overline{TEST}$	-7.5	-5	-2.5	µA
High level output current (1)	I_{OH1}	V_{OH1}=0.9·V_{DD}	R00–03, R10–13, R20–23, P00–03 P10–13, P20–23, P30–33, P40–43			-0.3	mA
High level output current (2)	I_{OH2}	V_{OH2}=0.9·V_{DD}	BZ			-0.3	mA
Low level output current (1)	I_{OL1}	V_{OL1}=0.1·V_{DD}	R00–03, R10–13, R20–23, P00–03 P10–13, P20–23, P30–33, P40–43	0.5			mA
Low level output current (2)	I_{OL2}	V_{OL2}=0.1·V_{DD}	BZ	0.5			mA

(Unless otherwise specified: V_{DD}=3.0V, V_{SS}=0V, f_{OSC1}=32.768kHz, Ta=25°C, V_{D1}/V_{C2} are internal voltage, C_1–C_3=0.2µF)

Characteristic	Symbol	Condition		Min.	Typ.	Max.	Unit
High level input voltage (1)	V_{IH1}		K00–03, K10–13, K20, P00–03 P10–13, P20–23, P30–33, P40–43	0.8·V_{DD}		V_{DD}	V
High level input voltage (2)	V_{IH2}		$\overline{RESET}$, $\overline{TEST}$	0.9·V_{DD}		V_{DD}	V
Low level input voltage (1)	V_{IL1}		K00–03, K10–13, K20, P00–03 P10–13, P20–23, P30–33, P40–43	0		0.2·V_{DD}	V
Low level input voltage (2)	V_{IL2}		$\overline{RESET}$, $\overline{TEST}$	0		0.1·V_{DD}	V
High level input current	I_{IH}	V_{IH}=3.0V	K00–03, K10–13, K20, P00–03 P10–13, P20–23, P30–33, P40–43 $\overline{RESET}$, $\overline{TEST}$	0		0.5	µA
Low level input current (1)	I_{IL1}	V_{IL1}=V_{SS} No Pull-up	K00–03, K10–13, K20, P00–03 P10–13, P20–23, P30–33, P40–43 $\overline{RESET}$, $\overline{TEST}$	-0.5		0	µA
Low level input current (2)	I_{IL2}	V_{IL2}=V_{SS} With Pull-up	K00–03, K10–13, K20, P00–03 P10–13, P20–23, P30–33, P40–43 $\overline{RESET}$, $\overline{TEST}$	-15	-10	-5	µA
High level output current (1)	I_{OH1}	V_{OH1}=0.9·V_{DD}	R00–03, R10–13, R20–23, P00–03 P10–13, P20–23, P30–33, P40–43			-1.5	mA
High level output current (2)	I_{OH2}	V_{OH2}=0.9·V_{DD}	BZ			-1.5	mA
Low level output current (1)	I_{OL1}	V_{OL1}=0.1·V_{DD}	R00–03, R10–13, R20–23, P00–03 P10–13, P20–23, P30–33, P40–43	3			mA
Low level output current (2)	I_{OL2}	V_{OL2}=0.1·V_{DD}	BZ	3			mA

● Analog Circuit Characteristics and Current Consumption

(Unless otherwise specified: V_{DD}=3.0V, V_{SS}=0V, f_{OSC1}=32.768kHz, C_G=25pF, Ta=25°C, V_{D1}/V_{C2} are internal voltage, C_1–C_3=0.2µF)

Characteristic	Symbol	Condition		Min.	Typ.	Max.	Unit
SVD voltage	V_{SVD}	SVDS0–3="0"		0.95	1.05	1.15	V
		SVDS0–3="1"		1.02	1.10	1.18	
		SVDS0–3="2"		1.07	1.15	1.23	
		SVDS0–3="3"		1.12	1.20	1.28	
		SVDS0–3="4"		1.16	1.25	1.34	
		SVDS0–3="5"		1.21	1.30	1.39	
		SVDS0–3="6"		1.30	1.40	1.50	
		SVDS0–3="7"		1.49	1.60	1.71	
		SVDS0–3="8"		1.81	1.95	2.09	
		SVDS0–3="9"		1.86	2.00	2.14	
		SVDS0–3="10"		1.91	2.05	2.19	
		SVDS0–3="11"		1.95	2.10	2.25	
		SVDS0–3="12"		2.05	2.20	2.35	
		SVDS0–3="13"		2.14	2.30	2.46	
		SVDS0–3="14"		2.33	2.50	2.68	
		SVDS0–3="15"		2.42	2.60	2.78	
SVD circuit response time	t_{SVD}					100	µS
Current consumption	I_{OP}	During HALT Normal mode *1	32.768kHz		2	3	µA
		During HALT Booster mode (V_{DD}=1.2V) *1	32.768kHz		2.5	5	µA
		During execution Normal mode *1	32.768kHz (Crystal oscillation)		4	6	µA
			60kHz (CR oscillation)		15	30	µA
			1.8MHz (CR oscillation)		500	800	µA
			4MHz (Ceramic oscillation)		900	1200	µA
		During execution Booster mode (V_{DD}=1.2V) *1	32.768kHz (Crystal oscillation)		8	12	µA

*1: The SVD circuit and the A/D converter are OFF. AV_{REF} is open.

● A/D Converter Characteristics

(Unless otherwise specified: AV_{DD}=V_{DD}=0.9 to 3.6V, AV_{SS}=V_{SS}=0V, Ta=-25 to 75°C)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Resolution			8	8	8	bit
Error		2.2V≤V_{DD}≤2.7V Fconv=OSC3/2≤1MHz or OSC1	-3		3	LSB
		1.6V≤V_{DD}≤2.2V Fconv=OSC1	-3		3	LSB
		0.9V≤V_{DD}≤1.6V Fconv=OSC1, VADSEL=1	-3		3	LSB
Convertion time	tconv	Fconv=OSC3/2=1MHz			21	µS
		Fconv=OSC1=32kHz			641	µS
Input voltage			AV_{SS}		AV_{REF}	V
Reference voltage	AV_{REF}		0.9		AV_{DD}	V
AV_{REF} resistance			15	20		kΩ

● Oscillation Characteristics

The oscillation characteristics change depending on the conditions (components used, board pattern, etc.). Use the following characteristics as reference values.

OSC1 Crystal Oscillation Circuit

(Unless otherwise specified: V_{DD}=3.0V, V_{SS}=0V, f_{OSC1}=32.768kHz, C_G=25pF, C_D=built-in, Ta=25°C)

Characteristic	Symbol	Condition		Min.	Typ.	Max.	Unit
Oscillation start voltage	Vsta	tsta≤3sec (V_{DD})		1.1			V
Oscillation stop voltage	Vstp	tstp≤10sec	Normal mode	1.1			V
		(V_{DD})	Booster mode	0.9			V
Built-in capacitance (drain)	C_D	Including the parasitic capacitance inside the IC (in chip)			14		pF
Frequency/voltage deviation	∂f/∂V	V_{DD}=0.9 to 3.6V	with VDC switching			10	ppm
			without VDC switching			5	ppm
Frequency/IC deviation	∂f/∂IC			-10		10	ppm
Frequency adjustment range	∂f/∂C_G	C_G=5 to 25pF		25	30		ppm
Harmonic oscillation start voltage	V_{hho}	C_G=5pF (V_{DD})		3.6			V
Permitted leak resistance	R_{leak}	Between OSC1 and V_{DD}, V_{SS}		200			MΩ

OSC1 CR Oscillation Circuit

(Unless otherwise specified: V_{DD}=3.0V, V_{SS}=0V, R_{CR1}=1.5MΩ, Ta=25°C, VDC=1)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation frequency dispersion	f_{OSC1}		-30	60kHz	30	%
Oscillation start voltage	Vsta	Normal mode (V_{DD})	2.2			V
Oscillation start time	tsta	V_{DD}=2.2 to 3.6V			3	mS
Oscillation stop voltage	Vstp	Normal mode (V_{DD})	2.2			V

(Unless otherwise specified: V_{DD}=3.0V, V_{SS}=0V, R_{CR1}=1MΩ, Ta=25°C, VDC=0)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation frequency dispersion	f_{OSC1}		-30	80kHz	30	%
Oscillation start voltage	Vsta	Normal mode (V_{DD})	1.3			V
Oscillation start time	tsta	V_{DD}=1.3 to 3.6V			3	mS
Oscillation stop voltage	Vstp	Normal mode (V_{DD})	1.3			V

OSC3 Ceramic Oscillation Circuit

(Unless otherwise specified: V_{DD}=3.0V, V_{SS}=0V, Ceramic oscillator: 4MHz, C_{GC}=C_{DC}=100pF, Ta=25°C)

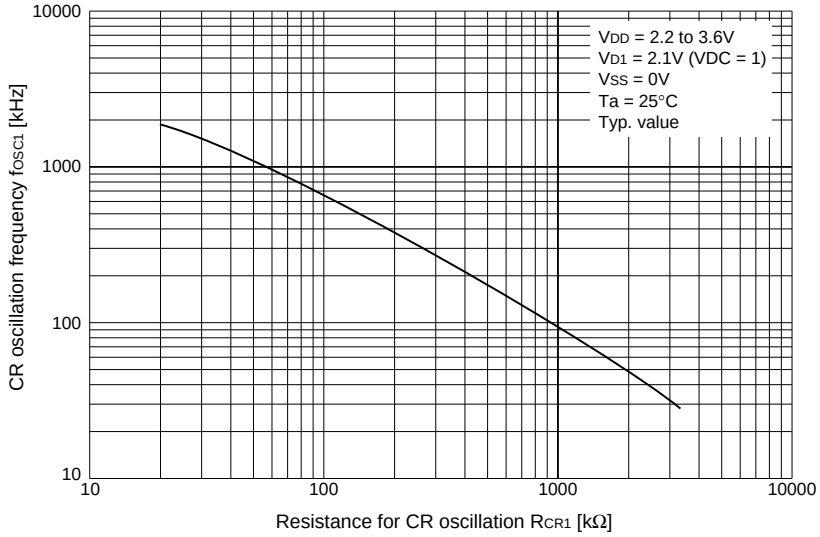
Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start voltage	Vsta	Normal mode (V_{DD})	2.2			V
Oscillation start time	tsta	V_{DD}=2.2 to 3.6V			5	mS
Oscillation stop voltage	Vstp	Normal mode (V_{DD})	2.2			V

OSC3 CR Oscillation Circuit

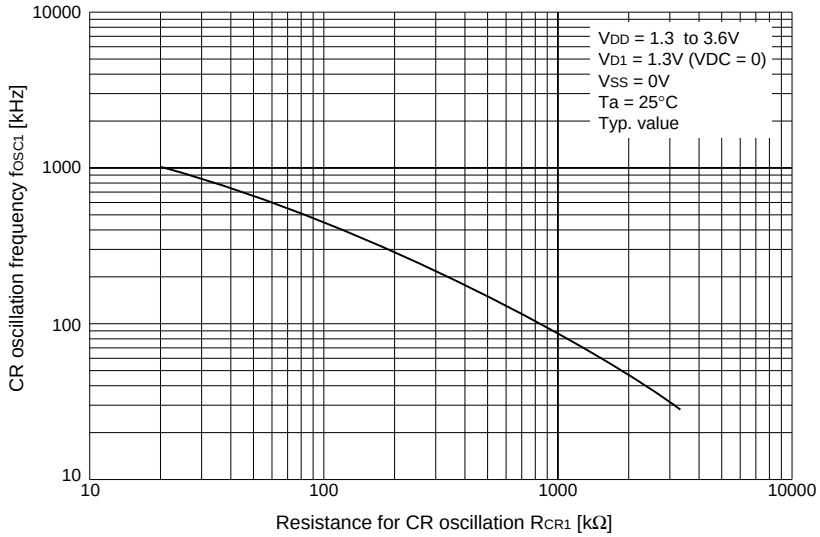
(Unless otherwise specified: V_{DD}=3.0V, V_{SS}=0V, R_{CR2}=40.2kΩ, Ta=25°C)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation frequency dispersion	f_{OSC3}		-30	1.8MHz	30	%
Oscillation start voltage	Vsta	Normal mode (V_{DD})	2.2			V
Oscillation start time	tsta	V_{DD}=2.2 to 3.6V			3	mS
Oscillation stop voltage	Vstp	Normal mode (V_{DD})	2.2			V

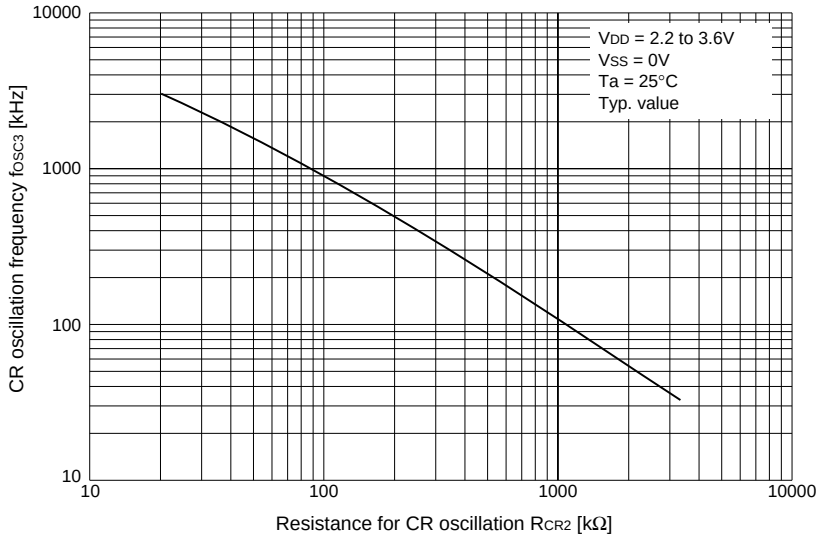
- **OSC1 CR oscillation frequency-resistance characteristic (VDC = 1)**



- **OSC1 CR oscillation frequency-resistance characteristic (VDC = 0)**



- **OSC3 CR oscillation frequency-resistance characteristic**



● Serial Interface AC Characteristics

Clock Synchronous Master Mode

• During 32 kHz operation

(Condition: V_{DD}=3.0V, V_{SS}=0V, Ta=25°C, V_{IH1}=0.8V_{DD}, V_{IL1}=0.2V_{DD}, V_{OH}=0.8V_{DD}, V_{OL}=0.2V_{DD})

Characteristic	Symbol	Min.	Typ.	Max.	Unit
Transmitting data output delay time	tsmd			5	µS
Receiving data input set-up time	tsms	10			µS
Receiving data input hold time	tsmh	5			µS

• During 1 MHz operation

(Condition: V_{DD}=3.0V, V_{SS}=0V, Ta=25°C, V_{IH1}=0.8V_{DD}, V_{IL1}=0.2V_{DD}, V_{OH}=0.8V_{DD}, V_{OL}=0.2V_{DD})

Characteristic	Symbol	Min.	Typ.	Max.	Unit
Transmitting data output delay time	tsmd			200	nS
Receiving data input set-up time	tsms	400			nS
Receiving data input hold time	tsmh	200			nS

Clock Synchronous Slave Mode

• During 32 kHz operation

(Condition: V_{DD}=3.0V, V_{SS}=0V, Ta=25°C, V_{IH1}=0.8V_{DD}, V_{IL1}=0.2V_{DD}, V_{OH}=0.8V_{DD}, V_{OL}=0.2V_{DD})

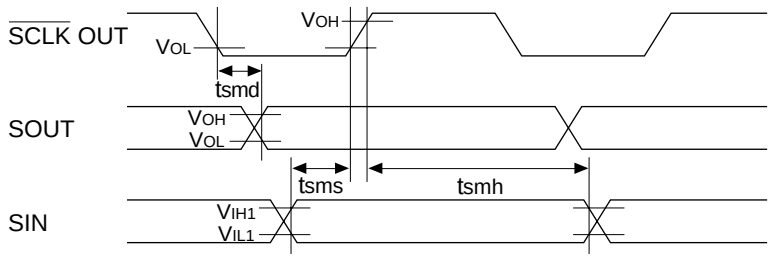
Characteristic	Symbol	Min.	Typ.	Max.	Unit
Transmitting data output delay time	tssd			10	µS
Receiving data input set-up time	tsss	10			µS
Receiving data input hold time	tssh	5			µS

• During 1 MHz operation

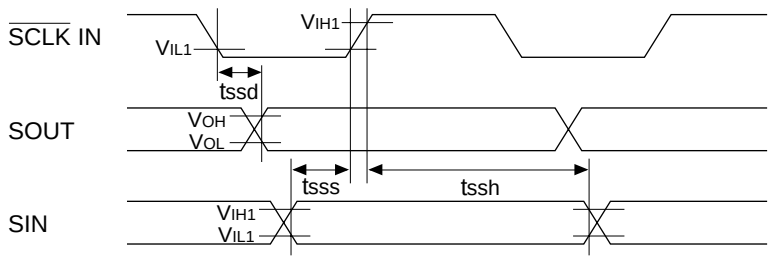
(Condition: V_{DD}=3.0V, V_{SS}=0V, Ta=25°C, V_{IH1}=0.8V_{DD}, V_{IL1}=0.2V_{DD}, V_{OH}=0.8V_{DD}, V_{OL}=0.2V_{DD})

Characteristic	Symbol	Min.	Typ.	Max.	Unit
Transmitting data output delay time	tssd			500	nS
Receiving data input set-up time	tsss	400			nS
Receiving data input hold time	tssh	200			nS

<Master mode>

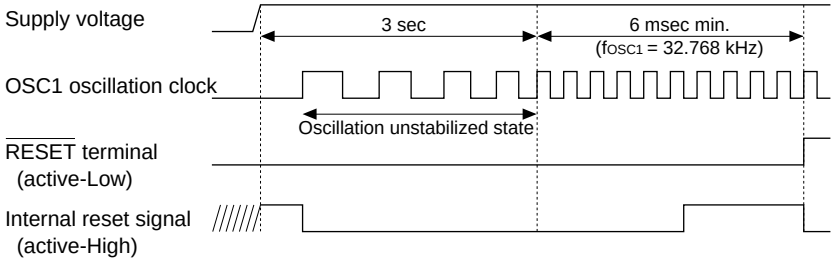


<Slave mode>

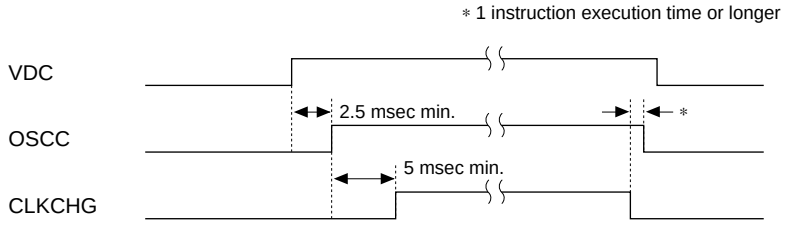


● Timing Chart

Reset

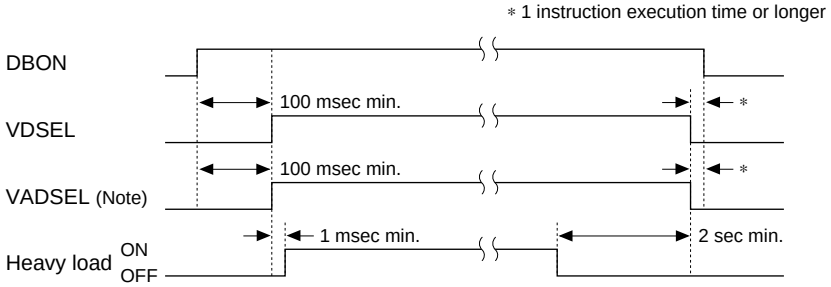


System clock switching



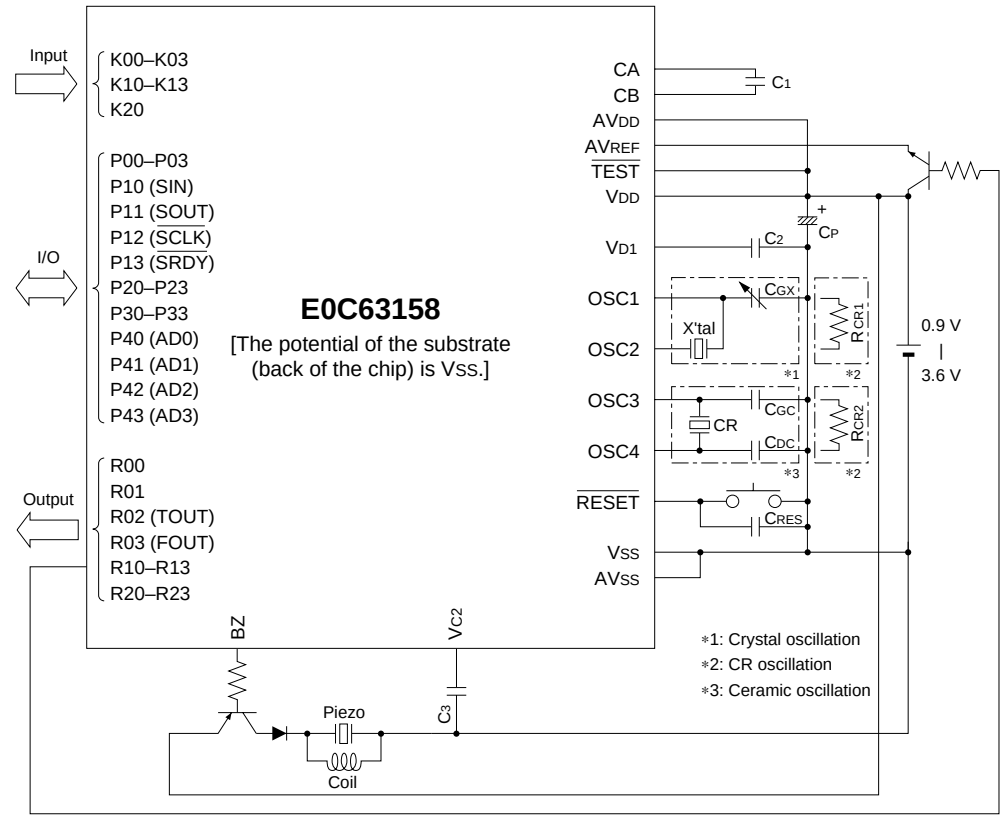
(Note) When the OSC1 oscillation circuit has been selected as the CR oscillation circuit, it is not necessary to set the VDC register.
Whether the VDC register value is "1" or "0" does not matter.

Supply voltage V_{C2} mode control during heavy load driving



(Note) VADSEL is used only when it is required.

■ BASIC EXTERNAL CONNECTION DIAGRAM



X'tal	Crystal oscillator	32.768 kHz, CI (Max.) = 34 kΩ
CGX	Trimmer capacitor	5–25 pF
RCR1	Resistor for OSC1 CR oscillation	1.5 MΩ (60 kHz)
CR	Ceramic oscillator	4 MHz (3.0 V)
CGC	Gate capacitor	100 pF
CDC	Drain capacitor	100 pF
RCR2	Resistor for OSC3 CR oscillation	40.2 kΩ (1.8 MHz)
C1–C3	Capacitor	0.2 µF
CP	Capacitor	3.3 µF
CRES	RESET terminal capacitor	0.1 µF

Note: The above table is simply an example, and is not guaranteed to work.

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