EPSON

E0C63358

4-bit Single Chip Microcomputer

Low Voltage Operation Products

■ DESCRIPTION

The E0C63358 is a microcomputer which has a high-performance 4-bit CPU E0C63000 as the core CPU, ROM (8,192 words × 13 bits), RAM (512 words × 4 bits), serial interface, watchdog timer, programmable timer, time base counter (1 system), SVD circuit, a segment type LCD driver that can drive a maximum 32 segments × 4 commons, a 4-channel A/D converter and a special input port that can implement key position discrimination function using with the A/D converter. The E0C63358 features low voltage/high speed (4MHz Max.) operation and low current consumption while the LCD is ON (current consumption in HALT: 2.5µA), this makes it suitable for battery driven portable equipment such as a head phone stereo.

■ FEATURES

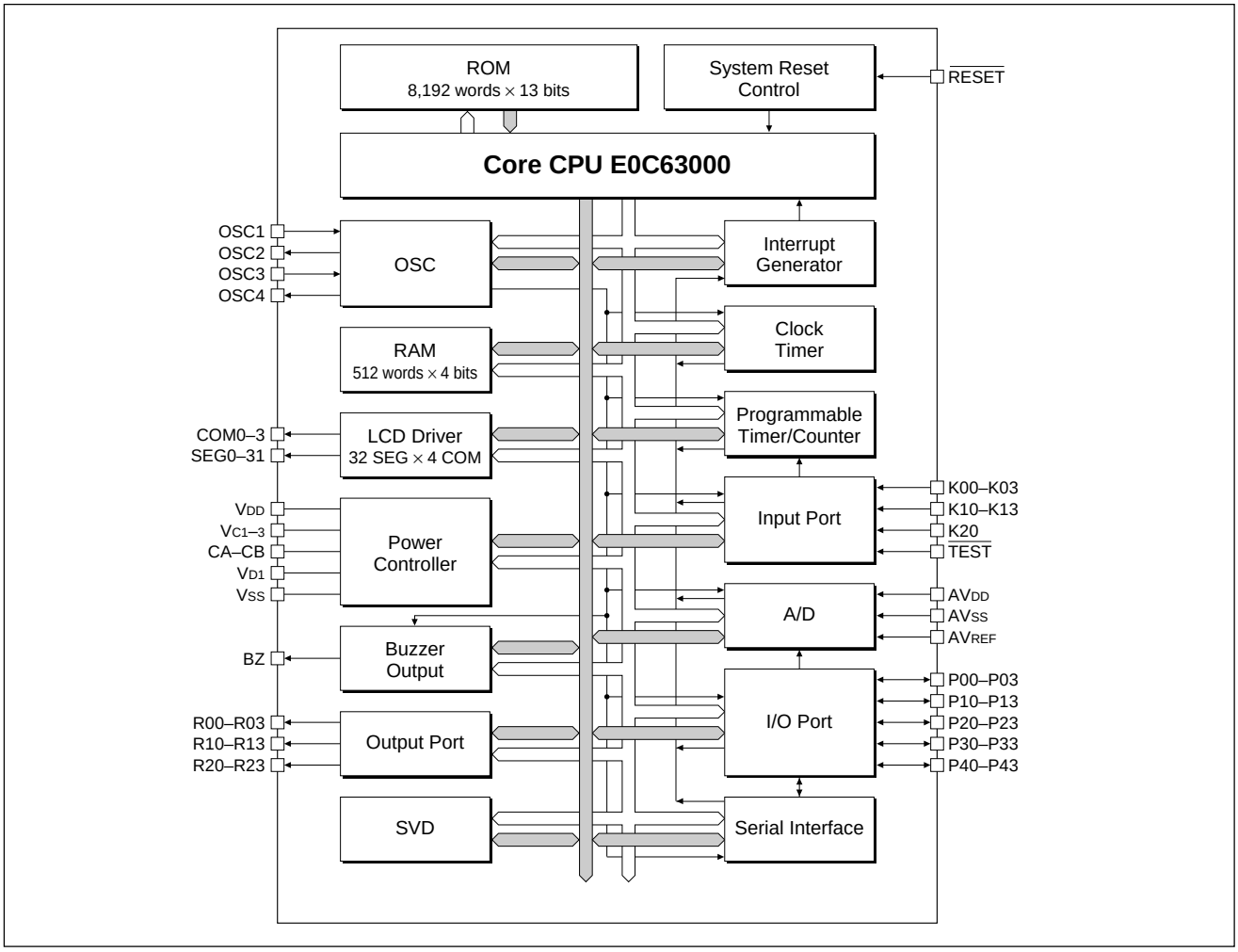
- CMOS LSI 4-bit parallel processing
- OSC1 oscillation circuit ..... 32.768kHz (Typ.) Crystal oscillation circuit or CR oscillation circuit (∗1)
- OSC3 oscillation circuit ..... 1.8MHz (Typ.) CR or 4MHz (Max.) Ceramic oscillation circuit (∗1)
  Operatable in 2.3V
- Instruction set ..... Basic instruction : 46 types (411 instructions with all)
  Addressing mode : 8 types
- Instruction execution time ..... During operation at 32.768kHz : Min. 61µsec
  During operation at 4MHz : Min. 0.5µsec
- ROM capacity ..... Code ROM : 8,192 words × 13 bits
- RAM capacity ..... Data memory : 512 words × 4 bits
  Display memory : 32 words × 4 bits
- Input port ..... 9 bits 8 bits (Pull-up resistors may be supplemented ∗1)
  1 bit (Input interrupt for key position sensing by A/D)
- Output port ..... 12 bits (It is possible to switch the 2 bits to special output ∗2)
- I/O port ..... 20 bits (It is possible to switch the 4 bits to serial input/output ∗2)
  (It is possible to switch the 4 bits to A/D input ∗2)
- Serial interface ..... 1 port (8-bit clock synchronous system)
- LCD driver ..... 32 segments × 4, 3 or 2 commons (∗2) 1/3 or 1/2 bias drive (∗1)
- Time base counter ..... 1 system (Clock timer)
- Programmable timer ..... Built-in, 2 channels × 8 bits, with event counter function
  or 1 channel × 16 bits (∗2)
- Watchdog timer ..... Built-in
- A/D converter ..... 8-bit resolution
  Maximum error :
  ±3 LSB, A/D clock : OSC1, OSC3, 2.7V to 3.6V
  ±3 LSB, A/D clock : OSC1, OSC3 ≤ 2.5MHz, 2.3V to 2.7V
  ±5 LSB, A/D clock : OSC1, 1.6V to 2.3V
  ±5 LSB, A/D clock : OSC1, 0.9V to 1.6V
- Buzzer output ..... Buzzer frequency : 2kHz or 4kHz (∗2), 2Hz interval (∗2)

- Supply voltage detection (SVD) circuit .. 16 values, programmable (1.05V to 2.60V)
- External interrupt ..... Input port interrupt : 2 systems
  Key sensing interrupt : 1 system
- Internal interrupt ..... Clock timer interrupt : 4 systems
  Programmable timer interrupt : 2 systems
  Serial interface interrupt : 1 system
  A/D converter : 1 system
- Power supply voltage ..... 0.9V to 3.6V (One battery or two batteries)
- Operating temperature range ..... -20°C to 70°C
- Current consumption (Typ.) ..... Single clock : During HALT (32kHz)
  1.5V (LCD power OFF) 2µA
  1.5V (LCD power ON) 2.5µA
  During operation (32kHz)
  1.5V (LCD power ON) 6µA
  Twin clock : During operation (4MHz)
  3.0V (LCD power ON) 900µA

Package ..... QFP15-100pin (plastic)

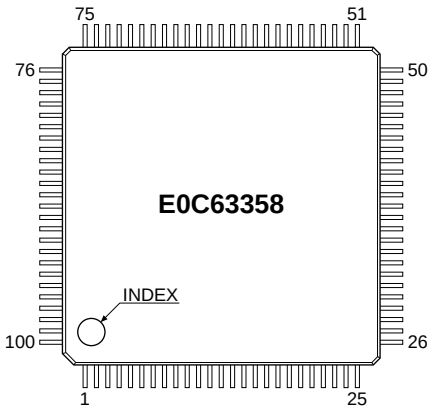
∗1: Can be selected with mask option ∗2: Can be selected with software

■ BLOCK DIAGRAM



■ PIN CONFIGURATION

QFP15-100pin



No.	Name	No.	Name	No.	Name	No.	Name
1	SEG7	26	N.C.	51	N.C.	76	R13
2	SEG8	27	N.C.	52	P43	77	R12
3	SEG9	28	COM0	53	P42	78	R11
4	SEG10	29	COM1	54	P41	79	R10
5	SEG11	30	COM2	55	P40	80	R03
6	SEG12	31	COM3	56	P33	81	R02
7	SEG13	32	CB	57	P32	82	R01
8	SEG14	33	CA	58	P31	83	R00
9	SEG15	34	V_{C3}	59	P30	84	BZ
10	SEG16	35	V_{C2}	60	P23	85	K00
11	SEG17	36	V_{C1}	61	P22	86	K01
12	SEG18	37	V_{SS}	62	P21	87	K02
13	SEG19	38	OSC1	63	P20	88	K03
14	SEG20	39	OSC2	64	P13	89	K10
15	SEG21	40	V_{D1}	65	P12	90	K11
16	SEG22	41	OSC3	66	P11	91	K12
17	SEG23	42	OSC4	67	P10	92	K13
18	SEG24	43	V_{DD}	68	P03	93	K20
19	SEG25	44	$\overline{RESET}$	69	P02	94	SEG0
20	SEG26	45	$\overline{TEST}$	70	P01	95	SEG1
21	SEG27	46	AV_{REF}	71	P00	96	SEG2
22	SEG28	47	AV_{DD}	72	R23	97	SEG3
23	SEG29	48	AV_{SS}	73	R22	98	SEG4
24	SEG30	49	N.C.	74	R21	99	SEG5
25	SEG31	50	N.C.	75	R20	100	SEG6

N.C. : No Connection

■ PIN DESCRIPTION

Pin name	Pin No.	In/Out	Function
V_{DD}	43	–	Power (+) supply pin
V_{SS}	37	–	Power (–) supply pin
V_{D1}	40	–	Oscillation/internal logic system regulated voltage output pin
V_{C1}–V_{C3}	36–34	–	LCD system power supply pin 1/3 or 1/2 bias (selected by mask option)
CA, CB	33, 32	–	LCD system boosting/reducing capacitor connecting pin
OSC1	38	I	Crystal or CR oscillation input pin (selected by mask option)
OSC2	39	O	Crystal or CR oscillation output pin (selected by mask option)
OSC3	41	I	Ceramic or CR oscillation input pin (selected by mask option)
OSC4	42	O	Ceramic or CR oscillation output pin (selected by mask option)
K00–K03	85–88	I	Input port
K10–K13	89–92	I	Input port
K20	93	I	Input port with control
P00–P03	71–68	I/O	I/O port
P10–P13	67–64	I/O	I/O port (switching to serial I/F input/output is possible by software)
P20–P23	63–60	I/O	I/O port
P30–P33	59–56	I/O	I/O port
P40–P43	55–52	I/O	I/O port (can be used as A/D input)
R00	83	O	Output port
R01	82	O	Output port
R02	81	O	Output port (switching to TOUT output is possible by software)
R03	80	O	Output port (switching to FOUT output is possible by software)
R10–R13	79–76	O	Output port
R20–R23	75–72	O	Output port
COM0–COM3	28–31	O	LCD common output pin (1/4, 1/3, 1/2 duty can be selected by software)
SEG0–SEG31	94–100, 1–25	O	LCD segment output pin
AV_{DD}	47	–	Power (+) supply pin for A/D converter
AV_{SS}	48	–	Power (–) supply pin for A/D converter
AV_{REF}	46	–	Reference voltage for A/D converter
BZ	84	O	Buzzer output pin
$\overline{RESET}$	44	I	Initial reset input pin
$\overline{TEST}$	45	I	Testing input pin

■ ELECTRICAL CHARACTERISTICS

● Absolute Maximum Ratings

(V_{SS}=0V)

Rating	Symbol	Value	Unit
Supply voltage	V_{DD}	-0.5 to 7.0	V
Input voltage (1)	V_I	-0.5 to V_{DD} + 0.3	V
Input voltage (2)	V_{IOSC}	-0.5 to V_{D1} + 0.3	V
Permissible total output current *1	ΣI_{VDD}	10	mA
Operating temperature	Topr	-20 to 70	°C
Storage temperature	Tstg	-65 to 150	°C
Soldering temperature / time	Tsol	260°C, 10sec (lead section)	–
Permissible dissipation *2	P_D	250	mW

*1: The permissible total output current is the sum total of the current (average current) that simultaneously flows from the output pins (or is draw in).
*2: In case of plastic package (QFP15-100pin).

● Recommended Operating Conditions

(Ta=-20 to 70°C)

Condition	Symbol	Remark		Min.	Typ.	Max.	Unit
Supply voltage	V_{DD}	V_{SS}=0V	Booster mode (OSC3 OFF)	0.9	1.1	1.4	V
			Normal mode (OSC3 OFF)	1.4	3.0	3.6	V
			Normal mode (OSC3 ON)	2.3	3.0	3.6	V
			OSC1 CR oscillation	2.3	3.0	3.6	V
	AV_{DD}	AV_{SS}=0V		0.9	3.0	3.6	V
	AV_{REF}						V
Oscillation frequency	f_{OSC1}	Crystal oscillation		–	32.768	–	kHz
		CR oscillation		40	60	80	kHz
	f_{OSC3}	CR oscillation			1800		kHz
		Ceramic oscillation				4100	kHz

● DC Characteristics

(Unless otherwise specified: V_{DD}=1.5V, V_{SS}=0V, f_{OSC1}=32.768kHz, Ta=25°C, V_{D1}/V_{C1}/V_{C2}/V_{C3} are internal voltage, C_1–C_5=0.2µF)

Characteristic	Symbol	Condition		Min.	Typ.	Max.	Unit
High level input voltage (1)	V_{IH1}		K00–03, K10–13, K20, P00–03 P10–13, P20–23, P30–33, P40–43	0.8·V_{DD}		V_{DD}	V
High level input voltage (2)	V_{IH2}		$\overline{RESET}$, $\overline{TEST}$	0.9·V_{DD}		V_{DD}	V
Low level input voltage (1)	V_{IL1}		K00–03, K10–13, K20, P00–03 P10–13, P20–23, P30–33, P40–43	0		0.2·V_{DD}	V
Low level input voltage (2)	V_{IL2}		$\overline{RESET}$, $\overline{TEST}$	0		0.1·V_{DD}	V
High level input current	I_{IH}	V_{IH}=1.5V	K00–03, K10–13, K20, P00–03 P10–13, P20–23, P30–33, P40–43 $\overline{RESET}$, $\overline{TEST}$	0		0.5	µA
Low level input current (1)	I_{IL1}	V_{IL1}=V_{SS} No Pull-up	K00–03, K10–13, K20, P00–03 P10–13, P20–23, P30–33, P40–43 $\overline{RESET}$, $\overline{TEST}$	-0.5		0	µA
Low level input current (2)	I_{IL2}	V_{IL2}=V_{SS} With Pull-up	K00–03, K10–13, K20, P00–03 P10–13, P20–23, P30–33, P40–43 $\overline{RESET}$, $\overline{TEST}$	-6	-3.5	-2.5	µA
High level output current (1)	I_{OH1}	V_{OH1}=0.9·V_{DD}	R00–03, R10–13, R20–23, P00–03 P10–13, P20–23, P30–33, P40–43			-0.3	mA
High level output current (2)	I_{OH2}	V_{OH2}=0.9·V_{DD}	BZ			-0.3	mA
Low level output current (1)	I_{OL1}	V_{OL1}=0.1·V_{DD}	R00–03, R10–13, R20–23, P00–03 P10–13, P20–23, P30–33, P40–43	0.5			mA
Low level output current (2)	I_{OL2}	V_{OL2}=0.1·V_{DD}	BZ	0.5			mA
Common output current	I_{OH3}	V_{OH3}=V_{C5}-0.05V	COM0–3			-10	µA
	I_{OL3}	V_{OL3}=V_{SS}+0.05V		10			µA
Segment output current (during LCD output)	I_{OH4}	V_{OH4}=V_{C5}-0.05V	SEG0–31			-10	µA
	I_{OL4}	V_{OL4}=V_{SS}+0.05V		10			µA
Segment output current (during DC output)	I_{OH5}	V_{OH5}=0.9·V_{DD}	SEG0–31			-50	µA
	I_{OL5}	V_{OL5}=0.1·V_{DD}		50			µA

(Unless otherwise specified: V_{DD}=3.0V, V_{SS}=0V, f_{OSC1}=32.768kHz, Ta=25°C, V_{D1}/V_{C1}/V_{C2}/V_{C3} are internal voltage, C_1–C_5=0.2µF)

Characteristic	Symbol	Condition		Min.	Typ.	Max.	Unit
High level input voltage (1)	V_{IH1}		K00–03, K10–13, K20, P00–03 P10–13, P20–23, P30–33, P40–43	0.8·V_{DD}		V_{DD}	V
High level input voltage (2)	V_{IH2}		$\overline{RESET}$, $\overline{TEST}$	0.9·V_{DD}		V_{DD}	V
Low level input voltage (1)	V_{IL1}		K00–03, K10–13, K20, P00–03 P10–13, P20–23, P30–33, P40–43	0		0.2·V_{DD}	V
Low level input voltage (2)	V_{IL2}		$\overline{RESET}$, $\overline{TEST}$	0		0.1·V_{DD}	V
High level input current	I_{IH}	V_{IH}=3.0V	K00–03, K10–13, K20, P00–03 P10–13, P20–23, P30–33, P40–43 $\overline{RESET}$, $\overline{TEST}$	0		0.5	µA
Low level input current (1)	I_{IL1}	V_{IL1}=V_{SS} No Pull-up	K00–03, K10–13, K20, P00–03 P10–13, P20–23, P30–33, P40–43 $\overline{RESET}$, $\overline{TEST}$	-0.5		0	µA
Low level input current (2)	I_{IL2}	V_{IL2}=V_{SS} With Pull-up	K00–03, K10–13, K20, P00–03 P10–13, P20–23, P30–33, P40–43 $\overline{RESET}$, $\overline{TEST}$	-12	-7	-5	µA
High level output current (1)	I_{OH1}	V_{OH1}=0.9·V_{DD}	R00–03, R10–13, R20–23, P00–03 P10–13, P20–23, P30–33, P40–43			-1.5	mA
High level output current (2)	I_{OH2}	V_{OH2}=0.9·V_{DD}	BZ			-1.5	mA
Low level output current (1)	I_{OL1}	V_{OL1}=0.1·V_{DD}	R00–03, R10–13, R20–23, P00–03 P10–13, P20–23, P30–33, P40–43	3			mA
Low level output current (2)	I_{OL2}	V_{OL2}=0.1·V_{DD}	BZ	3			mA
Common output current	I_{OH3}	V_{OH3}=V_{C5}-0.05V	COM0–3			-10	µA
	I_{OL3}	V_{OL3}=V_{SS}+0.05V		10			µA
Segment output current (during LCD output)	I_{OH4}	V_{OH4}=V_{C5}-0.05V	SEG0–31			-10	µA
	I_{OL4}	V_{OL4}=V_{SS}+0.05V		10			µA
Segment output current (during DC output)	I_{OH5}	V_{OH5}=0.9·V_{DD}	SEG0–31			-220	µA
	I_{OL5}	V_{OL5}=0.1·V_{DD}		220			µA

● Analog Circuit Characteristics and Current Consumption

(Unless otherwise specified: V_{DD}=3.0V, V_{SS}=0V, f_{OSC1}=32.768kHz, C_G=25pF, Ta=25°C, V_{D1}/V_{C1}/V_{C2}/V_{C3} are internal voltage, C_1–C_5=0.2µF)

Characteristic	Symbol	Condition		Min.	Typ.	Max.	Unit
LCD drive voltage	V_{C1}	Connect 1 MΩ load resistor between V_{SS} and V_{C1} (without panel load)		0.95	1.05	1.15	V
	V_{C2}	Connect 1 MΩ load resistor between V_{SS} and V_{C2} (without panel load)		2·V_{C1} ×0.9		2·V_{C1} +0.1	V
	V_{C3}	Connect 1 MΩ load resistor between V_{SS} and V_{C3} (without panel load)		3·V_{C1} ×0.9		3·V_{C1} +0.1	V
SVD voltage	V_{SVD}	SVDS0–3="0"		0.95	1.05	1.15	V
		SVDS0–3="1"		1.02	1.10	1.18	
		SVDS0–3="2"		1.07	1.15	1.23	
		SVDS0–3="3"		1.12	1.20	1.28	
		SVDS0–3="4"		1.16	1.25	1.34	
		SVDS0–3="5"		1.21	1.30	1.39	
		SVDS0–3="6"		1.30	1.40	1.50	
		SVDS0–3="7"		1.49	1.60	1.71	
		SVDS0–3="8"		1.81	1.95	2.09	
		SVDS0–3="9"		1.86	2.00	2.14	
		SVDS0–3="10"		1.91	2.05	2.19	
		SVDS0–3="11"		1.95	2.10	2.25	
		SVDS0–3="12"		2.05	2.20	2.35	
		SVDS0–3="13"		2.14	2.30	2.46	
		SVDS0–3="14"		2.33	2.50	2.68	
		SVDS0–3="15"		2.42	2.60	2.78	
SVD circuit response time	t_{SVD}					100	µS
Current consumption	I_{OP}	During HALT Normal mode LCD power OFF	32.768kHz		2	3	µA
		During HALT Normal mode *1 LCD power ON	32.768kHz		2.5	5	µA
		During HALT Booster mode (V_{DD}=1.2V) *1 LCD power ON	32.768kHz		2.5	5	µA
		During execution Normal mode *1 LCD power ON	32.768kHz (Crystal oscillation)		6	10	µA
			60kHz (CR oscillation)		30	60	µA
			1.8MHz (CR oscillation)		700	1000	µA
			4MHz (Ceramic oscillation)		900	1200	µA
		During execution Booster mode (V_{DD}=1.2V) *1 LCD power ON	32.768kHz (Crystal oscillation)		10	15	µA

*1: Without panel load. The SVD circuit and the A/D converter are OFF. AV_{REF} is open.

● A/D Converter Characteristics

(Unless otherwise specified: AV_{DD}=V_{DD}=0.9 to 3.6V, AV_{SS}=V_{SS}=0V, Ta=-25 to 75°C)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Resolution			8	8	8	bit
Error		2.7V≤V_{DD}≤3.6V Fconv=OSC3/2 or OSC1	-3		3	LSB
		2.2V≤V_{DD}≤2.7V Fconv=OSC3/2≤2.5MHz or OSC1	-3		3	LSB
		1.6V≤V_{DD}≤2.2V Fconv=OSC1 (only)	-5		5	LSB
		0.9V≤V_{DD}≤1.6V Fconv=OSC1 (only), VADSEL=1	-5		5	LSB
Convertion time	tconv	Fconv=OSC3/2=2MHz			10.5	µS
		Fconv=OSC1=32kHz			641	µS
Input voltage			AV_{SS}		AV_{REF}	V
Reference voltage	AV_{REF}		0.9		AV_{DD}	V
AV_{REF} resistance			15	20		kΩ

● Oscillation Characteristics

The oscillation characteristics change depending on the conditions (components used, board pattern, etc.). Use the following characteristics as reference values.

OSC1 Crystal Oscillation Circuit

(Unless otherwise specified:V_{DD}=3.0V, V_{SS}=0V, f_{OSC1}=32.768kHz, C_G=25pF, C_D=built-in, Ta=25°C)

Characteristic	Symbol	Condition		Min.	Typ.	Max.	Unit
Oscillation start voltage	Vsta	tsta≤3sec (V_{DD})		1.1			V
Oscillation stop voltage	Vstp	tstp≤10sec (V_{DD})	Normal mode	1.1			V
			Booster mode	0.9			V
Built-in capacitance (drain)	C_D	Including the parasitic capacitance inside the IC (in chip)			14		pF
Frequency/voltage deviation	∂f/∂V	V_{DD}=0.9 to 3.6V	with VDC switching			10	ppm
			without VDC switching			5	ppm
Frequency/IC deviation	∂f/∂IC			-10		10	ppm
Frequency adjustment range	∂f/∂C_G	C_G=5 to 25pF		25	30		ppm
Harmonic oscillation start voltage	V_{hho}	C_G=5pF (V_{DD})		3.6			V
Permitted leak resistance	R_{leak}	Between OSC1 and V_{DD}, V_{SS}		200			MΩ

OSC1 CR Oscillation Circuit

(Unless otherwise specified: V_{DD}=3.0V, V_{SS}=0V, R_{CR1}=600kΩ, Ta=25°C)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation frequency dispersion	f_{OSC1}		-30	60kHz	30	%
Oscillation start voltage	Vsta	Normal mode (V_{DD})	2.3			V
Oscillation start time	tsta	V_{DD}=2.3 to 3.6V			3	mS
Oscillation stop voltage	Vstp	Normal mode (V_{DD})	2.3			V

OSC3 Ceramic Oscillation Circuit

(Unless otherwise specified: V_{DD}=3.0V, V_{SS}=0V, Ceramic oscillator: 4MHz, C_{GC}=C_{DC}=100pF, Ta=25°C)

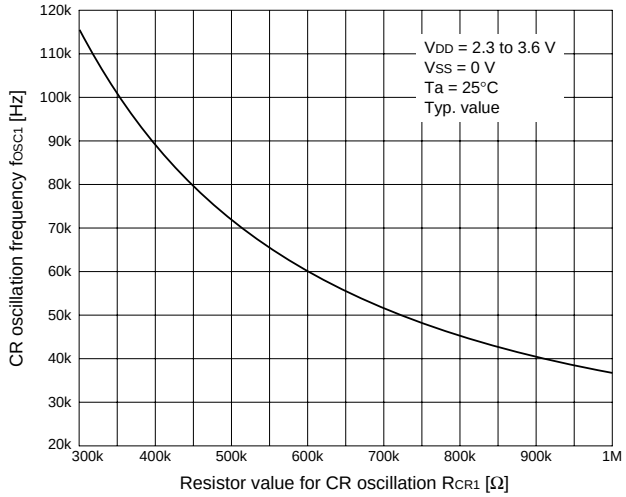
Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start voltage	Vsta	Normal mode (V_{DD})	2.3			V
Oscillation start time	tsta	V_{DD}=2.3 to 3.6V			5	mS
Oscillation stop voltage	Vstp	Normal mode (V_{DD})	2.3			V

OSC3 CR Oscillation Circuit

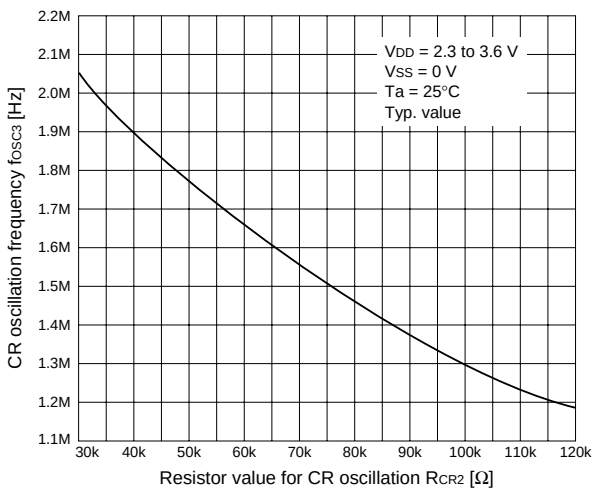
(Unless otherwise specified: V_{DD}=3.0V, V_{SS}=0V, R_{CR2}=47kΩ, Ta=25°C)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation frequency dispersion	f_{OSC3}		-30	1.8MHz	30	%
Oscillation start voltage	Vsta	Normal mode (V_{DD})	2.3			V
Oscillation start time	tsta	V_{DD}=2.3 to 3.6V			3	mS
Oscillation stop voltage	Vstp	Normal mode (V_{DD})	2.3			V

- **OSC1 CR oscillation frequency-resistance characteristic**



- **OSC3 CR oscillation frequency-resistance characteristic**



● Serial Interface AC Characteristics

Clock Synchronous Master Mode

• During 32 kHz operation

(Condition: V_{DD}=3.0V, V_{SS}=0V, Ta=25°C, V_{IH1}=0.8V_{DD}, V_{IL1}=0.2V_{DD}, V_{OH}=0.8V_{DD}, V_{OL}=0.2V_{DD})

Characteristic	Symbol	Min.	Typ.	Max.	Unit
Transmitting data output delay time	tsmd			5	µS
Receiving data input set-up time	tsms	10			µS
Receiving data input hold time	tsmh	5			µS

• During 1 MHz operation

(Condition: V_{DD}=3.0V, V_{SS}=0V, Ta=25°C, V_{IH1}=0.8V_{DD}, V_{IL1}=0.2V_{DD}, V_{OH}=0.8V_{DD}, V_{OL}=0.2V_{DD})

Characteristic	Symbol	Min.	Typ.	Max.	Unit
Transmitting data output delay time	tsmd			200	nS
Receiving data input set-up time	tsms	400			nS
Receiving data input hold time	tsmh	200			nS

Clock Synchronous Slave Mode

• During 32 kHz operation

(Condition: V_{DD}=3.0V, V_{SS}=0V, Ta=25°C, V_{IH1}=0.8V_{DD}, V_{IL1}=0.2V_{DD}, V_{OH}=0.8V_{DD}, V_{OL}=0.2V_{DD})

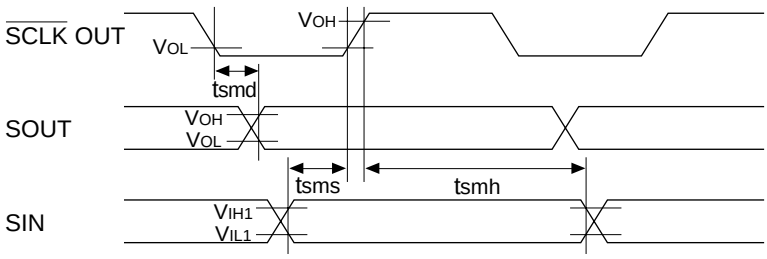
Characteristic	Symbol	Min.	Typ.	Max.	Unit
Transmitting data output delay time	tssd			10	µS
Receiving data input set-up time	tsss	10			µS
Receiving data input hold time	tssh	5			µS

• During 1 MHz operation

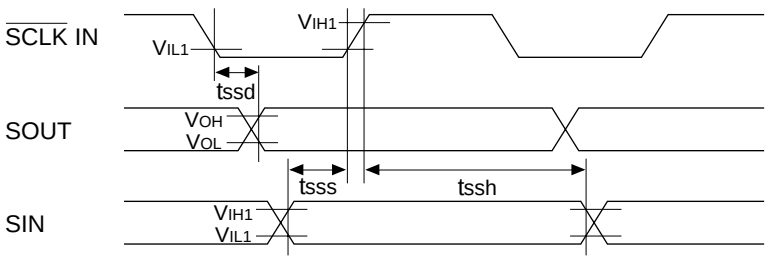
(Condition: V_{DD}=3.0V, V_{SS}=0V, Ta=25°C, V_{IH1}=0.8V_{DD}, V_{IL1}=0.2V_{DD}, V_{OH}=0.8V_{DD}, V_{OL}=0.2V_{DD})

Characteristic	Symbol	Min.	Typ.	Max.	Unit
Transmitting data output delay time	tssd			500	nS
Receiving data input set-up time	tsss	400			nS
Receiving data input hold time	tssh	200			nS

<Master mode>

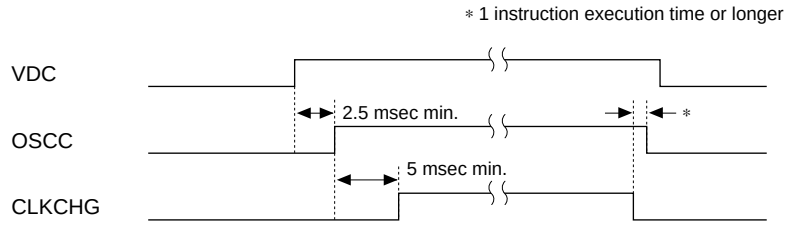


<Slave mode>



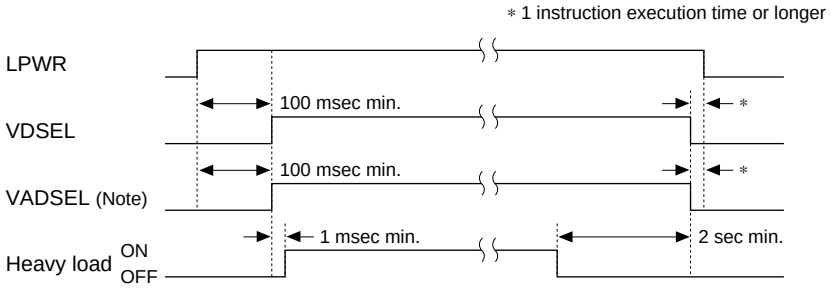
● Timing Chart

System clock switching



(Note) When the OSC1 oscillation circuit has been selected as the CR oscillation circuit, it is not necessary to set the VDC register.
Whether the VDC register value is "1" or "0" does not matter.

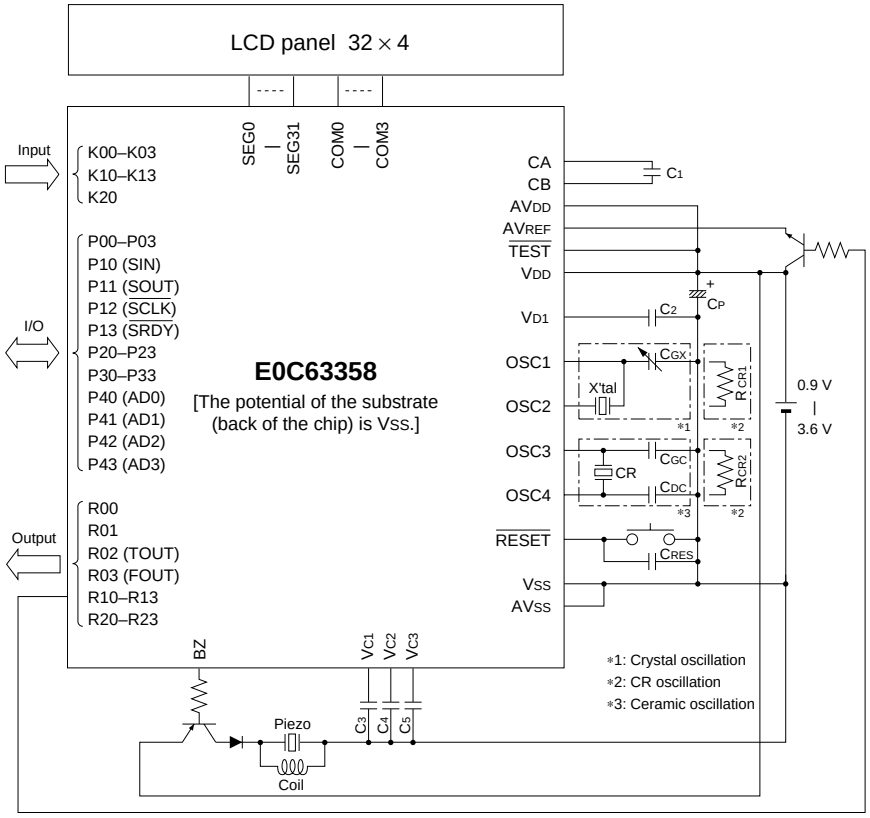
Supply voltage V_{C2} mode control during heavy load driving



(Note) VADSEL is used only when it is required.

■ BASIC EXTERNAL CONNECTION DIAGRAM

When negative polarity is selected for buzzer output (mask option selection)



X'tal	Crystal oscillator	32.768 kHz, CI (Max.) = 34 kΩ
CGX	Trimmer capacitor	5–25 pF
RCR1	Resistor for OSC1 CR oscillation	600 kΩ (60 kHz)
CR	Ceramic oscillator	4 MHz (3.0 V)
CGC	Gate capacitor	100 pF
CDC	Drain capacitor	100 pF
RCR2	Resistor for OSC3 CR oscillation	47 kΩ (1.8 MHz)
C1–C5	Capacitor	0.2 µF
CP	Capacitor	3.3 µF
CRES	RESET terminal capacitor	0.1 µF

Note: The above table is simply an example, and is not guaranteed to work.

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