EPSON

E0C63404

4-bit Single Chip Microcomputer

Wide Voltage Operation Products

- 4-bit Core CPU (2–6 clock / inst.)
- Dot-matrix Type LCD Driver
- Low Voltage Operation (1.8V Min.)
- Large Capacity RAM

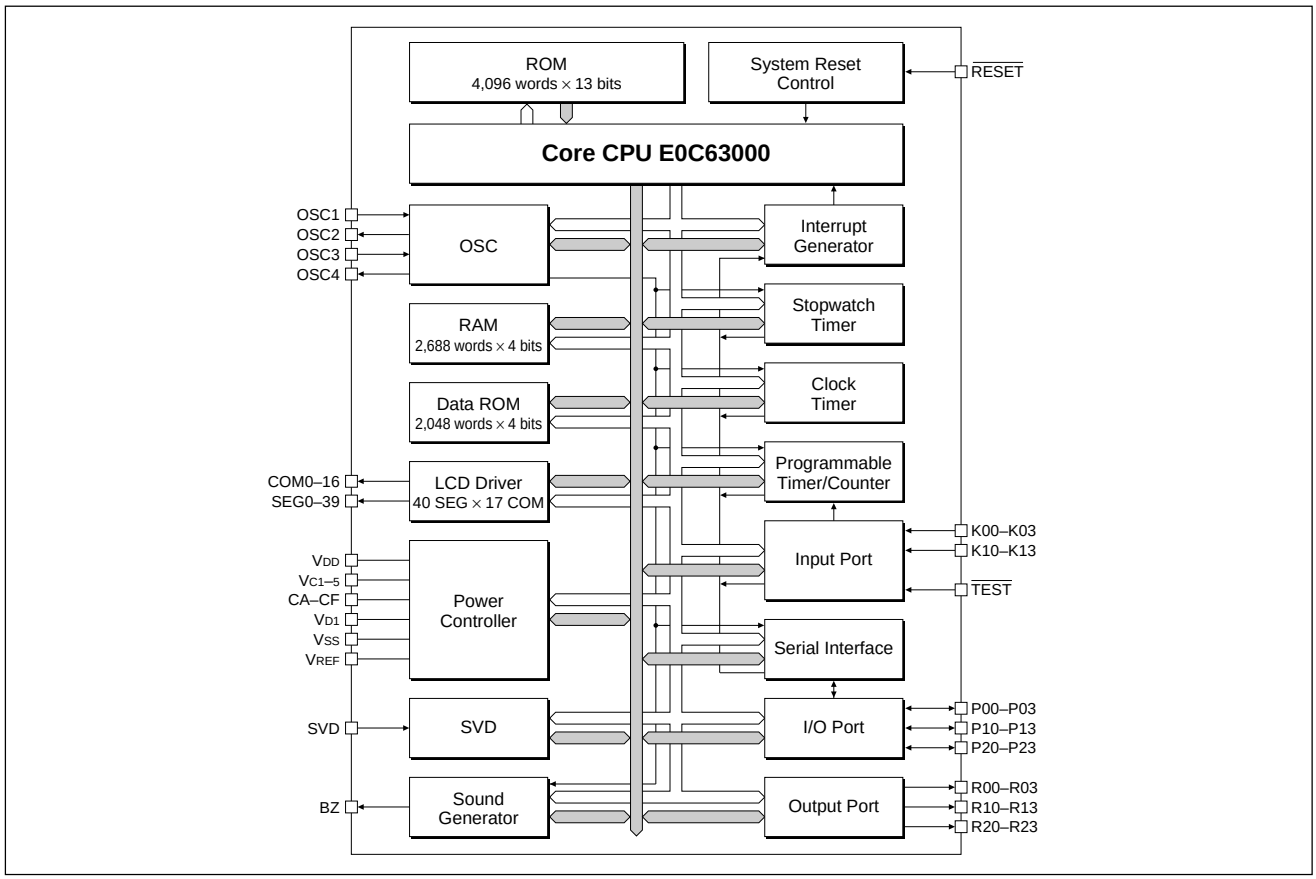
■ DESCRIPTION

The E0C63404 is a CMOS 4-bit microcomputer composed of a CMOS 4-bit core CPU, ROM, RAM, dot-matrix type LCD driver and timer. E0C63404 features high speed operation and low current consumption, this makes it suitable for applications working with batteries. It is also suitable for caller ID and portable data bank systems because it has a large capacity of RAM built-in.

■ FEATURES

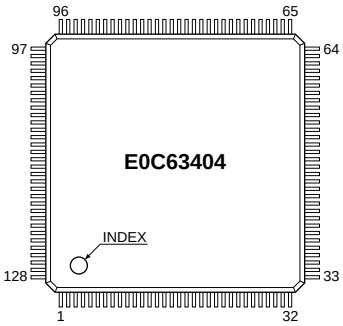
- CMOS LSI 4-bit parallel processing ..... E0C63000 core CPU
- Main clock ..... 32.768kHz (Typ.) Crystal oscillation or 60kHz (Typ.) CR oscillation
- Sub clock ..... 1MHz (Typ.) CR or Ceramic oscillation
- Instruction set ..... Basic instruction : 46 types (411 instructions with all)
  Addressing mode : 8 types
- Instruction execution time ..... During operation at 32.768kHz : 61µsec, 122µsec, 183µsec
  During operation at 60kHz : 33µsec, 67µsec, 100µsec
  During operation at 1MHz : 2µsec, 4µsec, 6µsec
- ROM capacity ..... Code ROM : 4,096 words × 13 bits
  Data ROM : 2,048 words × 4 bits
- RAM capacity ..... Data memory : 2,688 words × 4 bits
  Display memory : 200 words × 4 bits
- Input port ..... 8 bits
- Output port ..... 12 bits
- I/O port ..... 12 bits
- LCD driver ..... 40 segments × 8 / 16 / 17 commons
- Clock timer ..... 1 ch.
- Stopwatch timer ..... 1 ch.
- Programmable timer ..... 8 bits × 2 ch.
- Watchdog timer ..... Built-in
- Serial interface ..... 8-bit clock synchronous system
- Sound generator ..... With envelope and 1-shot output functions
- Supply voltage detection (SVD) circuit .... 16 values, programmable (1.85 to 3.30V)
- Interrupts ..... External : Input port interrupt 2 lines
  Internal : Clock timer interrupt 4 lines
  : Stopwatch timer interrupt 2 lines
  : Programmable timer interrupt 2 lines
  : Serial interface interrupt 1 line
- Supply voltage ..... 1.8 to 6.4V (Min. 2.2V when OSC3 and CR oscillation circuit are used)
- Current consumption ..... HALT mode (32.768kHz, LCD off) : 0.8µA
  OPERATING mode (32.768kHz, LCD on) : 10.0µA
- Package ..... QFP8-128pin (plastic), QFP15-128pin (plastic), Die form

■ BLOCK DIAGRAM

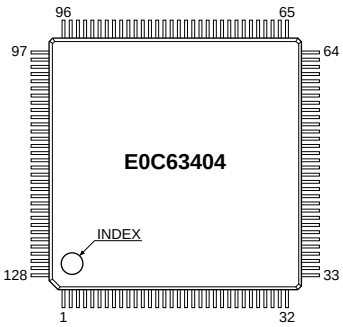


■ PIN CONFIGURATION

QFP8-128pin



QFP15-128pin



No.	Name	No.	Name	No.	Name	No.	Name
1	N.C.	33	R23	65	N.C.	97	N.C.
2	SEG3	34	R22	66	SVD	98	N.C.
3	SEG2	35	R21	67	N.C.	99	SEG32
4	SEG1	36	R20	68	N.C.	100	SEG31
5	SEG0	37	R13	69	V_{C1}	101	SEG30
6	COM7	38	R12	70	V_{C2}	102	SEG29
7	COM6	39	R11	71	V_{C3}	103	SEG28
8	COM5	40	R10	72	V_{C4}	104	SEG27
9	COM4	41	R03	73	V_{C5}	105	SEG26
10	COM3	42	R02	74	CF	106	SEG25
11	COM2	43	R01	75	CE	107	SEG24
12	COM1	44	R00	76	CD	108	SEG23
13	COM0	45	P23	77	CC	109	SEG22
14	N.C.	46	P22	78	CB	110	SEG21
15	N.C.	47	P21	79	CA	111	SEG20
16	N.C.	48	P20	80	COM8	112	SEG19
17	BZ	49	P13	81	COM9	113	SEG18
18	V_{SS}	50	P12	82	COM10	114	SEG17
19	OSC1	51	P11	83	COM11	115	SEG16
20	OSC2	52	P10	84	COM12	116	SEG15
21	V_{D1}	53	P03	85	COM13	117	SEG14
22	OSC3	54	P02	86	COM14	118	SEG13
23	OSC4	55	P01	87	COM15	119	SEG12
24	V_{DD}	56	P00	88	COM16	120	SEG11
25	N.C.	57	K13	89	SEG39	121	SEG10
26	N.C.	58	K12	90	SEG38	122	SEG9
27	N.C.	59	K11	91	SEG37	123	SEG8
28	$\overline{\text{RESET}}$	60	K10	92	SEG36	124	SEG7
29	$\overline{\text{TEST}}$	61	K03	93	SEG35	125	SEG6
30	V_{REF}	62	K02	94	SEG34	126	SEG5
31	N.C.	63	K01	95	SEG33	127	SEG4
32	N.C.	64	K00	96	N.C.	128	N.C.

N.C. : No Connection

■ PIN DESCRIPTION

Pin name	Pin No.	In/Out	Function
V_{DD}	24	–	Power (+) supply pin
V_{SS}	18	–	Power (–) supply pin
V_{D1}	21	–	Oscillation/internal logic system regulated voltage output pin
V_{C1}–V_{C5}	69–73	–	LCD system power supply pin 1/4 bias generated internally, 1/5 bias supplied externally (selected by mask option)
V_{REF}	30	O	LCD system power supply testing pin
CA–CF	79–74	–	LCD system boosting/reducing capacitor connecting pin
OSC1	19	I	Crystal or CR oscillation input pin (selected by mask option)
OSC2	20	O	Crystal or CR oscillation output pin (selected by mask option)
OSC3	22	I	Ceramic or CR oscillation input pin (selected by mask option)
OSC4	23	O	Ceramic or CR oscillation output pin (selected by mask option)
K00–K03	64–61	I	Input port
K10–K13	60–57	I	Input port
P00–P03	56–53	I/O	I/O port
P10–P13	52–49	I/O	I/O port (switching to serial I/F input/output is possible by software)
P20	48	I/O	I/O port
P21	47	I/O	I/O port
P22	46	I/O	I/O port (switching to CL signal output is possible by software)
P23	45	I/O	I/O port (switching to FR signal output is possible by software)
R00	44	O	Output port
R01	43	O	Output port
R02	42	O	Output port (switching to TOUT signal output is possible by software)
R03	41	O	Output port (switching to FOUT signal output is possible by software)
R10–R13	40–37	O	Output port
R20–R23	36–33	O	Output port
COM0–COM16	13–6, 80–88	O	LCD common output pin (1/8, 1/16, 1/17 duty can be selected by software)
SEG0–SEG39	5–2, 127–99, 95–89	O	LCD segment output pin
BZ	17	O	Sound output pin
SVD	66	I	SVD external voltage input pin
$\overline{\text{RESET}}$	28	I	Initial reset input pin
$\overline{\text{TEST}}$	29	I	Testing input pin

■ ELECTRICAL CHARACTERISTICS

● Absolute Maximum Ratings

(V_{SS}=0V)

Rating	Symbol	Value	Unit
Supply voltage	V_{DD}	-0.5 to 7.0	V
Input voltage (1)	V_I	-0.5 to V_{DD} + 0.3	V
Input voltage (2)	V_{IOSC}	-0.5 to V_{D1} + 0.3	V
Permissible total output current *1	ΣI_{VDD}	10	mA
Operating temperature	Topr	-20 to 70	°C
Storage temperature	Tstg	-65 to 150	°C
Soldering temperature / Time	Tsol	260°C, 10sec (lead section)	–
Permissible dissipation *2	P_D	250	mW

*1: The permissible total output current is the sum total of the current (average current) that simultaneously flows from the output pins (or is draw in).
*2: In case of plastic package (QFP8-128pin, QFP15-128pin).

● Recommended Operating Conditions

(Ta=-20 to 70°C)

Condition	Symbol	Remark		Min.	Typ.	Max.	Unit
Supply voltage	V_{DD}	V_{SS}=0V	OSC3 oscillation OFF	1.8	3.0	6.4	V
			OSC1 CR oscillation	2.2	3.0	6.4	V
			OSC3 oscillation ON	2.2	3.0	6.4	V
Oscillation frequency	f_{OSC1}	Crystal oscillation		–	32.768	–	kHz
		CR oscillation		40	60	80	kHz
	f_{OSC3}	Duty 50±5%, VDC="1", V_{DD}=2.2 to 6.5V		50	1,000	1,200	kHz
SVD terminal input voltage	SVD	V_{SS}=0V, SVD≤V_{DD}		0		6.4	V

● DC Characteristics

(Unless otherwise specified: V_{DD}=3.0V, V_{SS}=0V, f_{OSC1}=32.768kHz, Ta=25°C, V_{D1}/V_{C1}/V_{C2}/V_{C4}/V_{C5} are internal voltage, C_1–C_8=0.2µF)

Characteristic	Symbol	Condition		Min.	Typ.	Max.	Unit
High level input voltage (1)	V_{IH1}		K00–03, K10–13 P00–03, P10–13, P20–23	0.8•V_{DD}		V_{DD}	V
High level input voltage (2)	V_{IH2}		$\overline{RESET}$, $\overline{TEST}$	0.9•V_{DD}		V_{DD}	V
Low level input voltage (1)	V_{IL1}		K00–03, K10–13 P00–03, P10–13, P20–23	0		0.2•V_D	V
Low level input voltage (2)	V_{IL2}		$\overline{RESET}$, $\overline{TEST}$	0		0.1•V_{DD}	V
High level input current	I_{IH}	V_{IH}=3.0V	K00–03, K10–13 P00–03, P10–13, P20–23 $\overline{RESET}$, $\overline{TEST}$	0		0.5	µA
Low level input current (1)	I_{IL1}	V_{IL1}=V_{SS} No pull up	K00–03, K10–13 P00–03, P10–13, P20–23 $\overline{RESET}$, $\overline{TEST}$	-0.5		0	µA
Low level input current (2)	I_{IL2}	V_{IL2}=V_{SS} With pull up	K00–03, K10–13 P00–03, P10–13, P20–23 $\overline{RESET}$, $\overline{TEST}$	-16	-10	-6	µA
High level output current (1)	I_{OH1}	V_{OH1}=0.9•V_{DD}	R00–03, R10–13, R20–23 P00–03, P10–13, P20–23			-0.9	mA
High level output current (2)	I_{OH2}	V_{OH2}=0.9•V_{DD}	BZ			-0.9	mA
Low level output current (1)	I_{OL1}	V_{OL1}=0.1•V_{DD}	R00–03, R10–13, R20–23 P00–03, P10–13, P20–23	3.6			mA
Low level output current (2)	I_{OL2}	V_{OL2}=0.1•V_{DD}	BZ	3.6			mA
Common output current	I_{OH3}	V_{OH3}=V_{C5}-0.05V	COM0–COM16			-30	µA
	I_{OL3}	V_{OL3}=V_{SS}+0.05V		30			µA
Segment output current	I_{OH4}	V_{OH4}=V_{C5}-0.05V	SEG0–SEG39			-10	µA
	I_{OL4}	V_{OL4}=V_{SS}+0.05V		10			µA

(Unless otherwise specified: V_{DD}=5.0V, V_{SS}=0V, f_{OSC1}=32.768kHz, Ta=25°C, V_{D1}/V_{C1}/V_{C2}/V_{C4}/V_{C5} are internal voltage, C_1–C_8=0.2µF)

Characteristic	Symbol	Condition		Min.	Typ.	Max.	Unit
High level input voltage (1)	V_{IH1}		K00–03, K10–13 P00–03, P10–13, P20–23	0.8•V_{DD}		V_{DD}	V
High level input voltage (2)	V_{IH2}		$\overline{RESET}$, $\overline{TEST}$	0.9•V_{DD}		V_{DD}	V
Low level input voltage (1)	V_{IL1}		K00–03, K10–13 P00–03, P10–13, P20–23	0		0.2•V_D	V
Low level input voltage (2)	V_{IL2}		$\overline{RESET}$, $\overline{TEST}$	0		0.1•V_{DD}	V
High level input current	I_{IH}	V_{IH}=5.0V	K00–03, K10–13 P00–03, P10–13, P20–23 $\overline{RESET}$, $\overline{TEST}$	0		0.5	µA
Low level input current (1)	I_{IL1}	V_{IL1}=V_{SS} No pull up	K00–03, K10–13 P00–03, P10–13, P20–23 $\overline{RESET}$, $\overline{TEST}$	-0.5		0	µA
Low level input current (2)	I_{IL2}	V_{IL2}=V_{SS} With pull up	K00–03, K10–13 P00–03, P10–13, P20–23 $\overline{RESET}$, $\overline{TEST}$	-25	-15	-10	µA
High level output current (1)	I_{OH1}	V_{OH1}=0.9•V_{DD}	R00–03, R10–13, R20–23 P00–03, P10–13, P20–23			-2.4	mA
High level output current (2)	I_{OH2}	V_{OH2}=0.9•V_{DD}	BZ			-2.4	mA
Low level output current (1)	I_{OL1}	V_{OL1}=0.1•V_{DD}	R00–03, R10–13, R20–23 P00–03, P10–13, P20–23	9.4			mA
Low level output current (2)	I_{OL2}	V_{OL2}=0.1•V_{DD}	BZ	9.4			mA
Common output current	I_{OH3}	V_{OH3}=V_{C5}-0.05V	COM0–COM16			-30	µA
	I_{OL3}	V_{OL3}=V_{SS}+0.05V		30			µA
Segment output current	I_{OH4}	V_{OH4}=V_{C5}-0.05V	SEG0–SEG39			-10	µA
	I_{OL4}	V_{OL4}=V_{SS}+0.05V		10			µA

● Analog Circuit Characteristics

(Unless otherwise specified: V_{DD}=3.0V, V_{SS}=0V, f_{OSC1}=32.768kHz, C_G=25pF, Ta=25°C, V_{D1}/V_{C1}/V_{C2}/V_{C4}/V_{C5} are internal voltage, C_1–C_8=0.2µF)

Characteristic	Symbol	Condition		Min.	Typ.	Max.	Unit
LCD drive voltage (when V_{C1} standard is selected)	V_{C1}	Connect 1MΩ load resistor between V_{SS} and V_{C1} (No panel load)	LC0–3="0"		0.975		
			LC0–3="1"		0.990		
			LC0–3="2"		1.005		
			LC0–3="3"		1.020		
			LC0–3="4"		1.035		
			LC0–3="5"		1.050		
			LC0–3="6"		1.065		
			LC0–3="7"	Typ.×0.88	1.080	Typ.×1.12	V
			LC0–3="8"		1.095		
			LC0–3="9"		1.110		
			LC0–3="10"		1.125		
			LC0–3="11"		1.140		
			LC0–3="12"		1.155		
			LC0–3="13"		1.170		
			LC0–3="14"		1.185		
			LC0–3="15"		1.200		
	V_{C2}	Connect 1MΩ load resistor between V_{SS} and V_{C2} (No panel load)		2•V_{C1}		2•V_{C1} ×0.9	V
	V_{C4}	Connect 1MΩ load resistor between V_{SS} and V_{C4} (No panel load)		3•V_{C1}		3•V_{C1} ×0.9	V
	V_{C5}	Connect 1MΩ load resistor between V_{SS} and V_{C5} (No panel load)		4•V_{C1}		4•V_{C1} ×0.9	V
LCD drive voltage (when V_{C2} standard is selected)	V_{C1}	Connect 1MΩ load resistor between V_{SS} and V_{C1} (No panel load)		1/2•V_{C2} -0.1		1/2•V_{C2} ×0.95	V
	V_{C2}	Connect 1MΩ load resistor between V_{SS} and V_{C2} (No panel load)	LC0–3="0"		1.95		
			LC0–3="1"		1.98		
			LC0–3="2"		2.01		
			LC0–3="3"		2.04		
			LC0–3="4"		2.07		
			LC0–3="5"		2.10		
			LC0–3="6"		2.13		
			LC0–3="7"	Typ.×0.88	2.16	Typ.×1.12	V
			LC0–3="8"		2.19		
			LC0–3="9"		2.22		
			LC0–3="10"		2.25		
			LC0–3="11"		2.28		
			LC0–3="12"		2.31		
			LC0–3="13"		2.34		
			LC0–3="14"		2.37		
			LC0–3="15"		2.40		
	V_{C4}	Connect 1MΩ load resistor between V_{SS} and V_{C4} (No panel load)		3/2•V_{C2}		3/2•V_{C2} ×0.95	V
	V_{C5}	Connect 1MΩ load resistor between V_{SS} and V_{C5} (No panel load)		2•V_{C2}		2•V_{C2} ×0.95	V
SVD voltage	V_{SVD1}	SVDS0–3="0" (internal)		1.75	1.85	1.95	V
		SVDS0–3="1"		1.80	1.90	2.00	V
		SVDS0–3="2"		1.90	2.00	2.10	V
		SVDS0–3="3"		2.00	2.10	2.20	V
		SVDS0–3="4"		2.10	2.20	2.30	V
		SVDS0–3="5"		2.20	2.30	2.40	V
		SVDS0–3="6"		2.30	2.40	2.50	V
		SVDS0–3="7"		2.40	2.50	2.60	V
		SVDS0–3="8"		2.50	2.60	2.70	V
		SVDS0–3="9"		2.60	2.70	2.80	V
		SVDS0–3="10"		2.70	2.80	2.90	V
		SVDS0–3="11"		2.80	2.90	3.00	V
		SVDS0–3="12"		2.90	3.00	3.10	V
		SVDS0–3="13"		3.00	3.10	3.20	V
		SVDS0–3="14"		3.10	3.20	3.30	V
		SVDS0–3="15"		3.20	3.30	3.40	V
SVD voltage (external) *1	V_{SVD2}	SVDS0–3="0" (external)		0.95	1.05	1.15	V
SVD circuit response time	t_{SVD}					100	µS

*1; Please input the voltage, which is within the range between V_{SS} and V_{DD}, into the SVD terminal.

● Current Consumption

(Unless otherwise specified: V_{DD}=3.0V, V_{SS}=0V, f_{OSC1}=32.768kHz, C_G=25pF, Ta=25°C, V_{D1}/V_{C1}/V_{C2}/V_{C4}/V_{C5} are internal voltage, C_1–C_8=0.2µF)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Current consumption	I_{OP}	During HALT (32kHz crystal oscillation), LCD power OFF *1, *2, *3		0.8	2.0	µA
		During HALT (32kHz crystal oscillation), LCD power ON (V_{C1} standard) *1, *2, *3		6.5	12.0	µA
		During HALT (32kHz crystal oscillation), LCD power ON (V_{C2} standard) *1, *2, *3		4.5	8.0	µA
		During HALT (60kHz CR oscillation), LCD power OFF *1, *3		21	54	µA
		During HALT (60kHz CR oscillation), LCD power ON (V_{C1} standard) *1, *3		31	68	µA
		During HALT (60kHz CR oscillation), LCD power ON (V_{C2} standard) *1, *3		26	61	µA
		During execution (32kHz crystal oscillation), LCD power ON (V_{C1} standard) *1, *2, *3		10	19	µA
		During execution (60kHz CR oscillation), LCD power ON (V_{C1} standard) *1, *3		48	90	µA
		During execution (1MHz ceramic oscillation), LCD power ON (V_{C1} standard) *1		270	530	µA
		During execution (900kHz CR oscillation), LCD power ON (V_{C1} standard) *1		290	530	µA
		SVD circuit current (during supply voltage detection) V_{DD}=1.85 to 6.4V	2.0		10.0	µA
		SVD circuit current (during external voltage detection) V_{DD}=1.85 to 6.4V	0.5		3.0	µA

*1: No panel load. The SVD circuit is OFF.
*2: VDC="0"
*3: OSCC="0"

● Oscillation Characteristics

The oscillation characteristics change depending on the conditions (components used, board pattern, etc.). Use the following characteristics as reference values.

OSC1 crystal oscillation circuit

(Unless otherwise specified: V_{DD}=3.0V, V_{SS}=0V, f_{OSC1}=32.768kHz, C_G=25pF, C_D=built-in, Ta=25°C)

Characteristic	Symbol	Condition		Min.	Typ.	Max.	Unit
Oscillation start voltage	Vsta	tsta≤3sec (V_{DD})		1.8			V
Oscillation stop voltage	Vstp	tstp≤10sec (V_{DD})		1.8			V
Built-in capacitance (drain)	C_D	Including the parasitic capacity inside the IC (in chip)			14		pF
Frequency/voltage deviation	∂f/∂V	V_{DD}=0.9 to 6.4V	with VDC switching			5	ppm
			without VDC switching			10	ppm
Frequency/IC deviation	∂f/∂IC			-10		10	ppm
Frequency adjustment range	∂f/∂C_G	C_G=5 to 25pF		30	40		ppm
Harmonic oscillation start voltage	V_{hho}	C_G=5pF (V_{DD})		6.4			V
Permitted leak resistance	R_{leak}	Between OSC1 and V_{SS}		200			MΩ

OSC1 CR oscillation circuit

(Unless otherwise specified: V_{DD}=3.0V, V_{SS}=0V, R_{CR1}=510kΩ, Ta=25°C)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation frequency dispersion	f_{OSC1}		-30	60kHz	30	%
Oscillation start voltage	Vsta	(V_{DD})	2.2			V
Oscillation start time	tsta	V_{DD}=2.2 to 6.4V			3	mS
Oscillation stop voltage	Vstp	(V_{DD})	2.2			V

OSC3 CR oscillation circuit

(Unless otherwise specified: V_{DD}=3.0V, V_{SS}=0V, R_{CR2}=40.2kΩ, Ta=25°C)

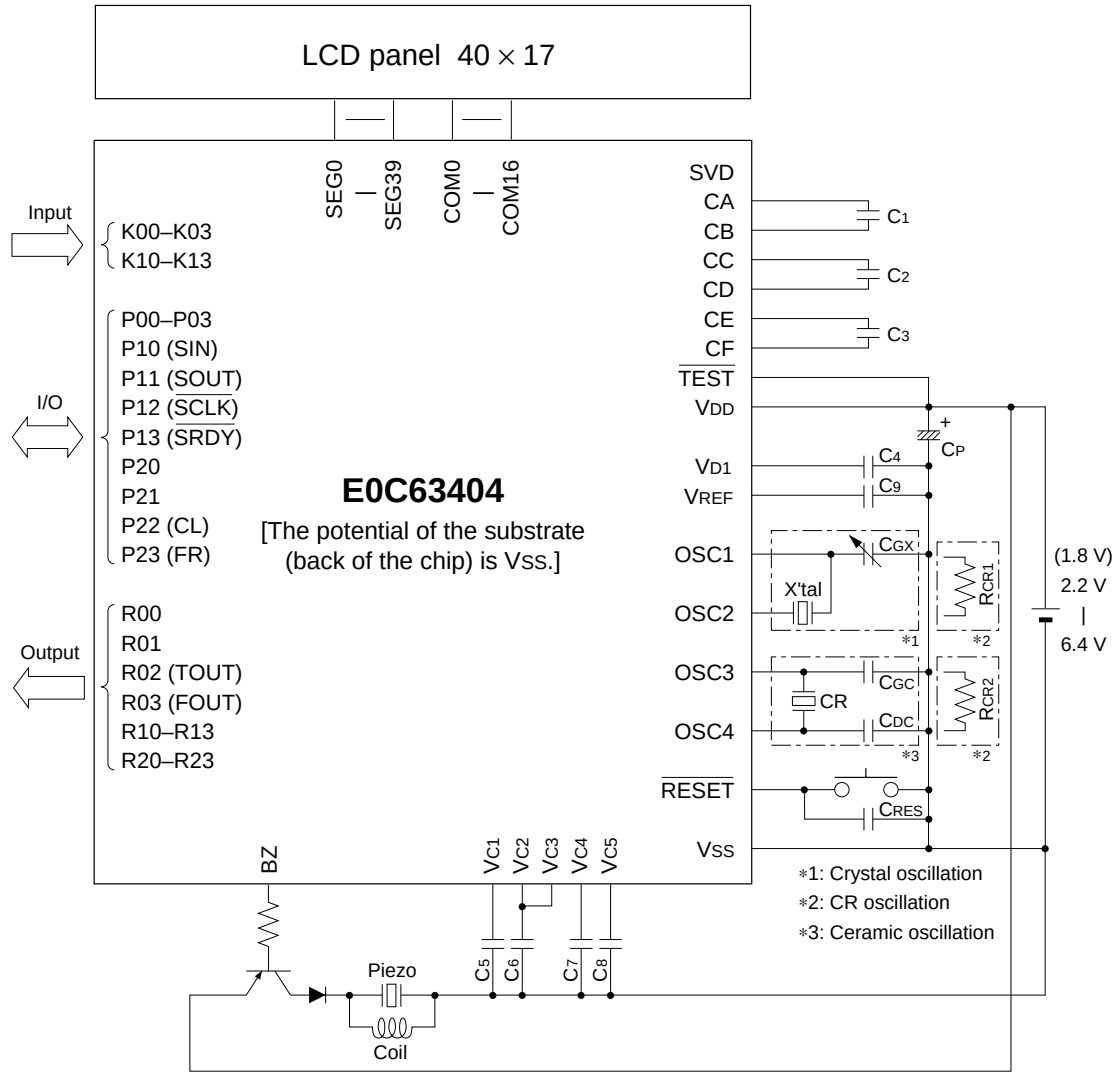
Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation frequency dispersion	f_{OSC3}		-30	900kHz	30	%
Oscillation start voltage	Vsta	(V_{DD})	2.2			V
Oscillation start time	tsta	V_{DD}=2.2 to 6.4V			3	mS
Oscillation stop voltage	Vstp	(V_{DD})	2.2			V

OSC3 ceramic oscillation circuit

(Unless otherwise specified: V_{DD}=3.0V, V_{SS}=0V, Ceramic oscillation: 1MHz, C_{GC}=C_{DC}=100pF, Ta=25°C)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start voltage	Vsta	(V_{DD})	2.2			V
Oscillation start time	tsta	V_{DD}=2.2 to 6.4V			5	mS
Oscillation stop voltage	Vstp	(V_{DD})	2.2			V

■ BASIC EXTERNAL CONNECTION DIAGRAM

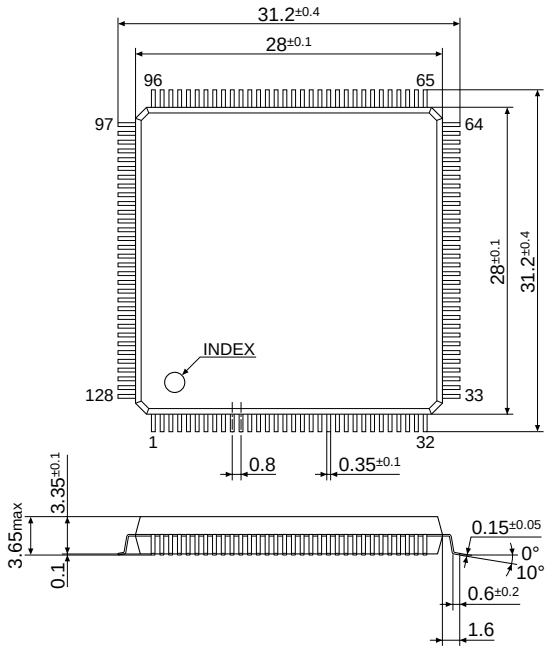


X'tal	Crystal oscillator	32.768 kHz, C_I (Max.) = 34 kΩ
C_{GX}	Trimmer capacitor	5–25 pF
R_{CR1}	Resistor for OSC1 CR oscillation	510 kΩ (60 kHz)
CR	Ceramic oscillator	1 MHz (3.0 V)
C_{GC}	Gate capacitor	100 pF
C_{DC}	Drain capacitor	100 pF
R_{CR2}	Resistor for OSC3 CR oscillation	40.2 kΩ (1 MHz)
C_1–C_8	Capacitor	0.2 µF
C_9	Capacitor	0.1 µF
C_P	Capacitor	3.3 µF
C_{RES}	$\overline{\text{RESET}}$ terminal capacitor	0.1 µF

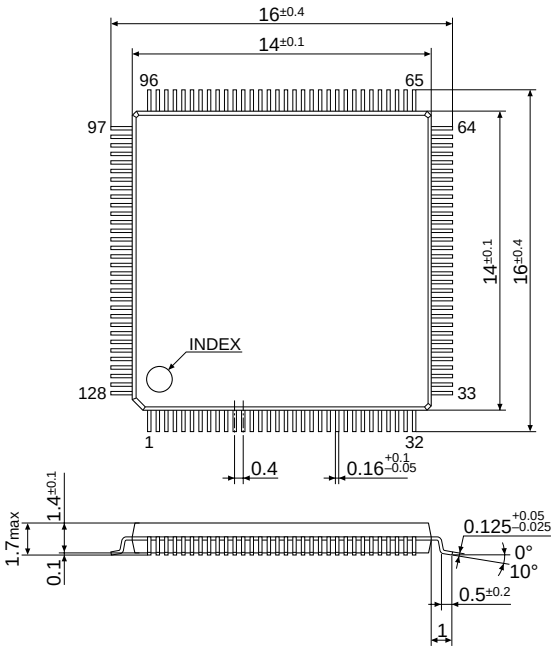
Note: The above table is simply an example, and is not guaranteed to work.

■ PACKAGE DIMENSIONS

Plastic QFP8-128pin



Plastic QFP15-128pin



Unit: mm

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