EPSON

E0C63454

4-bit Single Chip Microcomputer

Low Voltage Operation Products

- 4-bit E0C63000 Core CPU
- Built-in Dot-matrix Type LCD Driver
- Low Voltage Operation (1.8V min.)
- High Speed Instruction Cycle (2-6CPI)

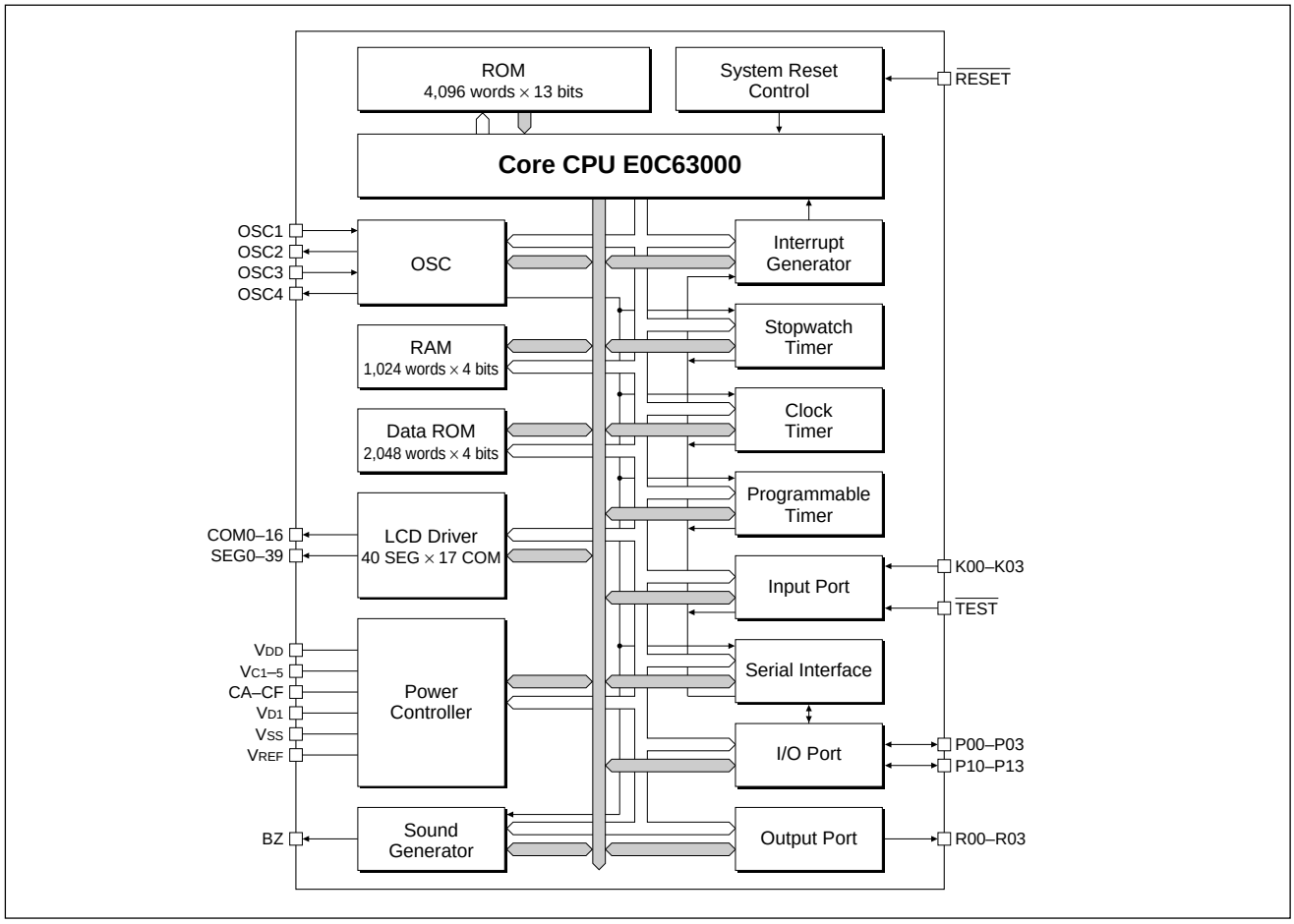
■ DESCRIPTION

The E0C63454 is a CMOS 4-bit microcomputer composed of a CMOS 4-bit core CPU, ROM, RAM, dot-matrix type LCD driver and counters. And the E0C63454 can be operated high speed and spend little current. The E0C63454 has a large RAM and LCD driver, so that the E0C63454 is best suited for systems such as Caller ID and Data-bank.

■ FEATURES

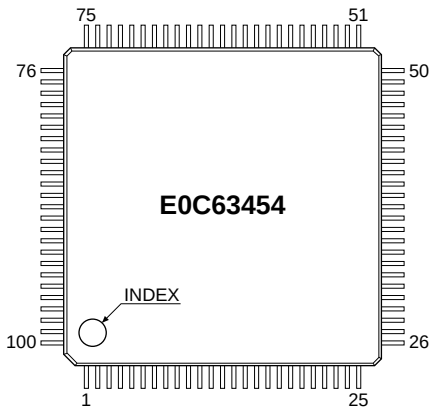
- CMOS LSI 4-bit parallel processing
- Main clock ..... 32.768kHz (Typ. X'tal)/60kHz (Typ. CR)
- Sub clock ..... 1.8MHz (Typ. CR)/4MHz (Max. Ceramic)
- Instruction set ..... 46 types (411 instructions with all)
- Instruction execution time ..... 32.768kHz : 61µsec (Min.)
  4MHz : 0.5µsec (Min.)
- ROM capacity ..... Code ROM : 4,096 words × 13 bits
  Data ROM : 2,048 words × 4 bits
- RAM capacity ..... Data memory : 1,024 words × 4 bits
  Display memory : 680 bits
- Input port ..... 4 bits
- Output port ..... 4 bits
- I/O port ..... 8 bits
- LCD driver ..... 40 segments × 8/16/17 commons
- Clock timer ..... 1 ch.
- Stopwatch timer ..... 1 ch.
- Programmable timer ..... 8 bits × 2 ch.
- Watchdog timer ..... Built-in
- Serial interface ..... Synchronous 8 bits
- Sound generator ..... With envelope and 1-shot output functions
- Supply voltage detection (SVD) circuit ..... 16 values by programmable (from 1.85 to 3.30V)
- Interrupts ..... External : Key interrupt 1 line
  Internal : Clock timer interrupt 4 lines
  : Stopwatch timer interrupt 2 lines
  : Programmable timer interrupt 2 lines
  : Serial interface interrupt 1 line
- Power supply voltage ..... 2.2 to 6.4V (Min. 1.8V with OSC1 X'tal oscillation circuit only)
- Current consumption ..... 1.0µA (32.768kHz, LCD off, 3.0V HALT)
  10.0µA (32.768kHz, LCD on, 3.0V RUN)
  1000µA (4MHz, LCD on, 3.0V RUN)
- Package ..... QFP15-100pin or Chip

■ BLOCK DIAGRAM



■ PIN CONFIGURATION

QFP15-100pin



No.	Name	No.	Name	No.	Name	No.	Name
1	SEG9	26	V_{DD}	51	V_{C1}	76	SEG34
2	SEG8	27	N.C.	52	V_{C2}	77	SEG33
3	SEG7	28	N.C.	53	V_{C3}	78	SEG32
4	SEG6	29	$\overline{RESET}$	54	V_{C4}	79	SEG31
5	SEG5	30	$\overline{TEST}$	55	V_{C5}	80	SEG30
6	SEG4	31	V_{REF}	56	CF	81	SEG29
7	SEG3	32	R03	57	CE	82	SEG28
8	SEG2	33	R02	58	CD	83	SEG27
9	SEG1	34	R01	59	CC	84	SEG26
10	SEG0	35	R00	60	CB	85	SEG25
11	COM7	36	P13	61	CA	86	SEG24
12	COM6	37	P12	62	COM8	87	SEG23
13	COM5	38	P11	63	COM9	88	SEG22
14	COM4	39	P10	64	COM10	89	SEG21
15	COM3	40	P03	65	COM11	90	SEG20
16	COM2	41	P02	66	COM12	91	SEG19
17	COM1	42	P01	67	COM13	92	SEG18
18	COM0	43	P00	68	COM14	93	SEG17
19	BZ	44	K03	69	COM15	94	SEG16
20	V_{SS}	45	K02	70	COM16	95	SEG15
21	OSC1	46	K01	71	SEG39	96	SEG14
22	OSC2	47	K00	72	SEG38	97	SEG13
23	V_{D1}	48	N.C.	73	SEG37	98	SEG12
24	OSC3	49	N.C.	74	SEG36	99	SEG11
25	OSC4	50	N.C.	75	SEG35	100	SEG10

N.C. : No Connection

■ PIN DESCRIPTION

Pin name	Pin No.	In/Out	Function
V_{DD}	26	–	Power (+) supply pin
V_{SS}	20	–	Power (–) supply pin
V_{D1}	23	–	Oscillation/internal logic system regulated voltage output pin
V_{C1}–V_{C5}	51–55	–	LCD system power supply pin 1/4 bias generated internally, 1/5 bias supplied externally (selected by mask option)
V_{REF}	31	O	LCD system power supply testing pin
CA–CF	61–56	–	LCD system boosting/reducing capacitor connecting pin
OSC1	21	I	Crystal or CR oscillation input pin (selected by mask option)
OSC2	22	O	Crystal or CR oscillation output pin (selected by mask option)
OSC3	24	I	Ceramic or CR oscillation input pin (selected by mask option)
OSC4	25	O	Ceramic or CR oscillation output pin (selected by mask option)
K00–K03	47–44	I	Input port
P00–P03	43–40	I/O	I/O port
P10–P13	39–36	I/O	I/O port (switching to serial I/F input/output is possible by software)
R00	35	O	Output port
R01	34	O	Output port
R02	33	O	Output port (switching to TOUT signal output is possible by software)
R03	32	O	Output port (switching to FOUT signal output is possible by software)
COM0–COM16	18–11, 62–70	O	LCD common output pin (1/8, 1/16, 1/17 duty can be selected by software)
SEG0–SEG39	10–1, 100–71	O	LCD segment output pin
BZ	19	O	Sound output pin
$\overline{RESET}$	29	I	Initial reset input pin
$\overline{TEST}$	30	I	Testing input pin

■ ELECTRICAL CHARACTERISTICS

● Absolute Maximum Ratings

(V_{SS}=0V)

Rating	Symbol	Value	Unit
Supply voltage	V_{DD}	-0.5 to 7.0	V
Input voltage (1)	V_I	-0.5 to V_{DD} + 0.3	V
Input voltage (2)	V_{IOSC}	-0.5 to V_{D1} + 0.3	V
Permissible total output current *1	ΣI_{VDD}	10	mA
Operating temperature	Topr	-20 to 70	°C
Storage temperature	Tstg	-65 to 150	°C
Soldering temperature / time	Tsol	260°C, 10sec (lead section)	–
Permissible dissipation *2	P_D	250	mW

*1: The permissible total output current is the sum total of the current (average current) that simultaneously flows from the output pins (or is draw in).
*2: In case of plastic package.

● Recommended Operating Conditions

(Ta=-20 to 70°C)

Condition	Symbol	Remark		Min.	Typ.	Max.	Unit
Supply voltage	V_{DD}	V_{SS}=0V	OSC3 oscillation OFF	1.8	3.0	6.4	V
			OSC1 CR oscillation	2.2	3.0	6.4	V
			OSC3 oscillation ON	2.2	3.0	6.4	V
Oscillation frequency	f_{OSC1}	Crystal oscillation		–	32.768	–	kHz
		CR oscillation		40	60	80	kHz
	f_{OSC3}	CR oscillation			1,800		kHz
		Ceramic oscillation				4,100	kHz

● DC Characteristics

(Unless otherwise specified: V_{DD}=3.0V, V_{SS}=0V, f_{OSC1}=32.768kHz, Ta=25°C, V_{D1}/V_{C1}/V_{C2}/V_{C4}/V_{C5} are internal voltage, C_1–C_8=0.2µF)

Characteristic	Symbol	Condition		Min.	Typ.	Max.	Unit
High level input voltage (1)	V_{IH1}		K00–03, P00–03, P10–13	0.8·V_{DD}		V_{DD}	V
High level input voltage (2)	V_{IH2}		$\overline{RESET}$, $\overline{TEST}$, P10–13	0.9·V_{DD}		V_{DD}	V
Low level input voltage (1)	V_{IL1}		K00–03, P00–03, P10–13	0		0.2·V_{DD}	V
Low level input voltage (2)	V_{IL2}		$\overline{RESET}$, $\overline{TEST}$, P10–13	0		0.1·V_{DD}	V
High level input current	I_{IH}	V_{IH}=3.0V	K00–03, P00–03, P10–13 $\overline{RESET}$, $\overline{TEST}$	0		0.5	µA
Low level input current (1)	I_{IL1}	V_{IL1}=V_{SS} No Pull-up	K00–03, P00–03, P10–13 $\overline{RESET}$, $\overline{TEST}$	-0.5		0	µA
Low level input current (2)	I_{IL2}	V_{IL2}=V_{SS} With Pull-up	K00–03, P00–03, P10–13 $\overline{RESET}$, $\overline{TEST}$	-12	-7	-5	µA
High level output current (1)	I_{OH1}	V_{OH1}=0.9·V_{DD}	R00–03, P00–03, P10–13			-2	mA
High level output current (2)	I_{OH2}	V_{OH2}=0.9·V_{DD}	BZ			-2	mA
Low level output current (1)	I_{OL1}	V_{OL1}=0.1·V_{DD}	R00–03, P00–03, P10–13	3			mA
Low level output current (2)	I_{OL2}	V_{OL2}=0.1·V_{DD}	BZ	3			mA
Common output current	I_{OH3}	V_{OH3}=V_{C5}-0.05V	COM0–16			-25	µA
	I_{OL3}	V_{OL3}=V_{SS}+0.05V		25			µA
Segment output current	I_{OH4}	V_{OH4}=V_{C5}-0.05V	SEG0–39			-10	µA
	I_{OL4}	V_{OL4}=V_{SS}+0.05V		10			µA

(Unless otherwise specified: V_{DD}=5.0V, V_{SS}=0V, f_{OSC1}=32.768kHz, Ta=25°C, V_{D1}/V_{C1}/V_{C2}/V_{C4}/V_{C5} are internal voltage, C_1–C_8=0.2µF)

Characteristic	Symbol	Condition		Min.	Typ.	Max.	Unit
High level input voltage (1)	V_{IH1}		K00–03, P00–03, P10–13	0.8·V_{DD}		V_{DD}	V
High level input voltage (2)	V_{IH2}		$\overline{RESET}$, $\overline{TEST}$, P10–13	0.9·V_{DD}		V_{DD}	V
Low level input voltage (1)	V_{IL1}		K00–03, P00–03, P10–13	0		0.2·V_{DD}	V
Low level input voltage (2)	V_{IL2}		$\overline{RESET}$, $\overline{TEST}$, P10–13	0		0.1·V_{DD}	V
High level input current	I_{IH}	V_{IH}=5.0V	K00–03, P00–03, P10–13 $\overline{RESET}$, $\overline{TEST}$	0		0.5	µA
Low level input current (1)	I_{IL1}	V_{IL1}=V_{SS} No Pull-up	K00–03, P00–03, P10–13 $\overline{RESET}$, $\overline{TEST}$	-0.5		0	µA
Low level input current (2)	I_{IL2}	V_{IL2}=V_{SS} With Pull-up	K00–03, P00–03, P10–13 $\overline{RESET}$, $\overline{TEST}$	-20	-12	-9	µA
High level output current (1)	I_{OH1}	V_{OH1}=0.9·V_{DD}	R00–03, P00–03, P10–13			-5	mA
High level output current (2)	I_{OH2}	V_{OH2}=0.9·V_{DD}	BZ			-5	mA
Low level output current (1)	I_{OL1}	V_{OL1}=0.1·V_{DD}	R00–03, P00–03, P10–13	7.5			mA
Low level output current (2)	I_{OL2}	V_{OL2}=0.1·V_{DD}	BZ	7.5			mA
Common output current	I_{OH3}	V_{OH3}=V_{C5}-0.05V	COM0–16			-25	µA
	I_{OL3}	V_{OL3}=V_{SS}+0.05V		25			µA
Segment output current	I_{OH4}	V_{OH4}=V_{C5}-0.05V	SEG0–39			-10	µA
	I_{OL4}	V_{OL4}=V_{SS}+0.05V		10			µA

● Analog Circuit Characteristics and Current Consumption

(Unless otherwise specified: V_{DD}=3.0V, V_{SS}=0V, f_{OSC1}=32.768kHz, C_G=25pF, R_{CR1}=600kΩ, R_{CR2}=47kΩ, Ta=25°C
V_{D1}/V_{C1}/V_{C2}/V_{C4}/V_{C5} are internal voltage, C_1–C_8=0.2µF)

Characteristic	Symbol	Condition		Min.	Typ.	Max.	Unit
LCD drive voltage (when V_{C1} standard is selected)	V_{C1}	Connect 1 MΩ load resistor between V_{SS} and V_{C1} (without panel load)	LC0–3="0"	Typ. ×0.88	0.975	Typ. ×1.12	V
			LC0–3="1"		0.990		
			LC0–3="2"		1.005		
			LC0–3="3"		1.020		
			LC0–3="4"		1.035		
			LC0–3="5"		1.050		
			LC0–3="6"		1.065		
			LC0–3="7"		1.080		
			LC0–3="8"		1.095		
			LC0–3="9"		1.110		
			LC0–3="10"		1.125		
			LC0–3="11"		1.140		
			LC0–3="12"		1.155		
			LC0–3="13"		1.170		
			LC0–3="14"		1.185		
			LC0–3="15"		1.200		
	V_{C2}	Connect 1 MΩ load resistor between V_{SS} and V_{C2} (without panel load)		$2 \cdot V_{C1}$ ×0.9		$2 \cdot V_{C1}$	V
	V_{C4}	Connect 1 MΩ load resistor between V_{SS} and V_{C4} (without panel load)		$3 \cdot V_{C1}$ ×0.9		$3 \cdot V_{C1}$	V
	V_{C5}	Connect 1 MΩ load resistor between V_{SS} and V_{C5} (without panel load)		$4 \cdot V_{C1}$ ×0.9		$4 \cdot V_{C1}$	V
LCD drive voltage (when V_{C2} standard is selected)	V_{C1}	Connect 1 MΩ load resistor between V_{SS} and V_{C1} (without panel load)		$1/2 \cdot V_{C2}$ ×0.95		$1/2 \cdot V_{C2}$ +0.1	V
	V_{C2}	Connect 1 MΩ load resistor between V_{SS} and V_{C2} (without panel load)	LC0–3="0"	Typ. ×0.88	1.95	Typ. ×1.12	V
			LC0–3="1"		1.98		
			LC0–3="2"		2.01		
			LC0–3="3"		2.04		
			LC0–3="4"		2.07		
			LC0–3="5"		2.10		
			LC0–3="6"		2.13		
			LC0–3="7"		2.16		
			LC0–3="8"		2.19		
			LC0–3="9"		2.22		
			LC0–3="10"		2.25		
			LC0–3="11"		2.28		
			LC0–3="12"		2.31		
			LC0–3="13"		2.34		
			LC0–3="14"		2.37		
			LC0–3="15"		2.40		
	V_{C4}	Connect 1 MΩ load resistor between V_{SS} and V_{C4} (without panel load)		$3/2 \cdot V_{C2}$ ×0.95		$3/2 \cdot V_{C2}$	V
	V_{C5}	Connect 1 MΩ load resistor between V_{SS} and V_{C5} (without panel load)		$2 \cdot V_{C2}$ ×0.95		$2 \cdot V_{C2}$	V
Current consumption	I_{OP}	HALT (32 kHz crystal), LCD power OFF	*1, *2		1	2	µA
		HALT (32 kHz crystal), LCD power ON (V_{C1} standard)	*1, *2		6	12	µA
		HALT (32 kHz crystal), LCD power ON (V_{C2} standard)	*1, *2		4	8	µA
		HALT (60 kHz CR), LCD power OFF	*2		23	45	µA
		HALT (60 kHz CR), LCD power ON (V_{C1} standard)	*2		30	60	µA
		HALT (60 kHz CR), LCD power ON (V_{C2} standard)	*2		26	50	µA
		RUN (32 kHz crystal), LCD power ON (V_{C1} standard)	*1, *2		10	19	µA
		RUN (60 kHz CR), LCD power ON (V_{C1} standard)	*2		45	80	µA
		RUN (2 MHz ceramic), LCD power ON (V_{C1} standard)			500	700	µA
		RUN (4 MHz ceramic), LCD power ON (V_{C1} standard)			1,000	1,200	µA
		RUN (1,800 kHz CR), LCD power ON (V_{C1} standard)			700	1,000	µA

*1: VDC = "0"
*2: OSCC = "0"

● Oscillation Characteristics

The oscillation characteristics change depending on the conditions (components used, board pattern, etc.). Use the following characteristics as reference values.

OSC1 Crystal Oscillation Circuit

(Unless otherwise specified: V_{DD}=3.0V, V_{SS}=0V, f_{OSC1}=32.768kHz, C_G=25pF, C_D=built-in, Ta=-20 to 70°C)

Characteristic	Symbol	Condition		Min.	Typ.	Max.	Unit
Oscillation start voltage	Vsta	tsta≤3sec (V_{DD})		1.8			V
Oscillation stop voltage	Vstp	tstp≤10sec (V_{DD})		1.8			V
Built-in capacitance (drain)	C_D	Including the parasitic capacitance inside the IC (in chip)			14		pF
Frequency/voltage deviation	∂f/∂V	V_{DD}=2.2 to 6.4V	with VDC switching			5	ppm
			without VDC switching			10	ppm
Frequency/IC deviation	∂f/∂IC			-10		10	ppm
Frequency adjustment range	∂f/∂C_G	C_G=5 to 25pF		10	20		ppm
Harmonic oscillation start voltage	V_{hho}	C_G=5pF (V_{DD})		6.4			V
Permitted leak resistance	R_{leak}	Between OSC1 and V_{SS}		200			MΩ

OSC1 CR Oscillation Circuit

(Unless otherwise specified: V_{DD}=3.0V, V_{SS}=0V, R_{CR1}=520kΩ, Ta=-20 to 70°C)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation frequency dispersion	f_{OSC1}		-30	60kHz	30	%
Oscillation start voltage	Vsta	(V_{DD})	2.2			V
Oscillation start time	tsta	V_{DD}=2.2 to 6.4V			3	mS
Oscillation stop voltage	Vstp	(V_{DD})	2.2			V

OSC3 Ceramic Oscillation Circuit

(Unless otherwise specified: V_{DD}=3.0V, V_{SS}=0V, Ceramic oscillator: 4MHz, C_{GC}=C_{DC}=30pF, Ta=-20 to 70°C)

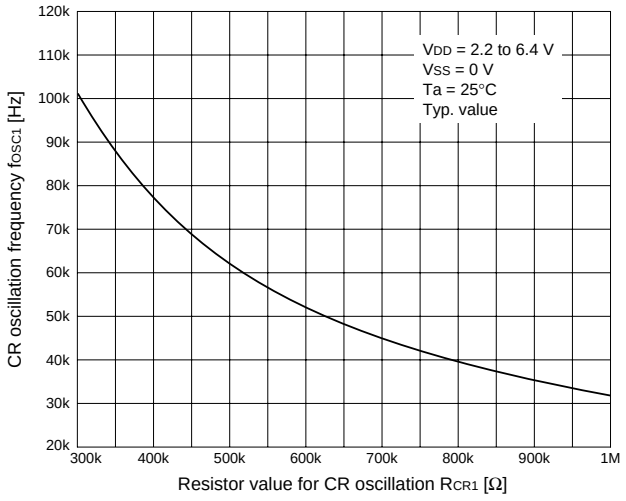
Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start voltage	Vsta	(V_{DD})	2.2			V
Oscillation start time	tsta	V_{DD}=2.2 to 6.4V			5	mS
Oscillation stop voltage	Vstp	(V_{DD})	2.2			V

OSC3 CR Oscillation Circuit

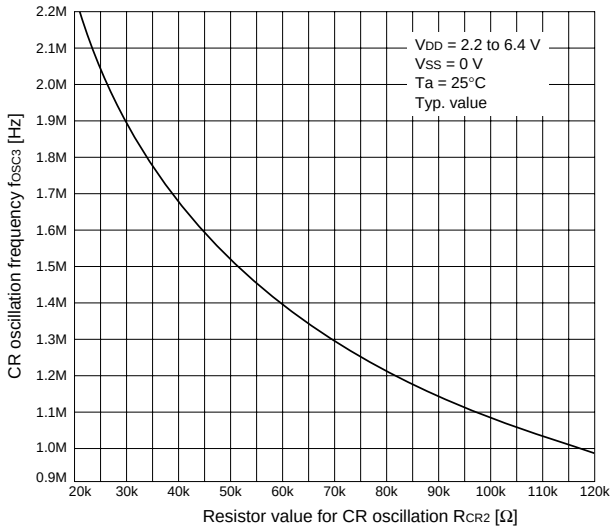
(Unless otherwise specified: V_{DD}=3.0V, V_{SS}=0V, R_{CR2}=34kΩ, Ta=-20 to 70°C)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation frequency dispersion	f_{OSC3}		-25	1,800kHz	25	%
Oscillation start voltage	Vsta	(V_{DD})	2.2			V
Oscillation start time	tsta	V_{DD}=2.2 to 6.4V			3	mS
Oscillation stop voltage	Vstp	(V_{DD})	2.2			V

- **OSC1 CR oscillation frequency-resistance characteristic**



- **OSC3 CR oscillation frequency-resistance characteristic**



● Serial Interface AC Characteristics

Clock Synchronous Master Mode

• During 32 kHz operation

(Condition: V_{DD}=3.0V, V_{SS}=0V, Ta=25°C, V_{IH1}=0.8V_{DD}, V_{IL1}=0.2V_{DD}, V_{OH}=0.8V_{DD}, V_{OL}=0.2V_{DD})

Characteristic	Symbol	Min.	Typ.	Max.	Unit
Transmitting data output delay time	tsmd			5	µS
Receiving data input set-up time	tsms	10			µS
Receiving data input hold time	tsmh	5			µS

• During 1 MHz operation

(Condition: V_{DD}=3.0V, V_{SS}=0V, Ta=25°C, V_{IH1}=0.8V_{DD}, V_{IL1}=0.2V_{DD}, V_{OH}=0.8V_{DD}, V_{OL}=0.2V_{DD})

Characteristic	Symbol	Min.	Typ.	Max.	Unit
Transmitting data output delay time	tsmd			200	nS
Receiving data input set-up time	tsms	400			nS
Receiving data input hold time	tsmh	200			nS

Note that the maximum clock frequency is limited to 1 MHz.

Clock Synchronous Slave Mode

• During 32 kHz operation

(Condition: V_{DD}=3.0V, V_{SS}=0V, Ta=25°C, V_{IH1}=0.8V_{DD}, V_{IL1}=0.2V_{DD}, V_{OH}=0.8V_{DD}, V_{OL}=0.2V_{DD})

Characteristic	Symbol	Min.	Typ.	Max.	Unit
Transmitting data output delay time	tssd			10	µS
Receiving data input set-up time	tsss	10			µS
Receiving data input hold time	tssh	5			µS

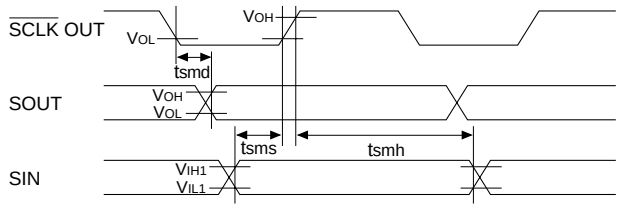
• During 1 MHz operation

(Condition: V_{DD}=3.0V, V_{SS}=0V, Ta=25°C, V_{IH1}=0.8V_{DD}, V_{IL1}=0.2V_{DD}, V_{OH}=0.8V_{DD}, V_{OL}=0.2V_{DD})

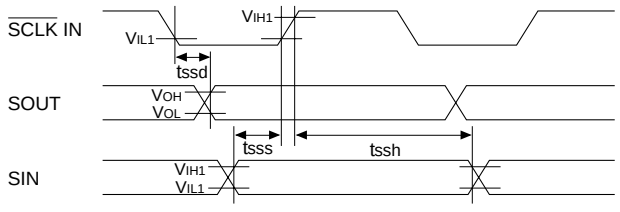
Characteristic	Symbol	Min.	Typ.	Max.	Unit
Transmitting data output delay time	tssd			500	nS
Receiving data input set-up time	tsss	400			nS
Receiving data input hold time	tssh	200			nS

Note that the maximum clock frequency is limited to 1 MHz.

<Master mode>

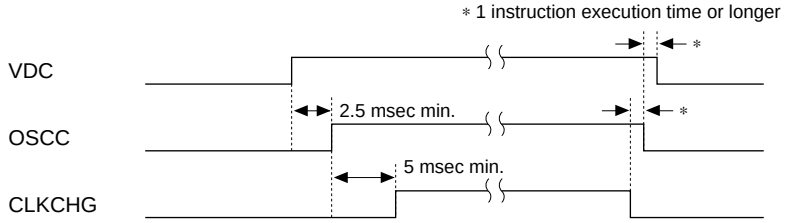


<Slave mode>



● Timing Chart

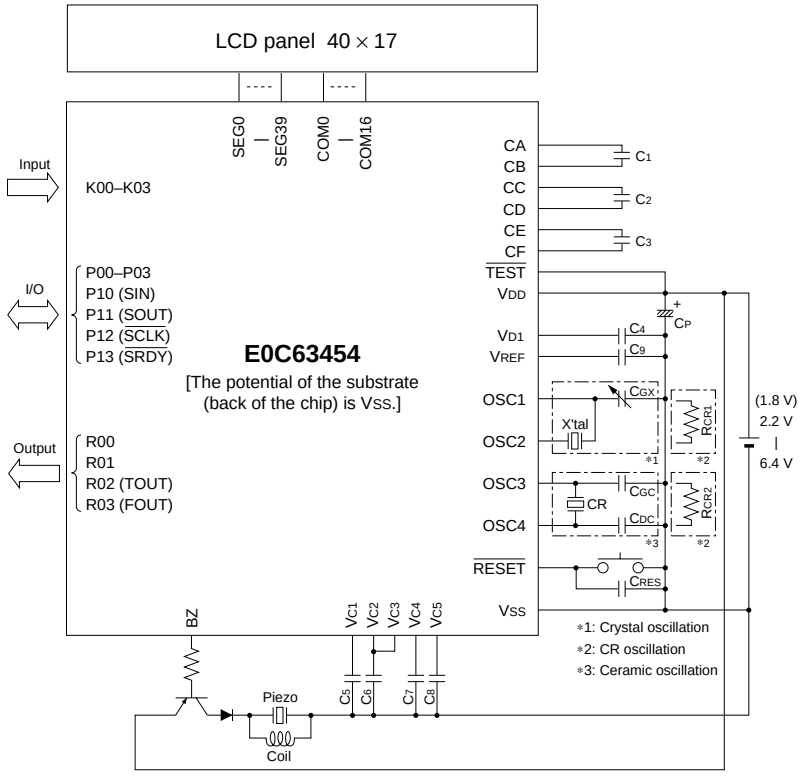
System clock switching



(Note) When the OSC1 oscillation circuit has been selected as the CR oscillation circuit, it is not necessary to set the VDC register.
Whether the VDC register value is "1" or "0" does not matter.

■ BASIC EXTERNAL CONNECTION DIAGRAM

When negative polarity is selected for buzzer output (mask option selection)



X'tal	Crystal oscillator	32.768 kHz, C_I (Max.) = 34 kΩ
C_{GX}	Trimmer capacitor	5–25 pF
R_{CR1}	Resistor for OSC1 CR oscillation	520 kΩ (60 kHz)
CR	Ceramic oscillator	4 MHz (3.0 V)
C_{GC}	Gate capacitor	30 pF
C_{DC}	Drain capacitor	30 pF
R_{CR2}	Resistor for OSC3 CR oscillation	34 kΩ (1.8 MHz)
C_1–C_8	Capacitor	0.2 µF
C_9	Capacitor	0.1 µF
C_P	Capacitor	3.3 µF
C_{RES}	$\overline{\text{RESET}}$ terminal capacitor	0.1 µF

Note: The above table is simply an example, and is not guaranteed to work.

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