

4-bit Single Chip Microcomputer



■ DESCRIPTION

The E0C63458 is a microcomputer which has a high-performance 4-bit CPU E0C63000 as the core CPU, ROM (8,192 words × 13 bits), RAM (5,120 words × 4 bits), serial interface, watchdog timer, programmable timer, time base counters (2 systems), SVD circuit, a dot-matrix LCD driver that can drive a maximum 60 segments × 17 commons and sound generator built-in. The E0C63458 features high speed operation and low current consumption in a wide operating voltage range (2.2V to 6.4V), this makes it suitable for applications working with batteries. It is also suitable for caller ID and portable data bank systems because it has a large capacity of RAM built-in.

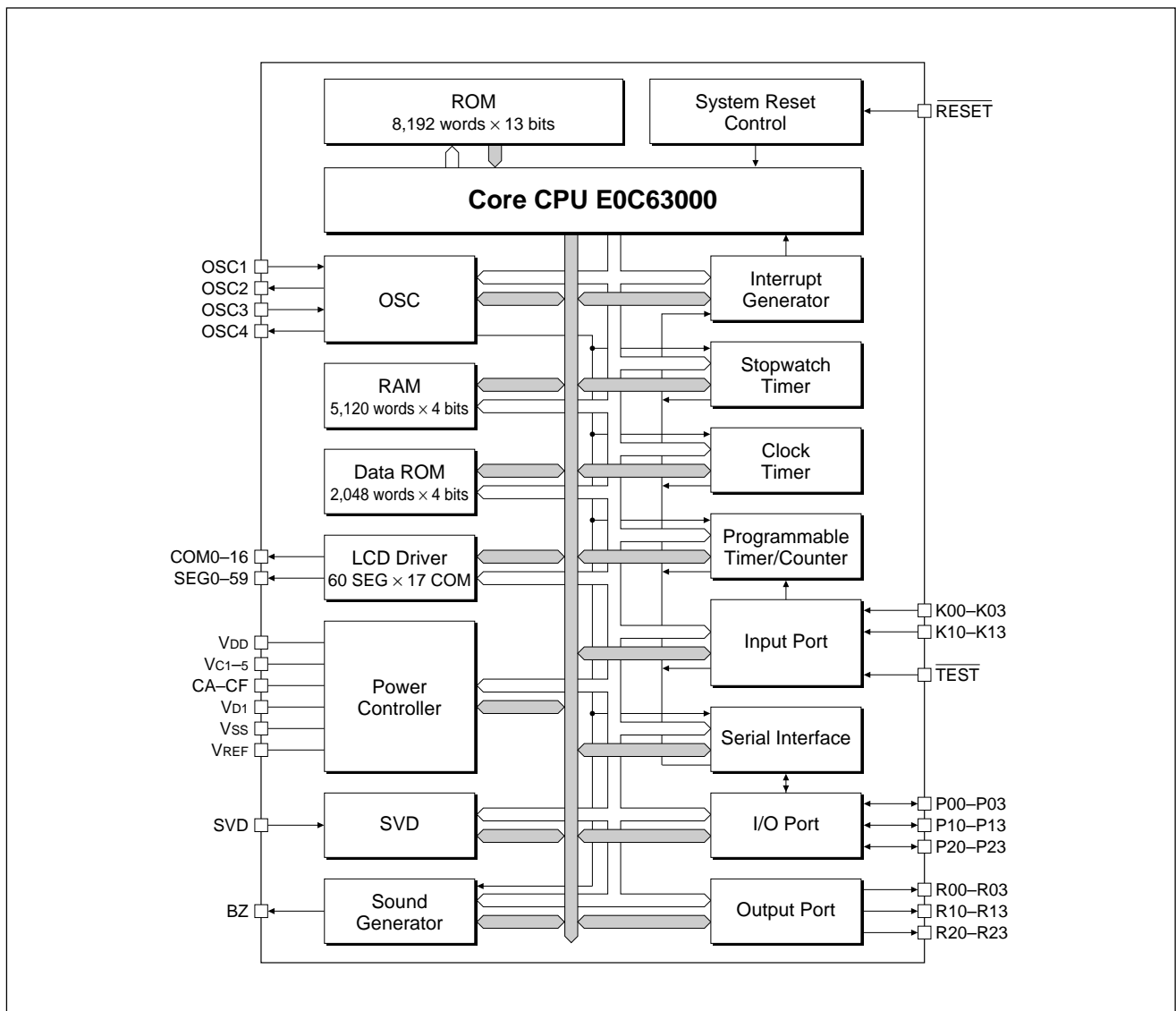
■ FEATURES

- CMOS LSI 4-bit parallel processing
- OSC1 oscillation circuit 32.768kHz (Typ.) crystal or 60kHz (Typ.) CR oscillation circuit (*1)
- OSC3 oscillation circuit 1.8MHz (Typ.) CR or 4MHz (Max.) ceramic oscillation circuit (*1)
- Instruction set Basic instruction : 46 types (411 instructions with all)
Addressing mode : 8 types
- Instruction execution time During operation at 32.768kHz : 61μsec 122μsec 183μsec
During operation at 60kHz : 33μsec 67μsec 100μsec
During operation at 4MHz : 0.5μsec 1μsec 1.5μsec
- ROM capacity Code ROM : 8,192 words × 13 bits
Data ROM : 2,048 words × 4 bits (= 8K bits)
- RAM capacity Data memory : 5,120 words × 4 bits
Display memory : 1,020 bits (240 words × 4 bits + 60 × 1 bit)
- Input port 8 bits (Pull-up resistors may be supplemented *1)
- Output port 12 bits (It is possible to switch the 2 bits to special output *2)
- I/O port 12 bits (It is possible to switch the 2 bits to special output and
the 4 bits to serial I/F input/output *2)
- Serial interface 1 port (8-bit clock synchronous system)
- LCD driver 60 segments × 8, 16 or 17 commons (*2)
- Time base counter 2 systems (Clock timer, stopwatch timer)
- Programmable timer Built-in, 2 inputs × 8 bits, with event counter function
- Watchdog timer Built-in
- Sound generator With envelope and 1-shot output functions
- Supply voltage detection (SVD) circuit .. 16 values, programmable (1.85V to 3.30V)
(It is possible to switch 1 value to the external voltage detection *1)
- External interrupt Input port interrupt : 2 systems
- Internal interrupt Clock timer interrupt : 4 systems
Stopwatch timer interrupt : 2 systems
Programmable timer interrupt : 2 systems
Serial interface interrupt : 1 system

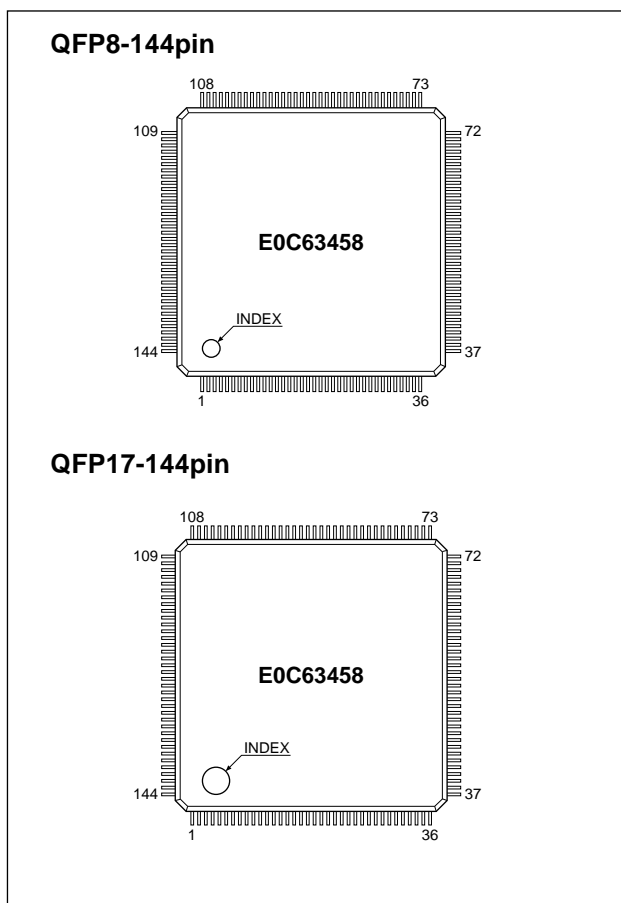
E0C63458

- Power supply voltage 2.2V to 6.4V
(Min. 1.8V when the OSC3 oscillation circuit is not used)
- Operating temperature range -20°C to 70°C
- Current consumption (Typ.) Single clock (OSC1: Crystal oscillation) :
 - During HALT (32kHz)
 - 3.0V (LCD power OFF) 1μA
 - 3.0V (LCD power ON, Vc1 standard) 6μA
 - 3.0V (LCD power ON, Vc2 standard) 4μA
 - During operation (32kHz)
 - 3.0V (LCD power ON, Vc1 standard) 10μA
 - Twin clock :
 - During operation (4MHz)
 - 3.0V (LCD power ON, Vc1 standard) 1,000μA
- Package QFP8-144pin, QFP17-144pin, QFP5-128pin (plastic) or chip
 - *1: Can be selected with mask option *2: Can be selected with software

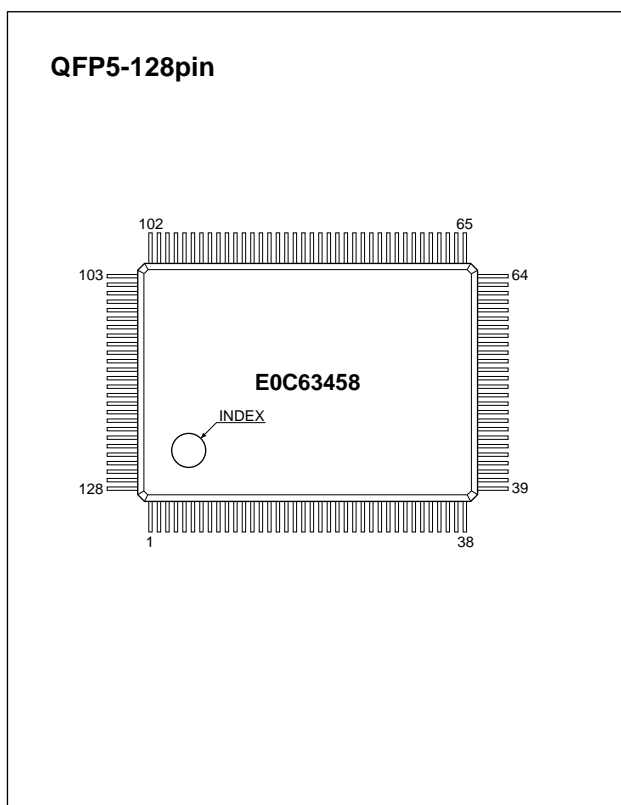
■ BLOCK DIAGRAM



■ PIN CONFIGURATION



| No. | Name | No. | Name | No. | Name | No. | Name |
|-----|-------|-----|------|-----|-------|-----|-------|
| 1 | SEG13 | 37 | N.C. | 73 | N.C. | 109 | N.C. |
| 2 | SEG12 | 38 | N.C. | 74 | SVD | 110 | SEG47 |
| 3 | SEG11 | 39 | R23 | 75 | Vc1 | 111 | SEG46 |
| 4 | SEG10 | 40 | R22 | 76 | Vc2 | 112 | SEG45 |
| 5 | SEG9 | 41 | R21 | 77 | Vc3 | 113 | SEG44 |
| 6 | SEG8 | 42 | R20 | 78 | Vc4 | 114 | SEG43 |
| 7 | SEG7 | 43 | R13 | 79 | Vc5 | 115 | SEG42 |
| 8 | SEG6 | 44 | R12 | 80 | CF | 116 | SEG41 |
| 9 | SEG5 | 45 | R11 | 81 | CE | 117 | SEG40 |
| 10 | SEG4 | 46 | R10 | 82 | CD | 118 | SEG39 |
| 11 | SEG3 | 47 | R03 | 83 | CC | 119 | SEG38 |
| 12 | SEG2 | 48 | R02 | 84 | CB | 120 | SEG37 |
| 13 | SEG1 | 49 | R01 | 85 | CA | 121 | SEG36 |
| 14 | SEG0 | 50 | R00 | 86 | COM8 | 122 | SEG35 |
| 15 | COM7 | 51 | P23 | 87 | COM9 | 123 | SEG34 |
| 16 | COM6 | 52 | P22 | 88 | COM10 | 124 | SEG33 |
| 17 | COM5 | 53 | P21 | 89 | COM11 | 125 | SEG32 |
| 18 | COM4 | 54 | P20 | 90 | COM12 | 126 | SEG31 |
| 19 | N.C. | 55 | P13 | 91 | COM13 | 127 | SEG30 |
| 20 | COM3 | 56 | P12 | 92 | COM14 | 128 | SEG29 |
| 21 | COM2 | 57 | P11 | 93 | COM15 | 129 | SEG28 |
| 22 | COM1 | 58 | P10 | 94 | COM16 | 130 | SEG27 |
| 23 | COM0 | 59 | P03 | 95 | SEG59 | 131 | SEG26 |
| 24 | BZ | 60 | P02 | 96 | SEG58 | 132 | SEG25 |
| 25 | Vss | 61 | P01 | 97 | SEG57 | 133 | SEG24 |
| 26 | OSC1 | 62 | P00 | 98 | SEG56 | 134 | SEG23 |
| 27 | OSC2 | 63 | K13 | 99 | SEG55 | 135 | SEG22 |
| 28 | Vd1 | 64 | K12 | 100 | SEG54 | 136 | SEG21 |
| 29 | OSC3 | 65 | K11 | 101 | SEG53 | 137 | SEG20 |
| 30 | OSC4 | 66 | K10 | 102 | SEG52 | 138 | SEG19 |
| 31 | VDD | 67 | K03 | 103 | SEG51 | 139 | SEG18 |
| 32 | RESET | 68 | K02 | 104 | SEG50 | 140 | SEG17 |
| 33 | TEST | 69 | K01 | 105 | SEG49 | 141 | SEG16 |
| 34 | VREF | 70 | K00 | 106 | SEG48 | 142 | SEG15 |
| 35 | N.C. | 71 | N.C. | 107 | N.C. | 143 | SEG14 |
| 36 | N.C. | 72 | N.C. | 108 | N.C. | 144 | N.C. |



| No. | Name | No. | Name | No. | Name | No. | Name |
|-----|-------|-----|-------|-----|-------|-----|-------|
| 1 | SEG49 | 33 | SEG17 | 65 | RESET | 97 | K02 |
| 2 | SEG48 | 34 | SEG16 | 66 | TEST | 98 | K01 |
| 3 | SEG47 | 35 | SEG15 | 67 | VREF | 99 | K00 |
| 4 | SEG46 | 36 | SEG14 | 68 | N.C. | 100 | SVD |
| 5 | SEG45 | 37 | SEG13 | 69 | R23 | 101 | Vc1 |
| 6 | SEG44 | 38 | SEG12 | 70 | R22 | 102 | Vc2 |
| 7 | SEG43 | 39 | SEG11 | 71 | R21 | 103 | Vc3 |
| 8 | SEG42 | 40 | SEG10 | 72 | R20 | 104 | Vc4 |
| 9 | SEG41 | 41 | SEG9 | 73 | R13 | 105 | Vc5 |
| 10 | SEG40 | 42 | SEG8 | 74 | R12 | 106 | CF |
| 11 | SEG39 | 43 | SEG7 | 75 | R11 | 107 | CE |
| 12 | SEG38 | 44 | SEG6 | 76 | R10 | 108 | CD |
| 13 | SEG37 | 45 | SEG5 | 77 | R03 | 109 | CC |
| 14 | SEG36 | 46 | SEG4 | 78 | R02 | 110 | CB |
| 15 | SEG35 | 47 | SEG3 | 79 | R01 | 111 | CA |
| 16 | SEG34 | 48 | SEG2 | 80 | R00 | 112 | COM8 |
| 17 | SEG33 | 49 | SEG1 | 81 | P23 | 113 | COM9 |
| 18 | SEG32 | 50 | SEG0 | 82 | P22 | 114 | COM10 |
| 19 | SEG31 | 51 | COM7 | 83 | P21 | 115 | COM11 |
| 20 | SEG30 | 52 | COM6 | 84 | P20 | 116 | COM12 |
| 21 | SEG29 | 53 | COM5 | 85 | P13 | 117 | COM13 |
| 22 | SEG28 | 54 | COM4 | 86 | P12 | 118 | COM14 |
| 23 | SEG27 | 55 | COM3 | 87 | P11 | 119 | SEG59 |
| 24 | SEG26 | 56 | COM2 | 88 | P10 | 120 | SEG58 |
| 25 | SEG25 | 57 | BZ | 89 | P03 | 121 | SEG57 |
| 26 | SEG24 | 58 | Vss | 90 | P02 | 122 | SEG56 |
| 27 | SEG23 | 59 | OSC1 | 91 | P01 | 123 | SEG55 |
| 28 | SEG22 | 60 | OSC2 | 92 | P00 | 124 | SEG54 |
| 29 | SEG21 | 61 | Vd1 | 93 | K13 | 125 | SEG53 |
| 30 | SEG20 | 62 | OSC3 | 94 | K11 | 126 | SEG52 |
| 31 | SEG19 | 63 | OSC4 | 95 | K10 | 127 | SEG51 |
| 32 | SEG18 | 64 | VDD | 96 | K03 | 128 | SEG50 |

N.C. : No Connection

■ PIN DESCRIPTION

| Pin name | Pin No. | | In/Out | Function |
|----------------------------------|-----------------------|----------------|--------|---|
| | QFP8-144, QFP17-144 | QFP5-128 | | |
| V _{DD} | 31 | 64 | – | Power (+) supply pin |
| V _{SS} | 25 | 58 | – | Power (–) supply pin |
| V _{D1} | 28 | 61 | – | Oscillation/internal logic system regulated voltage output pin |
| V _{C1} –V _{C5} | 75–79 | 101–105 | – | LCD system power supply pin 1/4 bias generated internally, 1/5 bias supplied externally (selected by mask option) |
| V _{REF} | 34 | 67 | O | LCD system power supply testing pin |
| CA–CF | 85–80 | 111–106 | – | LCD system boosting/reducing capacitor connecting pin |
| OSC1 | 26 | 59 | I | Crystal or CR oscillation input pin (selected by mask option) |
| OSC2 | 27 | 60 | O | Crystal or CR oscillation output pin (selected by mask option) |
| OSC3 | 29 | 62 | I | Ceramic or CR oscillation input pin (selected by mask option) |
| OSC4 | 30 | 63 | O | Ceramic or CR oscillation output pin (selected by mask option) |
| K00–K03 | 70–67 | 99–96 | I | Input port |
| K10, K11 | 66, 65 | 95, 94 | I | Input port |
| K12 | 64 | – | I | Input port |
| K13 | 63 | 93 | I | Input port |
| P00–P03 | 62–59 | 92–89 | I/O | I/O port |
| P10–P13 | 58–55 | 88–85 | I/O | I/O port (switching to serial I/F input/output is possible by software) |
| P20 | 54 | 84 | I/O | I/O port |
| P21 | 53 | 83 | I/O | I/O port |
| P22 | 52 | 82 | I/O | I/O port (switching to CL signal output is possible by software) |
| P23 | 51 | 81 | I/O | I/O port (switching to FR signal output is possible by software) |
| R00 | 50 | 80 | O | Output port |
| R01 | 49 | 79 | O | Output port |
| R02 | 48 | 78 | O | Output port (switching to TOUT signal output is possible by software) |
| R03 | 47 | 77 | O | Output port (switching to FOUT signal output is possible by software) |
| R10–R13 | 46–43 | 76–73 | O | Output port |
| R20–R23 | 42–39 | 72–69 | O | Output port |
| COM0, COM1 | 23, 22 | – | O | LCD common output pin (1/8, 1/16, 1/17 duty can be selected by software) |
| COM2–COM14 | 21, 20, 18–15, 86–92 | 56–51, 112–118 | | |
| COM15, COM16 | 93, 94 | – | | |
| SEG0–SEG59 | 14–1, 143–110, 106–95 | 50–1, 128–119 | O | LCD segment output pin |
| BZ | 24 | 57 | O | Sound output pin |
| SVD | 74 | 100 | I | SVD external voltage input pin |
| RESET | 32 | 65 | I | Initial reset input pin |
| TEST | 33 | 66 | I | Testing input pin |

■ ELECTRICAL CHARACTERISTICS

● Absolute Maximum Ratings

(V_{SS}=0V)

| Rating | Symbol | Value | Unit |
|-------------------------------------|-------------------|-------------------------------|------|
| Supply voltage | V _{DD} | -0.5 to 7.0 | V |
| Input voltage (1) | V _I | -0.5 to V _{DD} + 0.3 | V |
| Input voltage (2) | V _{IOSC} | -0.5 to V _{D1} + 0.3 | V |
| Permissible total output current *1 | ΣI _{VDD} | 10 | mA |
| Operating temperature | T _{opr} | -20 to 70 | °C |
| Storage temperature | T _{stg} | -65 to 150 | °C |
| Soldering temperature / time | T _{sol} | 260°C, 10sec (lead section) | – |
| Permissible dissipation *2 | P _D | 250 | mW |

*1: The permissible total output current is the sum total of the current (average current) that simultaneously flows from the output pins (or is draw in).

*2: In case of plastic package (QFP8-144pin, QFP17-144pin, QFP5-128pin).

● Recommended Operating Conditions

(Ta=-20 to 70°C)

| Condition | Symbol | Remark | Min. | Typ. | Max. | Unit | |
|----------------------------|--------|---------------------|----------------------|--------|-------|------|---|
| Supply voltage | VDD | VSS=0V | OSC3 oscillation OFF | 1.8 | 3.0 | 6.4 | V |
| | | | OSC1 CR oscillation | 2.2 | 3.0 | 6.4 | V |
| | | | OSC3 oscillation ON | 2.2 | 3.0 | 6.4 | V |
| Oscillation frequency | fosc1 | Crystal oscillation | — | 32.768 | — | kHz | |
| | | CR oscillation | 40 | 60 | 80 | kHz | |
| | fosc3 | CR oscillation | | 1,800 | | kHz | |
| | | Ceramic oscillation | | | 4,100 | kHz | |
| SVD terminal input voltage | SVD | VSS=0V, SVD≤VDD | 0 | | 6.4 | V | |

● DC Characteristics

(Unless otherwise specified: VDD=3.0V, VSS=0V, fosc1=32.768kHz, Ta=25°C, VD1/VC1/VC2/VC4/VC5 are internal voltage, C1-C8=0.2μF)

| Characteristic | Symbol | Condition | Min. | Typ. | Max. | Unit |
|-------------------------------|--------|---|---------|------|---------|------|
| High level input voltage (1) | VIH1 | K00-03, K10-13 P00-03, P10-13, P20-23 | 0.8·VDD | | VDD | V |
| High level input voltage (2) | VIH2 | RESET, TEST | 0.9·VDD | | VDD | V |
| Low level input voltage (1) | VIL1 | K00-03, K10-13 P00-03, P10-13, P20-23 | 0 | | 0.2·VDD | V |
| Low level input voltage (2) | VIL2 | RESET, TEST | 0 | | 0.1·VDD | V |
| High level input current | IiH | VIH=3.0V K00-03, K10-13 P00-03, P10-13, P20-23 RESET, TEST | 0 | | 0.5 | μA |
| Low level input current (1) | IiL1 | VIL1=VSS No Pull-up K00-03, K10-13 P00-03, P10-13, P20-23 RESET, TEST | -0.5 | | 0 | μA |
| Low level input current (2) | IiL2 | VIL2=VSS With Pull-up K00-03, K10-13 P00-03, P10-13, P20-23 RESET, TEST | -16 | -10 | -6 | μA |
| High level output current (1) | IOH1 | VOH1=0.9·VDD R00-03, R10-13, R20-23 P00-03, P10-13, P20-23 | | | -2 | mA |
| High level output current (2) | IOH2 | VOH2=0.9·VDD BZ | | | -2 | mA |
| Low level output current (1) | IOL1 | VOL1=0.1·VDD R00-03, R10-13, R20-23 P00-03, P10-13, P20-23 | 3 | | | mA |
| Low level output current (2) | IOL2 | VOL2=0.1·VDD BZ | 3 | | | mA |
| Common output current | IOH3 | VOH3=VC5-0.05V COM0-16 | | | -25 | μA |
| | IOL3 | VOL3=VSS+0.05V | 25 | | | μA |
| Segment output current | IOH4 | VOH4=VC5-0.05V SEG0-59 | | | -10 | μA |
| | IOL4 | VOL4=VSS+0.05V | 10 | | | μA |

(Unless otherwise specified: VDD=5.0V, VSS=0V, fosc1=32.768kHz, Ta=25°C, VD1/VC1/VC2/VC4/VC5 are internal voltage, C1-C8=0.2μF)

| Characteristic | Symbol | Condition | Min. | Typ. | Max. | Unit |
|-------------------------------|--------|---|---------|------|---------|------|
| High level input voltage (1) | VIH1 | K00-03, K10-13 P00-03, P10-13, P20-23 | 0.8·VDD | | VDD | V |
| High level input voltage (2) | VIH2 | RESET, TEST | 0.9·VDD | | VDD | V |
| Low level input voltage (1) | VIL1 | K00-03, K10-13 P00-03, P10-13, P20-23 | 0 | | 0.2·VDD | V |
| Low level input voltage (2) | VIL2 | RESET, TEST | 0 | | 0.1·VDD | V |
| High level input current | IiH | VIH=5.0V K00-03, K10-13 P00-03, P10-13, P20-23 RESET, TEST | 0 | | 0.5 | μA |
| Low level input current (1) | IiL1 | VIL1=VSS No Pull-up K00-03, K10-13 P00-03, P10-13, P20-23 RESET, TEST | -0.5 | | 0 | μA |
| Low level input current (2) | IiL2 | VIL2=VSS With Pull-up K00-03, K10-13 P00-03, P10-13, P20-23 RESET, TEST | -25 | -15 | -10 | μA |
| High level output current (1) | IOH1 | VOH1=0.9·VDD R00-03, R10-13, R20-23 P00-03, P10-13, P20-23 | | | -5 | mA |
| High level output current (2) | IOH2 | VOH2=0.9·VDD BZ | | | -5 | mA |
| Low level output current (1) | IOL1 | VOL1=0.1·VDD R00-03, R10-13, R20-23 P00-03, P10-13, P20-23 | 7.5 | | | mA |
| Low level output current (2) | IOL2 | VOL2=0.1·VDD BZ | 7.5 | | | mA |
| Common output current | IOH3 | VOH3=VC5-0.05V COM0-16 | | | -25 | μA |
| | IOL3 | VOL3=VSS+0.05V | 25 | | | μA |
| Segment output current | IOH4 | VOH4=VC5-0.05V SEG0-59 | | | -10 | μA |
| | IOL4 | VOL4=VSS+0.05V | 10 | | | μA |

E0C63458

● Analog Circuit Characteristics and Current Consumption

(Unless otherwise specified: $V_{DD}=3.0V$, $V_{SS}=0V$, $f_{osc1}=32.768kHz$, $C_G=25pF$, $T_a=25^\circ C$, $V_{D1}/V_{C1}/V_{C2}/V_{C4}/V_{C5}$ are internal voltage, $C_1-C_8=0.2\mu F$)

| Characteristic | Symbol | Condition | Min. | Typ. | Max. | Unit | | | | | | | | |
|---|----------|---|--------------------|-----------------------|---|-----------------------|---|------------|----------|--|-------------------------------------|--|--------------------|---|
| LCD drive voltage (when V_{C1} standard is selected) | V_{C1} | Connect 1 M Ω load resistor between V_{SS} and V_{C1} (without panel load) | LC0-3="0" | Typ. $\times 0.88$ | 0.975 | Typ. $\times 1.12$ | V | | | | | | | |
| | | | LC0-3="1" | | 0.990 | | | | | | | | | |
| | | | LC0-3="2" | | 1.005 | | | | | | | | | |
| | | | LC0-3="3" | | 1.020 | | | | | | | | | |
| | | | LC0-3="4" | | 1.035 | | | | | | | | | |
| | | | LC0-3="5" | | 1.050 | | | | | | | | | |
| | | | LC0-3="6" | | 1.065 | | | | | | | | | |
| | | | LC0-3="7" | | 1.080 | | | | | | | | | |
| | | | LC0-3="8" | | 1.095 | | | | | | | | | |
| | | | LC0-3="9" | | 1.110 | | | | | | | | | |
| | | | LC0-3="10" | | 1.125 | | | | | | | | | |
| | | | LC0-3="11" | | 1.140 | | | | | | | | | |
| | | | LC0-3="12" | | 1.155 | | | | | | | | | |
| | | | LC0-3="13" | | 1.170 | | | | | | | | | |
| | | | LC0-3="14" | | 1.185 | | | | | | | | | |
| | | | | 1.200 | | | | | | | | | | |
| | V_{C2} | Connect 1 M Ω load resistor between V_{SS} and V_{C2} (without panel load) | $2 \cdot V_{C1}$ | | $2 \cdot V_{C1}$ $\times 0.9$ | V | | | | | | | | |
| | V_{C4} | Connect 1 M Ω load resistor between V_{SS} and V_{C4} (without panel load) | $3 \cdot V_{C1}$ | | $3 \cdot V_{C1}$ $\times 0.9$ | V | | | | | | | | |
| | V_{C5} | Connect 1 M Ω load resistor between V_{SS} and V_{C5} (without panel load) | $4 \cdot V_{C1}$ | | $4 \cdot V_{C1}$ $\times 0.9$ | V | | | | | | | | |
| LCD drive voltage (when V_{C2} standard is selected) | V_{C1} | Connect 1 M Ω load resistor between V_{SS} and V_{C1} (without panel load) | $1/2 \cdot V_{C2}$ | Typ. $\times 0.88$ | $1/2 \cdot V_{C2}$ -0.1 | Typ. $\times 1.12$ | V | | | | | | | |
| | | | V_{C2} | | Connect 1 M Ω load resistor between V_{SS} and V_{C2} (without panel load) | | | LC0-3="0" | 1.95 | | | | | |
| | | | | | | | | LC0-3="1" | 1.98 | | | | | |
| | | | | | | | | LC0-3="2" | 2.01 | | | | | |
| | | | | | | | | LC0-3="3" | 2.04 | | | | | |
| | | | | | | | | LC0-3="4" | 2.07 | | | | | |
| | | | | | | | | LC0-3="5" | 2.10 | | | | | |
| | | | | | | | | LC0-3="6" | 2.13 | | | | | |
| | | | | | | | | LC0-3="7" | 2.16 | | | | | |
| | | | | | | | | LC0-3="8" | 2.19 | | | | | |
| | | | | | | | | LC0-3="9" | 2.22 | | | | | |
| | | | | | | | | LC0-3="10" | 2.25 | | | | | |
| | | | | | | | | LC0-3="11" | 2.28 | | | | | |
| | | | | | | | | LC0-3="12" | 2.31 | | | | | |
| | | | | | | | | LC0-3="13" | 2.34 | | | | | |
| | | | | | | | | LC0-3="14" | 2.37 | | | | | |
| | | | | | | | | LC0-3="15" | 2.40 | | | | | |
| | | | | | | | | | V_{C4} | Connect 1 M Ω load resistor between V_{SS} and V_{C4} (without panel load) | $3/2 \cdot V_{C2}$ $\times 0.95$ | | $3/2 \cdot V_{C2}$ | V |
| | | | | | | | | | V_{C5} | Connect 1 M Ω load resistor between V_{SS} and V_{C5} (without panel load) | $2 \cdot V_{C2}$ $\times 0.95$ | | $2 \cdot V_{C2}$ | V |

(Unless otherwise specified: $V_{DD}=3.0V$, $V_{SS}=0V$, $f_{OSC1}=32.768kHz$, $C_G=25pF$, $R_{CR1}=600k\Omega$, $R_{CR2}=47k\Omega$, $T_a=25^\circ C$,
 $V_{D1}/V_{C1}/V_{C2}/V_{C4}/V_{C5}$ are internal voltage, $C_1-C_8=0.2\mu F$)

| Characteristic | Symbol | Condition | Min. | Typ. | Max. | Unit | |
|---------------------------|------------|---|-----------------------|-------|-----------------------|---------|---------|
| SVD voltage | V_{SVD1} | SVDS0-3="0" (internal) | Typ. $\times 0.93$ | 1.85 | Typ. $\times 1.07$ | V | |
| | | SVDS0-3="1" | | 1.90 | | | |
| | | SVDS0-3="2" | | 2.00 | | | |
| | | SVDS0-3="3" | | 2.10 | | | |
| | | SVDS0-3="4" | | 2.20 | | | |
| | | SVDS0-3="5" | | 2.30 | | | |
| | | SVDS0-3="6" | | 2.40 | | | |
| | | SVDS0-3="7" | | 2.50 | | | |
| | | SVDS0-3="8" | | 2.60 | | | |
| | | SVDS0-3="9" | | 2.70 | | | |
| | | SVDS0-3="10" | | 2.80 | | | |
| | | SVDS0-3="11" | | 2.90 | | | |
| | | SVDS0-3="12" | | 3.00 | | | |
| | | SVDS0-3="13" | | 3.10 | | | |
| | | SVDS0-3="14" | | 3.20 | | | |
| SVDS0-3="15" | 3.30 | | | | | | |
| SVD voltage (external) *4 | V_{SVD2} | SVDS0-3="0" (external) | 0.95 | 1.05 | 1.15 | V | |
| SVD circuit response time | t_{SVD} | | | | 100 | μS | |
| Current consumption | I_{OP} | During HALT (32 kHz crystal oscillation), LCD power OFF | *1, *2, *3 | 1 | 2 | μA | |
| | | During HALT (32 kHz crystal oscillation), LCD power ON (V_{C1} standard) | *1, *2, *3 | 6 | 12 | μA | |
| | | During HALT (32 kHz crystal oscillation), LCD power ON (V_{C2} standard) | *1, *2, *3 | 4 | 8 | μA | |
| | | During HALT (60 kHz CR oscillation), LCD power OFF | *1, *3 | 23 | 45 | μA | |
| | | During HALT (60 kHz CR oscillation), LCD power ON (V_{C1} standard) | *1, *3 | 30 | 60 | μA | |
| | | During HALT (60 kHz CR oscillation), LCD power ON (V_{C2} standard) | *1, *3 | 26 | 50 | μA | |
| | | During execution (32 kHz crystal oscillation), LCD power ON (V_{C1} standard) | *1, *2, *3 | 10 | 19 | μA | |
| | | During execution (60 kHz CR oscillation), LCD power ON (V_{C1} standard) | *1, *3 | 45 | 80 | μA | |
| | | During execution (2 MHz ceramic oscillation), LCD power ON (V_{C1} standard) | *1 | 500 | 700 | μA | |
| | | During execution (4 MHz ceramic oscillation), LCD power ON (V_{C1} standard) | *1 | 1,000 | 1,200 | μA | |
| | | During execution (1,800 kHz CR oscillation), LCD power ON (V_{C1} standard) | *1 | 700 | 1,000 | μA | |
| | | SVD circuit current (during supply voltage detection) $V_{DD}=1.85$ to 6.4 V | | 1 | | 7 | μA |
| | | SVD circuit current (during external voltage detection) $V_{DD}=1.85$ to 6.4 V | | 0.5 | | 3 | μA |

*1: Without panel load. The SVD circuit is OFF.

*2: $V_{DC} = "0"$

*3: $OSCC = "0"$

*4: Please input the voltage, which is within the range between V_{SS} and V_{DD} , into the SVD terminal.

● Oscillation Characteristics

The oscillation characteristics change depending on the conditions (components used, board pattern, etc.). Use the following characteristics as reference values.

OSC1 Crystal Oscillation Circuit

(Unless otherwise specified: $V_{DD}=3.0V$, $V_{SS}=0V$, $f_{osc1}=32.768kHz$, $C_G=25pF$, $C_D=$ built-in, $T_a=-20$ to $70^\circ C$)

| Characteristic | Symbol | Condition | Min. | Typ. | Max. | Unit |
|------------------------------------|---------------------------|---|------|------|------|-----------|
| Oscillation start voltage | V_{sta} | $t_{sta} \leq 3sec (V_{DD})$ | 1.8 | | | V |
| Oscillation stop voltage | V_{stp} | $t_{stp} \leq 10sec (V_{DD})$ | 1.8 | | | V |
| Built-in capacitance (drain) | C_D | Including the parasitic capacitance inside the IC (in chip) | | 14 | | pF |
| Frequency/voltage deviation | $\partial f/\partial V$ | $V_{DD}=2.2$ to $6.4V$ | | | 5 | ppm |
| | | with VDC switching | | | 10 | ppm |
| Frequency/IC deviation | $\partial f/\partial IC$ | | -10 | | 10 | ppm |
| Frequency adjustment range | $\partial f/\partial C_G$ | $C_G=5$ to $25pF$ | 10 | 20 | | ppm |
| Harmonic oscillation start voltage | V_{hho} | $C_G=5pF (V_{DD})$ | 6.4 | | | V |
| Permitted leak resistance | R_{leak} | Between OSC1 and V_{SS} | 200 | | | $M\Omega$ |

OSC1 CR Oscillation Circuit

(Unless otherwise specified: $V_{DD}=3.0V$, $V_{SS}=0V$, $R_{CR1}=600k\Omega$, $T_a=-20$ to $70^\circ C$)

| Characteristic | Symbol | Condition | Min. | Typ. | Max. | Unit |
|----------------------------------|------------|------------------------|------|-------|------|------|
| Oscillation frequency dispersion | f_{osc1} | | -30 | 60kHz | 30 | % |
| Oscillation start voltage | V_{sta} | (V_{DD}) | 2.2 | | | V |
| Oscillation start time | t_{sta} | $V_{DD}=2.2$ to $6.4V$ | | | 3 | mS |
| Oscillation stop voltage | V_{stp} | (V_{DD}) | 2.2 | | | V |

OSC3 Ceramic Oscillation Circuit

(Unless otherwise specified: $V_{DD}=3.0V$, $V_{SS}=0V$, Ceramic oscillator: 4MHz, $C_{GC}=C_{DC}=30pF$, $T_a=-20$ to $70^\circ C$)

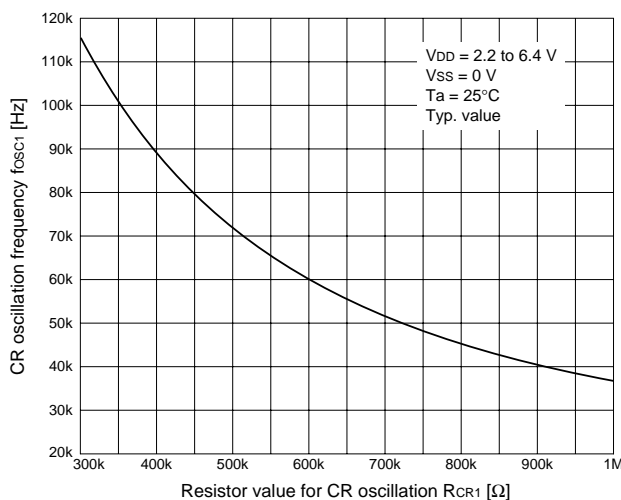
| Characteristic | Symbol | Condition | Min. | Typ. | Max. | Unit |
|---------------------------|-----------|------------------------|------|------|------|------|
| Oscillation start voltage | V_{sta} | (V_{DD}) | 2.2 | | | V |
| Oscillation start time | t_{sta} | $V_{DD}=2.2$ to $6.4V$ | | | 5 | mS |
| Oscillation stop voltage | V_{stp} | (V_{DD}) | 2.2 | | | V |

OSC3 CR Oscillation Circuit

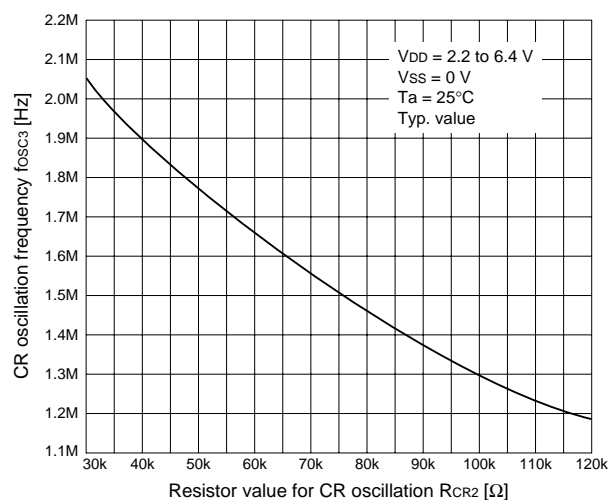
(Unless otherwise specified: $V_{DD}=3.0V$, $V_{SS}=0V$, $R_{CR2}=47k\Omega$, $T_a=-20$ to $70^\circ C$)

| Characteristic | Symbol | Condition | Min. | Typ. | Max. | Unit |
|----------------------------------|------------|------------------------|------|----------|------|------|
| Oscillation frequency dispersion | f_{osc3} | | -25 | 1,800kHz | 25 | % |
| Oscillation start voltage | V_{sta} | (V_{DD}) | 2.2 | | | V |
| Oscillation start time | t_{sta} | $V_{DD}=2.2$ to $6.4V$ | | | 3 | mS |
| Oscillation stop voltage | V_{stp} | (V_{DD}) | 2.2 | | | V |

• OSC1 CR oscillation frequency-resistance characteristic



• OSC3 CR oscillation frequency-resistance characteristic



● Serial Interface AC Characteristics

Clock Synchronous Master Mode

• During 32 kHz operation

(Condition: $V_{DD}=3.0V$, $V_{SS}=0V$, $T_a=25^\circ C$, $V_{IH1}=0.8V_{DD}$, $V_{IL1}=0.2V_{DD}$, $V_{OH}=0.8V_{DD}$, $V_{OL}=0.2V_{DD}$)

| Characteristic | Symbol | Min. | Typ. | Max. | Unit |
|-------------------------------------|-----------|------|------|------|---------|
| Transmitting data output delay time | t_{smd} | | | 5 | μS |
| Receiving data input set-up time | t_{sms} | 10 | | | μS |
| Receiving data input hold time | t_{smh} | 5 | | | μS |

• During 1 MHz operation

(Condition: $V_{DD}=3.0V$, $V_{SS}=0V$, $T_a=25^\circ C$, $V_{IH1}=0.8V_{DD}$, $V_{IL1}=0.2V_{DD}$, $V_{OH}=0.8V_{DD}$, $V_{OL}=0.2V_{DD}$)

| Characteristic | Symbol | Min. | Typ. | Max. | Unit |
|-------------------------------------|-----------|------|------|------|------|
| Transmitting data output delay time | t_{smd} | | | 200 | nS |
| Receiving data input set-up time | t_{sms} | 400 | | | nS |
| Receiving data input hold time | t_{smh} | 200 | | | nS |

Note that the maximum clock frequency is limited to 1 MHz.

Clock Synchronous Slave Mode

• During 32 kHz operation

(Condition: $V_{DD}=3.0V$, $V_{SS}=0V$, $T_a=25^\circ C$, $V_{IH1}=0.8V_{DD}$, $V_{IL1}=0.2V_{DD}$, $V_{OH}=0.8V_{DD}$, $V_{OL}=0.2V_{DD}$)

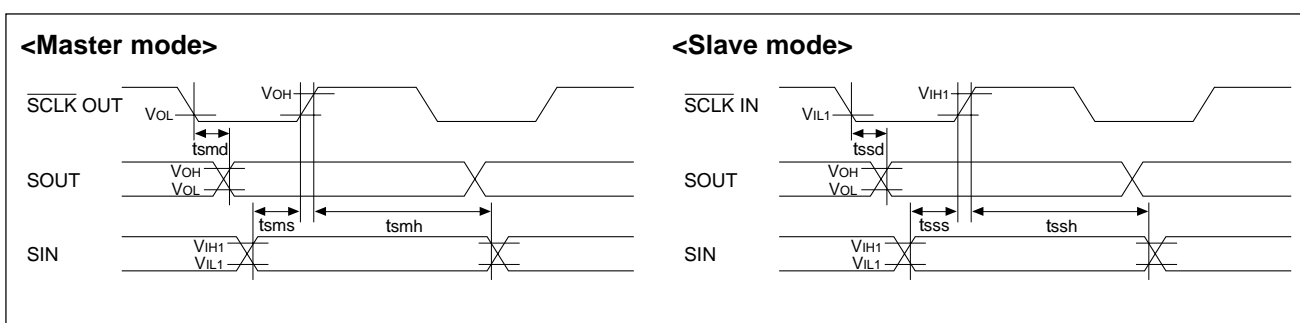
| Characteristic | Symbol | Min. | Typ. | Max. | Unit |
|-------------------------------------|-----------|------|------|------|---------|
| Transmitting data output delay time | t_{ssd} | | | 10 | μS |
| Receiving data input set-up time | t_{sss} | 10 | | | μS |
| Receiving data input hold time | t_{ssh} | 5 | | | μS |

• During 1 MHz operation

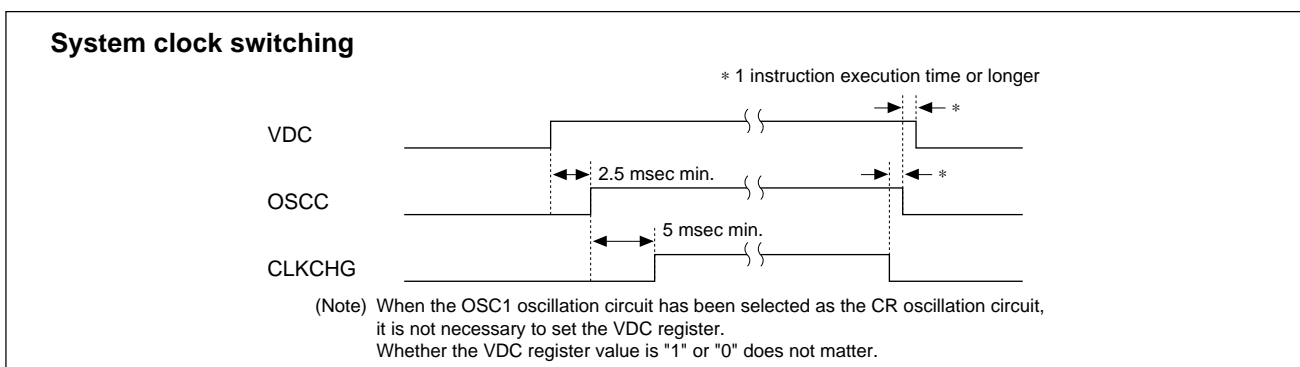
(Condition: $V_{DD}=3.0V$, $V_{SS}=0V$, $T_a=25^\circ C$, $V_{IH1}=0.8V_{DD}$, $V_{IL1}=0.2V_{DD}$, $V_{OH}=0.8V_{DD}$, $V_{OL}=0.2V_{DD}$)

| Characteristic | Symbol | Min. | Typ. | Max. | Unit |
|-------------------------------------|-----------|------|------|------|------|
| Transmitting data output delay time | t_{ssd} | | | 500 | nS |
| Receiving data input set-up time | t_{sss} | 400 | | | nS |
| Receiving data input hold time | t_{ssh} | 200 | | | nS |

Note that the maximum clock frequency is limited to 1 MHz.

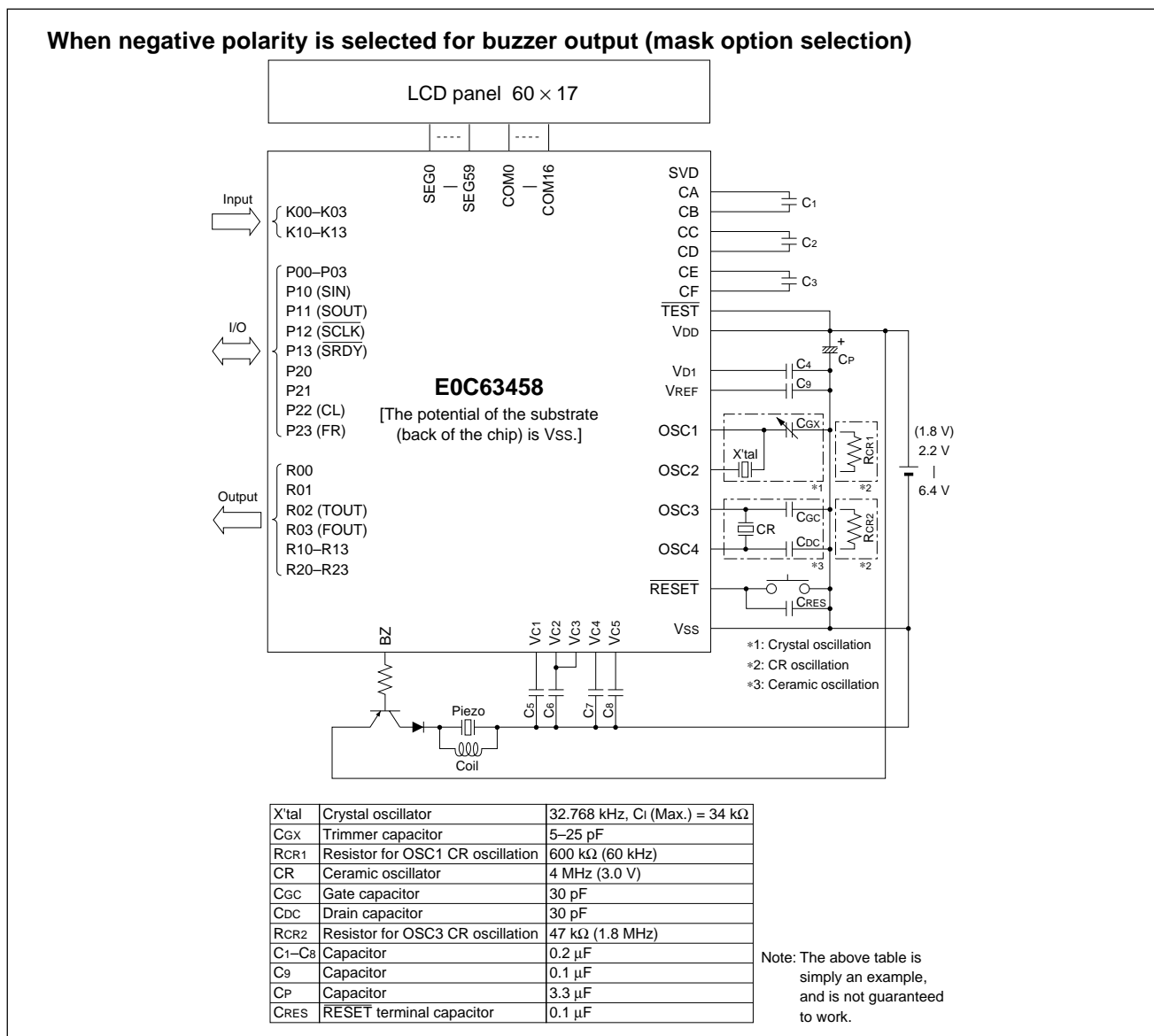


● Timing Chart



E0C63458

■ BASIC EXTERNAL CONNECTION DIAGRAM



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