EPSON

E0C63466

4-bit Single Chip Microcomputer

Low Voltage Operation Products

- 4-bit Core CPU (2–6 clock / inst.)
- Dot-matrix Type LCD Driver
- Low Voltage Operation (1.8V Min.)
- Large Capacity RAM

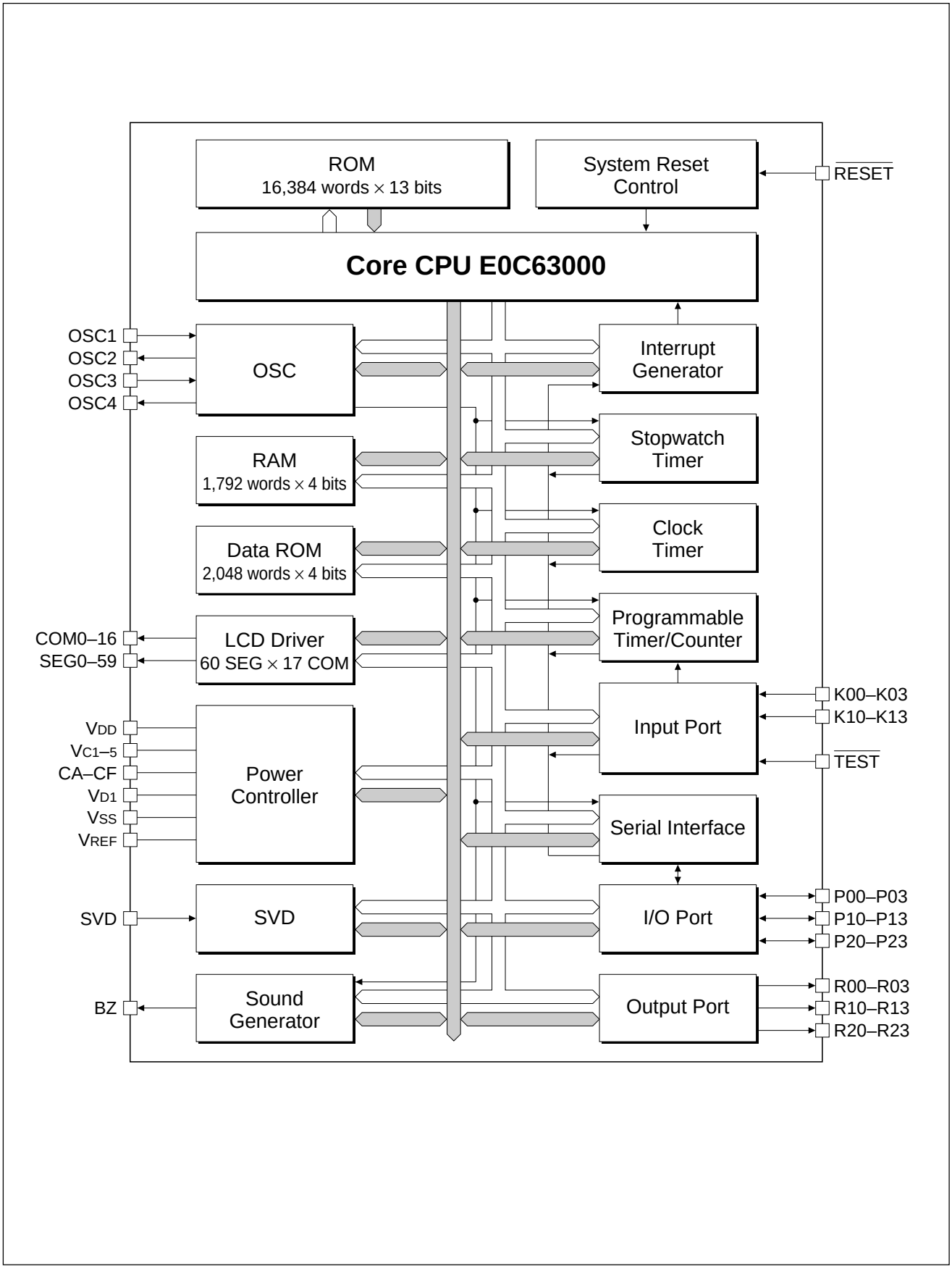
■ DESCRIPTION

The E0C63466 is a CMOS 4-bit microcomputer composed of a CMOS 4-bit core CPU, ROM, RAM, dot-matrix type LCD driver and timer. E0C63466 features high speed operation and low current consumption, this makes it suitable for applications working with batteries. It is also suitable for caller ID and portable data bank systems because it has a large capacity of RAM built-in.

■ FEATURES

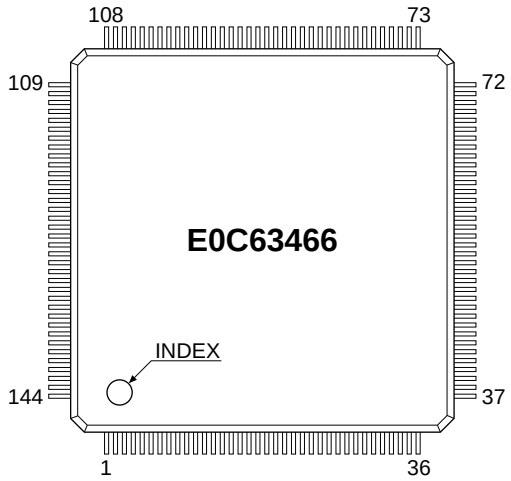
- CMOS LSI 4-bit parallel processing ..... E0C63000 core CPU
- Main clock ..... 32.768kHz (Typ.) Crystal oscillation or 60kHz (Typ.) CR oscillation
- Sub clock ..... 1.8MHz (Typ.) CR oscillation or 4MHz (Max.) Ceramic oscillation
- Instruction set ..... Basic instruction : 46 types (411 instructions with all)
  Addressing mode : 8 types
- Instruction execution time ..... During operation at 32.768kHz : 61µsec, 122µsec, 183µsec
  During operation at 60kHz : 33µsec, 67µsec, 100µsec
  During operation at 4MHz : 0.5µsec, 1µsec, 1.5µsec
- ROM capacity ..... Code ROM : 16,384 words × 13 bits
  Data ROM : 2,048 words × 4 bits
- RAM capacity ..... Data memory : 1,792 words × 4 bits
  Display memory : 1,020 bits (240 words × 4 bits + 60 × 1 bit)
- Input port ..... 8 bits
- Output port ..... 12 bits
- I/O port ..... 12 bits
- LCD driver ..... 60 segments × 8 / 16 / 17 commons
- Clock timer ..... 1 ch.
- Stopwatch timer ..... 1 ch.
- Programmable timer ..... 8 bits × 2 ch.
- Watchdog timer ..... Built-in
- Serial interface ..... 8-bit clock synchronous system
- Sound generator ..... With envelope and 1-shot output functions
- Supply voltage detection (SVD) circuit .... 16 values, programmable (1.85 to 3.30V)
- Interrupts ..... External : Input port interrupt 2 lines
  Internal : Clock timer interrupt 4 lines
  : Stopwatch timer interrupt 2 lines
  : Programmable timer interrupt 2 lines
  : Serial interface interrupt 1 line
- Supply voltage ..... 1.8 to 6.4V (Min. 2.2V when OSC3 and CR oscillation circuit are used)
- Current consumption ..... HALT mode (32.768kHz, LCD off) : 1.0µA
  OPERATING mode (32.768kHz, LCD on) : 10.0µA
- Package ..... QFP8-144pin / QFP17-144pin / QFP5-128pin (plastic), Die form

■ BLOCK DIAGRAM

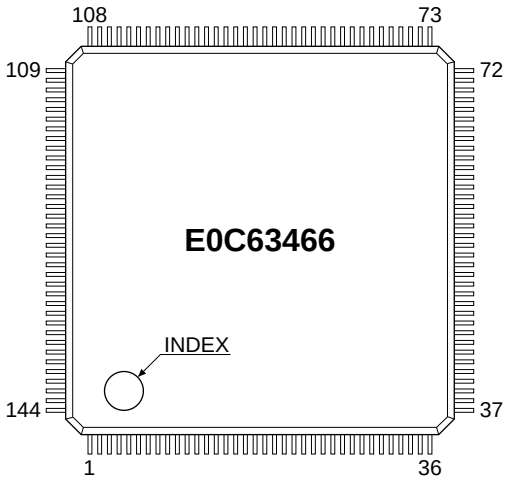


■ PIN CONFIGURATION

QFP8-144pin



QFP17-144pin

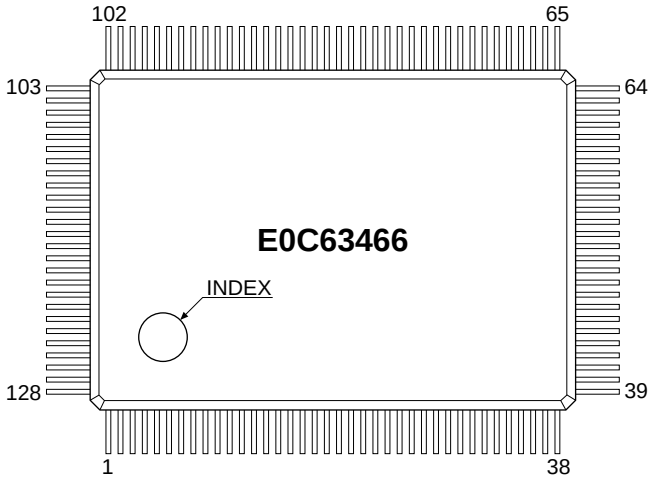


No.	Name	No.	Name	No.	Name	No.	Name
1	SEG13	37	N.C.	73	N.C.	109	N.C.
2	SEG12	38	N.C.	74	SVD	110	SEG47
3	SEG11	39	R23	75	V_{C1}	111	SEG46
4	SEG10	40	R22	76	V_{C2}	112	SEG45
5	SEG9	41	R21	77	V_{C3}	113	SEG44
6	SEG8	42	R20	78	V_{C4}	114	SEG43
7	SEG7	43	R13	79	V_{C5}	115	SEG42
8	SEG6	44	R12	80	CF	116	SEG41
9	SEG5	45	R11	81	CE	117	SEG40
10	SEG4	46	R10	82	CD	118	SEG39
11	SEG3	47	R03	83	CC	119	SEG38
12	SEG2	48	R02	84	CB	120	SEG37
13	SEG1	49	R01	85	CA	121	SEG36
14	SEG0	50	R00	86	COM8	122	SEG35
15	COM7	51	P23	87	COM9	123	SEG34
16	COM6	52	P22	88	COM10	124	SEG33
17	COM5	53	P21	89	COM11	125	SEG32
18	COM4	54	P20	90	COM12	126	SEG31
19	N.C.	55	P13	91	COM13	127	SEG30
20	COM3	56	P12	92	COM14	128	SEG29
21	COM2	57	P11	93	COM15	129	SEG28
22	COM1	58	P10	94	COM16	130	SEG27
23	COM0	59	P03	95	SEG59	131	SEG26
24	BZ	60	P02	96	SEG58	132	SEG25
25	V_{SS}	61	P01	97	SEG57	133	SEG24
26	OSC1	62	P00	98	SEG56	134	SEG23
27	OSC2	63	K13	99	SEG55	135	SEG22
28	V_{D1}	64	K12	100	SEG54	136	SEG21
29	OSC3	65	K11	101	SEG53	137	SEG20
30	OSC4	66	K10	102	SEG52	138	SEG19
31	V_{DD}	67	K03	103	SEG51	139	SEG18
32	$\overline{\text{RESET}}$	68	K02	104	SEG50	140	SEG17
33	$\overline{\text{TEST}}$	69	K01	105	SEG49	141	SEG16
34	V_{REF}	70	K00	106	SEG48	142	SEG15
35	N.C.	71	N.C.	107	N.C.	143	SEG14
36	N.C.	72	N.C.	108	N.C.	144	N.C.

N.C. : No Connection

Note: The pin layout diagram of the both package is same.

QFP5-128pin



No.	Name	No.	Name	No.	Name	No.	Name
1	SEG49	33	SEG17	65	$\overline{\text{RESET}}$	97	K02
2	SEG48	34	SEG16	66	$\overline{\text{TEST}}$	98	K01
3	SEG47	35	SEG15	67	V_{REF}	99	K00
4	SEG46	36	SEG14	68	N.C.	100	SVD
5	SEG45	37	SEG13	69	R23	101	V_{C1}
6	SEG44	38	SEG12	70	R22	102	V_{C2}
7	SEG43	39	SEG11	71	R21	103	V_{C3}
8	SEG42	40	SEG10	72	R20	104	V_{C4}
9	SEG41	41	SEG9	73	R13	105	V_{C5}
10	SEG40	42	SEG8	74	R12	106	CF
11	SEG39	43	SEG7	75	R11	107	CE
12	SEG38	44	SEG6	76	R10	108	CD
13	SEG37	45	SEG5	77	R03	109	CC
14	SEG36	46	SEG4	78	R02	110	CB
15	SEG35	47	SEG3	79	R01	111	CA
16	SEG34	48	SEG2	80	R00	112	COM8
17	SEG33	49	SEG1	81	P23	113	COM9
18	SEG32	50	SEG0	82	P22	114	COM10
19	SEG31	51	COM7	83	P21	115	COM11
20	SEG30	52	COM6	84	P20	116	COM12
21	SEG29	53	COM5	85	P13	117	COM13
22	SEG28	54	COM4	86	P12	118	COM14
23	SEG27	55	COM3	87	P11	119	SEG59
24	SEG26	56	COM2	88	P10	120	SEG58
25	SEG25	57	BZ	89	P03	121	SEG57
26	SEG24	58	V_{SS}	90	P02	122	SEG56
27	SEG23	59	OSC1	91	P01	123	SEG55
28	SEG22	60	OSC2	92	P00	124	SEG54
29	SEG21	61	V_{D1}	93	K13	125	SEG53
30	SEG20	62	OSC3	94	K11	126	SEG52
31	SEG19	63	OSC4	95	K10	127	SEG51
32	SEG18	64	V_{DD}	96	K03	128	SEG50

N.C. : No Connection

Note: This package does not have the K12 terminal. For the K12 mask option, "With pull-up resistor" should be chosen when using this package.

■ PIN DESCRIPTION

Pin name	Pin No.		In/Out	Function
	QFP8-144,QFP17-144	QFP5-128		
V_{DD}	31	64	–	Power (+) supply pin
V_{SS}	25	58	–	Power (–) supply pin
V_{D1}	28	61	–	Oscillation/internal logic system regulated voltage output pin
V_{C1}–V_{C5}	75–79	101–105	–	LCD system power supply pin 1/4 bias generated internally, 1/5 bias supplied externally (selected by mask option)
V_{REF}	34	67	O	LCD system power supply testing pin
CA–CF	85–80	111–106	–	LCD system boosting/reducing capacitor connecting pin
OSC1	26	59	I	Crystal or CR oscillation input pin (selected by mask option)
OSC2	27	60	O	Crystal or CR oscillation output pin (selected by mask option)
OSC3	29	62	I	Ceramic or CR oscillation input pin (selected by mask option)
OSC4	30	63	O	Ceramic or CR oscillation output pin (selected by mask option)
K00–K03	70–67	99–96	I	Input port
K10, K11	66,65	95,94	I	Input port
K12	64	–	I	Input port
K13	63	93	I	Input port
P00–P03	62–59	92–89	I/O	I/O port
P10–P13	58–55	88–85	I/O	I/O port (switching to serial I/F input/output is possible by software)
P20	54	84	I/O	I/O port
P21	53	83	I/O	I/O port
P22	52	82	I/O	I/O port (switching to CL signal output is possible by software)
P23	51	81	I/O	I/O port (switching to FR signal output is possible by software)
R00	50	80	O	Output port
R01	49	79	O	Output port
R02	48	78	O	Output port (switching to TOUT signal output is possible by software)
R03	47	77	O	Output port (switching to FOUT signal output is possible by software)
R10–R13	46–43	76–73	O	Output port
R20–R23	42–39	72–69	O	Output port
COM0, COM1	23,22	–	O	LCD common output pin (1/8, 1/16, 1/17 duty can be selected by software)
COM2–COM14	21,20,18–15,86–92	56–51,112–118		
COM15, COM16	93,94	–		
SEG0–SEG59	14–1,143–110,106–95	50–1,128–119	O	LCD segment output pin
BZ	24	57	O	Sound output pin
SVD	74	100	I	SVD external voltage input pin
$\overline{RESET}$	32	65	I	Initial reset input pin
$\overline{TEST}$	33	66	I	Testing input pin

■ ELECTRICAL CHARACTERISTICS

● Absolute Maximum Ratings

(V_{SS}=0V)

Item	Symbol	Value	Unit
Supply voltage	V_{DD}	-0.5 to 7.0	V
Input voltage (1)	V_I	-0.5 to V_{DD} + 0.3	V
Input voltage (2)	V_{IOSC}	-0.5 to V_{D1} + 0.3	V
Permissible total output current *1	ΣI_{VDD}	10	mA
Operating temperature	Topr	-20 to 70	°C
Storage temperature	Tstg	-65 to 150	°C
Soldering temperature / time	Tsol	260°C, 10sec (lead section)	–
Permissible dissipation *2	P_D	250	mW

*1 The permissible total output current is the sum total of the current (average current) that simultaneously flows from the output pin (or is drawn in).
*2 In case of plastic package (QFP8-144pin, QFP17-144pin, QFP5-128pin).

● Recommended Operating Conditions

(Ta=-20 to 70°C)

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Supply voltage	V_{DD}	V_{SS}=0V	OSC3 oscillation OFF	1.8	3.0	6.4	V
			OSC1 CR oscillation	2.2	3.0	6.4	V
			OSC3 oscillation ON	2.2	3.0	6.4	V
Oscillation frequency	f_{OSC1}	Crystal oscillation		–	32.768	–	kHz
		CR oscillation		40	60	80	kHz
	f_{OSC3}	CR oscillation			1,800	2,250	kHz
		Ceramic oscillation				4,100	kHz
SVD terminal input voltage	SVD	V_{SS}=0V, SVD≤V_{DD}		0		6.4	V

● DC Characteristics

(Unless otherwise specified: V_{DD}=3.0V, V_{SS}=0V, f_{OSC1}=32.768kHz, Ta=25°C, V_{D1}/V_{C1}/V_{C2}/V_{C4}/V_{C5} are internal voltage, C_1–C_8=0.2µF)

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
High level input voltage (1)	V_{IH1}		K00–03, K10–13 P00–03, P10–13, P20–23	0.8·V_{DD}		V_{DD}	V
High level input voltage (2)	V_{IH2}		$\overline{RESET}$, $\overline{TEST}$	0.9·V_{DD}		V_{DD}	V
Low level input voltage (1)	V_{IL1}		K00–03, K10–13 P00–03, P10–13, P20–23	0		0.2·V_{DD}	V
Low level input voltage (2)	V_{IL2}		$\overline{RESET}$, $\overline{TEST}$	0		0.1·V_{DD}	V
High level input current	I_{IH}	V_{IH}=3.0V	K00–03, K10–13 P00–03, P10–13, P20–23 $\overline{RESET}$, $\overline{TEST}$	0		0.5	µA
Low level input current (1)	I_{IL1}	V_{IL1}=V_{SS} No Pull-up	K00–03, K10–13 P00–03, P10–13, P20–23 $\overline{RESET}$, $\overline{TEST}$	-0.5		0	µA
Low level input current (2)	I_{IL2}	V_{IL2}=V_{SS} With Pull-up	K00–03, K10–13 P00–03, P10–13, P20–23 $\overline{RESET}$, $\overline{TEST}$	-12	-7	-5	µA
High level output current (1)	I_{OH1}	V_{OH1}=0.9·V_{DD}	R00–03, R10–13, R20–23 P00–03, P10–13, P20–23			-2	mA
High level output current (2)	I_{OH2}	V_{OH2}=0.9·V_{DD}	BZ			-2	mA
Low level output current (1)	I_{OL1}	V_{OL1}=0.1·V_{DD}	R00–03, R10–13, R20–23 P00–03, P10–13, P20–23	3			mA
Low level output current (2)	I_{OL2}	V_{OL2}=0.1·V_{DD}	BZ	3			mA
Common output current	I_{OH3}	V_{OH3}=V_{C5}-0.05V	COM0–16			-25	µA
	I_{OL3}	V_{OL3}=V_{SS}+0.05V		25			µA
Segment output current	I_{OH4}	V_{OH4}=V_{C5}-0.05V	SEG0–59			-10	µA
	I_{OL4}	V_{OL4}=V_{SS}+0.05V		10			µA

(Unless otherwise specified: V_{DD}=5.0V, V_{SS}=0V, f_{OSC1}=32.768kHz, Ta=25°C, V_{D1}/V_{C1}/V_{C2}/V_{C4}/V_{C5} are internal voltage, C_1–C_8=0.2µF)

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
High level input voltage (1)	V_{IH1}		K00–03, K10–13 P00–03, P10–13, P20–23	0.8·V_{DD}		V_{DD}	V
High level input voltage (2)	V_{IH2}		$\overline{RESET}$, $\overline{TEST}$	0.9·V_{DD}		V_{DD}	V
Low level input voltage (1)	V_{IL1}		K00–03, K10–13 P00–03, P10–13, P20–23	0		0.2·V_{DD}	V
Low level input voltage (2)	V_{IL2}		$\overline{RESET}$, $\overline{TEST}$	0		0.1·V_{DD}	V
High level input current	I_{IH}	V_{IH}=3.0V	K00–03, K10–13 P00–03, P10–13, P20–23 $\overline{RESET}$, $\overline{TEST}$	0		0.5	µA
Low level input current (1)	I_{IL1}	V_{IL1}=V_{SS} No Pull-up	K00–03, K10–13 P00–03, P10–13, P20–23 $\overline{RESET}$, $\overline{TEST}$	-0.5		0	µA
Low level input current (2)	I_{IL2}	V_{IL2}=V_{SS} With Pull-up	K00–03, K10–13 P00–03, P10–13, P20–23 $\overline{RESET}$, $\overline{TEST}$	-20	-7	-9	µA
High level output current (1)	I_{OH1}	V_{OH1}=0.9·V_{DD}	R00–03, R10–13, R20–23 P00–03, P10–13, P20–23			-5	mA
High level output current (2)	I_{OH2}	V_{OH2}=0.9·V_{DD}	BZ			-5	mA
Low level output current (1)	I_{OL1}	V_{OL1}=0.1·V_{DD}	R00–03, R10–13, R20–23 P00–03, P10–13, P20–23	7.5			mA
Low level output current (2)	I_{OL2}	V_{OL2}=0.1·V_{DD}	BZ	7.5			mA
Common output current	I_{OH3}	V_{OH3}=V_{C5}-0.05V	COM0–16			-25	µA
	I_{OL3}	V_{OL3}=V_{SS}+0.05V		25			µA
Segment output current	I_{OH4}	V_{OH4}=V_{C5}-0.05V	SEG0–59			-10	µA
	I_{OL4}	V_{OL4}=V_{SS}+0.05V		10			µA

● SVD Circuit and Current Consumption

(Unless otherwise specified: V_{DD}=3.0V, V_{SS}=0V, f_{OSC1}=32.768kHz, C_G=25pF, R_{CR1}=600kΩ, R_{CR2}=47kΩ, Ta=25°C, V_{D1}/V_{C1}/V_{C2}/V_{C4}/V_{C5} are internal voltage, C_1–C_8=0.2µF)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
SVD voltage	V_{SVD1}	SVDS0–3="0" (internal)		1.85		
		SVDS0–3="1"		1.90		
		SVDS0–3="2"		2.00		
		SVDS0–3="3"		2.10		
		SVDS0–3="4"		2.20		
		SVDS0–3="5"		2.30		
		SVDS0–3="6"		2.40		
		SVDS0–3="7"	Typ.	2.50	Typ.	V
		SVDS0–3="8"	×0.93	2.60	×1.07	
		SVDS0–3="9"		2.70		
		SVDS0–3="10"		2.80		
		SVDS0–3="11"		2.90		
		SVDS0–3="12"		3.00		
		SVDS0–3="13"		3.10		
		SVDS0–3="14"		3.20		
		SVDS0–3="15"		3.30		
SVD voltage (external) *4	V_{SVD2}	SVDS0–3="0" (external)	0.95	1.05	1.15	V
SVD circuit response time	t_{SVD}				100	µS
Current consumption	I_{OP}	During HALT (32 kHz crystal oscillation), LCD power OFF *1, *2, *3		1	2	µA
		During HALT (32 kHz crystal oscillation), LCD power ON (V_{C1} standard) *1, *2, *3		6	12	µA
		During HALT (32 kHz crystal oscillation), LCD power ON (V_{C2} standard) *1, *2, *3		4	8	µA
		During HALT (60 kHz CR oscillation), LCD power OFF *1, *3		23	45	µA
		During HALT (60 kHz CR oscillation), LCD power ON (V_{C1} standard) *1, *3		30	60	µA
		During HALT (60 kHz CR oscillation), LCD power ON (V_{C2} standard) *1, *3		26	50	µA
		During execution (32 kHz crystal oscillation), LCD power ON (V_{C1} standard) *1, *2, *3		10	19	µA
		During execution (60 kHz CR oscillation), LCD power ON (V_{C1} standard) *1, *3		45	80	µA
		During execution (2 MHz ceramic oscillation), LCD power ON (V_{C1} standard) *1		600	800	µA
		During execution (4 MHz ceramic oscillation), LCD power ON (V_{C1} standard) *1		1,200	1,400	µA
		During execution (1,800 kHz CR oscillation), LCD power ON (V_{C1} standard) *1		800	1,000	µA
		SVD circuit current (during supply voltage detection) V_{DD}=1.85 to 6.4 V	1		7	µA
		SVD circuit current (during external voltage detection) V_{DD}=1.85 to 6.4 V	0.5		3	µA

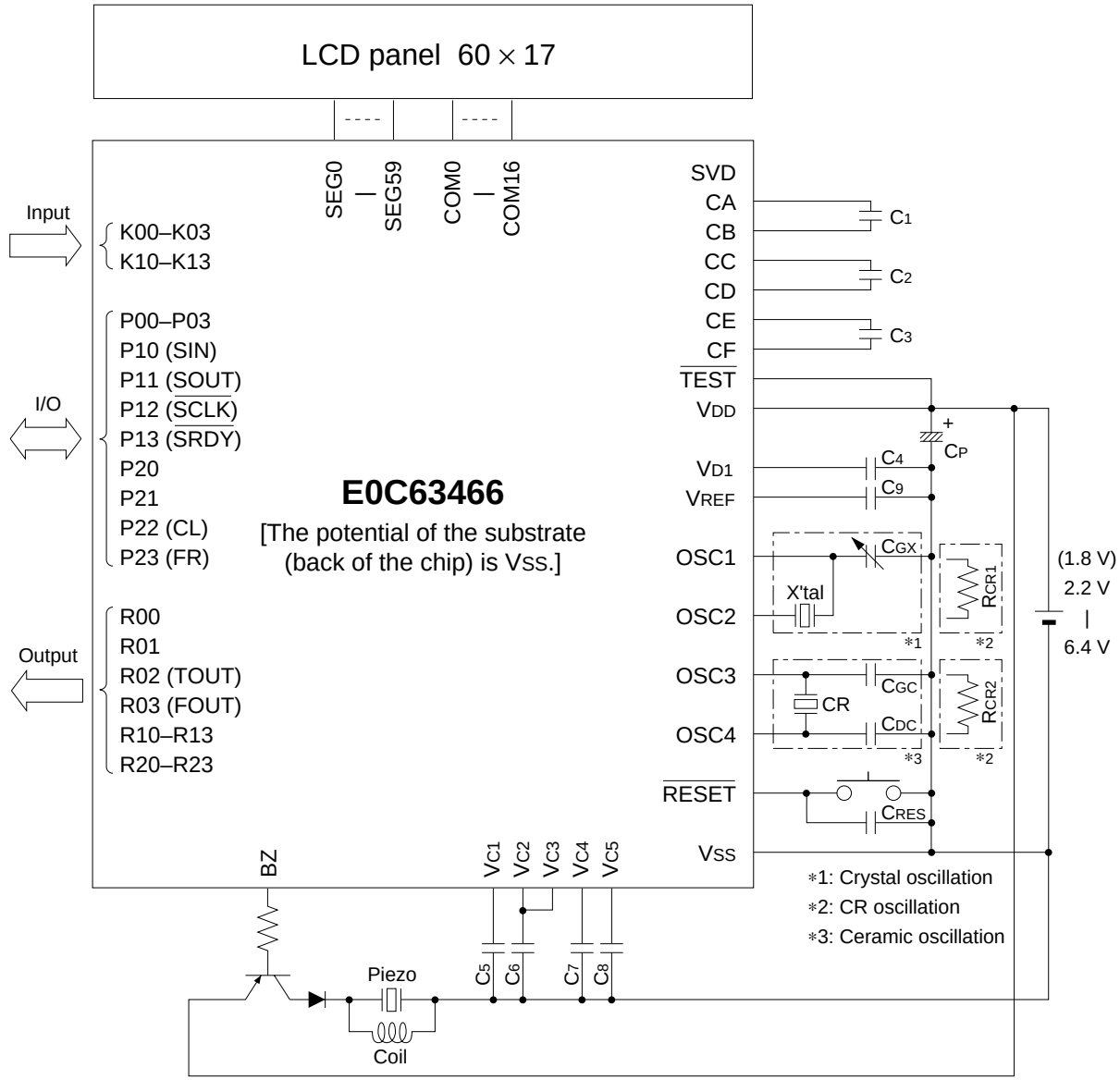
*1 Without panel load. The SVD circuit is OFF.
*2 VDC = "0"
*3 OSCC = "0"
*4 Please input the voltage, which is within the range between V_{SS} and V_{DD}, into the SVD terminal.

● LCD Driver

(Unless otherwise specified: V_{DD}=3.0V, V_{SS}=0V, f_{OSC1}=32.768kHz, C_G=25pF, Ta=25°C, V_{D1}/V_{C1}/V_{C2}/V_{C4}/V_{C5} are internal voltage, C_1–C_8=0.2µF)

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
LCD drive voltage (when V_{C1} standard is selected)	V_{C1}	Connect 1 MΩ load resistor between V_{SS} and V_{C1} (without panel load)	LC0–3="0"	Typ. ×0.88	0.975	Typ. ×1.12	V
			LC0–3="1"		0.990		
			LC0–3="2"		1.005		
			LC0–3="3"		1.020		
			LC0–3="4"		1.035		
			LC0–3="5"		1.050		
			LC0–3="6"		1.065		
			LC0–3="7"		1.080		
			LC0–3="8"		1.095		
			LC0–3="9"		1.110		
			LC0–3="10"		1.125		
			LC0–3="11"		1.140		
			LC0–3="12"		1.155		
			LC0–3="13"		1.170		
			LC0–3="14"		1.185		
			LC0–3="15"		1.200		
	V_{C2}	Connect 1 MΩ load resistor between V_{SS} and V_{C2} (without panel load)		2·V_{C1}		2·V_{C1} ×0.9	V
	V_{C4}	Connect 1 MΩ load resistor between V_{SS} and V_{C4} (without panel load)		3·V_{C1}		3·V_{C1} ×0.9	V
	V_{C5}	Connect 1 MΩ load resistor between V_{SS} and V_{C5} (without panel load)		4·V_{C1}		4·V_{C1} ×0.9	V
LCD drive voltage (when V_{C2} standard is selected)	V_{C1}	Connect 1 MΩ load resistor between V_{SS} and V_{C1} (without panel load)		1/2·V_{C2} -0.1		1/2·V_{C2} ×0.95	V
	V_{C2}	Connect 1 MΩ load resistor between V_{SS} and V_{C2} (without panel load)	LC0–3="0"	Typ. ×0.88	1.95	Typ. ×1.12	V
			LC0–3="1"		1.98		
			LC0–3="2"		2.01		
			LC0–3="3"		2.04		
			LC0–3="4"		2.07		
			LC0–3="5"		2.10		
			LC0–3="6"		2.13		
			LC0–3="7"		2.16		
			LC0–3="8"		2.19		
			LC0–3="9"		2.22		
			LC0–3="10"		2.25		
			LC0–3="11"		2.28		
			LC0–3="12"		2.31		
			LC0–3="13"		2.34		
			LC0–3="14"		2.37		
			LC0–3="15"		2.40		
	V_{C4}	Connect 1 MΩ load resistor between V_{SS} and V_{C4} (without panel load)		3/2·V_{C2} ×0.95		3/2·V_{C2}	V
	V_{C5}	Connect 1 MΩ load resistor between V_{SS} and V_{C5} (without panel load)		2·V_{C2} ×0.95		2·V_{C2}	V

■ BASIC EXTERNAL CONNECTION DIAGRAM

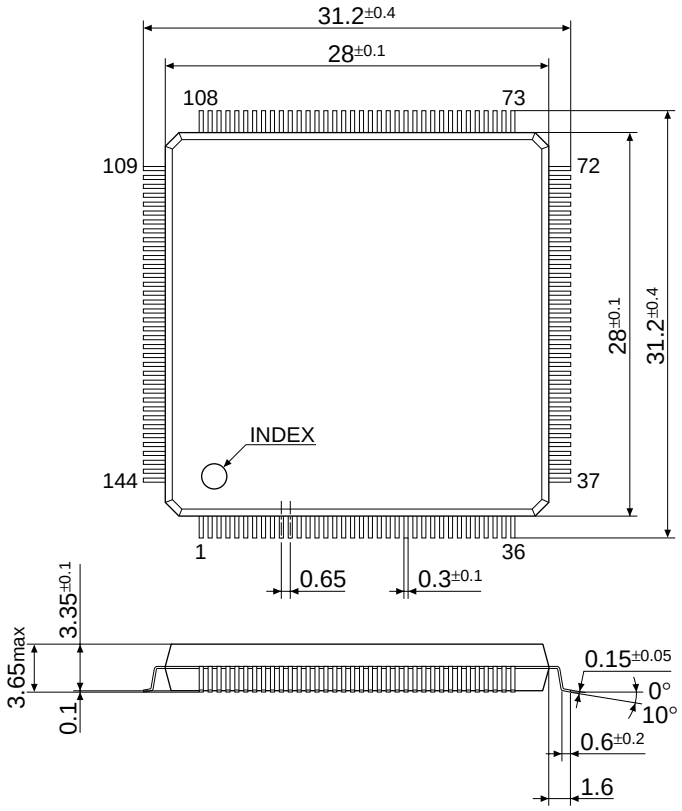


X'tal	Crystal oscillator	32.768 kHz, C_I (Max.) = 34 kΩ
C_{GX}	Trimmer capacitor	5–25 pF
R_{CR1}	Resistor for OSC1 CR oscillation	600 kΩ (60 kHz)
CR	Ceramic oscillator	4 MHz (3.0 V)
C_{GC}	Gate capacitor	30 pF
C_{DC}	Drain capacitor	30 pF
R_{CR2}	Resistor for OSC3 CR oscillation	47 kΩ (1.8 MHz)
C_1–C_8	Capacitor	0.2 µF
C_9	Capacitor	0.1 µF
C_P	Capacitor	3.3 µF
C_{RES}	$\overline{\text{RESET}}$ terminal capacitor	0.1 µF

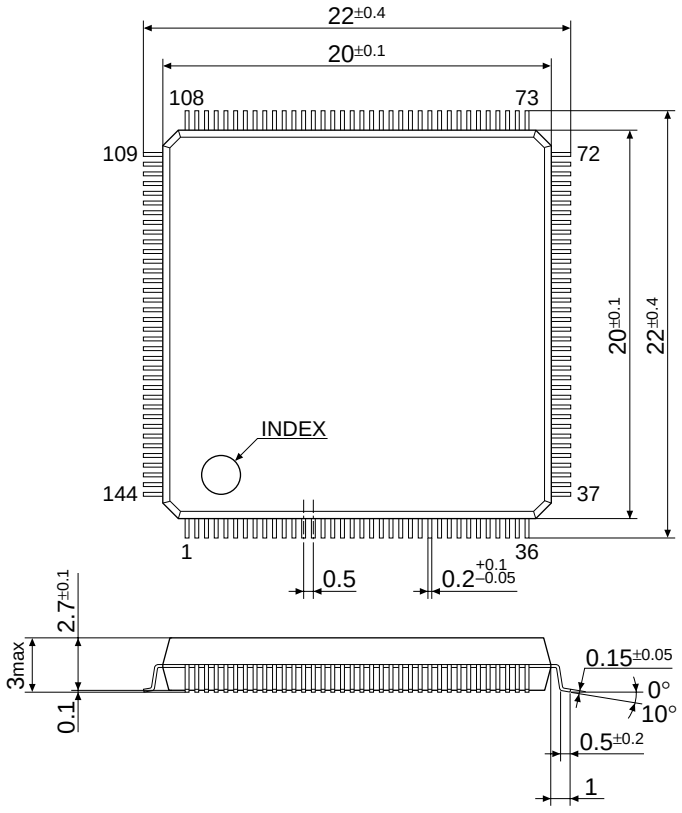
Note: The above table is simply an example, and is not guaranteed to work.

■ PACKAGE DIMENSIONS

QFP8-144pin

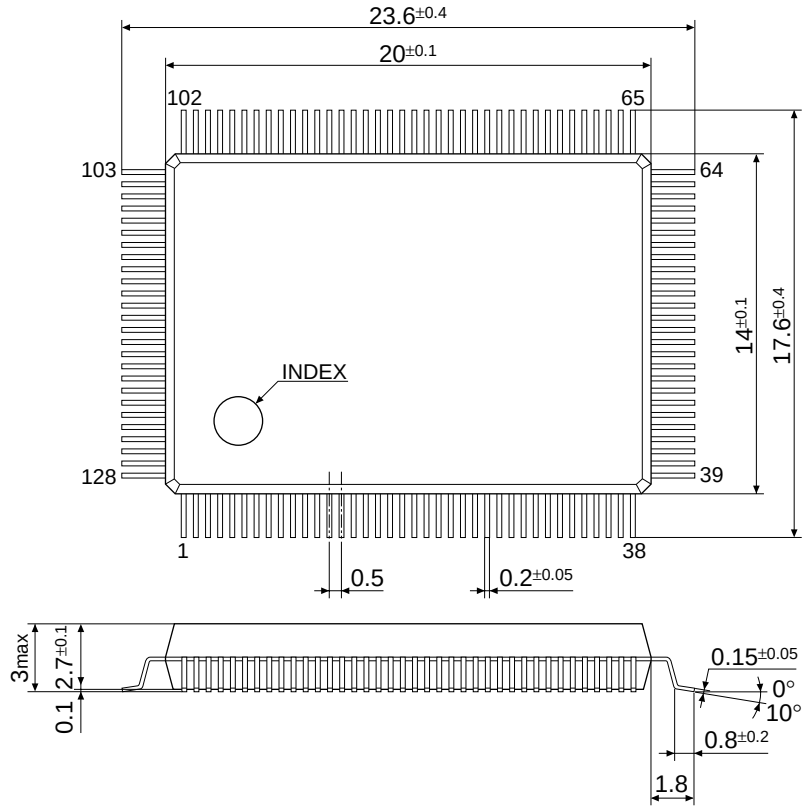


QFP17-144pin



Unit: mm

QFP5-128pin



Unit: mm

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