EPSON

E0C63467

4-bit Single Chip Microcomputer

Preliminary

- 4-bit E0C63000 Core CPU
- Built-in Dot-matrix LCD Driver
- High Speed Instruction Cycle (2-6CPI)

■ DESCRIPTION

The E0C63467 is a CMOS 4-bit microcomputer composed of a CMOS 4-bit core CPU, ROM, RAM, dot-matrix type LCD driver, serial interface and counters. And the E0C63467 can be operated with high speed and spend little current.

■ FEATURES

- CMOS LSI 4-bit parallel processing ..... E0C63000 core CPU
- Main clock ..... 32.768kHz (Typ.) crystal or 60kHz (Typ.) CR oscillation circuit (∗1)
  Built-in resistor is available for CR oscillation circuit (∗1)
- Sub clock ..... 1.8MHz (Typ.) CR or 4MHz (Max.) ceramic oscillation circuit (∗1)
  Built-in resistor is available for CR oscillation circuit (200kHz/1.8MHz ∗1)
- Instruction set ..... Basic instruction : 47 types (411 instructions with all)
  Addressing mode : 8 types
- Instruction execution time ..... During operation at 32.768kHz : 61µsec, 122µsec, 183µsec
  During operation at 60kHz : 33µsec, 67µsec, 100µsec
  During operation at 200kHz : 10µsec, 20µsec, 30µsec
  During operation at 4MHz : 0.5µsec, 1µsec, 1.5µsec
- ROM capacity ..... Code ROM : 16,384 words × 13 bits
  Data ROM : 1,024 words × 4 bits (= 4K bits)
- RAM capacity ..... Data memory : 2,304 words × 4 bits
  Display memory : 540 bits (120 words × 4 bits + 60 × 1 bit)
- Input port ..... 8 bits (Pull-up resistors are available ∗1)
- Output port ..... 4 bits (It is possible to switch 1 bit to FOUT output ∗2)
- I/O port ..... 16 bits (It is possible to switch 1 bit to external SVD input ∗1
  and 4 bits to serial I/O port ∗2)
- Serial interface ..... 1 port (8-bit clock synchronous system)
- LCD driver ..... 60 segments × 8 or 9 commons (∗2)
- Time base counter ..... 1 system (Clock timer)
- Watchdog timer ..... Built-in
- Sound generator ..... With envelope and 1-shot output functions
- Supply voltage detection (SVD) circuit .. 15 values, programmable (1.20 to 2.90V)
  (It is possible to switch 1 value to the external voltage detection ∗1)
- Interrupts ..... External interrupt : Input port interrupt 2 systems
  Internal interrupt : Clock timer interrupt 4 systems
  : Serial interface interrupt 1 system
- Power supply voltage ..... 1.2 to 3.6V (Min. 2.2V when OSC3 ceramic oscillator or external resistor type CR oscillator is used)
- Operating temperature range ..... -20°C to 70°C

● Current consumption (Typ.) ..... Low-power operation:

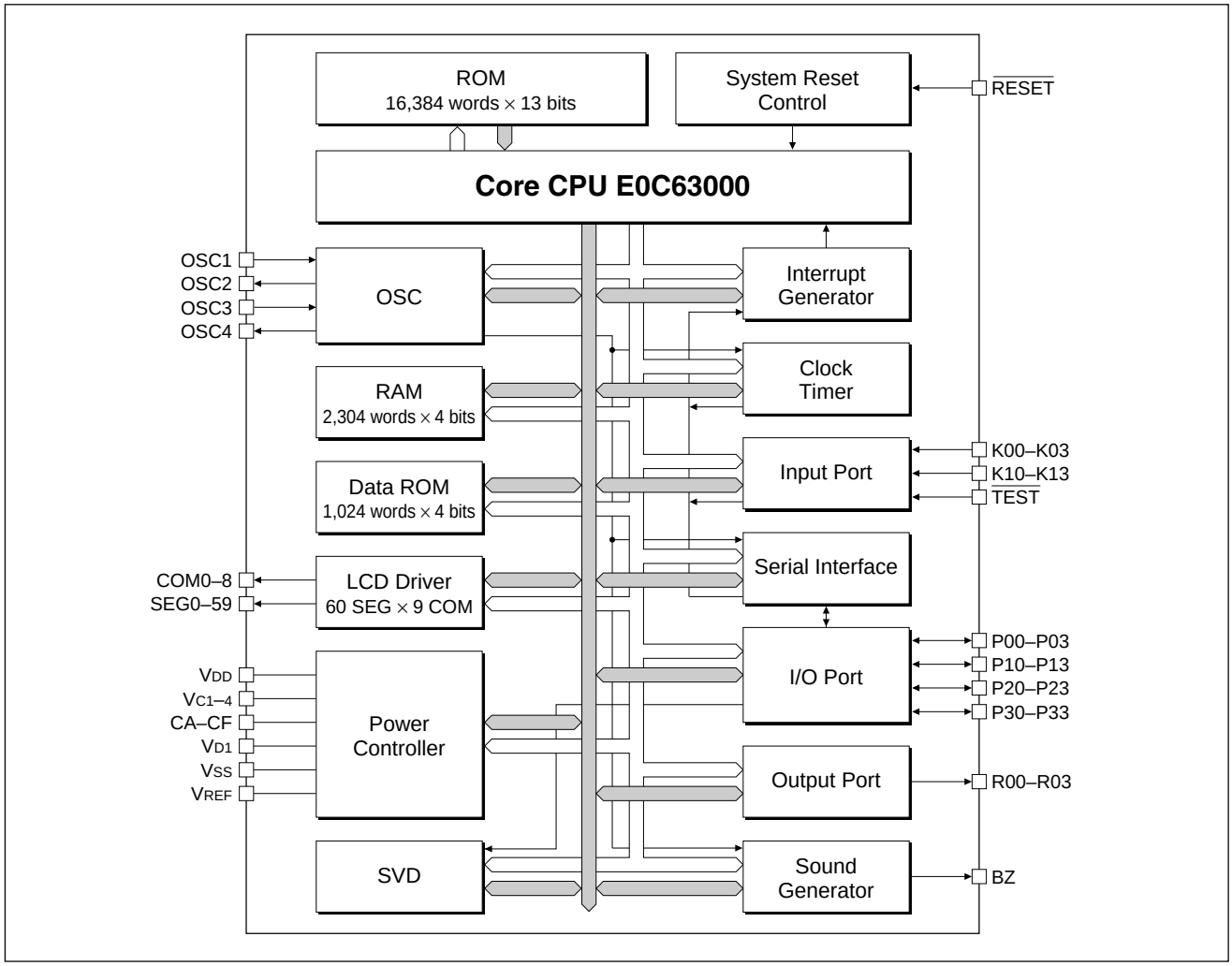
During SLEEP	0.5µA
During HALT (32kHz, crystal oscillation)	
1.5V (LCD power OFF)	2µA
1.5V (LCD power ON, V_{C1} standard)	6µA
3.0V (LCD power OFF)	2µA
3.0V (LCD power ON, V_{C1} standard)	6µA
3.0V (LCD power ON, V_{C2} standard)	4µA
During operation (32kHz)	
3.0V (LCD power ON, V_{C1} standard)	10µA
High-speed operation:	
During operation (200kHz, CR oscillation)	
1.5V (LCD power ON, V_{C1} standard)	20µA
During operation (4MHz, ceramic oscillation)	
3.0V (LCD power ON, V_{C1} standard)	1,000µA

● Package ..... QFP5-128pin (plastic) or chip

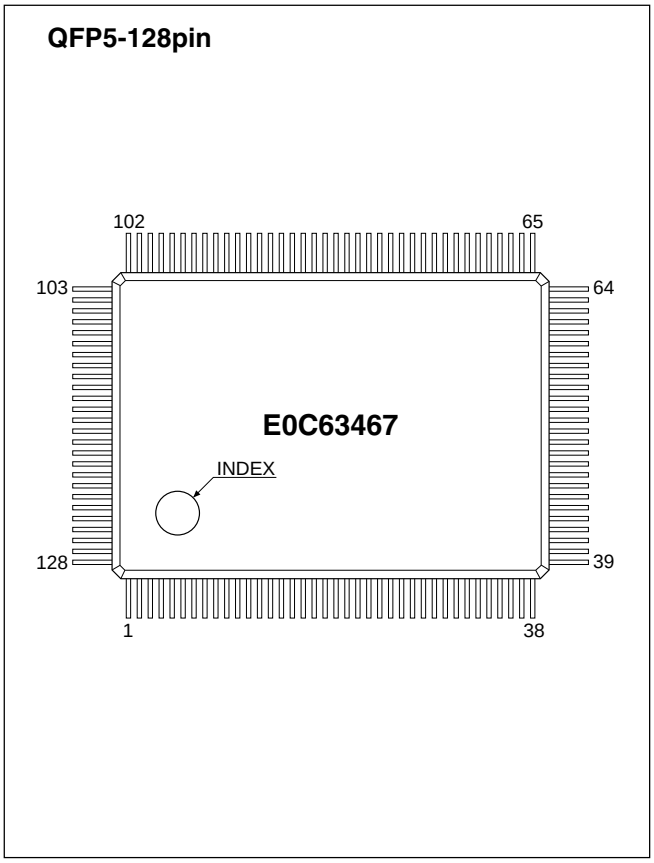
∗1: Can be selected with mask option ∗2: Can be selected with software

∗ This model is under development, therefore the contents of the above specifications may be revised at final.

■ BLOCK DIAGRAM



■ PIN CONFIGURATION



No.	Name	No.	Name	No.	Name	No.	Name
1	SEG45	33	$\overline{TEST}$	65	K10	97	SEG16
2	SEG46	34	$\overline{RESET}$	66	K11	98	N.C.
3	SEG47	35	N.C.	67	K12	99	SEG17
4	SEG48	36	N.C.	68	K13	100	SEG18
5	N.C.	37	N.C.	69	N.C.	101	SEG19
6	SEG49	38	N.C.	70	V_{REF}	102	SEG20
7	SEG50	39	P33	71	V_{C1}	103	N.C.
8	SEG51	40	P32	72	V_{C2}	104	SEG21
9	SEG52	41	P31	73	V_{C3}	105	SEG22
10	SEG53	42	P30	74	V_{C4}	106	SEG23
11	SEG54	43	P23	75	CA	107	SEG24
12	SEG55	44	P22	76	CB	108	SEG25
13	SEG56	45	P21	77	CC	109	SEG26
14	SEG57	46	P20	78	CD	110	SEG27
15	SEG58	47	P13	79	CE	111	SEG28
16	SEG59	48	P12	80	CF	112	SEG29
17	COM8	49	P11	81	SEG0	113	SEG30
18	COM7	50	P10	82	SEG1	114	SEG31
19	COM6	51	P03	83	SEG2	115	SEG32
20	COM5	52	P02	84	SEG3	116	SEG33
21	COM4	53	P01	85	SEG4	117	SEG34
22	COM3	54	P00	86	SEG5	118	SEG35
23	COM2	55	R00	87	SEG6	119	SEG36
24	COM1	56	R01	88	SEG7	120	SEG37
25	COM0	57	R02	89	SEG8	121	SEG38
26	V_{SS}	58	R03	90	SEG9	122	SEG39
27	OSC1	59	BZ	91	SEG10	123	SEG40
28	OSC2	60	K00	92	SEG11	124	SEG41
29	V_{D1}	61	K01	93	SEG12	125	SEG42
30	OSC3	62	K02	94	SEG13	126	SEG43
31	OSC4	63	K03	95	SEG14	127	SEG44
32	V_{DD}	64	N.C.	96	SEG15	128	N.C.

N.C. : No Connection

■ PIN DESCRIPTION

Pin name	Pin No.	In/Out	Function
V_{DD}	32	–	Power (+) supply pin
V_{SS}	26	–	Power (–) supply pin
V_{D1}	29	–	Oscillation/internal logic system regulated voltage output pin
V_{C1}–V_{C4}	71–74	–	LCD system power supply pin (1/4 bias)
V_{REF}	70	O	LCD system power supply testing pin
CA–CF	75–80	–	LCD system boosting/reducing capacitor connecting pin
OSC1	27	I	Crystal or CR oscillation input pin (selected by mask option)
OSC2	28	O	Crystal or CR oscillation output pin (selected by mask option)
OSC3	30	I	Ceramic or CR oscillation input pin (selected by mask option)
OSC4	31	O	Ceramic or CR oscillation output pin (selected by mask option)
K00–K03	60–63	I	Input port
K10–K13	65–68	I	Input port
P00–P03	54–51	I/O	I/O port
P10–P13	50–47	I/O	I/O port or serial I/F input/output (selected by software)
P20–P23	46–43	I/O	I/O port
P30–P32	42–40	I/O	I/O port
P33	39	I/O	I/O port or SVD external voltage input (selected by mask option)
R00–R02	55–57	O	Output port
R03	58	O	Output port or FOUT signal output (selected by software)
BZ	59	O	Sound output pin
COM0–COM8	25–17	O	LCD common output pin (1/8 or 1/9 duty can be selected by software)
SEG0–SEG59	81–97, 99–102 104–127, 1–4, 6–16	O	LCD segment output pin
$\overline{RESET}$	34	I	Initial reset input pin
$\overline{TEST}$	33	I	Testing input pin

■ MASK OPTION LIST

The following options can be set for the E0C63467. Multiple specifications are available in each option item as indicated in the option list. Using "E0C63467 Technical Manual" as reference, select the specifications that meet the target system and check the appropriate box. Be sure to record the specifications for unused functions too, according to the instructions provided. Refer to the "E0C63 Family Development Tool Manual" for the WINFOG.

1 OSC1 SYSTEM CLOCK

☐ 1. Crystal (32.768kHz, Normal Reset)
☐ 2. CR (60kHz, Normal Reset)
☐ 3. CR (60kHz, Special Reset)

2 OSC3 SYSTEM CLOCK

☐ 1. CR (200kHz)
☐ 2. CR (1.8MHz)
☐ 3. Ceramic (4MHz)
☐ 4. CR External Resistor

3 INPUT PORT PULL UP RESISTOR

• K00	☐ 1. With Resistor	☐ 2. Gate Direct
• K01	☐ 1. With Resistor	☐ 2. Gate Direct
• K02	☐ 1. With Resistor	☐ 2. Gate Direct
• K03	☐ 1. With Resistor	☐ 2. Gate Direct
• K10	☐ 1. With Resistor	☐ 2. Gate Direct
• K11	☐ 1. With Resistor	☐ 2. Gate Direct
• K12	☐ 1. With Resistor	☐ 2. Gate Direct
• K13	☐ 1. With Resistor	☐ 2. Gate Direct

4 OUTPUT PORT OUTPUT SPECIFICATION

• R00	☐ 1. Complementary	☐ 2. Nch Open Drain
• R01	☐ 1. Complementary	☐ 2. Nch Open Drain
• R02	☐ 1. Complementary	☐ 2. Nch Open Drain
• R03	☐ 1. Complementary	☐ 2. Nch Open Drain

5 I/O PORT OUTPUT SPECIFICATION

• P00	☐ 1. Complementary	☐ 2. Nch Open Drain
• P01	☐ 1. Complementary	☐ 2. Nch Open Drain
• P02	☐ 1. Complementary	☐ 2. Nch Open Drain
• P03	☐ 1. Complementary	☐ 2. Nch Open Drain
• P10	☐ 1. Complementary	☐ 2. Nch Open Drain
• P11	☐ 1. Complementary	☐ 2. Nch Open Drain
• P12	☐ 1. Complementary	☐ 2. Nch Open Drain
• P13	☐ 1. Complementary	☐ 2. Nch Open Drain
• P20	☐ 1. Complementary	☐ 2. Nch Open Drain
• P21	☐ 1. Complementary	☐ 2. Nch Open Drain
• P22	☐ 1. Complementary	☐ 2. Nch Open Drain
• P23	☐ 1. Complementary	☐ 2. Nch Open Drain
• P30	☐ 1. Complementary	☐ 2. Nch Open Drain
• P31	☐ 1. Complementary	☐ 2. Nch Open Drain
• P32	☐ 1. Complementary	☐ 2. Nch Open Drain
• P33	☐ 1. Complementary	☐ 2. Nch Open Drain

6 I/O PORT PULL UP RESISTOR

• P00	☐ 1. With Resistor	☐ 2. Gate Direct
• P01	☐ 1. With Resistor	☐ 2. Gate Direct
• P02	☐ 1. With Resistor	☐ 2. Gate Direct
• P03	☐ 1. With Resistor	☐ 2. Gate Direct
• P10	☐ 1. With Resistor	☐ 2. Gate Direct
• P11	☐ 1. With Resistor	☐ 2. Gate Direct
• P12	☐ 1. With Resistor	☐ 2. Gate Direct
• P13	☐ 1. With Resistor	☐ 2. Gate Direct
• P20	☐ 1. With Resistor	☐ 2. Gate Direct
• P21	☐ 1. With Resistor	☐ 2. Gate Direct
• P22	☐ 1. With Resistor	☐ 2. Gate Direct
• P23	☐ 1. With Resistor	☐ 2. Gate Direct
• P30	☐ 1. With Resistor	☐ 2. Gate Direct
• P31	☐ 1. With Resistor	☐ 2. Gate Direct
• P32	☐ 1. With Resistor	☐ 2. Gate Direct
• P33	☐ 1. With Resistor	☐ 2. Gate Direct

7 EXTERNAL SVD DETECTION FROM P33 PAD

☐ 1. Enable
☐ 2. Disable

8 SERIAL INTERFACE POLARITY

☐ 1. Positive
☐ 2. Negative

9 SOUND GENERATOR POLARITY

☐ 1. Positive
☐ 2. Negative

■ ELECTRICAL CHARACTERISTICS

● Absolute Maximum Ratings

(V_{SS}=0V)

Rating	Symbol	Value	Unit
Supply voltage	V_{DD}	-0.5 to 7.0	V
Input voltage (1)	V_I	-0.5 to V_{DD} + 0.3	V
Input voltage (2)	V_{IOSC}	-0.5 to V_{D1} + 0.3	V
Permissible total output current *1	ΣI_{VDD}	10	mA
Operating temperature	Topr	-20 to 70	°C
Storage temperature	Tstg	-65 to 150	°C
Soldering temperature / time	Tsol	260°C, 10sec (lead section)	–
Permissible dissipation *2	P_D	250	mW

*1 The permissible total output current is the sum total of the current (average current) that simultaneously flows from the output pin (or is drawn in).
*2 In case of plastic package (QFP5-128pin).

● Recommended Operating Conditions

(Ta=-20 to 70°C)

Condition	Symbol	Remark		Min.	Typ.	Max.	Unit
Supply voltage	V_{DD}	V_{SS}=0V	OSC3 oscillation OFF	1.20	1.50	3.60	V
			OSC3 oscillation (200kHz) ON	1.20	1.50	3.60	V
			OSC3 oscillation (1.8MHz/4MHz) ON	2.20	3.00	3.60	V
Oscillation frequency	f_{OSC1}	Crystal oscillation		–	32.768	–	kHz
		CR oscillation (built-in R)			60		kHz
	f_{OSC3}	CR oscillation (Typ. 200kHz, built-in R)			200		kHz
		CR oscillation (Typ. 1.8MHz, built-in R)			1,800		kHz
		CR oscillation (Typ. 1.8MHz, external R)			1,800		kHz
		Ceramic oscillation				4,100	kHz
SVD terminal input voltage	SVD	V_{SS}=0V, SVD≤V_{DD}		0		3.6	V

● DC Characteristics

Input Characteristics

(Unless otherwise specified: V_{DD}=1.2 to 3.6V, V_{SS}=0V, Ta=-20 to 70°C)

Characteristic	Symbol	Condition		Min.	Typ.	Max.	Unit
High-level input voltage	V_{IH1}		Kxx	0.8V_{DD}		V_{DD}	V
	V_{IH2}		Pxx (V_{DC}=0)	1.0		V_{DD}	V
			Pxx (V_{DC}=1)	1.7		V_{DD}	V
Low-level input voltage	V_{IL1}		Kxx	0		0.2V_{DD}	V
	V_{IL2}		Pxx (V_{DC}=0)	0		0.3	V
			Pxx (V_{DC}=1)	0		0.6	V
High-level schmitt input voltage	V_{T+}		$\overline{RESET}$	0.5V_{DD}		0.9V_{DD}	V
Low-level schmitt input voltage	V_{T-}			0.1V_{DD}		0.5V_{DD}	V
Input leak current	I_{LIH}	V_{LIH}=V_{DD}	Kxx, Pxx, $\overline{RESET}$	0		1.0	µA
	I_{LIL}	V_{LIL}=V_{SS}		-1.0		0	µA
Input pull-up resistance	R_{IN}		Kxx, Pxx, $\overline{RESET}$	200		700	kΩ
Input terminal capacitance	C_{IN}	V_{IN}=0V, f=32kHz	Kxx, Pxx			15	pF

Output Characteristics

(Unless otherwise specified: V_{DD}=1.5V, V_{SS}=0V, Ta=-20 to 70°C, V_{D1}/V_{C1}/V_{C2}/V_{C3}/V_{C4} are internal voltage, C_1–C_8=0.2µF)

Characteristic	Symbol	Condition		Min.	Typ.	Max.	Unit
High-level output voltage	I_{OH1}	V_{OH1}=0.9·V_{DD}	Pxx, Rxx, BZ			-0.3	mA
Low-level output voltage	I_{OL1}	V_{OL1}=0.1·V_{DD}	Pxx, Rxx, BZ	0.45			mA
Output leak current	I_{LOH}	V_{LOH}=V_{DD}	Pxx, Rxx, BZ	-0.5		0.5	µA
	I_{LOL}	V_{LOL}=V_{SS}		-0.5		0.5	µA
Common output current	I_{COMH}	V_{COMH}=V_{C4}-0.05V	COMx			-25	µA
	I_{COML}	V_{COML}=V_{SS}+0.05V		25			µA
Segment output current	I_{SEGH}	V_{SEGH}=V_{C4}-0.05V	SEGxx			-10	µA
	I_{SEGL}	V_{SEGL}=V_{SS}+0.05V		10			µA

● Analog Circuit Characteristics

(Unless otherwise specified: V_{DD}=3.0V, V_{SS}=0V, f_{OSC1}=32.768kHz, C_G=25pF, Ta=25°C, V_{D1}/V_{C1}/V_{C2}/V_{C3}/V_{C4} are internal voltage, C_1–C_8=0.2µF)

Characteristic	Symbol	Condition		Min.	Typ.	Max.	Unit
LCD drive voltage (when V_{C1} standard is selected)	V_{C1}	Connect 1 MΩ load resistor between V_{SS} and V_{C1} (without panel load)	LC0–3="0"	Typ. ×0.88	0.975	Typ. ×1.12	V
			LC0–3="1"		0.990		
			LC0–3="2"		1.005		
			LC0–3="3"		1.020		
			LC0–3="4"		1.035		
			LC0–3="5"		1.050		
			LC0–3="6"		1.065		
			LC0–3="7"		1.080		
			LC0–3="8"		1.095		
			LC0–3="9"		1.110		
			LC0–3="10"		1.125		
			LC0–3="11"		1.140		
			LC0–3="12"		1.155		
			LC0–3="13"		1.170		
			LC0–3="14"		1.185		
			LC0–3="15"		1.200		
	V_{C2}	Connect 1 MΩ load resistor between V_{SS} and V_{C2} (without panel load)		2·V_{C1}		2·V_{C1} ×0.9	V
	V_{C3}	Connect 1 MΩ load resistor between V_{SS} and V_{C3} (without panel load)		3·V_{C1}		3·V_{C1} ×0.9	V
	V_{C4}	Connect 1 MΩ load resistor between V_{SS} and V_{C4} (without panel load)		4·V_{C1}		4·V_{C1} ×0.9	V
LCD drive voltage (when V_{C2} standard is selected)	V_{C1}	Connect 1 MΩ load resistor between V_{SS} and V_{C1} (without panel load)		1/2·V_{C2} -0.1		1/2·V_{C2} ×0.95	V
	V_{C2}	Connect 1 MΩ load resistor between V_{SS} and V_{C2} (without panel load)	LC0–3="0"	Typ. ×0.88	1.95	Typ. ×1.12	V
			LC0–3="1"		1.98		
			LC0–3="2"		2.01		
			LC0–3="3"		2.04		
			LC0–3="4"		2.07		
			LC0–3="5"		2.10		
			LC0–3="6"		2.13		
			LC0–3="7"		2.16		
			LC0–3="8"		2.19		
			LC0–3="9"		2.22		
			LC0–3="10"		2.25		
			LC0–3="11"		2.28		
			LC0–3="12"		2.31		
			LC0–3="13"		2.34		
			LC0–3="14"		2.37		
			LC0–3="15"		2.40		
	V_{C3}	Connect 1 MΩ load resistor between V_{SS} and V_{C3} (without panel load)		3/2·V_{C2} ×0.95		3/2·V_{C2}	V
	V_{C4}	Connect 1 MΩ load resistor between V_{SS} and V_{C4} (without panel load)		2·V_{C2} ×0.95		2·V_{C2}	V
SVD voltage	V_{SVD1}	SVDS0–3="0" (internal)		Typ. ×0.93	1.20	Typ. ×1.07	V
		SVDS0–3="1"			1.20		
		SVDS0–3="2"			1.25		
		SVDS0–3="3"			1.30		
		SVDS0–3="4"			1.35		
		SVDS0–3="5"			1.40		
		SVDS0–3="6"			1.45		
		SVDS0–3="7"			1.50		
		SVDS0–3="8"			2.20		
		SVDS0–3="9"			2.30		
		SVDS0–3="10"			2.40		
		SVDS0–3="11"			2.50		
		SVDS0–3="12"			2.60		
		SVDS0–3="13"			2.70		
		SVDS0–3="14"			2.80		
		SVDS0–3="15"			2.90		
SVD voltage (external)*1	V_{SVD2}	SVDS0–3="0" (external)		0.88	0.98	1.08	V
SVD circuit response time	t_{SVD}					100	µS

*1 Please input the voltage, which is within the range between V_{SS} and V_{DD}, into the SVD terminal.

● Current Consumption

(Unless otherwise specified: V_{DD}=1.2 to 3.6V, V_{SS}=0V, f_{OSC1}=32.768kHz, C_G=25pF, Ta=-25°C, V_{D1}/V_{C1}/V_{C2}/V_{C3}/V_{C4} are internal voltage, C_1–C_8=0.2µF)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Current consumption during SLEEP	I_{SLP}	LCD off *1				µA
Current consumption during HALT	I_{HALT}	V_{DD}=1.5V, OSC1=32kHz crystal, LCD off *2				µA
		V_{DD}=1.5V, OSC1=32kHz crystal, LCD on (V_{C1} std.) *2				µA
		V_{DD}=1.5V, OSC1=60kHz CR, LCD off *2				µA
		V_{DD}=1.5V, OSC1=60kHz CR, LCD on (V_{C1} std.) *2				µA
		V_{DD}=3.0V, OSC1=32kHz crystal, LCD off *2				µA
		V_{DD}=3.0V, OSC1=32kHz crystal, LCD on (V_{C1} std.) *2				µA
		V_{DD}=3.0V, OSC1=32kHz crystal, LCD on (V_{C2} std.) *2				µA
		V_{DD}=3.0V, OSC1=60kHz CR, LCD off *2				µA
		V_{DD}=3.0V, OSC1=60kHz CR, LCD on (V_{C1} std.) *2				µA
		V_{DD}=3.0V, OSC1=60kHz CR, LCD on (V_{C2} std.) *2				µA
Current consumption during execution (software duty = 100%)	I_{EXE}	V_{DD}=1.5V, OSC1=32kHz crystal, LCD on (V_{C1} std.) *3				µA
		V_{DD}=1.5V, OSC1=60kHz CR, LCD on (V_{C1} std.) *3				µA
		V_{DD}=3.0V, OSC1=32kHz crystal, LCD on (V_{C1} std.) *3				µA
		V_{DD}=3.0V, OSC1=32kHz crystal, LCD on (V_{C2} std.) *3				µA
		V_{DD}=3.0V, OSC1=60kHz CR, LCD on (V_{C1} std.) *3				µA
		V_{DD}=3.0V, OSC1=60kHz CR, LCD on (V_{C2} std.) *3				µA
		V_{DD}=1.5V, OSC3=200kHz CR, LCD on (V_{C1} std.) *4				µA
		V_{DD}=3.0V, OSC3=1.8MHz CR, LCD on (V_{C1} std.) *4				µA
		V_{DD}=3.0V, OSC3=1.8MHz CR, LCD on (V_{C2} std.) *4				µA
		V_{DD}=3.0V, OSC3=4MHz ceramic, LCD on (V_{C1} std.) *4				µA
		V_{DD}=3.0V, OSC3=4MHz ceramic, LCD on (V_{C2} std.) *4				µA
SVD circuit current	I_{SVD}	V_{DD}=1.2 to 3.6V, during supply voltage detection				µA
		V_{DD}=1.2 to 3.6V, during external voltage detection				µA

*1 No panel load, No heavy load, OSC1=off, OSC3=off, CPU/ROM/RAM=sleep, Timer=stop, SVD=off
*2 No panel load, No heavy load, OSC1=on, OSC3=off, CPU/ROM/RAM=halt, Timer=run, SVD=off
*3 No panel load, No heavy load, OSC1=on, OSC3=off, CPU/ROM/RAM=run, Timer=run, SVD=off
*4 No panel load, No heavy load, OSC1=on, OSC3=on, CPU/ROM/RAM=run, Timer=run, SVD=off

● Oscillation Characteristics

The oscillation characteristics change depending on the conditions (components used, board pattern, etc.). Use the following characteristics as reference values.

OSC1 Crystal Oscillation Circuit

(Unless otherwise specified: V_{DD}=1.5V, V_{SS}=0V, f_{OSC1}=32.768kHz, C_G=25pF, C_D=built-in, Ta=-20 to 70°C)

Characteristic	Symbol	Condition		Min.	Typ.	Max.	Unit
Oscillation start voltage	Vsta	tsta≤3sec (V_{DD})		1.2			V
Oscillation stop voltage	Vstp	tstp≤10sec (V_{DD})		1.2			V
Built-in capacitance (drain)	C_D	Including the parasitic capacitance inside the IC (in chip)			14		pF
Frequency/voltage deviation	∂f/∂V	V_{DD}=1.2 to 3.6V	with VDC switching			5	ppm
			without VDC switching			10	ppm
Frequency/IC deviation	∂f/∂IC			-10		10	ppm
Frequency adjustment range	∂f/∂C_G	C_G=5 to 25pF		10	20		ppm
Harmonic oscillation start voltage	V_{hho}	C_G=5pF (V_{DD})		3.6			V
Permitted leak resistance	R_{leak}	Between OSC1 and V_{SS}		200			MΩ

OSC1 CR Oscillation Circuit (built-in resistor)

(Unless otherwise specified: V_{DD}=1.5V, V_{SS}=0V, R_{CR1}=built-in, Ta=-20 to 70°C)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation frequency dispersion	f_{OSC1}		-30	60kHz	30	%
Oscillation start voltage	Vsta	(V_{DD})	1.2			V
Oscillation start time	tsta	V_{DD}=1.2 to 3.6V			3	mS
Oscillation stop voltage	Vstp	(V_{DD})	1.2			V

OSC3 CR Oscillation Circuit (built-in resistor)

(Unless otherwise specified: V_{DD}=1.5V, V_{SS}=0V, R_{CR2}=built-in, Ta=-20 to 70°C)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation frequency dispersion	f_{OSC3}		-30	200kHz	30	%
Oscillation start voltage	Vsta	(V_{DD})	1.2			V
Oscillation start time	tsta	V_{DD}=1.2 to 3.6V			5	mS
Oscillation stop voltage	Vstp	(V_{DD})	1.2			V

(Unless otherwise specified: V_{DD}=3.0V, V_{SS}=0V, R_{CR2}=built-in, Ta=-20 to 70°C)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation frequency dispersion	f_{OSC3}		-30	1800kHz	30	%
Oscillation start voltage	Vsta	(V_{DD})	2.2			V
Oscillation start time	tsta	V_{DD}=2.2 to 3.6V			3	mS
Oscillation stop voltage	Vstp	(V_{DD})	2.2			V

OSC3 CR Oscillation Circuit (external resistor)

(Unless otherwise specified: V_{DD}=3.0V, V_{SS}=0V, R_{CR2}=47kΩ, Ta=-20 to 70°C)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation frequency dispersion	f_{OSC3}		-25	1800kHz	25	%
Oscillation start voltage	Vsta	(V_{DD})	2.2			V
Oscillation start time	tsta	V_{DD}=2.2 to 3.6V			3	mS
Oscillation stop voltage	Vstp	(V_{DD})	2.2			V

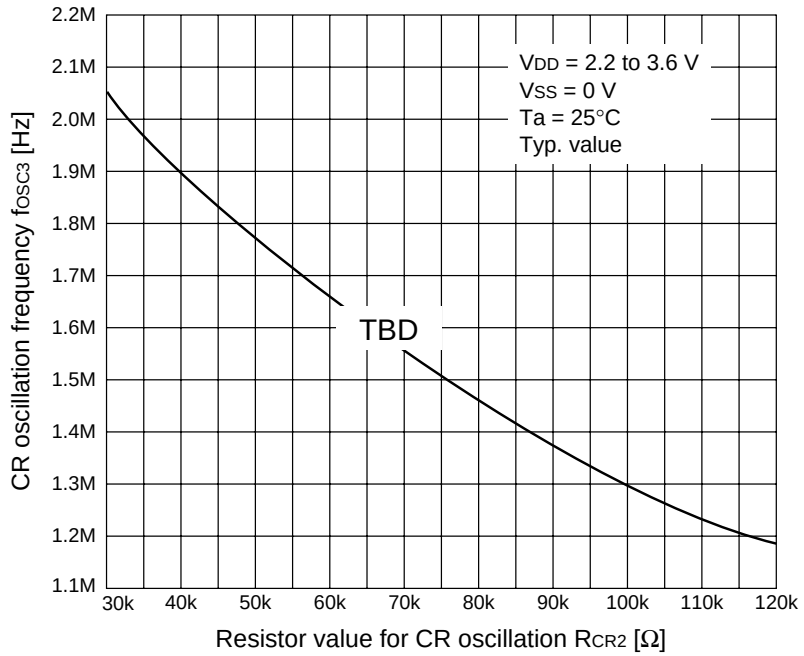
OSC3 Ceramic Oscillation Circuit

(Unless otherwise specified: V_{DD}=3.0V, V_{SS}=0V, Ceramic oscillator: 4MHz, C_{GC}=C_{DC}=30pF, Ta=-20 to 70°C)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start voltage	Vsta	(V_{DD})	2.2			V
Oscillation start time	tsta	V_{DD}=2.2 to 3.6V			5	mS
Oscillation stop voltage	Vstp	(V_{DD})	2.2			V

- **OSC3 CR oscillation (external resistor) frequency-resistance characteristic**

  The oscillation characteristics change depending on the conditions (components used, board pattern, etc.). Use the following characteristics as reference values and evaluate the characteristics on the actual product.



● AC Characteristics

Serial Interface

Clock synchronous master mode

• During 32 kHz operation

(Unless otherwise specified: V_{DD}=3.0V, V_{SS}=0V, Ta=25°C, V_{IH1}=0.8V_{DD}, V_{IL1}=0.2V_{DD}, V_{OH}=0.8V_{DD}, V_{OL}=0.2V_{DD})

Characteristic	Symbol	Min.	Typ.	Max.	Unit
Transmitting data output delay time	tsmd			5	µS
Receiving data input set-up time	tsms	10			µS
Receiving data input hold time	tsmh	5			µS

• During 1 MHz operation

(Unless otherwise specified: V_{DD}=3.0V, V_{SS}=0V, Ta=25°C, V_{IH1}=0.8V_{DD}, V_{IL1}=0.2V_{DD}, V_{OH}=0.8V_{DD}, V_{OL}=0.2V_{DD})

Characteristic	Symbol	Min.	Typ.	Max.	Unit
Transmitting data output delay time	tsmd			200	nS
Receiving data input set-up time	tsms	400			nS
Receiving data input hold time	tsmh	200			nS

Note that the maximum clock frequency is limited to 1 MHz.

Clock synchronous slave mode

• During 32 kHz operation

(Unless otherwise specified: V_{DD}=3.0V, V_{SS}=0V, Ta=25°C, V_{IH1}=0.8V_{DD}, V_{IL1}=0.2V_{DD}, V_{OH}=0.8V_{DD}, V_{OL}=0.2V_{DD})

Characteristic	Symbol	Min.	Typ.	Max.	Unit
Transmitting data output delay time	tssd			10	µS
Receiving data input set-up time	tsss	10			µS
Receiving data input hold time	tssh	5			µS

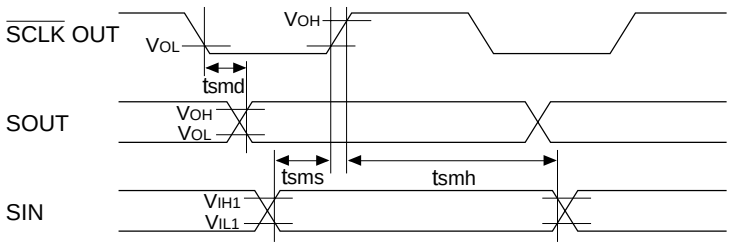
• During 1 MHz operation

(Unless otherwise specified: V_{DD}=3.0V, V_{SS}=0V, Ta=25°C, V_{IH1}=0.8V_{DD}, V_{IL1}=0.2V_{DD}, V_{OH}=0.8V_{DD}, V_{OL}=0.2V_{DD})

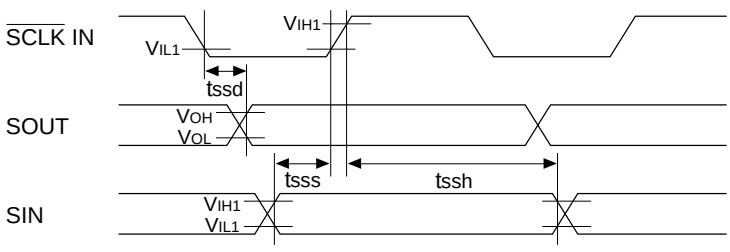
Characteristic	Symbol	Min.	Typ.	Max.	Unit
Transmitting data output delay time	tssd			500	nS
Receiving data input set-up time	tsss	400			nS
Receiving data input hold time	tssh	200			nS

Note that the maximum clock frequency is limited to 1 MHz.

<Master mode>



<Slave mode>



Operating Range

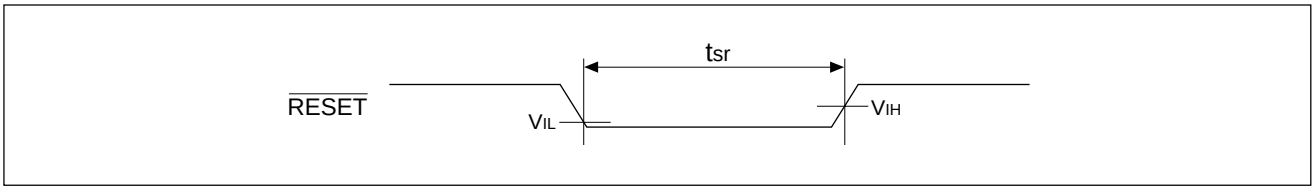
(Unless otherwise specified: V_{DD}=1.2 to 3.6V, V_{SS}=0V, Ta=-20 to 70°C)

Characteristic	Symbol	Condition		Min.	Typ.	Max.	Unit
Operating clock frequency	f_{OSC1}	OSC1 crystal oscillation		–	32.768	–	kHz
		OSC1 CR oscillation			60		kHz
	f_{OSC3}	OSC3 CR oscillation (Typ. 200kHz, built-in resistor)			200		kHz
		OSC3 CR oscillation (Typ. 1.8MHz, built-in resistor)			1,800		kHz
		OSC3 CR oscillation (Typ. 1.8MHz, external resistor)			1,800		kHz
		OSC3 ceramic oscillation				4,100	kHz
Instruction execution time	tcy	OSC1 crystal oscillation	1-cycle instruction	–	61.0	–	µS
			2-cycle instruction	–	122.1	–	µS
			3-cycle instruction	–	183.1	–	µS
		OSC1 CR oscillation	1-cycle instruction	25.0	33.3	50	µS
			2-cycle instruction	50.0	66.7	100	µS
			3-cycle instruction	75.0	100	150	µS
		OSC3 CR oscillation (built-in resistor)	1-cycle instruction		10		µS
			2-cycle instruction		20		µS
			3-cycle instruction		30		µS
		OSC3 CR oscillation (external resistor)	1-cycle instruction		1.1		µS
			2-cycle instruction		2.2		µS
			3-cycle instruction		3.3		µS
		OSC3 ceramic oscillation	1-cycle instruction	0.49			µS
			2-cycle instruction	0.98			µS
			3-cycle instruction	1.95			µS

$\overline{\text{RESET}}$ Input Clock (In the case of the special reset is selected by mask option)

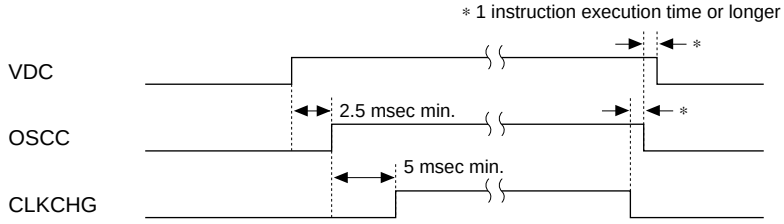
(Unless otherwise specified: V_{DD}=1.2 to 3.6V, V_{SS}=0V, Ta=-20 to 70°C, V_{IH}=0.5·V_{DD}, V_{IL}=0.1·V_{DD})

Characteristic	Symbol	Condition	Min.	Max.	Unit
$\overline{\text{RESET}}$ input time	tsr		1		mS



● Timing Chart

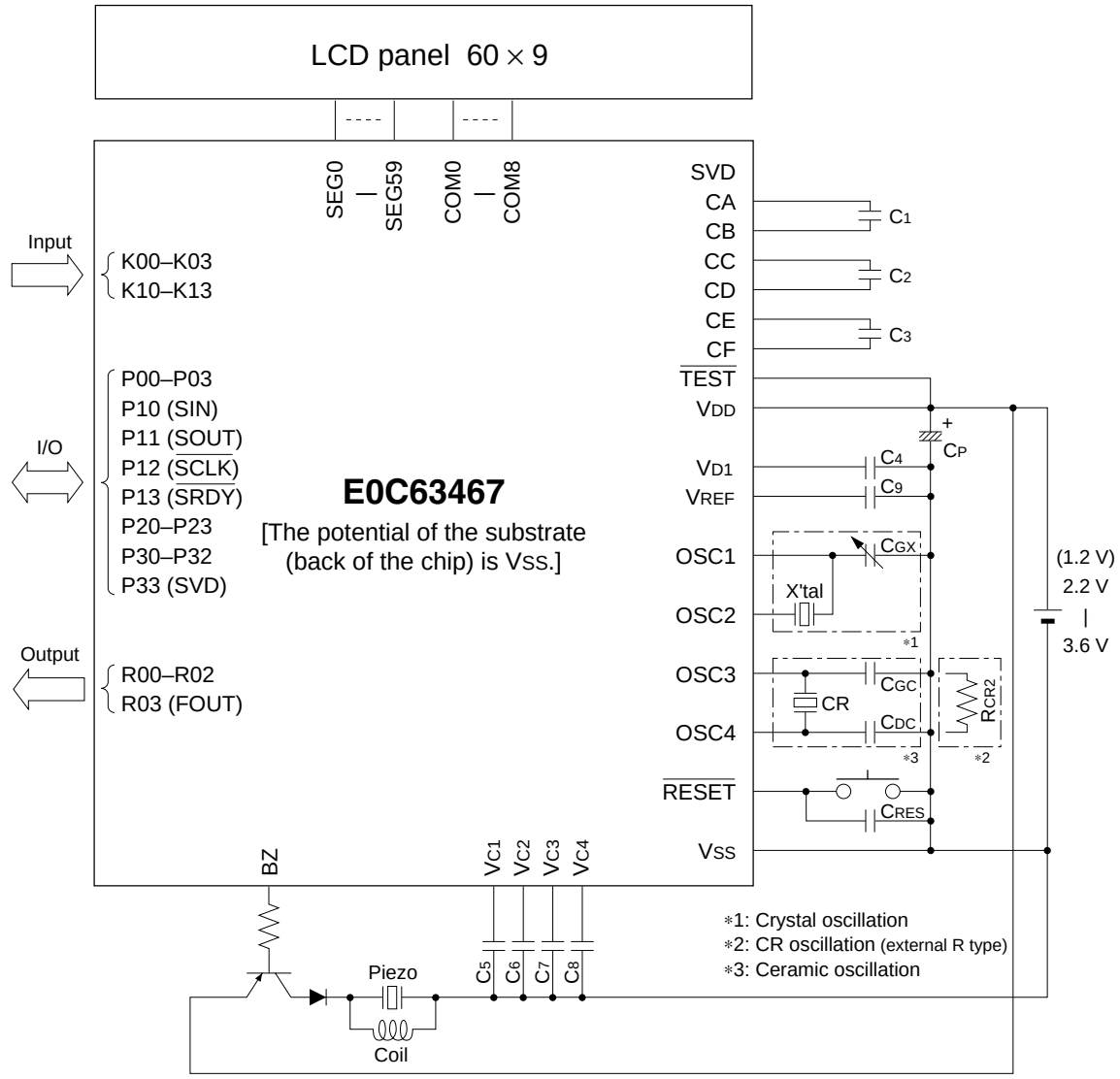
System clock switching



Note: When the OSC3 oscillation circuit has been selected as the 200-kHz CR oscillation circuit (built-in R type), it is not necessary to set the VDC register.

■ BASIC EXTERNAL CONNECTION DIAGRAM

• When negative polarity is selected for buzzer output (mask option selection)

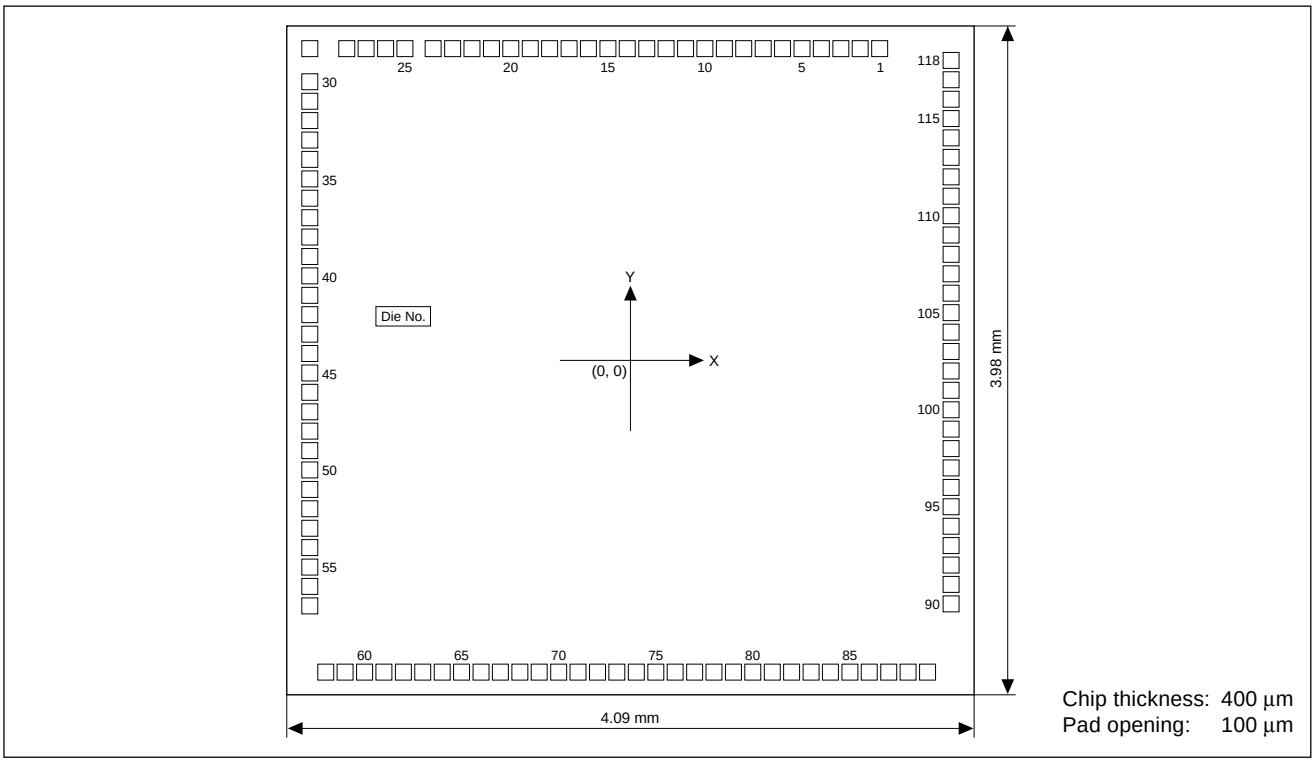


X'tal	Crystal oscillator	32.768 kHz, C_I (Max.) = 34 kΩ
C_{GX}	Trimmer capacitor	5–25 pF
CR	Ceramic oscillator	4 MHz (3.0 V)
C_{GC}	Gate capacitor	30 pF
C_{DC}	Drain capacitor	30 pF
R_{CR2}	Resistor for OSC3 CR oscillation	47 kΩ (1.8 MHz)
C_1–C_8	Capacitor	0.2 µF
C_9	Capacitor	0.1 µF
C_P	Capacitor	3.3 µF
C_{RES}	$\overline{\text{RESET}}$ terminal capacitor	0.1 µF

Notes:
- The above table is simply an example, and is not guaranteed to work.
- In order to prevent unstable operation of the OSC3 oscillation circuit due to current leak between OSC3 and V_{DD}, please keep enough distance between V_{DD} and other signals on the board pattern.
- In order to get a stable frequency for ceramic oscillation, please use maker's recommendatory value for C_{GC} and C_{DC}.

■ PAD LAYOUT

● Diagram of Pad Layout



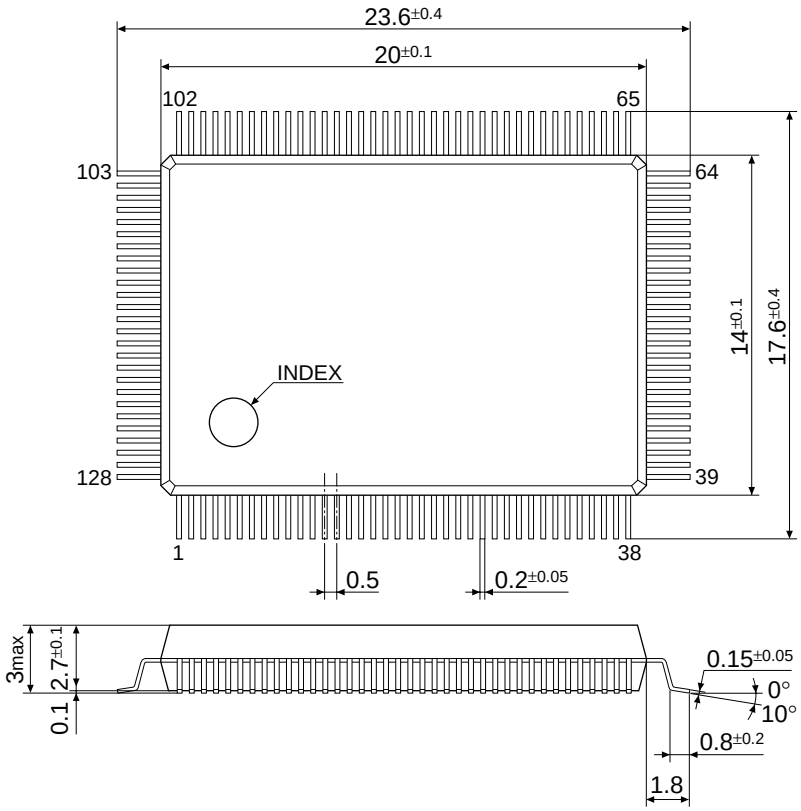
● Pad Coordinates

Unit: µm

No.	Pad name	X	Y	No.	Pad name	X	Y	No.	Pad name	X	Y	No.	Pad name	X	Y
1	P33	1,483	1,855	31	V_{C1}	-1,908	1,542	61	SEG20	-1,467	-1,855	91	SEG50	1,908	-1,333
2	P32	1,367	1,855	32	V_{C2}	-1,908	1,427	62	SEG21	-1,351	-1,855	92	SEG51	1,908	-1,218
3	P31	1,252	1,855	33	V_{C3}	-1,908	1,311	63	SEG22	-1,236	-1,855	93	SEG52	1,908	-1,102
4	P30	1,136	1,855	34	V_{C4}	-1,908	1,196	64	SEG23	-1,120	-1,855	94	SEG53	1,908	-987
5	P23	1,021	1,855	35	CA	-1,908	1,080	65	SEG24	-1,005	-1,855	95	SEG54	1,908	-871
6	P22	905	1,855	36	CB	-1,908	965	66	SEG25	-889	-1,855	96	SEG55	1,908	-756
7	P21	790	1,855	37	CC	-1,908	849	67	SEG26	-774	-1,855	97	SEG56	1,908	-640
8	P20	674	1,855	38	CD	-1,908	734	68	SEG27	-658	-1,855	98	SEG57	1,908	-525
9	P13	559	1,855	39	CE	-1,908	618	69	SEG28	-543	-1,855	99	SEG58	1,908	-409
10	P12	443	1,855	40	CF	-1,908	503	70	SEG29	-427	-1,855	100	SEG59	1,908	-294
11	P11	328	1,855	41	SEG0	-1,908	387	71	SEG30	-312	-1,855	101	COM8	1,908	-178
12	P10	212	1,855	42	SEG1	-1,908	272	72	SEG31	-196	-1,855	102	COM7	1,908	-63
13	P03	97	1,855	43	SEG2	-1,908	156	73	SEG32	-81	-1,855	103	COM6	1,908	53
14	P02	-19	1,855	44	SEG3	-1,908	41	74	SEG33	35	-1,855	104	COM5	1,908	168
15	P01	-134	1,855	45	SEG4	-1,908	-75	75	SEG34	151	-1,855	105	COM4	1,908	284
16	P00	-250	1,855	46	SEG5	-1,908	-190	76	SEG35	266	-1,855	106	COM3	1,908	400
17	R00	-365	1,855	47	SEG6	-1,908	-306	77	SEG36	382	-1,855	107	COM2	1,908	515
18	R01	-481	1,855	48	SEG7	-1,908	-421	78	SEG37	497	-1,855	108	COM1	1,908	631
19	R02	-596	1,855	49	SEG8	-1,908	-537	79	SEG38	613	-1,855	109	COM0	1,908	746
20	R03	-712	1,855	50	SEG9	-1,908	-652	80	SEG39	728	-1,855	110	V_{SS}	1,908	861
21	BZ	-827	1,855	51	SEG10	-1,908	-768	81	SEG40	844	-1,855	111	OSC1	1,908	977
22	K00	-943	1,855	52	SEG11	-1,908	-883	82	SEG41	959	-1,855	112	OSC2	1,908	1,092
23	K01	-1,058	1,855	53	SEG12	-1,908	-999	83	SEG42	1,075	-1,855	113	V_{D1}	1,908	1,208
24	K02	-1,174	1,855	54	SEG13	-1,908	-1,114	84	SEG43	1,190	-1,855	114	OSC3	1,908	1,324
25	K03	-1,342	1,855	55	SEG14	-1,908	-1,230	85	SEG44	1,306	-1,855	115	OSC4	1,908	1,439
26	K10	-1,457	1,855	56	SEG15	-1,908	-1,345	86	SEG45	1,421	-1,855	116	V_{DD}	1,908	1,554
27	K11	-1,573	1,855	57	SEG16	-1,908	-1,461	87	SEG46	1,537	-1,855	117	$\overline{TEST}$	1,908	1,670
28	K12	-1,688	1,855	58	SEG17	-1,813	-1,855	88	SEG47	1,652	-1,855	118	$\overline{RESET}$	1,908	1,785
29	K13	-1,908	1,855	59	SEG18	-1,698	-1,855	89	SEG48	1,768	-1,855	–			
30	V_{REF}	-1,908	1,658	60	SEG19	-1,582	-1,855	90	SEG49	1,908	-1,449	–			

■ PACKAGE DIMENSIONS

Plastic QFP5-128pin



Unit: mm

THIS PAGE IS BLANK.

SEIKO EPSON CORPORATION
ELECTRONIC DEVICES MARKETING DIVISION
IC Marketing & Engineering Group

ED International Marketing Department Europe & U.S.A.
421-8, Hino, Hino-shi, Tokyo 191-8501, JAPAN
Phone : 042-587-5812 FAX : 042-587-5564

ED International Marketing Department Asia
421-8, Hino, Hino-shi, Tokyo 191-8501, JAPAN
Phone : 042-587-5814 FAX : 042-587-5110

■ EPSON Electronic Devices Website
http://www.epson.co.jp/device/

Issue MAY 2000, Printed in Japan Ⓜ