EPSON

E0C63557

4-bit Single Chip Microcomputer

Low Voltage Operation Products

- 4-bit E0C63000 Core CPU
- Built-in Dot-matrix LCD Driver
- Low Voltage Operation (2.2V Min.)
- High Speed Instruction Cycle (2-6CPI)

■ DESCRIPTION

The E0C63557 is a CMOS 4-bit microcomputer composed of a CMOS 4-bit core CPU, ROM, RAM, dot-matrix type LCD driver and counters. And the E0C63557 can be operated with high speed and spend little current. The E0C63557 has large RAM and LCD driver, so that the E0C63557 is best suited for systems such as Caller ID and Data-bank.

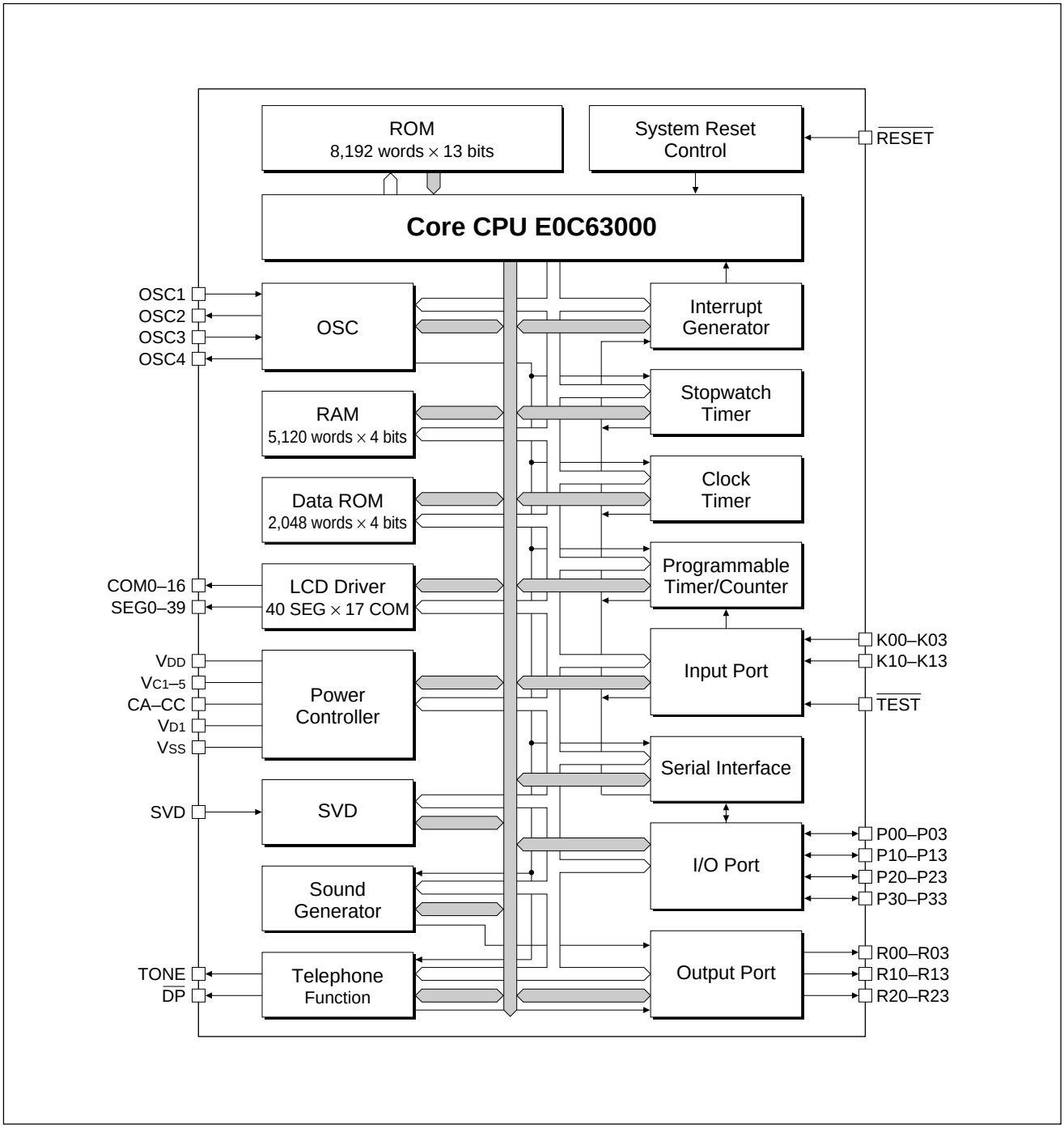
■ FEATURES

- CMOS LSI 4-bit parallel processing ..... E0C63000 core CPU
- Main clock ..... 32.768kHz (X'tal)
- Sub clock ..... 3.58MHz (Typ. / Ceramic OSC)
- Instruction set ..... 46 types (411 instructions with all)
- Instruction execution time ..... 32kHz : 61µsec (Min.)
  3.58MHz : 0.56µsec (Min.)
- ROM capacity ..... ROM : 8,192 words × 13 bits
  Data ROM : 2,048 words × 4 bits
- RAM capacity ..... Data RAM : 5,120 words × 4 bits
  Display RAM : 680 bits
- I/O port ..... I : 8 bits (Pull-up resistors may be supplemented ∗1)
  O : 12 bits (It is possible to switch the 8 bits to special output)
  I/O : 16 bits (It is possible to switch the 2 bits to special output and the 4 bits to serial I/F input/output)
- LCD driver ..... 40 segments × 8 / 16 / 17 commons
  (LCD drive voltage internally, cannot use external voltage)
- Clock timer ..... 1 ch.
- Stopwatch timer ..... 1 ch.
- Programmable timer ..... 8 bits × 2 ch., with event counter function
- Watchdog timer ..... Built-in
- Serial interface ..... 1 ch. (It is possible to switch synchronous/asynchronous)
- Sound generator ..... With envelope and 1-shot output functions
  (It is possible to switch the output port)
- DTMF/DP generator ..... DTMF (Dual Tone Multi-Frequency) generator built-in
  DP (Dialing Pulse) generator built-in
  Pause/Flash/Hold line/Mute control/Handfree
  Hook switch control built-in
  (It is possible to switch the output port)
- Interrupts ..... External : Kye interrupt 1 system
  Internal : Clock timer interrupt 4 systems
  : Stopwatch timer interrupt 2 systems
  : Programmable timer interrupt 2 systems
  : Serial interface interrupt 2 systems
  : DTMF interrupt 1 system

- Power supply voltage ..... 2.2 to 5.5V
- Operating temperature range ..... -20°C to 70°C
- Pad pitch 115µm
- Current consumption ..... 1.5µA (32.768kHz, LCD OFF, 3.0V, HALT)
  10µA (32.768kHz, LCD ON, 3.0V, RUN)
  1000µA (3.58MHz, LCD ON, 3.0V, RUN)
- Package ..... QFP15-128pin, Die form

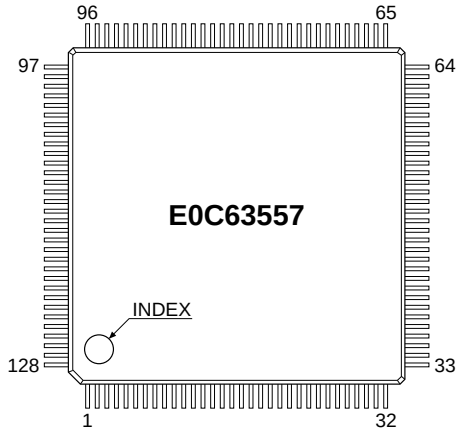
∗1: Can be selected with mask option

■ BLOCK DIAGRAM



■ PIN CONFIGURATION

QFP15-128pin



No.	Pin name	No.	Pin name	No.	Pin name	No.	Pin name
1	N.C.	33	N.C.	65	N.C.	97	N.C.
2	SEG34	34	N.C.	66	R21	98	N.C.
3	SEG33	35	N.C.	67	R20	99	N.C.
4	SEG32	36	SEG4	68	R13	100	K03
5	SEG31	37	SEG3	69	R12	101	K02
6	SEG30	38	SEG2	70	R11	102	K01
7	SEG29	39	SEG1	71	R10	103	K00
8	SEG28	40	SEG0	72	R03	104	SVD
9	SEG27	41	COM7	73	R02	105	V_{C1}
10	SEG26	42	COM6	74	R01	106	V_{C23}
11	SEG25	43	COM5	75	R00	107	V_{C4}
12	SEG24	44	COM4	76	P33	108	V_{C5}
13	SEG23	45	COM3	77	P32	109	CC
14	SEG22	46	COM2	78	P31	110	CB
15	SEG21	47	COM1	79	P30	111	CA
16	SEG20	48	COM0	80	P23	112	COM8
17	SEG19	49	V_{SS}	81	P22	113	COM9
18	SEG18	50	OSC1	82	P21	114	COM10
19	SEG17	51	OSC2	83	P20	115	COM11
20	SEG16	52	V_{D1}	84	P13	116	COM12
21	SEG15	53	OSC3	85	P12	117	COM13
22	SEG14	54	OSC4	86	P11	118	COM14
23	SEG13	55	V_{DD}	87	P10	119	COM15
24	SEG12	56	$\overline{RESET}$	88	P03	120	COM16
25	SEG11	57	$\overline{TEST}$	89	P02	121	SEG39
26	SEG10	58	TONE	90	P01	122	SEG38
27	SEG9	59	$\overline{DP}$	91	P00	123	SEG37
28	SEG8	60	R23	92	K13	124	SEG36
29	SEG7	61	R22	93	K12	125	SEG35
30	SEG6	62	N.C.	94	K11	126	N.C.
31	SEG5	63	N.C.	95	K10	127	N.C.
32	N.C.	64	N.C.	96	N.C.	128	N.C.

N.C. : No Connection

■ PIN DESCRIPTION

Pin name	Pin No.	In/Out	Function
V_{DD}	55	–	Power (+) supply pin
V_{SS}	49	–	Power (–) supply pin
V_{D1}	52	–	Oscillation system regulated voltage output pin
V_{C1}–V_{C5}	105–108	–	LCD system power supply pin (1/4 bias generated internally)
CA–CC	111–109	–	LCD system boosting/reducing capacitor connecting pin
OSC1	50	I	Crystal oscillation input pin
OSC2	51	O	Crystal oscillation output pin
OSC3	53	I	Ceramic oscillation input pin
OSC4	54	O	Ceramic oscillation output pin
K00–K03	103–100	I	Input port
K10–K13	95–92	I	Input port
P00–P03	91–88	I/O	I/O port
P10–P13	87–84	I/O	I/O port (switching to serial I/F input/output is possible by software)
P20	83	I/O	I/O port
P21	82	I/O	I/O port
P22	81	I/O	I/O port (switching to CL signal output is possible by software)
P23	80	I/O	I/O port (switching to FR signal output is possible by software)
P30–P33	79–76	I/O	I/O port
R00	75	O	Output port (switching to XBZ signal output is possible by software)
R01	74	O	Output port (switching to BZ signal output is possible by software)
R02	73	O	Output port (switching to TOUT signal output is possible by software)
R03	72	O	Output port (switching to FOUT signal output is possible by software)
R10	71	O	Output port (switching to XTMUTE signal output is possible by software)
R11	70	O	Output port (switching to XRMUTE signal output is possible by software)
R12	69	O	Output port (switching to HDO signal output is possible by software)
R13	68	O	Output port (switching to HFO signal output is possible by software)
R20–R23	67, 66, 61, 60	O	Output port
COM0–COM16	48–41, 112–120	O	LCD common output pin (1/8, 1/16, 1/17 duty can be selected by software)
SEG0–SEG39	40–36, 31–2, 125–121	O	LCD segment output pin
SVD	104	I	SVD external voltage input pin
$\overline{DP}$	59	O	Dial pulse output pin
TONE	58	O	DTMF output pin
$\overline{RESET}$	56	I	Initial reset input pin
$\overline{TEST}$	57	I	Testing input pin

■ ELECTRICAL CHARACTERISTICS

● Absolute Maximum Ratings

(VSS=0V)

Rating	Symbol	Value	Unit
Supply voltage	V_{DD}	-0.5 to 7.0	V
Input voltage (1)	V_I	-0.5 to V_{DD} + 0.3	V
Input voltage (2)	V_{IOSC}	-0.5 to V_{D1} + 0.3	V
Permissible total output current *1	ΣI_{VDD}	10	mA
Operating temperature	Topr	-20 to 70	°C
Storage temperature	Tstg	-65 to 150	°C
Soldering temperature / time	Tsol	260°C, 10sec (lead section)	–
Permissible dissipation *2	P_D	250	mW

*1: The permissible total output current is the sum total of the current (average current) that simultaneously flows from the output pins (or is draw in).
*2: In case of plastic package (QFP15-128pin).

● Recommended Operating Conditions

(Ta=-20 to 70°C)

Condition	Symbol	Remark		Min.	Typ.	Max.	Unit
Supply voltage	V_{DD}	VSS=0V	OSC3 oscillation OFF	2.2	3.0	5.5	V
			OSC3 oscillation ON	2.2	3.0	5.5	V
Oscillation frequency	f_{OSC1}	Crystal oscillation		–	32.768	–	kHz
	f_{OSC3}	Ceramic oscillation		–	3.58	–	MHz
SVD terminal input voltage	SVD	VSS=0V, SVD≤V_{DD}		0		5.5	V

● DC Characteristics

(Unless otherwise specified: V_{DD}=3.0V, V_{SS}=0V, f_{OSC1}=32.768kHz, Ta=-20 to 70°C, V_{D1}/V_{C1}/V_{C23}/V_{C4}/V_{C5} are internal voltage, C_1–C_7=0.2µF)

Characteristic	Symbol	Condition		Min.	Typ.	Max.	Unit
High level input voltage (1)	V_{IH1}		K00–03, K10–13 P00–03, P10–13, P20–23, P30–33	0.8·V_{DD}		V_{DD}	V
High level input voltage (2)	V_{IH2}		$\overline{RESET}$, $\overline{TEST}$	0.9·V_{DD}		V_{DD}	V
Low level input voltage (1)	V_{IL1}		K00–03, K10–13	0		0.2·V_{DD}	V
Low level input voltage (2)	V_{IL2}		P00–03, P10–13, P20–23, P30–33	0		0.4	V
Low level input voltage (3)	V_{IL3}		$\overline{RESET}$, $\overline{TEST}$	0		0.1·V_{DD}	V
High level input current	I_{IH}	V_{IH}=3.0V	K00–03, K10–13 P00–03, P10–13, P20–23, P30–33 $\overline{RESET}$, $\overline{TEST}$	0		0.5	µA
Low level input current (1)	I_{IL1}	V_{IL1}=V_{SS} No Pull-up	K00–03, K10–13 P00–03, P10–13, P20–23, P30–33 $\overline{RESET}$, $\overline{TEST}$	-0.5		0	µA
Low level input current (2)	I_{IL2}	V_{IL2}=V_{SS} With Pull-up	K00–03, K10–13 P00–03, P10–13, P20–23, P30–33 $\overline{RESET}$, $\overline{TEST}$	-16	-10	-6	µA
High level output current (1)	I_{OH1}	V_{OH1}=0.9·V_{DD}	R02, R03, R10–13, R20–23 P00–03, P10–13, P20–23, P30–33			-0.6	mA
High level output current (2)	I_{OH2}	V_{OH2}=0.9·V_{DD}	R00, R01			-0.6	mA
Low level output current (1)	I_{OL1}	V_{OL1}=0.1·V_{DD}	R02, R03, R10–13, R20–23 P00–03, P10–13, P20–23, P30–33	1.5			mA
Low level output current (2)	I_{OL2}	V_{OL2}=0.1·V_{DD}	R00, R01	1.5			mA
Common output current	I_{OH3}	V_{OH3}=V_{C5}-0.05V	COM0–16			-25	µA
	I_{OL3}	V_{OL3}=V_{SS}+0.05V		25			µA
Segment output current	I_{OH4}	V_{OH4}=V_{C5}-0.05V	SEG0–39			-10	µA
	I_{OL4}	V_{OL4}=V_{SS}+0.05V		10			µA

(Unless otherwise specified: V_{DD}=5.0V, V_{SS}=0V, f_{OSC1}=32.768kHz, Ta=-20 to 70°C, V_{D1}/V_{C1}/V_{C23}/V_{C4}/V_{C5} are internal voltage, C_1–C_7=0.2µF)

Characteristic	Symbol	Condition		Min.	Typ.	Max.	Unit
High level input voltage (1)	V_{IH1}		K00–03, K10–13 P00–03, P10–13, P20–23, P30–33	0.8·V_{DD}		V_{DD}	V
High level input voltage (2)	V_{IH2}		$\overline{RESET}$, $\overline{TEST}$	0.9·V_{DD}		V_{DD}	V
Low level input voltage (1)	V_{IL1}		K00–03, K10–13	0		0.2·V_{DD}	V
Low level input voltage (2)	V_{IL2}		P00–03, P10–13, P20–23, P30–33	0		0.4	V
Low level input voltage (3)	V_{IL3}		$\overline{RESET}$, $\overline{TEST}$	0		0.1·V_{DD}	V
High level input current	I_{IH}	V_{IH}=5.0V	K00–03, K10–13 P00–03, P10–13, P20–23, P30–33 $\overline{RESET}$, $\overline{TEST}$	0		0.5	µA
Low level input current (1)	I_{IL1}	V_{IL1}=V_{SS} No Pull-up	K00–03, K10–13 P00–03, P10–13, P20–23, P30–33 $\overline{RESET}$, $\overline{TEST}$	-0.5		0	µA
Low level input current (2)	I_{IL2}	V_{IL2}=V_{SS} With Pull-up	K00–03, K10–13 P00–03, P10–13, P20–23, P30–33 $\overline{RESET}$, $\overline{TEST}$	-25	-15	-10	µA
High level output current (1)	I_{OH1}	V_{OH1}=0.9·V_{DD}	R02, R03, R10–13, R20–23 P00–03, P10–13, P20–23, P30–33			-1.5	mA
High level output current (2)	I_{OH2}	V_{OH2}=0.9·V_{DD}	R00, R01			-1.5	mA
Low level output current (1)	I_{OL1}	V_{OL1}=0.1·V_{DD}	R02, R03, R10–13, R20–23 P00–03, P10–13, P20–23, P30–33	3.5			mA
Low level output current (2)	I_{OL2}	V_{OL2}=0.1·V_{DD}	R00, R01	3.5			mA
Common output current	I_{OH3}	V_{OH3}=V_{C5}-0.05V	COM0–16			-25	µA
	I_{OL3}	V_{OL3}=V_{SS}+0.05V		25			µA
Segment output current	I_{OH4}	V_{OH4}=V_{C5}-0.05V	SEG0–39			-10	µA
	I_{OL4}	V_{OL4}=V_{SS}+0.05V		10			µA

● Analog Circuit Characteristics and Current Consumption

(Unless otherwise specified: V_{DD}=3.0V, V_{SS}=0V, f_{OSC1}=32.768kHz, C_G=25pF, Ta=-20 to 70°C, V_{D1}/V_{C1}/V_{C23}/V_{C4}/V_{C5} are internal voltage, C_1–C_7=0.2µF)

Characteristic	Symbol	Condition		Min.	Typ.	Max.	Unit
LCD drive voltage	V_{C1}	Connect 1 MΩ load resistor between V_{SS} and V_{C1} (without panel load)		1/2·V_{C23} -0.1		1/2·V_{C23} ×0.95	V
	V_{C23}	Connect 1 MΩ load resistor between V_{SS} and V_{C23} (without panel load)	LC0–3="0"	Typ. ×0.88	1.95	Typ. ×1.12	V
			LC0–3="1"		1.98		
			LC0–3="2"		2.01		
			LC0–3="3"		2.04		
			LC0–3="4"		2.07		
			LC0–3="5"		2.10		
			LC0–3="6"		2.13		
			LC0–3="7"		2.16		
			LC0–3="8"		2.19		
			LC0–3="9"		2.22		
			LC0–3="10"		2.25		
			LC0–3="11"		2.28		
			LC0–3="12"		2.31		
			LC0–3="13"		2.34		
			LC0–3="14"		2.37		
			LC0–3="15"		2.40		
	V_{C4}	Connect 1 MΩ load resistor between V_{SS} and V_{C4} (without panel load)		3/2·V_{C23} ×0.95		3/2·V_{C23}	V
	V_{C5}	Connect 1 MΩ load resistor between V_{SS} and V_{C5} (without panel load)		2·V_{C23} ×0.95		2·V_{C23}	V
SVD voltage (Ta=25°C)	V_{SVD1}	SVDS0–3="0" (internal)		Typ. ×0.93	2.20	Typ. ×1.07	V
		SVDS0–3="1"			2.20		
		SVDS0–3="2"			2.20		
		SVDS0–3="3"			2.20		
		SVDS0–3="4"			2.20		
		SVDS0–3="5"			2.30		
		SVDS0–3="6"			2.40		
		SVDS0–3="7"			2.50		
		SVDS0–3="8"			2.60		
		SVDS0–3="9"			2.70		
		SVDS0–3="10"			2.80		
		SVDS0–3="11"			2.90		
		SVDS0–3="12"			3.00		
		SVDS0–3="13"			3.10		
		SVDS0–3="14"			3.20		
		SVDS0–3="15"			3.30		
SVD voltage (external) *3	V_{SVD2}	SVDS0–3="0" (external), Ta = 25°C		0.95	1.05	1.15	V
SVD circuit response time	t_{SVD}	Ta = 25°C				100	µS
Current consumption (Ta=25°C)	I_{OP}	During HALT (32 kHz crystal oscillation)	LCD power OFF *1, *2		1.5	3	µA
			LCD power ON *1, *2		4	8	µA
		During execution (32 kHz crystal oscillation)	LCD power ON *1, *2		10	19	µA
		During execution (3.58 MHz ceramic oscillation)	LCD power ON *1		1,000	1,200	µA
		SVD circuit current (during supply voltage detection) V_{DD}=2.2 to 5.5 V		1		15	µA
		SVD circuit current (during external voltage detection) V_{DD}=2.2 to 5.5 V		0.5		6	µA

*1: Without panel load. The SVD circuit is OFF.

*2: OSCC = "0"

*3: Please input the voltage, which is within the range between V_{SS} and V_{DD}, into the SVD terminal.

● Oscillation Characteristics

The oscillation characteristics change depending on the conditions (components used, board pattern, etc.). Use the following characteristics as reference values.

OSC1 Crystal Oscillation Circuit

(Unless otherwise specified: V_{DD}=3.0V, V_{SS}=0V, f_{OSC1}=32.768kHz, C_G=25pF, C_D=built-in, Ta=-20 to 70°C)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start voltage	Vsta	tsta≤3sec (V_{DD})	2.2			V
Oscillation stop voltage	Vstp	tstp≤10sec (V_{DD})	2.2			V
Built-in capacitance (drain)	C_D	Including the parasitic capacitance inside the IC (in chip)		14		pF
Frequency/voltage deviation	Δf/ΔV	V_{DD}=2.2 to 5.5V			10	ppm
Frequency/IC deviation	Δf/ΔIC		-10		10	ppm
Frequency adjustment range	Δf/ΔC_G	C_G=5 to 25pF	10	20		ppm
Harmonic oscillation start voltage	V_{hho}	C_G=5pF (V_{DD})	5.5			V
Permitted leak resistance	R_{leak}	Between OSC1 and V_{SS}	200			MΩ

OSC3 Ceramic Oscillation Circuit

(Unless otherwise specified: V_{DD}=3.0V, V_{SS}=0V, Ceramic oscillator: 3.58MHz, C_{GC}=C_{DC}=30pF, Ta=-20 to 70°C)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start voltage	Vsta	(V_{DD})	2.2			V
Oscillation start time	tsta	V_{DD}=2.2 to 5.5V			5	mS
Oscillation stop voltage	Vstp	(V_{DD})	2.2			V

● Serial Interface AC Characteristics

Clock Synchronous Master Mode

• During 32 kHz operation

(Condition: V_{DD}=3.0V, V_{SS}=0V, Ta=25°C, V_{IH1}=0.8V_{DD}, V_{IL1}=0.2V_{DD}, V_{OH}=0.8V_{DD}, V_{OL}=0.2V_{DD})

Characteristic	Symbol	Min.	Typ.	Max.	Unit
Transmitting data output delay time	tsmd			5	µS
Receiving data input set-up time	tsms	10			µS
Receiving data input hold time	tsmh	5			µS

• During 1 MHz operation

(Condition: V_{DD}=3.0V, V_{SS}=0V, Ta=25°C, V_{IH1}=0.8V_{DD}, V_{IL1}=0.2V_{DD}, V_{OH}=0.8V_{DD}, V_{OL}=0.2V_{DD})

Characteristic	Symbol	Min.	Typ.	Max.	Unit
Transmitting data output delay time	tsmd			200	nS
Receiving data input set-up time	tsms	400			nS
Receiving data input hold time	tsmh	200			nS

Clock Synchronous Slave Mode

• During 32 kHz operation

(Condition: V_{DD}=3.0V, V_{SS}=0V, Ta=25°C, V_{IH1}=0.8V_{DD}, V_{IL1}=0.2V_{DD}, V_{OH}=0.8V_{DD}, V_{OL}=0.2V_{DD})

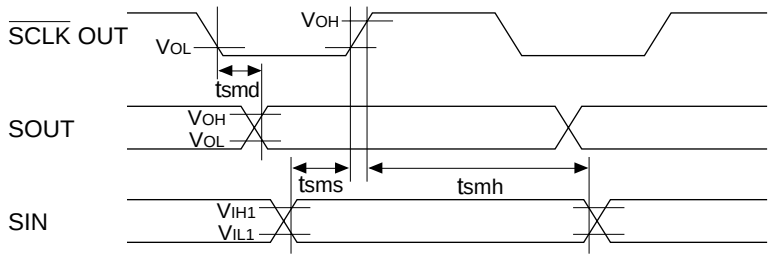
Characteristic	Symbol	Min.	Typ.	Max.	Unit
Transmitting data output delay time	tssd			10	µS
Receiving data input set-up time	tsss	10			µS
Receiving data input hold time	tssh	5			µS

• During 1 MHz operation

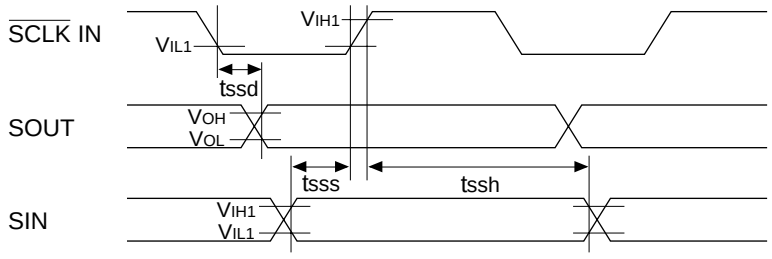
(Condition: V_{DD}=3.0V, V_{SS}=0V, Ta=25°C, V_{IH1}=0.8V_{DD}, V_{IL1}=0.2V_{DD}, V_{OH}=0.8V_{DD}, V_{OL}=0.2V_{DD})

Characteristic	Symbol	Min.	Typ.	Max.	Unit
Transmitting data output delay time	tssd			500	nS
Receiving data input set-up time	tsss	400			nS
Receiving data input hold time	tssh	200			nS

<Master mode>



<Slave mode>



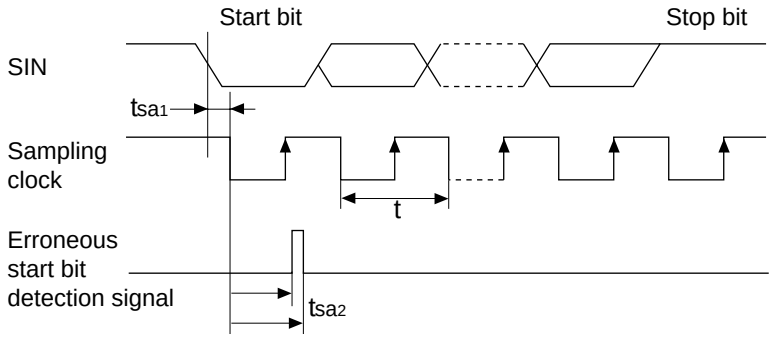
Asynchronous System

(Condition: V_{DD}=2.2 to 5.5V, V_{SS}=0V, Ta=-20 to 70°C)

Characteristic	Symbol	Min.	Typ.	Max.	Unit
Start bit detection error time *1	t_{sa1}	0		t/16	S
Erroneous start bit detection range time *2	t_{sa2}	9t/16		10t/16	S

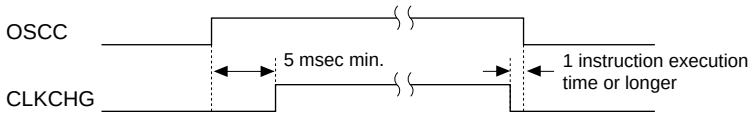
*1: Start bit detection error time is a logical delay time from inputting the start bit until internal sampling begins operating. (Time as far as AC is excluded.)

*2: Erroneous start bit detection range time is a logical range to detect whether a LOW level (start bit) has been input again after a start bit has been detected and the internal sampling clock has started. When a HIGH level is detected, the start bit detection circuit is reset and goes into a wait status until the next start bit. (Time as far as AC is excluded.)

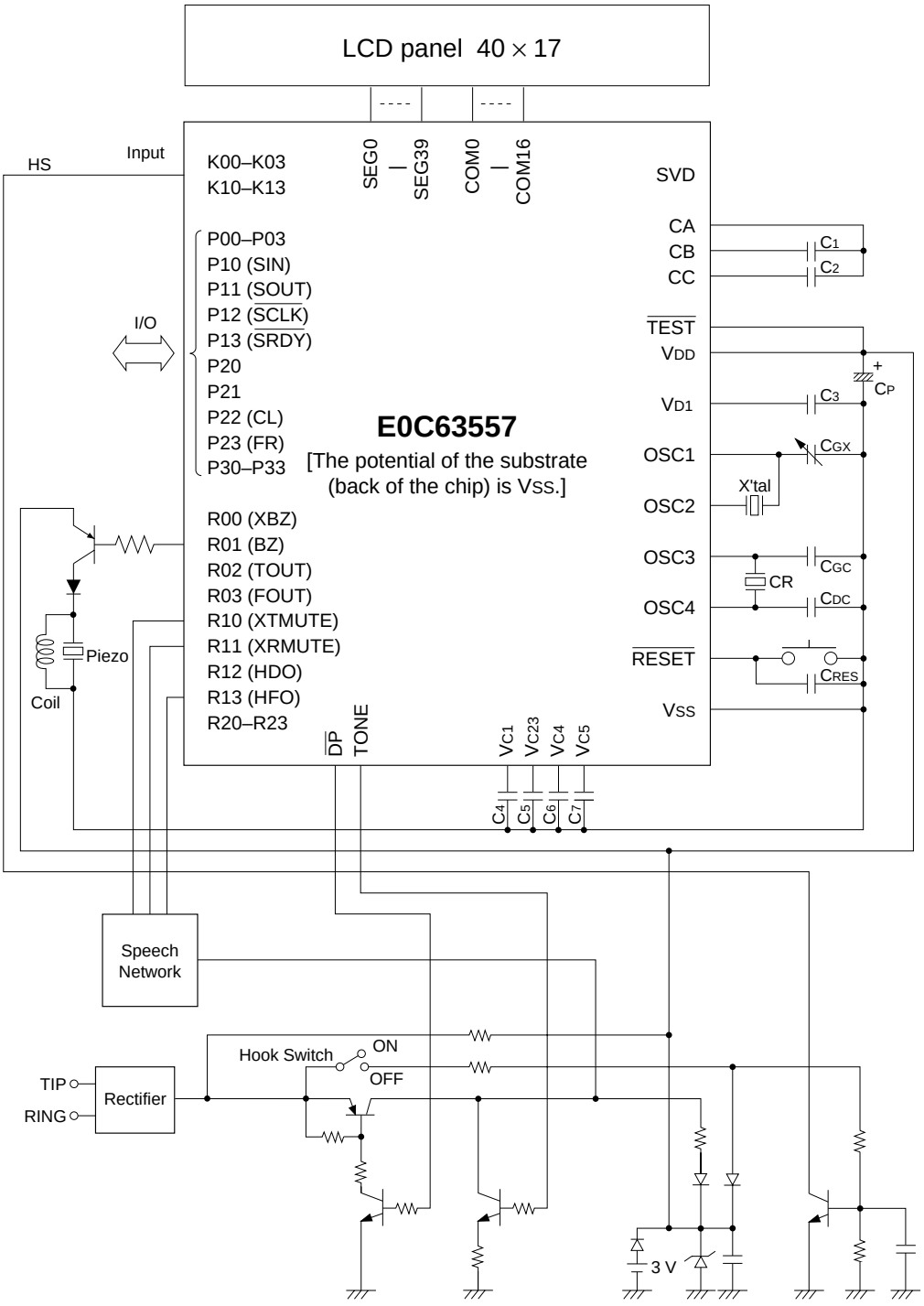


● Timing Chart

System clock switching



■ BASIC EXTERNAL CONNECTION DIAGRAM



X'tal	Crystal oscillator	32.768 kHz, CI(Max.) = 34 kΩ
CGX	Trimmer capacitor	5–25 pF
CR	Ceramic oscillator	3.58 MHz (3.0 V)
CGC	Gate capacitor	30 pF
CDC	Drain capacitor	30 pF
C1–C7	Capacitor	0.2 µF
CP	Capacitor	3.3 µF
CRES	RESET terminal capacitor	0.1 µF

Note: The above table is simply an example, and is not guaranteed to work.

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