EPSON

E0C63B07

4-bit Single Chip Microcomputer

Low Voltage Operation Products

- 4-bit Low Cycle / Inst. Core CPU
- Built-in 7 Segment Type LCD Driver
- Low Voltage Operation (0.9V Min.)
- Built-in Gate Array

■ DESCRIPTION

The E0C63B07 is a CMOS 4-bit microcomputer composed of a CMOS 4-bit core CPU, ROM, RAM, 7 segment type LCD driver, 10000 gates of gate array and counters. And the E0C63B07 can be operated by single Manganese battery with LCD display. So that tha E0C63B07 is best suited for systems such as numeric pager.

■ FEATURES

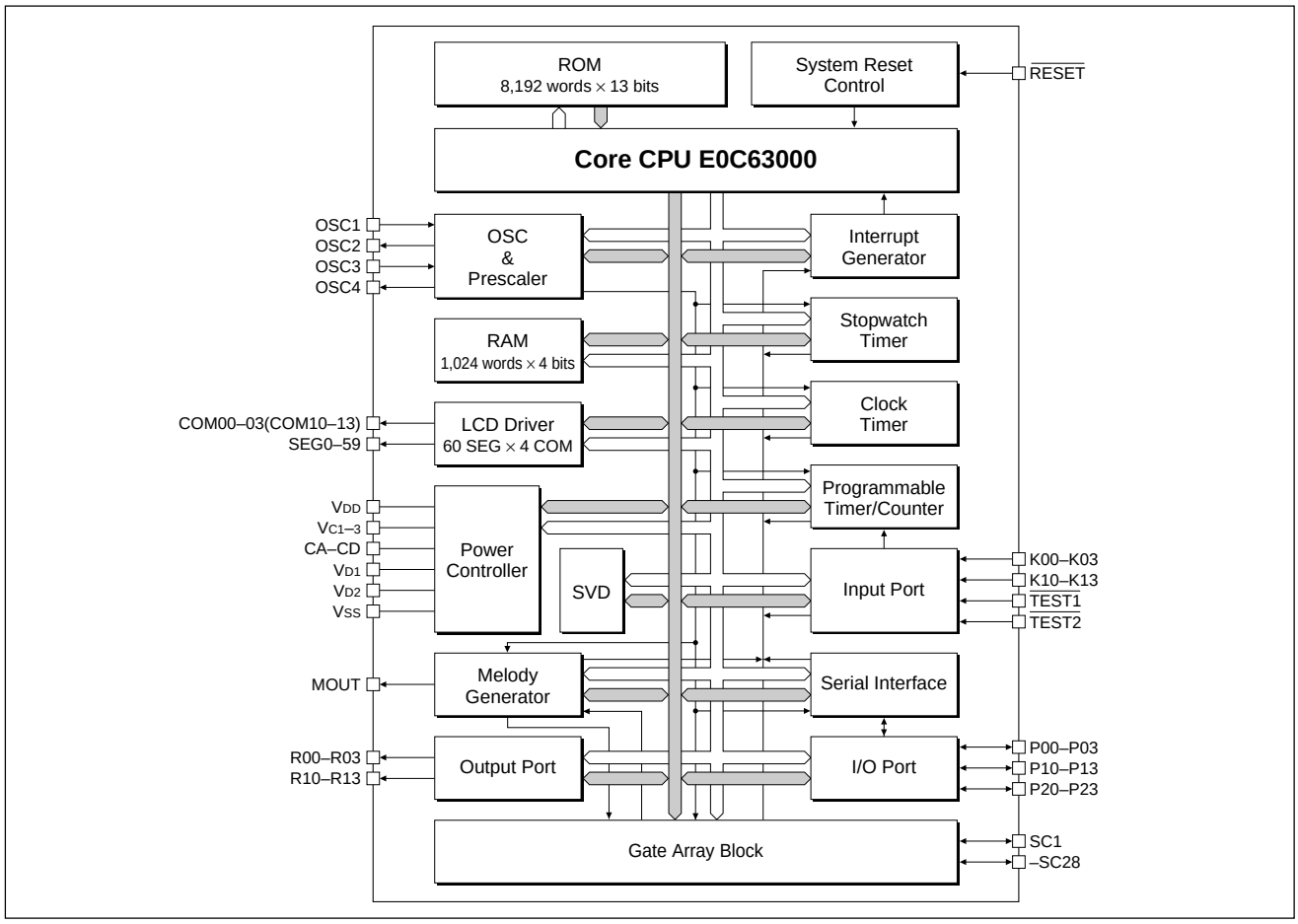
- CMOS LSI 4-bit parallel processing
- OSC1 oscillation circuit ..... 32.768/76.8/153.6kHz (Typ.) Crystal oscillation circuit (∗1)
- OSC3 oscillation circuit ..... 400kHz (Max.) CR oscillation circuit, Operatable in 0.9V
- Instruction set ..... Basic instruction : 46 types (411 instructions with all)
  Addressing mode : 8 types
- Instruction execution time ..... During operation at 32.768kHz : 61µsec 122µsec 183µsec
  During operation at 76.8kHz : 26µsec 52µsec 78µsec
  During operation at 153.6kHz : 13µsec 26µsec 39µsec
  During operation at 400kHz : 5µsec 10µsec 15µsec
- ROM capacity ..... Code ROM: 8,192 words × 13 bits
- RAM capacity ..... Data memory : 1,024 words × 4 bits
  Display memory : 60 words × 4 bits
- Input port ..... 8 bits (Pull-up resistors may be supplemented ∗1)
- Output port ..... 8 bits (It is possible to switch the 2 bits to special output ∗2)
- I/O port ..... 12 bits (It is possible to switch the 4 bits to serial input/output *2)
- Serial interface ..... 1 port (8-bit clock synchronous system)
- LCD driver ..... 60 segments × 4, 3 or 2 commons (∗2) 1/3 or 1/2 bias drive (∗1)
- Time base counter ..... 2 systems (Clock timer, stopwatch timer)
- Programmable timer ..... Built-in, 2 inputs × 8 bits, with event counter function
- Watchdog timer ..... Built-in
- Gate array ..... SOG : 10,000 gates
  Number of terminals : 28 bits
  CPU interface : Bus interface
- Melody generator ..... Equivalent to SVM7100M Series
  Maximum 16 melodies
  Melody ROM capacity : 495 words
  (words can be optionally arranged for each melody)
  Address control ROM : 80 words
  (words can be optionally arranged for each melody)
  Play output waveform : Single sound square wave
- Supply voltage detection (SVD) circuit .. 16 values, programmable (1.05V to 2.60V)
- External interrupt ..... Input port interrupt : 2 systems

- Internal interrupt ..... Clock timer interrupt : 4 systems
  Stopwatch timer interrupt : 2 systems
  Programmable timer interrupt : 2 systems
  Serial interface interrupt : 1 system
  Gate array interrupt : 4 systems
  Melody interrupt : 1 system
- Power supply voltage ..... 0.9V to 3.6V
- Operating temperature range ..... -20°C to 70°C
- Current consumption (Typ.) ..... Single clock:
  During HALT (32kHz)
  1.5V (normal mode, LCD power OFF) 1.2µA
  1.5V (normal mode, LCD power ON) 2.0µA
  3.0V (halver mode, LCD power ON) 1.5µA
  During operation (32kHz)
  1.5V (normal mode, LCD power ON) 6.0µA
  3.0V (halver mode, LCD power ON) 3.5µA
  Twin clock:
  During operation (400kHz)
  3.0V (normal mode, LCD power ON) 85µA

Package ..... QFP8-160pin (plastic) or chip

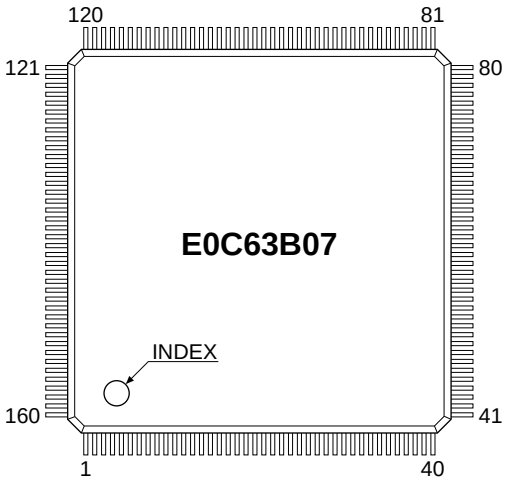
∗1: Can be selected with mask option ∗2: Can be selected with software

■ BLOCK DIAGRAM



■ PIN CONFIGURATION

QFP8-160pin



No.	Name	No.	Name	No.	Name	No.	Name
1	K10	41	P03	81	R01	121	N.C.
2	N.C.	42	P02	82	R02	122	N.C.
3	K03	43	P01	83	R03	123	N.C.
4	K02	44	P00	84	R10	124	SEG29
5	K01	45	COM13	85	R11	125	SEG28
6	K00	46	COM12	86	R12	126	SEG27
7	N.C.	47	COM11	87	R13	127	SEG26
8	N.C.	48	COM10	88	SC1	128	SEG25
9	N.C.	49	SEG30	89	SC2	129	SEG24
10	N.C.	50	SEG31	90	SC3	130	SEG23
11	N.C.	51	SEG32	91	SC4	131	SEG22
12	CA	52	SEG33	92	SC5	132	SEG21
13	CB	53	SEG34	93	SC6	133	SEG20
14	CC	54	SEG35	94	SC7	134	SEG19
15	CD	55	SEG36	95	SC8	135	SEG18
16	V_{C3}	56	SEG37	96	SC9	136	SEG17
17	V_{C2}	57	SEG38	97	SC10	137	SEG16
18	V_{C1}	58	SEG39	98	SC11	138	SEG15
19	V_{D2}	59	SEG40	99	SC12	139	SEG14
20	V_{SS}	60	SEG41	100	SC13	140	SEG13
21	OSC1	61	SEG42	101	SC14	141	SEG12
22	OSC2	62	SEG43	102	SC15	142	SEG11
23	V_{D1}	63	SEG44	103	SC16	143	SEG10
24	OSC3	64	SEG45	104	SC17	144	SEG9
25	OSC4	65	SEG46	105	SC18	145	SEG8
26	V_{DD}	66	SEG47	106	SC19	146	SEG7
27	$\overline{\text{RESET}}$	67	SEG48	107	SC20	147	SEG6
28	$\overline{\text{TEST2}}$	68	SEG49	108	SC21	148	SEG5
29	$\overline{\text{TEST1}}$	69	SEG50	109	SC22	149	SEG4
30	MOUT	70	SEG51	110	SC23	150	SEG3
31	P23	71	SEG52	111	SC24	151	SEG2
32	P22	72	SEG53	112	SC25	152	SEG1
33	P21	73	SEG54	113	SC26	153	SEG0
34	P20	74	SEG55	114	SC27	154	COM03
35	P13	75	SEG56	115	SC28	155	COM02
36	P12	76	SEG57	116	N.C.	156	COM01
37	P11	77	SEG58	117	N.C.	157	COM00
38	P10	78	SEG59	118	N.C.	158	K13
39	N.C.	79	N.C.	119	N.C.	159	K12
40	N.C.	80	R00	120	N.C.	160	K11

N.C. : No Connection

■ PIN DESCRIPTION

Signal name	Pin No.	In/Out	Function
V_{DD}	26	–	Power (+) supply
V_{SS}	20	–	Power (–) supply
V_{D1}	23	–	Oscillation/internal logic system regulated voltage output
V_{D2}	19	–	Supply voltage doubler/halver output
V_{C1}–V_{C3}	18–16	–	LCD system power supply 1/3 or 1/2 bias (selected by mask option)
CA, CB	12, 13	–	LCD system boosting/reducing capacitor connecting
CC, CD	14, 15	–	Supply voltage doubling/halving capacitor connecting
OSC1	21	I	Crystal oscillation input
OSC2	22	O	Crystal oscillation output
OSC3	24	I	CR oscillation input
OSC4	25	O	CR oscillation output
K00–K03	6–3	I	Input port
K10–K13	1, 160–158	I	Input port
P00–P03	44–41	I/O	I/O port
P10–P13	38–35	I/O	I/O port (switching to serial I/F input/output is possible by software)
P20–P23	34–31	I/O	I/O port
R00	80	O	Output port
R01	81	O	Output port
R02	82	O	Output port (switching to TOUT output is possible by software)
R03	83	O	Output port (switching to FOUT output is possible by software)
R10–R13	84–87	O	Output port
COM00–COM03	157–154	O	LCD common output (1/4, 1/3, 1/2 duty can be selected by software)
COM10–COM13	48–45		
SEG0–SEG59	153–124, 49–78	O	LCD segment output
MOUT	30	O	Melody output
SC1–SC28	88–115	I, O, I/O	G/A input/output
$\overline{RESET}$	27	I	Initial reset input
$\overline{TEST1}$	29	I	Testing input
$\overline{TEST2}$	28	I	Testing input

■ ELECTRICAL CHARACTERISTICS

● Absolute Maximum Ratings

(V_{SS}=0V)

Rating	Symbol	Value	Unit
Supply voltage	V_{DD}	-0.5 to 7.0	V
Input voltage (1)	V_I	-0.5 to V_{DD} + 0.3	V
Input voltage (2)	V_{IOSC}	-0.5 to V_{D1} + 0.3	V
Permissible total output current *1	ΣI_{VDD}	10	mA
Operating temperature	Topr	-20 to 70	°C
Storage temperature	Tstg	-65 to 150	°C
Soldering temperature / Time	Tsol	260°C, 10sec (lead section)	–
Permissible dissipation *2	P_D	250	mW

*1: The permissible total output current is the sum total of the current (average current) that simultaneously flows from the output pins (or is draw in).
*2: In case of plastic package (QFP8-160pin).

● Recommended Operating Conditions

(Ta=-20 to 70°C)

Condition	Symbol	Remark		Min.	Typ.	Max.	Unit
Supply voltage	V_{DD}	V_{SS}=0V	Doubler mode (OSC3 OFF)	0.9	1.1	1.25	V
			Doubler mode (OSC3 ON)	0.9	1.1	2.2	V
			Normal mode (OSC3 OFF)	1.25	3.0	3.6	V
			Normal mode (OSC3 ON)	2.2	3.0	3.6	V
			Halver mode (OSC3 OFF)	2.5	3.0	3.6	V
Oscillation frequency	f_{OSC1}	Any one is selected		–	32.768	–	kHz
				–	76.8	–	kHz
				–	153.6	–	kHz
	f_{OSC3}	Duty 50±5%, VDC="1"		50		400	kHz

● DC Characteristics

(Unless otherwise specified: V_{DD}=1.5V, V_{SS}=0V, f_{OSC1}=32.768kHz, Ta=25°C, V_{D1}/V_{C1}/V_{C2}/V_{C3} are internal voltage, C_1–C_5=0.2µF, C_6–C_7=0.4µF)

Characteristic	Symbol	Condition		Min.	Typ.	Max.	Unit
High level input voltage (1)	V_{IH1}		K00–03, K10–13 P00–03, P10–13, P20–23	0.8·V_{DD}		V_{DD}	V
High level input voltage (2)	V_{IH2}		$\overline{RESET}$, $\overline{TEST1}$, $\overline{TEST2}$	0.9·V_{DD}		V_{DD}	V
Low level input voltage (1)	V_{IL1}		K00–03, K10–13 P00–03, P10–13, P20–23	0		0.2·V_{DD}	V
Low level input voltage (2)	V_{IL2}		$\overline{RESET}$, $\overline{TEST1}$, $\overline{TEST2}$	0		0.1·V_{DD}	V
High level input current	I_{IH}	V_{IH}=1.5V	K00–03, K10–13 P00–03, P10–13, P20–23 $\overline{RESET}$, $\overline{TEST1}$, $\overline{TEST2}$	0		0.5	µA
Low level input current (1)	I_{IL1}	V_{IL1}=V_{SS} No pull-up	K00–03, K10–13 P00–03, P10–13, P20–23 $\overline{RESET}$, $\overline{TEST1}$, $\overline{TEST2}$	-0.5		0	µA
Low level input current (2)	I_{IL2}	V_{IL2}=V_{SS} With pull-up	K00–03, K10–13 P00–03, P10–13, P20–23 $\overline{RESET}$, $\overline{TEST1}$, $\overline{TEST2}$	-8	-5	-3	µA
High level output current (1)	I_{OH1}	V_{OH1}=0.9•V_{DD}	R00–03, R10–13 P00–03, P10–13, P20–23			-0.3	mA
High level output current (2)	I_{OH2}	V_{OH2}=0.9•V_{DD}	MOUT			-0.3	mA
Low level output current (1)	I_{OL1}	V_{OL1}=0.1•V_{DD}	R00–03, R10–13 P00–03, P10–13, P20–23	0.7			mA
Low level output current (2)	I_{OL2}	V_{OL2}=0.1•V_{DD}	BZ	0.7			mA
Common output current	I_{OH3}	V_{OH3}=V_{C3}-0.05V	COM0–COM3(10–13)			-10	µA
	I_{OL3}	V_{OL3}=V_{SS}+0.05V		10			µA
Segment output current (during LCD output)	I_{OH4}	V_{OH4}=V_{C3}-0.05V	SEG0–SEG59			-10	µA
	I_{OL4}	V_{OL4}=V_{SS}+0.05V		10			µA
Segment output current (during DC output)	I_{OH5}	V_{OH5}=0.9•V_{DD}	SEG0–SEG59			-100	µA
	I_{OL5}	V_{OL5}=0.1•V_{DD}		100			µA

(Unless otherwise specified: V_{DD}=3.0V, V_{SS}=0V, f_{OSC1}=32.768kHz, Ta=25°C, V_{D1}/V_{C1}/V_{C2}/V_{C3} are internal voltage, C_1–C_5=0.2µF, C_6–C_7=0.4µF)

Characteristic	Symbol	Condition		Min.	Typ.	Max.	Unit
High level input voltage (1)	V_{IH1}		K00–03, K10–13 P00–03, P10–13, P20–23	0.8·V_{DD}		V_{DD}	V
High level input voltage (2)	V_{IH2}		$\overline{RESET}$, $\overline{TEST1}$, $\overline{TEST2}$	0.9·V_{DD}		V_{DD}	V
Low level input voltage (1)	V_{IL1}		K00–03, K10–13 P00–03, P10–13, P20–23	0		0.2·V_{DD}	V
Low level input voltage (2)	V_{IL2}		$\overline{RESET}$, $\overline{TEST1}$, $\overline{TEST2}$	0		0.1·V_{DD}	V
High level input current	I_{IH}	V_{IH}=3.0V	K00–03, K10–13 P00–03, P10–13, P20–23 $\overline{RESET}$, $\overline{TEST1}$, $\overline{TEST2}$	0		0.5	µA
Low level input current (1)	I_{IL1}	V_{IL1}=V_{SS} No pull-up	K00–03, K10–13 P00–03, P10–13, P20–23 $\overline{RESET}$, $\overline{TEST1}$, $\overline{TEST2}$	-0.5		0	µA
Low level input current (2)	I_{IL2}	V_{IL2}=V_{SS} With pull-up	K00–03, K10–13 P00–03, P10–13, P20–23 $\overline{RESET}$, $\overline{TEST1}$, $\overline{TEST2}$	-16	-5	-6	µA
High level output current (1)	I_{OH1}	V_{OH1}=0.9•V_{DD}	R00–03, R10–13 P00–03, P10–13, P20–23			-1.5	mA
High level output current (2)	I_{OH2}	V_{OH2}=0.9•V_{DD}	MOUT			-1.5	mA
Low level output current (1)	I_{OL1}	V_{OL1}=0.1•V_{DD}	R00–03, R10–13 P00–03, P10–13, P20–23	6			mA
Low level output current (2)	I_{OL2}	V_{OL2}=0.1•V_{DD}	BZ	6			mA
Common output current	I_{OH3}	V_{OH3}=V_{C3}-0.05V	COM0–COM3(10–13)			-10	µA
	I_{OL3}	V_{OL3}=V_{SS}+0.05V		10			µA
Segment output current (during LCD output)	I_{OH4}	V_{OH4}=V_{C3}-0.05V	SEG0–SEG59			-10	µA
	I_{OL4}	V_{OL4}=V_{SS}+0.05V		10			µA
Segment output current (during DC output)	I_{OH5}	V_{OH5}=0.9•V_{DD}	SEG0–SEG59			-300	µA
	I_{OL5}	V_{OL5}=0.1•V_{DD}		300			µA

● Analog Circuit Characteristics and Current Consumption

(Unless otherwise specified: V_{DD}=3.0V, V_{SS}=0V, f_{OSC1}=32.768kHz, C_G=25pF, Ta=25°C, V_{D1}/V_{C1}–V_{C3} are internal voltage, C_1–C_5=0.2µF, C_6–C_7=0.4µF)

Characteristic	Symbol	Condition		Min.	Typ.	Max.	Unit
LCD drive voltage	V_{C1}	Connect 1MΩ load resistor between V_{SS} and V_{C1} (No panel load)		0.95	1.05	1.15	V
	V_{C2}	Connect 1MΩ load resistor between V_{SS} and V_{C2} (No panel load)		2•V_{C1} ×0.9		2•V_{C1} +0.1	V
	V_{C3}	Connect 1MΩ load resistor between V_{SS} and V_{C3} (No panel load)		3•V_{C1} ×0.9		3•V_{C1} +0.1	V
SVD voltage	V_{SVD}	SVDS0–3="0"		0.95	1.05	1.15	V
		SVDS0–3="1"		1.05	1.10	1.15	V
		SVDS0–3="2"		1.10	1.15	1.20	V
		SVDS0–3="3"		1.15	1.20	1.25	V
		SVDS0–3="4"		1.20	1.25	1.30	V
		SVDS0–3="5"		1.25	1.30	1.35	V
		SVDS0–3="6"		1.35	1.40	1.45	V
		SVDS0–3="7"		1.55	1.60	1.65	V
		SVDS0–3="8"		1.90	1.95	2.00	V
		SVDS0–3="9"		1.95	2.00	2.05	V
		SVDS0–3="10"		2.00	2.05	2.10	V
		SVDS0–3="11"		2.05	2.10	2.15	V
		SVDS0–3="12"		2.15	2.20	2.25	V
		SVDS0–3="13"		2.25	2.30	2.35	V
		SVDS0–3="14"		2.45	2.50	2.55	V
		SVDS0–3="15"		2.55	2.60	2.65	V
SVD circuit response time	t_{SVD}					100	µS
Current consumption	I_{OP}	During HALT	32.768kHz		1.2	2.3	µA
		Normal mode	76.8kHz		1.8	3.0	µA
		LCD power OFF	153.6kHz		3.4	6.0	µA
		During HALT	32.768kHz		2.0	3.5	µA
		Normal mode *1	76.8kHz		2.7	4.5	µA
		LCD power ON	153.6kHz		4.3	7.5	µA
		During HALT	32.768kHz		4.8	8.0	µA
		Doubler mode (V_{DD}=1.2V) *1	76.8kHz		6.0	10.0	µA
		LCD power ON	153.6kHz		10.0	17.0	µA
		During HALT	32.768kHz		1.5	2.4	µA
		Halver mode (V_{DD}=3.0V) *1	76.8kHz		1.8	3.0	µA
		LCD power ON	153.6kHz		2.5	4.5	µA
		During execution	32.768kHz		6.0	10.0	µA
		Normal mode *1	76.8kHz		12.0	20.0	µA
		LCD power ON	153.6kHz		23.0	35.0	µA
			400kHz (CR oscillation)		85.0	130.0	µA
		During execution	32.768kHz		13.0	20.0	µA
		Doubler mode (V_{DD}=1.2V) *1	76.8kHz		25.0	40.0	µA
		LCD power ON	153.6kHz		45.0	70.0	µA
			400kHz (CR oscillation)		170.0	260.0	µA
		During execution	32.768kHz		3.5	6.0	µA
		Halver mode (V_{DD}=3.0V) *1	76.8kHz		7.0	10.0	µA
		LCD power ON	153.6kHz		12.0	18.0	µA

*1: No panel load. The SVD circuit is OFF.

● Oscillation Characteristics

The oscillation characteristics change depending on the conditions (components used, board pattern, etc.). Use the following characteristics as reference values.

OSC1 crystal oscillation circuit

(Unless otherwise specified: V_{DD}=3.0V, V_{SS}=0V, f_{OSC1}=32.768kHz, C_G=25pF, C_D=built-in, Ta=25°C)

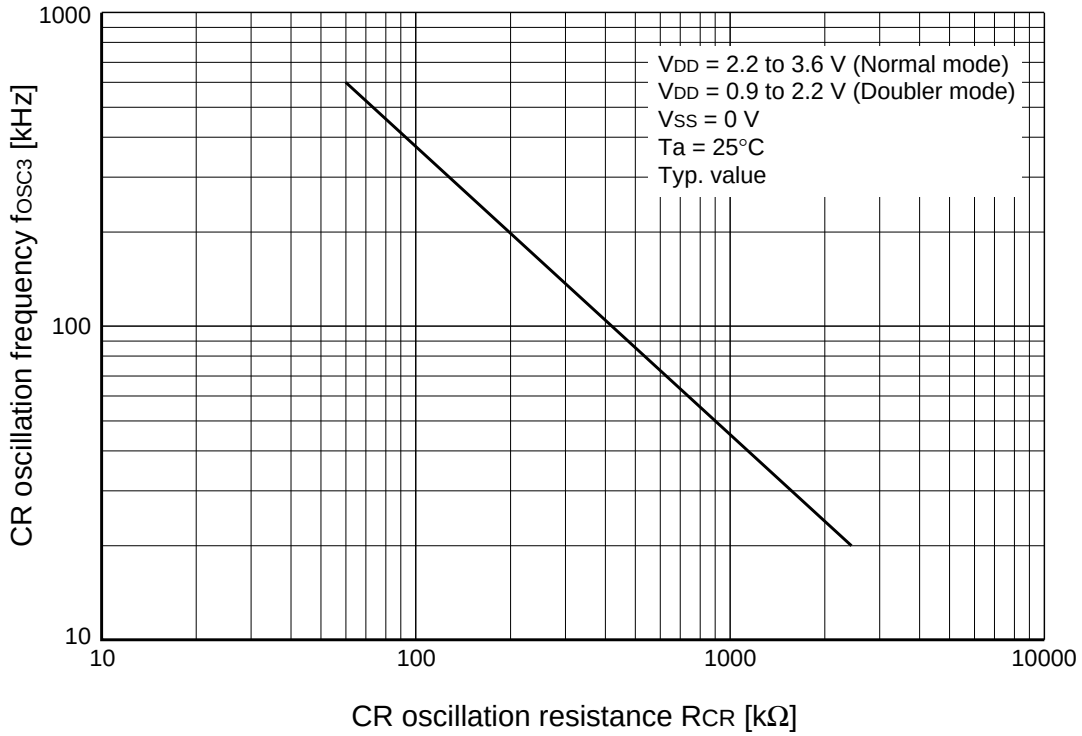
Characteristic	Symbol	Condition		Min.	Typ.	Max.	Unit
Oscillation start voltage	Vsta	tsta≤3sec (V_{DD})		1.1			V
Oscillation stop voltage	Vstp	tstp≤10sec	Normal mode	1.1			V
		(V_{DD})	Doubler mode	0.9			V
Built-in capacitance (drain)	C_D	Including the parasitic capacity inside the IC (in chip)			14		pF
Frequency/voltage deviation	∂f/∂V	V_{DD}=0.9 to 3.6V	with VDC switching			10	ppm
			without VDC switching			5	ppm
Frequency/IC deviation	∂f/∂IC			-10		10	ppm
Frequency adjustment range	∂f/∂C_G	C_G=5 to 25pF	32.768kHz	30	40		ppm
			76.8kHz	20	25		ppm
			153.6kHz	8	10		ppm
Harmonic oscillation start voltage	V_{hho}	C_G=5pF (V_{DD})		3.6			V
Permitted leak resistance	R_{leak}	Between OSC1 and V_{DD}, V_{SS}		200			MΩ

OSC3 CR oscillation circuit

(Unless otherwise specified: V_{DD}=3.0V, V_{SS}=0V, R_{CR}=120kΩ, Ta=25°C)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation frequency dispersion	f_{OSC3}		-30	310kHz	30	%
Oscillation start voltage	Vsta	Normal mode (V_{DD})	2.2			V
		Doubler mode (V_{DD})	0.9			V
Oscillation start time	tsta	V_{DD}=2.2 to 3.6V (Doubler mode: V_{DD}=0.9 to 2.2V)			3	mS
Oscillation stop voltage	Vstp	Normal mode (V_{DD})	2.2			V
		Doubler mode (V_{DD})	0.9			V

CR oscillation frequency-resistance characteristics



● Serial Interface AC Characteristics

Clock synchronous master mode (during 32 kHz operation)

(Condition: V_{DD}=1.5V, V_{SS}=0V, Ta=25°C, V_{IH1}=0.8V_{DD}, V_{IL1}=0.2V_{DD}, V_{OH}=0.8V_{DD}, V_{OL}=0.2V_{DD})

Characteristic	Symbol	Min.	Typ.	Max.	Unit
Transmitting data output delay time	tsmd			5	µS
Receiving data input set-up time	tsms	10			µS
Receiving data input hold time	tsmh	5			µS

Clock synchronous master mode (during 400 kHz operation)

(Condition: V_{DD}=3.0V, V_{SS}=0V, Ta=25°C, V_{IH1}=0.8V_{DD}, V_{IL1}=0.2V_{DD}, V_{OH}=0.8V_{DD}, V_{OL}=0.2V_{DD})

Characteristic	Symbol	Min.	Typ.	Max.	Unit
Transmitting data output delay time	tsmd			200	nS
Receiving data input set-up time	tsms	400			nS
Receiving data input hold time	tsmh	200			nS

Clock synchronous slave mode (during 32 kHz operation)

(Condition: V_{DD}=1.5V, V_{SS}=0V, Ta=25°C, V_{IH1}=0.8V_{DD}, V_{IL1}=0.2V_{DD}, V_{OH}=0.8V_{DD}, V_{OL}=0.2V_{DD})

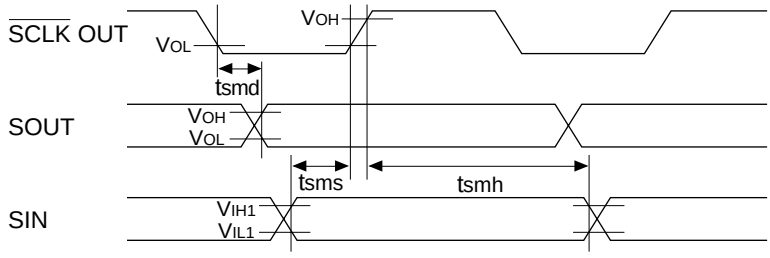
Characteristic	Symbol	Min.	Typ.	Max.	Unit
Transmitting data output delay time	tssd			10	µS
Receiving data input set-up time	tsss	10			µS
Receiving data input hold time	tssh	5			µS

Clock synchronous slave mode (during 400 kHz operation)

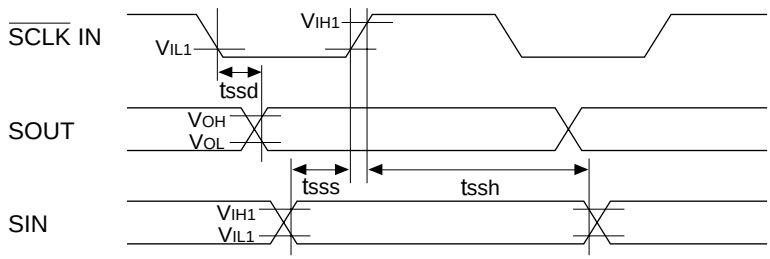
(Condition: V_{DD}=3.0V, V_{SS}=0V, Ta=25°C, V_{IH1}=0.8V_{DD}, V_{IL1}=0.2V_{DD}, V_{OH}=0.8V_{DD}, V_{OL}=0.2V_{DD})

Characteristic	Symbol	Min.	Typ.	Max.	Unit
Transmitting data output delay time	tssd			500	nS
Receiving data input set-up time	tsss	400			nS
Receiving data input hold time	tssh	200			nS

Master mode



Slave mode



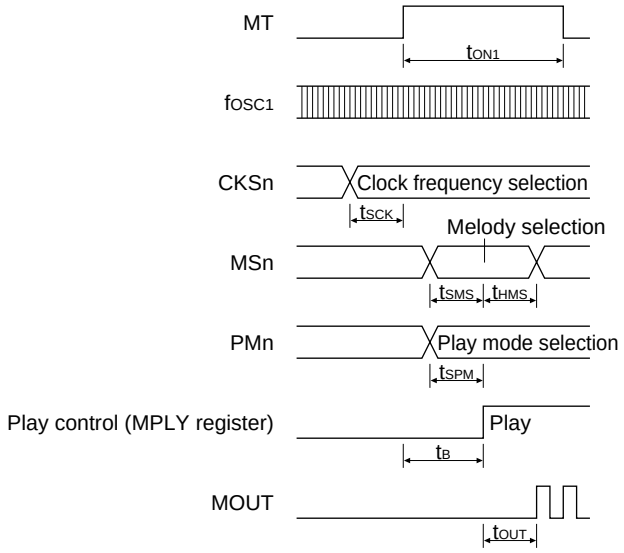
● Melody Generator AC Characteristics

(Unless otherwise specified: V_{DD}=3.0V, V_{SS}=0V, Ta=25°C)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Play start MT minimum pulse width	t_{ON1}		27.4 *1			mS
Frequency selection data set-up time	t_{SCK}		10			µS
Melody selection data set-up time	t_{SMS}		10			µS
Melody selection data hold time	t_{HMS}	"Melody change during play is impossible" option	10			µS
Play mode selection data set-up time	t_{SPM}		10			µS
Play start delay time	t_B				31.25 *1	mS
Output inverting time	t_{OUT}	f_{OSC1}=76.8, 153.6 kHz			1.68	mS
		f_{OSC1}=32.768 kHz			1.96	mS
Play suspension time (1)	t_{E1}		0.0039		1 beat	Sec
Play suspension time (2)	t_{E2}		1 beat		2 beats	Sec
MT=0 minimum pulse width	t_{OFF}		1 beat			Sec
MT=1 minimum pulse width	t_{ON2}		1 beat			Sec
Melody changing time during play	t_{MC}	"Melody change during play is possible" option	0		Note length at change	

*1 The quantization error becomes smaller than the standard value about by synchronization with the external clock. Therefore, actual time t is as follows: (Standard value - external clock 1 cycle) < t < standard value)

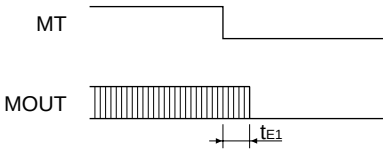
Play start timing



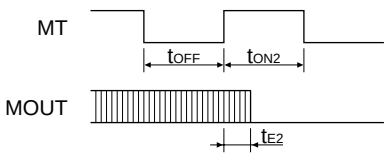
Melody and play mode selections should be done before starting the play (before setting the MT register to "1"), though it is no problem if the set-up time can be maintained.

Play stop timing

• Level hold play and One-shot C play

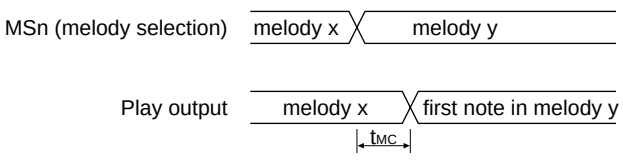


• Start/stop control by MT



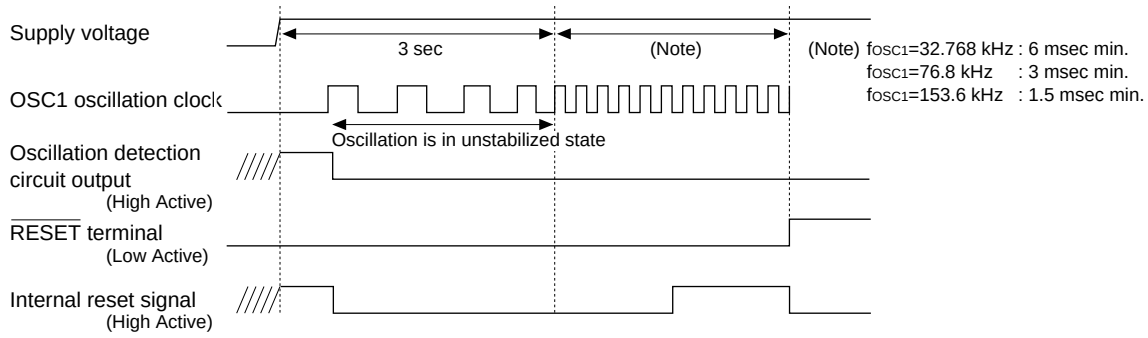
Change of melody during playing

• When the mask option "possible to change" is selected

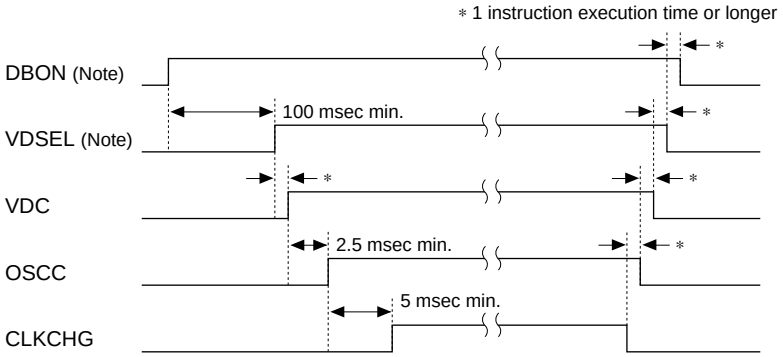


● Timing Chart

Initial reset

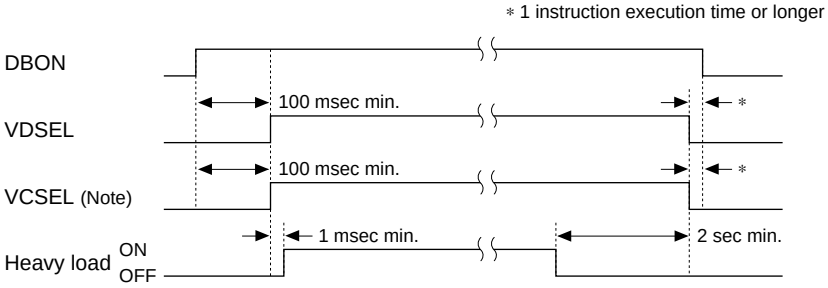


System clock switching



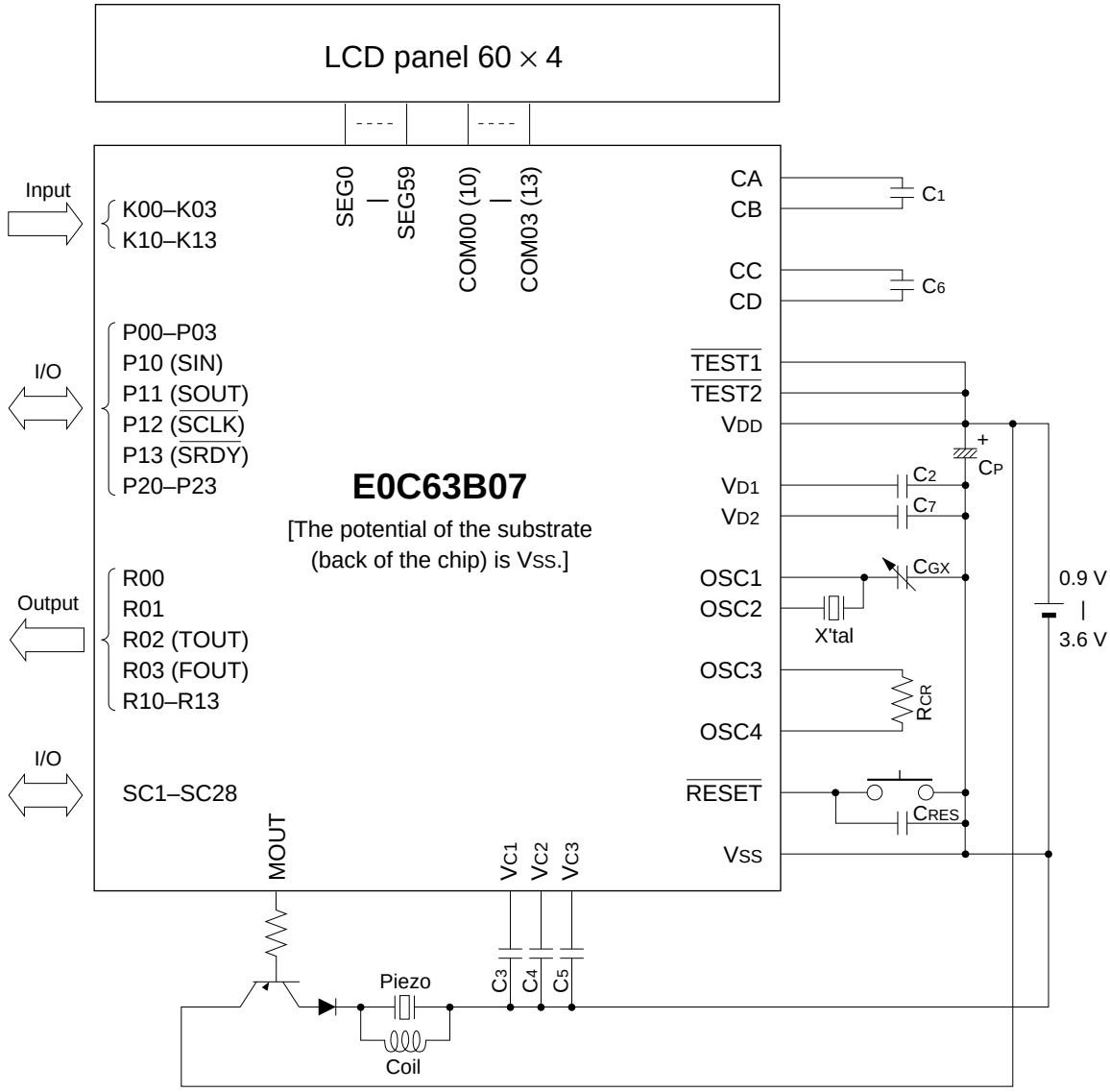
(Note) Use DBON and VDSEL only when changes are requied.

Supply voltage doubler control during heavy load driving



(Note) VCSEL is used only when it is required.

■ BASIC EXTERNAL CONNECTION DIAGRAM



X'tal	Crystal oscillator	32.768 kHz/76.8 kHz/153.6 kHz, C_I (Max.) = 34 kΩ
C_{GX}	Trimmer capacitor	5–25 pF
R_{CR}	Resistor for CR oscillation	120 kΩ (Max. 400 kHz)
C_1–C_5	Capacitor	0.2 µF
C_6, C_7	Capacitor	0.4 µF
C_P	Capacitor	3.3 µF

Note: The above table is simply an example, and is not guaranteed to work.

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