EPSON

E0C63B08

4-bit Single Chip Microcomputer

Low Voltage Operation Products

- 4-bit Low Cycle / Inst. Core CPU
- Built-in 7 Segment Type LCD Driver
- Low Voltage Operation (0.9V Min.)
- Built-in Gate Array

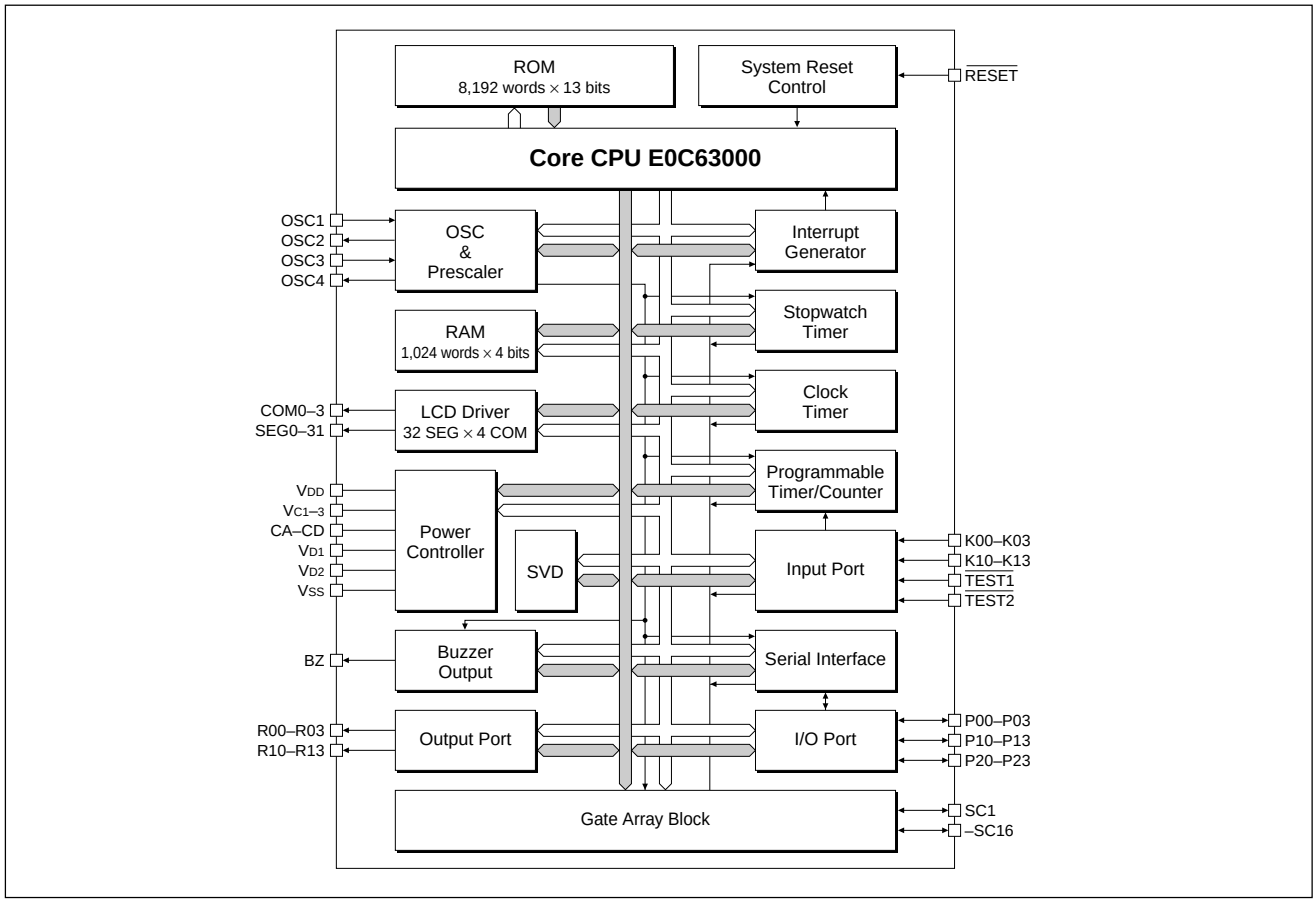
■ DESCRIPTION

The E0C63B08 is a CMOS 4-bit microcomputer composed of a CMOS 4-bit core CPU, ROM, RAM, 7 segment type LCD driver, 5000 gates of gate array and counters. And the E0C63B08 can be operated by single Manganese battery with LCD display. So that tha E0C63B08 is best suited for systems such as numeric pager.

■ FEATURES

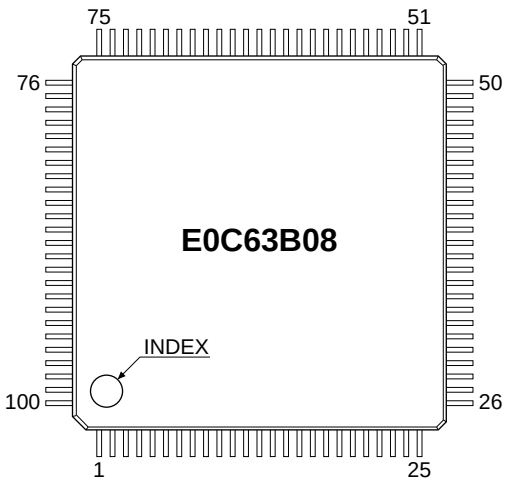
- CMOS LSI 4-bit parallel processing
- Main clock ..... 32.768 / 76.8 / 153.6kHz (Typ.)
- Sub clock ..... 400kHz (Max.)
- Instruction set ..... 46 kinds, 411 instructions
- Instruction execution time ..... 32kHz 61µsec (Min.)
  400kHz 5µsec (Min.)
- ROM capacity ..... 8,192 × 13 bit
- RAM capacity ..... 1,024 × 4 bit
- I/O port ..... Input : 8 bit
  Output : 8 bit
  I/O : 12 bit
- LCD driver ..... 32 segments × 4 commons
- Gate array ..... 5,000 usable gates (Bus interface)
- Supply voltage detect ..... 1.2V / 1.8V
- Clock timer ..... 1 ch.
- Watchdog timer ..... Built-in
- Programmable timer ..... 8 bit × 2 ch.
- Serial interface ..... Synchronous 8-bit
- Interrupts ..... External : Key interrupt 1 line
  Internal : Clock timer (1, 2, 8, 16Hz) 1 line
  : Programmable timer 1 line
  : Serial interface 1 line
  : Gate array 4 lines
- Supply voltage ..... 0.9 to 3.6V
- Current consumption ..... HALT mode (32.768kHz, 1.5V) : 1.8µA (Typ.)
- Package ..... QFP15-100pin (plastic), Die form

■ BLOCK DIAGRAM



■ PIN CONFIGURATION

QFP15-100pin



No.	Name	No.	Name	No.	Name	No.	Name
1	SEG25	26	N.C.	51	BZ	76	SEG0
2	SEG26	27	CA	52	K00	77	SEG1
3	SEG27	28	$\overline{\text{RESET}}$	53	K01	78	SEG2
4	SEG28	29	$\overline{\text{TEST2}}$	54	K02	79	SEG3
5	SEG29	30	$\overline{\text{TEST1}}$	55	K03	80	SEG4
6	SEG30	31	P23	56	K10	81	SEG5
7	SEG31	32	P22	57	K11	82	SEG6
8	COM0	33	P21	58	K12	83	SEG7
9	COM1	34	P20	59	K13	84	SEG8
10	COM2	35	P13	60	SC1	85	SEG9
11	COM3	36	P12	61	SC2	86	SEG10
12	CD	37	P11	62	SC3	87	SEG11
13	CC	38	P10	63	SC4	88	SEG12
14	V_{C3}	39	P03	64	SC5	89	SEG13
15	V_{C2}	40	P02	65	SC6	90	SEG14
16	V_{C1}	41	P01	66	SC7	91	SEG15
17	V_{D2}	42	P00	67	SC8	92	SEG16
18	V_{SS}	43	R13	68	SC9	93	SEG17
19	OSC1	44	R12	69	SC10	94	SEG18
20	OSC2	45	R11	70	SC11	95	SEG19
21	V_{D1}	46	R10	71	SC12	96	SEG20
22	OSC3	47	R03	72	SC13	97	SEG21
23	OSC4	48	R02	73	SC14	98	SEG22
24	V_{DD}	49	R01	74	SC15	99	SEG23
25	CB	50	R00	75	SC16	100	SEG24

N.C. : No Connection

■ PIN DESCRIPTION

Pin name	Pin No.	In/Out	Function
V_{DD}	24	–	Power (+) supply pin
V_{SS}	18	–	Power (–) supply pin
V_{D1}	21	–	Oscillation/internal logic system regulated voltage output pin
V_{D2}	17	–	Supply voltage doubler/halver output pin
V_{C1}–V_{C3}	16–14	–	LCD system power supply pin 1/3 or 1/2 bias (selected by mask option)
CA, CB	27, 25	–	LCD system boosting/reducing capacitor connecting pin
CC, CD	13, 12	–	Supply voltage doubling/halving capacitor connecting pin
OSC1	19	I	Crystal oscillation input pin
OSC2	20	O	Crystal oscillation output pin
OSC3	22	I	CR oscillation input pin
OSC4	23	O	CR oscillation output pin
K00–K03	52–55	I	Input port
K10–K13	56–59	I	Input port
P00–P03	42–39	I/O	I/O port
P10–P13	38–35	I/O	I/O port (switching to serial I/F input/output is possible by software)
P20–P23	34–31	I/O	I/O port
R00	50	O	Output port
R01	49	O	Output port
R02	48	O	Output port (switching to TOUT output is possible by software)
R03	47	O	Output port (switching to FOUT output is possible by software)
R10–R13	46–43	O	Output port
COM0–COM3	8–11	O	LCD common output pin (1/4, 1/3, 1/2 duty can be selected by software)
SEG0–SEG31	76–100, 1–7	O	LCD segment output pin
BZ	51	O	Buzzer output pin
SC1–SC16	60–75	I, O, I/O	G/A input/output pin
$\overline{RESET}$	28	I	Initial reset input pin
$\overline{TEST1}$	30	I	Testing input pin
$\overline{TEST2}$	29	I	Testing input pin

■ ELECTRICAL CHARACTERISTICS

● Absolute Maximum Ratings

(V_{SS}=0V)

Rating	Symbol	Value	Unit
Supply voltage	V_{DD}	-0.5 to 7.0	V
Input voltage (1)	V_I	-0.5 to V_{DD} + 0.3	V
Input voltage (2)	V_{IOSC}	-0.5 to V_{D1} + 0.3	V
Permissible total output current *1	ΣI_{VDD}	10	mA
Operating temperature	Topr	-20 to 70	°C
Storage temperature	Tstg	-65 to 150	°C
Soldering temperature / Time	Tsol	260°C, 10sec (lead section)	–
Permissible dissipation *2	P_D	250	mW

*1: The permissible total output current is the sum total of the current (average current) that simultaneously flows from the output pins (or is draw in).
*2: In case of plastic package (QFP15-100pin).

● Recommended Operating Conditions

(Ta=-20 to 70°C)

Condition	Symbol	Remark		Min.	Typ.	Max.	Unit
Supply voltage	V_{DD}	V_{SS}=0V	Doubler mode (OSC3 OFF)	0.9	1.1	1.25	V
			Doubler mode (OSC3 ON)	0.9	1.1	2.2	V
			Normal mode (OSC3 OFF)	1.25	3.0	3.6	V
			Normal mode (OSC3 ON)	2.2	3.0	3.6	V
			Halver mode (OSC3 OFF)	2.5	3.0	3.6	V
Oscillation frequency (1)	f_{OSC1}	Any one is selected		–	32.768	–	kHz
				–	76.8	–	kHz
				–	153.6	–	kHz
Oscillation frequency (2)	f_{OSC3}	Duty 50±5%, VDC="1"		50		400	kHz

● DC Characteristics

(Unless otherwise specified: V_{DD}=1.5V, V_{SS}=0V, f_{OSC1}=32.768kHz, Ta=25°C, V_{D1}/V_{C1}–V_{C3} are internal voltage, C_1–C_5=0.2µF, C_6–C_7=0.4µF)

Characteristic	Symbol	Condition		Min.	Typ.	Max.	Unit
High level input voltage (1)	V_{IH1}		K00–03, K10–13 P00–03, P10–13, P20–23	0.8•V_{DD}		V_{DD}	V
High level input voltage (2)	V_{IH2}		$\overline{RESET}$, $\overline{TEST1}$, $\overline{TEST2}$	0.9•V_{DD}		V_{DD}	V
Low level input voltage (1)	V_{IL1}		K00–03, K10–13 P00–03, P10–13, P20–23	0		0.2•V_D	V
Low level input voltage (2)	V_{IL2}		$\overline{RESET}$, $\overline{TEST1}$, $\overline{TEST2}$	0		0.1•V_{DD}	V
High level input current	I_{IH}	V_{IH}=1.5V	K00–03, K10–13 P00–03, P10–13, P20–23 $\overline{RESET}$, $\overline{TEST1}$, $\overline{TEST2}$	0		0.5	µA
Low level input current (1)	I_{IL1}	V_{IL1}=V_{SS} No pull up	K00–03, K10–13 P00–03, P10–13, P20–23 $\overline{RESET}$, $\overline{TEST1}$, $\overline{TEST2}$	-0.5		0	µA
Low level input current (2)	I_{IL2}	V_{IL2}=V_{SS} With pull up	K00–03, K10–13 P00–03, P10–13, P20–23 $\overline{RESET}$, $\overline{TEST1}$, $\overline{TEST2}$	-8	-5	-3	µA
High level output current (1)	I_{OH1}	V_{OH1}=0.9•V_{DD}	R00–03, R10–13 P00–03, P10–13, P20–23			-0.3	mA
High level output current (2)	I_{OH2}	V_{OH2}=0.9•V_{DD}	BZ			-0.3	mA
Low level output current (1)	I_{OL1}	V_{OL1}=0.1•V_{DD}	R00–03, R10–13 P00–03, P10–13, P20–23	0.7			mA
Low level output current (2)	I_{OL2}	V_{OL2}=0.1•V_{DD}	BZ	0.7			mA
Common output current	I_{OH3}	V_{OH3}=V_{C3}-0.05V	COM0–COM3			-10	µA
	I_{OL3}	V_{OL3}=V_{SS}+0.05V		10			µA
Segment output current (during LCD output)	I_{OH4}	V_{OH4}=V_{C3}-0.05V	SEG0–SEG31			-10	µA
	I_{OL4}	V_{OL4}=V_{SS}+0.05V		10			µA
Segment output current (during DC output)	I_{OH5}	V_{OH5}=0.9•V_{DD}	SEG0–SEG31			-100	µA
	I_{OL5}	V_{OL5}=0.1•V_{DD}		100			µA

(Unless otherwise specified: V_{DD}=3.0V, V_{SS}=0V, f_{OSC1}=32.768kHz, Ta=25°C, V_{D1}/V_{C1}–V_{C3} are internal voltage, C_1–C_5=0.2µF, C_6–C_7=0.4µF)

Characteristic	Symbol	Condition		Min.	Typ.	Max.	Unit
High level input voltage (1)	V_{IH1}		K00–03, K10–13 P00–03, P10–13, P20–23	0.8•V_{DD}		V_{DD}	V
High level input voltage (2)	V_{IH2}		$\overline{RESET}$, $\overline{TEST1}$, $\overline{TEST2}$	0.9•V_{DD}		V_{DD}	V
Low level input voltage (1)	V_{IL1}		K00–03, K10–13 P00–03, P10–13, P20–23	0		0.2•V_D	V
Low level input voltage (2)	V_{IL2}		$\overline{RESET}$, $\overline{TEST1}$, $\overline{TEST2}$	0		0.1•V_{DD}	V
High level input current	I_{IH}	V_{IH}=3.0V	K00–03, K10–13 P00–03, P10–13, P20–23 $\overline{RESET}$, $\overline{TEST1}$, $\overline{TEST2}$	0		0.5	µA
Low level input current (1)	I_{IL1}	V_{IL1}=V_{SS} No pull up	K00–03, K10–13 P00–03, P10–13, P20–23 $\overline{RESET}$, $\overline{TEST1}$, $\overline{TEST2}$	-0.5		0	µA
Low level input current (2)	I_{IL2}	V_{IL2}=V_{SS} With pull up	K00–03, K10–13 P00–03, P10–13, P20–23 $\overline{RESET}$, $\overline{TEST1}$, $\overline{TEST2}$	-16	-5	-6	µA
High level output current (1)	I_{OH1}	V_{OH1}=0.9•V_{DD}	R00–03, R10–13 P00–03, P10–13, P20–23			-1.5	mA
High level output current (2)	I_{OH2}	V_{OH2}=0.9•V_{DD}	BZ			-1.5	mA
Low level output current (1)	I_{OL1}	V_{OL1}=0.1•V_{DD}	R00–03, R10–13 P00–03, P10–13, P20–23	6			mA
Low level output current (2)	I_{OL2}	V_{OL2}=0.1•V_{DD}	BZ	6			mA
Common output current	I_{OH3}	V_{OH3}=V_{C3}-0.05V	COM0–COM3			-10	µA
	I_{OL3}	V_{OL3}=V_{SS}+0.05V		10			µA
Segment output current (during LCD output)	I_{OH4}	V_{OH4}=V_{C3}-0.05V	SEG0–SEG31			-10	µA
	I_{OL4}	V_{OL4}=V_{SS}+0.05V		10			µA
Segment output current (during DC output)	I_{OH5}	V_{OH5}=0.9•V_{DD}	SEG0–SEG31			-300	µA
	I_{OL5}	V_{OL5}=0.1•V_{DD}		300			µA

● Analog Circuit Characteristics and Current Consumption

(Unless otherwise specified: V_{DD}=3.0V, V_{SS}=0V, f_{OSC1}=32.768kHz, C_G=25pF, Ta=25°C, V_{D1}/V_{C1}–V_{C3} are internal voltage, C_1–C_5=0.2µF, C_6–C_7=0.4µF)

Characteristic	Symbol	Condition		Min.	Typ.	Max.	Unit
LCD drive voltage	V_{C1}	Connect 1MΩ load resistor between V_{SS} and V_{C1} (No panel load)		0.95	1.05	1.15	V
	V_{C2}	Connect 1MΩ load resistor between V_{SS} and V_{C2} (No panel load)		2•V_{C1} ×0.9		2•V_{C1} +0.1	V
	V_{C3}	Connect 1MΩ load resistor between V_{SS} and V_{C3} (No panel load)		3•V_{C1} ×0.9		3•V_{C1} +0.1	V
SVD voltage	V_{SVD}	SVDS0–3="0"		0.95	1.05	1.15	V
		SVDS0–3="1"		1.05	1.10	1.15	V
		SVDS0–3="2"		1.10	1.15	1.20	V
		SVDS0–3="3"		1.15	1.20	1.25	V
		SVDS0–3="4"		1.20	1.25	1.30	V
		SVDS0–3="5"		1.25	1.30	1.35	V
		SVDS0–3="6"		1.35	1.40	1.45	V
		SVDS0–3="7"		1.55	1.60	1.65	V
		SVDS0–3="8"		1.90	1.95	2.00	V
		SVDS0–3="9"		1.95	2.00	2.05	V
		SVDS0–3="10"		2.00	2.05	2.10	V
		SVDS0–3="11"		2.05	2.10	2.15	V
		SVDS0–3="12"		2.15	2.20	2.25	V
		SVDS0–3="13"		2.25	2.30	2.35	V
		SVDS0–3="14"		2.45	2.50	2.55	V
		SVDS0–3="15"		2.55	2.60	2.65	V
SVD circuit response time	t_{SVD}					100	µS
Current consumption	I_{OP}	During HALT	32.768kHz		1.22	1.54	µA
		Normal mode	76.8kHz		1.76	2.13	µA
		LCD power OFF	153.6kHz		3.48	4.36	µA
		During HALT	32.768kHz		1.88	2.19	µA
		Normal mode *1	76.8kHz		2.42	2.75	µA
		LCD power ON	153.6kHz		4.13	5.00	µA
		During HALT	32.768kHz		4.06	4.75	µA
		Doubler mode (V_{DD}=1.2V) *1	76.8kHz		5.33	6.08	µA
		LCD power ON	153.6kHz		8.88	10.55	µA
		During HALT	32.768kHz		1.31	1.50	µA
		Halver mode (V_{DD}=3.0V) *1	76.8kHz		1.70	1.87	µA
		LCD power ON	153.6kHz		2.50	2.83	µA
		During execution	32.768kHz		5.33	5.83	µA
		Normal mode *1	76.8kHz		10.75	11.09	µA
		LCD power ON	153.6kHz		20.83	22.30	µA
			400kHz (CR oscillation)		87.50	90.00	µA
		During execution	32.768kHz		11.17	12.33	µA
		Doubler mode (V_{DD}=1.2V) *1	76.8kHz		20.90	21.00	µA
		LCD power ON	153.6kHz		41.70	45.00	µA
			400kHz (CR oscillation)		175.0	177.5	µA
		During execution	32.768kHz		3.17	3.33	µA
		Halver mode (V_{DD}=3.0V) *1	76.8kHz		6.00	6.15	µA
		LCD power ON	153.6kHz		11.1	11.7	µA

*1: No panel load. The SVD circuit is OFF.

● Oscillation Characteristics

The oscillation characteristics change depending on the conditions (components used, board pattern, etc.). Use the following characteristics as reference values.

OSC1 crystal oscillation circuit

(Unless otherwise specified: V_{DD}=3.0V, V_{SS}=0V, f_{OSC1}=32.768kHz, C_G=25pF, C_D=built-in, Ta=25°C)

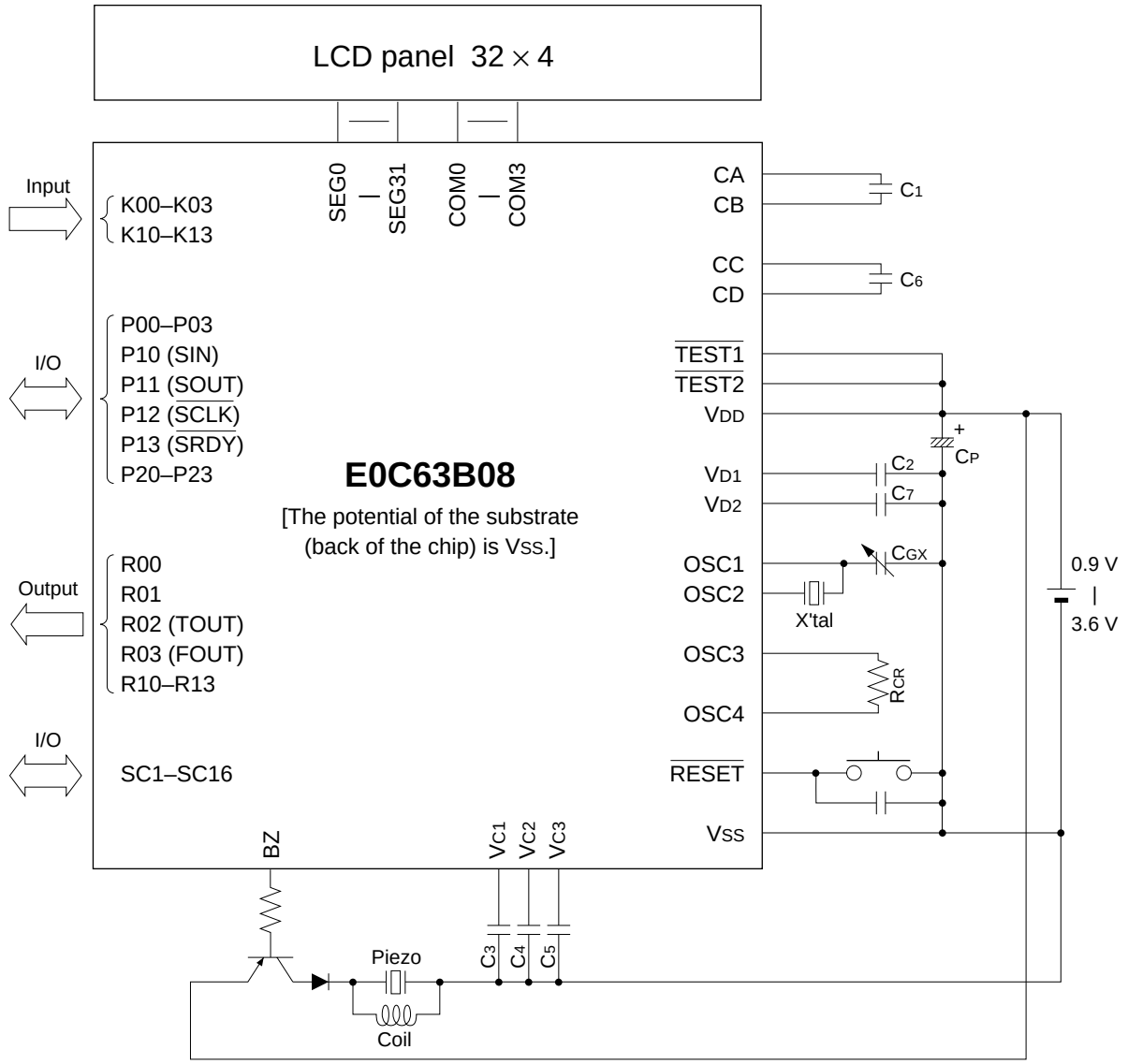
Characteristic	Symbol	Condition		Min.	Typ.	Max.	Unit
Oscillation start voltage	Vsta	tsta≤3sec (V_{DD})		1.1			V
Oscillation stop voltage	Vstp	tstp≤10sec	Normal mode	1.1			V
		(V_{DD})	Doubler mode	0.9			V
Built-in capacitance (drain)	C_D	Including the parasitic capacity inside the IC (in chip)			14		pF
Frequency/voltage deviation	∂f/∂V	V_{DD}=0.9 to 3.6V	with VDC switching			10	ppm
			without VDC switching			5	ppm
Frequency/IC deviation	∂f/∂IC			-10		10	ppm
Frequency adjustment range	∂f/∂C_G	C_G=5 to 25pF	32.768kHz	30	40		ppm
			76.8kHz	20	25		ppm
			153.6kHz	8	10		ppm
Harmonic oscillation start voltage	V_{hho}	C_G=5pF (V_{DD})		3.6			V
Permitted leak resistance	R_{leak}	Between OSC1 and V_{DD}, V_{SS}		200			MΩ

OSC3 CR oscillation circuit

(Unless otherwise specified: V_{DD}=3.0V, V_{SS}=0V, R_{CR}=120kΩ, Ta=25°C)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation frequency dispersion	f_{OSC3}		-30	310kHz	30	%
Oscillation start voltage	Vsta	Normal mode (V_{DD})	2.2			V
		Doubler mode (V_{DD})	0.9			V
Oscillation start time	tsta	V_{DD}=2.2 to 3.6V (Doubler mode: V_{DD}=0.9 to 2.2V)			3	mS
Oscillation stop voltage	Vstp	Normal mode (V_{DD})	2.2			V
		Doubler mode (V_{DD})	0.9			V

■ BASIC EXTERNAL CONNECTION DIAGRAM

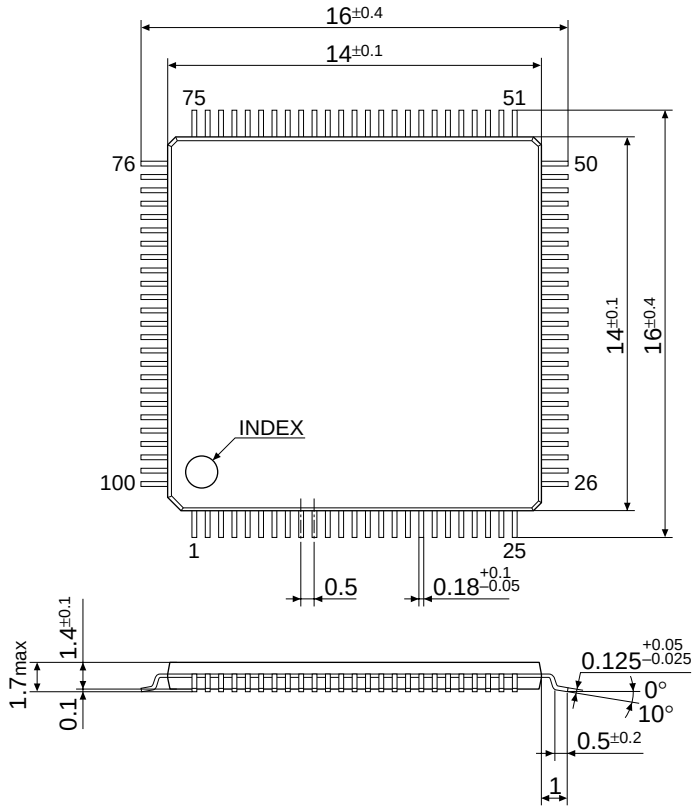


X'tal	Crystal oscillator	32.768 kHz/76.8 kHz/153.6 kHz, CI (Max.) = 34 kΩ
CGX	Trimmer capacitor	5–25 pF
RCR	Resistor for CR oscillation	120 kΩ (Max. 400 kHz)
C1–C5	Capacitor	0.2 µF
C6, C7	Capacitor	0.4 µF
CP	Capacitor	3.3 µF

Note: The above table is simply an example, and is not guaranteed to work.

■ PACKAGE DIMENSIONS

Plastic QFP15-100pin



Unit: mm

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ENERGY SAVING EPSON