MF1329-01

EPSON

CMOS CALLING NUMBER IDENTIFICATION RECEIVER IC **E0C5251**

TECHNICAL MANUAL

ENERGY SAVING EPSON

SEIKO EPSON CORPORATION

CONTENTS

1 Overview

The E0C5251 (CAS + FSK IC), an upgraded version of the E0C5250, is a CMOS IC for calling number identification with the Call Waiting function.
It provides an interface to various call information delivery services based on Bellcore GR-30-CORE, such as CND (Calling Number Delivery), CNAM (Calling Name Delivery), and CIDCW (Calling Identity on Call Waiting), as well as British Telecom's CLIP (Calling Line Identification Service) and Cable Communications Association's CDS (Caller Display Service).
The E0C5251 incorporates power-down, ring detection, and carrier detection circuits, a synchronous receive data output function, and a clock-synchronized serial interface. All these features make it suitable for various applications such as those listed below.

- Calling number delivery service with a Call Waiting function
- Telephone sets and similar auxiliary equipment
- Telephone answering equipment
- Multifunction telephones
- Facsimiles
- Computer peripheral circuits
- Message waiting telephones

1.1 Features

- Conforms to Bellcore GR-30-CORE and SR-TSV-002476 (same as E0C5250)
- Conforms to British Telecom SIN227 and SIN242 (same as E0C5250)
- Can detect Bellcore CPE alert signal (CAS) and British Telecom idle-tone alert signal using a programmable band-pass filter (same as E0C5250)
- FSK demodulation circuit based on ITU-T V.23 and BELL202 (same as E0C5250)
- Filter bypass mode to detect call progress mode (CPM) signal (same as E0C5250)
- Programmable alert-signal detection level (same as E0C5250)
- Carrier/ring detection output (same as E0C5250)
- FSK energy mode to detect FSK signal in power-down mode (new function for E0C5251)
- Supports CAS signal single-end input (new function for E0C5251)
- Off-hook detection (new function for E0C5251)
- Supports 3.57945 MHz crystal oscillator or external clock input (same as E0C5250)
- Serial-receive data output (same as E0C5250)
- Serial host interface (same as E0C5250)
- Power-down mode (same as E0C5250)
- Power supply voltage: 2.7 V to 5.5 V (same as E0C5250)
- Operating temperature range: -20°C to 70°C (same as E0C5250)
- Current consumption: 3 mA when operating (same as E0C5250)
  1 µA in zero-power mode (same as E0C5250)
  6 µA in FSK energy detection mode (new function for E0C5251)
- Shipping form: SOP2-28pin package (plastic), DIP-28pin package (ceramic) or chip (package for E0C5251)

1.2 Block Diagram

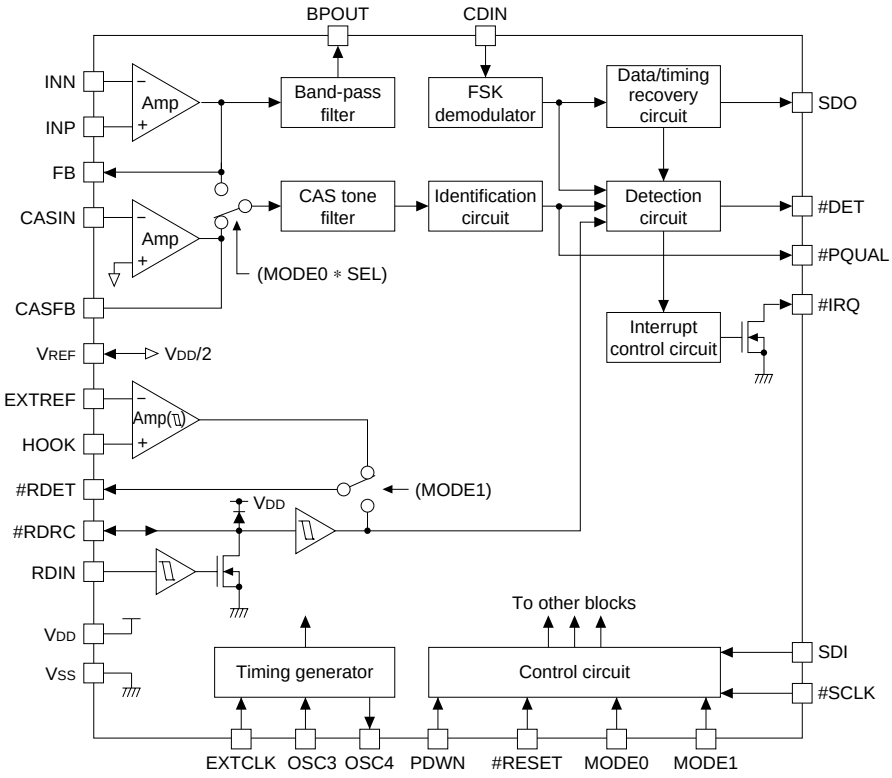
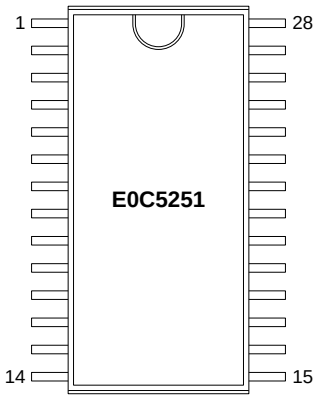


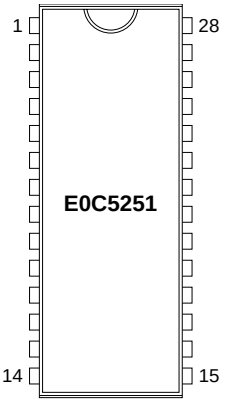
Figure 1.2.1 Block diagram

1.3 Pin Assignment

SOP2-28pin



DIP-28pin



No.	Pin name	No.	Pin name	No.	Pin name	No.	Pin name
1	INP	8	HOOK	15	OSC3	22	#IRQ
2	INN	9	RDIN	16	OSC4	23	#SCLK
3	FB	10	#RDRC	17	EXTCLK	24	SDI
4	CASIN	11	#RDET	18	MODE0	25	SDO
5	CASFB	12	PDWN	19	MODE1	26	CDIN
6	VREF	13	#RESET	20	#PQUAL	27	BPOUT
7	EXTREF	14	VSS	21	#DET	28	VDD

Figure 1.3.1 Pin assignment

1.4 Pin Description

Note: The signal and pin names prefixed by # in this manual are those of active-low signals and pins.

Table 1.4.1 Pin description

Pin name	Pin No.	Type	Power-down status	Description
INP	1	Input Analog	Off/ Active	**+ Input:** Non-inverting amplifier input. This pin is connected to the telephone wire through an input gain-setting resistor and a DC cut capacitor. Under the power down mode, this pin is functionary disconnected from the internal circuitry when the MODE1 pin is set to low level. When the MODE1 pin is set to high level, this pin stays active to detect FSK signal energy to send wake up signal to the host through the #IRQ pin. Do not connect any external components to this pin except gain setting resistors to this pin. Excess load may cause improper operation of the circuit.
INN	2	Input Analog	Off/ Active	**- Input:** Inverting amplifier input. This pin is connected to the telephone wire through an input gain-setting resistor and a DC cut capacitor. Under the power down mode, this pin is functionary disconnected from the internal circuitry when the MODE1 pin is set to low level. When the MODE1 pin is set to high level, this pin stays active to detect FSK signal energy to send wake up signal to the host through the #IRQ pin. Do not connect any external components to this pin except gain setting resistors to this pin. Excess load may cause improper operation of the circuit.
FB	3	Output Analog	High-Z/ Active	**Amplifier Output:** A feed back resistor is connected between this pin and the INN pin to set gain. Under the power down mode, this output pin is set to high impedance when the MODE1 pin is set to low level. When the MODE1 pin is set to high level in power down, this pin stays active to detect FSK signal energy to send wake up signal to the host through the #DET pin. Do not connect any external components to this pin except a gain setting resistor to this pin. Excess load may cause improper operation of the circuit.
CASIN	4	Input Analog	Off	**CAS Tone Input:** CAS tone amplifier input. For the telephone application, this pin is connected to the output of telephone hybrid circuit through input gain-setting resistor and a DC cut capacitor. Under the power down mode, this pin is functionary disconnected from the internal circuitry. Do not connect any external components to this pin except gain setting resistors to this pin. Excess load may cause improper operation of the circuit.
CASFB	5	Output Analog	High-Z	**CAS Amplifier Output:** A feed back resistor is connected between this pin and the CASIN pin to set CAS gain. Under the power down mode, this output pin is set to high impedance. Do not connect any external components to this pin except a gain setting resistor to this pin. Excess load may cause improper operation of the circuit.
V_{REF}	6	Output Analog	High-Z/ V_{DD}/2 level	**Reference Voltage Output:** 1/2 V_{DD} voltage output. This pin must be bypassed to ground through 0.1 µF capacitor. During power down mode, this output pin is set to high impedance when the MODE1 pin is low level. When the MODE1 pin is set to high level in power down, this pin stays at V_{DD}/2. Do not connect any external components to this pin except a jumper to V_{REF} pin or a bypass capacitor to ground. Excess load may cause improper operation of the circuit.
EXTREF	7	Input Analog	Active	**External Reference Voltage Input:** External DC reference voltage is connected to this pin. This voltage set the off-hook detection threshold level.
HOOK	8	Input Analog	Active	**Off-Hook Detection Input:** Diode bridge output from the TIP/RING lines is connected to this pin through external resistor divider to detect off-hook/on-hook states.
RDIN	9	Schmitt trigger input	Active	**Ring Detect Input:** The attenuated ring signal is connected to this pin for the ring detection. This circuit is always active even if the device is in the power down mode.

Pin name	Pin No.	Type	Power-down status	Description
#RDRC	10	Open-drain output Schmitt trigger input	Active	**Ring Detect RC Terminal:** RC network will be connected to this pin to set time delays for the ring signal detection. This circuit is always active even if the device is in the power down mode.
#RDET	11	Output	Active	**Ring Detect Output:** When the MODE1 pin is set to low level, this pin is connected from output of a Schmitt trigger buffer which input is connected to the #RDRC pin. Low level at this pin indicates that the ring signal is detected. When the MODE1 pin bit is set to high level, this pin is connected from output of a hook detect circuit which input is connected from the HOOK pin. High level at this pin indicates on-hook condition and low level at this pin indicates off-hook condition.
PDWN	12	Input	Active	**Power Down Input:** This pin must be kept at low level for the normal operation. When it is set to high level, the device enters the power down mode. During power down mode, the OSC4 pin is set to high level, and the VREF, CASFB and FB pins are set to high impedance. (The FB and VREF pins are set to high impedance only when the MODE1 pin is at low level.)
#RESET	13	Input	Active	**Reset Input:** When this pin is set to low level, all internal host registers are reset to their default conditions. This pin must be set to high level to write data to the internal registers.
Vss	14	Power supply (-)		**Device Ground:** This pin is connected to the system ground.
OSC3	15	Input	Off	**Crystal Oscillator/External Clock Input:** A crystal resonator is connected between this pin and the OSC4 pin. This pin may be driven from an external clock source. The proper value load capacitor must be connected between this pin and ground. During power down, this input pin is disconnected from internal circuits.
OSC4	16	Output	High level	**Crystal Oscillator Output:** A crystal or ceramic resonator is connected between this pin and OSC3 pin. This pin must be kept open when the OSC3 pin is driven from an external clock source. The proper value load capacitor must be connected between this pin and ground. During power down, this output pin is set to high level.
EXTCLK	17	Input	Active	**External Clock Input:** Typically 32.768 kHz clock signal is applied to this pin from the host device to enable pre-qualification logic used in FSK energy detection circuitry.
MODE0	18	Input	Active	**Mode0 Select Input:** This pin select CAS or FSK/CPM mode. When this pin is set to high level, CAS mode is selected. In this mode, CAS detection is enabled and the FSK function is disabled. The host device also can write internal registers through the SDI and #SCLK pin. Before writing data into registers, this pin must be set to low level once to synchronize the serial interface circuit for data writing sequence. When this pin is set to low level, FSK/CPM mode is selected. In this mode, CAS detection is disabled and the FSK/CPM function is enabled. The host device also can read the received data from the SDO pin under this mode. Refer to Table 3.2.1 for more details.
MODE1	19	Input	Active	**Mode1 Select Input:** This pin enables FSK energy and off-hook detection mode. When this pin is set to high level, FSK energy and off-hook detection mode is enabled. When this pin is set to low level, FSK energy and off-hook detection mode is disabled. Refer to Table 3.2.1 for more details.
#PQUAL	20	Output	High level	**Pre-qualification Output:** Early qualification output will be monitored at this pin. When no tones are detected, this pin stays at high level.

Pin name	Pin No.	Type	Power-down status	Description
#DET	21	Output	Active	**Detection Output:** When the device is in the power down mode and the MODE1 pin is set to low level, low level at this pin indicates the presence of ring signal or phone line reversal. If the MODE1 pin is set to high level, low level at this pin indicates the presence of ring signal or FSK inbound signal. When in the power up mode and FSK mode is selected, low level at this pin indicates the presence of FSK inbound signal. If CPM mode is selected, pulses from this pin indicate the presence of CPM tone signal. If CAS mode is selected, low level at this pin indicates the presence of CAS tone signal. Refer to Table 3.2.1 for more details.
#IRQ	22	Open-drain output	Active	**Interrupt Request Output:** When the device is in the power down mode, low level at this pin indicates the presence of ring signal or phone line reversal. When in the power up mode and FSK mode is selected, low level at this pin indicates that the received data is ready in the internal register for the host device to read. In this mode, this pin is set to high level after the first bit of the received data is read. If CPM mode is selected, low level at this pin indicates the presence of CPM. If CAS mode is selected, low level at this pin indicates that the CAS tone is detected. In this mode, this pin remains low level while CAS tones exist. Refer to Table 3.2.1 for more details.
#SCLK	23	Input	Active	**Serial Clock Input:** The host device supplies a clock to this pin to write internal registers or to read received data. The received data changes its state at falling edge of the clock supplied by the host device.
SDI	24	Input	Active	**Serial Data Input:** The host device writes control bits through this pin.
SDO	25	Output	High level	**Serial Data Output:** The host device reads the serial receive data from this pin. If asynchronous mode is selected, the asynchronous format serial data appears at this pin. If synchronous mode is selected, the received serial data is read from this pin by the host device with the serial clock supplied to the #SCLK pin. During the power down, CPM or CAS mode, this output pin is set to high level.
CDIN	26	Input Analog	V_{REF}	**Capacitor Input:** A 0.1 µF capacitor is connected between this pin and the BPOUT pin. The FSK signal can be applied from the FB pin to this pin through this 0.1 µF capacitor to bypass the band pass filter for internal testing purpose. Do not connect any external components except this capacitor to this pin. Excess load may cause improper operation of the circuit.
BPOUT	27	Output Analog	High-Z	**Capacitor Output:** A 0.1 µF capacitor is connected between this pin and the CDIN pin. The band pass filter output is monitored at this pin for internal testing purpose. Do not connect any external components except this capacitor to this pin. Excess load may cause improper operation of the circuit.
V_{DD}	28	Power supply (+)		**Device Power Supply:** Positive power supply pin.

2 Power Supply Block and Initial Reset

2.1 Power Supply

The following shows the operating power supply voltage of the E0C5251.

Power supply voltage: 2.7 V to 5.5 V

The E0C5251 is operated in the above voltage range by a single power supply that is connected between VDD and VSS. The voltage required for internal operation (VREF = 1/2 VDD) is generated by the IC itself.

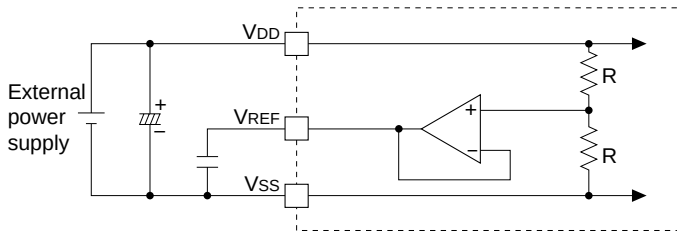


Figure 2.1.1 Power supply block

2.2 Initial Reset

The E0C5251 contains control registers that can be accessed by the external CPU through a serial interface. The control registers are initialized by an initial reset which is applied from the #RESET pin.

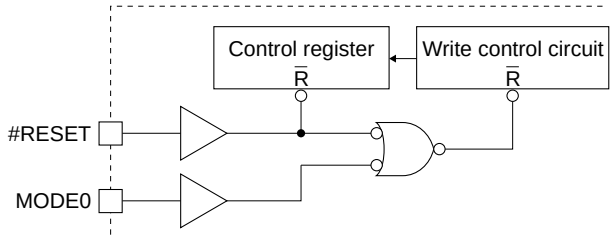


Figure 2.2.1 Initial reset circuit

Specifically, the control registers are reset by pulling the #RESET pin to Low level (VSS) from outside of the IC. Then, the reset state is eliminated by releasing the #RESET pin back to High level (VDD). Also, the write control circuit for the control register is reset when the #RESET pin or MODE0 pin is at Low level. Before data can be written to the control register, both #RESET and MODE0 must be at High level.

3 Functional Description

3.1 Register Description

The E0C5251 contains eight 4-bit registers that can be accessed by the CPU.
The CPU can access these CPU interface registers through the serial interface pins (SDI, #SCLK, and MODE0) and control the mode of the E0C5251. The CPU uses the first four bits of transmit data to specify the address A[3:0] of the internal register to be accessed. The data is transmitted beginning with the LSB (A0). The four bits that follow the LSB are data bits D[3:0] which are the data to be written to the specified register. This data is also transmitted beginning with the LSB (D0).
Table 3.1.1 shows registers and control bit assignments.

Table 3.1.1 Register structure

Register name	Address A[3:0]	Initial value	Data bit			
			D3	D2	D1	D0
MDR	0000	0000	TEST	SEL	BT	SYNC
GLR	0001	0100	GL3	GL2	GL1	GL0
GHR	0010	0100	GH3	GH2	GH1	GH0
TLR	0011	0110	TL3	TL2	TL1	TL0
THR	0100	XXX1	X	X	X	TH0
AVR	0101	X011	X	AV2	AV1	AV0
WLR	0110	0001	WL3	WL2	WL1	WL0
WHR	0111	0001	WH3	WH2	WH1	WH0

Each register is detailed below.

MDR: Mode Register (Address = 0h)

Table 3.1.2 MDR register

Bit	Bit name	Initial value	Description
D0	SYNC	0	Asynchronous/synchronous mode selection This bit is used to select asynchronous or synchronous mode. SYNC bit — Mode 0 — Selects asynchronous mode 1 — Selects synchronous mode Asynchronous mode is selected by setting this bit to 0, in which case the 8-bit serial data output from the SDO pin is forwarded in asynchronous mode. Synchronous mode is selected by setting this bit to 1. When the FSK signal is received in FSK mode, serial data is output from the SDO pin and read by the CPU synchronously with the clock signal fed from the CPU to the #SCLK pin. Also, in synchronous mode, when the receive data is ready for output, the #IRQ pin changes to Low level, indicating that the CPU can read the data.
D1	BT	0	Bellcore/BT selection This bit is used to select Bellcore or BT (British Telecom) mode. BT bit — Mode 0 — Selects Bellcore mode 1 — Selects BT mode When this bit is set to 0, the gain in the dual-tone filter is set directly by the GLR and GHR registers. When this bit is set to 1, the value set by the GLR (Table 3.1.3) and GHR (Table 3.1.4) registers plus 6 dB is set as the gain in the dual-tone filter.
D2	SEL	0	FSK/CPM mode selection This bit is used to select FSK or CPM mode when the MODE0 pin is low. SEL bit — Mode 0 — Selects FSK mode 1 — Selects CPM mode If this bit is set to 1 when the MODE0 pin is held at Low level (FSK/CPM mode), the receive filter is bypassed, and when the CPM tone is input to the INP/INN pin, the #IRQ pin goes to Low level. Also, since the pulse generated from the CPM tone signal is output from the #DET pin, the CPM (dial) tone can be identified by measuring the frequency of the pulse. If this bit is set to 0 when the MODE0 pin is held at Low level (FSK/CPM mode), the FSK function is enabled. If this bit is set to 1 when the MODE0 pin is high (CAS mode), the CAS signal can be input to the CASIN pin. If this bit is set to 0 when the MODE0 pin is high, the CAS signal can be input to the INP/INN pin.
D3	TEST	0	Test mode selection This bit is used to test the IC. This bit normally must be fixed to 0.

GLR: Low-Tone Gain Setting Register (Address = 1h)

Table 3.1.3 GLR register

Bit	Bit name	Initial value	Description
D0 D1 D2 D3	GL0 GL1 GL2 GL3	0100	Low-tone filter gain selection These bits control gain in the 2,130-Hz tone filter. GL3 GL2 Gain (dB) GL1 GL0 Gain (dB) 0 0 0 0 0 0 0 1 -4 0 1 -1 1 0 -8 1 0 -2 1 1 -12 1 1 -3 GL1 and GL0 change the gain in increments of 1 dB, whereas GL3 and GL2 change the gain in increments of 4 dB. The alert-tone detection level is attenuated (sensitivity is lowered) by an amount equal to the total gain set here.

GHR: High-Tone Gain Setting Register (Address = 2h)

Table 3.1.4 GHR register

Bit	Bit name	Initial value	Description
D0 D1 D2 D3	GH0 GH1 GH2 GH3	0100	High-tone filter gain selection These bits control gain in the 2,750-Hz tone filter. GH3 GH2 Gain (dB) GH1 GH0 Gain (dB) 0 0 0 0 0 0 0 1 -4 0 1 -1 1 0 -8 1 0 -2 1 1 -12 1 1 -3 GH1 and GH0 change the gain in increments of 1 dB, whereas GH3 and GH2 change the gain in increments of 4 dB. The alert-tone detection level is attenuated (sensitivity is lowered) by an amount equal to the total gain set here.

TLR, THR: Detection Threshold Setting Registers (Address = 3h, 4h)

Table 3.1.5 TLR and THR registers

Bit	Bit name	Initial value	Description
D0 D1 D2 D3 D0 D1 D2 D3	TL0 TL1 TL2 TL3 TH0 X X X	0110 XXX1	CAS detection threshold selection These bits control the minimum duration of tone with which the CAS tone is identified. TH0 (THR register bit 0) is the MSB of the threshold set.

TH0	TL3	TL2	TL1	TL0	Threshold value (msec)
0	0	0	0	0	5
0	0	0	0	1	9
0	0	0	1	0	12
0	0	0	1	1	16
0	0	1	0	0	19
0	0	1	0	1	21
0	0	1	1	0	23
0	0	1	1	1	26
0	1	0	0	0	29
0	1	0	0	1	32
0	1	0	1	0	34
0	1	0	1	1	36
0	1	1	0	0	39
0	1	1	0	1	43
0	1	1	1	0	46
0	1	1	1	1	48
1	0	0	0	0	50
1	0	0	0	1	53
1	0	0	1	0	56
1	0	0	1	1	59
1	0	1	0	0	61
1	0	1	0	1	64
1	**0**	**1**	**1**	**0**	**67**
1	0	1	1	1	70
1	1	0	0	0	73
1	**1**	**0**	**0**	**1**	**76**
1	1	0	1	0	78
1	1	0	1	1	81
1	1	1	0	0	84
1	1	1	0	1	87
1	1	1	1	0	90
1	1	1	1	1	Invalid (Cannot be set)

The bit setting 10110 corresponds to Bellcore and British Telecom Loop State service; the bit setting 11001 corresponds to British Telecom Idle State service.

AVR: Average Divide-Ratio Select Register (Address = 5h)

Table 3.1.6 AVR register

Bit	Bit name	Initial value	Description
D0 D1 D2 D3	AV0 AV1 AV2 X	X011	Average counter divide-ratio selection These bits control the frequency divide ratio of the internal average counter. Setting to 011 is recommended.

AV2	AV1	AV0	Divide ratio
0	0	0	1/1
0	0	1	1/2
0	1	0	1/4
0	1	1	1/8
1	0	0	1/16
1	0	1	1/32
1	1	0	1/64

WLR: Low-Tone Record Window Select Register (Address = 6h)

Table 3.1.7 WLR register

Bit	Bit name	Initial value	Description
D0 D1 D2 D3	WL0 WL1 WL2 WL3	0001	Low-tone window width selection These bits are used the low-tone record window width of the identification block. A tone can be identified when one cycle of it is within the specified range. WL3 WL2 WL1 WL0 Window width (%) 0 0 0 0 0.51, -0.50 **0 0 0 1 0.57, -0.56** **0 0 1 0 0.63, -0.62** 0 0 1 1 0.69, -0.68 0 1 0 0 0.75, -0.74 0 1 0 1 0.81, -0.80 0 1 1 0 0.87, -0.85 0 1 1 1 0.93, -0.91 1 0 0 0 0.99, -0.97 1 0 0 1 1.06, -1.03 1 0 1 0 1.12, -1.09 1 0 1 1 1.18, -1.15 **1 1 0 0 1.24, -1.20** 1 1 0 1 1.30, -1.26 1 1 1 0 1.36, -1.32 1 1 1 1 1.42, -1.38 Bit setting 0001 is Bellcore's default value. Bit setting 0010 corresponds to British Telecom Loop State service and setting 1100 corresponds to British Telecom Idle State service.

WHR: High-Tone Record Window Select Register (Address = 7h)

Table 3.1.8 WHR register

Bit	Bit name	Initial value	Description
D0 D1 D2 D3	WH0 WH1 WH2 WH3	0001	High-tone window width selection These bits are used to select the high-tone record window width of the identification block. A tone can be identified when one cycle of it is within the specified range. WH3 WH2 WH1 WH0 Window width (%) 0 0 0 0 0.51, -0.49 **0 0 0 1 0.59, -0.56** **0 0 1 0 0.67, -0.64** 0 0 1 1 0.75, -0.71 0 1 0 0 0.83, -0.79 0 1 0 1 0.90, -0.86 0 1 1 0 0.98, -0.94 0 1 1 1 1.06, -1.02 1 0 0 0 1.14, -1.09 **1 0 0 1 1.22, -1.17** 1 0 1 0 1.30, -1.24 1 0 1 1 1.37, -1.32 1 1 0 0 1.45, -1.39 1 1 0 1 1.53, -1.46 1 1 1 0 1.61, -1.54 1 1 1 1 1.69, -1.61 Bit setting 0001 is Bellcore's default value. Bit setting 0010 corresponds to British Telecom Loop State service and setting 1001 corresponds to British Telecom Idle State service.

3.2 Outputs from the #RDET, #IRQ and #DET Pins

The signals output from the #RDET, #IRQ, and #DET pins changes according to the operation mode. Table 3.2.1 lists the corresponding between the operation mode and the pin function.

Table 3.2.1 Pin functions in each operation mode

PDWN	MODE1	MODE0	SEL bit	Function	FSK input pin	CAS input pin	#RDET	#IRQ	#DET	Power mode
0	0	0	0	RING detection FSK receiving	INP/INN	Off	RING detection	FSK receive completion	FSK signal detection	Power on
0	0	0	1	CPM detection RING detection	INP/INN	Off	RING detection	CPM detection	CPM signal output	
0	0	1	0	CAS detection RING detection	Off	INP/INN	RING detection	CAS detection	CAS detection	
0	0	1	1	CAS detection RING detection	Off	CASIN	RING detection	CAS detection	CAS detection	
1	0	X	X	Zero-power mode RING detection	Off	Off	RING detection	RING detection	RING detection	Power down
0	1	0	0	FSK detection Hook detection	INP/INN	Off	Off-hook detection	FSK receive completion	FSK signal detection	Power on
0	1	0	1	CPM detection Hook detection	INP/INN	Off	Off-hook detection	CPM detection	CPM signal output	
0	1	1	0	CAS detection Hook detection	Off	INP/INN	Off-hook detection	CAS detection	CAS detection	
0	1	1	1	CAS detection Hook detection	Off	CASIN	Off-hook detection	CAS detection	CAS detection	
1	1	X	X	FSK energy detection mode RING detection Hook detection FSK energy detection	INP/INN	Off	Off-hook detection	RING detection	RING detection or FSK energy detection	Power down

3.3 Input Amp Circuit

3.3.1 Differential Input

The amp at the input stage must have its circuit configured to allow gain to be set correctly. For this reason, it requires five to six external resistors.

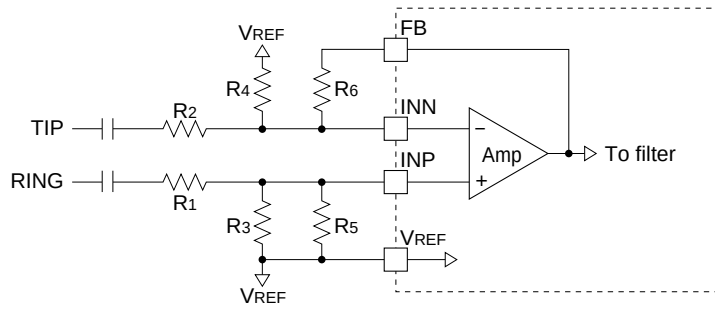


Figure 3.3.1 Input amp circuit

The gain in the input amp can be set depending on values R1 to R6 as shown below. Note that R3 and R5 may be replaced by one resistor.

$$G_{AMP} = \frac{R_5}{R_1} = \frac{R_6}{R_2} \text{ [times]} \qquad (When\ R_1 = R_2, R_3 = R_4, R_5 = R_6)$$

To set the FSK and CAS tone signal-detection levels, determine each resistance value with respect to VDD as shown below.

$$G_{AMP} = \frac{R_5}{R_1} = \frac{R_6}{R_2} = \frac{V_{DD}}{5} \times 0.562 \text{ [times]}$$

VDD is the power supply voltage fed to the VDD pin of the E0C5251. For R3 and R4, Seiko Epson recommends using a resistance of about 200 kΩ for noise prevention.

Tables 3.3.1 and 3.3.2 show typical resistance values and amp gain for the case where VDD = 5 V and VDD = 3 V, respectively. Do not use resistors with lower values than those shown in the table below when the MODE1 pin is set to 1 (FSK detection during power down).

Table 3.3.1 Resistance values and gain (VDD = 5 V)

Parameter	Value		Condition
	Bellcore	BT	
R1, R2	1000 kΩ	1000 kΩ	1%
R3, R4	200 kΩ	200 kΩ	1%
R5, R6	562 kΩ	562 kΩ	1%
Input amp gain	0.562 times (-5 dB)	0.562 times (-5 dB)	
FSK/CPM - CD ON level (Typ.)	-43.0 dBm	-45.2 dBV	
FSK/CPM - CD OFF level (Typ.)	-45.0 dBm	-47.2 dBV	
CAS - CD ON level (Typ.)	-35.9 dBm	-44.1 dBV	Tone filter gain = -4 dB

Table 3.3.2 Resistance values and gain (VDD = 3 V)

Parameter	Value		Condition
	Bellcore	BT	
R1, R2	1000 kΩ	1000 kΩ	1%
R3, R4	200 kΩ	200 kΩ	1%
R5, R6	338 kΩ	338 kΩ	1%
Input amp gain	0.3372 times (-9.4 dB)	0.3372 times (-9.4 dB)	
FSK/CPM - CD ON level (Typ.)	-43.0 dBm	-45.2 dBV	
FSK/CPM - CD OFF level (Typ.)	-45.0 dBm	-47.2 dBV	
CAS - CD ON level (Typ.)	-35.9 dBm	-44.1 dBV	Tone filter gain = -4 dB

3.3.2 Single End Input

When the amp is used as single end input, two external resistors are required.

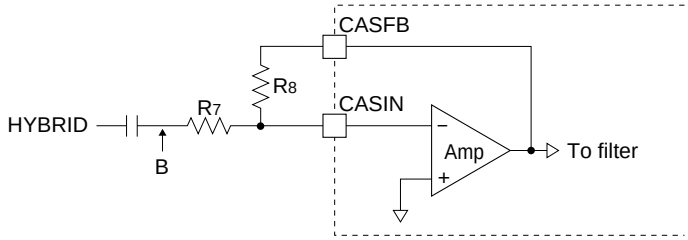


Figure 3.3.2 Input amp circuit

The gain in the input amp can be set depending on values R_7 and R_8 as shown below.

$$G_{AMP} = \frac{R_8}{R_7} \text{ [times]}$$

To set the FSK and CAS tone signal-detection levels at node B, determine each resistance value with respect to V_{DD} as shown below.

$$G_{AMP} = \frac{R_8}{R_7} = \frac{V_{DD}}{5} \times 0.562 \text{ [times]}$$

V_{DD} is the power supply voltage fed to the V_{DD} pin of the E0C5251.
Tables 3.3.3 and 3.3.4 show typical resistance values and amp gain for the case where V_{DD} = 5 V and V_{DD} = 3 V, respectively.

Table 3.3.3 Resistance values and gain (V_{DD} = 5 V)

Parameter	Value		Condition
	Bellcore	BT	
R_7	1000 kΩ	1000 kΩ	1%
R_8	562 kΩ	562 kΩ	1%
Input amp gain (Typ.)	-5.0 dB	-5.0 dB	
CAS - CD ON level (Typ.)	-35.9 dBm	-44.1 dBV	Tone filter gain = -4 dB

Table 3.3.4 Resistance values and gain (V_{DD} = 3 V)

Parameter	Value		Condition
	Bellcore	BT	
R_7	1000 kΩ	1000 kΩ	1%
R_8	338 kΩ	338 kΩ	1%
Input amp gain	-9.4 dB	-9.4dB	
CAS - CD ON level (Typ.)	-35.9 dBm	-44.1 dBV	Tone filter gain = -4 dB

3.4 Ring/Line Reversal Signal Detection

Figure 3.4.1 shows a typical circuit used to detect the Bellcore ring signal and British Telecom Line Reversal signal. When the E0C5251 is in power-down mode, this circuit detects the ring signal or Line Reversal signal. The Line Reversal or ring signal causes the voltage on the RDIN pin to rise, which drives the Schmitt rigger output high. This causes the Nch transistor to turn on and the #RDRC pin to change to Low level. Since the RDIN pin is normally at the VSS level, the #RDRC pin is at the High level. When the ring signal is input or the Line Reversal signal is generated, the capacitor of the #RDRC pin discharges, causing the #RDRC pin to change state from High to Low. The #RDET pin operates in the same way, except that in any mode other than power-down mode, the #RDET pin always responds to input on the RDIN pin.

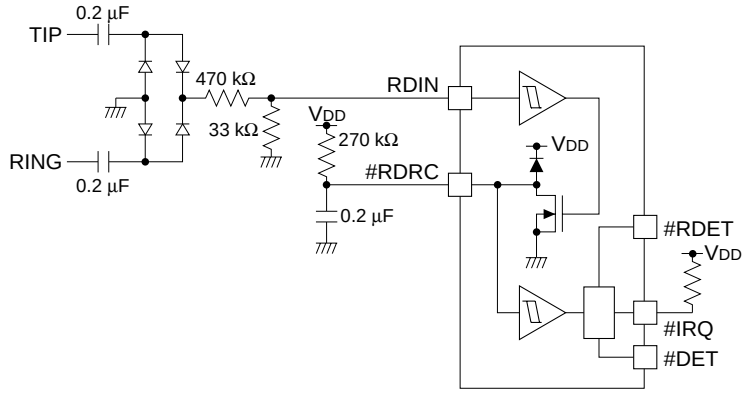


Figure 3.4.1 Ring/line reversal signal detection circuit

3.5 FSK Demodulation

The received FSK-modulated signal, after being processed by the band-pass filter, is demodulated by the FSK demodulation circuit. If the FSK signal is input when the PDWN pin is set to Low level and FSK mode has been selected by the host CPU, the #DET pin changes to Low level. The received data is read out from the SDO pin by the host CPU. Also, the #IRQ pin is driven Low each time one byte is received. This demodulation circuit supports a FSK-modulated signal that conforms to ITU-T V.23 or Bell202.

Table 3.5.1 FSK data characteristics

Parameter	Bellcore	BT
Mark frequency	1200 Hz ±1%	1300 Hz ±1.5%
Space frequency	2200 Hz ±1%	2100 Hz ±1.5%
Receive signal level	Mark: -32 dBm to -12 dBm Space: -36 dBm to -12 dBm	Mark: -40 dBV to -14 dBV Space: -36 dBV to -8 dBV
Signal distortion	≥ 25 dB	≥ 20 dB
Transfer rate	1200 baud ±1%	1200 baud ±1%

3.6 Dual-Tone Detection

Dual tones (Bellcore CPE alert signal (CAS), British Telecom tone alert signal) are detected using two tone filters and digital identification circuits. If dual tones are received when the PDWN pin is set low and CAS mode has been selected by the host CPU, the #DET pin and the #IRQ pin changes to Low level.

Table 3.6.1 Dual-tone characteristics

Parameter	Bellcore (CPE alert signal)	BT (tone alert signal)	
		Line disconnected	Line connected
Low tone frequency	2130 Hz ±0.5%	2130 Hz ±1.1%	2130 Hz ±0.6%
High tone frequency	2750 Hz ±0.5%	2750 Hz ±1.1%	2750 Hz ±0.6%
Receive signal level	-32 dBm to -14 dBm/tone, off-hook	-40 dBV to -2 dBV/tone, on-hook	-40 dBV to -8 dBV/tone, off-hook
Rejection signal level	≤ -45 dBm	≤ -46 dBV	
Receive tone twist	0 to 6 dB	0 to 7 dB	0 to 7 dB
Tone output time	75 msec to 85 msec	88 msec to 110 msec	80 msec to 85 msec
Simultaneous voice reception	Yes	No	Yes

3.7 Off-Hook Detection

Figure 3.7.1 shows an example of an off-hook detection circuit. Set the MODE1 pin to 1 to detect off-hook status. The example below can detect on-hook/off-hook status even if the device is in the power down mode. The hook status is detected by comparing the voltage values between the HOOK and EXTREF pins. When off-hook (HOOK pin voltage < EXTREF pin voltage) is detected, the #RDET pin outputs 0.

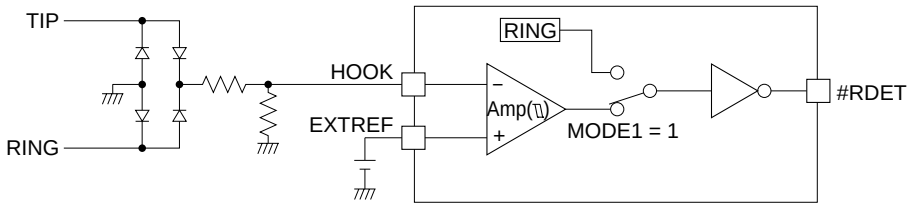


Figure 3.7.1 Off-hook detection circuit

4 Precautions on Mounting

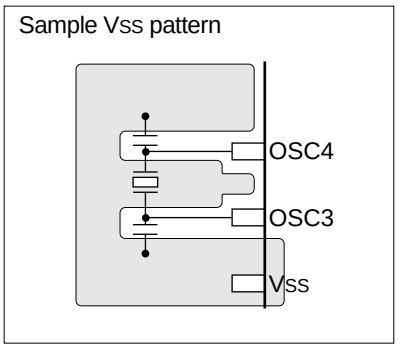
<Oscillation Circuit>

- Oscillation characteristics change depending on conditions (board pattern, components used, etc.). In particular, when a crystal oscillator is used, use the oscillator manufacturer's recommended values for constants such as capacitance.

- Disturbances of the oscillation clock due to noise may cause a malfunction. Consider the following points to prevent this:

  (1) Components which are connected to the OSC3, OSC4 terminals, such as oscillators and capacitors, should be connected in the shortest line.

  (2) As shown in the right hand figure, make a VSS pattern as large as possible at circumscription of the OSC3, OSC4 terminals and the components connected to these terminals.
  Furthermore, do not use this VSS pattern for any purpose other than the oscillation system.



  (3) When supplying an external clock to the OSC3 terminal, the clock source should be connected to the OSC3 terminal in the shortest line.
  Furthermore, do not connect anything else to the OSC4 terminal.

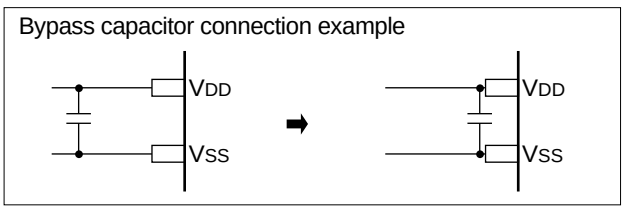
- In order to prevent unstable operation of the oscillation circuit due to current leak between OSC3 and VDD, please keep enough distance between OSC3 and VDD or other signals on the board pattern.

<Power Supply Circuit>

- Sudden power supply variation due to noise may cause malfunction. Consider the following points to prevent this:

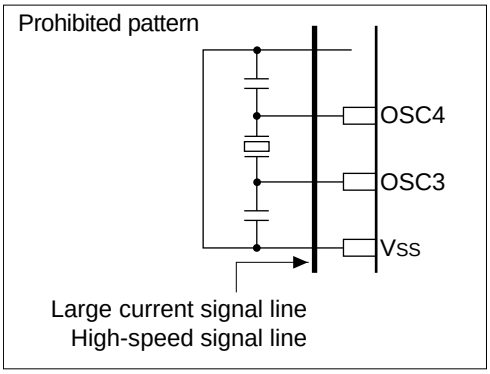
  (1) The power supply should be connected to the VDD, VSS and VREF terminals with patterns as short and large as possible.

  (2) When connecting between the VDD and VSS terminals with a bypass capacitor, the terminals should be connected as short as possible.



<Arrangement of Signal Lines>

- In order to prevent generation of electromagnetic induction noise caused by mutual inductance, do not arrange a large current signal line near the circuits that are sensitive to noise such as the oscillation unit.
- When a signal line is parallel with a high-speed line in long distance or intersects a high-speed line, noise may generated by mutual interference between the signals and it may cause a malfunction.
  Do not arrange a high-speed signal line especially near circuits that are sensitive to noise such as the oscillation unit.



<Precautions for Visible Radiation (when bare chip is mounted)>

- Visible radiation causes semiconductor devices to change the electrical characteristics. It may cause this IC to malfunction. When developing products which use this IC, consider the following precautions to prevent malfunctions caused by visible radiations.

  (1) Design the product and implement the IC on the board so that it is shielded from visible radiation in actual use.

  (2) The inspection process of the product needs an environment that shields the IC from visible radiation.

  (3) As well as the face of the IC, shield the back and side too.

5 Electrical Characteristics

5.1 Absolute Maximum Ratings

Parameter	Symbol	Rated value	Unit
Power supply voltage	V_{DD}	-0.5 to 7	V
Input voltage	V_I	-0.3 to V_{DD}+0.3	V
Total output current	ΣI_{VDD}	±10	mA
Power dissipation	P_D	250	mW
Storage temperature	T_{STG}	-65 to 150	°C
Solder temperature	T_{SOL}	255	°C
Soldering time	t_{SOL}	10	Sec
Operating temperature	T_{OPR}	-20 to 70	°C
Electrostatic withstand voltage	V_E	EIAJ test (C=200pF): 250V or more MIL test (C=100pF, R=1.5kΩ): 1200V or more	V

The voltages are referenced to the V_{SS} pin as the ground level.

5.2 Recommended Operating Conditions

Parameter	Symbol	Condition	Unit
Power supply voltage	V_{DD}	2.7 to 5.5	V
Crystal/clock frequency	f_{CLK}	3.579545	MHz
Crystal/clock frequency error	f_{ERR}	±0.01	%

The voltages are referenced to the V_{SS} pin as the ground level.

5.3 DC Characteristics

Unless otherwise noted: V_{DD}=2.7V to 5.5V, V_{SS}=0V, f_{CLK}=3.579545MHz, Ta=-20 to 70°C

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit
High level input voltage (1)	V_{IH1}		OSC3, MODE0, MODE1, #SCLK, SDI, PDWN, #RESET, EXTCLK	0.8V_{DD}		V_{DD}	V
High level input voltage (2)	V_{IH2}		RDIN, #RDRC	0.7V_{DD}		V_{DD}	V
Low level input voltage (1)	V_{IL1}		OSC3, MODE0, MODE1, #SCLK, SDI, PDWN, #RESET, EXTCLK	0		0.2V_{DD}	V
Low level input voltage (2)	V_{IL2}		RDIN, #RDRC	0		0.3V_{DD}	V
High level input current	I_{IH}	V_{IH}=V_{DD}	RDIN, OSC3, MODE0, MODE1, #SCLK, SDI, PDWN, #RESET, #IRQ, #RDRC (RDIN = Low), EXTCLK	0		0.5	µA
Low level input current	I_{IL}	V_{IL}=V_{SS}	RDIN, OSC3, MODE0, MODE1, #SCLK, SDI, PDWN, #RESET, #RDRC, #IRQ, EXTCLK	-0.5		0	µA
High level output current	I_{OH}	V_{OH}=0.9V_{DD}	SDO, #DET, #RDET, #PQUAL			-1.5	mA
Low level output current	I_{OL}	V_{OL}=0.1V_{DD}	SDO, #DET, #RDET, #PQUAL, #IRQ, #RDRC	2.5			mA
V_{REF} output voltage	V_{REF}				V_{DD}/2		V
Input impedance	R_{IN}		INP, INN, HOOK, EXTREF, CASIN	10			MΩ
	R_{CDIN}		CDIN	140	200	260	kΩ

5.4 Current Consumption

Unless otherwise noted: V_{DD}=2.7V to 5.5V, V_{SS}=0V, f_{CLK}=3.579545MHz, Ta=-20 to 70°C

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit
Current consumption	I_{OP}	Zero-power mode (PDWN=High)	V_{DD}=5V			1.0	µA
		FSK energy detection mode (PDWN=High)	V_{DD}=5V		6.0	8.0	µA
		Power up mode (no signal inputs)	V_{DD}=5V		3.0		mA
			V_{DD}=3V		1.8		mA

5.5 Crystal Oscillation Characteristics

Unless otherwise noted: V_{DD}=2.7V to 5.5V, V_{SS}=0V, C_G=C_D=18pF, Ta=25°C

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start time	tsta	3.579545Mhz oscillator			20	msec

5.6 FSK Demodulation Circuit Characteristics

5.6.1 FSK AC Characteristics

Unless otherwise noted: V_{DD}=5.0/3.0V, V_{SS}=0V, f_{CLK}=3.579545MHz, Ta=-20 to 70°C

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Transfer rate	TRATE		1188	1200	1212	Baud
Bell 202 mark (logic 1) frequency	f_{B1}		1188	1200	1212	Hz
Bell 202 space (logic 0) frequency	f_{B0}		2178	2200	2222	Hz
ITU-T V.23 mark (logic 1) frequency	f_{V1}		1280	1300	1320	Hz
ITU-T V.23 space (logic 0) frequency	f_{V2}		2068	2100	2132	Hz
SN ratio	SNR		20	–	–	dB
Carrier-detect ON sensitivity ∗1 (input level at TPI/RING)	CDONFSK	V_{DD}=5V	-45.0	-43.0	-41.0	dBm
		Input amp gain (G_{AMP})=-5dB	-47.2	-45.2	-43.2	dBV
		V_{DD}=3V	-45.0	-43.0	-41.0	dBm
		Input amp gain (G_{AMP})=-9.4dB	-47.2	-45.2	-43.2	dBV
Carrier-detect OFF sensitivity ∗1	CDOFFFSK	V_{DD}=5V	-47.0	-45.0	-43.0	dBm
		Input amp gain (G_{AMP})=-5dB	-49.2	-47.2	-45.2	dBV
		V_{DD}=3V	-47.0	-45.0	-43.0	dBm
		Input amp gain (G_{AMP})=-9.4dB	-49.2	-47.2	-45.2	dBV

∗1 When the gain in the input amp is set to G_{AMP} (dB), the CDONFSK and CDOFFFSK values (Typ.) can be calculated from the equation below.

$$CD_{ONFSK}\ [dBm] = -G_{AMP} - 48.0 + 20\log(\frac{V_{DD}}{5})\ [dBm], \quad CD_{ONFSK}\ [dBV] = -G_{AMP} - 50.2 + 20\log(\frac{V_{DD}}{5})\ [dBV]$$

$$CD_{OFFFSK}\ [dBm] = -G_{AMP} - 50.0 + 20\log(\frac{V_{DD}}{5})\ [dBm], \quad CD_{OFFFSK}\ [dBV] = -G_{AMP} - 52.2 + 20\log(\frac{V_{DD}}{5})\ [dBV]$$

5.6.2 FSK Switching Characteristics

Unless otherwise noted: V_{DD}=5.0/3.0V, V_{SS}=0V, f_{CLK}=3.579545MHz, Ta=-20 to 70°C, C_L=50pF

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
PDWN fall → FSK	tSUPD				20	msec
Carrier detect start time	tCDON		5	10	15	msec
Data end → #DET rise	tCDOFF		5	10	15	msec
PDWN rise → Oscillation start	tDOCH	V_{DD}=5V		7	12	msec
		V_{DD}=3V		10	15	msec

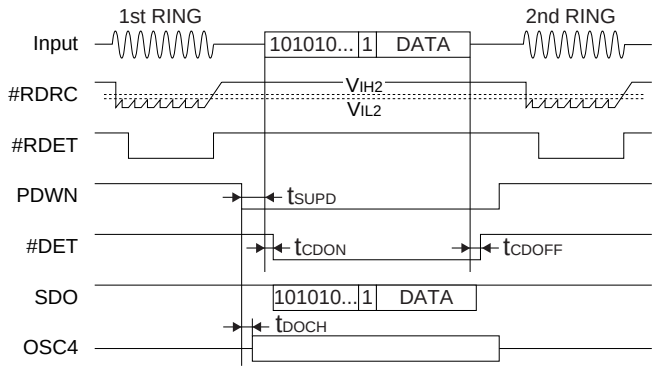


Figure 5.6.1 FSK switching characteristics

5.6.3 FSK Energy Detection Mode AC Characteristics

Unless otherwise noted: V_{DD}=5.0/3.0V, V_{SS}=0V, f_{CLK}=3.579545MHz, Ta=-20 to 70°C

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Transfer rate	TRATE		1188	1200	1212	Baud
Bell 202 mark (logic 1) frequency	f_{B1}		1188	1200	1212	Hz
Bell 202 space (logic 0) frequency	f_{B0}		2178	2200	2222	Hz
ITU-T V.23 mark (logic 1) frequency	f_{V1}		1280	1300	1320	Hz
ITU-T V.23 space (logic 0) frequency	f_{V2}		2068	2100	2132	Hz
SN ratio	SNR		20	–	–	dB
Carrier-detect ON sensitivity ∗1 (input level at TPI/RING)	CDONFSK	V_{DD}=5V	-44.0	-41.0	-38.0	dBm
		Input amp gain (GAMP)=-5dB	-46.2	-43.2	-40.2	dBV
		V_{DD}=3V	-44.0	-41.0	-38.0	dBm
		Input amp gain (GAMP)=-9.4dB	-46.2	-43.2	-40.2	dBV

∗1 When the gain in the input amp is set to GAMP (dB), the CDONFSK value (Typ.) can be calculated from the equation below.

$$CD_{ONFSK}\ [dBm] = -G_{AMP} - 46.0 + 20\log(\frac{V_{DD}}{5})\ [dBm], \quad CD_{ONFSK}\ [dBV] = -G_{AMP} - 48.2 + 20\log(\frac{V_{DD}}{5})\ [dBV]$$

5.6.4 FSK Energy Detection Mode Switching Characteristics

Unless otherwise noted: V_{DD}=5.0/3.0V, V_{SS}=0V, f_{CLK}=3.579545MHz, Ta=-20 to 70°C, C_L=50pF

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
FSK energy detect capture time	t_{EGAQ}	V_{DD}=5V		12	20	msec
FSK end → #IRQ rise	t_{EGIH}	V_{DD}=5V		24	40	msec

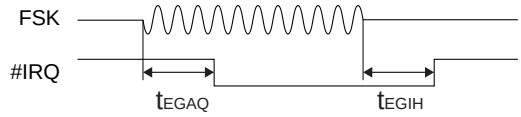


Figure 5.6.2 FSK energy detection mode switching characteristics

5.7 Dual-Tone (CAS) Detection Circuit Characteristics

5.7.1 CAS AC Characteristics

Unless otherwise noted: V_{DD}=5.0/3.0V, V_{SS}=0V, f_{CLK}=3.579545MHz, Ta=-20 to 70°C

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Carrier-detect sensitivity ∗1 (input level at TPI/RING)	CDONTONE	VDD=5V, Bellcore mode Input amp gain (GAMP)=-5dB Tone filter gain=-4dB	-39.9	-35.9	-31.9	dBm
		VDD=5V, BT mode ∗2 nput amp gain (GAMP)=-5dB Tone filter gain=-4dB	-48.1	-44.1	-40.1	dBV
		VDD=3V, BT mode ∗2 nput amp gain (GAMP)=-9.4dB Tone filter gain=-4dB	-39.9	-35.9	-31.9	dBm
		VDD=3V, BT mode ∗2 nput amp gain (GAMP)=-9.4dB Tone filter gain=-4dB	-48.1	-44.1	-40.1	dBV
Low tone frequency	fLTONE	Bellcore (±0.5%)	2119.35	2130	2140.65	Hz
		BT line disconnected	2110	2130	2150	Hz
		BT line connected (±0.6%)	2117.22	2130	2142.78	Hz
High tone frequency	fHTONE	Bellcore (±0.5%)	2736.25	2750	2763.75	Hz
		BT line disconnected	2720	2750	2780	Hz
		BT line connected (±0.6%)	2733.50	2750	2766.50	Hz

∗1 When the gain in the input amp is set to GAMP (dB), the CDONTONE value (Typ.) can be calculated from the equation below.
(When the internal tone filter gain = –4 dB)

$$CD_{ONTONE}\ [dBm] = -G_{AMP} - 40.9 + 20\log\left(\frac{V_{DD}}{5}\right)\ [dBm],\quad CD_{ONTONE}\ [dBV] = -G_{AMP} - 49.1 + 20\log\left(\frac{V_{DD}}{5}\right)\ [dBV]$$

∗2 BT mode is selected by setting the mode register (address = 0h) bit 2 to 1. By this setting, the gain in each dual-tone filter is raised +6 dB for adjustment to the British Telecom CD level.

5.7.2 CAS Switching Characteristics

Unless otherwise noted: V_{DD}=5.0/3.0V, V_{SS}=0V, f_{CLK}=3.579545MHz, Ta=-20 to 70°C, C_L=50pF

Parameter	Symbol	Min.	Typ.	Max.	Unit
CAS detect capture time	t_{CASAQ}		2.8×(N+2)+16.9		msec
CAS end → #DET rise	t_{CASDH}		2.8×(31-N)+13.1		msec
CAS width	t_{CASW}	75	80	85	msec

N = TH0 × 16 + TL3 × 8 + TL2 × 4 + TL1 × 2 + TL0

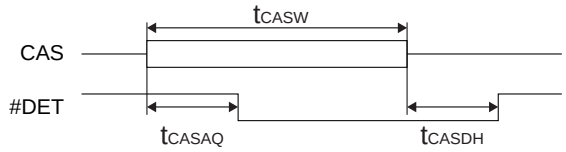


Figure 5.7.1 CAS switching characteristics

5.8 Call Progress Mode (CPM) Detection Circuit Characteristics

5.8.1 CPM AC Characteristics

Unless otherwise noted: V_{DD}=5.0/3.0V, V_{SS}=0V, f_{CLK}=3.579545MHz, Ta=-20 to 70°C

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Carrier-detect ON sensitivity ∗1 (input level at TPI/RING)	CD_{ONCPM}	V_{DD}=5V	-45.0	-43.0	-41.0	dBm
		Input amp gain (G_{AMP})=-5dB	-47.2	-45.2	-43.2	dBV
		V_{DD}=3V	-45.0	-43.0	-41.0	dBm
		Input amp gain (G_{AMP})=-9.4dB	-47.2	-45.2	-43.2	dBV
Carrier-detect OFF sensitivity ∗1	CD_{OFFCPM}	V_{DD}=5V	-47.0	-45.0	-43.0	dBm
		Input amp gain (G_{AMP})=-5dB	-49.2	-47.2	-45.2	dBV
		V_{DD}=3V	-47.0	-45.0	-43.0	dBm
		Input amp gain (G_{AMP})=-9.4dB	-49.2	-47.2	-45.2	dBV

∗1 When the gain in the input amp is set to G_{AMP} (dB), the CD_{ONCPM} and CD_{OFFCPM} values (Typ.) can be calculated from the equation below.

$$CD_{ONCPM}\ [dBm] = -G_{AMP} - 48.0 + 20\log(\frac{V_{DD}}{5})\ [dBm], \quad CD_{ONCPM}\ [dBV] = -G_{AMP} - 50.2 + 20\log(\frac{V_{DD}}{5})\ [dBV]$$

$$CD_{OFFCPM}\ [dBm] = -G_{AMP} - 50.0 + 20\log(\frac{V_{DD}}{5})\ [dBm], \quad CD_{OFFCPM}\ [dBV] = -G_{AMP} - 52.2 + 20\log(\frac{V_{DD}}{5})\ [dBV]$$

5.8.2 CPM Switching Characteristics

Unless otherwise noted: V_{DD}=5.0/3.0V, V_{SS}=0V, f_{CLK}=3.579545MHz, Ta=-20 to 70°C, C_L=50pF

Parameter	Symbol	Min.	Typ.	Max.	Unit
CPM tone-detect capture time	t_{CPMAQ}		25		msec
CPM tone end → #IRQ rise	t_{CPMIH}		30		msec

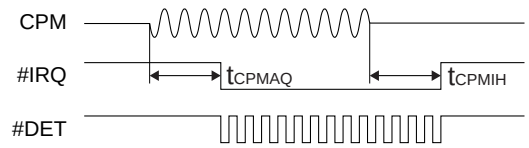


Figure 5.8.1 CPM switching characteristics

5.9 Serial Interface Circuit Characteristics

5.9.1 Serial Interface AC Characteristics

Unless otherwise noted: V_{DD}=5.0/3.0V, V_{SS}=0V, f_{CLK}=3.579545MHz, Ta=-20 to 70°C, C_L=50pF

Parameter	Symbol	Min.	Typ.	Max.	Unit
#SCLK frequency	f_{SCLK}			1	MHz
#SCLK pulse width	t_{WSCLK}	400			nsec
SDI setup time	t_{SSDI}	250			nsec
SDI hold time	t_{HSDI}	500			nsec
SDO delay time	t_{DSDO}			250	nsec
MODE0 High setup time	t_{SMH}	1			µsec
MODE0 High hold time	t_{HMH}	1			µsec
MODE0 Low setup time	t_{SML}	1			µsec
MODE0 Low hold time	t_{HML}	1			µsec
MODE0 Low pulse width	t_{MDW}	1			µsec

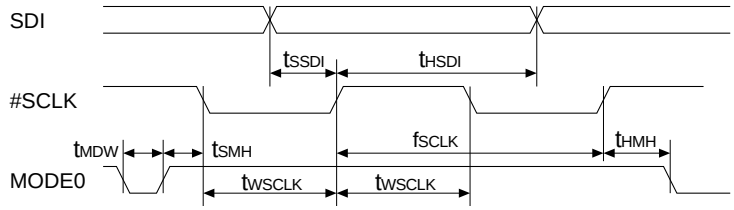


Figure 5.9.1 Serial interface input timing

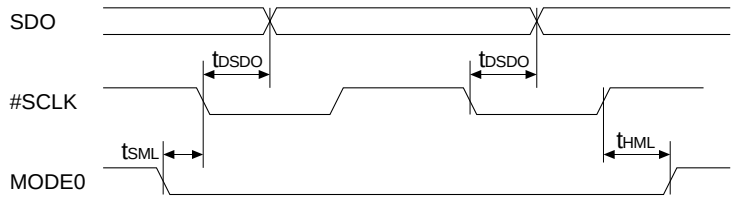


Figure 5.9.2 Serial interface output timing

5.9.2 FSK Demodulated Data Read Mode

The FSK signal fed to the INP and INN pins is demodulated into 8-bit asynchronous (start-stop) data. The demodulated data is then sampled by the internal 8-bit shift register. When the data has been stored in the shift register, the #IRQ pin changes to Low level, indicating that the data can be read by the host CPU.
If the MODE pin is set to Low level and synchronous mode has been selected (MDR[0] = 1), the host CPU reads out the 8-bit data synchronously with the clock signal fed from the host CPU to the #SCLK pin. Figure 5.9.3 shows the timing at which this data is read. Each bit of the 8-bit data is output from the SDO pin synchronously with falling edges of the #SCLK clock signal, beginning with bit 0. The host CPU latches each bit into the internal logic at rising edges of the #SCLK clock signal.
If the MODE pin is set to Low level and asynchronous mode has been set (MDR[0] = 0), the data is output from the SDO pin at a transfer rate of 1,200 baud. The clock signal from the host CPU is unnecessary. The host CPU latches the data synchronously with the start bit.

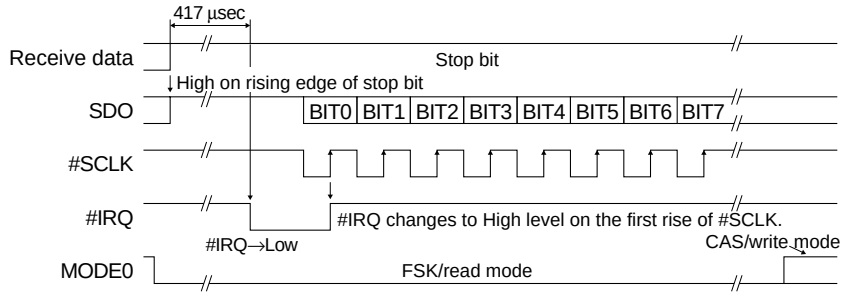


Figure 5.9.3 Data read timing in synchronous mode

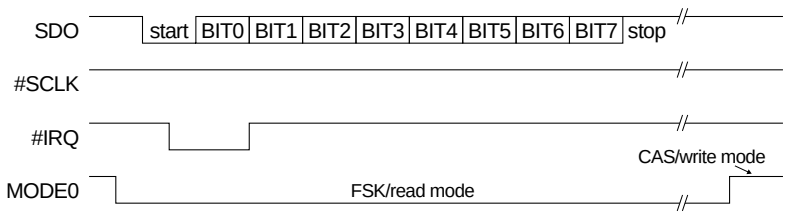


Figure 5.9.4 Data read timing in asynchronous mode

5.9.3 CAS Detection Circuit Control-Register Write Mode

The host CPU can write 4-bit data to the internal registers through the SDI pin in order to set each control bit. The host CPU must temporarily pull the MODE pin to Low level to initialize the write control circuit before it can write data. Then, after releasing the MODE pin back to High level, the host CPU must be held at High level while writing data to the internal register. The data input to the SDI pin is sampled at rising edges of the clock signal fed from the host CPU to the #SCLK pin. The first four bits of data sent from the host CPU are the address A[3:0] of the internal register to be accessed. The subsequent four bits are the data bits D[3:0] to be written to the specified register. The data is input beginning with the LSB.

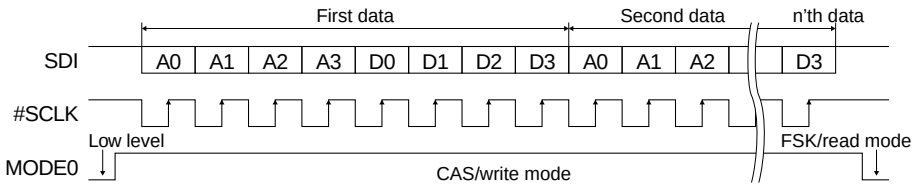


Figure 5.9.5 Data write timing

5.10 E0C5251 Timing Chart

5.10.1 Bellcore On-Hook Data Transfer

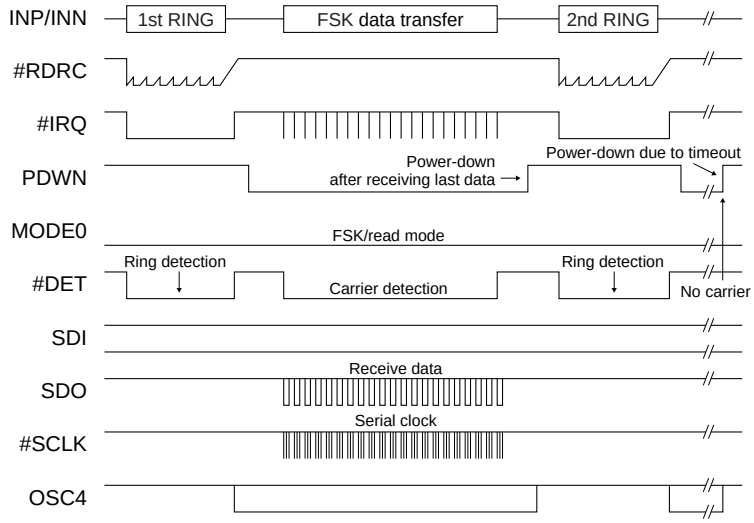


Figure 5.10.1 Bellcore on-hook data transfer timing chart

5.10.2 Bellcore Off-Hook Data Transfer

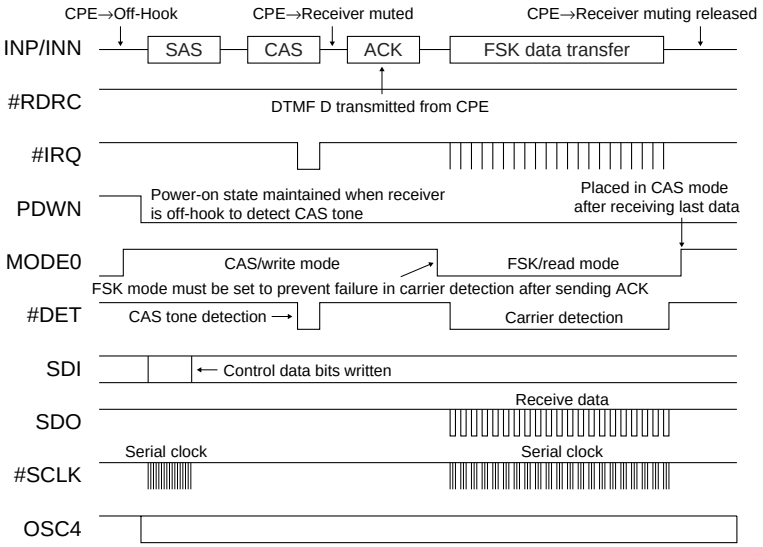


Figure 5.10.2 Bellcore off-hook data transfer timing chart

5.10.3 BT Idle State CLI Service

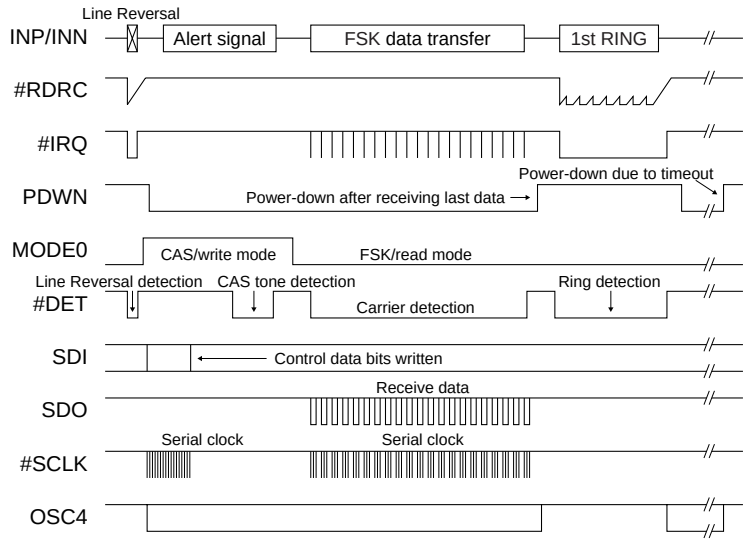


Figure 5.10.3 BT Idle State CLI service timing chart

5.10.4 BT Loop State CLI Service

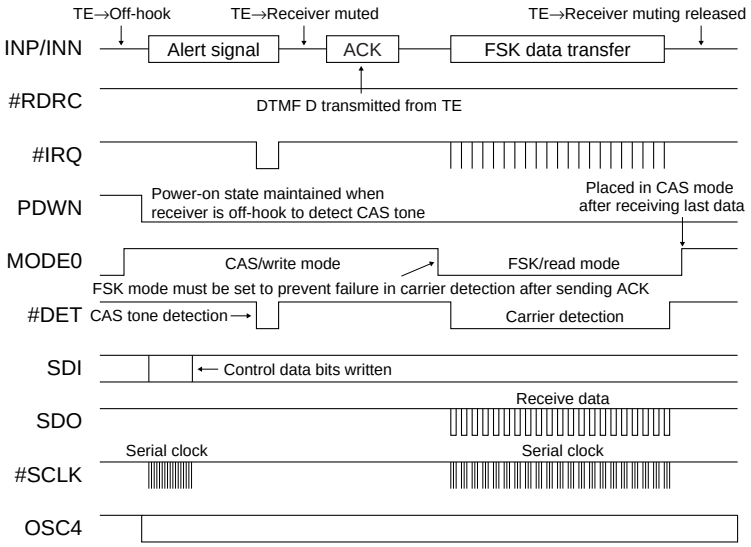


Figure 5.10.4 BT Loop State CLI service timing chart

5.11 External Wiring Diagram (Example)

5.11.1 Example of Bellcore-Compatible Telephone Circuit

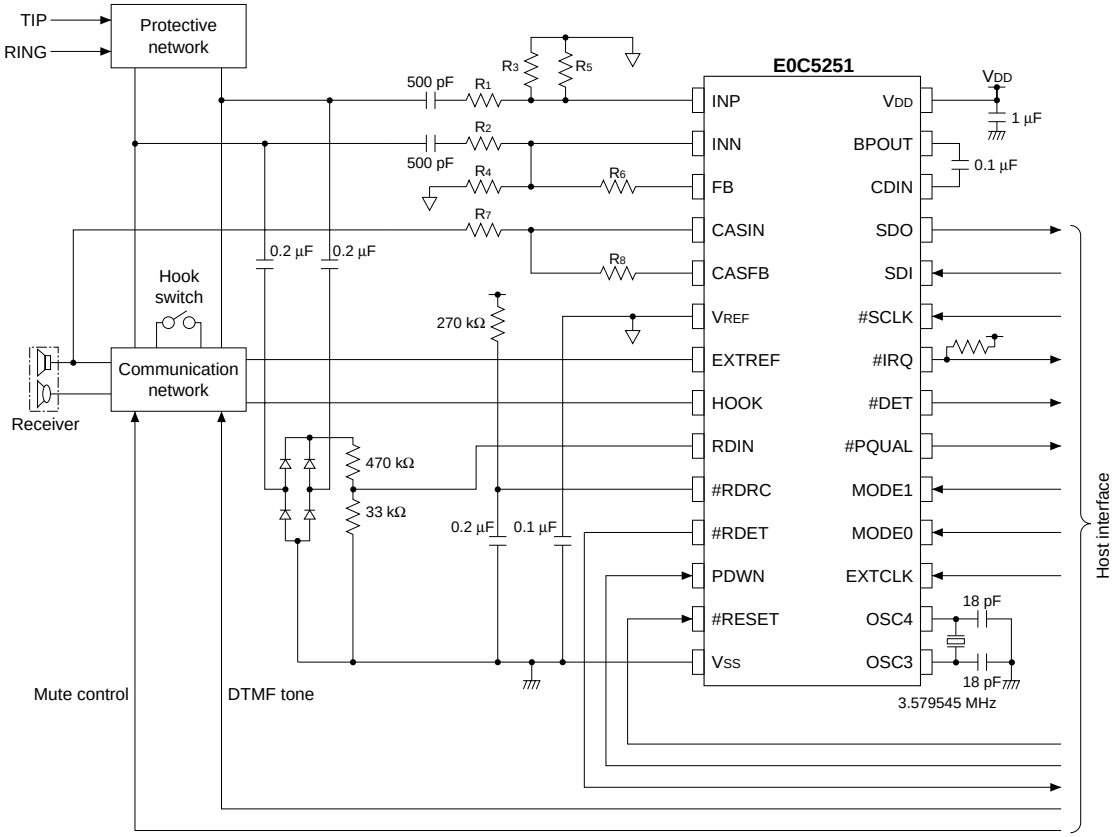


Figure 5.11.1 Example of Bellcore-compatible telephone circuit

Note: The above circuit diagram is merely an example, and does not guarantee the operation of the circuit.

∗ See Section 3.3, "Input Amp Circuit", for the R1 to R8 values.

5.11.2 Example of Bellcore-Compatible Auxiliary Circuit

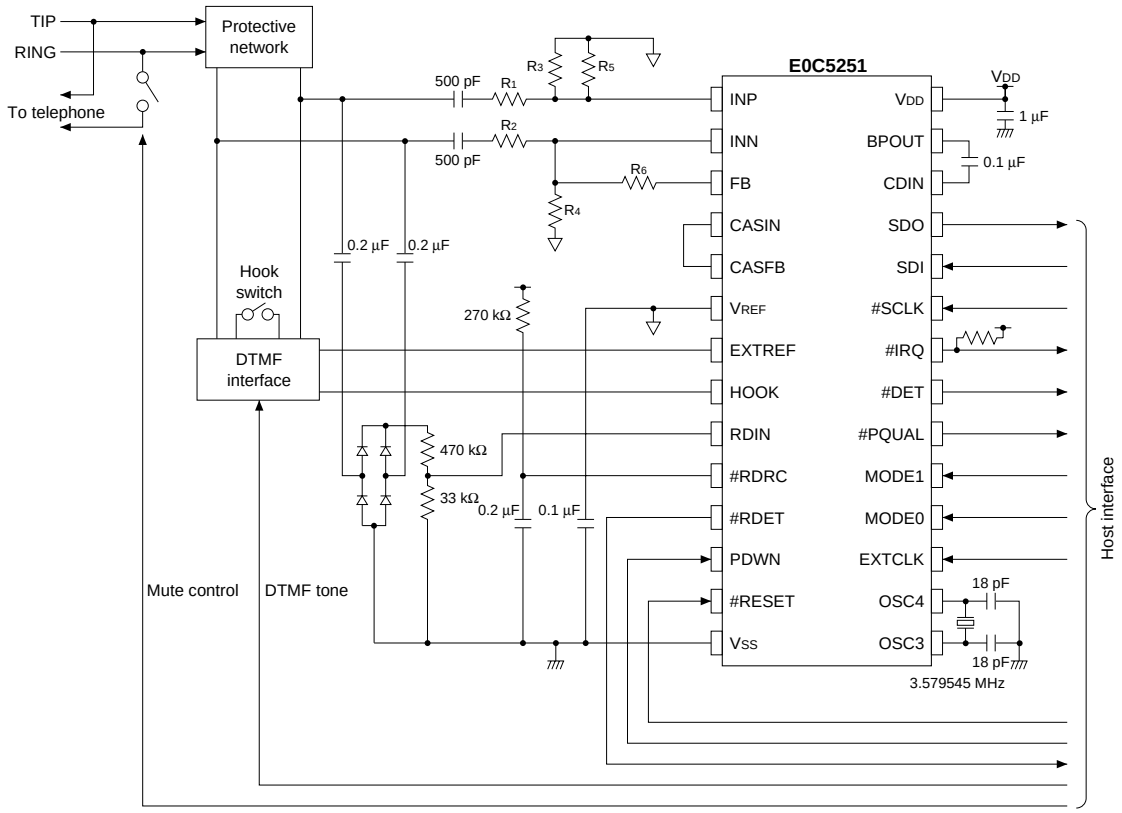


Figure 5.11.2 Example of Bellcore-compatible auxiliary circuit

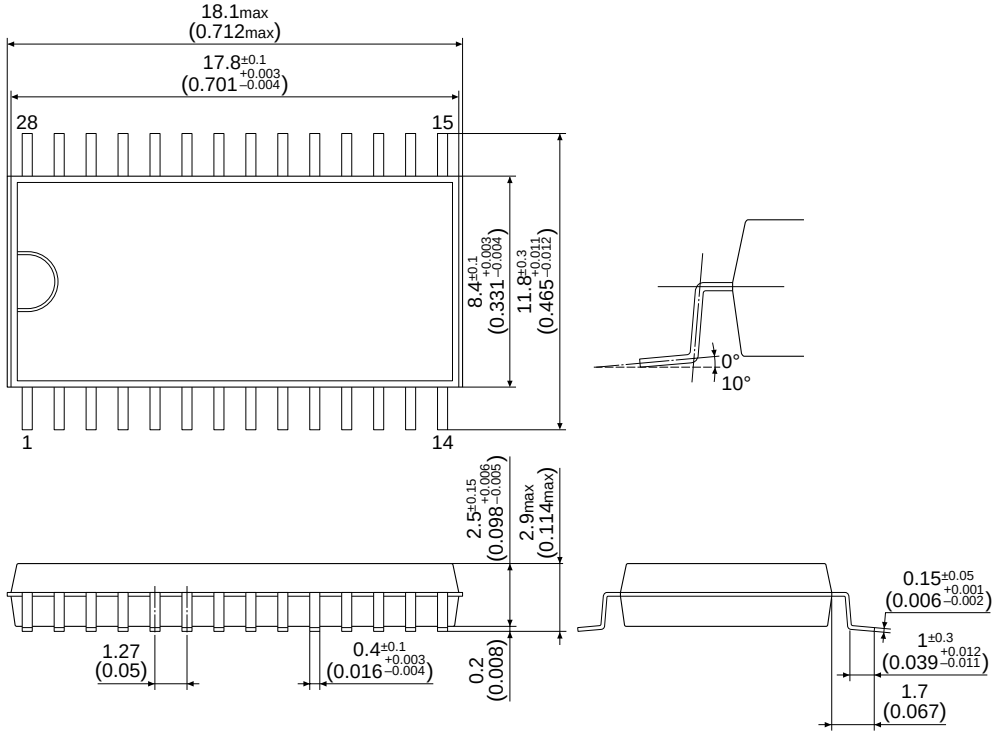
Note: The above circuit diagram is merely an example, and does not guarantee the operation of the circuit.

∗ See Section 3.3, "Input Amp Circuit", for the R1 to R6 values.

6 Package

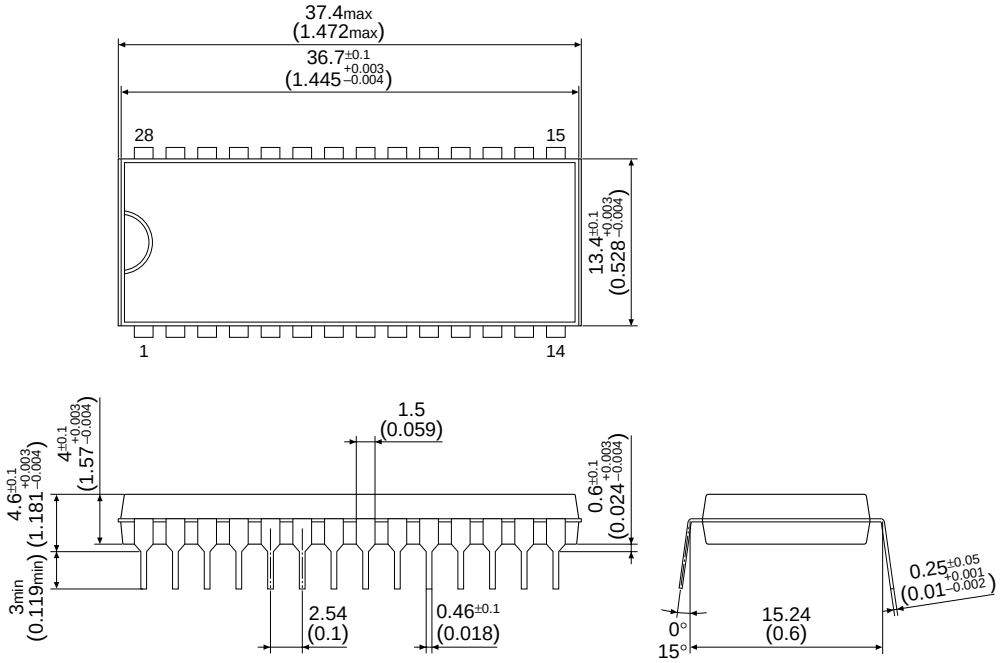
SOP2-28pin Plastic Package

Unit: mm (inch)



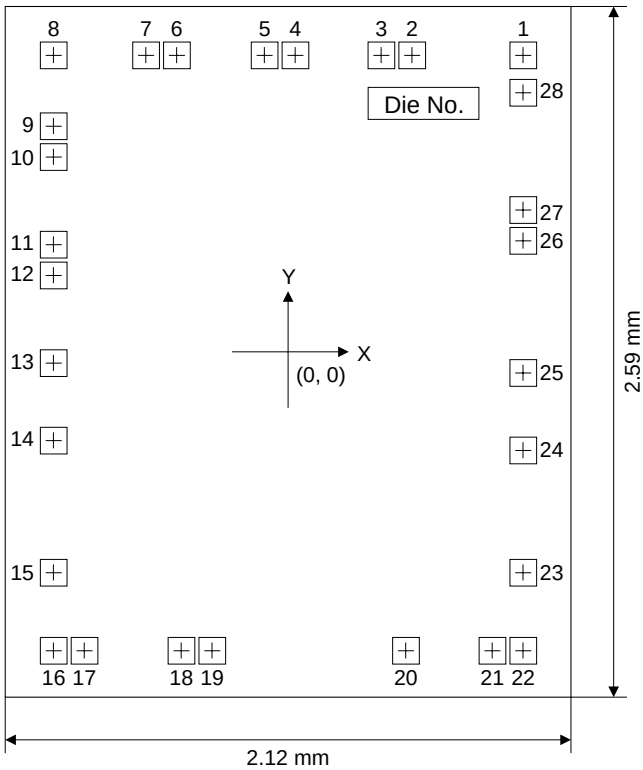
DIP-28pin Ceramic Package

Unit: mm (inch)



7 Pad Layout

7.1 Pad Layout Diagram



Chip thickness: 400 µm
Pad opening: 100 µm

7.2 Pad Coordinates

(Unit: µm)

Pad No.	Pad name	X coordinate	Y coordinate	Pad No.	Pad name	X coordinate	Y coordinate
1	SD0	879.9	1116.3	15	#RDET	-879.8	-823.8
2	CDIN	463.7	1116.3	16	PDWN	-879.8	-1116.4
3	BPOUT	348.2	1116.3	17	#RESET	-764.3	-1116.4
4	V_{DD}	26.1	1116.3	18	V_{SS}	-401.0	-1116.4
5	INP	-89.4	1116.3	19	OSC3	-285.5	-1116.4
6	INN	-418.1	1116.3	20	OSC4	440.3	-1116.4
7	FB	-533.6	1116.3	21	EXTCLK	764.4	-1116.4
8	CASIN	-879.8	1116.3	22	MODE0	879.9	-1116.4
9	CASFB	-879.8	850.5	23	MODE1	879.9	-823.8
10	V_{REF}	-879.8	735.0	24	#PQUAL	879.9	-365.3
11	EXTREF	-879.8	406.4	25	#DET	879.9	-74.7
12	HOOK	-879.8	290.9	26	#IRQ	879.9	420.8
13	RDIN	-879.8	-37.8	27	#SCLK	879.9	536.3
14	#RDRC	-879.8	-328.4	28	SDI	879.9	976.1

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