MF1085-01a

EPSON

CMOS 4-BIT SINGLE CHIP MICROCOMPUTER

E0C63158 TECHNICAL MANUAL

E0C63158 Technical Hardware

SEIKO EPSON CORPORATION

CONTENTS

CHAPTER 1 OUTLINE

The E0C63158 is a microcomputer which has a high-performance 4-bit CPU E0C63000 as the core CPU, ROM (8,192 words × 13 bits), RAM (512 words × 4 bits), serial interface, watchdog timer, programmable timer, time base counter (1 system), SVD circuit, a 4-channel A/D converter and a special input port that can implement key position discrimination function using with the A/D converter. The E0C63158 features low voltage/high speed (4 MHz Max.) operation and low current consumption (2 µA Typ. in HALT mode), this makes it suitable for battery driven portable equipment such as a head phone stereo.

1.1 Features

OSC1 oscillation circuit	32.768 kHz (Typ.) Crystal oscillation circuit or CR oscillation circuit (∗1)
OSC3 oscillation circuit	2 MHz (Typ.) CR or Ceramic oscillation circuit (∗1)
Instruction set	Basic instruction: 46 types (411 instructions with all) Addressing mode: 8 types
Instruction execution time	During operation at 32.768 kHz: Min. 61 µsec During operation at 4 MHz: Min. 0.5 µsec
ROM capacity	Code ROM: 8,192 words × 13 bits
RAM capacity	Data memory: 512 words × 4 bits
Input port	9 bits 8 bits (Pull-up resistors may be supplemented ∗1) 1 bit (Input interrupt for key position sensing by A/D)
Output port	12 bits (It is possible to switch the 2 bits to special output ∗2)
I/O port	20 bits (It is possible to switch the 4 bits to serial input/output ∗2) (It is possible to switch the 4 bits to A/D input ∗2)
Serial interface	1 port (8-bit clock synchronous system)
Time base counter	1 system (Clock timer)
Programmable timer	Built-in, 2 channels × 8 bits, with event counter function or 1 channel × 16 bits (∗2)
Watchdog timer	Built-in
A/D converter	8-bit resolution Maximum error: ±3 LSB, A/D clock: Max. 1MHz (0.9 to 3.6 V, VC2 mode should be set when the supply voltage is 1.6 V or less.)
Buzzer output	Buzzer frequency: 2 kHz or 4 kHz (∗2), 2 Hz interval (∗2)
Supply voltage detection (SVD) circuit	16 values, programmable (1.05 V to 2.60 V)
External interrupt	Input port interrupt: 2 systems Key sensing interrupt: 1 system
Internal interrupt	Clock timer interrupt: 4 systems Programmable timer interrupt: 2 systems Serial interface interrupt: 1 system A/D converter: 1 system
Power supply voltage	0.9 V to 3.6 V
Operating temperature range	-20°C to 70°C
Current consumption (Typ.)	Single clock: During HALT (32 kHz) 1.5 V (normal mode) 2 µA During operation (32 kHz) 1.5 V (normal mode) 4 µA Twin clock: During operation (4 MHz) 3.0 V (normal mode) 900 µA
Package	QFP12-48pin, QFP13-64pin (plastic) or chip

∗1: Can be selected with mask option
∗2: Can be selected with software

1.2 Block Diagram

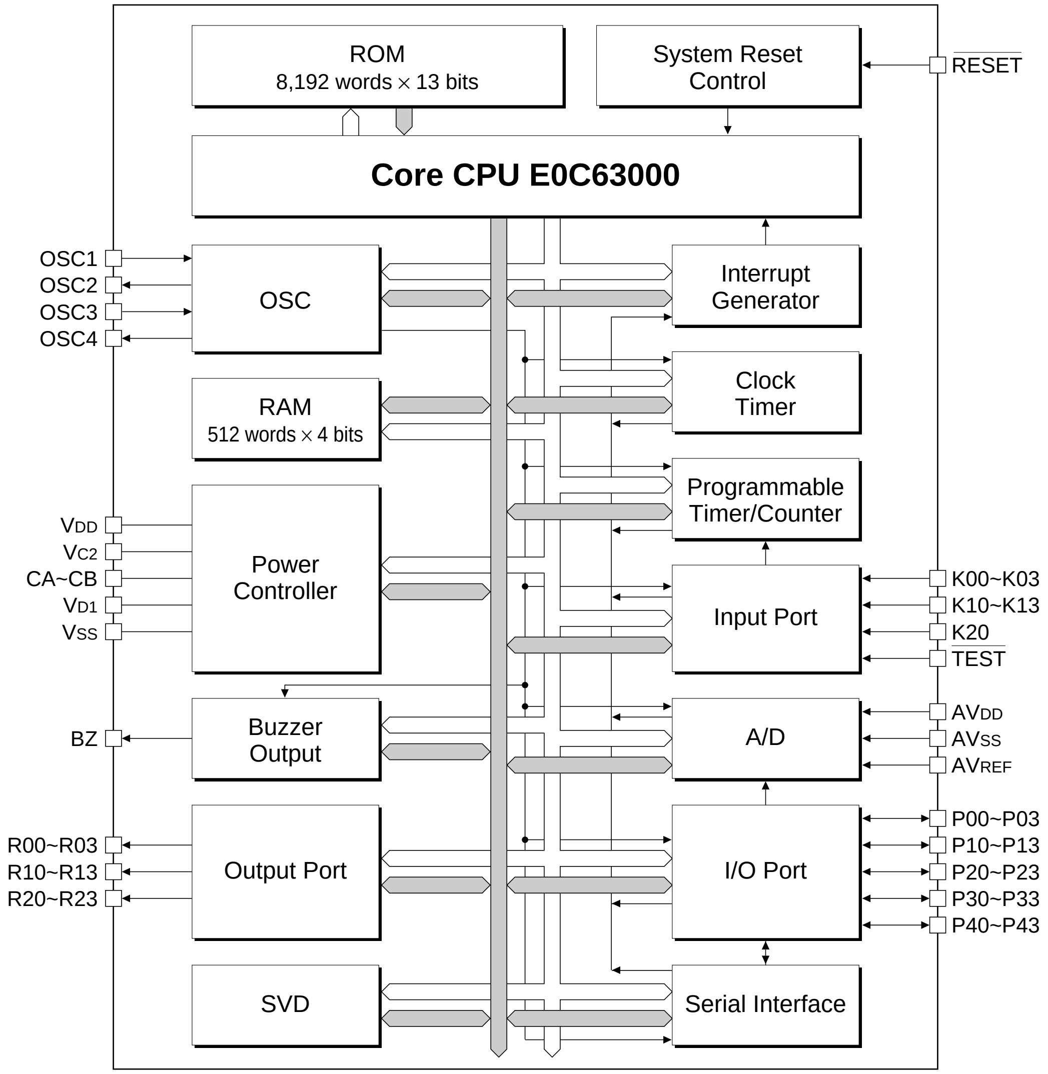
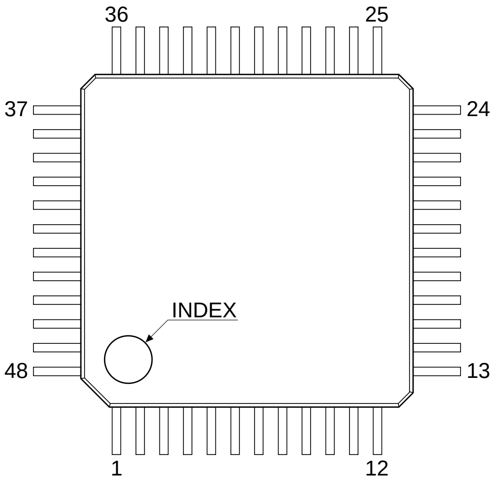


Fig. 1.2.1 Block diagram

1.3 Pin Layout Diagram

QFP12-48pin

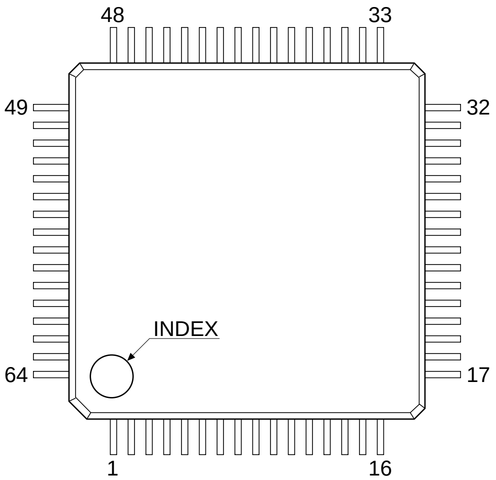


No.	Pin name	No.	Pin name	No.	Pin name	No.	Pin name
1	V_{SS}	13	V_{C2}	25	P10	37	R01
2	OSC1	14	P43	26	P03	38	R00
3	OSC2	15	P42	27	P02	39	BZ
4	V_{D1}	16	P41	28	P01	40	K00
5	OSC3	17	P40	29	P00	41	K01
6	OSC4	18	P23	30	R13	42	K02
7	V_{DD}	19	P22	31	R12	43	K03
8	$\overline{RESET}$	20	P21	32	R11	44	K10
9	$\overline{TEST}$	21	P20	33	R10	45	K11
10	AV_{REF}	22	P13	34	R03	46	K12
11	CB	23	P12	35	R02	47	K13
12	CA	24	P11	36	N.C.	48	K20

N.C.: No Connection

Fig. 1.3.1 Pin layout diagram (QFP12-48pin)

QFP13-64pin



No.	Pin name	No.	Pin name	No.	Pin name	No.	Pin name
1	V_{SS}	17	P43	33	P03	49	N.C.
2	OSC1	18	P42	34	P02	50	N.C.
3	OSC2	19	P41	35	P01	51	N.C.
4	V_{D1}	20	P40	36	P00	52	R01
5	OSC3	21	P33	37	R23	53	R00
6	OSC4	22	P32	38	R22	54	BZ
7	V_{DD}	23	P31	39	R21	55	K00
8	$\overline{RESET}$	24	P30	40	R20	56	K01
9	$\overline{TEST}$	25	P23	41	R13	57	K02
10	AV_{DD}	26	P22	42	R12	58	K03
11	AV_{SS}	27	P21	43	R11	59	K10
12	AV_{REF}	28	P20	44	R10	60	K11
13	CB	29	P13	45	R03	61	K12
14	CA	30	P12	46	R02	62	K13
15	V_{C2}	31	P11	47	N.C.	63	K20
16	N.C.	32	P10	48	N.C.	64	N.C.

N.C.: No Connection

Fig. 1.3.2 Pin layout diagram (QFP13-64pin)

1.4 Pin Description

Table 1.4.1 Pin description

Pin name	Pin No.		In/Out	Function
	QFP12-48	QFP13-64		
VDD	7	7	–	Power (+) supply pin
VSS	1	1	–	Power (–) supply pin
VD1	4	4	–	Oscillation/internal logic system regulated voltage output pin
VC2	13	15	–	Booster power supply pin
CA, CB	12, 11	14, 13	–	Boosting capacitor connecting pin
OSC1	2	2	I	Crystal or CR oscillation input pin (selected by mask option)
OSC2	3	3	O	Crystal or CR oscillation output pin (selected by mask option)
OSC3	5	5	I	CR or ceramic oscillation input pin (selected by mask option)
OSC4	6	6	O	CR or ceramic oscillation output pin (selected by mask option)
K00–K03	40–43	55–58	I	Input port
K10–K13	44–47	59–62	I	Input port
K20	48	63	I	Input port (key-position detect interrupt port)
P00–P03	29–26	36–33	I/O	I/O port
P10–P13	25–22	32–29	I/O	I/O port (switching to serial I/F input/output is possible by software)
P20–P23	21–18	28–25	I/O	I/O port
P30–P33 *1	–	24–21	I/O	I/O port
P40–P43	17–14	20–17	I/O	I/O port (can be used as A/D converter inputs)
R00	38	53	O	Output port
R01	37	52	O	Output port
R02	35	46	O	Output port (switching to TOUT output is possible by software)
R03	34	45	O	Output port (switching to FOUT output is possible by software)
R10–R13	33–30	44–41	O	Output port
R20–R23 *1	–	40–37	O	Output port
AVDD *2	–	10	–	Power (+) supply pin for A/D converter
AVSS *2	–	11	–	Power (–) supply pin for A/D converter
AVREF	10	12	–	Reference voltage for A/D converter
BZ	39	54	O	Buzzer output pin
$\overline{\text{RESET}}$	8	8	I	Initial reset input pin
$\overline{\text{TEST}}$	9	9	I	Testing input pin

∗1: P30–P33 and R20–R23 are not available in the QFP12-48pin package.
∗2: In the QFP12-48pin package, AVDD and AVSS are connected with VDD and VSS inside of the IC, respectively.

1.5 Mask Option

Mask options shown below are provided for the E0C63158. Several hardware specifications are prepared in each mask option, and one of them can be selected according to the application. The function option generator FOG63158 that has been prepared as the development software tool of E0C63158, is used for this selection. Mask pattern of the IC is finally generated based on the data created by the FOG63158. Refer to the "E0C63158 Development Tool Manual" for the FOG63158.

<Functions selectable with E0C63158 mask options>

(1) Shipping form

A plastic package (QFP12-48pin or QFP13-64pin) or chip form may be selected.

(2) External reset by simultaneous LOW input to the input port (K00–K03)

This function resets the IC when several keys are pressed simultaneously. The mask option is used to select whether this function is used or not. Further when the function is used, a combination of the input ports (K00–K03), which are connected to the keys to be pressed simultaneously, can be selected. Refer to Section 2.2.2, "Simultaneous low input to terminals K00–K03", for details.

(3) Time authorize circuit for the simultaneous LOW input reset function

When using the external reset function (shown in 2 above), using the time authorize circuit or not can be selected by the mask option. The reset function works only when the input time of simultaneous LOW is more than the rule time if the time authorize circuit is being used.
Refer to Section 2.2.2, "Simultaneous low input to terminals K00–K03", for details.

(4) Input port pull-up resistor

The mask option is used to select whether the pull-up resistor is supplemented to the input ports or not. It is possible to select for each bit of the input ports.
Refer to Section 4.5.3, "Mask option", for details.

(5) Output specification of the output port

Either complementary output or N-channel open drain output may be selected as the output specification of the output ports. The selection is done in 1-bit units or 4-bit units according to the output port.
1-bit unit: R00, R01, R02, R03
4-bit unit: R10–R13, R20–R23

Refer to Section 4.6.2, "Mask option", for details.

(6) Output specification / pull-up resistor of the I/O ports

Either complementary output or N-channel open drain output may be selected as the output specification when the I/O ports are in the output mode. Furthermore, whether or not the pull-up resistors working in the input mode are supplemented can be selected. These selections are done in 1-bit units or 4-bit units according to the I/O port.

1-bit unit: P20, P21, P22, P23, P40, P41, P42, P43
4-bit unit: P00–P03, P10–P13, P30–P33

Refer to Section 4.7.2, "Mask option", for details.

(7) Synchronous clock polarity in the serial interface

The polarity of the synchronous clock $\overline{\text{SCLK}}$ and the $\overline{\text{SRDY}}$ signal in slave mode of the serial interface is selected by the mask option. Either positive polarity or negative polarity can be selected.
Refer to Section 4.11.2, "Mask option", for details.

(8) Polarity of the buzzer output signal

It is possible to select the polarity of the buzzer signal output from the BZ terminal. Select either positive polarity or negative polarity according to the external drive transistor to be used.
Refer to Section 4.12.2, "Mask option", for details.

(9) OSC1 oscillation frequency

Either crystal oscillation circuit or CR oscillation circuit may be selected as the OSC1 oscillation circuit. Refer to Section 4.4.2, "OSC1 oscillation circuit", for details.

(10) OSC3 oscillation circuit

Either CR oscillation circuit or ceramic oscillation circuit may be selected as the OSC3 oscillation circuit. It is also possible to disable the OSC3 oscillation circuit by selecting "Not used".
Refer to Section 4.4.3, "OSC3 oscillation circuit", for details.

CHAPTER 2 POWER SUPPLY AND INITIAL RESET

2.1 Power Supply

The E0C63158 operating power voltage is as follows:

0.9 V to 3.6 V

Note: • *When a voltage within 0.9 V to 1.35 V is used as the operating power voltage, software control is necessary (see Section 4.2).*

The E0C63158 operates by supplying a single power source voltage within the above range between VDD/AVDD and VSS/AVSS. The E0C63158 itself generates the voltage necessary for all the internal circuits by the built-in power supply circuits shown in Table 2.1.1.

Table 2.1.1 Power supply circuits

Circuit	Power supply circuit	Output voltage
Oscillation and internal circuits	Oscillation sysrem voltage regulator	VD1
Oscillation sysrem voltage regulator	Supply voltage (VDD) or voltage booster circuit (VC2)	VDD or VC2
A/D converter	Analog supply voltage (AVDD) and supply voltage (VDD) or voltage booster circuit (VC2)	AVDD and VDD or VC2

Note: • *Do not drive external loads with the output voltage from the internal power supply circuits.*
• *See Chapter 7, "Electrical Characteristics", for voltage values and drive capability.*

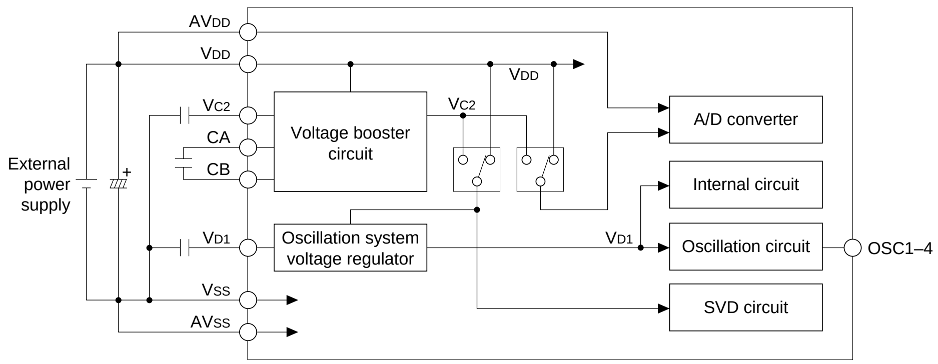


Fig. 2.1.1 Configuration of power supply

2.1.1 Voltage <VD1> for oscillation circuit and internal circuits

VD1 is a voltage for the oscillation circuit and the internal logic circuits, and is generated by the oscillation system voltage regulator for stabilizing the oscillation. The E0C63158 is designed with twin clock specification; it has two types of oscillation circuits OSC1 and OSC3 built-in. Use OSC1 clock for normal operation, and switch it to OSC3 by the software when high-speed operation is necessary. When switching the clock, the operating voltage VD1 must be switched by the software to stabilize the operation of the oscillation circuit and internal circuits. The oscillation system voltage regulator can output the following two types of VD1 voltage. It should be set at the value according to the oscillation circuit and oscillation frequency by the software.

1. Operation with OSC1 clock: VD1 = 1.3 V
2. Operation with OSC3 clock: VD1 = 2.1 V

Refer to Section 4.4, "Oscillation Circuit", for the VD1 switching procedure.
However, since the VD1 voltage value is fixed at 2.1 V when CR oscillation is selected for the OSC1 oscillation circuit by mask option and the OSC3 oscillation circuit (CR or ceramic oscillation) is also used, it is not necessary to switch VD1 by software. When the OSC3 oscillation circuit is not used, the OSC1 oscillation circuit can operate with 1.3 V of VD1 even if CR oscillation is selected.

2.1.2 Voltage source for oscillation system voltage regulator

(1) V_{C2} mode (booster mode)

The E0C63158 operates with 0.9–3.6 V supply voltage. However, a minimum 1.35 V supply voltage during single clock operation (OSC1) or a minimum 2.2 V during twin clock operation (OSC3, 2 MHz Typ.) is needed for the oscillation system voltage regulator. Therefore, when operating with the following supply voltage (V_{DD}), switch the power source for driving the oscillation system voltage regulator to V_{C2}.

- During single clock operation (OSC1): V_{DD} = 0.9–1.35 V (V_{C2} = 1.8–2.7 V)

When the supply voltage is more than needed for operation, do not set in this mode because the V_{C2} mode will increases current consumption to the oscillation system voltage regulator.

Note: Set the V_{C2} mode when a supply voltage drop is detected by the SVD circuit, such as during heavy load operation (driving buzzer or lamp) or by battery life. (∗)

(2) Normal mode

In this mode, the oscillation system voltage regulator directly operates by the power supply voltage V_{DD} within the range of 1.35–3.6 V (2.2–3.6 V when the OSC3 clock is used) without changing the power source to V_{C2}. At initial reset, this mode is set.

Table 2.1.2.1 Correspondence between power supply voltage and operating mode (oscillation system voltage ragulator)

Power supply circuit	Operating condition	Power supply voltage V_{DD} (V)		
		0.9–1.35	1.35–2.2	2.2–3.6
Oscillation system voltage regulator	OSC1	V_{C2} mode	Normal mode ∗	
	OSC3, 4 MHz	Cannot work		Normal mode

∗ See above Note in V_{C2} mode.

Refer to Section 4.2, " Setting of Power Supply and Operating Mode", for setting procedure of the operating mode.

2.1.3 Voltage source for A/D converter

(1) V_{C2} mode (booster mode)

The A/D converter operates with 0.9–3.6 V supply voltage. However, a minimum 1.6 V supply voltage is required for the A/D converter maximum error within ±3 LSB. Therefore, when operating with a 1.6 V or less of supply voltage (V_{DD}), switch the power source for driving the A/D converter circuit to V_{C2}.

(2) Normal mode

In this mode, the A/D converter circuit directly operates by the power supply voltage V_{DD} above 1.6 V without changing the power source to V_{C2}.

Table 2.1.4.1 Correspondence between power supply voltage and operating mode (A/D converter)

Circuit	Power supply voltage V_{DD} (V)	
	0.9–1.6	1.6–3.6
A/D converter	V_{C2} mode	Normal mode

2.2 *Initial Reset*

To initialize the E0C63158 circuits, initial reset must be executed. There are two ways of doing this.

(1) External initial reset by the RESET terminal
(2) External initial reset by simultaneous low input to terminals K00–K03 (mask option)

When the power is turned on, be sure to initialize using the above reset function. The circuit operation cannot be guaranteed if the IC starts operating by only turning the power on.

Figure 2.2.1 shows the configuration of the initial reset circuit.

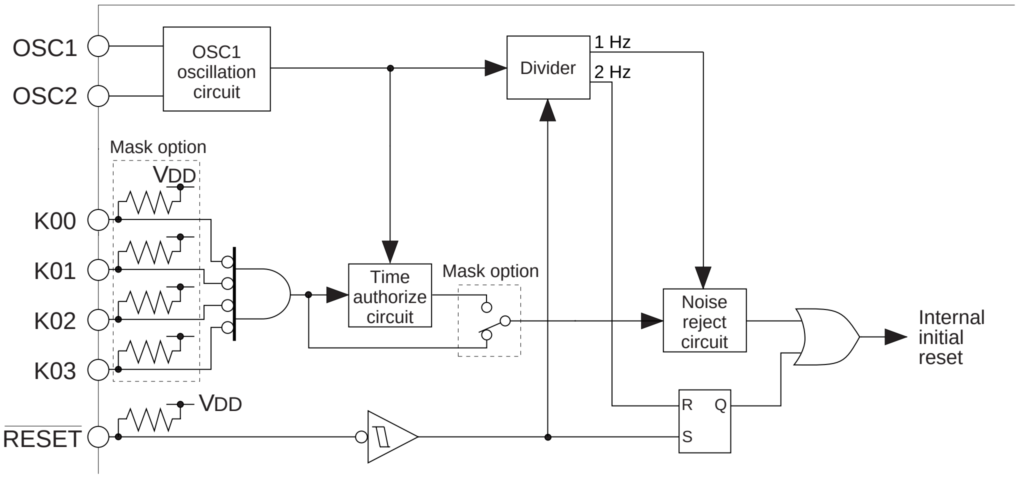


Fig. 2.2.1 Configuration of initial reset circuit

2.2.1 Reset terminal (RESET)

Initial reset can be executed externally by setting the reset terminal to a low level (VSS). After that the initial reset is released by setting the reset terminal to a high level (VDD) and the CPU starts operation. The reset input signal is maintained by the RS latch and becomes the internal initial reset signal. The RS latch is designed to be released by a 2 Hz signal that is divided by the OSC1 clock. Therefore in normal operation, a maximum of 250 msec (when f_{OSC1} = 32.768 kHz) is needed until the internal initial reset is released after the reset terminal goes to high level. Be sure to maintain a reset input of 0.1 msec or more. However, when turning the power on, the reset terminal should be set at a low level as in the timing shown in Figure 2.2.1.1.

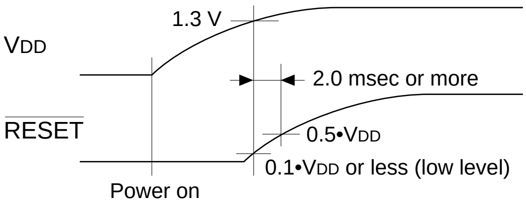


Fig. 2.2.1.1 Initial reset at power on

The reset terminal should be set to 0.1•VDD or less (low level) until the supply voltage becomes 1.3 V or more.
After that, a level of 0.5•VDD or less should be maintained more than 2.0 msec.

2.2.2 Simultaneous low input to terminals K00–K03

Another way of executing initial reset externally is to input a low signal simultaneously to the input ports (K00–K03) selected with the mask option.
Since this initial reset passes through the noise reject circuit, maintain the specified input port terminals at low level for at least 1.5 msec (when the oscillation frequency f_{OSC1} is 32.768 kHz) during normal operation. The noise reject circuit does not operate immediately after turning the power on until the oscillation circuit starts oscillating. Therefore, maintain the specified input port terminals at low level until the oscillation starts.
Table 2.2.2.1 shows the combinations of input ports (K00–K03) that can be selected with the mask option.

Table 2.2.2.1 Combinations of input ports

1	Not use
2	K00∗K01∗K02∗K03
3	K00∗K01∗K02
4	K00∗K01

When, for instance, mask option 2 (K00∗K01∗K02∗K03) is selected, initial reset is executed when the signals input to the four ports K00–K03 are all low at the same time. When 3 or 4 is selected, the initial reset is done when a key entry including a combination of selected input ports is made.
Further, the time authorize circuit can be selected with the mask option. The time authorize circuit checks the input time of the simultaneous low input and performs initial reset if that time is the defined time (1 to 2 sec) or more.
If using this function, make sure that the specified ports do not go low at the same time during ordinary operation.

2.2.3 Internal register at initial resetting

Initial reset initializes the CPU as shown in Table 2.2.3.1.

The registers and flags which are not initialized by initial reset should be initialized in the program if necessary.
In particular, the stack pointers SP1 and SP2 must be set as a pair because all the interrupts including NMI are masked after initial reset until both the SP1 and SP2 stack pointers are set with software.

When data is written to the EXT register, the E flag is set and the following instruction will be executed in the extended addressing mode. If an instruction which does not permit extended operation is used as the following instruction, the operation is not guaranteed. Therefore, do not write data to the EXT register for initialization only.
Refer to the "E0C63000 Core CPU Manual" for extended addressing and usable instructions.

Table 2.2.3.1 Initial values

CPU core			
Name	Symbol	Number of bits	Setting value
Data register A	A	4	Undefined
Data register B	B	4	Undefined
Extension register EXT	EXT	8	Undefined
Index register X	X	16	Undefined
Index register Y	Y	16	Undefined
Program counter	PC	16	0110H
Stack pointer SP1	SP1	8	Undefined
Stack pointer SP2	SP2	8	Undefined
Zero flag	Z	1	Undefined
Carry flag	C	1	Undefined
Interrupt flag	I	1	0
Extension flag	E	1	0
Queue register	Q	16	Undefined

Peripheral circuits		
Name	Number of bits	Setting value
RAM	4	Undefined
Display memory	4	Undefined
Other pheripheral circuits	–	∗

∗ See Section 4.1, "Memory Map".

2.2.4 Terminal settings at initial resetting

The output port (R) terminals and I/O port (P) terminals are shared with special output terminals, input/output terminals of the serial interface and input terminals of the A/D converter. These functions are selected by the software. At initial reset, these terminals are set to the general purpose output port terminals and I/O port terminals. Set them according to the system in the initial routine. In addition, take care of the initial status of output terminals when designing a system.
Table 2.2.4.1 shows the list of the shared terminal settings.

Table 2.2.4.1 List of shared terminal settings

Terminal name	Terminal status at initial reset	Special output		Serial I/F		A/D converter
		TOUT	FOUT	Master	Slave	
R00	R00 (High output)					
R01	R01 (High output)					
R02	R02 (High output)	TOUT				
R03	R03 (High output)		FOUT			
R10–R13	R10–R13 (High output)					
R20–R23	R20–R23 (High output)					
P00–P03	P00–P03 (Input & Pull-up)					
P10	P10 (Input & Pull-up ∗)			SIN(I)	SIN(I)	
P11	P11 (Input & Pull-up ∗)			SOUT(O)	SOUT(O)	
P12	P12 (Input & Pull-up ∗)			$\overline{\text{SCLK}}$(O)	$\overline{\text{SCLK}}$(I)	
P13	P13 (Input & Pull-up ∗)				$\overline{\text{SRDY}}$(O)	
P20–P23	P20–P23 (Input & Pull-up ∗)					
P30–P33	P30–P33 (Input & Pull-up ∗)					
P40	P40 (Input & Pull-up ∗)					AD0(I)
P41	P41 (Input & Pull-up ∗)					AD1(I)
P42	P42 (Input & Pull-up ∗)					AD2(I)
P43	P43 (Input & Pull-up ∗)					AD3(I)

∗ When "with pull-up" is selected by mask option (high impedance when "gate direct" is selected)

For setting procedure of the functions, see explanations for each of the peripheral circuits.

2.3 Test Terminal ($\overline{\text{TEST}}$)

This is the terminal used for the factory inspection of the IC. During normal operation, connect the $\overline{\text{TEST}}$ terminal to VDD.

CHAPTER 3 CPU, ROM, RAM

3.1 CPU

The E0C63158 has a 4-bit core CPU E0C63000 built-in as its CPU part.
Refer to the "E0C63000 Core CPU Manual" for the E0C63000.

Note: The SLP instruction cannot be used because the SLEEP operation is not assumed in the E0C63158.

3.2 Code ROM

The built-in code ROM is a mask ROM for loading programs, and has a capacity of 8,192 steps × 13 bits. The core CPU can linearly access the program space up to step FFFFH from step 0000H, however, the program area of the E0C63158 is step 0000H to step 1FFFH. The program start address after initial reset is assigned to step 0110H. The non-maskable interrupt (NMI) vector and hardware interrupt vectors are allocated to step 0100H and steps 0102H–010EH, respectively.

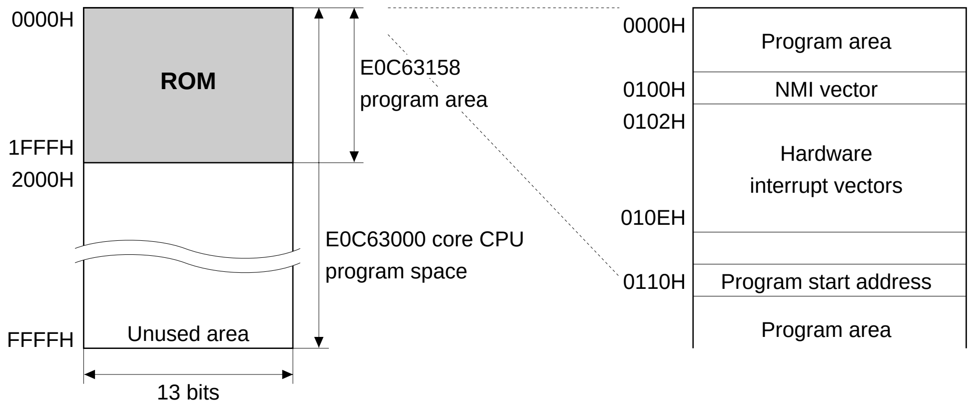


Fig. 3.2.1 Configuration of code ROM

3.3 RAM

The RAM is a data memory for storing various kinds of data, and has a capacity of 512 words × 4 bits. The RAM area is assigned to addresses 0000H to 01FFH on the data memory map. Addresses 0100H to 01FFH are 4-bit/16-bit data accessible areas and in other areas it is only possible to access 4-bit data.
When programming, keep the following points in mind.

(1) Part of the RAM area is used as a stack area for subroutine call and register evacuation, so pay attention not to overlap the data area and stack area.

(2) The E0C63000 core CPU handles the stack using the stack pointer for 4-bit data (SP2) and the stack pointer for 16-bit data (SP1).
16-bit data are accessed in stack handling by SP1, therefore, this stack area should be allocated to the area where 4-bit/16-bit access is possible (0100H to 01FFH). The stack pointers SP1 and SP2 change cyclically within their respective range: the range of SP1 is 0000H to 03FFH and the range of SP2 is 0000H to 00FFH. Therefore, pay attention to the SP1 value because it may be set to 0200H or more exceeding the 4-bit/16-bit accessible range in the E0C63158 or it may be set to 00FFH or less. Memory accesses except for stack operations by SP1 are 4-bit data access.
After initial reset, all the interrupts including NMI are masked until both the stack pointers SP1 and SP2 are set by software. Further, if either SP1 or SP2 is re-set when both are set already, the interrupts including NMI are masked again until the other is re-set. Therefore, the settings of SP1 and SP2 must be done as a pair.

(3) Subroutine calls use 4 words (for PC evacuation) in the stack area for 16-bit data (SP1). Interrupts use 4 words (for PC evacuation) in the stack area for 16-bit data (SP1) and 1 word (for F register evacuation) in the stack area for 4-bit data.

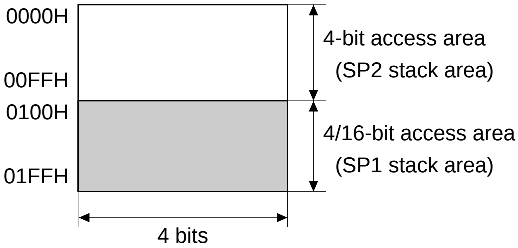


Fig. 3.3.1 Configuration of data RAM

CHAPTER 4 PERIPHERAL CIRCUITS AND OPERATION

The peripheral circuits of E0C63158 (timer, A/D, I/O, etc.) are interfaced with the CPU in the memory mapped I/O method. Thus, all the peripheral circuits can be controlled by accessing the I/O memory on the memory map using the memory operation instructions. The following sections explain the detailed operation of each peripheral circuit.

4.1 Memory Map

The E0C63158 data memory consists of 512-word RAM and 73-word peripheral I/O memory area. Figure 4.1.1 shows the overall memory map of the E0C63158, and Tables 4.1.1(a)–(f) the peripheral circuits' (I/O space) memory maps.

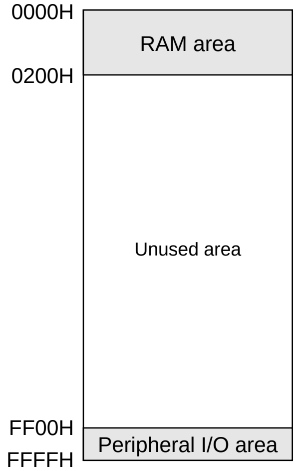


Fig. 4.1.1 Memory map

Note: Memory is not implemented in unused areas within the memory map. Further, some non-implementation areas and unused (access prohibition) areas exist in the peripheral I/O area. If the program that accesses these areas is generated, its operation cannot be guaranteed. Refer to the I/O memory maps shown in Tables 4.1.1 (a)–(f) for the peripheral I/O area.

Table 4.1.1 (a) I/O memory map (FF00H–FF28H)

Address	Register D3	Register D2	Register D1	Register D0	Name	Init *1	1	0	Comment
FF00H	CLKCHG	OSCC	0	VDC	CLKCHG	0	OSC3	OSC1	CPU clock switch
					OSCC	0	On	Off	OSC3 oscillation On/Off
	R/W		R	R/W	0 *3	– *2			Unused
					VDC	0	2.1 V	1.3 V	CPU operating voltage switch (1.3 V: OSC1, 2.1 V: OSC3)
FF01H	VADSEL	VDSEL	0	DBON	VADSEL	0	V_{C2}	V_{DD}	Power source selection for A/D converter
					VDSEL	0	V_{C2}	V_{DD}	Power supply selection for oscillation system voltage regulator
	R/W		R	R/W	0 *3	– *2			Unused
					DBON	0	On	Off	Voltage booster circuit On/Off
FF04H	SVDS3	SVDS2	SVDS1	SVDS0	SVDS3	0			SVD criteria voltage setting
					SVDS2	0			[SVDS3–0] 0 / 1 / 2 / 3 / 4 / 5 / 6 / 7 Voltage(V) 1.05 / 1.10 / 1.15 / 1.20 / 1.25 / 1.30 / 1.40 / 1.60
	R/W				SVDS1	0			[SVDS3–0] 8 / 9 / 10 / 11 / 12 / 13 / 14 / 15
					SVDS0	0			Voltage(V) 1.95 / 2.00 / 2.05 / 2.10 / 2.20 / 2.30 / 2.50 / 2.60
FF05H	0	0	SVDDT	SVDON	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R			R/W	SVDDT	0	Low	Normal	SVD evaluation data
					SVDON	0	On	Off	SVD circuit On/Off
FF06H	FOUTE	0	FOFQ1	FOFQ0	FOUTE	0	Enable	Disable	FOUT output enable
					0 *3	– *2			Unused
	R/W	R	R/W		FOFQ1	0			FOUT frequency selection: [FOFQ1, 0] 0 / 1 / 2 / 3
					FOFQ0	0			Frequency f_{OSC1}/64 / f_{OSC1}/8 / f_{OSC1} / f_{OSC3}
FF07H	0	0	WDEN	WDRST	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R		R/W	W	WDEN	1	Enable	Disable	Watchdog timer enable
					WDRST*3	Reset	Reset	Invalid	Watchdog timer reset (writing)
FF20H	SIK03	SIK02	SIK01	SIK00	SIK03	0	Enable	Disable	K00–K03 interrupt selection register
					SIK02	0	Enable	Disable	
	R/W				SIK01	0	Enable	Disable	
					SIK00	0	Enable	Disable	
FF21H	K03	K02	K01	K00	K03	– *2	High	Low	K00–K03 input port data
					K02	– *2	High	Low	
	R				K01	– *2	High	Low	
					K00	– *2	High	Low	
FF22H	KCP03	KCP02	KCP01	KCP00	KCP03	1	↓	↑	K00–K03 input comparison register
					KCP02	1	↓	↑	
	R/W				KCP01	1	↓	↑	
					KCP00	1	↓	↑	
FF24H	SIK13	SIK12	SIK11	SIK10	SIK13	0	Enable	Disable	K10–K13 interrupt selection register
					SIK12	0	Enable	Disable	
	R/W				SIK11	0	Enable	Disable	
					SIK10	0	Enable	Disable	
FF25H	K13	K12	K11	K10	K13	– *2	High	Low	K10–K13 input port data
					K12	– *2	High	Low	
	R				K11	– *2	High	Low	
					K10	– *2	High	Low	
FF26H	KCP13	KCP12	KCP11	KCP10	KCP13	1	↓	↑	K10–K13 input comparison register
					KCP12	1	↓	↑	
	R/W				KCP11	1	↓	↑	
					KCP10	1	↓	↑	
FF28H	0	0	0	SIK20	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R			R/W	0 *3	– *2			Unused
					SIK20	0	Enable	Disable	K20 interrupt selection register

Remarks

*1 Initial value at initial reset
*2 Not set in the circuit
*3 Constantly "0" when being read

Table 4.1.1 (b) I/O memory map (FF29H–FF44H)

Address	Register D3	Register D2	Register D1	Register D0	Name	Init *1	1	0	Comment
FF29H	0	0	0	K20	0 *3	– *2			Unused
	R				0 *3	– *2			Unused
					0 *3	– *2			Unused
					K20	– *2	High	Low	K20 input port data
FF2AH	0	0	0	KCP20	0 *3	– *2			Unused
	R			R/W	0 *3	– *2			Unused
					0 *3	– *2			Unused
					KCP20	1	↓	↑	K20 input comparison register
FF2BH	0	0	0	SENON	0 *3	– *2			Unused
	R			R/W	0 *3	– *2			Unused
					0 *3	– *2			Unused
					SENON	1	On	Off	Key sense On/Off control
FF30H	R03HIZ	R02HIZ	R01HIZ	R00HIZ	R03HIZ	0	High-Z	Output	R03 output high impedance control (FOUTE=0) FOUT output high impedance control (FOUTE=1)
	R/W				R02HIZ	0	High-Z	Output	R02 output high impedance control (PTOUT=0) TOUT output high impedance control (PTOUT=1)
					R01HIZ	0	High-Z	Output	R01 output high impedance control
					R00HIZ	0	High-Z	Output	R00 output high impedance control
FF31H	R03	R02	R01	R00	R03	1	High	Low	R03 output port data (FOUTE=0) Fix at "1" when FOUT is used
	R/W				R02	1	High	Low	R02 output port data (PTOUT=0) Fix at "1" when TOUT is used
					R01	1	High	Low	R01 output port data
					R00	1	High	Low	R00 output port data
FF32H	0	0	0	R1HIZ	0 *3	– *2			Unused
	R			R/W	0 *3	– *2			Unused
					0 *3	– *2			Unused
					R1HIZ	0	High-Z	Output	R1 output high impedance control
FF33H	R13	R12	R11	R10	R13	1	High	Low	R10–R13 output port data
	R/W				R12	1	High	Low	
					R11	1	High	Low	
					R10	1	High	Low	
FF34H	0	0	0	R2HIZ	0 *3	– *2			Unused
	R			R/W	0 *3	– *2			Unused
					0 *3	– *2			Unused
					R2HIZ	0	High-Z	Output	R2 output high impedance control
FF35H	R23	R22	R21	R20	R23	1	High	Low	R20–R23 output port data
	R/W				R22	1	High	Low	
					R21	1	High	Low	
					R20	1	High	Low	
FF40H	IOC03	IOC02	IOC01	IOC00	IOC03	0	Output	Input	P00–P03 I/O control register
	R/W				IOC02	0	Output	Input	
					IOC01	0	Output	Input	
					IOC00	0	Output	Input	
FF41H	PUL03	PUL02	PUL01	PUL00	PUL03	1	On	Off	P00–P03 pull-up control register
	R/W				PUL02	1	On	Off	
					PUL01	1	On	Off	
					PUL00	1	On	Off	
FF42H	P03	P02	P01	P00	P03	– *2	High	Low	P00–P03 I/O port data
	R/W				P02	– *2	High	Low	
					P01	– *2	High	Low	
					P00	– *2	High	Low	
FF44H	IOC13	IOC12	IOC11	IOC10	IOC13	0	Output	Input	P13 I/O control register functions as a general-purpose register when SIF (slave) is selected
	R/W				IOC12	0	Output	Input	P12 I/O control register (EISF=0) functions as a general-purpose register when SIF is selected
					IOC11	0	Output	Input	P11 I/O control register (EISF=0) functions as a general-purpose register when SIF is selected
					IOC10	0	Output	Input	P10 I/O control register (EISF=0) functions as a general-purpose register when SIF is selected

Table 4.1.1 (c) I/O memory map (FF45H–FF51H)

Address	Register D3	Register D2	Register D1	Register D0	Name	Init *1	1	0	Comment
FF45H	PUL13	PUL12	PUL11	PUL10	PUL13	1	On	Off	P13 pull-up control register functions as a general-purpose register when SIF (slave) is selected
	R/W				PUL12	1	On	Off	P12 pull-up control register (EISF=0) functions as a general-purpose register when SIF (master) is selected $\overline{\text{SCLK}}$ (I) pull-up control register when SIF (slave) is selected
					PUL11	1	On	Off	P11 pull-up control register (EISF=0) functions as a general-purpose register when SIF is selected
					PUL10	1	On	Off	P10 pull-up control register (EISF=0) SIN pull-up control register when SIF is selected
FF46H	P13	P12	P11	P10	P13	– *2	High	Low	P13 I/O port data functions as a general-purpose register when SIF (slave) is selected
	R/W				P12	– *2	High	Low	P12 I/O port data (EISF=0) functions as a general-purpose register when SIF is selected
					P11	– *2	High	Low	P11 I/O port data (EISF=0) functions as a general-purpose register when SIF is selected
					P10	– *2	High	Low	P10 I/O port data (EISF=0) functions as a general-purpose register when SIF is selected
FF48H	IOC23	IOC22	IOC21	IOC20	IOC23	0	Output	Input	P20–P23 I/O control register
	R/W				IOC22	0	Output	Input	
					IOC21	0	Output	Input	
					IOC20	0	Output	Input	
FF49H	PUL23	PUL22	PUL21	PUL20	PUL23	1	On	Off	P20–P23 pull-up control register
	R/W				PUL22	1	On	Off	
					PUL21	1	On	Off	
					PUL20	1	On	Off	
FF4AH	P23	P22	P21	P20	P23	– *2	High	Low	P20–P23 I/O port data
	R/W				P22	– *2	High	Low	
					P21	– *2	High	Low	
					P20	– *2	High	Low	
FF4CH	IOC33	IOC32	IOC31	IOC30	IOC33	0	Output	Input	P30–P33 I/O control register
	R/W				IOC32	0	Output	Input	
					IOC31	0	Output	Input	
					IOC30	0	Output	Input	
FF4DH	PUL33	PUL32	PUL31	PUL30	PUL33	1	On	Off	P30–P33 pull-up control register
	R/W				PUL32	1	On	Off	
					PUL31	1	On	Off	
					PUL30	1	On	Off	
FF4EH	P33	P32	P31	P30	P33	– *2	High	Low	P30–P33 I/O port data
	R/W				P32	– *2	High	Low	
					P31	– *2	High	Low	
					P30	– *2	High	Low	
FF50H	IOC43	IOC42	IOC41	IOC40	IOC43	0	Output	Input	P43 I/O control register (PAD3=0) functions as a general-purpose register when A/D is enabled
	R/W				IOC42	0	Output	Input	P42 I/O control register (PAD2=0) functions as a general-purpose register when A/D is enabled
					IOC41	0	Output	Input	P41 I/O control register (PAD1=0) functions as a general-purpose register when A/D is enabled
					IOC40	0	Output	Input	P40 I/O control register (PAD0=0) functions as a general-purpose register when A/D is enabled
FF51H	PUL43	PUL42	PUL41	PUL40	PUL43	1	On	Off	P43 pull-up control register (PAD3=0) functions as a general-purpose register when A/D is enabled
	R/W				PUL42	1	On	Off	P42 pull-up control register (PAD2=0) functions as a general-purpose register when A/D is enabled
					PUL41	1	On	Off	P41 pull-up control register (PAD1=0) functions as a general-purpose register when A/D is enabled
					PUL40	1	On	Off	P40 pull-up control register (PAD0=0) functions as a general-purpose register when A/D is enabled

Table 4.1.1 (d) I/O memory map (FF52H–FFC3H)

Address	Register D3	Register D2	Register D1	Register D0	Name	Init *1	1	0	Comment
FF52H	P43	P42	P41	P40	P43	– *2	High	Low	P43 I/O port data (PAD3=0) functions as a general-purpose register when A/D is enabled
	R/W				P42	– *2	High	Low	P42 I/O port data (PAD2=0) functions as a general-purpose register when A/D is enabled
					P41	– *2	High	Low	P41 I/O port data (PAD1=0) functions as a general-purpose register when A/D is enabled
					P40	– *2	High	Low	P40 I/O port data (PAD0=0) functions as a general-purpose register when A/D is enabled
FF64H	0	ENON	BZFQ	BZON	0 *3	– *2			Unused
	R	R/W			ENON	0	On	Off	2 Hz intervai On/Off
					BZFQ	0	2 kHz	4 kHz	Buzzer frequency selection
					BZON	0	On	Off	Buzzer output On/Off
FF70H	0	ESOUT	SCTRG	ESIF	0 *3	– *2			Unused
	R	R/W			ESOUT	0	Enable	Disable	SOUT enable/disable control
					SCTRG	0	Trigger	Invalid	Serial I/F clock trigger (writing)
							Run	Stop	Serial I/F clock status (reading)
					ESIF	0	SIF	I/O	Serial I/F enable (P1 port function selection)
FF71H	SDP	SCPS	SCS1	SCS0	SDP	0	MSB first	LSB first	Serial I/F data input/output permutation
	R/W				SCPS	0			Serial I/F clock phase selection
							↓	↑	–Negative polarity (mask option)
							↑	↓	–Positive polarity (mask option)
					SCS1	0			Serial I/F clock mode selection: [SCS1, 0] 0: Clock Slave; 1: Clock PT; 2: Clock OSC1/2; 3: Clock OSC1
					SCS0	0			
FF72H	SD3	SD2	SD1	SD0	SD3	– *2	High	Low	MSB
	R/W				SD2	– *2	High	Low	Serial I/F transmit/receive data (low-order 4 bits)
					SD1	– *2	High	Low	
					SD0	– *2	High	Low	LSB
FF73H	SD7	SD6	SD5	SD4	SD7	– *2	High	Low	MSB
	R/W				SD6	– *2	High	Low	Serial I/F transmit/receive data (high-order 4 bits)
					SD5	– *2	High	Low	
					SD4	– *2	High	Low	LSB
FF78H	0	0	TMRST	TMRUN	0 *3	– *2			Unused
	R		W	R/W	0 *3	– *2			Unused
					TMRST*3	Reset	Reset	Invalid	Clock timer reset (writing)
					TMRUN	0	Run	Stop	Clock timer Run/Stop
FF79H	TM3	TM2	TM1	TM0	TM3	0			Clock timer data (16 Hz)
	R				TM2	0			Clock timer data (32 Hz)
					TM1	0			Clock timer data (64 Hz)
					TM0	0			Clock timer data (128 Hz)
FF7AH	TM7	TM6	TM5	TM4	TM7	0			Clock timer data (1 Hz)
	R				TM6	0			Clock timer data (2 Hz)
					TM5	0			Clock timer data (4 Hz)
					TM4	0			Clock timer data (8 Hz)
FFC0H	MODE16	EVCNT	FCSEL	PLPOL	MODEL16	0	16 bit × 1	8 bit × 2	8 bit × 2 or 16 bit × 1 timer mode selection
	R/W				EVCNT	0	Event ct.	Timer	Timer 0 counter mode selection
					FCSEL	0	With NR	No NR	Timer 0 function selection (for event counter mode)
					PLPOL	0	↑	↓	Timer 0 pulse polarity selection (for event counter mode)
FFC1H	CHSEL	PTOUT	CKSEL1	CKSEL0	CHSEL	0	Timer1	Timer0	TOUT output channel selection
	R/W				PTOUT	0	On	Off	TOUT output control
					CKSEL1	0	OSC3	OSC1	Prescaler 1 source clock selection
					CKSEL0	0	OSC3	OSC1	Prescaler 0 source clock selection
FFC2H	PTPS01	PTPS00	PTRST0	PTRUN0	PTPS01	0			Prescaler 0 division ratio selection: [PTPS01, 00] 0: Division ratio 1/1; 1: 1/4; 2: 1/32; 3: 1/256
	R/W		W	R/W	PTPS00	0			
					PTRST0*3	– *2	Reset	Invalid	Timer 0 reset (reload)
					PTRUN0	0	Run	Stop	Timer 0 Run/Stop
FFC3H	PTPS11	PTPS10	PTRST1	PTRUN1	PTPS11	0			Prescaler 1 division ratio selection: [PTPS11, 10] 0: Division ratio 1/1; 1: 1/4; 2: 1/32; 3: 1/256
	R/W		W	R/W	PTPS10	0			
					PTRST1*3	– *2	Reset	Invalid	Timer 1 reset (reload)
					PTRUN1	0	Run	Stop	Timer 1 Run/Stop

Table 4.1.1 (e) I/O memory map (FFC4H–FFE3H)

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
FFC4H	RLD03	RLD02	RLD01	RLD00	RLD03	0			MSB
	R/W				RLD02	0			Programmable timer 0 reload data (low-order 4 bits)
					RLD01	0			
					RLD00	0			LSB
FFC5H	RLD07	RLD06	RLD05	RLD04	RLD07	0			MSB
	R/W				RLD06	0			Programmable timer 0 reload data (high-order 4 bits)
					RLD05	0			
					RLD04	0			LSB
FFC6H	RLD13	RLD12	RLD11	RLD10	RLD13	0			MSB
	R/W				RLD12	0			Programmable timer 1 reload data (low-order 4 bits)
					RLD11	0			
					RLD10	0			LSB
FFC7H	RLD17	RLD16	RLD15	RLD14	RLD17	0			MSB
	R/W				RLD16	0			Programmable timer 1 reload data (high-order 4 bits)
					RLD15	0			
					RLD14	0			LSB
FFC8H	PTD03	PTD02	PTD01	PTD00	PTD03	0			MSB
	R				PTD02	0			Programmable timer 0 data (low-order 4 bits)
					PTD01	0			
					PTD00	0			LSB
FFC9H	PTD07	PTD06	PTD05	PTD04	PTD07	0			MSB
	R				PTD06	0			Programmable timer 0 data (high-order 4 bits)
					PTD05	0			
					PTD04	0			LSB
FFCAH	PTD13	PTD12	PTD11	PTD10	PTD13	0			MSB
	R				PTD12	0			Programmable timer 1 data (low-order 4 bits)
					PTD11	0			
					PTD10	0			LSB
FFCBH	PTD17	PTD16	PTD15	PTD14	PTD17	0			MSB
	R				PTD16	0			Programmable timer 1 data (high-order 4 bits)
					PTD15	0			
					PTD14	0			LSB
FFD0H	ADRUN	ADCLK	CHS1	CHS0	ADRUN	0	Start	Invalid	A/D Run/Off control
	W	R/W			ADCLK	0	OSC3	OSC1	A/D input clock selection
					CHS1	0			A/D input channel selection: [CHS1, 0] 0 / 1 / 2 / 3
					CHS0	0			Input channel P40 / P41 / P42 / P43
FFD1H	PAD3	PAD2	PAD1	PAD0	PAD3	0	Enable	Disable	P43 input channel enable/disable control
	R/W				PAD2	0	Enable	Disable	P42 input channel enable/disable control
					PAD1	0	Enable	Disable	P41 input channel enable/disable control
					PAD0	0	Enable	Disable	P40 input channel enable/disable control
FFD2H	ADDR3	ADDR2	ADDR1	ADDR0	ADDR3	– *2			A/D converted data (D0–D3)
	R				ADDR2	– *2			
					ADDR1	– *2			
					ADDR0	– *2			
FFD3H	ADDR8	ADDR6	ADDR5	ADDR4	ADDR7	– *2			A/D converted data (D4–D7)
	R				ADDR6	– *2			
					ADDR5	– *2			
					ADDR4	– *2			
FFE2H	0	0	EIPT1	EIPT0	0 *3	– *2			Unused
	R		R/W		0 *3	– *2			Unused
					EIPT1	0	Enable	Mask	Interrupt mask register (Programmable timer 1)
					EIPT0	0	Enable	Mask	Interrupt mask register (Programmable timer 0)
FFE3H	0	0	0	EISIF	0 *3	– *2			Unused
	R			R/W	0 *3	– *2			Unused
					0 *3	– *2			Unused
					EISIF	0	Enable	Mask	Interrupt mask register (Serial I/F)

Table 4.1.1 (f) I/O memory map (FFE4H–FFF7H)

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
FFE4H	0	0	0	EIK0	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R	R	R	R/W	0 *3	– *2			Unused
					EIK0	0	Enable	Mask	Interrupt mask register (K00–K03)
FFE5H	0	0	EIK2	EIK1	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R	R	R/W	R/W	EIK2	0	Enable	Mask	Interrupt mask register (K20)
					EIK1	0	Enable	Mask	Interrupt mask register (K10–K13)
FFE6H	EIT3	EIT2	EIT1	EIT0	EIT3	0	Enable	Mask	Interrupt mask register (Clock timer 1 Hz)
					EIT2	0	Enable	Mask	Interrupt mask register (Clock timer 2 Hz)
	R/W	R/W	R/W	R/W	EIT1	0	Enable	Mask	Interrupt mask register (Clock timer 8 Hz)
					EIT0	0	Enable	Mask	Interrupt mask register (Clock timer 16 Hz)
FFE7H	0	0	0	EIAD	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R	R	R	R/W	0 *3	– *2			Unused
					EIAD	0	Enable	Mask	Interrupt mask register (A/D converter)
FFF2H	0	0	IPT1	IPT0	0 *3	– *2	(R)	(R)	Unused
					0 *3	– *2	Yes	No	Unused
	R	R	R/W	R/W	IPT1	0	(W)	(W)	Interrupt factor flag (Programmable timer 1)
					IPT0	0	Reset	Invalid	Interrupt factor flag (Programmable timer 0)
FFF3H	0	0	0	ISIF	0 *3	– *2	(R)	(R)	Unused
					0 *3	– *2	Yes	No	Unused
	R	R	R	R/W	0 *3	– *2	(W)	(W)	Unused
					ISIF	0	Reset	Invalid	Interrupt factor flag (Serial I/F)
FFF4H	0	0	0	IK0	0 *3	– *2	(R)	(R)	Unused
					0 *3	– *2	Yes	No	Unused
	R	R	R	R/W	0 *3	– *2	(W)	(W)	Unused
					IK0	0	Reset	Invalid	Interrupt factor flag (K00–K03)
FFF5H	0	0	IK2	IK1	0 *3	– *2	(R)	(R)	Unused
					0 *3	– *2	Yes	No	Unused
	R	R	R/W	R/W	IK2	0	(W)	(W)	Interrupt factor flag (K20)
					IK1	0	Reset	Invalid	Interrupt factor flag (K10–K13)
FFF6H	IT3	IT2	IT1	IT0	IT3	0	(R)	(R)	Interrupt factor flag (Clock timer 1 Hz)
					IT2	0	Yes	No	Interrupt factor flag (Clock timer 2 Hz)
	R/W	R/W	R/W	R/W	IT1	0	(W)	(W)	Interrupt factor flag (Clock timer 8 Hz)
					IT0	0	Reset	Invalid	Interrupt factor flag (Clock timer 16 Hz)
FFF7H	0	0	0	IAD	0 *3	– *2	(R)	(R)	Unused
					0 *3	– *2	Yes	No	Unused
	R	R	R	R/W	0 *3	– *2	(W)	(W)	Unused
					IAD	0	Reset	Invalid	Interrupt factor flag (A/D converter)

4.2 Setting of Power Supply and Operating Mode

This section explains how to control the operating mode according to the supply voltage. Refer to Section 2.1, "Power Supply" for the configuration of the power supply circuit.

4.2.1 Control of supply voltage

When the voltage value necessary to drive the oscillation system voltage regulator is not provided from the power supply voltage supplied externally ($V_{DD} \leq 1.35$ V), the E0C63158 drives the power supply circuit using the voltage V_{C2} generated by the voltage booster circuit. The supply voltage V_{C2} is controlled using the register DBON.

- For normal operation: Set DBON = "0"
- To use V_{C2} supply voltage: Set DBON = "1"

The supply voltage V_{C2} is common to the oscillation system voltage regulator and the A/D converter circuit. Therefore when using the V_{C2} voltage for either of these circuits, turn on the voltage booster circuit. The V_{C2} voltage is output from the voltage booster circuit.

The oscillation system voltage regulator and the A/D converter can independently select the drive voltage between V_{DD} and V_{C2}. This operation mode is controlled using the register VDSEL for the oscillation system voltage regulator and the register VADSEL for the A/D converter. By writing "1" to the register, V_{C2} is selected as the drive voltage and writing "0" selects V_{DD}. Approximately 100 msec is necessary until the V_{C2} voltage stables after turning the voltage booster ON by the DBON. Therefore, the operating mode should be switched as in the following sequence.

Normal mode → V_{C2} mode

1. Turn the voltage booster ON (set DBON = "1").
2. Maintain 100 msec or more.
3. Set "1" in the VDSEL (for the oscillation system voltage regulator) or VADSEL (for the A/D converter).

V_{C2} mode → Normal mode

1. Set "0" in the VDSEL or VADSEL.
2. Turn the voltage booster OFF (set DBON = "0").

* DBON should be kept at "1" if neither VDSEL or VADSEL is set to "0".

Note:
- *If the power supply voltage is out of the specified voltage range for an operating mode, do not switch into the operating mode. It may cause malfunction or increase current consumption.*
- *When operating the E0C63158 with a 0.9–1.35 V power supply voltage, software control is necessary. Set the oscillation system voltage regulator into the V_{C2} mode. When 1.35 V or more power supply voltage is used, do not set the oscillation system voltage regulator into the V_{C2} mode. At initial reset the normal mode is set.*
- *When using the A/D converter circuit with a 0.9–1.6 V power supply voltage, software control is necessary. Set the A/D converter circuit into the V_{C2} mode. When 1.6 V or more power supply voltage is used, don't set the A/D converter circuit into the V_{C2} mode. At initial reset the normal mode is set.*

4.2.2 Operating mode for the oscillation system voltage regulator and the internal operating voltage

The oscillation system voltage regulator generates the operating voltage V_{D1} for the oscillation circuit and internal logic circuits. This V_{D1} voltage must be switched according to the oscillation circuit to be used. Further the operating mode for the oscillation system voltage regulator must be switched according to the power supply voltage.
Control of V_{D1} and the oscillation circuit will be explained in Section 4.4, "Oscillation Circuit". This section explains the operating mode for the oscillation system voltage regulator that must be set before controlling them. The following shows the setting contents according to the power supply voltage and the oscillation circuit.

Table 4.2.2.1 Power supply voltage and operating mode

Power supply circuit	Operating condition	Operating voltage V_{D1}	Power supply voltage V_{DD} (V)		
			0.9–1.35	1.35–2.2	2.2–3.6
Oscillation system voltage regulator	OSC1	1.3 V	V_{C2} mode	Normal mode *	
	OSC3, 4 MHz	2.1 V	Cannot work		Normal mode

* Set the V_{C2} mode when a supply voltage drop is detected by the SVD circuit, such as during a heavy load operation (driving buzzer or lamp) or by battery deletion.

(1) Power supply voltage V_{DD} = 0.9 V to 1.35 V

When the power supply voltage is in this range, the oscillation system voltage regulator can operate only in the V_{C2} mode.
Set the V_{C2} mode with software, and do not change it to another mode during operation.

(2) Power supply voltage V_{DD} = 1.35 V to 2.2 V

When the CPU operates with the OSC1 clock (OSC3 oscillation circuit is OFF), the oscillation system voltage regulator can operate in the normal mode. Do not to set in the V_{C2} mode, since the V_{C2} mode increases current consumption.

(3) Power supply voltage V_{DD} = 2.2 V to 3.6 V

When the power supply voltage is in this range, the oscillation system voltage regulator can always operate in the normal mode regardless of the oscillation circuit setting. Be sure not to set in the V_{C2} mode.
The OSC3 oscillation circuit can be used in this voltage range.

4.2.3 Operating mode for A/D converter

The A/D converter uses AV_{DD} for the analog block and V_{DD} or V_{C2} as the power source for internal control circuit.

Table 4.2.3.1 Power supply voltage and operating mode

Circuit	Power supply voltage V_{DD} (V)	
	0.9–1.6	1.6–3.6
A/D converter	V_{C2} mode	Normal mode

(1) Power supply voltage V_{DD} = 0.9 V to 1.6 V

When the power supply voltage is in this range, VADSEL should be set to "1", to choose V_{C2} as the A/D converter power. This control is necessary to ensure the conversion accuracy.

(2) Power supply voltage V_{DD} = 1.6 V to 3.6 V

When the power supply voltage is in this range, it is possible to operate in the normal mode. Do not set in the V_{C2} mode.

4.2.4 I/O memory of power supply and operating mode

Table 4.2.4.1 shows the I/O addresses and control bits for the power supply and the operation mode.

Table 4.2.4.1 Control bits of power supply and operating mode

Address	Register								Comment
	D3	D2	D1	D0	Name	Init *1	1	0	
FF01H	VADSEL	VDSEL	0	DBON	VADSEL	0	V_{C2}	V_{DD}	Power source selection for A/D converter
					VDSEL	0	V_{C2}	V_{DD}	Power supply selection for oscillation system voltage regulator
	R/W		R	R/W	0 *3	– *2			Unused
					DBON	0	On	Off	Voltage booster circuit On/Off

*1 Initial value at initial reset

*2 Not set in the circuit

*3 Constantly "0" when being read

DBON: Booster control (ON/OFF) register (FF01H•D0)

Controls the voltage booster circuit.

When "1" is written: Booster ON
When "0" is written: Booster OFF
Reading: Valid

When the power supply voltage is in a range of 0.9 to 1.35 V, generate V_{C2} using the voltage booster to drive the internal power supply circuit. When "1" is written to the DBON register, the voltage booster generates V_{C2}. When "0" is written, boosting is not performed. When the power supply voltage is 1.35 V or more, do not use the voltage V_{C2} for oscillation system voltage regulator. However, this does not apply when the battery voltage falls by heavy load such as driving a buzzer and turning a lamp on.
When the power supply voltage is 1.6 V or more, do not use the voltage V_{C2} for the A/D converter.
At initial reset, this register is set to "0".

VDSEL: Power supply selection register for oscillation system voltage regulator (FF01H•D2)

Selects the power supply for the oscillation system voltage regulator.

When "1" is written: V_{C2}
When "0" is written: V_{DD}
Reading: Valid

When "1" is written to the VDSEL register, the oscillation system voltage regulator enters the V_{C2} mode and operates with V_{C2} output from the voltage booster. When "0" is written to the VDSEL register, the oscillation system voltage regulator operates with V_{DD} and the operating mode changes to the normal mode.
When switching from the normal mode to the V_{C2} mode, the VDSEL register should be set to "1" after taking a 100 msec or longer interval for the V_{C2} to stabilize from setting the DBON register to "1".
At initial reset, this register is set to "0".

VADSEL: Power supply selection register for A/D converter (FF01H•D3)

Selects the power supply for the A/D converter.

When "1" is written: V_{C2}
When "0" is written: V_{DD}
Reading: Valid

When "1" is written to the VADSEL register, the A/D converter enters the V_{C2} mode and operates with V_{C2} output from the voltage booster. When "0" is written to the VADSEL register, the A/D converter operates with V_{DD} and the operating mode changes to the normal mode.
When switching from the normal mode to the V_{C2} mode, the VADSEL register should be set to "1" after taking a 100 msec or longer interval for the V_{C2} to stabilize from setting the DBON register to "1".
At initial reset, this register is set to "0".
When using the A/D converter with a 1.6 V or less power supply voltage, set the V_{C2} mode.

4.2.5 Programming notes

(1) When driving the E0C63158 with a 0.9–1.35 V power supply voltage, software control is necessary. Set the oscillation system voltage regulator to the V_{C2} mode. When 1.35 V or more power supply voltage is used, do not set the oscillation system voltage regulator into the V_{C2} mode.

(2) When using the A/D converter with a 0.9–1.6 V power supply voltage, software control is necessary. Set the A/D converter voltage circuit to the V_{C2} mode. When 1.6 V or more power supply voltage is used, do not set the A/D converter circuit into the V_{C2} mode.

(3) If the power supply voltage is out of the specified voltage range for an operating mode, do not switch to the operating mode. It may cause malfunction or increase current consumption.

(4) When switching from the normal mode to the V_{C2} mode, the VDSEL and/or VADSEL registers should be set to "1" after taking a 100 msec or longer interval for the V_{C2} to stabilize from switching the DBON register to "1".

(5) When switching from the V_{C2} mode to the normal mode, use separate instructions to switch the mode (VDSEL = "0" or VADSEL = "0") and turn the voltage booster OFF (DBON = "0"). Simultaneous processing with a single instruction may cause malfunction.

(6) The OSC3 oscillation circuit can operate only in the normal mode with a power supply voltage from 2.2 V to 3.6 V.

4.3 Watchdog Timer

4.3.1 Configuration of watchdog timer

The E0C63158 has a built-in watchdog timer that operates with a 256 Hz divided clock from the OSC1 as the source clock. The watchdog timer starts operating after initial reset, however, it can be stopped by the software. The watchdog timer must be reset cyclically by the software while it operates. If the watchdog timer is not reset in at least 3–4 seconds, it generates a non-maskable interrupt (NMI) to the CPU.
Figure 4.3.1.1 is the block diagram of the watchdog timer.

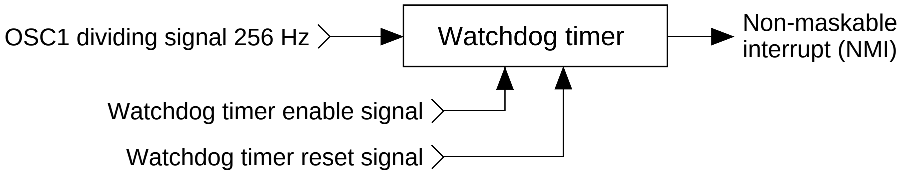


Fig. 4.3.1.1 Watchdog timer block diagram

The watchdog timer contains a 10-bit binary counter, and generates the non-maskable interrupt when the last stage of the counter (0.25 Hz) overflows.
Watchdog timer reset processing in the program's main routine enables detection of program overrun, such as when the main routine's watchdog timer processing is bypassed. Ordinarily this routine is incorporated where periodic processing takes place, just as for the timer interrupt routine.
The watchdog timer operates in the HALT mode. If a HALT status continues for 3–4 seconds, the non-maskable interrupt releases the HALT status.

4.3.2 Interrupt function

If the watchdog timer is not reset periodically, the non-maskable interrupt (NMI) is generated to the core CPU. Since this interrupt cannot be masked, it is accepted even in the interrupt disable status (I flag = "1"). However, it is not accepted when the CPU is in the interrupt mask state until SP1 and SP2 are set as a pair, such as after initial reset or during re-setting the stack pointer. The interrupt vector of NMI is assigned to 0100H in the program memory.

4.3.3 I/O memory of watchdog timer

Table 4.3.3.1 shows the I/O address and control bits for the watchdog timer.

Table 4.3.3.1 Control bits of watchdog timer

Address	Register								Comment
	D3	D2	D1	D0	Name	Init *1	1	0	
FF07H	0	0	WDEN	WDRST	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R		R/W	W	WDEN	1	Enable	Disable	Watchdog timer enable
					WDRST*3	Reset	Reset	Invalid	Watchdog timer reset (writing)

*1 Initial value at initial reset
*2 Not set in the circuit
*3 Constantly "0" when being read

WDEN: Watchdog timer enable register (FF07H•D1)

Selects whether the watchdog timer is used (enabled) or not (disabled).

When "1" is written: Enabled
When "0" is written: Disabled
Reading: Valid

When "1" is written to the WDEN register, the watchdog timer starts count operation. When "0" is written, the watchdog timer does not count and does not generate the interrupt (NMI).
At initial reset, this register is set to "1".

WDRST: Watchdog timer reset (FF07H•D0)

Resets the watchdog timer.

When "1" is written: Watchdog timer is reset
When "0" is written: No operation
Reading: Always "0"

When "1" is written to WDRST, the watchdog timer is reset and restarts immediately after that. When "0" is written, no operation results.
This bit is dedicated for writing, and is always "0" for reading.

4.3.4 Programming notes

(1) When the watchdog timer is being used, the software must reset it within 3-second cycles.

(2) Because the watchdog timer is set in operation state by initial reset, set the watchdog timer to disabled state (not used) before generating an interrupt (NMI) if it is not used.

4.4 Oscillation Circuit

4.4.1 Configuration of oscillation circuit

The E0C63158 has two oscillation circuits (OSC1 and OSC3). OSC1 is either a crystal or a CR oscillation circuit that supplies the operating clock to the CPU and peripheral circuits. OSC3 is either a CR or a ceramic oscillation circuit. When processing with the E0C63158 requires high-speed operation, the CPU operating clock can be switched from OSC1 to OSC3 by the software. To stabilize operation of the internal circuits, the operating voltage V_{D1} must be switched according to the oscillation circuit to be used. Figure 4.4.1.1 is the block diagram of this oscillation system.

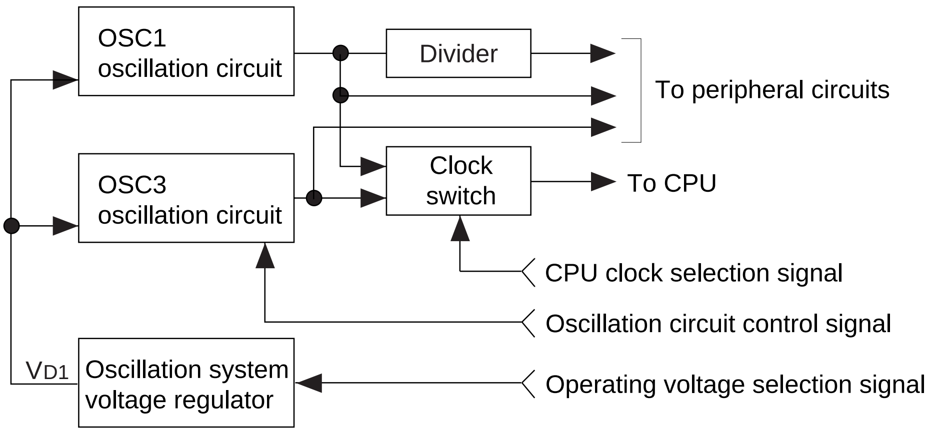
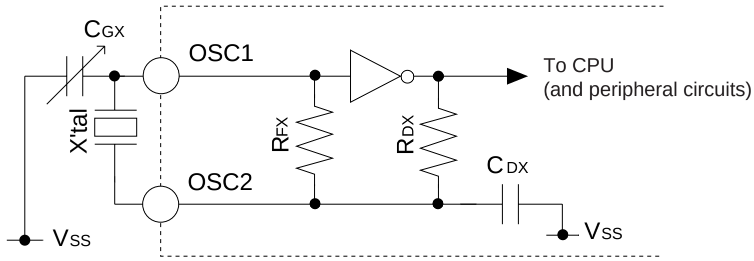


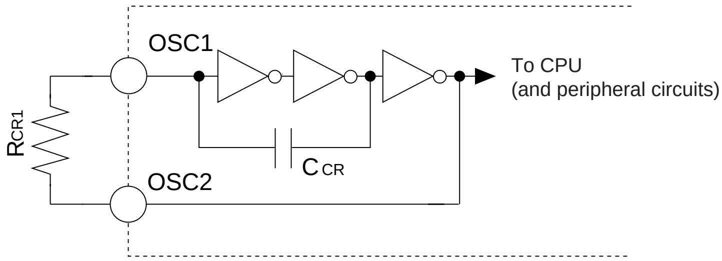
Fig. 4.4.1.1 Oscillation system block diagram

4.4.2 OSC1 oscillation circuit

The OSC1 oscillation circuit generates the main clock for the CPU and the peripheral circuits. Either the crystal oscillation circuit or the CR oscillation circuit can be selected as the circuit type by mask option. The oscillation frequency of the crystal oscillation circuit is 32.768 kHz (Typ.) and the CR oscillation circuit is 60 kHz (Typ.).
Figure 4.4.2.1 is the block diagram of the OSC1 oscillation circuit.



(a) Crystal oscillation circuit



(b) CR oscillation circuit

Fig. 4.4.2.1 OSC1 oscillation circuit

As shown in Figure 4.4.2.1, the crystal oscillation circuit can be configured simply by connecting the crystal oscillator (X'tal) of 32.768 kHz (Typ.) between the OSC1 and OSC2 terminals and the trimmer capacitor (C_{GX}) between the OSC1 and V_{SS} terminals when crystal oscillation is selected.

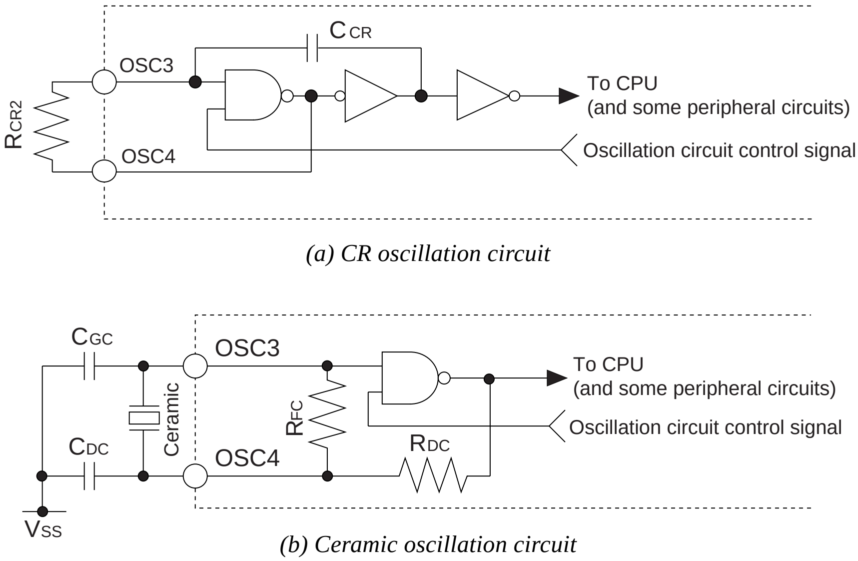
The CR oscillation circuit can be configured simply by connecting the resistor R_{CR1} between the OSC1 and OSC2 terminals when CR oscillation is selected. See Chapter 7, "Electrical Characteristics" for resistance value of R_{CR1}.

Note: • *The current consumption of CR oscillation is larger than crystal oscillation.*

• *Be aware that the CR oscillation frequency changes slightly.*
Pay special attention to the circuits that use f_{OSC1} as the source clock, such as the timer (time lag), the LCD frame frequency (display quality, flicker in low frequency) and the sound generator (sound quality).

4.4.3 OSC3 oscillation circuit

The E0C63158 has built-in the OSC3 oscillation circuit that generates the CPU's sub-clock (Typ. 2 MHz) for high speed operation and the source clock for peripheral circuits needing a high speed clock (programmable timer, FOUT output). The mask option enables selection of either the CR or ceramic oscillation circuit. When CR oscillation is selected, only a resistance is required as an external element. When ceramic oscillation is selected, a ceramic oscillator and two capacitors (gate and drain capacitance) are required.
Figure 4.4.3.1 is the block diagram of the OSC3 oscillation circuit.



(a) CR oscillation circuit

(b) Ceramic oscillation circuit

Fig. 4.4.3.1 OSC3 oscillation circuit

As shown in Figure 4.4.3.1, the CR oscillation circuit can be configured simply by connecting the resistor R_{CR2} between the OSC3 and OSC4 terminals when CR oscillation is selected. See Chapter 7, "Electrical Characteristics" for resistance value of R_{CR2}.
When ceramic oscillation is selected, the ceramic oscillation circuit can be configured by connecting the ceramic oscillator (Typ. 2 MHz) between the OSC3 and OSC4 terminals, capacitor C_{GC} between the OSC3 and OSC4 terminals, and capacitor C_{DC} between the OSC4 and V_{SS} terminals. For both C_{GC} and C_{DC}, connect capacitors that are about 100 pF. To reduce current consumption of the OSC3 oscillation circuit, oscillation can be stopped by the software (OSCC register).

4.4.4 Switching of operating voltage

The CPU system clock is switched to OSC1 or OSC3 by the software (CLKCHG register). In this case, to obtain stable operation, the operating voltage V_{D1} for the internal circuits must be switched by the software (VDC register). As described in Section 4.2, "Setting of Power Supply and Operating Mode", the oscillation system voltage regulator that generates V_{D1} must be set in an appropriate operating mode according to the supply voltage.
Table 4.4.4.1 shows the correspondence of the system clock, operating voltage V_{D1} and operating mode for the oscillation system voltage regulator.

Table 4.4.4.1 System clock and operating voltage

Operating condition	Operating voltage V_{D1}	Power supply voltage V_{DD} (V)		
		0.9–1.35	1.35–2.2	2.2–3.6
OSC1	1.3 V	V_{C2} mode	Normal mode ∗	
OSC3, 4 MHz	2.1 V	Cannot work		Normal mode

* Set the V_{C2} mode when a power supply voltage drop is detected by the SVD circuit, such as during a heavy load operation (driving buzzer or lamp) or by battery deletion.

When switching the operating voltage and the system clock, properly set the operating mode for the oscillation system voltage regulator before and after. (See Section 4.2, "Setting of Power Supply and Operation Mode".)

When OSC3 is to be used as the CPU system clock, it should be done as the following procedure using the software: first switch the operating mode (if necessary) and the operating voltage V_{D1}, turn the OSC3 oscillation ON after waiting 2.5 msec or more for the above operation to stabilize, switch the clock after waiting 5 msec or more for oscillation stabilization.
When switching from OSC3 to OSC1, turn the OSC3 oscillation circuit OFF after switching the clock then set the operating voltage V_{D1} to 1.3 V. After that, switch the operating mode if necessary.

OSC1 → OSC3

1. Set operation mode for OSC3. ∗
2. Set VDC to "1" (1.3 V → 2.1 V).
3. Maintain 2.5 msec or more.
4. Set OSCC to "1" (OSC3 oscillation ON).
5. Maintain 5 msec or more.
6. Set CLKCHG to "1" (OSC1 → OSC3).

OSC3 → OSC1

1. Set CLKCHG to "0" (OSC3 → OSC1).
2. Set OSCC to "0" (OSC3 oscillation OFF).
3. Set VDC to "0" (2.1 V → 1.3 V).
4. Set operation mode for OSC1. ∗

(∗: Should be done only when necessary.)

However, since the V_{D1} voltage value is fixed at 2.1 V when CR oscillation is selected for the OSC1 oscillation circuit by mask option and the OSC3 oscillation circuit (CR or ceramic oscillation) is also used, it is not necessary to switch V_{D1} by software. When the OSC3 oscillation circuit is not used, the OSC1 oscillation circuit can operate with 1.3 V of V_{D1} even if CR oscillation is selected.

The following shows the operating mode settings for the oscillation system voltage regulator depending on the power supply voltage.

(1) Power supply voltage V_{DD} = 0.9 V to 1.35 V

When the power supply voltage is in this range, the oscillation system voltage regulator can be operated only in the V_{C2} mode.

(2) Power supply voltage V_{DD} = 1.35 V to 2.2 V

When the system clock is OSC1, operate the oscillation system voltage regulator in the normal mode.

(3) Power supply voltage V_{DD} = 2.2 V to 3.6 V

When the power supply voltage is in this range, the oscillation system voltage regulator can always be operated in the normal mode regardless of the system clock selection. Therefore, it is nor necessary to switch the operating mode before and after switching the system clock.

4.4.5 Clock frequency and instruction execution time

Table 4.4.5.1 shows the instruction execution time according to each frequency of the system clock.

Table 4.4.5.1 Clock frequency and instruction execution time

Clock frequency	Instruction execution time (μsec)		
	1-cycle instruction	2-cycle instruction	3-cycle instruction
OSC1: 32.768 kHz	61	122	183
OSC1: 60 kHz	33	66	100
OSC3: 4 MHz	0.5	1	1.5

4.4.6 I/O memory of oscillation circuit

Table 4.4.6.1 shows the I/O address and the control bits for the oscillation circuit.

Table 4.4.6.1 Control bits of oscillation circuit

Address	Register D3	Register D2	Register D1	Register D0	Name	Init *1	1	0	Comment
FF00H	CLKCHG	OSCC	0	VDC	CLKCHG	0	OSC3	OSC1	CPU clock switch
	R/W	R/W	R	R/W	OSCC	0	On	Off	OSC3 oscillation On/Off
					0 *3	– *2			Unused
					VDC	0	2.1 V	1.3 V	CPU operating voltage switch (1.3 V: OSC1, 2.1 V: OSC3)

*1 Initial value at initial reset

*2 Not set in the circuit

*3 Constantly "0" when being read

VDC: CPU operating voltage switching register (FF00H•D0)

It is used to switch the operating voltage VD1, when the crystal oscillation circuit has been selected as the OSC1 oscillation circuit by mask option.

When "1" is written: 2.1 V (for OSC3 operation)
When "0" is written: 1.3 V (for OSC1 operation)
Reading: Valid

When switching the CPU system clock, the operating voltage VD1 should also be switched according to the clock.
When switching from OSC1 to OSC3, first set VD1 to 2.1 V. After that maintain 2.5 msec or more, and then turn the OSC3 oscillation ON.
When switching from OSC3 to OSC1, set VD1 to 1.3 V after switching to OSC1 and turning the OSC3 oscillation OFF.
However, since the VD1 voltage value is fixed at 2.1 V when CR oscillation is selected for the OSC1 oscillation circuit by mask option and the OSC3 oscillation circuit (CR or ceramic oscillation) is also used, it is not necessary to switch VD1 by software. When the OSC3 oscillation circuit is not used, the OSC1 oscillation circuit can operate with 1.3 V of VD1 even if CR oscillation is selected.
At initial reset, this register is set to "0".

OSCC: OSC3 oscillation control register (FF00H•D2)

Controls oscillation ON/OFF for the OSC3 oscillation circuit.

When "1" is written: OSC3 oscillation ON
When "0" is written: OSC3 oscillation OFF
Reading: Valid

When it is necessary to operate the CPU at high speed, set OSCC to "1". At other times, set it to "0" to reduce current consumption. Furthermore, when the crystal oscillation circuit has been selected as the OSC1 oscillation circuit by mask option, it is necessary to switch the operating voltage VD1 when turning the OSC3 oscillation circuit ON and OFF
At initial reset, this register is set to "0".

CLKCHG: CPU system clock switching register (FF00H•D3)

The CPU's operation clock is selected with this register.

When "1" is written: OSC3 clock is selected
When "0" is written: OSC1 clock is selected
Reading: Valid

When the CPU clock is to be OSC3, set CLKCHG to "1"; for OSC1, set CLKCHG to "0".
After turning the OSC3 oscillation ON (OSCC = "1"), switching of the clock should be done after waiting 5 msec or more.
When V_{D1} is 1.3 V (VDC = "0") and when OSC3 oscillation is OFF (OSCC = "0"), setting of CLKCHG = "1" becomes invalid and switching to OSC3 is not performed. When the CR oscillation circuit has been selected as the OSC1 oscillation circuit by mask option, setting VDC to "0" makes no difference.
At initial reset, this register is set to "0".

4.4.7 Programming notes

(1) When switching the CPU system clock from OSC1 to OSC3, first set V_{D1}. After that maintain 2.5 msec or more, and then turn the OSC3 oscillation ON.
When switching from OSC3 to OSC1, set V_{D1} after switching to OSC1 and turning the OSC3 oscillation OFF. However, when the CR oscillation circuit has been selected as the OSC1 oscillation circuit, it is not necessary to set V_{D1}.

(2) It takes at least 5 msec from the time the OSC3 oscillation circuit goes ON until the oscillation stabilizes. Consequently, when switching the CPU operation clock from OSC1 to OSC3, do this after a minimum of 5 msec have elapsed since the OSC3 oscillation went ON.
Further, the oscillation stabilization time varies depending on the external oscillator characteristics and conditions of use, so allow ample margin when setting the wait time.

(3) When switching the clock form OSC3 to OSC1, use a separate instruction for switching the OSC3 oscillation OFF. An error in the CPU operation can result if this processing is performed at the same time by the one instruction.

(4) Since the V_{D1} voltage value is fixed at 2.1 V when CR oscillation is selected for the OSC1 oscillation circuit by mask option and the OSC3 oscillation circuit (CR or ceramic oscillation) is also used, it is not necessary to switch V_{D1} by software. When the OSC3 oscillation circuit is not used, the OSC1 oscillation circuit can operate with 1.3 V of V_{D1} even if CR oscillation is selected.

4.5 Input Ports (K00–K03, K10–K13 and K20)

4.5.1 Configuration of input ports

The E0C63158 has nine bits general-purpose input ports. Each of the input port terminals (K00–K03, K10–K13, K20) provides internal pull-up resistor. Pull-up resistor can be selected for each bit with the mask option.
Figure 4.5.1.1 shows the configuration of input port (K00–K03, K10–K13).
Figure 4.5.1.2 shows the configuration of input port (K20).

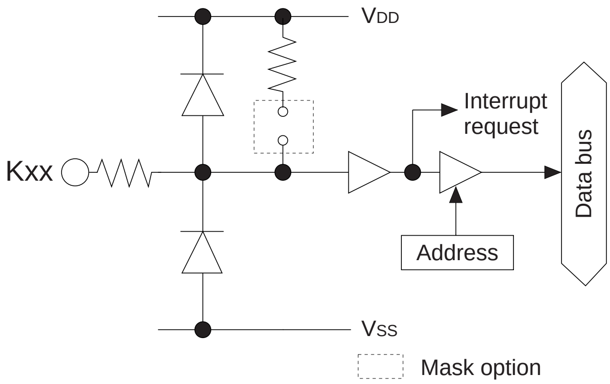


Fig. 4.5.1.1 Configuration of input port (K00–K03, K10–K13)

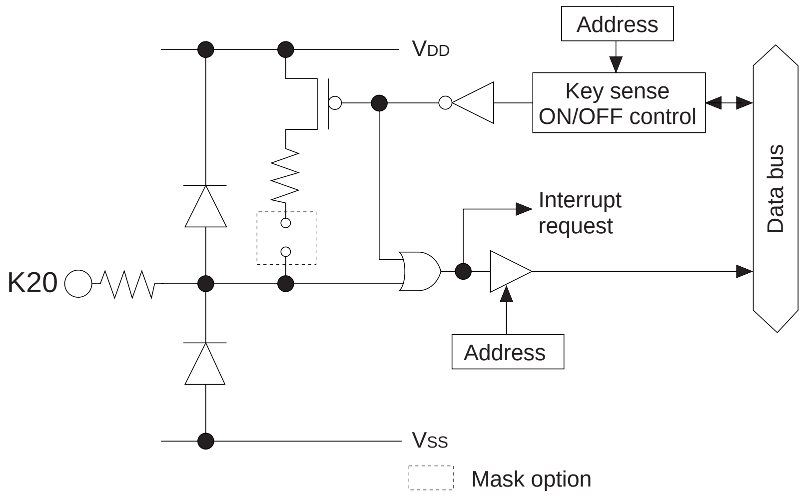


Fig. 4.5.1.2 Configuration of input port (K20)

Selection of "With pull-up resistor" with the mask option suits input from the push switch, key matrix, and so forth. When "Gate direct" is selected, the port can be used for slide switch input and interfacing with other LSIs.

4.5.2 Interrupt function

All nine bits of the input ports (K00–K03, K10–K13, K20) provide the interrupt function. The conditions for issuing an interrupt can be set by the software. Further, whether to mask the interrupt function can be selected by the software. The input interrupts are divided into three systems: K0 (K00–K03), K1 (K10–K13) and K20 systems.
Figure 4.5.2.1 shows the configuration of K00–K03 (K10–K13) interrupt circuit.
Figure 4.5.2.2 shows the configuration of K20 interrupt circuit.

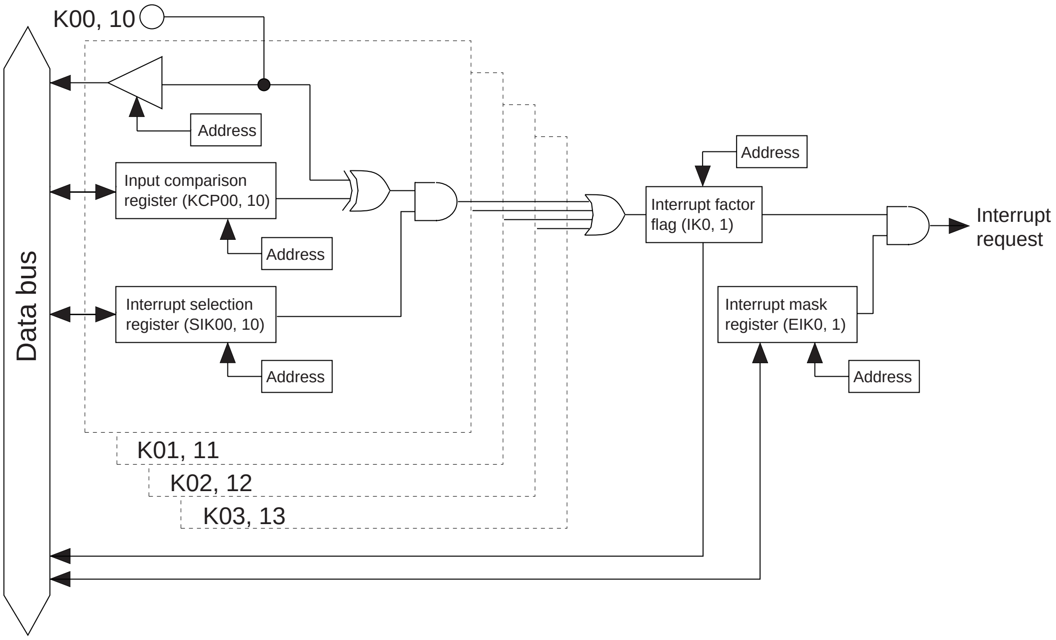


Fig. 4.5.2.1 Input interrupt circuit configuration (K00–K03, K10–K13)

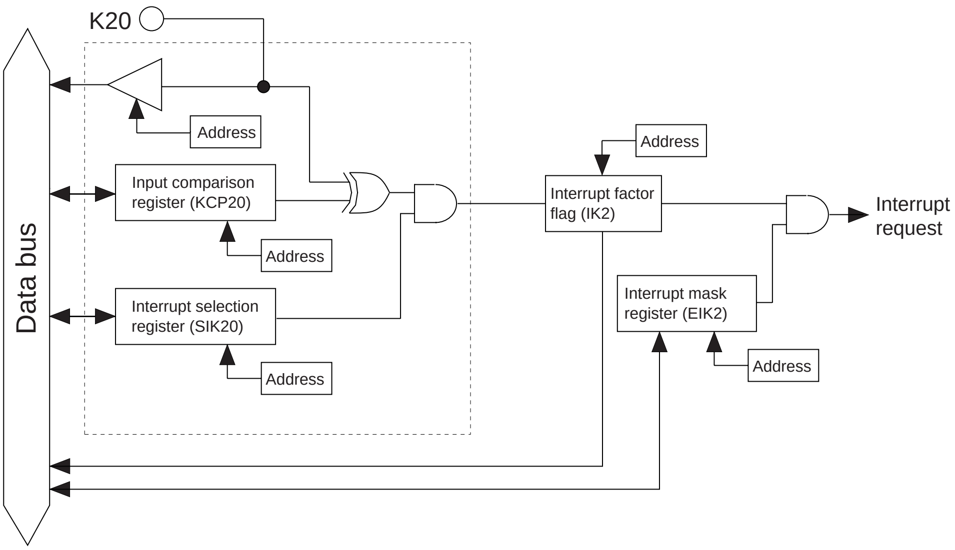


Fig. 4.5.2.2 Input interrupt circuit configuration (K20)

The interrupt selection register (SIK) and input comparison register (KCP) are individually set for the input ports K00–K03, K10–K13 and K20, and can specify the terminals for generating interrupt and interrupt timing.
The interrupt selection registers (SIK00–SIK03, SIK10–SIK13, SIK20) select what input of K00–K03, K10–K13 and K20 to use for the interrupt. Writing "1" into an interrupt selection register incorporates that input port into the interrupt generation conditions. The changing the input port where the interrupt selection register has been set to "0" does not affect the generation of the interrupt.
The input interrupt timing can select that the interrupt be generated at the rising edge of the input or that it be generated at the falling edge according to the set value of the input comparison registers (KCP00–KCP03, KCP10–KCP13, KCP20).
By setting these two conditions, the interrupt for K00–K03, K10–K13 or K20 is generated when input ports in which an interrupt has been enabled by the input selection registers and the contents of the input comparison registers have been changed from matching to no matching.
The interrupt mask registers (EIK0, EIK1, EIK2) enable the interrupt mask to be selected for K00–K03, K10–K13 and K20.
When the interrupt is generated, the interrupt factor flag (IK0, IK1, IK2) is set to "1".
Figure 4.5.2.3 shows an example of an interrupt for K00–K03.

Interrupt selection register

SIK03	SIK02	SIK01	SIK00
1	1	1	0

Input comparison register

KCP03	KCP02	KCP01	KCP00
1	0	1	0

With the above setting, the interrupt of K00–K03 is generated under the following condition:

Input port

(1)

K03	K02	K01	K00
1	0	1	0

(Initial value)

↓

(2)

K03	K02	K01	K00
1	0	1	1

↓

(3)

K03	K02	K01	K00
0	0	1	1

→ Interrupt generation

Because K00 interrupt is set to disable, interrupt will be generated when no matching occurs between the contents of the 3 bits K01–K03 and the 3 bits input comparison register KCP01–KCP03.

↓

(4)

K03	K02	K01	K00
0	1	1	1

Fig. 4.5.2.3 Example of interrupt of K00–K03

K00 interrupt is disabled by the interrupt selection register (SIK00), so that an interrupt does not occur at (2). At (3), K03 changes to "0"; the data of the terminals that are interrupt enabled no longer match the data of the input comparison registers, so that interrupt occurs. As already explained, the condition for the interrupt to occur is the change in the port data and contents of the input comparison registers from matching to no matching. Hence, in (4), when the no matching status changes to another no matching status, an interrupt does not occur. Further, terminals that have been masked for interrupt do not affect the conditions for interrupt generation.

4.5.3 Mask option

Internal pull-up resistor can be selected for each of the nine bits of the input ports (K00–K03, K10–K13, K20) with the input port mask option.
When "Gate direct" is selected, take care that the floating status does not occur for the input. Select "With pull-up resistor" for input ports that are not being used.

4.5.4 I/O memory of input ports

Table 4.5.4.1 shows the I/O addresses and the control bits for the input ports.

Table 4.5.4.1 Control bits of input ports

Address	Register D3	Register D2	Register D1	Register D0	Name	Init *1	1	0	Comment
FF20H	SIK03	SIK02	SIK01	SIK00	SIK03	0	Enable	Disable	K00–K03 interrupt selection register
					SIK02	0	Enable	Disable	
	R/W				SIK01	0	Enable	Disable	
					SIK00	0	Enable	Disable	
FF21H	K03	K02	K01	K00	K03	– *2	High	Low	K00–K03 input port data
					K02	– *2	High	Low	
	R				K01	– *2	High	Low	
					K00	– *2	High	Low	
FF22H	KCP03	KCP02	KCP01	KCP00	KCP03	1	↓	↑	K00–K03 input comparison register
					KCP02	1	↓	↑	
	R/W				KCP01	1	↓	↑	
					KCP00	1	↓	↑	
FF24H	SIK13	SIK12	SIK11	SIK10	SIK13	0	Enable	Disable	K10–K13 interrupt selection register
					SIK12	0	Enable	Disable	
	R/W				SIK11	0	Enable	Disable	
					SIK10	0	Enable	Disable	
FF25H	K13	K12	K11	K10	K13	– *2	High	Low	K10–K13 input port data
					K12	– *2	High	Low	
	R				K11	– *2	High	Low	
					K10	– *2	High	Low	
FF26H	KCP13	KCP12	KCP11	KCP10	KCP13	1	↓	↑	K10–K13 input comparison register
					KCP12	1	↓	↑	
	R/W				KCP11	1	↓	↑	
					KCP10	1	↓	↑	
FF28H	0	0	0	SIK20	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R			R/W	0 *3	– *2			Unused
					SIK20	0	Enable	Disable	K20 interrupt selection register
FF29H	0	0	0	K20	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R				0 *3	– *2			Unused
					K20	– *2	High	Low	K20 input port data
FF2AH	0	0	0	KCP20	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R			R/W	0 *3	– *2			Unused
					KCP20	1	↓	↑	K20 input comparison register
FF2BH	0	0	0	SENON	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R			R/W	0 *3	– *2			Unused
					SENON	1	On	Off	Key sense On/Off control
FFE4H	0	0	0	EIK0	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R			R/W	0 *3	– *2			Unused
					EIK0	0	Enable	Mask	Interrupt mask register (K00–K03)
FFE5H	0	0	EIK2	EIK1	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R		R/W		EIK2	0	Enable	Mask	Interrupt mask register (K20)
					EIK1	0	Enable	Mask	Interrupt mask register (K10–K13)
FFF4H	0	0	0	IK0	0 *3	– *2	(R)	(R)	Unused
					0 *3	– *2	Yes	No	Unused
	R			R/W	0 *3	– *2	(W)	(W)	Unused
					IK0	0	Reset	Invalid	Interrupt factor flag (K00–K03)
FFF5H	0	0	IK2	IK1	0 *3	– *2	(R)	(R)	Unused
					0 *3	– *2	Yes	No	Unused
	R		R/W		IK2	0	(W)	(W)	Interrupt factor flag (K20)
					IK1	0	Reset	Invalid	Interrupt factor flag (K10–K13)

*1 Initial value at initial reset *2 Not set in the circuit *3 Constantly "0" when being read

K00–K03: K0 port input port data (FF21H)
K10–K13: K1 port input port data (FF25H)
K20: K20 port input port data (FF29H•D0)

Input data of the input port terminals can be read with these registers.

When "1" is read: High level
When "0" is read: Low level
Writing: Invalid

The reading is "1" when the terminal voltage of the nine bits of the input ports (K00–K03, K10–K13, K20) goes high (VDD), and "0" when the voltage goes low (VSS).
These bits are dedicated for reading, so writing cannot be done.

SIK00–SIK03: K0 port interrupt selection register (FF20H)
SIK10–SIK13: K1 port interrupt selection register (FF24H)
SIK20: K20 port interrupt selection register (FF28H•D0)

Selects the ports to be used for the K00–K03, K10–K13 and K20 input interrupts.

When "1" is written: Enable
When "0" is written: Disable
Reading: Valid

Enables the interrupt for the input ports (K00–K03, K10–K13, K20) for which "1" has been written into the interrupt selection registers (SIK00–SIK03, SIK10–SIK13, SIK20). The input port set for "0" does not affect the interrupt generation condition.
At initial reset, these registers are set to "0".

KCP00–KCP03: K0 port input comparison register (FF22H)
KCP10–KCP13: K1 port input comparison register (FF26H)
KCP20: K20 port input comparison register (FF2AH•D0)

Interrupt conditions for terminals K00–K03, K10–K13 and K20 can be set with these registers.

When "1" is written: Falling edge
When "0" is written: Rising edge
Reading: Valid

The interrupt conditions can be set for the rising or falling edge of input for each of the nine bits (K00–K03, K10–K13, K20), through the input comparison registers (KCP00–KCP03, KCP10–KCP13, KCP20).
For KCP00–KCP03, a comparison is done only with the ports that are enabled by the interrupt among K00–K03 by means of the SIK00–SIK03 registers. For KCP10–KCP13, a comparison is done only with the ports that are enabled by the interrupt among K10–K13 by means of the SIK10–SIK13 registers. For KCP20, a comparison is done only when the K20 port has been enabled by means of the SIK20 register.
At initial reset, these registers are set to "0".

EIK0: K0 input interrupt mask register (FFE4H•D0)
EIK1: K1 input interrupt mask register (FFE5H•D0)
EIK2: K20 input interrupt mask register (FFE5H•D1)

Masking the interrupt of the input port can be selected with these registers.

When "1" is written: Enable
When "0" is written: Mask
Reading: Valid

With these registers, masking of the input port interrupt can be selected for each of the three systems (K00–K03, K10–K13, K20).
At initial reset, these registers are set to "0".

IK0: K0 input interrupt factor flag (FFF4H•D0)
IK1: K1 input interrupt factor flag (FFF5H•D0)
IK2: K20 input interrupt factor flag (FFF5H•D1)

These flags indicate the occurrence of input interrupt.

When "1" is read: Interrupt has occurred
When "0" is read: Interrupt has not occurred

When "1" is written: Flag is reset
When "0" is written: Invalid

The interrupt factor flags IK0, IK1 and IK2 are associated with K00–K03, K10–K13 and K20, respectively. From the status of these flags, the software can decide whether an input interrupt has occurred.
The interrupt factor flag is set to "1" when the interrupt condition is established regardless of the interrupt mask register setting. However, the interrupt does not occur to the CPU when the interrupt is masked.
These flags are reset to "0" by writing "1" to them.
After an interrupt occurs, the same interrupt will occur again if the interrupt enabled state (I flag = "1") is set or the RETI instruction is executed unless the interrupt factor flag is reset. Therefore, be sure to reset (write "1" to) the interrupt factor flag in the interrupt service routine before shifting to the interrupt enabled state.
At initial reset, these flags are set to "0".

SENON: K20 port key sense ON/OFF control (FF2BH•D0)

Controls the key sense function.

When "1" is written: On
When "0" is written: Off
Reading: Valid

When using K20 as a general purpose input port, fix this register at "1" (On).
When K20 is used for the key sense function, set SENON on during the key sense stage. If any key is pressed (see Figure 4.5.4.1), the K20 port generates an interrupt to the CPU. Then set SENON to off (K20 port key sense OFF), turn the outside N-P-N transistor on using an output port and start the A/D converter. The A/D converter converts the input voltage that varies according to the pressed key into a digital value. The software can discriminates which key was pressed from the conversion result. After that, turn SENON off to reduce current consumption.

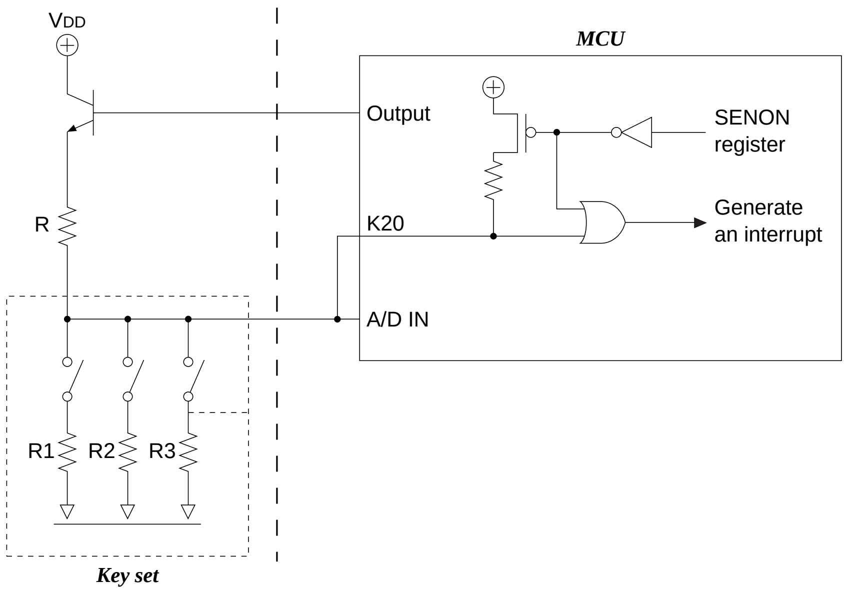


Fig. 4.5.4.1 Key position sensing circuit

This chart is an example of the circuit that discriminates the pressed key with only two wires connected between the MCU chip and the key set. It is useful to reduce the connection wires when the key set location is far from the MCU chip.

Operation: The keys are connected to the ground via a resistor that is different from other keys. So each key will generate a different voltage for inputting to the A/D converter.
Pressing a key generates an interrupt to the MCU. The interrupt turns the transistor on using the output port and starts A/D conversion. The MCU can discriminate the pressed key using the digital value converted by the A/D converter.

4.5.5 Programming notes

(1) When input ports are changed from low to high by pull-up resistors, the rise of the waveform is delayed on account of the time constant of the pull-up resistor and input gate capacitance. Hence, when fetching input ports, set an appropriate waiting time.
Particular care needs to be taken of the key scan during key matrix configuration.
Make this waiting time the amount of time or more calculated by the following expression.
$10 \times C \times R$
C: terminal capacitance□5 pF + parasitic capacitance□? pF
R: pull-up resistance 300 kΩ

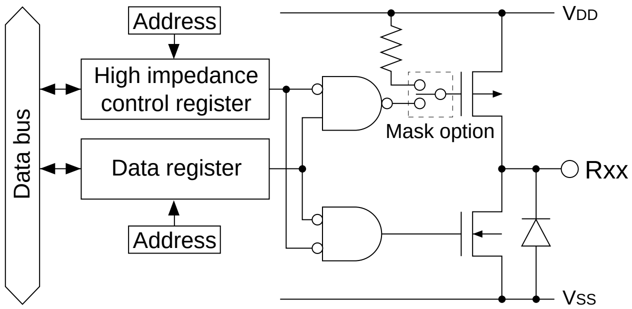
(2) The K13 terminal functions as the clock input terminal for the programmable timer, and the input signal is shared with the input port and the programmable timer. Therefore, when the K13 terminal is set to the clock input terminal for the programmable timer, take care of the interrupt setting.

(3) After an interrupt occurs, the same interrupt will occur again if the interrupt enabled state (I flag = "1") is set or the RETI instruction is executed unless the interrupt factor flag is reset. Therefore, be sure to reset (write "1" to) the interrupt factor flag in the interrupt service routine before shifting to the interrupt enabled state.

4.6 Output Ports (R00–R03, R10–R13 and R20–R23)

4.6.1 Configuration of output ports

The E0C63158 has 12 bits general output ports.
Output specifications of the output ports can be selected individually with the mask option. Two kinds of output specifications are available: complementary output and N-channel open drain output.
Figure 4.6.1.1 shows the configuration of the output port.



(R00–R03 are fixed at complementary output.)

Fig. 4.6.1.1 Configuration of output port

The R02 and R03 output terminals are shared with special output terminals (TOUT, FOUT), and this function is selected by the software.
At initial reset, these are all set to the general purpose output port.
Table 4.6.1.1 shows the setting of the output terminals by function selection.

Table 4.6.1.1 Function setting of output terminals

Terminal name	Terminal status at initial reset	Special output	
		TOUT	FOUT
R00	R00 (High output)	R00	R00
R01	R01 (High output)	R01	R01
R02	R02 (High output)	TOUT	
R03	R03 (High output)		FOUT
R10–R13	R10–R13 (High output)	R10–R13	R10–R13
R20–R23	R20–R23 (High output)	R20–R23	R20–R23

When using the output port (R02, R03) as the special output port, the data register must be fixed at "1" and the high impedance control register must be fixd at "0" (data output).

4.6.2 Mask option

Output specifications of the output ports can be selected with the mask option.
Either complementary output or N-channel open drain output may be selected as the output specification of the output ports. The selection is done in 1-bit units or 4-bit units according to the output port.

1-bit unit: R00, R01, R02, R03
4-bit unit: R10–R13, R20–R23

However, when N-channel open drain output is selected, do not apply a voltage exceeding the power supply voltage to the output port.

4.6.3 High impedance control

The terminal output status of the output ports can be set to a high impedance status. This control is done using the high impedance control registers.
The high impedance control registers are provided to correspond with the output ports as shown below.

High impedance control register	Corresponding output port
R00HIZ	R00 (1-bit)
R01HIZ	R01 (1-bit)
R02HIZ	R02 (1-bit)
R03HIZ	R03 (1-bit)
R1HIZ	R10–R13 (4-bit)
R2HIZ	R20–R23 (4-bit)

When "1" is written to the high impedance control register, the corresponding output port terminal goes into high impedance status. When "0" is written, the port outputs a signal according to the data register.

4.6.4 Special output

In addition to the regular DC output, special output can be selected for the output ports R02 and R03 as shown in Table 4.6.4.1 with the software.
Figure 4.6.4.1 shows the configuration of the R02 and R03 output ports.

Table 4.6.4.1 Special output

Terminal	Special output	Output control register
R03	FOUT	FOUTE
R02	TOUT	PTOUT

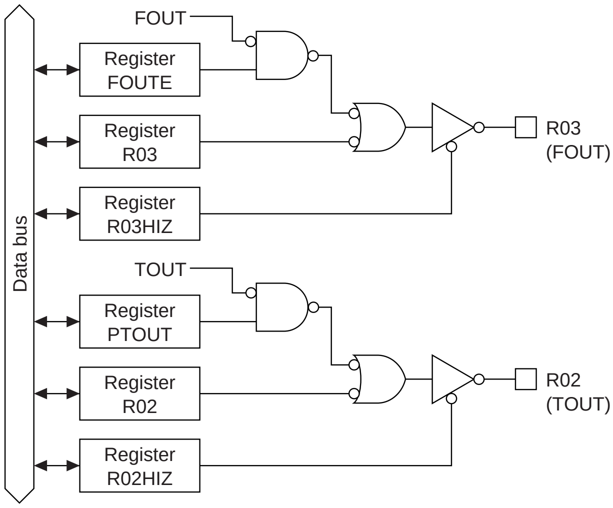


Fig. 4.6.4.1 Configuration of R02 and R03 output ports

At initial reset, the output port data register is set to "1" and the high impedance control register is set to "0". Consequently, the output terminal goes high (V_{DD}).
When using the output port (R02, R03) as the special output port, fix the data register (R02, R03) at "1" and the high impedance control register (R02HIZ, R03HIZ) at "0" (data output). The respective signal should be turned ON and OFF using the special output control register.

Note: • *Be aware that the output terminal is fixed at a low (Vss) level the same as the DC output if "0" is written to the R02 and R03 registers when the special output has been selected.*

• *Be aware that the output terminal shifts into high impedance status when "1" is written to the high impedance control register (R02HIZ, R03HIZ).*

- **TOUT (R02)**

The R02 terminal can output a TOUT signal.
The TOUT signal is the clock that is output from the programmable timer, and can be used to provide a clock signal to an external device.
To output the TOUT signal, fix the R02 register at "1" and the R02HIZ register at "0", and turn the signal ON and OFF using the PTOUT register. It is, however, necessary to control the programmable timer.
Refer to Section 4.10, "Programmable Timer" for details of the programmable timer.

Note: A hazard may occur when the TOUT signal is turned ON and OFF.

Figure 4.6.4.2 shows the output waveform of the TOUT signal.

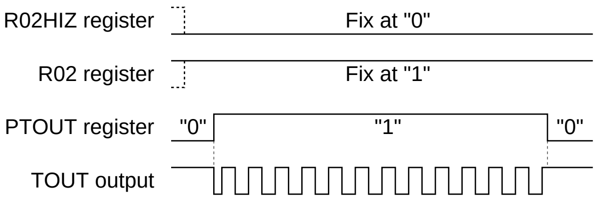


Fig. 4.6.4.2 Output waveform of TOUT signal

- **FOUT (R03)**

The R03 terminal can output a FOUT signal.
The FOUT signal is a clock (f_{OSC1} or f_{OSC3}) that is output from the oscillation circuit or a clock that the f_{OSC1} clock has divided in the internal circuit, and can be used to provide a clock signal to an external device.
To output the FOUT signal, fix the R03 register at "1" and the R03HIZ register at "0", and turn the signal ON and OFF using the FOUTE register.
The frequency of the output clock may be selected from among 4 types shown in Table 4.6.4.2 by setting the FOFQ0 and FOFQ1 registers.

Table 4.6.4.2 FOUT clock frequency

FOFQ1	FOFQ0	Clock frequency
1	1	f_{OSC3}
1	0	f_{OSC1}
0	1	$f_{OSC1} \times 1/8$
0	0	$f_{OSC1} \times 1/64$

f_{OSC1}: Clock that is output from the OSC1 oscillation circuit
f_{OSC3}: Clock that is output from the OSC3 oscillation circuit

When f_{OSC3} is selected for the FOUT signal frequency, it is necessary to control the OSC3 oscillation circuit before output.
Refer to Section 4.4, "Oscillation Circuit", for the control and notes.

Note: A hazard may occur when the FOUT signal is turned ON and OFF.

Figure 4.6.4.3 shows the output waveform of the FOUT signal.

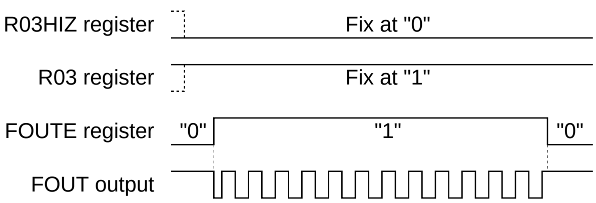


Fig. 4.6.4.3 Output waveform of FOUT signal

4.6.5 I/O memory of output ports

Table 4.6.5.1 shows the I/O addresses and control bits for the output ports.

Table 4.6.5.1 Control bits of output ports

Address	Register								Comment
	D3	D2	D1	D0	Name	Init *1	1	0	
FF06H	FOUTE	0	FOFQ1	FOFQ0	FOUTE	0	Enable	Disable	FOUT output enable
	R/W	R	R/W		0 *3	– *2			Unused
					FOFQ1	0			FOUT frequency selection: [FOFQ1, 0] 0 / 1 / 2 / 3 — Frequency $f_{OSC1}/64$ / $f_{OSC1}/8$ / f_{OSC1} / f_{OSC3}
					FOFQ0	0			
FF30H	R03HIZ	R02HIZ	R01HIZ	R00HIZ	R03HIZ	0	High-Z	Output	R03 output high impedance control (FOUTE=0) FOUT output high impedance control (FOUTE=1)
	R/W				R02HIZ	0	High-Z	Output	R02 output high impedance control (PTOUT=0) TOUT output high impedance control (PTOUT=1)
					R01HIZ	0	High-Z	Output	R01 output high impedance control
					R00HIZ	0	High-Z	Output	R00 output high impedance control
FF31H	R03	R02	R01	R00	R03	1	High	Low	R03 output port data (FOUTE=0) Fix at "1" when FOUT is used
	R/W				R02	1	High	Low	R02 output port data (PTOUT=0) Fix at "1" when TOUT is used
					R01	1	High	Low	R01 output port data
					R00	1	High	Low	R00 output port data
FF32H	0	0	0	R1HIZ	0 *3	– *2			Unused
	R			R/W	0 *3	– *2			Unused
					0 *3	– *2			Unused
					R1HIZ	0	High-Z	Output	R1 output high impedance control
FF33H	R13	R12	R11	R10	R13	1	High	Low	R10–R13 output port data
	R/W				R12	1	High	Low	
					R11	1	High	Low	
					R10	1	High	Low	
FF34H	0	0	0	R2HIZ	0 *3	– *2			Unused
	R			R/W	0 *3	– *2			Unused
					0 *3	– *2			Unused
					R2HIZ	0	High-Z	Output	R2 output high impedance control
FF35H	R23	R22	R21	R20	R23	1	High	Low	R20–R23 output port data
	R/W				R22	1	High	Low	
					R21	1	High	Low	
					R20	1	High	Low	
FFC1H	CHSEL	PTOUT	CKSEL1	CKSEL0	CHSEL	0	Timer1	Timer0	TOUT output channel selection
	R/W				PTOUT	0	On	Off	TOUT output control
					CKSEL1	0	OSC3	OSC1	Prescaler 1 source clock selection
					CKSEL0	0	OSC3	OSC1	Prescaler 0 source clock selection

*1 Initial value at initial reset
*2 Not set in the circuit
*3 Constantly "0" when being read

R00HIZ–R03HIZ: R0 port high impedance control register (FF30H)
R1HIZ: R1 port high impedance control register (FF32H•D0)
R2HIZ: R2 port high impedance control register (FF34H•D0)

Controls high impedance output of the output port.

When "1" is written: High impedance
When "0" is written: Data output
Reading: Valid

By writing "0" to the high impedance control register, the corresponding output terminal outputs according to the data register. When "1" is written, it shifts into high impedance status.
When the output ports R02 and R03 are used for special output (TOUT, FOUT), fix the R02HIZ register and the R03HIZ register at "0" (data output).
At initial reset, these registers are set to "0".

R00–R03: R0 output port data register (FF31H)
R10–R13: R1 output port data register (FF33H)
R20–R23: R2 output port data register (FF35H)

Set the output data for the output ports.

When "1" is written: High level output
When "0" is written: Low level output
Reading: Valid

The output port terminals output the data written in the corresponding data registers without changing it. When "1" is written to the register, the output port terminal goes high (V_{DD}), and when "0" is written, the output port terminal goes low (V_{SS}).
When the output ports R02 and R03 are used for special output (TOUT, FOUT), fix the R02 register and the R03 register at "1".
At initial reset, these registers are all set to "1".

FOUTE: FOUT output control register (FF06H•D3)

Controls the FOUT output.

When "1" is written: FOUT output ON
When "0" is written: FOUT output OFF
Reading: Valid

By writing "1" to the FOUTE register when the R03 register has been set to "1" and the R03HIZ register has been set to "0", an FOUT signal is output from the R03 terminal. When "0" is written, the R03 terminal goes high (V_{DD}).
When using the R03 output port for DC output, fix this register at "0".
At initial reset, this register is set to "0".

FOFQ0, FOFQ1: FOUT frequency selection register (FF06H•D0, D1)

Selects a frequency of the FOUT signal.

Table 4.6.5.2 FOUT clock frequency

FOFQ1	FOFQ0	Clock frequency
1	1	f_{OSC3}
1	0	f_{OSC1}
0	1	$f_{OSC1} \times 1/8$
0	0	$f_{OSC1} \times 1/64$

At initial reset, this register is set to "0".

PTOUT: TOUT output control register (FFC1H•D2)

Controls the TOUT output.

When "1" is written: TOUT output ON
When "0" is written: TOUT output OFF
Reading: Valid

By writing "1" to the PTOUT register when the R02 register has been set to "1" and the R02HIZ register has been set to "0", the TOUT signal is output from the R02 terminal. When "0" is written, the R02 terminal goes high (V_{DD}).
When using the R02 output port for DC output, fix this register at "0".
At initial reset, this register is set to "0".

4.6.6 Programming notes

(1) When using the output port (R02, R03) as the special output port, fix the data register (R02, R03) at "1" and the high impedance control register (R02HIZ, R03HIZ) at "0" (data output).
Be aware that the output terminal is fixed at a low (V_{SS}) level the same as the DC output if "0" is written to the R02 and R03 registers when the special output has been selected.
Be aware that the output terminal shifts into high impedance status when "1" is written to the high impedance control register (R02HIZ, R03HIZ).

(2) A hazard may occur when the FOUT signal and the TOUT signal are turned ON and OFF.

(3) When f_{OSC3} is selected for the FOUT signal frequency, it is necessary to control the OSC3 oscillation circuit before output.
Refer to Section 4.4, "Oscillation Circuit", for the control and notes.

4.7 I/O Ports (P00–P03, P10–P13, P20–P23, P30–P33 and P40–P43)

4.7.1 Configuration of I/O ports

The E0C63158 has 20 bits general-purpose I/O ports. Figure 4.7.1.1 shows the configuration of the I/O port.

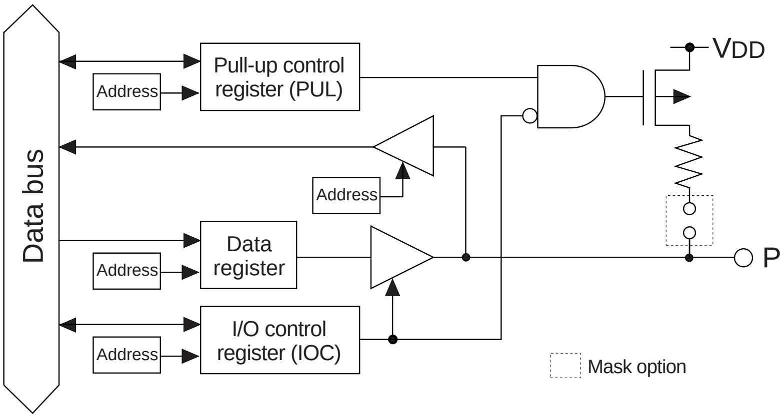


Fig. 4.7.1.1 Configuration of I/O port

The P10–P13 I/O port terminals are shared with the serial interface input/output terminals and this function is selected by the software. The P40–P43 I/O port terminals are shared with the A/D converter input terminals and this function is also selected by the software.
At initial reset, these are all set to the I/O port.
Table 4.7.1.1 shows the setting of the input/output terminals by function selection.

Table 4.7.1.1 Function setting of input/output terminals

Terminal name	Terminal status at initial reset	Serial I/F		A/D converter
		Master	Slave	
P00–P03	P00–P03 (Input & pull-up)	P00–P03	P00–P03	P00–P03
P10	P10 (Input & pull-up ∗)	SIN(I)	SIN(I)	
P11	P11 (Input & pull-up ∗)	SOUT(O)	SOUT(O)	
P12	P12 (Input & pull-up ∗)	$\overline{\text{SCLK}}$(O)	$\overline{\text{SCLK}}$(I)	
P13	P13 (Input & pull-up ∗)	P13	$\overline{\text{SRDY}}$(O)	
P20–P23	P20–P23 (Input & pull-up ∗)	P20–P23	P20–P23	P20–P23
P30–P33	P30–P33 (Input & pull-up ∗)	P30–P33	P30–P33	P30–P33
P40	P40 (Input & Pull-up ∗)			AD0(I)
P41	P41 (Input & Pull-up ∗)			AD1(I)
P42	P42 (Input & Pull-up ∗)			AD2(I)
P43	P43 (Input & Pull-up ∗)			AD3(I)

∗ When "with pull-up resistor" is selected by the mask option (high impedance when "gate direct" is set)

When these ports are used as I/O ports, the ports can be set to either input mode or output mode (in 1-bit unit). Modes can be set by writing data to the I/O control registers.
Refer to Section 4.11, "Serial Interface", for control of the serial interface.
Refer to Section 4.9, "A/D Converter", for control of the A/D converter.

4.7.2 Mask option

In the I/O ports, the output specification during output mode can be selected from either complementary output or N-channel open drain output by mask option. The mask option also enables selection of whether the pull-up resistor is used or not during input mode. They are selected in 1-bit units or 4-bit units according to the terminal group.

Ports to be selected in 1-bit units: P20, P21, P22, P23, P40, P41, P42, P43
Ports to be selected in 4-bit units: P00–P03, P10–P13, P30–P33

When N-channel open drain output is selected, do not apply a voltage exceeding the power supply voltage to the port.
When "without pull-up" during the input mode is selected, take care that the floating status does not occur.

This option is effective even when I/O ports are used for input/output of the serial interface or input of the A/D converter. When using the A/D converter, select "N-channel open drain" and "without pull-up" for the port corresponding to the A/D channel to be used.

4.7.3 I/O control registers and input/output mode

Input or output mode can be set for the I/O ports by writing data into the corresponding I/O control registers IOCxx.

To set the input mode, write "0" to the I/O control register. When an I/O port is set to input mode, it becomes high impedance status and works as an input port.
However, when the pull-up explained in the following section has been set by software, the input line is pulled up only during this input mode.

To set the output mode, write "1" is to the I/O control register. When an I/O port is set to output mode , it works as an output port, it outputs a high level (V_{DD}) when the port output data is "1", and a low level (V_{SS}) when the port output data is "0".

If perform the read out in each mode; when output mode, the register value is read out, and when input mode, the port value is read out.

At initial reset, the I/O control registers are set to "0", and the I/O ports enter the input mode.

The I/O control registers of the ports that are set as input/output for the serial interface and A/D converter can be used as general purpose registers that do not affect the I/O control. (See Table 4.7.1.1.)

4.7.4 Pull-up during input mode

A pull-up resistor that operates during the input mode is built into each I/O port of the E0C63158. Mask option can set the use or non-use of this pull-up. The pull-up resistor becomes effective by writing "1" to the pull-up control register PULxx that corresponds to each port, and the input line is pulled up during the input mode. When "0" has been written, no pull-up is done.
At initial reset, the pull-up control registers are set to "1".
The pull-up control registers of the ports in which "without pull-up" have been selected can be used as general purpose registers. Even when "with pull-up" has been selected, the pull-up control registers of the ports that are set as input/output for the serial interface can be used as general purpose registers that do not affect the pull-up control. (See Table 4.7.1.1.)
The pull-up control registers of the port, that are set as input for the serial interface, function the same as the I/O port.

4.7.5 I/O memory of I/O ports

Tables 4.7.5.1(a) and (b) show the I/O addresses and the control bits for the I/O ports.

Table 4.7.5.1(a) Control bits of I/O ports (1)

Address	Register D3	Register D2	Register D1	Register D0	Name	Init *1	1	0	Comment
FF40H	IOC03	IOC02	IOC01	IOC00	IOC03	0	Output	Input	P00–P03 I/O control register
	R/W				IOC02	0	Output	Input	
					IOC01	0	Output	Input	
					IOC00	0	Output	Input	
FF41H	PUL03	PUL02	PUL01	PUL00	PUL03	1	On	Off	P00–P03 pull-up control register
	R/W				PUL02	1	On	Off	
					PUL01	1	On	Off	
					PUL00	1	On	Off	
FF42H	P03	P02	P01	P00	P03	– *2	High	Low	P00–P03 I/O port data
	R/W				P02	– *2	High	Low	
					P01	– *2	High	Low	
					P00	– *2	High	Low	
FF44H	IOC13	IOC12	IOC11	IOC10	IOC13	0	Output	Input	P13 I/O control register functions as a general-purpose register when SIF (slave) is selected
	R/W				IOC12	0	Output	Input	P12 I/O control register (EISF=0) functions as a general-purpose register when SIF is selected
					IOC11	0	Output	Input	P11 I/O control register (EISF=0) functions as a general-purpose register when SIF is selected
					IOC10	0	Output	Input	P10 I/O control register (EISF=0) functions as a general-purpose register when SIF is selected
FF45H	PUL13	PUL12	PUL11	PUL10	PUL13	1	On	Off	P13 pull-up control register functions as a general-purpose register when SIF (slave) is selected
	R/W				PUL12	1	On	Off	P12 pull-up control register (EISF=0) functions as a general-purpose register when SIF (master) is selected $\overline{\text{SCLK}}$ (I) pull-up control register when SIF (slave) is selected
					PUL11	1	On	Off	P11 pull-up control register (EISF=0) functions as a general-purpose register when SIF is selected
					PUL10	1	On	Off	P10 pull-up control register (EISF=0) SIN pull-up control register when SIF is selected
FF46H	P13	P12	P11	P10	P13	– *2	High	Low	P13 I/O port data functions as a general-purpose register when SIF (slave) is selected
	R/W				P12	– *2	High	Low	P12 I/O port data (EISF=0) functions as a general-purpose register when SIF is selected
					P11	– *2	High	Low	P11 I/O port data (EISF=0) functions as a general-purpose register when SIF is selected
					P10	– *2	High	Low	P10 I/O port data (EISF=0) functions as a general-purpose register when SIF is selected
FF48H	IOC23	IOC22	IOC21	IOC20	IOC23	0	Output	Input	P20–P23 I/O control register
	R/W				IOC22	0	Output	Input	
					IOC21	0	Output	Input	
					IOC20	0	Output	Input	
FF49H	PUL23	PUL22	PUL21	PUL20	PUL23	1	On	Off	P20–P23 pull-up control register
	R/W				PUL22	1	On	Off	
					PUL21	1	On	Off	
					PUL20	1	On	Off	
FF4AH	P23	P22	P21	P20	P23	– *2	High	Low	P20–P23 I/O port data
					P22	– *2	High	Low	
					P21	– *2	High	Low	
					P20	– *2	High	Low	
FF4CH	IOC33	IOC32	IOC31	IOC30	IOC33	0	Output	Input	P30–P33 I/O control register
	R/W				IOC32	0	Output	Input	
					IOC31	0	Output	Input	
					IOC30	0	Output	Input	

*1 Initial value at initial reset
*2 Not set in the circuit
*3 Constantly "0" when being read

Table 4.7.5.1(b) Control bits of I/O ports (2)

Address	Register D3	Register D2	Register D1	Register D0	Name	Init *1	1	0	Comment
FF4DH	PUL33	PUL32	PUL31	PUL30	PUL33	1	On	Off	P30–P33 pull-up control register
	R/W				PUL32	1	On	Off	
					PUL31	1	On	Off	
					PUL30	1	On	Off	
FF4EH	P33	P32	P31	P30	P33	– *2	High	Low	P30–P33 I/O port data
	R/W				P32	– *2	High	Low	
					P31	– *2	High	Low	
					P30	– *2	High	Low	
FF50H	IOC43	IOC42	IOC41	IOC40	IOC43	0	Output	Input	P43 I/O control register (PAD3=0) functions as a general-purpose register when A/D is enabled
	R/W				IOC42	0	Output	Input	P42 I/O control register (PAD2=0) functions as a general-purpose register when A/D is enabled
					IOC41	0	Output	Input	P41 I/O control register (PAD1=0) functions as a general-purpose register when A/D is enabled
					IOC40	0	Output	Input	P40 I/O control register (PAD0=0) functions as a general-purpose register when A/D is enabled
FF51H	PUL43	PUL42	PUL41	PUL40	PUL43	1	On	Off	P43 pull-up control register (PAD3=0) functions as a general-purpose register when A/D is enabled
	R/W				PUL42	1	On	Off	P42 pull-up control register (PAD2=0) functions as a general-purpose register when A/D is enabled
					PUL41	1	On	Off	P41 pull-up control register (PAD1=0) functions as a general-purpose register when A/D is enabled
					PUL40	1	On	Off	P40 pull-up control register (PAD0=0) functions as a general-purpose register when A/D is enabled
FF52H	P43	P42	P41	P40	P43	– *2	High	Low	P43 I/O port data (PAD3=0) functions as a general-purpose register when A/D is enabled
	R/W				P42	– *2	High	Low	P42 I/O port data (PAD2=0) functions as a general-purpose register when A/D is enabled
					P41	– *2	High	Low	P41 I/O port data (PAD1=0) functions as a general-purpose register when A/D is enabled
					P40	– *2	High	Low	P40 I/O port data (PAD0=0) functions as a general-purpose register when A/D is enabled
FF70H	0	ESOUT	SCTRG	ESIF	0 *3	– *2			Unused
	R	R/W			ESOUT	0	Enable	Disable	SOUT enable/disable control
					SCTRG	0	Trigger	Invalid	Serial I/F clock trigger (writing)
							Run	Stop	Serial I/F clock status (reading)
					ESIF	0	SIF	I/O	Serial I/F enable (P1 port function selection)
FFD1H	PAD3	PAD2	PAD1	PAD0	PAD3	0	Enable	Disable	P43 input channel enable/disable control
	R/W				PAD2	0	Enable	Disable	P42 input channel enable/disable control
					PAD1	0	Enable	Disable	P41 input channel enable/disable control
					PAD0	0	Enable	Disable	P40 input channel enable/disable control

*1 Initial value at initial reset
*2 Not set in the circuit
*3 Constantly "0" when being read

ESIF: Serial interface enable register (FF70H•D0)

Selects function for P10–P13.

When "1" is written: Serial interface input/output port
When "0" is written: I/O port
Reading: Valid

When using the serial interface, write "1" to this register and when P10–P13 are used as the I/O port, write "0". The configuration of the terminals within P10–P13 that are used for the serial interface is decided by the mode selected with the SCS1 and SCS0 registers (see Section 4.11).
In the slave mode, all the P10–P13 ports are set to the serial interface input/output port. In the master mode, P10–P12 are set to the serial interface input/output port and P13 can be used as the I/O port.
At initial reset, this register is set to "0".

PAD0–PAD3: A/D input channel enable/disable control register (FFD1H)

Selects function for P40–P43.

When "1" is written: A/D converter input
When "0" is written: I/O port
Reading: Valid

When using the A/D converter, write "1" to the register. PAD0–PAD3 correspond to P40–P43, respectively. When using a port from P40 to P43 as an I/O port, write "0" to the corresponding PAD register.
At initial reset, this register is set to "0".

P00–P03: P0 I/O port data register (FF42H)
P10–P13: P1 I/O port data register (FF46H)
P20–P23: P2 I/O port data register (FF4AH)
P30–P33: P3 I/O port data register (FF4EH)
P40–P43: P4 I/O port data register (FF52H)

I/O port data can be read and output data can be set through these registers.

• ***When writing data***

When "1" is written: High level
When "0" is written: Low level

When an I/O port is set to the output mode, the written data is output unchanged from the I/O port terminal. When "1" is written as the port data, the port terminal goes high (V_{DD}), and when "0" is written, the terminal goes low (V_{SS}).
Port data can be written also in the input mode.

• ***When reading data***

When "1" is read: High level
When "0" is read: Low level

The terminal voltage level of the I/O port is read out. When the I/O port is in the input mode the voltage level being input to the port terminal can be read out; in the output mode the register value can be read. When the terminal voltage is high (V_{DD}) the port data that can be read is "1", and when the terminal voltage is low (V_{SS}) the data is "0".
When "with pull-up resistor" has been selected with the mask option and the PUL register is set to "1", the built-in pull-up resister goes ON during input mode, so that the I/O port terminal is pulled up.

The data registers of the ports that are set as input/output for the serial interface or A/D converter can be used as general purpose registers that do not affect the input/output.

Note: When in the input mode, I/O ports are changed from low to high by pull-up resistor, the rise of the waveform is delayed on account of the time constant of the pull-up resistor and input gate capacitance. Hence, when fetching input ports, set an appropriate wait time.
Particular care needs to be taken of the key scan during key matrix configuration.
Make this waiting time the amount of time or more calculated by the following expression.
$10 \times C \times R$
C: terminal capacitance 5 pF + parasitic capacitance ? pF
R: pull-up resistance 300 kΩ

IOC00–IOC03: P0 port I/O control register (FF40H)
IOC10–IOC13: P1 port I/O control register (FF44H)
IOC20–IOC23: P2 port I/O control register (FF48H)
IOC30–IOC33: P3 port I/O control register (FF4CH)
IOC40–IOC43: P4 port I/O control register (FF50H)

The input and output modes of the I/O ports are set with these registers.

When "1" is written: Output mode
When "0" is written: Input mode
Reading: Valid

The input and output modes of the I/O ports are set in 1-bit unit.
Writing "1" to the I/O control register makes the corresponding I/O port enter the output mode, and writing "0" induces the input mode.
At initial reset, these registers are all set to "0", so the I/O ports are in the input mode.
The I/O control registers of the ports that are set as input/output for the serial interface or A/D converter can be used as general purpose registers that do not affect the input/output.

PUL00–PUL03: P0 port pull-up control register (FF41H)
PUL10–PUL13: P1 port pull-up control register (FF45H)
PUL20–PUL23: P2 port pull-up control register (FF49H)
PUL30–PUL33: P3 port pull-up control register (FF4DH)
PUL40–PUL43: P4 port pull-up control register (FF51H)

The pull-up during the input mode are set with these registers.

When "1" is written: Pull-up ON
When "0" is written: Pull-up OFF
Reading: Valid

The built-in pull-up resistor which is turned ON during input mode is set to enable in 1-bit units. (The pull-up resistor is included into the ports selected by the mask option.)
By writing "1" to the pull-up control register, the corresponding I/O ports are pulled up (during input mode), while writing "0" turns the pull-up function OFF.
At initial reset, these registers are all set to "1", so the pull-up function is set to ON.

The pull-up control registers of the ports in which the pull-up resistor is not included become the general purpose register. The registers of the ports that are set as input/output for the serial interface or A/D converter can also be used as general purpose registers that do not affect the pull-up control.
The pull-up control registers of the port that are set as input for the serial interface function the same as the I/O port.

4.7.6 Programming note

When in the input mode, I/O ports are changed from low to high by pull-up resistor, the rise of the waveform is delayed on account of the time constant of the pull-up resistor and input gate capacitance. Hence, when fetching input ports, set an appropriate wait time.
Particular care needs to be taken of the key scan during key matrix configuration.
Make this waiting time the amount of time or more calculated by the following expression.

$10 \times C \times R$

C: terminal capacitance 5 pF + parasitic capacitance ? pF
R: pull-up resistance 300 kΩ

4.8 Clock Timer

4.8.1 Configuration of clock timer

The E0C63158 has a built-in clock timer that uses OSC1 (crystal oscillator) as the source oscillator. The clock timer is configured of an 8-bit binary counter that serves as the input clock, fOSC1 divided clock output from the prescaler. Timer data (128–16 Hz and 8–1 Hz) can be read out by the software.
Figure 4.8.1.1 is the block diagram for the clock timer.

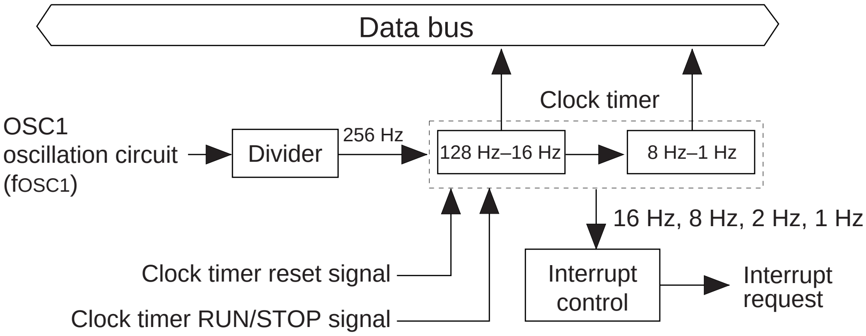


Fig. 4.8.1.1 Block diagram for the clock timer

Ordinarily, this clock timer is used for all types of timing functions such as clocks.

Note: When the CR oscillation circuit is selected as the OSC1 oscillation circuit by mask option, the frequencies and times differ from the values described in this section because the oscillation frequency will be 60 kHz (Typ.). Therefore, the clock timer can not be used for the clock function.

4.8.2 Data reading and hold function

The 8 bits timer data are allocated to the address FF79H and FF7AH.

<FF79H>	D0: TM0 = 128 Hz	D1: TM1 = 64 Hz	D2: TM2 = 32 Hz	D3: TM3 = 16 Hz
<FF7AH>	D0: TM4 = 8 Hz	D1: TM5 = 4 Hz	D2: TM6 = 2 Hz	D3: TM7 = 1 Hz

Since the clock timer data has been allocated to two addresses, a carry is generated from the low-order data within the count (TM0–TM3: 128–16 Hz) to the high-order data (TM4–TM7: 8–1 Hz). When this carry is generated between the reading of the low-order data and the high-order data, a content combining the two does not become the correct value (the low-order data is read as FFH and the high-order data becomes the value that is counted up 1 from that point).
The high-order data hold function in the E0C63158 is designed to operate to avoid this. This function temporarily stops the counting up of the high-order data (by carry from the low-order data) at the point where the low-order data has been read and consequently the time during which the high-order data is held is the shorter of the two indicated here following.

1. Period until it reads the high-order data.
2. 0.48–1.5 msec, fOSC1 = 32.768 kHz (Varies due to the read timing.)

Note: Since the low-order data is not held when the high-order data has previously been read, the low-order data should be read first.

4.8.3 Interrupt function

The clock timer can cause interrupts at the falling edge of 16 Hz, 8 Hz, 2 Hz and 1 Hz signals. Software can set whether to mask any of these frequencies.
Figure 4.8.3.1 is the timing chart of the clock timer.

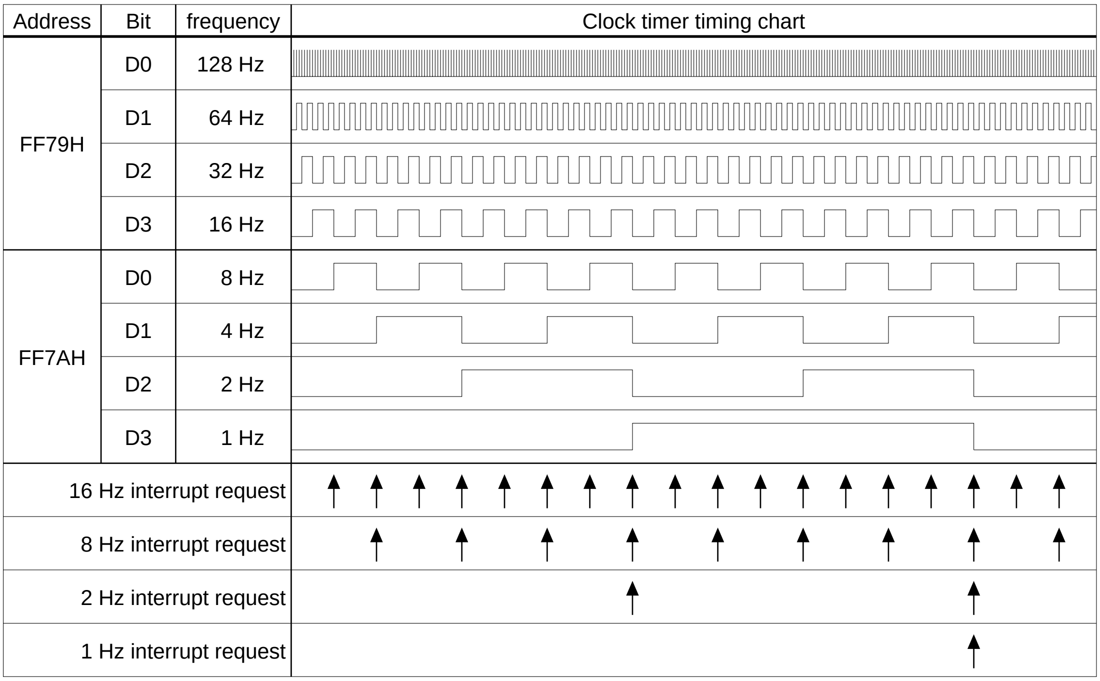


Fig. 4.8.3.1 Timing chart of clock timer

As shown in Figure 4.8.3.1, interrupt is generated at the falling edge of the frequencies (16 Hz, 8 Hz, 2 Hz, 1 Hz). At this time, the corresponding interrupt factor flag (IT0, IT1, IT2, IT3) is set to "1". Selection of whether to mask the separate interrupts can be made with the interrupt mask registers (EIT0, EIT1, EIT2, EIT3). However, regardless of the interrupt mask register setting, the interrupt factor flag is set to "1" at the falling edge of the corresponding signal.

4.8.4 I/O memory of clock timer

Table 4.8.4.1 shows the I/O addresses and the control bits for the clock timer.

Table 4.8.4.1 Control bits of clock timer

Address	Register D3	Register D2	Register D1	Register D0	Name	Init *1	1	0	Comment
FF78H	0	0	TMRST	TMRUN	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R		W	R/W	TMRST*3	Reset	Reset	Invalid	Clock timer reset (writing)
					TMRUN	0	Run	Stop	Clock timer Run/Stop
FF79H	TM3	TM2	TM1	TM0	TM3	0			Clock timer data (16 Hz)
					TM2	0			Clock timer data (32 Hz)
	R				TM1	0			Clock timer data (64 Hz)
					TM0	0			Clock timer data (128 Hz)
FF7AH	TM7	TM6	TM5	TM4	TM7	0			Clock timer data (1 Hz)
					TM6	0			Clock timer data (2 Hz)
	R				TM5	0			Clock timer data (4 Hz)
					TM4	0			Clock timer data (8 Hz)
FFE6H	EIT3	EIT2	EIT1	EIT0	EIT3	0	Enable	Mask	Interrupt mask register (Clock timer 1 Hz)
					EIT2	0	Enable	Mask	Interrupt mask register (Clock timer 2 Hz)
	R/W				EIT1	0	Enable	Mask	Interrupt mask register (Clock timer 8 Hz)
					EIT0	0	Enable	Mask	Interrupt mask register (Clock timer 16 Hz)
FFF6H	IT3	IT2	IT1	IT0	IT3	0	(R)	(R)	Interrupt factor flag (Clock timer 1 Hz)
					IT2	0	Yes	No	Interrupt factor flag (Clock timer 2 Hz)
	R/W				IT1	0	(W)	(W)	Interrupt factor flag (Clock timer 8 Hz)
					IT0	0	Reset	Invalid	Interrupt factor flag (Clock timer 16 Hz)

*1 Initial value at initial reset

*2 Not set in the circuit

*3 Constantly "0" when being read

TM0–TM7: Timer data (FF79H, FF7AH)

The 128–1 Hz timer data of the clock timer can be read out with these registers. These eight bits are read only, and writing operations are invalid.

By reading the low-order data (FF79H), the high-order data (FF7AH) is held until reading or for 0.48–1.5 msec (one of shorter of them).

At initial reset, the timer data is initialized to "00H".

TMRST: Clock timer reset (FF78H•D1)

This bit resets the clock timer.

When "1" is written: Clock timer reset
When "0" is written: No operation
Reading: Always "0"

The clock timer is reset by writing "1" to TMRST. When the clock timer is reset in the RUN status, operation restarts immediately. Also, in the STOP status the reset data is maintained. No operation results when "0" is written to TMRST.

This bit is write-only, and so is always "0" at reading.

TMRUN: Clock timer RUN/STOP control register (FF78H•D0)
Controls RUN/STOP of the clock timer.

When "1" is written: RUN
When "0" is written: STOP
Reading: Valid

The clock timer enters the RUN status when "1" is written to the TMRUN register, and the STOP status when "0" is written.
In the STOP status, the timer data is maintained until the next RUN status or the timer is reset. Also, when the STOP status changes to the RUN status, the data that is maintained can be used for resuming the count.
At initial reset, this register is set to "0".

EIT0: 16 Hz interrupt mask register (FFE6H•D0)
EIT1: 8 Hz interrupt mask register (FFE6H•D1)
EIT2: 2 Hz interrupt mask register (FFE6H•D2)
EIT3: 1 Hz interrupt mask register (FFE6H•D3)
These registers are used to select whether to mask the clock timer interrupt.

When "1" is written: Enabled
When "0" is written: Masked
Reading: Valid

The interrupt mask registers (EIT0, EIT1, EIT2, EIT3) are used to select whether to mask the interrupt to the separate frequencies (16 Hz, 8 Hz, 2 Hz, 1 Hz).
At initial reset, these registers are set to "0".

IT0: 16 Hz interrupt factor flag (FFF6H•D0)
IT1: 8 Hz interrupt factor flag (FFF6H•D1)
IT2: 2 Hz interrupt factor flag (FFF6H•D2)
IT3: 1 Hz interrupt factor flag (FFF6H•D3)
These flags indicate the status of the clock timer interrupt.

When "1" is read: Interrupt has occurred
When "0" is read: Interrupt has not occurred

When "1" is written: Flag is reset
When "0" is written: Invalid

The interrupt factor flags (IT0, IT1, IT2, IT3) correspond to the clock timer interrupts of the respective frequencies (16 Hz, 8 Hz, 2 Hz, 1 Hz). The software can judge from these flags whether there is a clock timer interrupt. However, even if the interrupt is masked, the flags are set to "1" at the falling edge of the signal.
These flags are reset to "0" by writing "1" to them.
After an interrupt occurs, the same interrupt will occur again if the interrupt enabled state (I flag = "1") is set or the RETI instruction is executed unless the interrupt factor flag is reset. Therefore, be sure to reset (write "1" to) the interrupt factor flag in the interrupt service routine before shifting to the interrupt enabled state.
At initial reset, these flags are set to "0".

4.8.5 Programming notes

(1) Be sure to read timer data in the order of low-order data (TM0–TM3) then high-order data (TM4–TM7).

(2) After an interrupt occurs, the same interrupt will occur again if the interrupt enabled state (I flag = "1") is set or the RETI instruction is executed unless the interrupt factor flag is reset. Therefore, be sure to reset (write "1" to) the interrupt factor flag in the interrupt service routine before shifting to the interrupt enabled state.

(3) When the CR oscillation circuit is selected as the OSC1 oscillation circuit by mask option, the frequencies and times differ from the values described in this section because the oscillation frequency will be 60 kHz (Typ.). Therefore, the clock timer can not be used for the clock function.

4.9 A/D Converter

4.9.1 Characteristics and configuration of A/D converter

The E0C63158 has a built-in A/D converter with the following characteristics.

- Conversion method: Successive-approximation type
- Resolution: 8 bits
  Maximum error: ±3 LSB, A/D clock: f ≤ 1 MHz
  (0.9 to 3.6 V, V_{C2} mode should be used if V_{DD} ≤ 1.6V)
- Input channels: Maximum 4 channels
- Conversion time: Minimum 21 µsec (during operation at 1 MHz)
- Setting of analog conversion voltage range is possible with reference voltage terminal (AV_{REF})
- A/D conversion result is possible to read from 8-bit data register
- Sample & hold circuit built-in
- A/D conversion completion generates an interrupt

Figure 4.9.1.1 shows the configuration of the A/D converter.

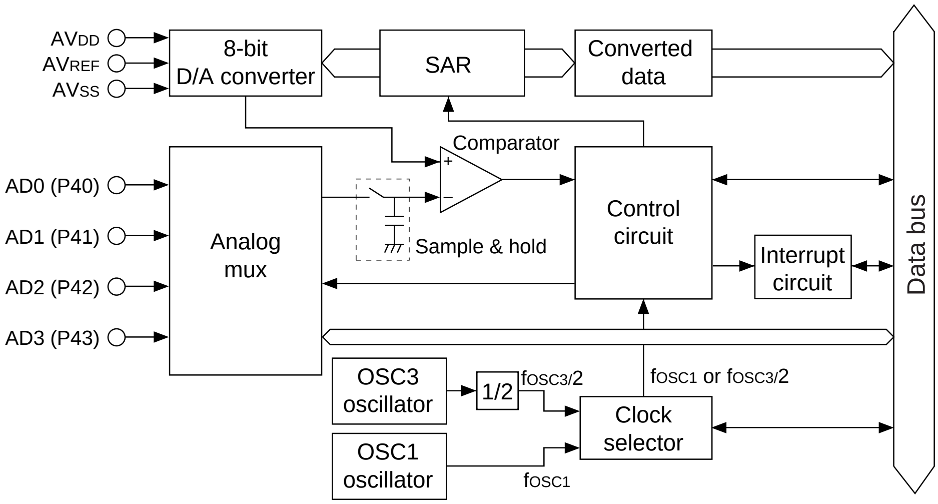


Fig. 4.9.1.1 Configuration of A/D converter

4.9.2 Terminal configuration of A/D converter

The terminals used with the A/D converter are as follows:

AV_{DD}, AV_{SS} (power supply terminal)

The AV_{DD} and AV_{SS} terminals are power supply terminals for the A/D converter. The voltage should be input as AV_{DD} ≤ V_{DD} and AV_{SS} = V_{SS}.

AV_{REF} (reference voltage input terminal)

The AV_{REF} terminal is the reference voltage terminal of the analog block. Input voltage range of the A/D conversion is decided by this input (AV_{SS}–AV_{REF}). The voltage should be input as AV_{REF} ≤ AV_{DD}.

AD0–AD3 (analog input terminal)

The analog input terminals AD0–AD3 are shared with the I/O port terminals P40–P43. Therefore, it is necessary to set them for the A/D converter by software when using them as analog input terminals. This setting can be done for each terminal. (Refer to Section 4.9.4 for setting.)
At initial reset, all the terminals are set in the I/O port terminals.
Analog voltage value AV_{IN} that can be input is in the range of AV_{SS} ≤ AV_{IN} ≤ AV_{REF}.

4.9.3 Mask option

The analog input terminals of the A/D converter are shared with the I/O port terminals P40–P43. Therefore, the terminal specification of the A/D converter is decided by setting the I/O port mask option. Select "Without pull-up" for the port corresponding to the channel to be used to obtain the conversion precision.

4.9.4 Control of A/D converter

(1) Setting of A/D input terminal

When using the A/D converter, it is necessary to set up the terminals used for analog input from the P40–P43 initialized as the I/O port terminals. Four terminals can all be used as analog input terminals.

The PAD (PAD0–PAD3) register is used to set analog input terminals. When the PAD register bits are set to "1", the corresponding terminals function as the analog input terminals.

At initial reset, these terminals are all set in the I/O port terminals, and each terminal goes to a high impedance.

Table 4.9.4.1 Correspondence between A/D input terminal and PAD register

Terminal	A/D input enable /disable	Comment
P40 (AD0)	PAD0	
P41 (AD1)	PAD1	
P42 (AD2)	PAD2	
P43 (AD3)	PAD3	

(2) Setting of input clock

The clock selector selects the A/D conversion clock from OSC1 or OSC3 according to the value written in the ADCLK register. Table 4.9.4.2 shows the input clock selection with the ADCLK register.

Table 4.9.4.2 Input clock selection

ADCLK	Clock source
0	OSC1
1	OSC3/2

The clock selector outputs the selected clock to the A/D converter by writing "1" to the ADRUN register.

Note:
- *When the supply voltage is in the range of 2.2 to 3.6 V, the input clock can be selected from OSC1 or OSC3. When the supply voltage is in the range of 0.9 to 2.2 V, OSC1 can only be selected.*
- *The A/D clock freguency must be 1 MHz or less.*
- *Be sure to select (change) the input clock while the A/D converter is stopped. Changing the clock during A/D operation may cause malfunction.*
- *To prevent malfunction, do not start A/D conversion (writing "1" to the ADRUN register) when the A/D conversion clock is not being output from the clock selector, and do not turn the clock off during A/D conversion.*

(3) Input signal selection

The analog signals from the AD0 (P40)–AD3 (P43) terminals are input to the multiplexer, and the analog input channel for A/D conversion is selected by software. This selection can be done using the CHS register as shown in Table 4.9.4.3.

Table 4.9.4.3 Selection of analog input channel

CHS1	CHS0	Input channel
1	1	AD3 (P43)
1	0	AD2 (P42)
0	1	AD1 (P41)
0	0	AD0 (P40)

(4) A/D conversion operation

An A/D conversion starts by writing "1" to the ADRUN register (FFD0H•D3). However, when the supply voltage is 1.6 V or less, the V_{C2} mode must be set by writing "1" to the VADSEL register before starting A/D conversion.
For example, when performing A/D conversion using AD1 as the analog input, write "1" (0, 1) to the CHS register (CHS1, CHS0). However, it is necessary that the P41 terminal has been set as an analog input terminal. Then write "1" to the ADRUN register. The A/D converter start converting of the analog signal input to the AD1 terminal.

The built-in sample/hold circuit starts sampling of the analog input specified from t_{AD} after writing. When the sampling is completed, the held analog input voltage is converted into a 8-bit digital value in successive-approximation architecture.
The conversion result is loaded into the ADDR (ADDR0–ADDR7) register. ADDR0 is the LSB and ADDR7 is the MSB.

Note: *If the CHS register selects an input channel which is not included in the analog input terminals set by the PAD register (the PAD register can select several terminals simultaneously), the A/D conversion does not result in a correct converted value.*

Example)
Terminal setting: PAD3=1, PAD2–PAD0=0 (AD3 terminal is used)
Selection of input channel: CHS1=0, CHS0=0 (AD0 is selected)
In a setting like this, the A/D conversion result will be invalid because the contents of the settings are not matched.

Figure 4.9.4.1 shows the flow chart for starting an A/D conversion.

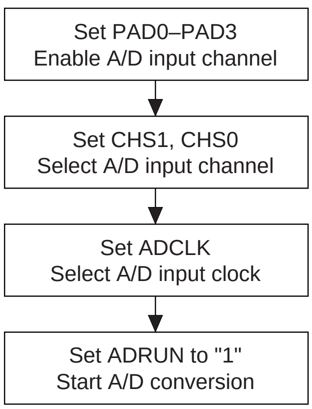


Fig. 4.9.4.1 Flowchart for starting A/D conversion

An A/D conversion is completed when the conversion result is loaded into the ADDR register. At that point, the A/D converter generates an interrupt (explained in the next section).
Figure 4.9.4.2 shows the timing chart of A/D conversion.

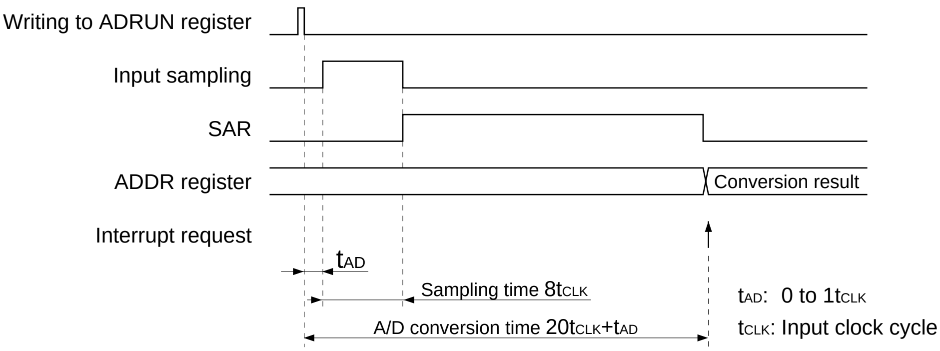


Fig. 4.9.4.2 Timing chart of A/D conversion

4.9.5 Interrupt function

The A/D converter can generate an interrupt when an A/D conversion has completed.
Figure 4.9.5.1 shows the configuration of the A/D converter interrupt circuit.

The A/D converter sets the interrupt factor flag IAD to "1" immediately after storing the conversion result to the ADDR register.
At this time, if the interrupt mask register EIAD is "1" , an interrupt is generated to the CPU.
By setting the EIAD register to "0", the interrupt to the CPU can be disabled. However, the interrupt factor flag is set to "1" when an A/D conversion has completed regardless of the interrupt mask register setting.
The interrupt factor flag set in "1" is reset to "0" by writing "1".

The interrupt vector for the A/D conversion completion has been set in 010EH.

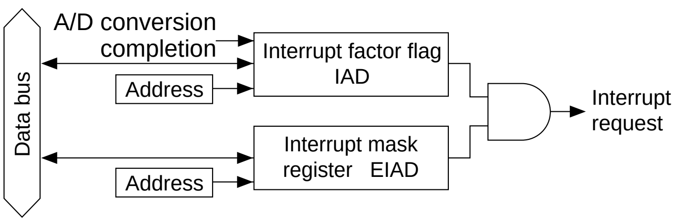


Fig. 4.9.5.1 Configuration of A/D converter interrupt circuit

4.9.6 I/O memory of A/D converter

Table 4.9.6.1 shows the I/O addresses and the control bits for the A/D converter.

Table 4.9.6.1 Control bits of A/D converter

Address	Register D3	Register D2	Register D1	Register D0	Name	Init *1	1	0	Comment
FF01H	VADSEL	VDSEL	0	0	VADSEL	0	V_{C2}	V_{DD}	Power source selection for A/D converter
					VDSEL	0	V_{C2}	V_{DD}	Power supply selection for oscillation system voltage regulator
	R/W		R		0 *3	– *2			Unused
					0 *3	– *2			Unused
FFD0H	ADRUN	ADCLK	CHS1	CHS0	ADRUN	0	Start	Invalid	A/D Run/Off control
					ADCLK	0	OSC3	OSC1	A/D input clock selection
	W	R/W			CHS1	0			A/D input channel selection: [CHS1, 0] 0 / 1 / 2 / 3; Input channel P40 / P41 / P42 / P43
					CHS0	0			
FFD1H	PAD3	PAD2	PAD1	PAD0	PAD3	0	Enable	Disable	P43 input channel enable/disable control
					PAD2	0	Enable	Disable	P42 input channel enable/disable control
	R/W				PAD1	0	Enable	Disable	P41 input channel enable/disable control
					PAD0	0	Enable	Disable	P40 input channel enable/disable control
FFD2H	ADDR3	ADDR2	ADDR1	ADDR0	ADDR3	– *2			A/D converted data (D0–D3)
					ADDR2	– *2			
	R				ADDR1	– *2			
					ADDR0	– *2			
FFD3H	ADDR7	ADDR6	ADDR5	ADDR4	ADDR7	– *2			A/D converted data (D4–D7)
					ADDR6	– *2			
	R				ADDR5	– *2			
					ADDR4	– *2			
FFE7H	0	0	0	EIAD	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R			R/W	0 *3	– *2			Unused
					EIAD	0	Enable	Mask	Interrupt mask register (A/D converter)
FFF7H	0	0	0	IAD	0 *3	– *2	(R)	(R)	Unused
					0 *3	– *2	Yes	No	Unused
	R			R/W	0 *3	– *2	(W)	(W)	Unused
					IAD	0	Reset	Invalid	Interrupt factor flag (A/D converter)

*1 Initial value at initial reset
*2 Not set in the circuit
*3 Constantly "0" when being read

PAD0–PAD3: A/D converter input control register (FFD1H)

Sets the P40–P43 terminals as the analog input terminals for the A/D converter.

When "1" is written: A/D converter input
When "0" is written: I/O port
Reading: Valid

When "1" is written to PADn, the P4n terminal is set to the analog input terminal ADn. (n=0–3)
When "0" is written, the terminal is used with the I/O port.
At initial reset, this register is set to "0" (I/O port).

ADCLK: A/D converter clock source selection register (FFD0H•D2)

Selects the clock source for the A/D converter.

When "1" is written: OSC3
When "0" is written: OSC1
Reading: Valid

When "1" is written to ADCLK, OSC3 is selected as the clock source for the A/D converter. However, the supply voltage must be 2.2 V or more.
When "0" is written, OSC1 is selected.
At initial reset, this register is set to "0" (OSC1).

CHS0, CHS1: Analog input channel selection register (FFD0H•D0, D1)

Selects an analog input channel.

Table 4.9.6.3 Selection of analog input channel

CHS1	CHS0	Input channel
1	1	AD3 (P43)
1	0	AD2 (P42)
0	1	AD1 (P41)
0	0	AD0 (P40)

At initial reset, this register is set to "0" (AD0).

VADSEL: A/D power source selection register (FF01H•D3)

Selects the power supply for the A/D converter.

When "1" is written: V_{C2}
When "0" is written: V_{DD}
Reading: Valid

When "1" is written to the VADSEL register, the A/D converter operates with the V_{C2} voltage output from the LCD voltage booster. Use V_{C2} when the supply voltage is 1.6 V or less. To generate V_{C2}, write "1" to the LPWR register (FF60H•D0) and wait at least 100 msec to stabilize the V_{C2} voltage.
When "0" is written, the A/D converter operates with V_{DD}. In this case, V_{DD} must be 1.6 V or more.
At initial reset, this register is set to "0" (V_{DD}).

ADRUN: A/D conversion control (FFD0H•D3)

Starts an A/D conversion.

When "1" is written: Start
When "0" is written: No operation
Reading: Invalid

When "1" is written to ADRUN, the A/D converter starts A/D conversion of the channel selected by the CHS register and stores the conversion result to the ADDR register.
At initial reset, this bit is set to "0".

ADDR0–ADDR7: A/D conversion result (FFD2H/lower 4 bits, FFD3H/upper 4 bits)

A/D conversion result is stored.
ADDR0 is the LSB and ADDR7 is the MSB.
At initial reset, data is undefined.

EIAD: A/D converter interrupt mask register (FFE7H•D0)

This register is used to select whether to mask the A/D converter interrupt or not.

When "1" is written: Enabled
When "0" is written: Masked
Reading: Valid

Writing "1" to the EIAD register enables the A/D converter interrupt and writing "0" disables the interrupt.
At initial reset, this register is set to "0".

IAD: A/D converter interrupt factor flag (FFF7H•D0)

This flag indicates the status of the A/D converter interrupt.

When "1" is read: Interrupt has occurred
When "0" is read: Interrupt has not occurred

When "1" is written: Flag is reset
When "0" is written: Invalid

IAD is the A/D converter interrupt factor flag that is set when an A/D conversion has finished. The software can judge from this flag whether there is an A/D converter interrupt or not. This flag is set to "1" even if the interrupt is masked.
This flag is reset to "0" by writing "1".
After an interrupt occurs, the same interrupt will occur again if the interrupt enabled state (I flag = "1") is set or the RETI instruction is executed unless the interrupt factor flag is reset. Therefore, be sure to reset (write "1" to) the interrupt factor flag in the interrupt service routine before shifting to the interrupt enabled state.
At initial reset, this flag is set to "0".

4.9.7 Programming notes

(1) When supply voltage is 1.6 V or less, it is necessary to set the A/D converter circuit into the V_{C2} mode by writting "1" to VADSEL register befor starting A/D conversion.

(2) The A/D converter can operate by inputting the clock from the clock selector. Therefore, it is necessary to select the clock source and to turn the clock output on before starting A/D conversion. Furthermore, it is also necessary that the OSC3 oscillation circuit is operating when using the OSC3 clock.

(3) When using the OSC3 clock as the A/D conversion clock, do not stop the OSC3 oscillation circuit during A/D conversion. If the OSC3 oscillation circuit stops, correct A/D conversion result cannot be obtained.

(4) The input clock and analog input terminals should be set when the A/D converter stops. Changing these settings in the A/D converter operation may cause errors.

(5) To prevent malfunction, do not start A/D conversion (writing "1" to the ADRUN register) when the A/D conversion clock is not being output from the clock selector, and do not turn the clock off during A/D conversion.

(6) If the CHS register selects an input channel which is not included in the analog input terminals set by the PAD register (the PAD register can select several terminals simultaneously), the A/D conversion does not result in a correct converted value.

(7) During A/D conversion, do not operate the P4n terminals which are not used for analog inputs of the A/D converter (for input/output of digital signals). It affects the A/D conversion precision.

4.10 Programmable Timer

4.10.1 Configuration of programmable timer

The E0C63158 has two 8-bit programmable timer systems (timer 0 and timer 1) built-in.
Timer 0 and timer 1 are composed of 8-bit presettable down counters and they can be used as 8-bit × 2 channel programmable timers or a 16-bit × 1 channel programmable timer by software setting. Timer 0 also has an event counter function using the K13 input port terminal.
Figure 4.10.1.1 shows the configuration of the programmable timer.

The programmable timer is designed to count down from the initial value set in the counter with software. An underflow according to the initial value occurs by counting down and is used for the following functions:

- Presetting the initial value to the counter to generate the periodical underflow signal
- Generating an interrupt
- Generating a TOUT signal output from the R02 output port terminal
- Generating the synchronous clock source for the serial interface (timer 1 underflow is used, and it is possible to set the transfer rate)

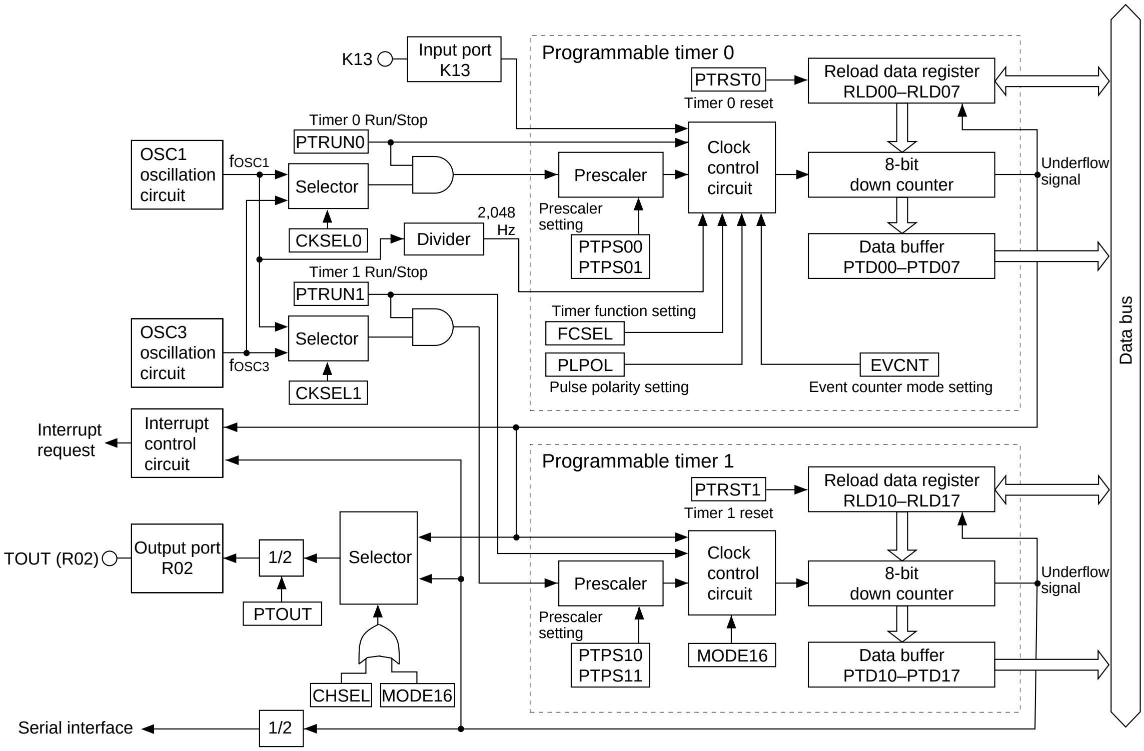


Fig. 4.10.1.1 Configuration of programmable timer

4.10.2 Tow separate 8-bit timer (MODE16 = "0") operation

4.10.2.1 Setting of initial value and counting down

Timers 0 and 1 each have a down counter and reload data register.

The reload data registers RLD00–RLD07 (timer 0) and RLD10–RLD17 (timer 1) are used to set the initial value to the down counter.
By writing "1" to the timer reset bit PTRST0 (timer 0) or PTRST1 (timer 1), the down counter loads the initial value set in the reload register RLD. Therefore, down-counting is executed from the stored initial value by the input clock.

The registers PTRUN0 (timer 0) and PTRUN1 (timer 1) are provided to control the RUN/STOP for timers 0 and 1. By writing "1" to the register after presetting the reload data to the down counter, the down counter starts counting down. Writing "0" stops the input count clock and the down counter stops counting. This control (RUN/STOP) does not affect the counter data. The counter maintains its data while stopped, and can restart counting continuing from that data.

The counter data can be read via the data buffers PTD00–PTD07 (timer 0) and PTD10–PTD17 (timer 1) in optional timing. However, the counter has the data hold function the same as the clock timer, that holds the high-order data when the low-order data is read in order to prevent the borrowing operation between low- and high-order reading, therefore be sure to read the low-order data first.

The counter reloads the initial value set in the reload data register RLD when an underflow occurs through the count down. It continues counting down from the initial value after reloading.
In addition to reloading the counter, this underflow signal controls the interrupt generation, pulse (TOUT signal) output and clock supplying to the serial interface.

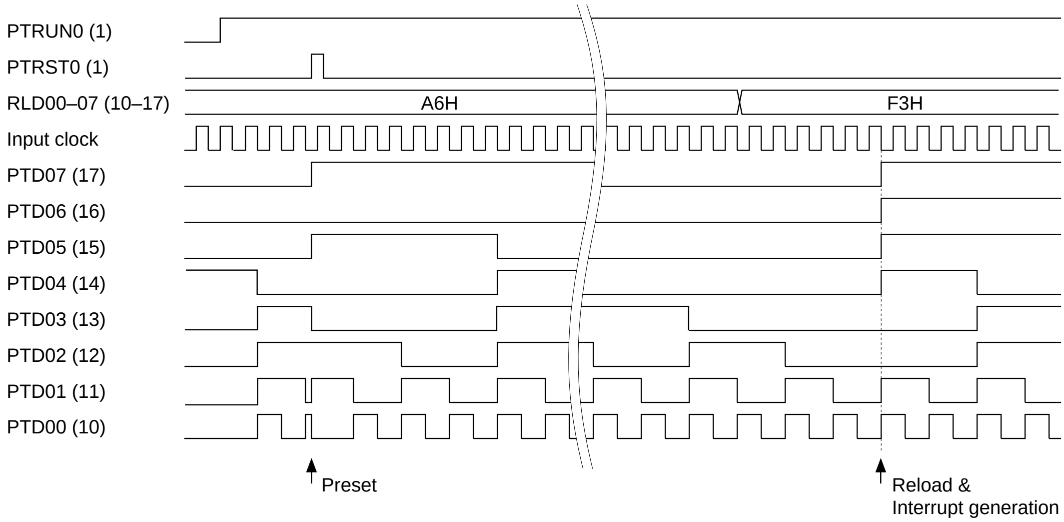


Fig. 4.10.2.1.1 Basic operation timing of down counter

4.10.2.2 Counter mode

The programmable timer can operate in two counter modes, timer mode and event counter mode. It can be selected by software.

(1) Timer mode

The timer mode counts down using the prescaler output as an input clock. In this mode, the programmable timer operates as a periodical timer using the OSC1 or OSC3 oscillation clock as a clock source.
Timer 0 can operate in both the timer mode and the event counter mode. The mode can be switched using the timer 0 counter mode selection register EVCNT. When the EVCNT register is set to "0", timer 0 operates in the timer mode.
Timer 1 operates only in the timer mode.
At initial reset, this mode is set.

Refer to Section 4.10.2.1, "Setting of initial value and counting down" for basic operation and control.

The input clock in the timer mode is generated by the prescaler built into the programmable timer. The prescaler generates the input clock by dividing the OSC1 or OSC3 oscillation clock. Refer to the next section for setting the input clock.

(2) Event counter mode

The timer 0 has an event counter function that counts an external clock input to the input port K13. This function is selected by writing "1" to the timer 0 counter mode selection register EVCNT. The timer 1 operates only in the timer mode, and cannot be used as an event counter.

In the event counter mode, the clock is supplied to timer 0 from outside of the IC, therefore, the settings of the timer 0 prescaler division ratio selection registers PTPS00 and PTPS01 and the settings of the timer 0 source clock selection register CKSEL0 become invalid.

Count down timing can be selected from either the falling or rising edge of the input clock using the timer 0 pulse polarity selection register PLPOL. When "0" is written to the PLPOL register, the falling edge is selected, and when "1" is written, the rising edge is selected. The count down timing is shown in Figure 4.10.2.2.1.

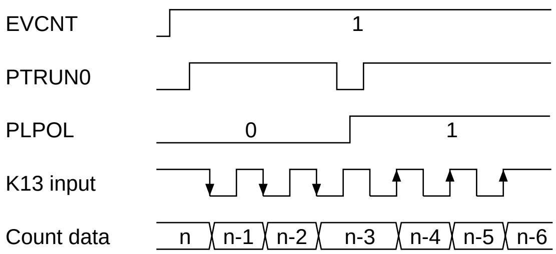


Fig. 4.10.2.2.1 Timing chart in event counter mode

The event counter mode also includes a noise reject function to eliminate noise such as chattering on the external clock (K13 input signal). This function is selected by writing "1" to the timer 0 function selection register FCSEL.
When "with noise rejector" is selected, an input pulse width for both low and high levels must be 0.98 msec or more to count reliably. (The noise rejecter allows the counter to input the clock at the second falling edge of the internal 2,048 Hz signal after changing the input level of the K13 input port terminal. Consequently, the pulse width of noise that can reliably be rejected is 0.48 msec or less.)
Figure 4.10.2.2.2 shows the count down timing with noise rejecter.

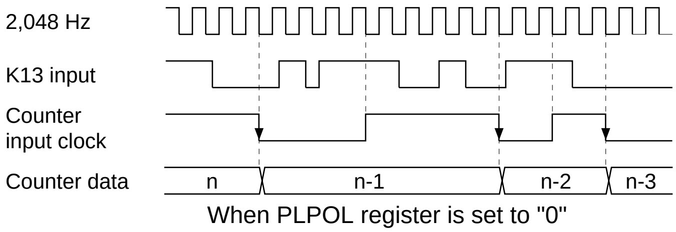


Fig. 4.10.2.2.2 Count down timing with noise rejecter

The operation of the event counter mode is the same as the timer mode except it uses the K13 input as the clock.
Refer to Section 4.10.2.1, "Setting of initial value and counting down" for basic operation and control.

4.10.2.3 Setting of input clock in timer mode

Timer 0 and timer 1 each include a prescaler. The prescalers generate the input clock for each timer by dividing the source clock supplied from the OSC1 or OSC3 oscillation circuit.
The source clock (OSC1 or OSC3) and the division ratio of the prescaler can be selected with software for timer 0 and timer 1 individually.
The set input clock is used for the count clock during operation in the timer mode. When the timer 0 is used in the event counter mode, the following settings become invalid.

The input clock is set in the following sequence.

(1) Selection of source clock

Select the source clock input to each prescaler from either OSC1 or OSC3. This selection is done using the source clock selection registers CKSEL0 (timer 0) and CKSEL1 (timer 1); when "0" is written to the register, OSC1 is selected and when "1" is written, OSC3 is selected.
When the OSC3 oscillation clock is selected for the clock source, it is necessary to turn the OSC3 oscillation ON, prior to using the programmable timer. However the OSC3 oscillation circuit requires a time interval of several msec to several 10 msec from turning the circuit ON until the oscillation stabilizes. Therefore, allow an adequate interval from turning the OSC3 oscillation circuit ON to starting the programmable timer. Refer to Section 4.4, "Oscillation Circuit", for the control and notes of the OSC3 oscillation circuit.
At initial reset, the OSC3 oscillation circuit is set in the OFF state.

(2) Selection of prescaler division ratio

Select the division ratio for each prescaler from among 4 types. This selection is done using the prescaler division ratio selection registers PTPS00/PTPSC01 (timer 0) and PTPS10/PTPS11 (timer 1). Table 4.10.2.3.1 shows the correspondence between the setting value and the division ratio.

Table 4.10.2.3.1 Selection of prescaler division ratio

PTPS11 PTPS01	PTPS10 PTPS00	Prescaler division ratio
1	1	Source clock / 256
1	0	Source clock / 32
0	1	Source clock / 4
0	0	Source clock / 1

By writing "1" to the register PTRUN0 (timer 0) or PTRUN1 (timer 1), the prescaler inputs the source clock and outputs the clock divided by the selected division ratio. The counter starts counting down by inputting the clock.

4.10.2.4 Interrupt function

The programmable timer can generate an interrupt due to an underflow of the timer 0 and timer 1. See Figure 4.10.2.1.1 for the interrupt timing.

An underflow of timer 0 and timer 1 sets the corresponding interrupt factor flag IPT0 (timer 0) or IPT1 (timer 1) to "1", and generates an interrupt. The interrupt can also be masked by setting the corresponding interrupt mask register EIPT0 (timer 0) or EIPT1 (timer 1). However, the interrupt factor flag is set to "1" by an underflow of the corresponding timer regardless of the interrupt mask register setting.

4.10.2.5 Setting of TOUT output

The programmable timer can generate a TOUT signal due to an underflow of timer 0 or timer 1. The TOUT signal is generated by dividing the underflows in 1/2. It is possible to select which timer's underflow is to be used by the TOUT output channel selection register CHSEL. When "0" is written to the CHSEL register, timer 0 is selected and when "1" is written, timer 1 is selected.
Figure 4.10.2.5.1 shows the TOUT signal waveform when the channel is changed.

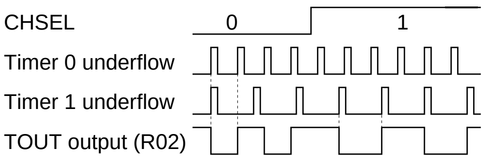


Fig. 4.10.2.5.1 TOUT signal waveform at channel change

The TOUT signal can be output from the R02 output port terminal. Programmable clocks can be supplied to external devices.
Figure 4.10.2.5.2 shows the configuration of the output port R02.

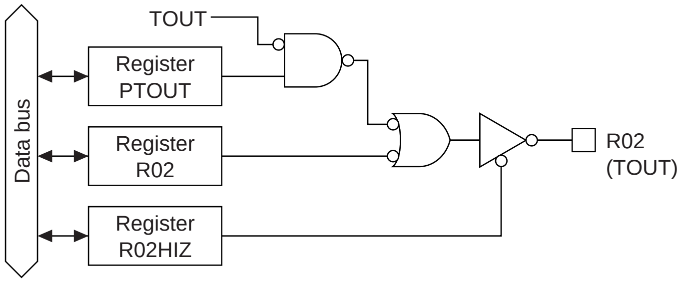


Fig. 4.10.2.5.2 Configuration of R02

The output of a TOUT signal is controlled by the PTOUT register. When "1" is written to the PTOUT register, the TOUT signal is output from the R02 output port terminal and when "0" is written, the terminal goes to a high (VDD) level. However, the data register R02 must always be "1" and the high impedance control register R02HIZ must always be "0" (data output state).

Since the TOUT signal is generated asynchronously from the PTOUT register, a hazard within 1/2 cycle is generated when the signal is turned ON and OFF by setting the register.
Figure 4.10.2.5.3 shows the output waveform of the TOUT signal.

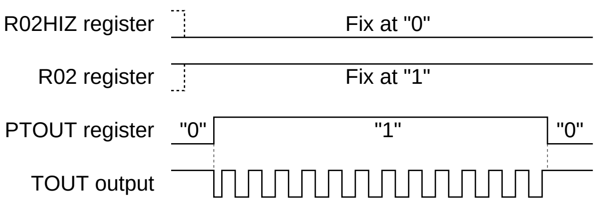


Fig. 4.10.2.5.3 Output waveform of the TOUT signal

4.10.2.6 Transfer rate setting for serial interface

The signal that is made from underflows of timer 1 by dividing them in 1/2, can be used as the clock source for the serial interface.
The programmable timer outputs the clock to the serial interface by setting timer 1 into RUN state (PTRUN1 = "1"). It is not necessary to control with the PTOUT register.

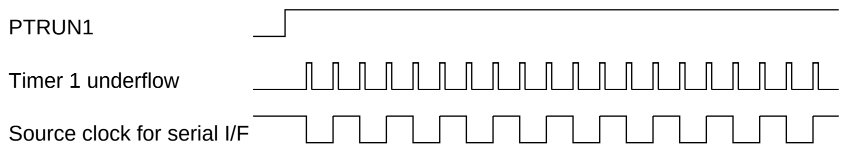


Fig. 4.10.2.6.1 Synchronous clock of serial interface

A setting value for the RLD1X register according to a transfer rate is calculated by the following expression:

RLD1X = fosc / (2 ∗ bps ∗ division ratio of the prescaler) - 1
fosc: Oscillation frequency (OSC1/OSC3)
bps: Transfer rate
(00H can be set to RLD1X)

4.10.3 One channel × 16-bit timer (MODE16 = "1") operation

Timer 0 and timer 1 are chained together to form 16-bit down counter low byte in timer 0, high byte in timer 1.

4.10.3.1 Setting of initial value and counting down

Timers 0 and 1 each have a down counter and reload data register.

The reload data registers RLD00–RLD07 (timer 0) and RLD10–RLD17 (timer 1) are used to set the initial value to the down counter.
By writing "1" to the timer reset bit PTRST0 (timer 0) or PTRST1 (timer 1), the down counter loads the initial value set in the reload register RLD. Therefore, down-counting is executed from the stored initial value by the input clock.

The register PTRUN0 (timer 0) is used to control the RUN/STOP for timers 0 and 1. By writing "1" to the register after presetting the reload data to the down counter, the down counter starts counting down. Writing "0" stops the input count clock and the down counter stops counting. This control (RUN/STOP) does not affect the counter data. The counter maintains its data while stopped, and can restart counting continuing from that data.

The counter data can be read via the data buffers PTD00–PTD07 (timer 0) and PTD10–PTD17 (timer 1) in optional timing. However, the counter has the data hold function the same as the clock timer, that holds the high-order data when the low-order data is read in order to prevent the borrowing operation between low- and high-order reading, therefore be sure to read the low-order data first.

The counter reloads the initial value set in the reload data register RLD when an underflow occurs through the count down. It continues counting down from the initial value after reloading.
In addition to reloading the counter, this underflow signal controls the interrupt generation, pulse (TOUT signal) output and clock supplying to the serial interface.

4.10.3.2 Counter mode

The programmable timer can operate in two counter modes, timer mode and event counter mode. It can be selected by software.

(1) Timer mode

The timer mode counts down using the prescaler output as an input clock. In this mode, the programmable timer operates as a periodical timer using the OSC1 or OSC3 oscillation clock as a clock source. The programmable timer can operate in both the timer mode and the event counter mode. The mode can be switched using the timer 0 counter mode selection register EVCNT. When the EVCNT register is set to "0", the programmable timer operates in the timer mode.
At initial reset, this mode is set.

Refer to Section 4.10.3.1, "Setting of initial value and counting down" for basic operation and control.

The input clock in the timer mode is generated by the prescaler built into the programmable timer. The prescaler generates the input clock by dividing the OSC1 or OSC3 oscillation clock. Refer to the next section for setting the input clock.

(2) Event counter mode

The programmable timer has an event counter function that counts an external clock input to the input port K13. This function is selected by writing "1" to the timer 0 counter mode selection register EVCNT.

In the event counter mode, the clock is supplied to timer 0 from outside of the IC, therefore, the settings of the timer 0 prescaler division ratio selection registers PTPS00 and PTPS01 and the settings of the timer 0 source clock selection register CKSEL0 become invalid.

Count down timing can be selected from either the falling or rising edge of the input clock using the timer 0 pulse polarity selection register PLPOL. When "0" is written to the PLPOL register, the falling edge is selected, and when "1" is written, the rising edge is selected. The count down timing is shown in Figure 4.10.3.2.1.

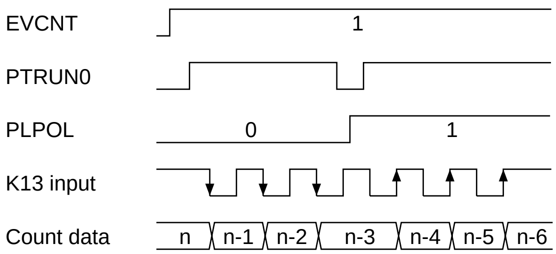


Fig. 4.10.3.2.1 Timing chart in event counter mode

The event counter mode also includes a noise reject function to eliminate noise such as chattering on the external clock (K13 input signal). This function is selected by writing "1" to the timer 0 function selection register FCSEL.
When "with noise rejector" is selected, an input pulse width for both low and high levels must be 0.98 msec or more to count reliably. (The noise rejecter allows the counter to input the clock at the second falling edge of the internal 2,048 Hz signal after changing the input level of the K13 input port terminal. Consequently, the pulse width of noise that can reliably be rejected is 0.48 msec or less.)
Figure 4.10.3.2.2 shows the count down timing with noise rejecter.

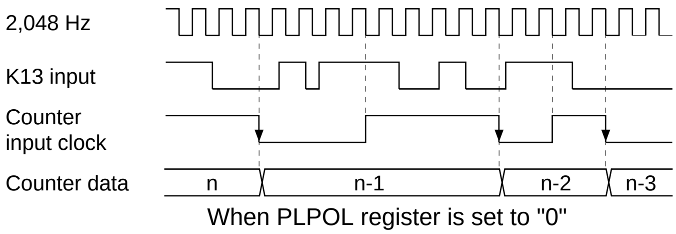


Fig. 4.10.3.2.2 Count down timing with noise rejecter

The operation of the event counter mode is the same as the timer mode except it uses the K13 input as the clock.
Refer to Section 4.10.3.1, "Setting of initial value and counting down" for basic operation and control.

4.10.3.3 Setting of input clock in timer mode

The 16 bit programmable timer include a prescaler. The prescalers generate the input clock for this programmable timer by dividing the source clock supplied from the OSC1 or OSC3 oscillation circuit. The source clock (OSC1 or OSC3) and the division ratio of the prescaler can be selected with software. The set input clock is used for the count clock during operation in the timer mode. When the 16 bit programmable timer is used in the event counter mode, the following settings become invalid.

The input clock is set in the following sequence.

(1) Selection of source clock

Select the source clock input to the prescaler from either OSC1 or OSC3. This selection is done using the source clock selection register CKSEL0 (timer 0); when "0" is written to the register, OSC1 is selected and when "1" is written, OSC3 is selected.
When the OSC3 oscillation clock is selected for the clock source, it is necessary to turn the OSC3 oscillation ON, prior to using the programmable timer. However the OSC3 oscillation circuit requires a time interval of several msec to several 10 msec from turning the circuit ON until the oscillation stabilizes. Therefore, allow an adequate interval from turning the OSC3 oscillation circuit ON to starting the programmable timer. Refer to Section 4.4, "Oscillation Circuit", for the control and notes of the OSC3 oscillation circuit.
At initial reset, the OSC3 oscillation circuit is set in the OFF state.

(2) Selection of prescaler division ratio

Select the division ratio for the prescaler from among 4 types. This selection is done using the prescaler division ratio selection registers PTPS00/PTPSC01 (timer 0). Table 4.10.3.3.1 shows the correspondence between the setting value and the division ratio.

Table 4.10.3.3.1 Selection of prescaler division ratio

PTPS01	PTPS00	Prescaler division ratio
1	1	Source clock / 256
1	0	Source clock / 32
0	1	Source clock / 4
0	0	Source clock / 1

By writing "1" to the register PTRUN0 (timer 0), the prescaler inputs the source clock and outputs the clock divided by the selected division ratio. The counter starts counting down by inputting the clock.

4.10.3.4 Interrupt function

The programmable timer can generate an interrupt due to an underflow.

An underflow of this 16 bit programmable timer sets the corresponding interrupt factor flag IPT1 (timer 1) to "1", and generates an interrupt. The interrupt can also be masked by setting the corresponding interrupt mask register EIPT1 (timer 1). However, the interrupt factor flag is set to "1" by an underflow of the corresponding timer regardless of the interrupt mask register setting.

4.10.3.5 Setting of TOUT output

The programmable timer can generate a TOUT signal due to an underflow of this 16 bit programmable timer. The TOUT signal is generated by dividing the underflows in 1/2.

The TOUT signal can be output from the R02 output port terminal. Programmable clocks can be supplied to external devices.
Figure 4.10.3.5.1 shows the configuration of the output port R02.

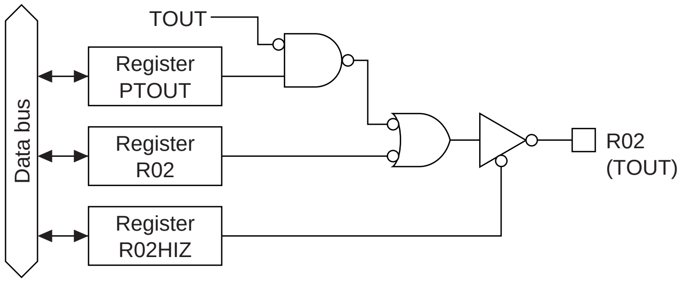


Fig. 4.10.3.5.1 Configuration of R02

The output of a TOUT signal is controlled by the PTOUT register. When "1" is written to the PTOUT register, the TOUT signal is output from the R02 output port terminal and when "0" is written, the terminal goes to a high (VDD) level. However, the data register R02 must always be "1" and the high impedance control register R02HIZ must always be "0" (data output state).

Since the TOUT signal is generated asynchronously from the PTOUT register, a hazard within 1/2 cycle is generated when the signal is turned ON and OFF by setting the register.
Figure 4.10.3.5.2 shows the output waveform of the TOUT signal.

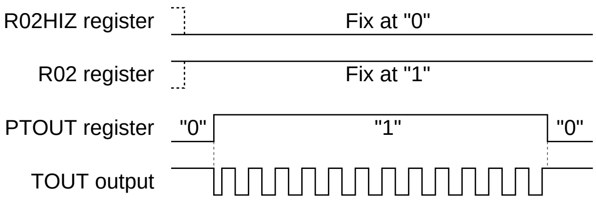


Fig. 4.10.3.5.2 Output waveform of the TOUT signal

4.10.3.6 Transfer rate setting for serial interface

The signal that is made from underflows of the 16 bit programmable timer by dividing them in 1/2, can be used as the clock source for the serial interface.
The programmable timer outputs the clock to the serial interface by setting this 16 bit programmable timer into RUN state (PTRUN0 = "1"). It is not necessary to control with the PTOUT register.

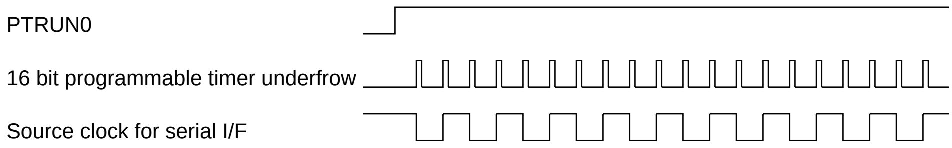


Fig. 4.10.3.6.1 Synchronous clock of serial interface

A setting value for the RLD1X register according to a transfer rate is calculated by the following expression:

RLD1X, RLD0X = fosc / (2 ∗ bps ∗ division ratio of the prescaler) - 1

fosc: Oscillation frequency (OSC1/OSC3)
bps: Transfer rate
(00H can be set to RLD1X)

4.10.4 I/O memory of programmable timer

Table 4.10.4.1 shows the I/O addresses and the control bits for the programmable timer.

Table 4.10.4.1 Control bits of programmable timer

Address	Register D3	Register D2	Register D1	Register D0	Name	Init *1	1	0	Comment
FFC0H	MODE16	EVCNT	FCSEL	PLPOL	MODE16	0	16 bit × 1	8 bit × 2	8 bit × 2 or 16 bit × 1 timer mode selection
					EVCNT	0	Event ct.	Timer	Timer 0 counter mode selection
	R/W				FCSEL	0	With NR	No NR	Timer 0 function selection (for event counter mode)
					PLPOL	0	↑	↓	Timer 0 pulse polarity selection (for event counter mode)
FFC1H	CHSEL	PTOUT	CKSEL1	CKSEL0	CHSEL	0	Timer1	Timer0	TOUT output channel selection
					PTOUT	0	On	Off	TOUT output control
	R/W				CKSEL1	0	OSC3	OSC1	Prescaler 1 source clock selection
					CKSEL0	0	OSC3	OSC1	Prescaler 0 source clock selection
FFC2H	PTPS01	PTPS00	PTRST0	PTRUN0	PTPS01	0			Prescaler 0 division ratio selection: [PTPS01, 00] 0 1 2 3
					PTPS00	0			Division ratio 1/1 1/4 1/32 1/256
	R/W		W	R/W	PTRST0*3	– *2	Reset	Invalid	Timer 0 reset (reload)
					PTRUN0	0	Run	Stop	Timer 0 Run/Stop
FFC3H	PTPS11	PTPS10	PTRST1	PTRUN1	PTPS11	0			Prescaler 1 division ratio selection: [PTPS11, 10] 0 1 2 3
					PTPS10	0			Division ratio 1/1 1/4 1/32 1/256
	R/W		W	R/W	PTRST1*3	– *2	Reset	Invalid	Timer 1 reset (reload)
					PTRUN1	0	Run	Stop	Timer 1 Run/Stop
FFC4H	RLD03	RLD02	RLD01	RLD00	RLD03	0			MSB
					RLD02	0			Programmable timer 0 reload data (low-order 4 bits)
	R/W				RLD01	0			
					RLD00	0			LSB
FFC5H	RLD07	RLD06	RLD05	RLD04	RLD07	0			MSB
					RLD06	0			Programmable timer 0 reload data (high-order 4 bits)
	R/W				RLD05	0			
					RLD04	0			LSB
FFC6H	RLD13	RLD12	RLD11	RLD10	RLD13	0			MSB
					RLD12	0			Programmable timer 1 reload data (low-order 4 bits)
	R/W				RLD11	0			
					RLD10	0			LSB
FFC7H	RLD17	RLD16	RLD15	RLD14	RLD17	0			MSB
					RLD16	0			Programmable timer 1 reload data (high-order 4 bits)
	R/W				RLD15	0			
					RLD14	0			LSB
FFC8H	PTD03	PTD02	PTD01	PTD00	PTD03	0			MSB
					PTD02	0			Programmable timer 0 data (low-order 4 bits)
	R				PTD01	0			
					PTD00	0			LSB
FFC9H	PTD07	PTD06	PTD05	PTD04	PTD07	0			MSB
					PTD06	0			Programmable timer 0 data (high-order 4 bits)
	R				PTD05	0			
					PTD04	0			LSB
FFCAH	PTD13	PTD12	PTD11	PTD10	PTD13	0			MSB
					PTD12	0			Programmable timer 1 data (low-order 4 bits)
	R				PTD11	0			
					PTD10	0			LSB
FFCBH	PTD17	PTD16	PTD15	PTD14	PTD17	0			MSB
					PTD16	0			Programmable timer 1 data (high-order 4 bits)
	R				PTD15	0			
					PTD14	0			LSB
FFE2H	0	0	EIPT1	EIPT0	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R		R/W		EIPT1	0	Enable	Mask	Interrupt mask register (Programmable timer 1)
					EIPT0	0	Enable	Mask	Interrupt mask register (Programmable timer 0)
FFF2H	0	0	IPT1	IPT0	0 *3	– *2	(R)	(R)	Unused
					0 *3	– *2	Yes	No	Unused
	R		R/W		IPT1	0	(W)	(W)	Interrupt factor flag (Programmable timer 1)
					IPT0	0	Reset	Invalid	Interrupt factor flag (Programmable timer 0)

*1 Initial value at initial reset *2 Not set in the circuit *3 Constantly "0" when being read

CKSEL0: Prescaler 0 source clock selection register (FFC1H•D0)
CKSEL1: Prescaler 1 source clock selection register (FFC1H•D1)

Selects the source clock of the prescaler.

When "1" is written: OSC3 clock
When "0" is written: OSC1 clock
Reading: Valid

The source clock for the prescaler is selected from OSC1 or OSC3. When "0" is written to the CKSEL0 register, the OSC1 clock is selected as the input clock for the prescaler 0 (for timer 0) and when "1" is written, the OSC3 clock is selected.
Same as above, the source clock for prescaler 1 is selected by the CKSEL1 register.
When the event counter mode is selected to timer 0, the setting of the CKSEL0 register becomes invalid.
At initial reset, these registers are set to "0".

PTPS00, PTPS01: Timer 0 prescaler division ratio selection register (FFC2H•D2, D3)
PTPS10, PTPS11: Timer 1 prescaler division ratio selection register (FFC3H•D2, D3)

Selects the division ratio of the prescaler.
Two bits of PSC00 and PSC01 are the prescaler division ratio selection register for timer 0, and two bits of PSC10 and PSC11 are for timer 1. The prescaler division ratios that can be set by these registers are shown in Table 4.10.4.2.

Table 4.10.4.2 Selection of prescaler division ratio

PTPS11 PTPS01	PTPS10 PTPS00	Prescaler division ratio
1	1	Source clock / 256
1	0	Source clock / 32
0	1	Source clock / 4
0	0	Source clock / 1

When the event counter mode is selected to timer 0, the setting of the PTPS00 and PTPS01 becomes invalid.
At initial reset, these registers are set to "0".

EVCNT: Timer 0 counter mode selection register (FFC0H•D2)

Selects a counter mode for timer 0.

When "1" is written: Event counter mode
When "0" is written: Timer mode
Reading: Valid

The counter mode for timer 0 is selected from either the event counter mode or timer mode. When "1" is written to the EVCNT register, the event counter mode is selected and when "0" is written, the timer mode is selected.
At initial reset, this register is set to "0".

MODE16: 8-bit × 2 or 16-bit × 1 timer mode selection register (FFC0H•D3)

Selects 8-bit × 2 channels mode (timer 0 and timer 1) or 16-bit × 1 channel mode.

When "1" is written: 16-bit × 1 channel
When "0" is written: 8-bit × 2 channels (timer 0 and timer 1)
Reading: Valid

When 8-bit × 2 channels is selected, timer 0 and timer 1 can be used independently.
When 16-bit × 1 channel is selected, timer 0 and timer 1 are chained together and are used as a 16-bit programmable timer. The clock is input to timer 0 and interrupts will be generated from timer 1.
At initial reset, this register is set to "0".

FCSEL: Timer 0 function selection register (FFC0H•D1)
Selects whether the noise rejector of the clock input circuit will be used or not in the event counter mode.

When "1" is written: With noise rejecter
When "0" is written: Without noise rejecter
Reading: Valid

When "1" is written to the FCSEL register, the noise rejecter is used and counting is done by an external clock (K13) with 0.98 msec or more pulse width. (The noise rejecter allows the counter to input the clock at the second falling edge of the internal 2,048 Hz signal after changing the input level of the K13 input port terminal. Consequently, the pulse width of noise that can reliably be rejected is 0.48 msec or less.)
When "0" is written to the FCSEL register, the noise rejector is not used and the counting is done directly by an external clock input to the K13 input port terminal.
Setting of this register is effective only when timer 0 is used in the event counter mode.
At initial reset, this register is set to "0".

PLPOL: Timer 0 pulse polarity selection register (FFC0H•D0)
Selects the count pulse polarity in the event counter mode.

When "1" is written: Rising edge
When "0" is written: Falling edge
Reading: Valid

The count timing in the event counter mode (timer 0) is selected from either the falling edge of the external clock input to the K10 input port terminal or the rising edge. When "0" is written to the PLPOL register, the falling edge is selected and when "1" is written, the rising edge is selected.
Setting of this register is effective only when timer 0 is used in the event counter mode.
At initial reset, this register is set to "0".

RLD00–RLD07: Timer 0 reload data register (FFC4H, FFC5H)
RLD10–RLD17: Timer 1 reload data register (FFC6H, FFC7H)
Sets the initial value for the counter.
The reload data written in this register is loaded to the respective counters. The counter counts down using the data as the initial value for counting.
Reload data is loaded to the counter when the counter is reset by writing "1" to the PTRST0 or PTRST1 register, or when counter underflow occurs.
At initial reset, these registers are set to "00H".

PTD00–PTD07: Timer 0 counter data (FFC8H, FFC9H)
PTD10–PTD17: Timer 1 counter data (FFCAH, FFCBH)
Count data in the programmable timer can be read from these latches.
The low-order 4 bits of the count data in timer 0 can be read from PTD00–PTD03, and the high-order data can be read from PTD04–PTD07. Similarly, for timer 1, the low-order 4 bits can be read from PTD10–PTD13, and the high-order data can be read from PTD14–PTD17.
Since the high-order 4 bits are held by reading the low-order 4 bits, be sure to read the low-order 4 bits first.
Since these latches are exclusively for reading, the writing operation is invalid.
At initial reset, these counter data are set to "00H".

PTRST0: Timer 0 reset (reload) (FFC2H•D1)
PTRST1: Timer 1 reset (reload) (FFC3H•D1)

Resets the timer and presets reload data to the counter.

When "1" is written: Reset
When "0" is written: No operation
Reading: Always "0"

By writing "1" to PTRST0, the reload data in the reload register PLD00–PLD07 is preset to the counter in timer 0. Similarly, the reload data in PLD10–PLD17 is preset to the counter in timer 1 by PTRST1.
When the counter is preset in the RUN status, the counter restarts immediately after presetting. In the case of STOP status, the reload data is preset to the counter and is maintained.
No operation results when "0" is written.
Since these bits are exclusively for writing, always set to "0" during reading.

PTRUN0: Timer 0 RUN/STOP control register (FFC2H•D0)
PTRUN1: Timer 1 RUN/STOP control register (FFC3H•D0)

Controls the RUN/STOP of the counter.

When "1" is written: RUN
When "0" is written: STOP
Reading: Valid

The counter in timer 0 starts counting down by writing "1" to the PTRUN0 register and stops by writing "0".
In STOP status, the counter data is maintained until the counter is reset or is set in the next RUN status. When STOP status changes to RUN status, the data that has been maintained can be used for resuming the count.
Same as above, the timer 1 counter is controlled by the PTRUN1 register.
At initial reset, these registers are set to "0".

CHSEL: TOUT output channel selection register (FFC1H•D3)

Selects the channel used for TOUT signal output.

When "1" is written: Timer 1
When "0" is written: Timer 0
Reading: Valid

This register selects which timer's underflow (timer 0 or timer 1) is used to generate a TOUT signal. When "0" is written to the CHSEL register, timer 0 is selected and when "1" is written, timer 1 is selected. In the 16-bit × 2 channels mode (MODE16 = "1"), timer 1 is always selected regardless of this register setting.
At initial reset, this register is set to "0".

PTOUT: TOUT output control register (FFC1H•D2)

Turns TOUT signal output ON and OFF.

When "1" is written: ON
When "0" is written: OFF
Reading: Valid

PTOUT is the output control register for the TOUT signal. When "1" is written to the register, the TOUT signal is output from the output port terminal R02 and when "0" is written, the terminal goes to a high (V_{DD}) level. However, the data register R02 must always be "1" and the high impedance control register R02HIZ must always be "0" (data output state).
At initial reset, this register is set to "0".

EIPT0: Timer 0 interrupt mask register (FFE2H•D0)
EIPT1: Timer 1 interrupt mask register (FFE2H•D1)

These registers are used to select whether to mask the programmable timer interrupt or not.

When "1" is written: Enabled
When "0" is written: Masked
Reading: Valid

Timer 0 and timer 1 interrupts can be masked individually by the interrupt mask registers EIPT0 (timer 0) and EIPT1 (timer 1).
At initial reset, these registers are set to "0".

IPT0: Timer 0 interrupt factor flag (FFF2H•D0)
IPT1: Timer 1 interrupt factor flag (FFF2H•D1)

These flags indicate the status of the programmable timer interrupt.

When "1" is read: Interrupt has occurred
When "0" is read: Interrupt has not occurred

When "1" is written: Flag is reset
When "0" is written: Invalid

The interrupt factor flags IPT0 and IPT1 correspond to timer 0 and timer 1 interrupts, respectively. The software can judge from these flags whether there is a programmable timer interrupt. However, even if the interrupt is masked, the flags are set to "1" by the underflows of the corresponding counters.
These flags are reset to "0" by writing "1" to them.
After an interrupt occurs, the same interrupt will occur again if the interrupt enabled state (I flag = "1") is set or the RETI instruction is executed unless the interrupt factor flag is reset. Therefore, be sure to reset (write "1" to) the interrupt factor flag in the interrupt service routine before shifting to the interrupt enabled state.
At initial reset, these flags are set to "0".

4.10.5 Programming notes

(1) When reading counter data, be sure to read the low-order 4 bits (PTD00–PTD03, PTD10–PTD13) first. Furthermore, the high-order 4 bits (PTD04–PTD07, PTD14–PTD17) should be read within 0.73 msec of reading the low-order 4 bits (PTD00–PTD03, PTD10–PTD13).
For the 16 bit × 1 mode, be sure to read as following sequence:
(PTD00–PTD03) → (PTD04–PTD07) → (PTD10–PTD13) → (PTD14–PTD17)
The read sequence time should be within 1.46 msec.

(2) The programmable timer actually enters RUN/STOP status in synchronization with the falling edge of the input clock after writing to the PTRUN0/PTRUN1 register. Consequently, when "0" is written to the PTRUN0/PTRUN1 register, the timer enters STOP status at the point where the counter is decremented (-1). The PTRUN0/PTRUN1 register maintains "1" for reading until the timer actually stops.
Figure 4.10.5.1 shows the timing chart for the RUN/STOP control.

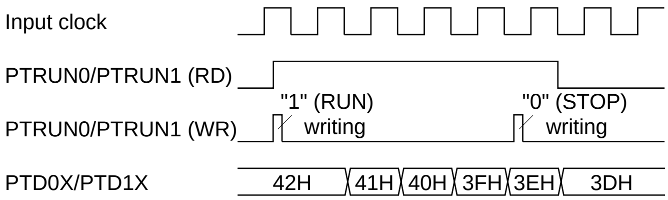


Fig. 4.10.5.1 Timing chart for RUN/STOP control

It is the same even in the event counter mode. Therefore, be aware that the counter does not enter RUN/STOP status if a clock is not input after setting the RUN/STOP control register (PTRUN0).

(3) Since the TOUT signal is generated asynchronously from the PTOUT register, a hazard within 1/2 cycle is generated when the signal is turned ON and OFF by setting the register.

(4) When the OSC3 oscillation clock is selected for the clock source, it is necessary to turn the OSC3 oscillation ON, prior to using the programmable timer. However the OSC3 oscillation circuit requires a time interval of several msec to several 10 msec from turning the circuit ON until the oscillation stabilizes. Therefore, allow an adequate interval from turning the OSC3 oscillation circuit ON to starting the programmable timer. Refer to Section 4.4, "Oscillation Circuit", for the control and notes of the OSC3 oscillation circuit.
At initial reset, the OSC3 oscillation circuit is set in the OFF state.

(5) After an interrupt occurs, the same interrupt will occur again if the interrupt enabled state (I flag = "1") is set or the RETI instruction is executed unless the interrupt factor flag is reset. Therefore, be sure to reset (write "1" to) the interrupt factor flag in the interrupt service routine before shifting to the interrupt enabled state.

4.11 Serial Interface (SIN, SOUT, $\overline{SCLK}$, $\overline{SRDY}$)

4.11.1 Configuration of serial interface

The E0C63158 has a synchronous clock type 8 bits serial interface built-in.
The configuration of the serial interface is shown in Figure 4.11.1.1.
The CPU, via the 8-bit shift register, can read the serial input data from the SIN terminal. Moreover, via the same 8-bit shift register, it can convert parallel data to serial data and output it to the SOUT terminal.
The synchronous clock for serial data input/output may be set by selecting by software any one of three types of master mode (internal clock mode: when the E0C63158 is to be the master for serial input/output) and a type of slave mode (external clock mode: when the E0C63158 is to be the slave for serial input/output).
Also, when the serial interface is used at slave mode, $\overline{SRDY}$ signal which indicates whether or not the serial interface is available to transmit or receive can be output to the $\overline{SRDY}$ terminal.

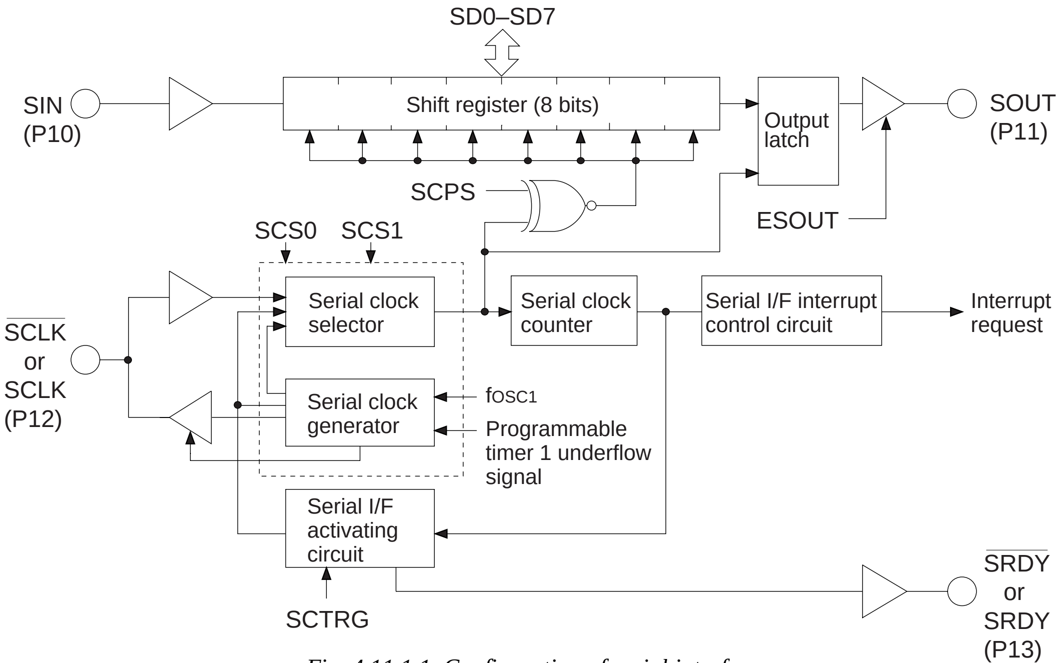


Fig. 4.11.1.1 Configuration of serial interface

The input/output ports of the serial interface are shared with the I/O ports P10–P13, and function of these ports can be selected through the software.
P10–P13 terminals and serial input/output correspondence are as follows:

Master mode	***Slave mode***
P10 = SIN (I)	P10 = SIN (I)
P11 = SOUT (O)	P11 = SOUT (O)
P12 = $\overline{SCLK}$ (O)	P12 = $\overline{SCLK}$ (I)
P13 = I/O port (I/O)	P13 = $\overline{SRDY}$ (O)

Note: At initial reset, P10–P13 are set to I/O ports.
When using the serial interface, switch the function (ESIF = "1") in the initial routine.

The SOUT (data output) signal passes through a tri-state buffer. To output serial data, write "1" to the ESOUT register to set the buffer in data output status. When the ESOUT register is set to "0", the SOUT signal is disabled and the SOUT terminal goes high-impedance status.

4.11.2 Mask option

(1) Terminal specification

Since the input/output terminals of the serial interface is shared with the I/O ports (P10–P13), the mask option that selects the output specification for the I/O port is also applied to the serial interface. The output specification of the terminals SOUT, $\overline{\text{SCLK}}$ (during the master mode) and $\overline{\text{SRDY}}$ (during the slave mode) that are used as output in the input/output port of the serial interface is respectively selected by the mask options of P11, P12 and P13. Either complementary output or N-channel open drain output can be selected as the output specification. However, when N-channel open drain output is selected, do not apply a voltage exceeding the power supply voltage to the terminal.

Furthermore, the pull-up resistor for the SIN terminal and the $\overline{\text{SCLK}}$ terminal (during slave mode) that are used as input terminals can be selected by the mask options of P10 and P12.
When "Gate dirct" is selected, take care that the floating status does not occur.

(2) Polarity of synchronous clock and ready signal

Polarity of the synchronous clock and the ready signal that is output in the slave mode can be selected from either positive polarity (high active, SCLK & SRDY) or negative polarity (low active, $\overline{\text{SCLK}}$ & $\overline{\text{SRDY}}$).
When operating the serial interface in the slave mode, the synchronous clock is input from a external device. Be aware that the terminal specification is pull-up only and a pull-down resistor cannot be built in if positive polarity is selected.
In the following explanation, it is assumed that negative polarity ($\overline{\text{SCLK}}$, $\overline{\text{SRDY}}$) has been selected.

4.11.3 Master mode and slave mode of serial interface

The serial interface of the E0C63158 has two types of operation mode: master mode and slave mode.
The master mode uses an internal clock as the synchronous clock for the built-in shift register, and outputs this internal clock from the $\overline{\text{SCLK}}$ (P12) terminal to control the external (slave side) serial device.
In the slave mode, the synchronous clock output from the external (master side) serial device is input from the $\overline{\text{SCLK}}$ (P12) terminal and it is used as the synchronous clock for the built-in shift register.
The master mode and slave mode are selected by writing data to the SCS1 and SCS0 registers.
When the master mode is selected, a synchronous clock may be selected from among 3 types as shown in Table 4.11.3.1.

Table 4.11.3.1 Synchronous clock selection

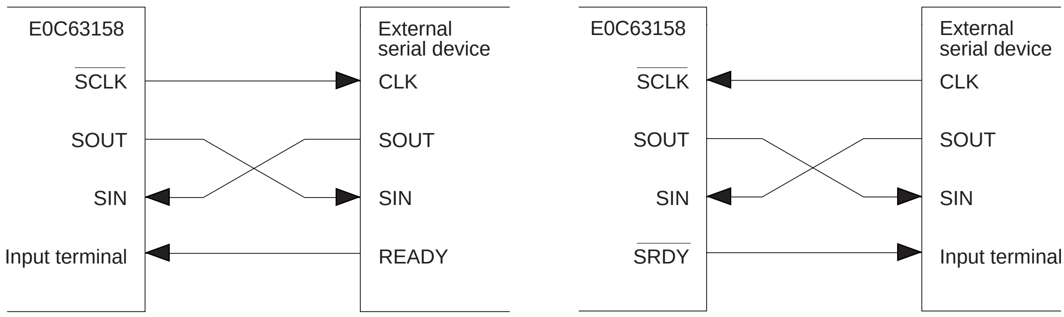
SCS1	SCS0	Mode	Synchronous clock
1	1	Master mode	OSC1
1	0		OSC1 /2
0	1		Programmable timer
0	0	Slave mode	External clock

When the programmable timer is selected, the signal that is generated by dividing the underflow signal of the programmable timer (timer 1) in 1/2 is used as the synchronous clock. In this case, the programmable timer must be controlled before operating the serial interface. Refer to Section 4.10, "Programmable Timer" for the control of the programmable timer.

At initial reset, the slave mode (external clock mode) is selected.
Moreover, the synchronous clock, along with the input/output of the 8-bit serial data, is controlled as follows:

- In the master mode, after output of 8 clocks from the $\overline{\text{SCLK}}$ (P12) terminal, clock output is automatically suspended and the $\overline{\text{SCLK}}$ (P12) terminal is fixed at high level.
- In the slave mode, after input of 8 clocks to the $\overline{\text{SCLK}}$ (P12) terminal, subsequent clock inputs are masked.

A sample basic serial input/output portion connection is shown in Figure 4.11.3.1.



(a) Master mode (b) Slave mode

Fig. 4.11.3.1 Sample basic connection of serial input/output section

4.11.4 Data input/output and interrupt function

The serial interface of E0C63158 can input/output data via the internal 8-bit shift register. The shift register operates by synchronizing with either the synchronous clock output from the $\overline{\text{SCLK}}$ (P12) terminal (master mode), or the synchronous clock input to the $\overline{\text{SCLK}}$ (P12) terminal (slave mode).
The serial interface generates an interrupt on completion of the 8-bit serial data input/output. Detection of serial data input/output is done by counting of the synchronous clock $\overline{\text{SCLK}}$; the clock completes input/output operation when 8 counts (equivalent to 8 cycles) have been made and then generates an interrupt.
The serial data input/output procedure is explained below:

(1) Serial data output procedure and interrupt

The E0C63158 serial interface is capable of outputting parallel data as serial data, in units of 8 bits.
By setting the parallel data to the data registers SD0–SD3 (FF72H) and SD4–SD7 (FF73H) and writing "1" to SCTRG bit (FF70H•D1), it synchronizes with the synchronous clock and the serial data is output to the SOUT (P11) terminal. The synchronous clock used here is as follows: in the master mode, internal clock which is output to the $\overline{\text{SCLK}}$ (P12) terminal while in the slave mode, external clock which is input from the $\overline{\text{SCLK}}$ (P12) terminal.
Shift timing of serial data is as follows:

- ***When negative polarity is selected for the synchronous clock (mask option):***
  The serial data output to the SOUT (P11) terminal changes at the falling edge of the clock input or output from/to the $\overline{\text{SCLK}}$ (P12) terminal. The data in the shift register is shifted at the falling edge of the $\overline{\text{SCLK}}$ signal when the SCPS register (FF71H•D2) is "1" and is shifted at the rising edge of the $\overline{\text{SCLK}}$ signal when the SCPS register is "0".

- ***When positive polarity is selected for the synchronous clock (mask option):***
  The serial data output to the SOUT (P11) terminal changes at the rising edge of the clock input or output from/to the SCLK (P12) terminal. The data in the shift register is shifted at the rising edge of the SCLK signal when the SCPS register is "1" and is shifted at the falling edge of the SCLK signal when the SCPS register is "0".

When the output of the 8-bit data from SD0 to SD7 is completed, the interrupt factor flag ISIF (FFF3H•D0) is set to "1" and an interrupt occurs. Moreover, the interrupt can be masked by the interrupt mask register EISIF (FFE3H•D0). However, regardless of the interrupt mask register setting, the interrupt factor flag is set to "1" after output of the 8-bit data.

(2) Serial data input procedure and interrupt

The E0C63158 serial interface is capable of inputting serial data as parallel data, in units of 8 bits.
The serial data is input from the SIN (P10) terminal, synchronizes with the synchronous clock, and is sequentially read in the 8-bit shift register. As in the above item (1), the synchronous clock used here is as follows: in the master mode, internal clock which is output to the $\overline{SCLK}$ (P12) terminal while in the slave mode, external clock which is input from the $\overline{SCLK}$ (P12) terminal.
Shift timing of serial data is as follows:

- ***When negative polarity is selected for the synchronous clock (mask option):***
  The serial data is read into the built-in shift register at the falling edge of the $\overline{SCLK}$ signal when the SCPS register is "1" and is read at the rising edge of the $\overline{SCLK}$ signal when the SCPS register is "0". The shift register is sequentially shifted as the data is fetched.
- ***When positive polarity is selected for the synchronous clock (mask option):***
  The serial data is read into the built-in shift register at the rising edge of the SCLK signal when the SCPS register is "1" and is read at the falling edge of the SCLK signal when the SCPS register is "0". The shift register is sequentially shifted as the data is fetched.

When the input of the 8-bit data from SD0 to SD7 is completed, the interrupt factor flag ISIF is set to "1" and an interrupt is generated. Moreover, the interrupt can be masked by the interrupt mask register EISIF. However, regardless of the interrupt mask register setting, the interrupt factor flag is set to "1" after input of the 8-bit data.
The data input in the shift register can be read from data registers SD0–SD7 by software.

(3) Serial data input/output permutation

The E0C63158 allows the input/output permutation of serial data to be selected by the SDP register (FF71H•D3) as to either LSB first or MSB first. The block diagram showing input/output permutation in case of LSB first and MSB first is provided in Figure 4.11.4.1. The SDP register should be set before setting data to SD0–SD7.

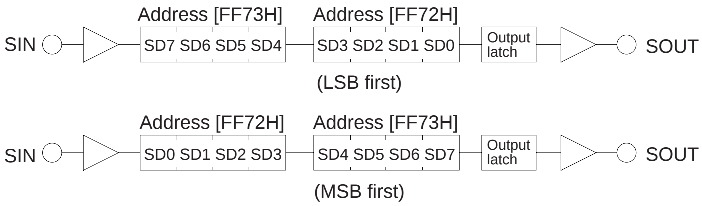


Fig. 4.11.4.1 Serial data input/output permutation

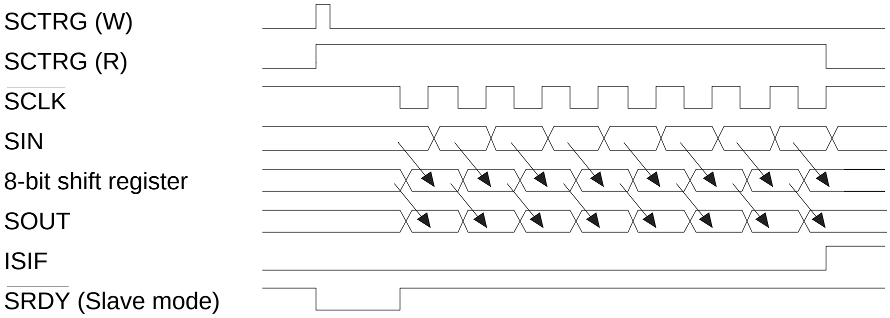
(4) $\overline{SRDY}$ signal

When the E0C63158 serial interface is used in the slave mode (external clock mode), $\overline{SRDY}$ signal is used to indicate whether the internal serial interface is available to transmit or receive data for the master side (external) serial device. $\overline{SRDY}$ signal is output from the $\overline{SRDY}$ (P13) terminal.
Output timing of $\overline{SRDY}$ signal is as follows:

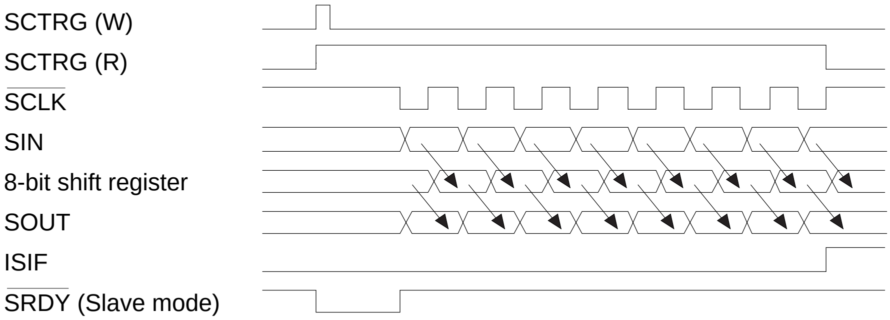
- ***When negative polarity is selected (mask option):***
  $\overline{SRDY}$ signal goes "0" (low) when the E0C63158 serial interface is available to transmit or receive data; normally, it is at "1" (high).
  $\overline{SRDY}$ signal changes from "1" to "0" immediately after "1" is written to SCTRG and returns from "0" to "1" when "0" is input to the $\overline{SCLK}$ (P12) terminal (i.e., when the serial input/output begins transmitting or receiving data). Moreover, when high-order data is read from or written to SD4–SD7, the $\overline{SRDY}$ signal returns to "1".
- ***When positive polarity is selected (mask option):***
  SRDY signal goes "1" (high) when the E0C63158 serial interface is available to transmit or receive data; normally, it is at "0" (low).
  SRDY signal changes from "0" to "1" immediately after "1" is written to SCTRG and returns from "1" to "0" when "1" is input to the SCLK (P12) terminal (i.e., when the serial input/output begins transmitting or receiving data). Moreover, when high-order data is read from or written to SD4–SD7, the SRDY signal returns to "0".

(5) Timing chart

The E0C63158 serial interface timing charts are shown in Figures 4.11.4.2 and 4.11.4.3.

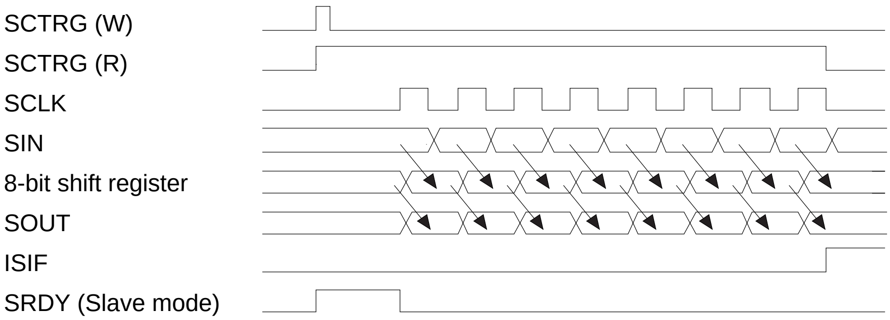


(a) When SCPS = "1"

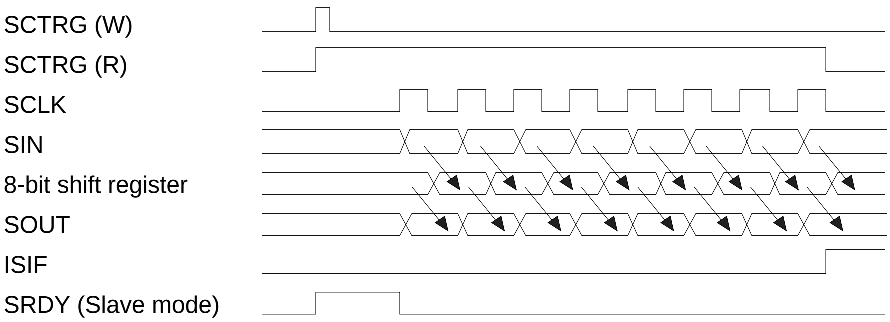


(b) When SCPS = "0"

Fig. 4.11.4.2 Serial interface timing chart (when synchronous clock is negative polarity SCLK)



(a) When SCPS = "1"



(b) When SCPS = "0"

Fig. 4.11.4.3 Serial interface timing chart (when synchronous clock is positive polarity SCLK)

4.11.5 I/O memory of serial interface

Table 4.11.5.1 shows the I/O addresses and the control bits for the serial interface.

Table 4.11.5.1 Control bits of serial interface

Address	Register D3	Register D2	Register D1	Register D0	Name	Init *1	1	0	Comment
FF45H	PUL13	PUL12	PUL11	PUL10	PUL13	1	On	Off	P13 pull-up control register functions as a general-purpose register when SIF (slave) is selected
	R/W				PUL12	1	On	Off	P12 pull-up control register (EISF=0) functions as a general-purpose register when SIF (master) is selected $\overline{SCLK}$ (I) pull-up control register when SIF (slave) is selected
					PUL11	1	On	Off	P11 pull-up control register (EISF=0) functions as a general-purpose register when SIF is selected
					PUL10	1	On	Off	P10 pull-up control register (EISF=0) SIN pull-up control register when SIF is selected
FF70H	0	ESOUT	SCTRG	ESIF	0 *3	– *2			Unused
	R	R/W			ESOUT	0	Enable	Disable	SOUT enable/disable control
					SCTRG	0	Trigger	Invalid	Serial I/F clock trigger (writing)
							Run	Stop	Serial I/F clock status (reading)
					ESIF	0	SIF	I/O	Serial I/F enable (P1 port function selection)
FF71H	SDP	SCPS	SCS1	SCS0	SDP	0	MSB first	LSB first	Serial I/F data input/output permutation
	R/W				SCPS	0			Serial I/F clock phase selection –Negative polarity (mask option) –Positive polarity (mask option)
					SCS1	0			Serial I/F clock mode selection [SCS1, 0]: 0 / 1 — Clock: Slave / PT [SCS1, 0]: 2 / 3 — Clock: OSC1/2 / OSC1
					SCS0	0			
FF72H	SD3	SD2	SD1	SD0	SD3	– *2	High	Low	MSB
	R/W				SD2	– *2	High	Low	Serial I/F transmit/receive data (low-order 4 bits)
					SD1	– *2	High	Low	
					SD0	– *2	High	Low	LSB
FF73H	SD7	SD6	SD5	SD4	SD7	– *2	High	Low	MSB
	R/W				SD6	– *2	High	Low	Serial I/F transmit/receive data (high-order 4 bits)
					SD5	– *2	High	Low	
					SD4	– *2	High	Low	LSB
FFE3H	0	0	0	EISIF	0 *3	– *2			Unused
	R			R/W	0 *3	– *2			Unused
					0 *3	– *2			Unused
					EISIF	0	Enable	Mask	Interrupt mask register (Serial I/F)
FFF3H	0	0	0	ISIF	0 *3	– *2	(R)	(R)	Unused
	R			R/W	0 *3	– *2	Yes	No	Unused
					0 *3	– *2	(W)	(W)	Unused
					ISIF	0	Reset	Invalid	Interrupt factor flag (Serial I/F)

*1 Initial value at initial reset

*2 Not set in the circuit

*3 Constantly "0" when being read

ESIF: Serial interface enable register (P1 port function selection) (FF70H•D0)

Sets P10–P13 to the input/output port for the serial interface.

When "1" is written: Serial interface
When "0" is written: I/O port
Reading: Valid

When "1" is written to the ESIF register, P10, P11, P12 and P13 function as SIN, SOUT, $\overline{SCLK}$, $\overline{SRDY}$, respectively.
In the slave mode, the P13 terminal functions as $\overline{SRDY}$ output terminal, while in the master mode, it functions as the I/O port terminal.
At initial reset, this register is set to "0".

ESOUT: SOUT enable/disable control register (FF70H•D2)

Enables output of the SOUT signal.

When "1" is written: Enabled
When "0" is written: Disabled
Reading: Valid

When "1" is written to the ESOUT register, the SOUT terminal can output serial data. When "0" is written, the SOUT terminal goes high-impedance status.
At initial reset, this register is set to "0".

PUL10: SIN (P10) pull-up control register (FF45H•D0)
PUL12: $\overline{SCLK}$ (P12) pull-up control register (FF45H•D2)

Sets the pull-up of the SIN terminal and the $\overline{SCLK}$ terminals (in the slave mode).

When "1" is written: Pull-up ON
When "0" is written: Pull-up OFF
Reading: Valid

Sets the pull-up resistor built into the SIN (P10) and $\overline{SCLK}$ (P12) terminals to ON or OFF. (Pull-up resistor is only built in the port selected by mask option.)
$\overline{SCLK}$ pull-up is effective only in the slave mode. In the master mode, the PUL12 register can be used as a general purpose register.
At initial reset, these registers are set to "1" and pull-up goes ON.

SCS1, SCS0: Clock mode selection register (FF71H•D0, D1)

Selects the synchronous clock ($\overline{SCLK}$) for the serial interface.

Table 4.11.5.2 Synchronous clock selection

SCS1	SCS0	Mode	Synchronous clock
1	1	Master mode	OSC1
1	0		OSC1 /2
0	1		Programmable timer
0	0	Slave mode	External clock

Synchronous clock ($\overline{SCLK}$) is selected from among the above 4 types: 3 types of internal clock and external clock.
When the programmable timer is selected, the signal that is generated by dividing the underflow signal of the programmable timer (timer 1) in 1/2 is used as the synchronous clock. In this case, the programmable timer must be controlled before operating the serial interface. Refer to Section 4.10, "Programmable Timer" for the control of the programmable timer.
At initial reset, external clock is selected.

SCPS: Clock phase selection register (FF71H•D2)

Selects the timing for reading in the serial data input from the SIN (P10) terminal.

• ***When negative polarity is selected:***

When "1" is written: Falling edge of $\overline{SCLK}$
When "0" is written: Rising edge of $\overline{SCLK}$
Reading: Valid

• ***When positive polarity is selected:***

When "1" is written: Rising edge of SCLK
When "0" is written: Falling edge of SCLK
Reading: Valid

Select whether the fetching for the serial input data to registers (SD0–SD7) at the rising edge or falling edge of the synchronous signal.

Pay attention to the polarity of the synchronous clock selected by the mask option because the selection content is different.
The input data fetch timing may be selected but output timing for output data is fixed at the falling edge of $\overline{\text{SCLK}}$ (when negative polarity is selected) or at the rising edge of SCLK (when positive polarity is selected).
At initial reset, this register is set to "0".

SDP: Data input/output permutation selection register (FF71H•D3)

Selects the serial data input/output permutation.

When "1" is written: MSB first
When "0" is written: LSB first
Reading: Valid

Select whether the data input/output permutation will be MSB first or LSB first.
At initial reset, this register is set to "0".

SCTRG: Clock trigger/status (FF70H•D1)

This is a trigger to start input/output of synchronous clock ($\overline{\text{SCLK}}$).

• ***When writing***

When "1" is written: Trigger
When "0" is written: No operation

When this trigger is supplied to the serial interface activating circuit, the synchronous clock ($\overline{\text{SCLK}}$) input/output is started.
As a trigger condition, it is required that data writing or reading on data registers SD0–SD7 be performed prior to writing "1" to SCTRG. (The internal circuit of the serial interface is initiated through data writing/reading on data registers SD0–SD7.) In addition, be sure to enable the serial interface with the ESIF register before setting the trigger.
Supply trigger only once every time the serial interface is placed in the RUN state. Refrain from performing trigger input multiple times, as leads to malfunctioning.
Moreover, when the synchronous clock $\overline{\text{SCLK}}$ is external clock, start to input the external clock after the trigger.

• ***When reading***

When "1" is read: RUN (during input/output the synchronous clock)
When "0" is read: STOP (the synchronous clock stops)
Writing: Invalid

When this bit is read, it indicates the status of serial interface clock.
After "1" is written to SCTRG, this value is latched till serial interface clock stops (8 clock counts). Therefore, if "1" is read, it indicates that the synchronous clock is in input/output operation.
When the synchronous clock input/output is completed, this latch is reset to "0".
At initial reset, this bit is set to "0".

SD0–SD3, SD4–SD7: Serial interface data register (FF72H, FF73H)

These registers are used for writing and reading serial data.

• ***When writing***

When "1" is written: High level
When "0" is written: Low level

Write data to be output in these registers. The register data is converted into serial data and output from the SOUT (P11) terminal; data bits set at "1" are output as high (V_{DD}) level and data bits set at "0" are output as low (V_{SS}) level.

• ***When reading***

When "1" is read: High level
When "0" is read: Low level

The serial data input from the SIN (P10) terminal can be read from these registers.
The serial data input from the SIN (P10) terminal is converted into parallel data, as a high (VDD) level bit into "1" and as a low (VSS) level bit into "0", and is loaded to these registers. Perform data reading only while the serial interface is not running (i.e., the synchronous clock is neither being input or output).

At initial reset, these registers are undefined.

EISIF: Interrupt mask register (FFE3H•D0)
Masking the interrupt of the serial interface can be selected with this register.

When "1" is written: Enabled
When "0" is written: Masked
Reading: Valid

With this register, it is possible to select whether the serial interface interrupt is to be masked or not.
At initial reset, this register is set to "0".

ISIF: Interrupt factor flag (FFF3H•D0)
This flag indicates the occurrence of serial interface interrupt.

When "1" is read: Interrupt has occurred
When "0" is read: Interrupt has not occurred
Writing: Invalid

From the status of this flag, the software can decide whether the serial interface interrupt.
This flag is set to "1" after an 8-bit data input/output even if the interrupt is masked.
This flag is reset to "0" by writing "1" to it.
After an interrupt occurs, the same interrupt will occur again if the interrupt enabled state (I flag = "1") is set or the RETI instruction is executed unless the interrupt factor flag is reset. Therefore, be sure to reset (write "1" to) the interrupt factor flag in the interrupt service routine before shifting to the interrupt enabled state.
At initial reset, this flag is set to "0".

4.11.6 Programming notes

(1) Perform data writing/reading to the data registers SD0–SD7 only while the serial interface is not running (i.e., the synchronous clock is neither being input or output).

(2) As a trigger condition, it is required that data writing or reading on data registers SD0–SD7 be performed prior to writing "1" to SCTRG. (The internal circuit of the serial interface is initiated through data writing/reading on data registers SD0–SD7.) In addition, be sure to enable the serial interface with the ESIF register before setting the trigger.
Supply trigger only once every time the serial interface is placed in the RUN state. Refrain from performing trigger input multiple times, as leads to malfunctioning. Moreover, when the synchronous clock $\overline{\text{SCLK}}$ is external clock, start to input the external clock after the trigger.

(3) Setting of the input/output permutation (MSB first/LSB first) with the SDP register should be done before setting data to SD0–SD7.

(4) After an interrupt occurs, the same interrupt will occur again if the interrupt enabled state (I flag = "1") is set or the RETI instruction is executed unless the interrupt factor flag is reset. Therefore, be sure to reset (write "1" to) the interrupt factor flag in the interrupt service routine before shifting to the interrupt enabled state.

(5) Be aware that the maximum clock frequency for the serial interface is limited to 1 MHz when OSC3 is used as the clock source of the programmable timer or in the slave mode.

4.12 Buzzer Output Circuit

4.12.1 Configuration of buzzer output circuit

The E0C63158 is capable of generating buzzer signal to drive a piezo-electric buzzer. The buzzer signal is output from the BZ terminal by software control. Furthermore, the buzzer signal frequency can be set to 2 kHz or 4 kHz with 2 Hz interval by software.
Figure 4.12.1.1 shows the configuration of the buzzer output circuit.

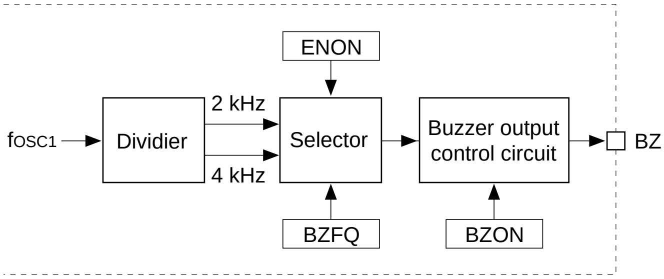
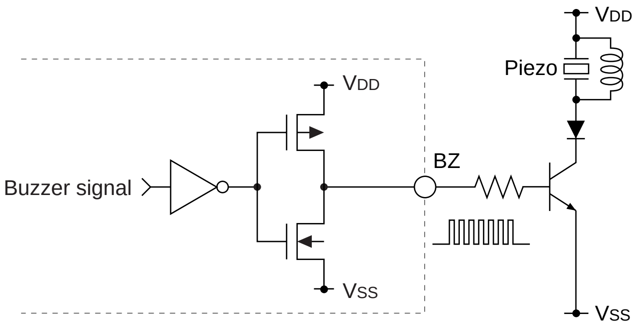


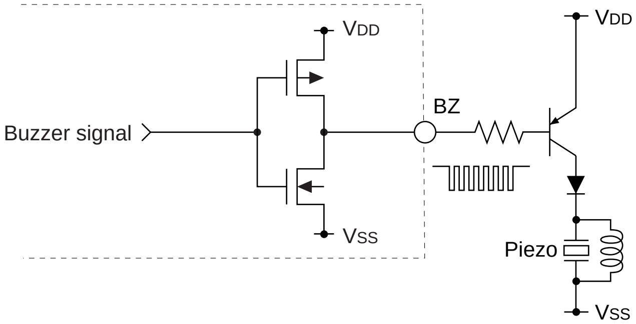
Fig. 4.12.1.1 Configuration of buzzer output circuit

4.12.2 Mask option

Polarity of the buzzer signal output from the BZ terminal can be selected as either positive polarity or negative polarity. Figure 4.12.2.1 shows each output circuit configuration and the output waveform.
When positive polarity is selected, the BZ terminal goes to a low (V_{SS}) level when the buzzer signal is not output. Select positive polarity when driving a piezo buzzer by externally connecting an NPN transistor.
When negative polarity is selected, the BZ terminal goes to a high (V_{DD}) level when the buzzer signal is not output. Select negative polarity when driving a piezo buzzer by externally connecting a PNP transistor.



(a) When positive polarity is selected



(b) When negative polarity is selected

Fig. 4.12.2.1 Configuration of output circuit

4.12.3 Control of buzzer output

The buzzer signal frequency is selected by the buzzer frequency selection register BZFQ. When "1" is written to the BZFQ register, the frequency is set to 2 kHz. When "0" is written, it is set to 4 kHz. This signal is generated by dividing the fOSC1.

fOSC1	2 kHz	4 kHz
32.768 kHz	fOSC1 /16	fOSC1 /8

The buzzer signal is output from the BZ terminal by writing "1" to the buzzer output control register BZON.
When negative polarity is selected, the BZ terminal goes to a high (VDD) level by writing "0" to the BZON register. When positive polarity is selected, the BZ terminal goes to a low (VSS) level by writing "0".

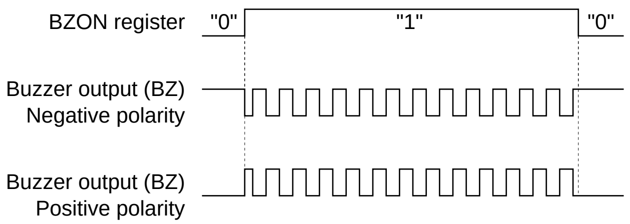


Fig. 4.12.3.1 Timing chart of buzzer signal output

2 Hz intervals can be added to the buzzer signal when "1" is written to the ENON register.

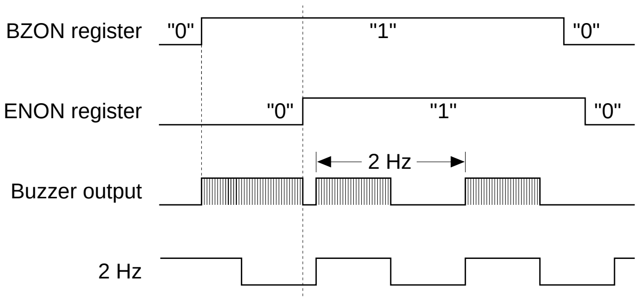


Fig. 4.12.3.2 2 Hz interval

Note: Since it generates a buzzer signal that is out of synchronization with the BZON register, hazards may at times be produced when the signal goes ON/OFF due to the setting of the BZON register.

4.12.4 I/O memory of buzzer output circuit

Table 4.12.4.1 shows the I/O address and the control bits for the buzzer output circuit.

Table 4.12.4.1 Control bits of buzzer output circuit

Address	Register								Comment
	D3	D2	D1	D0	Name	Init *1	1	0	
FF64H	0	ENON	BZFQ	BZON	0 *3	– *2			Unused
					ENON	0	On	Off	2 Hz interval On/Off
	R	R/W			BZFQ	0	2 kHz	4 kHz	Buzzer frequency selection
					BZON	0	On	Off	Buzzer output On/Off

*1 Initial value at initial reset

*2 Not set in the circuit

*3 Constantly "0" when being read

ENON: Interval ON/OFF control register (FF64H•D2)

Controls the addition of a 2 Hz interval onto the buzzer signal.

When "1" is written: ON
When "0" is written: OFF
Reading: Valid

Writing "1" into the ENON causes a 2 Hz ON/OFF interval to be added during buzzer signal output.
When "0" has been written, a 2 Hz ON/OFF interval is not added.
At initial reset, this register is set to "0".

BZFQ: Buzzer frequency selection register (FF64H•D1)

Selects the buzzer signal frequency.

When "1" is written: 2 kHz
When "0" is written: 4 kHz
Reading: Valid

When "1" is written to BZFQ, the frequency is set to 2 kHz. When "0" is written, it is set to 4 kHz.
At initial reset, this register is set to "0".

BZON: Buzzer output control (ON/OFF) register (FF64H•D0)

Controls the buzzer signal output.

When "1" is written: Buzzer output ON
When "0" is written: Buzzer output OFF
Reading: Valid

When "1" is written to BZON, the buzzer signal is output from the BZ terminal. When "0" is written, the BZ terminal goes to a high (V_{DD}) level (when negative polarity is selected by mask option) or to a low (V_{SS}) level (when positive polarity is selected by mask option).
At initial reset, this register is set to "0".

4.12.5 Programming note

Since it generates a buzzer signal that is out of synchronization with the BZON register, hazards may at times be produced when the signal goes ON/OFF due to the setting of the BZON register.

4.13 SVD (Supply Voltage Detection) Circuit

4.13.1 Configuration of SVD circuit

The E0C63158 has a built-in SVD (supply voltage detection) circuit, so that the software can find when the source voltage lowers. Turning the SVD circuit ON/OFF and the SVD criteria voltage setting can be done with software.
Figure 4.13.1.1 shows the configuration of the SVD circuit.

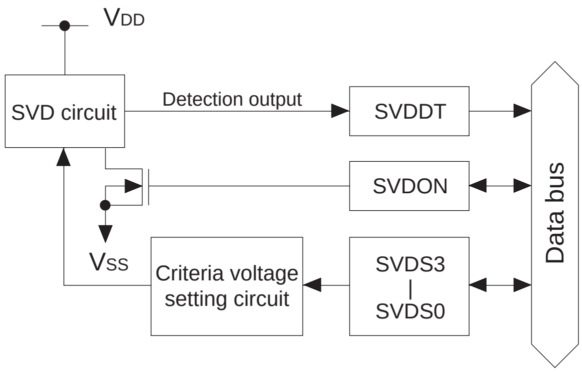


Fig. 4.13.1.1 Configuration of SVD circuit

4.13.2 SVD operation

The SVD circuit compares the criteria voltage set by software and the supply voltage (VDD–VSS) and sets its results into the SVDDT latch. By reading the data of this SVDDT latch, it can be determined by means of software whether the supply voltage is normal or has dropped.
The criteria voltage can be set for the 16 types shown in Table 4.13.2.1 by the SVDS3–SVDS0 registers.

Table 4.13.2.1 Criteria voltage setting

SVDS3	SVDS2	SVDS1	SVDS0	Criteria voltage (V)	SVDS3	SVDS2	SVDS1	SVDS0	Criteria voltage (V)
0	1	1	1	1.60	1	1	1	1	2.60
0	1	1	0	1.40	1	1	1	0	2.50
0	1	0	1	1.30	1	1	0	1	2.30
0	1	0	0	1.25	1	1	0	0	2.20
0	0	1	1	1.20	1	0	1	1	2.10
0	0	1	0	1.15	1	0	1	0	2.05
0	0	0	1	1.10	1	0	0	1	2.00
0	0	0	0	1.05	1	0	0	0	1.95

When the SVDON register is set to "1", source voltage detection by the SVD circuit is executed. As soon as the SVDON register is reset to "0", the result is loaded to the SVDDT latch and the SVD circuit goes OFF.
To obtain a stable detection result, the SVD circuit must be ON for at least l00 µsec. So, to obtain the SVD detection result, follow the programming sequence below.

1. Set SVDON to "1"
2. Maintain for 100 µsec minimum
3. Set SVDON to "0"
4. Read SVDDT

When the SVD circuit is ON, the IC draws a large current, so keep the SVD circuit off unless it is.

4.13.3 I/O memory of SVD circuit

Table 4.13.3.1 shows the I/O addresses and the control bits for the SVD circuit.

Table 4.13.3.1 Control bits of SVD circuit

Address	Register								Comment
	D3	D2	D1	D0	Name	Init *1	1	0	
FF04H	SVDS3	SVDS2	SVDS1	SVDS0	SVDS3	0			SVD criteria voltage setting (see below)
	R/W				SVDS2	0			
					SVDS1	0			
					SVDS0	0			
FF05H	0	0	SVDDT	SVDON	0 *3	– *2			Unused
	R			R/W	0 *3	– *2			Unused
					SVDDT	0	Low	Normal	SVD evaluation data
					SVDON	0	On	Off	SVD circuit On/Off

SVD criteria voltage setting:

[SVDS3–0]	0	1	2	3	4	5	6	7
Voltage(V)	1.05	1.10	1.15	1.20	1.25	1.30	1.40	1.60
[SVDS3–0]	8	9	10	11	12	13	14	15
Voltage(V)	1.95	2.00	2.05	2.10	2.20	2.30	2.50	2.60

*1 Initial value at initial reset
*2 Not set in the circuit
*3 Constantly "0" when being read

SVDS3–SVDS0: SVD criteria voltage setting register (FF04H)
Criteria voltage for SVD is set as shown in Table 4.13.2.1.
At initial reset, this register is set to "0".

SVDON: SVD control (ON/OFF) register (FF05H•D0)
Turns the SVD circuit ON and OFF.

When "1" is written: SVD circuit ON
When "0" is written: SVD circuit OFF
Reading: Valid

When the SVDON register is set to "1", a source voltage detection is executed by the SVD circuit. As soon as SVDON is reset to "0", the result is loaded to the SVDDT latch. To obtain a stable detection result, the SVD circuit must be ON for at least l00 µsec.
At initial reset, this register is set to "0".

SVDDT: SVD data (FF05H•D1)
This is the result of supply voltage detection.

When "0" is read: Supply voltage (V_{DD}–V_{SS}) ≥ Criteria voltage
When "1" is read: Supply voltage (V_{DD}–V_{SS}) < Criteria voltage
Writing: Invalid

The result of supply voltage detection at time of SVDON is set to "0" can be read from this latch.
At initial reset, SVDDT is set to "0".

4.13.4 Programming notes

(1) To obtain a stable detection result, the SVD circuit must be ON for at least l00 µsec. So, to obtain the SVD detection result, follow the programming sequence below.

1. Set SVDON to "1"
2. Maintain for 100 µsec minimum
3. Set SVDON to "0"
4. Read SVDDT

(2) The SVD circuit should normally be turned OFF because SVD operation increase current consumption.

4.14 Interrupt and HALT

<Interrupt types>

The E0C63158 provides the following interrupt functions.

External interrupt:	• Input interrupt	(3 systems)
Internal interrupt:	• Watchdog timer interrupt	(NMI, 1 system)
	• Programmable timer interrupt	(2 systems)
	• Serial interface interrupt	(1 system)
	• Timer interrupt	(4 systems)
	• A/D converter interrupt	(1 system)

To authorize interrupt, the interrupt flag must be set to "1" (EI) and the necessary related interrupt mask registers must be set to "1" (enable).
When an interrupt occurs the interrupt flag is automatically reset to "0" (DI), and interrupts after that are inhibited.

The watchdog timer interrupt is an NMI (non-maskable interrupt), therefore, the interrupt is generated regardless of the interrupt flag setting. Also the interrupt mask register is not provided. However, it is possible to not generate NMI since software can stop the watchdog timer operation.

Figure 4.14.1 shows the configuration of the interrupt circuit.

Note: After an initial reset, all the interrupts including NMI are masked until both the stack pointers SP1 and SP2 are set with the software. Be sure to set the SP1 and SP2 in the initialize routine. Further, when re-setting the stack pointer, the SP1 and SP2 must be set as a pair. When one of them is set, all the interrupts including NMI are masked and interrupts cannot be accepted until the other one is set.

<HALT>

The E0C63158 has HALT functions that considerably reduce the current consumption when it is not necessary.
The CPU enters HALT status when the HALT instruction is executed.
In HALT status, the operation of the CPU is stopped. However, timers continue counting since the oscillation circuit operates. Reactivating the CPU from HALT status is done by generating a hardware interrupt request including NMI.

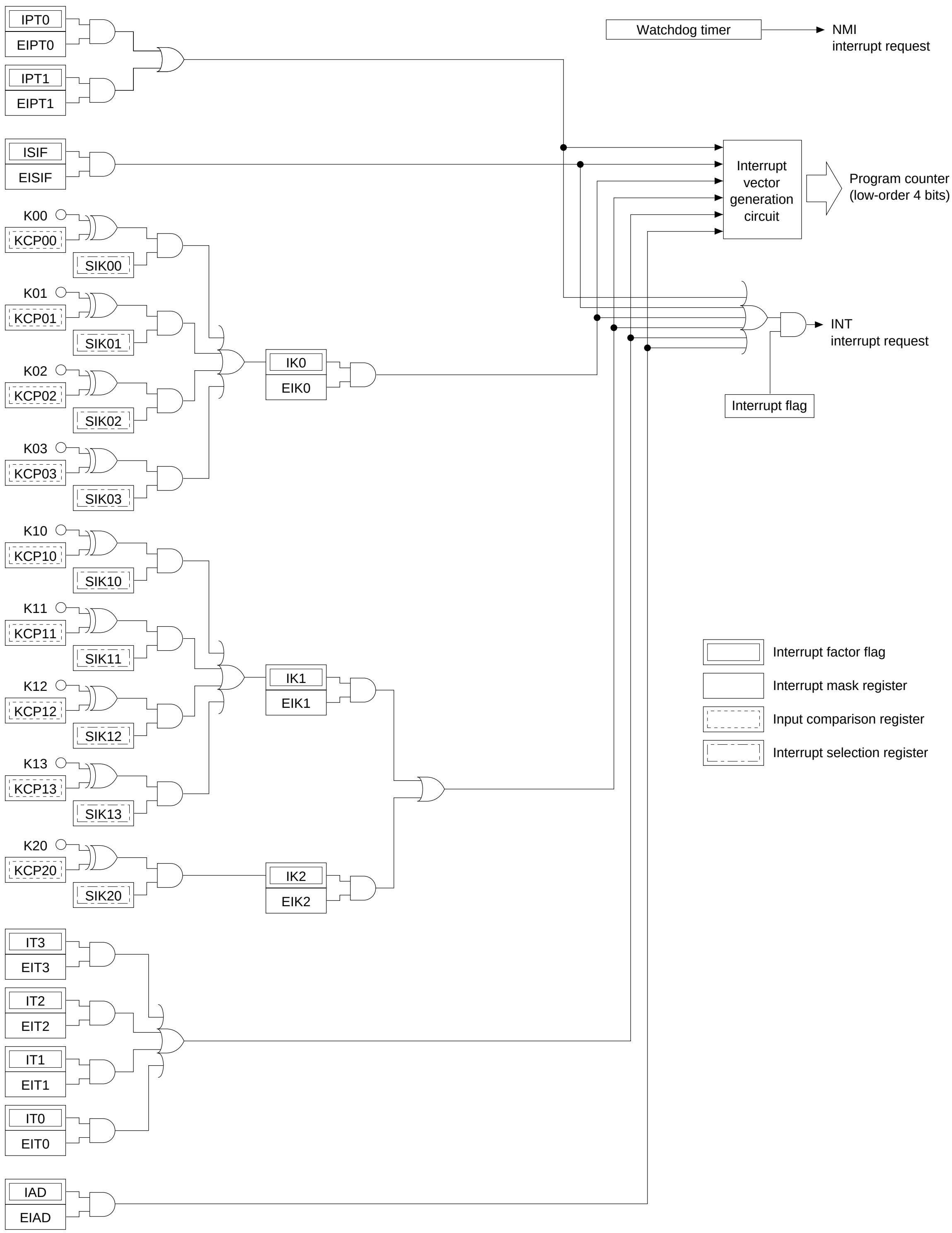


Fig. 4.14.1 Configuration of the interrupt circuit

4.14.1 Interrupt factor

Table 4.14.1.1 shows the factors for generating interrupt requests.

The interrupt flags are set to "1" depending on the corresponding interrupt factors.
The CPU operation is interrupted when an interrupt factor flag is set to "1" if the following conditions are established.

- The corresponding mask register is "1" (enabled)
- The interrupt flag is "1" (EI)

The interrupt factor flag is reset to "0" when "1" is written.
At initial reset, the interrupt factor flags are reset to "0".

∗ Since the watchdog timer's interrupt is NMI, the interrupt is generated regardless of the setting above, and no interrupt factor flag is provided.

Table 4.14.1.1 Interrupt factors

Interrupt factor	Interrupt factor flag	
Programmable timer 1 (counter = 0)	IPT1	(FFF2H•D1)
Programmable timer 0 (counter = 0)	IPT0	(FFF2H•D0)
Serial interface (8-bit data input/output completion)	ISIF	(FFF3H•D0)
K00–K03 input (falling edge or rising edge)	IK0	(FFF4H•D0)
K10–K13 input (falling edge or rising edge)	IK1	(FFF5H•D0)
K20 input (falling edge or rising edge)	IK2	(FFF5H•D1)
Clock timer 1 Hz (falling edge)	IT3	(FFF6H•D3)
Clock timer 2 Hz (falling edge)	IT2	(FFF6H•D2)
Clock timer 8 Hz (falling edge)	IT1	(FFF6H•D1)
Clock timer 16 Hz (falling edge)	IT0	(FFF6H•D0)
A/D converter	IAD	(FFF7H•D0)

Note: After an interrupt occurs, the same interrupt will occur again if the interrupt enabled state (I flag = "1") is set or the RETI instruction is executed unless the interrupt factor flag is reset. Therefore, be sure to reset (write "1" to) the interrupt factor flag in the interrupt service routine before shifting to the interrupt enabled state.

4.14.2 Interrupt mask

The interrupt factor flags can be masked by the corresponding interrupt mask registers.
The interrupt mask registers are read / write registers. They are enabled (interrupt authorized) when "1" is written to them, and masked (interrupt inhibited) when "0" is written to them.
At initial reset, the interrupt mask register is set to "0".
Table 4.14.2.1 shows the correspondence between interrupt mask registers and interrupt factor flags.

Table 4.14.2.1 Interrupt mask registers and interrupt factor flags

Interrupt mask register		Interrupt factor flag	
EIPT1	(FFE2H•D1)	IPT1	(FFF2H•D1)
EIPT0	(FFE2H•D0)	IPT0	(FFF2H•D0)
EISIF	(FFE3H•D0)	ISIF	(FFF3H•D0)
EIK0	(FFE4H•D0)	IK0	(FFF4H•D0)
EIK1	(FFE5H•D0)	IK1	(FFF5H•D0)
EIK2	(FFE5H•D1)	IK2	(FFF5H•D1)
EIT3	(FFE 6H•D3)	IT3	(FFF6H•D3)
EIT2	(FFE6H•D2)	IT2	(FFF6H•D2)
EIT1	(FFE6H•D1)	IT1	(FFF6H•D1)
EIT0	(FFE6H•D0)	IT0	(FFF6H•D0)
EIAD	(FFE7H•D0)	IAD	(FFF7H•D0)

4.14.3 Interrupt vector

When an interrupt request is input to the CPU, the CPU begins interrupt processing. After the program being executed is terminated, the interrupt processing is executed in the following order.

1 The content of the flag register is evacuated, then the I flag is reset.

2 The address data (value of program counter) of the program to be executed next is saved in the stack area (RAM).

3 The interrupt request causes the value of the interrupt vector (0100H–010EH) to be set in the program counter.

4 The program at the specified address is executed (execution of interrupt processing routine by software).

Table 4.14.3.1 shows the correspondence of interrupt requests and interrupt vectors.

Table 4.14.3.1 Interrupt request and interrupt vectors

Interrupt vector	Interrupt factor	Priority
0100H	Watchdog timer	High
0104H	Programmable timer	↑
0106H	Serial interface	
0108H	K00–K03 input	
010AH	K10–K13 input, K20 input	
010CH	Clock timer	↓
010EH	A/D converter	Low

The four low-order bits of the program counter are indirectly addressed through the interrupt request.

4.14.4 I/O memory of interrupt

Tables 4.14.4.1(a) and (b) show the I/O addresses and the control bits for controlling interrupts.

Table 4.14.4.1(a) Control bits of interrupt (1)

Address	Register D3	Register D2	Register D1	Register D0	Name	Init *1	1	0	Comment
FF20H	SIK03	SIK02	SIK01	SIK00	SIK03	0	Enable	Disable	K00–K03 interrupt selection register
					SIK02	0	Enable	Disable	
	R/W				SIK01	0	Enable	Disable	
					SIK00	0	Enable	Disable	
FF22H	KCP03	KCP02	KCP01	KCP00	KCP03	1	↓	↑	K00–K03 input comparison register
					KCP02	1	↓	↑	
	R/W				KCP01	1	↓	↑	
					KCP00	1	↓	↑	
FF24H	SIK13	SIK12	SIK11	SIK10	SIK13	0	Enable	Disable	K10–K13 interrupt selection register
					SIK12	0	Enable	Disable	
	R/W				SIK11	0	Enable	Disable	
					SIK10	0	Enable	Disable	
FF26H	KCP13	KCP12	KCP11	KCP10	KCP13	1	↓	↑	K10–K13 input comparison register
					KCP12	1	↓	↑	
	R/W				KCP11	1	↓	↑	
					KCP10	1	↓	↑	
FF28H	0	0	0	SIK20	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R			R/W	0 *3	– *2			Unused
					SIK20	0	Enable	Disable	K20 interrupt selection register
FF2AH	0	0	0	KCP20	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R			R/W	0 *3	– *2			Unused
					KCP20	1	↓	↑	K20 input comparison register
FFE2H	0	0	EIPT1	EIPT0	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R		R/W		EIPT1	0	Enable	Mask	Interrupt mask register (Programmable timer 1)
					EIPT0	0	Enable	Mask	Interrupt mask register (Programmable timer 0)
FFE3H	0	0	0	EISIF	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R			R/W	0 *3	– *2			Unused
					EISIF	0	Enable	Mask	Interrupt mask register (Serial I/F)
FFE4H	0	0	0	EIK0	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R			R/W	0 *3	– *2			Unused
					EIK0	0	Enable	Mask	Interrupt mask register (K00–K03)
FFE5H	0	0	EIK2	EIK1	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R		R/W		EIK2	0	Enable	Mask	Interrupt mask register (K20)
					EIK1	0	Enable	Mask	Interrupt mask register (K10–K13)
FFE6H	EIT3	EIT2	EIT1	EIT0	EIT3	0	Enable	Mask	Interrupt mask register (Clock timer 1 Hz)
					EIT2	0	Enable	Mask	Interrupt mask register (Clock timer 2 Hz)
	R/W				EIT1	0	Enable	Mask	Interrupt mask register (Clock timer 8 Hz)
					EIT0	0	Enable	Mask	Interrupt mask register (Clock timer 16 Hz)
FFE7H	0	0	0	EIAD	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R			R/W	0 *3	– *2			Unused
					EIAD	0	Enable	Mask	Interrupt mask register (A/D converter)

*1 Initial value at initial reset
*2 Not set in the circuit
*3 Constantly "0" when being read

Table 4.14.4.1(b) Control bits of interrupt (2)

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
FFF2H	0	0	IPT1	IPT0	0 *3	– *2	(R)	(R)	Unused
					0 *3	– *2	Yes	No	Unused
	R		R/W		IPT1	0	(W)	(W)	Interrupt factor flag (Programmable timer 1)
					IPT0	0	Reset	Invalid	Interrupt factor flag (Programmable timer 0)
FFF3H	0	0	0	ISIF	0 *3	– *2	(R)	(R)	Unused
					0 *3	– *2	Yes	No	Unused
	R			R/W	0 *3	– *2	(W)	(W)	Unused
					ISIF	0	Reset	Invalid	Interrupt factor flag (Serial I/F)
FFF4H	0	0	0	IK0	0 *3	– *2	(R)	(R)	Unused
					0 *3	– *2	Yes	No	Unused
	R			R/W	0 *3	– *2	(W)	(W)	Unused
					IK0	0	Reset	Invalid	Interrupt factor flag (K00–K03)
FFF5H	0	0	IK2	IK1	0 *3	– *2	(R)	(R)	Unused
					0 *3	– *2	Yes	No	Unused
	R		R/W		IK2	0	(W)	(W)	Interrupt factor flag (K20)
					IK1	0	Reset	Invalid	Interrupt factor flag (K10–K13)
FFF6H	IT3	IT2	IT1	IT0	IT3	0	(R)	(R)	Interrupt factor flag (Clock timer 1 Hz)
					IT2	0	Yes	No	Interrupt factor flag (Clock timer 2 Hz)
	R/W				IT1	0	(W)	(W)	Interrupt factor flag (Clock timer 8 Hz)
					IT0	0	Reset	Invalid	Interrupt factor flag (Clock timer 16 Hz)
FFF7H	0	0	0	IAD	0 *3	– *2	(R)	(R)	Unused
					0 *3	– *2	Yes	No	Unused
	R			R/W	0 *3	– *2	(W)	(W)	Unused
					IAD	0	Reset	Invalid	Interrupt factor flag (A/D converter)

*1 Initial value at initial reset
*2 Not set in the circuit
*3 Constantly "0" when being read

EIPT1, EIPT0: Interrupt mask registers (FFE2H•D1, D0)
IPT1, IPT0: Interrupt factor flags (FFF2H•D1, D0)
Refer to Section 4.10, "Programmable Timer".

EISIF: Interrupt mask register (FFE3H•D0)
ISIF: Interrupt factor flag (FFF3H•D0)
Refer to Section 4.11, "Serial Interface".

KCP03–KCP00, KCP13–KCP10, KCP20: Input comparison registers (FF22H, FF26H, FF2AH•D0)
SIK03–SIK00, SIK13–SIK10, SIK20: Interrupt selection registers (FF20H, FF24H, FF28H•D0)
EIK0, EIK1, EIK2: Interrupt mask registers (FFE4H•D0, FFE5H•D0, FFE5H•D1)
IK0, IK1, IK2: Interrupt factor flags (FFF4H•D0, FFF5H•D0, FFF5H•D1)
Refer to Section 4.5, "Input Ports".

EIT3–EIT0: Interrupt mask registers (FFE6H)
IT3–IT0: Interrupt factor flags (FFF6H)
Refer to Section 4.8, "Clock Timer".

EIAD: Interrupt mask register (FFE7H•D0)
IAD: Interrupt factor flag (FFF7H•D0)
Refer to Section 4.9, "A/D Converter".

4.14.5 Programming notes

(1) The interrupt factor flags are set when the interrupt condition is established, even if the interrupt mask registers are set to "0".

(2) After an interrupt occurs, the same interrupt will occur again if the interrupt enabled state (I flag = "1") is set or the RETI instruction is executed unless the interrupt factor flag is reset. Therefore, be sure to reset (write "1" to) the interrupt factor flag in the interrupt service routine before shifting to the interrupt enabled state.

(3) After an initial reset, all the interrupts including NMI are masked until both the stack pointers SP1 and SP2 are set with the software. Be sure to set the SP1 and SP2 in the initialize routine.
Further, when re-setting the stack pointer, the SP1 and SP2 must be set as a pair. When one of them is set, all the interrupts including NMI are masked and interrupts cannot be accepted until the other one is set.

CHAPTER 5 SUMMARY OF NOTES

5.1 Notes for Low Current Consumption

The E0C63158 contains control registers for each of the circuits so that current consumption can be reduced.
These control registers reduce the current consumption through programs that operate the circuits at the minimum levels.
The following lists the circuits that can control operation and their control registers. Refer to these when programming.

Table 5.1.1 Circuits and control registers

Circuit (and item)	Control register
CPU	HALT instruction
CPU operating frequency	CLKCHG, OSCC
Oscillation system voltage regulator	VDC
Voltage booster circuit	DBON, VDSEL, VADSEL
SVD circuit	SVDON

Refer to Chapter 7, "Electrical Characteristics" for current consumption.

Below are the circuit statuses at initial reset.

CPU: Operating status

CPU operating frequency: Low speed side (CLKCHG = "0")
OSC3 oscillation circuit is in OFF status (OSCC = "0")

Oscillation system voltage regulator: Low speed side 1.3 V (VDC = "0")

Supply voltage booster: Voltage regulator is driven with V_{DD}, Normal mode
(DBON = "0", VDSEL = "0", VADSEL = "0")

SVD circuit: OFF status (SVDON = "0")

5.2 Summary of Notes by Function

Here, the cautionary notes are summed up by function category. Keep these notes well in mind when programming.

Memory and stack

(1) Memory is not implemented in unused areas within the memory map. Further, some non-implementation areas and unused (access prohibition) areas exist in the peripheral I/O area. If the program that accesses these areas is generated, its operation cannot be guaranteed. Refer to the I/O memory maps shown in Tables 4.1.1 (a)–(f) for the peripheral I/O area.

(2) Part of the RAM area is used as a stack area for subroutine call and register evacuation, so pay attention not to overlap the data area and stack area.

(3) The E0C63000 core CPU handles the stack using the stack pointer for 4-bit data (SP2) and the stack pointer for 16-bit data (SP1).
16-bit data are accessed in stack handling by SP1, therefore, this stack area should be allocated to the area where 4-bit/16-bit access is possible (0100H to 01FFH). The stack pointers SP1 and SP2 change cyclically within their respective range: the range of SP1 is 0000H to 03FFH and the range of SP2 is 0000H to 00FFH. Therefore, pay attention to the SP1 value because it may be set to 0200H or more exceeding the 4-bit/16-bit accessible range in the E0C63158 or it may be set to 00FFH or less. Memory accesses except for stack operations by SP1 are 4-bit data access.
After initial reset, all the interrupts including NMI are masked until both the stack pointers SP1 and SP2 are set by software. Further, if either SP1 or SP2 is re-set when both are set already, the interrupts including NMI are masked again until the other is re-set. Therefore, the settings of SP1 and SP2 must be done as a pair.

Power supply and operating mode

(1) When driving the E0C63158 with a 0.9–1.35 V power supply voltage, software control is necessary. Set the oscillation system voltage regulator to the V_{C2} mode. When 1.35 V or more power supply voltage is used, do not set the oscillation system voltage regulator into the V_{C2} mode.

(2) When using the A/D converter with a 0.9–1.6 V power supply voltage, software control is necessary. Set the A/D converter voltage circuit to the V_{C2} mode. When 1.6 V or more power supply voltage is used, do not set the A/D converter circuit into the V_{C2} mode.

(3) If the power supply voltage is out of the specified voltage range for an operating mode, do not switch to the operating mode. It may cause malfunction or increase current consumption.

(4) When switching from the normal mode to the V_{C2} mode, the VDSEL and/or VADSEL registers should be set to "1" after taking a 100 msec or longer interval for the V_{C2} to stabilize from switching the DBON register to "1".

(5) When switching from the V_{C2} mode to the normal mode, use separate instructions to switch the mode (VDSEL = "0" or VADSEL = "0") and turn the voltage booster OFF (DBON = "0"). Simultaneous processing with a single instruction may cause malfunction.

(6) The OSC3 oscillation circuit can operate only in the normal mode with a power supply voltage from 2.2 V to 3.6 V.

Watchdog timer

(1) When the watchdog timer is being used, the software must reset it within 3-second cycles.

(2) Because the watchdog timer is set in operation state by initial reset, set the watchdog timer to disabled state (not used) before generating an interrupt (NMI) if it is not used.

Oscillation circuit

(1) When switching the CPU system clock from OSC1 to OSC3, first set V_{D1}. After that maintain 2.5 msec or more, and then turn the OSC3 oscillation ON.
When switching from OSC3 to OSC1, set V_{D1} after switching to OSC1 and turning the OSC3 oscillation OFF. However, when the CR oscillation circuit has been selected as the OSC1 oscillation circuit, it is not necessary to set V_{D1}.

(2) It takes at least 5 msec from the time the OSC3 oscillation circuit goes ON until the oscillation stabilizes. Consequently, when switching the CPU operation clock from OSC1 to OSC3, do this after a minimum of 5 msec have elapsed since the OSC3 oscillation went ON.
Further, the oscillation stabilization time varies depending on the external oscillator characteristics and conditions of use, so allow ample margin when setting the wait time.

(3) When switching the clock form OSC3 to OSC1, use a separate instruction for switching the OSC3 oscillation OFF. An error in the CPU operation can result if this processing is performed at the same time by the one instruction.

(4) Since the V_{D1} voltage value is fixed at 2.1 V when CR oscillation is selected for the OSC1 oscillation circuit by mask option and the OSC3 oscillation circuit (CR or ceramic oscillation) is also used, it is not necessary to switch V_{D1} by software. When the OSC3 oscillation circuit is not used, the OSC1 oscillation circuit can operate with 1.3 V of V_{D1} even if CR oscillation is selected.

Input port

(1) When input ports are changed from low to high by pull-up resistors, the rise of the waveform is delayed on account of the time constant of the pull-up resistor and input gate capacitance. Hence, when fetching input ports, set an appropriate waiting time.
Particular care needs to be taken of the key scan during key matrix configuration.
Make this waiting time the amount of time or more calculated by the following expression.
$10 \times C \times R$
C: terminal capacitance 5 pF + parasitic capacitance ? pF
R: pull-up resistance 300 kΩ

(2) The K13 terminal functions as the clock input terminal for the programmable timer, and the input signal is shared with the input port and the programmable timer. Therefore, when the K13 terminal is set to the clock input terminal for the programmable timer, take care of the interrupt setting.

Output port

(1) When using the output port (R02, R03) as the special output port, fix the data register (R02, R03) at "1" and the high impedance control register (R02HIZ, R03HIZ) at "0" (data output).
Be aware that the output terminal is fixed at a low (V_{SS}) level the same as the DC output if "0" is written to the R02 and R03 registers when the special output has been selected.
Be aware that the output terminal shifts into high impedance status when "1" is written to the high impedance control register (R02HIZ, R03HIZ).

(2) A hazard may occur when the FOUT signal and the TOUT signal are turned ON and OFF.

(3) When f_{OSC3} is selected for the FOUT signal frequency, it is necessary to control the OSC3 oscillation circuit before output.
Refer to Section 4.4, "Oscillation Circuit", for the control and notes.

I/O port

When in the input mode, I/O ports are changed from low to high by pull-up resistor, the rise of the waveform is delayed on account of the time constant of the pull-up resistor and input gate capacitance. Hence, when fetching input ports, set an appropriate wait time.
Particular care needs to be taken of the key scan during key matrix configuration.
Make this waiting time the amount of time or more calculated by the following expression.
$10 \times C \times R$
C: terminal capacitance 5 pF + parasitic capacitance ? pF
R: pull-up resistance 300 kΩ

Clock timer

(1) Be sure to read timer data in the order of low-order data (TM0–TM3) then high-order data (TM4–TM7).

(2) When the CR oscillation circuit is selected as the OSC1 oscillation circuit by mask option, the frequencies and times differ from the values described in this section because the oscillation frequency will be 60 kHz (Typ.). Therefore, the clock timer can not be used for the clock function.

A/D converter

(1) When supply voltage is 1.6 V or less, it is necessary to set the A/D converter circuit into the V_{C2} mode by writting "1" to VADSEL register befor starting A/D conversion.

(2) The A/D converter can operate by inputting the clock from the clock selector. Therefore, it is necessary to select the clock source and to turn the clock output on before starting A/D conversion. Furthermore, it is also necessary that the OSC3 oscillation circuit is operating when using the OSC3 clock.

(3) When using the OSC3 clock as the A/D conversion clock, do not stop the OSC3 oscillation circuit during A/D conversion. If the OSC3 oscillation circuit stops, correct A/D conversion result cannot be obtained.

(4) The input clock and analog input terminals should be set when the A/D converter stops. Changing these settings in the A/D converter operation may cause errors.

(5) To prevent malfunction, do not start A/D conversion (writing "1" to the ADRUN register) when the A/D conversion clock is not being output from the clock selector, and do not turn the clock off during A/D conversion.

(6) If the CHS register selects an input channel which is not included in the analog input terminals set by the PAD register (the PAD register can select several terminals simultaneously), the A/D conversion does not result in a correct converted value.

(7) During A/D conversion, do not operate the P4n terminals which are not used for analog inputs of the A/D converter (for input/output of digital signals). It affects the A/D conversion precision.

(8) Be aware that the maximum A/D clock frequency for the A/D converter is limited to 1 MHz when OSC3 is used as the clock source.

Programmable timer

(1) When reading counter data, be sure to read the low-order 4 bits (PTD00–PTD03, PTD10–PTD13) first. Furthermore, the high-order 4 bits (PTD04–PTD07, PTD14–PTD17) should be read within 0.73 msec of reading the low-order 4 bits (PTD00–PTD03, PTD10–PTD13).
For the 16 bit × 1 mode, be sure to read as following sequence:
(PTD00–PTD03) → (PTD04–PTD07) → (PTD10–PTD13) → (PTD14–PTD17)
The read sequence time should be within 1.46 msec.

(2) The programmable timer actually enters RUN/STOP status in synchronization with the falling edge of the input clock after writing to the PTRUN0/PTRUN1 register. Consequently, when "0" is written to the PTRUN0/PTRUN1 register, the timer enters STOP status at the point where the counter is decremented (-1). The PTRUN0/PTRUN1 register maintains "1" for reading until the timer actually stops.
Figure 5.2.1 shows the timing chart for the RUN/STOP control.

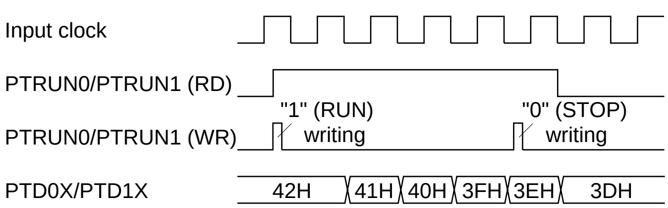


Fig. 5.2.1 Timing chart for RUN/STOP control

It is the same even in the event counter mode. Therefore, be aware that the counter does not enter RUN/STOP status if a clock is not input after setting the RUN/STOP control register (PTRUN0).

(3) Since the TOUT signal is generated asynchronously from the PTOUT register, a hazard within 1/2 cycle is generated when the signal is turned ON and OFF by setting the register.

(4) When the OSC3 oscillation clock is selected for the clock source, it is necessary to turn the OSC3 oscillation ON, prior to using the programmable timer. However the OSC3 oscillation circuit requires a time interval of several msec to several 10 msec from turning the circuit ON until the oscillation stabilizes. Therefore, allow an adequate interval from turning the OSC3 oscillation circuit ON to starting the programmable timer. Refer to Section 4.4, "Oscillation Circuit", for the control and notes of the OSC3 oscillation circuit.
At initial reset, the OSC3 oscillation circuit is set in the OFF state.

Serial interface

(1) Perform data writing/reading to the data registers SD0–SD7 only while the serial interface is not running (i.e., the synchronous clock is neither being input or output).

(2) As a trigger condition, it is required that data writing or reading on data registers SD0–SD7 be performed prior to writing "1" to SCTRG. (The internal circuit of the serial interface is initiated through data writing/reading on data registers SD0–SD7.) In addition, be sure to enable the serial interface with the ESIF register before setting the trigger.
Supply trigger only once every time the serial interface is placed in the RUN state. Refrain from performing trigger input multiple times, as leads to malfunctioning. Moreover, when the synchronous clock $\overline{\text{SCLK}}$ is external clock, start to input the external clock after the trigger.

(3) Setting of the input/output permutation (MSB first/LSB first) with the SDP register should be done before setting data to SD0–SD7.

(4) Be aware that the maximum clock frequency for the serial interface is limited to 1 MHz when OSC3 is used as the clock source of the programmable timer or in the slave mode.

Buzzer output circuit

Since it generates a buzzer signal that is out of synchronization with the BZON register, hazards may at times be produced when the signal goes ON/OFF due to the setting of the BZON register.

SVD circuit

(1) To obtain a stable detection result, the SVD circuit must be ON for at least l00 µsec. So, to obtain the SVD detection result, follow the programming sequence below.

1. Set SVDON to "1"
2. Maintain for 100 µsec minimum
3. Set SVDON to "0"
4. Read SVDDT

(2) The SVD circuit should normally be turned OFF because SVD operation increase current consumption.

Interrupt

(1) The interrupt factor flags are set when the interrupt condition is established, even if the interrupt mask registers are set to "0".

(2) After an interrupt occurs, the same interrupt will occur again if the interrupt enabled state (I flag = "1") is set or the RETI instruction is executed unless the interrupt factor flag is reset. Therefore, be sure to reset (write "1" to) the interrupt factor flag in the interrupt service routine before shifting to the interrupt enabled state.

(3) After an initial reset, all the interrupts including NMI are masked until both the stack pointers SP1 and SP2 are set with the software. Be sure to set the SP1 and SP2 in the initialize routine.
Further, when re-setting the stack pointer, the SP1 and SP2 must be set as a pair. When one of them is set, all the interrupts including NMI are masked and interrupts cannot be accepted until the other one is set.

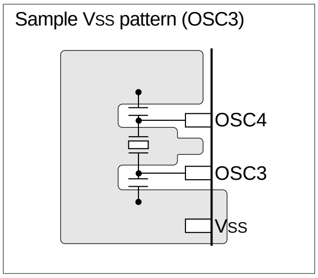
5.3 Precautions on Mounting

<Oscillation Circuit>

- Oscillation characteristics change depending on conditions (board pattern, components used, etc.). In particular, when a ceramic oscillator or crystal oscillator is used, use the oscillator manufacturer's recommended values for constants such as capacitance and resistance.
- Disturbances of the oscillation clock due to noise may cause a malfunction. Consider the following points to prevent this:

  (1) Components which are connected to the OSC1, OSC2, OSC3 and OSC4 terminals, such as oscillators, resistors and capacitors, should be connected in the shortest line.

  (2) As shown in the right hand figure, make a V_{SS} pattern as large as possible at circumscription of the OSC1, OSC2, OSC3 and OSC4 terminals and the components connected to these terminals. Furthermore, do not use this V_{SS} pattern for any purpose other than the oscillation system.



- In order to prevent unstable operation of the oscillation circuit due to current leak between OSC1/OSC3 and V_{DD}, please keep enough distance between OSC1/OSC3 and V_{DD} or other signals on the board pattern.

<Reset Circuit>

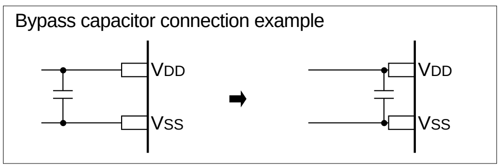
- The power-on reset signal which is input to the $\overline{RESET}$ terminal changes depending on conditions (power rise time, components used, board pattern, etc.).
  Decide the time constant of the capacitor and resistor after enough tests have been completed with the application product.
  When the built-in pull-up resistor is added to the $\overline{RESET}$ terminal by mask option, take into consideration dispersion of the resistance for setting the constant.
- In order to prevent any occurrences of unnecessary resetting caused by noise during operating, components such as capacitors and resistors should be connected to the $\overline{RESET}$ terminal in the shortest line.

<Power Supply Circuit>

- Sudden power supply variation due to noise may cause malfunction. Consider the following points to prevent this:

  (1) The power supply should be connected to the V_{DD}, V_{SS}, AV_{DD}, AV_{SS} and AV_{REF} terminal with patterns as short and large as possible.
  In particular, the power supply for AV_{DD}, AV_{SS} and AV_{REF} affects A/D conversion precision.

  (2) When connecting between the V_{DD} and V_{SS} terminals with a bypass capacitor, the terminals should be connected as short as possible.



  (3) Components which are connected to the V_{D1} and V_{C2} terminals, such as capacitors, should be connected in the shortest line.

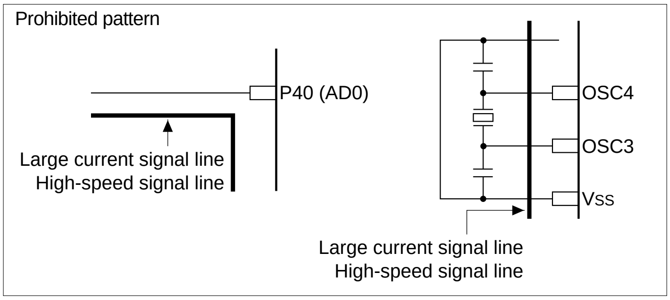
<A/D Converter>

- When the A/D converter is not used, the power supply terminals for the analog system should be connected as shown below.

  AVDD → VDD
  AVSS → VSS
  AVREF → VSS

<Arrangement of Signal Lines>

- In order to prevent generation of electromagnetic induction noise caused by mutual inductance, do not arrange a large current signal line near the circuits that are sensitive to noise such as the oscillation unit and analog input unit.
- When a signal line is parallel with a high-speed line in long distance or intersects a high-speed line, noise may generated by mutual interference between the signals and it may cause a malfunction. Do not arrange a high-speed signal line especially near circuits that are sensitive to noise such as the oscillation unit and analog input unit.



<Precautions for Visible Radiation (when bare chip is mounted)>

- Visible radiation causes semiconductor devices to change the electrical characteristics. It may cause this IC to malfunction. When developing products which use this IC, consider the following precautions to prevent malfunctions caused by visible radiations.

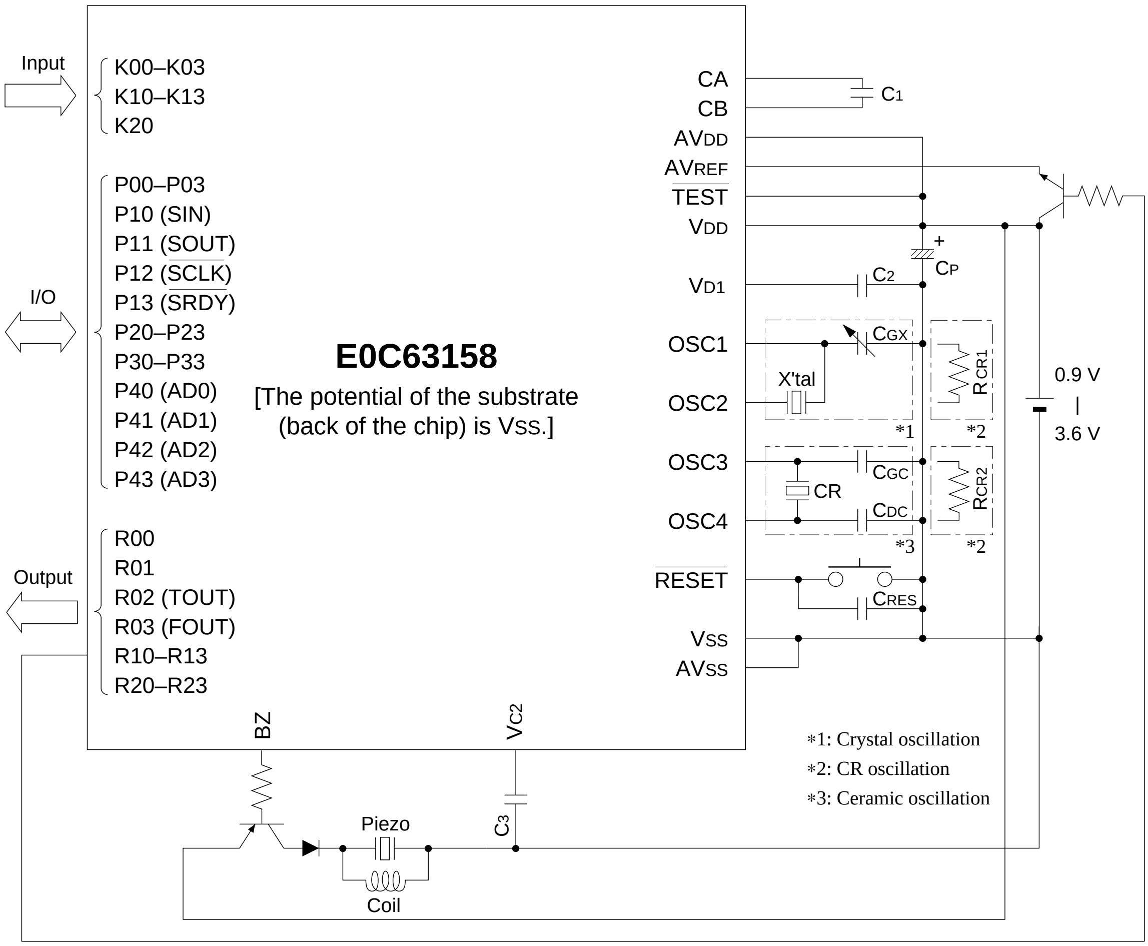
  (1) Design the product and implement the IC on the board so that it is shielded from visible radiation in actual use.

  (2) The inspection process of the product needs an environment that shields the IC from visible radiation.

  (3) As well as the face of the IC, shield the back and side too.

CHAPTER 6 BASIC EXTERNAL WIRING DIAGRAM

• When negative polarity is selected for buzzer output (mask option selection)



X'tal	Crystal oscillator	32.768 kHz, CI (Max.) = 34 kΩ
CGX	Trimmer capacitor	5–25 pF
RCR1	Resistor for OSC1 CR oscillation	1.5 MΩ (60 kHz)
CR	Ceramic oscillator	4 MHz (3.0 V)
CGC	Gate capacitor	100 pF
CDC	Drain capacitor	100 pF
RCR2	Resistor for OSC3 CR oscillation	40.2 kΩ (1.8 MHz)
C1–C3	Capacitor	0.2 µF
CP	Capacitor	3.3 µF
CRES	RESET terminal capacitor	0.1 µF

Note: The above table is simply an example, and is not guaranteed to work.

CHAPTER 7 ELECTRICAL CHARACTERISTICS

7.1 Absolute Maximum Rating

(V_{SS}=0V)

Item	Symbol	Rated value	Unit
Supply voltage	V_{DD}	-0.5 to 4.6	V
Input voltage (1)	V_I	-0.5 to V_{DD} + 0.3	V
Input voltage (2)	V_{IOSC}	-0.5 to V_{D1} + 0.3	V
Permissible total output current ∗1	ΣI_{VDD}	10	mA
Operating temperature	Topr	-20 to 70	°C
Storage temperature	Tstg	-65 to 150	°C
Soldering temperature / time	Tsol	260°C, 10sec (lead section)	–
Permissible dissipation ∗2	P_D	250	mW

∗1 The permissible total output current is the sum total of the current (average current) that simultaneously flows from the output pin (or is drawn in).

∗2 In case of plastic package (QFP12-48pin, QFP13-64pin).

7.2 Recommended Operating Conditions

(Ta=-20 to 70°C)

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Supply voltage	V_{DD}	V_{SS}=0V	Booster mode (OSC3 OFF)	0.9	1.1	1.35	V
			Normal mode (OSC3 OFF)	1.35	3.0	3.6	V
			Normal mode (OSC3 ON)	2.2	3.0	3.6	V
	AV_{DD}	AV_{SS}=0V		0.9	3.0	3.6	V
	AV_{REF}	$AV_{REF} \leq AV_{DD}$		0.9	3.0	3.6	V
Oscillation frequency	f_{OSC1}	Crystal oscillation		–	32.768	–	kHz
		CR oscillation		40	60	80	kHz
	f_{OSC3}	CR oscillation			1800		kHz
		Ceramic oscillation				4100	kHz

7.3 DC Characteristics

Unless otherwise specified:
V_{DD}=1.5V, V_{SS}=0V, f_{OSC1}=32.768kHz, Ta=25°C, V_{D1}/V_{C2} are internal voltage, C_1–C_3=0.2µF

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
High level input voltage (1)	V_{IH1}		K00–03, K10–13, K20, P00–03 P10–13, P20–23, P30–33, P40–43	0.8·V_{DD}		V_{DD}	V
High level input voltage (2)	V_{IH2}		$\overline{\text{RESET}}$, $\overline{\text{TEST}}$	0.9·V_{DD}		V_{DD}	V
Low level input voltage (1)	V_{IL1}		K00–03, K10–13, K20, P00–03 P10–13, P20–23, P30–33, P40–43	0		0.2·V_{DD}	V
Low level input voltage (2)	V_{IL2}		$\overline{\text{RESET}}$, $\overline{\text{TEST}}$	0		0.1·V_{DD}	V
High level input current	I_{IH}	V_{IH}=1.5V	K00–03, K10–13, K20, P00–03 P10–13, P20–23, P30–33, P40–43 $\overline{\text{RESET}}$, $\overline{\text{TEST}}$	0		0.5	µA
Low level input current (1)	I_{IL1}	V_{IL1}=V_{SS} No Pull-up	K00–03, K10–13, K20, P00–03 P10–13, P20–23, P30–33, P40–43 $\overline{\text{RESET}}$, $\overline{\text{TEST}}$	-0.5		0	µA
Low level input current (2)	I_{IL2}	V_{IL2}=V_{SS} With Pull-up	K00–03, K10–13, K20, P00–03 P10–13, P20–23, P30–33, P40–43 $\overline{\text{RESET}}$, $\overline{\text{TEST}}$	-7.5	-5	-2.5	µA
High level output current (1)	I_{OH1}	V_{OH1}=0.9·V_{DD}	R00–03, R10–13, R20–23, P00–03 P10–13, P20–23, P30–33, P40–43			-0.3	mA
High level output current (2)	I_{OH2}	V_{OH2}=0.9·V_{DD}	BZ			-0.3	mA
Low level output current (1)	I_{OL1}	V_{OL1}=0.1·V_{DD}	R00–03, R10–13, R20–23, P00–03 P10–13, P20–23, P30–33, P40–43	0.5			mA
Low level output current (2)	I_{OL2}	V_{OL2}=0.1·V_{DD}	BZ	0.5			mA

Unless otherwise specified:
V_{DD}=3.0V, V_{SS}=0V, f_{OSC1}=32.768kHz, Ta=25°C, V_{D1}/V_{C2} are internal voltage, C_1–C_3=0.2µF

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
High level input voltage (1)	V_{IH1}		K00–03, K10–13, K20, P00–03 P10–13, P20–23, P30–33, P40–43	0.8·V_{DD}		V_{DD}	V
High level input voltage (2)	V_{IH2}		$\overline{\text{RESET}}$, $\overline{\text{TEST}}$	0.9·V_{DD}		V_{DD}	V
Low level input voltage (1)	V_{IL1}		K00–03, K10–13, K20, P00–03 P10–13, P20–23, P30–33, P40–43	0		0.2·V_{DD}	V
Low level input voltage (2)	V_{IL2}		$\overline{\text{RESET}}$, $\overline{\text{TEST}}$	0		0.1·V_{DD}	V
High level input current	I_{IH}	V_{IH}=3.0V	K00–03, K10–13, K20, P00–03 P10–13, P20–23, P30–33, P40–43 $\overline{\text{RESET}}$, $\overline{\text{TEST}}$	0		0.5	µA
Low level input current (1)	I_{IL1}	V_{IL1}=V_{SS} No Pull-up	K00–03, K10–13, K20, P00–03 P10–13, P20–23, P30–33, P40–43 $\overline{\text{RESET}}$, $\overline{\text{TEST}}$	-0.5		0	µA
Low level input current (2)	I_{IL2}	V_{IL2}=V_{SS} With Pull-up	K00–03, K10–13, K20, P00–03 P10–13, P20–23, P30–33, P40–43 $\overline{\text{RESET}}$, $\overline{\text{TEST}}$	-15	-10	-5	µA
High level output current (1)	I_{OH1}	V_{OH1}=0.9·V_{DD}	R00–03, R10–13, R20–23, P00–03 P10–13, P20–23, P30–33, P40–43			-1.5	mA
High level output current (2)	I_{OH2}	V_{OH2}=0.9·V_{DD}	BZ			-1.5	mA
Low level output current (1)	I_{OL1}	V_{OL1}=0.1·V_{DD}	R00–03, R10–13, R20–23, P00–03 P10–13, P20–23, P30–33, P40–43	3			mA
Low level output current (2)	I_{OL2}	V_{OL2}=0.1·V_{DD}	BZ	3			mA

7.4 Analog Circuit Characteristics and Power Current Consumption

Unless otherwise specified:

V_{DD}=3.0V, V_{SS}=0V, f_{OSC1}=32.768kHz, C_G=25pF, Ta=25°C, V_{D1}/V_{C2} are internal voltage, C_1–C_3=0.2µF

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
SVD voltage	V_{SVD}	SVDS0–3="0"		0.95	1.05	1.15	V
		SVDS0–3="1"		1.02	1.10	1.18	
		SVDS0–3="2"		1.07	1.15	1.23	
		SVDS0–3="3"		1.12	1.20	1.28	
		SVDS0–3="4"		1.16	1.25	1.34	
		SVDS0–3="5"		1.21	1.30	1.39	
		SVDS0–3="6"		1.30	1.40	1.50	
		SVDS0–3="7"		1.49	1.60	1.71	
		SVDS0–3="8"		1.81	1.95	2.09	
		SVDS0–3="9"		1.86	2.00	2.14	
		SVDS0–3="10"		1.91	2.05	2.19	
		SVDS0–3="11"		1.95	2.10	2.25	
		SVDS0–3="12"		2.05	2.20	2.35	
		SVDS0–3="13"		2.14	2.30	2.46	
		SVDS0–3="14"		2.33	2.50	2.68	
		SVDS0–3="15"		2.42	2.60	2.78	
SVD circuit response time	t_{SVD}					100	µS
Current consumption	I_{OP}	During HALT Normal mode *1	32.768kHz		2	3	µA
		During HALT Booster mode (V_{DD}=1.2V) ∗1	32.768kHz		2.5	5	µA
		During execution Normal mode *1	32.768kHz (Crystal oscillation)		4	6	µA
			60kHz (CR oscillation)		15	30	µA
			1.8MHz (CR oscillation)		500	800	µA
			4MHz (Ceramic oscillation)		900	1200	µA
		During execution Booster mode (V_{DD}=1.2V) ∗1	32.768kHz (Crystal oscillation)		8	12	µA

∗1 The SVD circuit and the A/D converter are OFF. AV_{REF} is open.

A/D converter characteristic

Unless otherwise specified:

AV_{DD}=V_{DD}=0.9 to 3.6V, AV_{SS}=V_{SS}=0V, Ta=-25 to -75°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Resolution			8	8	8	bit
Error		2.2V≤V_{DD}≤2.7V Fconv=OSC3/2≤1MHz or OSC1	-3		3	LSB
		1.6V≤V_{DD}≤2.2V Fconv=OSC1	-3		3	LSB
		0.9V≤V_{DD}≤1.6V Fconv=OSC1, VADSEL=1	-3		3	LSB
Convertion time	t_{conv}	Fconv=OSC3/2=1MHz			21	µS
		Fconv=OSC1=32kHz			641	µS
Input voltage			AV_{SS}		AV_{REF}	V
Reference voltage	AV_{REF}		0.9		AV_{DD}	V
AV_{REF} resistance			15	20		kΩ

7.5 Oscillation Characteristics

The oscillation characteristics change depending on the conditions (components used, board pattern, etc.). Use the following characteristics as reference values.

OSC1 crystal oscillation circuit

Unless otherwise specified:
V_{DD}=3.0V, V_{SS}=0V, f_{OSC1}=32.768kHz, C_G=25pF, C_D=built-in, Ta=25°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start voltage	Vsta	t_{sta}≤3sec (V_{DD})	1.1			V
Oscillation stop voltage	Vstp	t_{stp}≤10sec (V_{DD}), Normal mode	1.1			V
		t_{stp}≤10sec (V_{DD}), Booster mode	0.9			V
Built-in capacitance (drain)	C_D	Including the parasitic capacitance inside the IC (in chip)		14		pF
Frequency/voltage deviation	∂f/∂V	V_{DD}=0.9 to 3.6V, with VDC switching			10	ppm
		V_{DD}=0.9 to 3.6V, without VDC switching			5	ppm
Frequency/IC deviation	∂f/∂IC		-10		10	ppm
Frequency adjustment range	∂f/∂C_G	C_G=5 to 25pF	25	30		ppm
Harmonic oscillation start voltage	V_{hho}	C_G=5pF (V_{DD})	3.6			V
Permitted leak resistance	R_{leak}	Between OSC1 and V_{DD}, V_{SS}	200			MΩ

OSC1 CR oscillation circuit

Unless otherwise specified:
V_{DD}=3.0V, V_{SS}=0V, R_{CR1}=1.5MΩ, Ta=25°C, VDC=1

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation frequency dispersion	f_{OSC1}		-30	60kHz	30	%
Oscillation start voltage	Vsta	Normal mode (V_{DD})	2.2			V
Oscillation start time	tsta	V_{DD}=2.2 to 3.6V			3	mS
Oscillation stop voltage	Vstp	Normal mode (V_{DD})	2.2			V

Unless otherwise specified:
V_{DD}=3.0V, V_{SS}=0V, R_{CR1}=1MΩ, Ta=25°C, VDC=0

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation frequency dispersion	f_{OSC1}		-30	80kHz	30	%
Oscillation start voltage	Vsta	Normal mode (V_{DD})	1.3			V
Oscillation start time	tsta	V_{DD}=1.3 to 3.6V			3	mS
Oscillation stop voltage	Vstp	Normal mode (V_{DD})	1.3			V

OSC3 ceramic oscillation circuit

Unless otherwise specified:
V_{DD}=3.0V, V_{SS}=0V, Ceramic oscillator: 4MHz, C_{GC}=C_{DC}=100pF, Ta=25°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start voltage	Vsta	Normal mode (V_{DD})	2.2			V
Oscillation start time	tsta	V_{DD}=2.2 to 3.6V			5	mS
Oscillation stop voltage	Vstp	Normal mode (V_{DD})	2.2			V

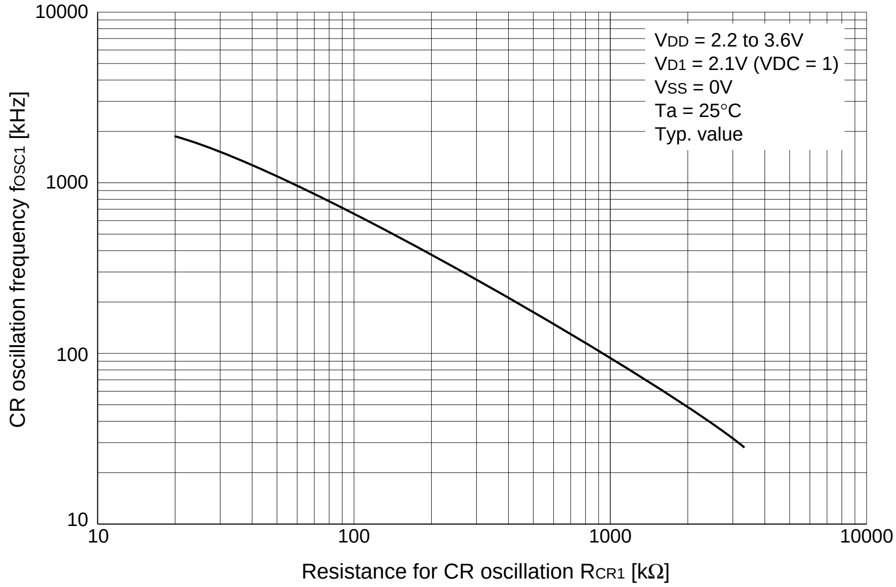
OSC3 CR oscillation circuit

Unless otherwise specified:
V_{DD}=3.0V, V_{SS}=0V, R_{CR2}=40.2kΩ, Ta=25°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation frequency dispersion	f_{OSC3}		-30	1.8MHz	30	%
Oscillation start voltage	Vsta	Normal mode (V_{DD})	2.2			V
Oscillation start time	tsta	V_{DD}=2.2 to 3.6V			3	mS
Oscillation stop voltage	Vstp	Normal mode (V_{DD})	2.2			V

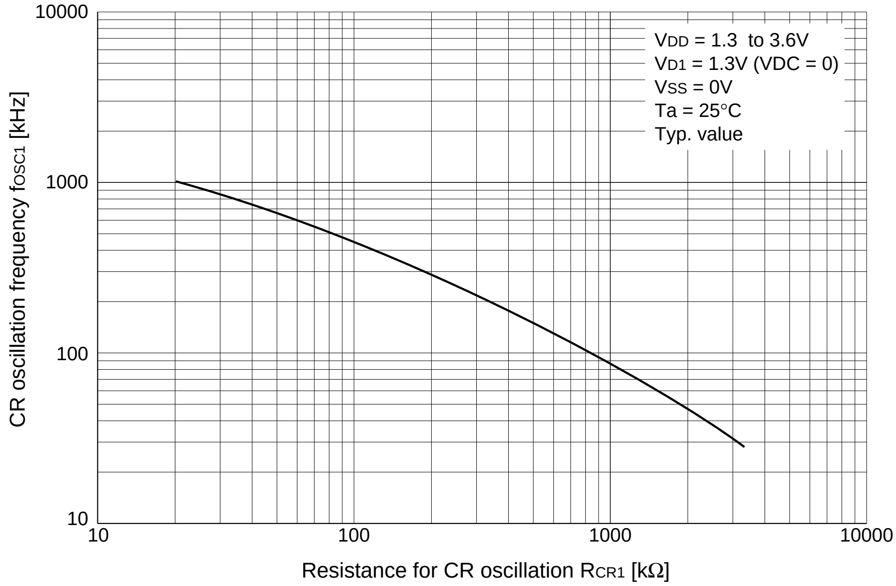
OSC1 CR oscillation frequency-resistance characteristic (VDC = 1)

The oscillation characteristics change depending on the conditions (components used, board pattern, etc.). Use the following characteristics as reference values and evaluate the characteristics on the actual product.



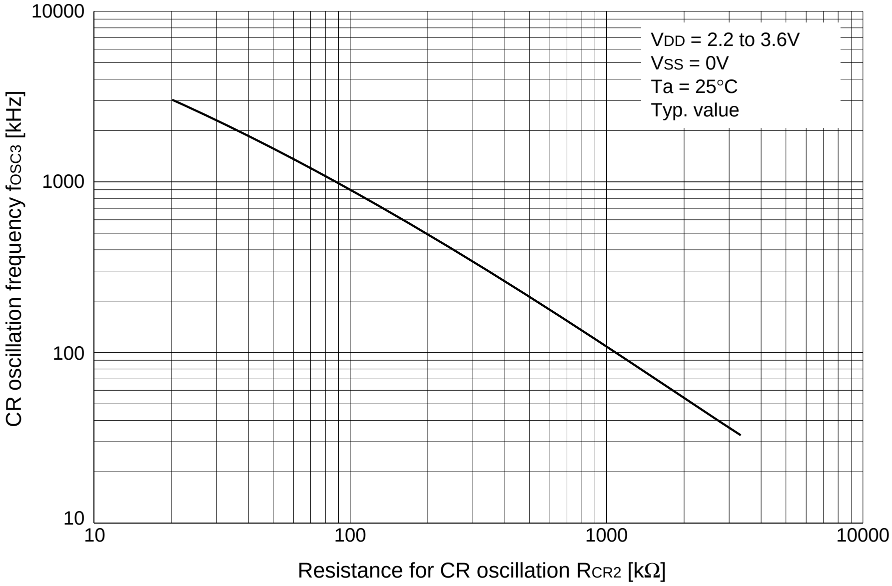
OSC1 CR oscillation frequency-resistance characteristic (VDC = 0)

The oscillation characteristics change depending on the conditions (components used, board pattern, etc.). Use the following characteristics as reference values and evaluate the characteristics on the actual product.



OSC3 CR oscillation frequency-resistance characteristic

The oscillation characteristics change depending on the conditions (components used, board pattern, etc.). Use the following characteristics as reference values and evaluate the characteristics on the actual product.



7.6 Serial Interface AC Characteristics

Clock synchronous master mode

• *During 32 kHz operation*

Condition: V_{DD}=3.0V, V_{SS}=0V, Ta=25°C, V_{IH1}=0.8V_{DD}, V_{IL1}=0.2V_{DD}, V_{OH}=0.8V_{DD}, V_{OL}=0.2V_{DD}

Item	Symbol	Min.	Typ.	Max.	Unit
Transmitting data output delay time	tsmd			5	µS
Receiving data input set-up time	tsms	10			µS
Receiving data input hold time	tsmh	5			µS

• *During 1 MHz operation*

Condition: V_{DD}=3.0V, V_{SS}=0V, Ta=25°C, V_{IH1}=0.8V_{DD}, V_{IL1}=0.2V_{DD}, V_{OH}=0.8V_{DD}, V_{OL}=0.2V_{DD}

Item	Symbol	Min.	Typ.	Max.	Unit
Transmitting data output delay time	tsmd			200	nS
Receiving data input set-up time	tsms	400			nS
Receiving data input hold time	tsmh	200			nS

Clock synchronous slave mode

• *During 32 kHz operation*

Condition: V_{DD}=3.0V, V_{SS}=0V, Ta=25°C, V_{IH1}=0.8V_{DD}, V_{IL1}=0.2V_{DD}, V_{OH}=0.8V_{DD}, V_{OL}=0.2V_{DD}

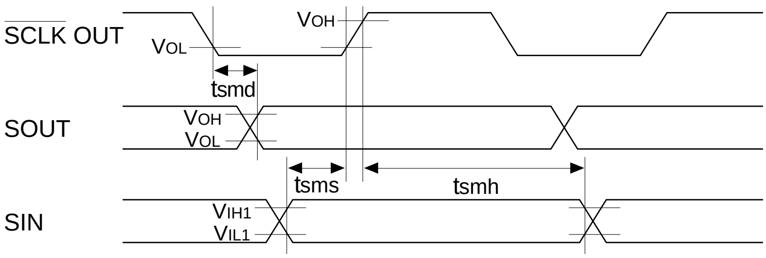
Item	Symbol	Min.	Typ.	Max.	Unit
Transmitting data output delay time	tssd			10	µS
Receiving data input set-up time	tsss	10			µS
Receiving data input hold time	tssh	5			µS

• *During 1 MHz operation*

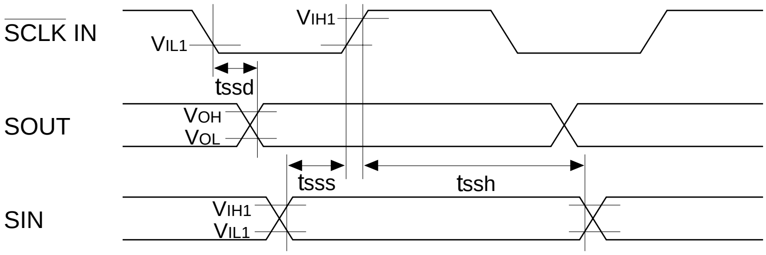
Condition: V_{DD}=3.0V, V_{SS}=0V, Ta=25°C, V_{IH1}=0.8V_{DD}, V_{IL1}=0.2V_{DD}, V_{OH}=0.8V_{DD}, V_{OL}=0.2V_{DD}

Item	Symbol	Min.	Typ.	Max.	Unit
Transmitting data output delay time	tssd			500	nS
Receiving data input set-up time	tsss	400			nS
Receiving data input hold time	tssh	200			nS

<Master mode>

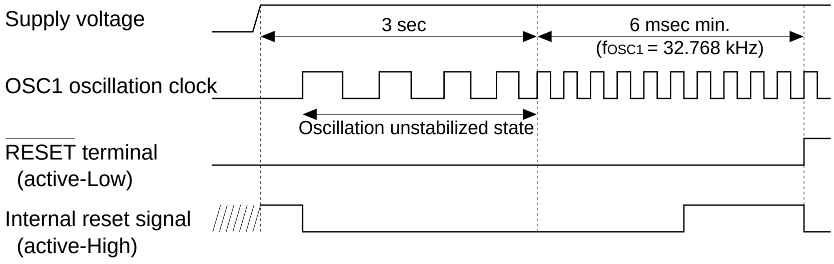


<Slave mode>

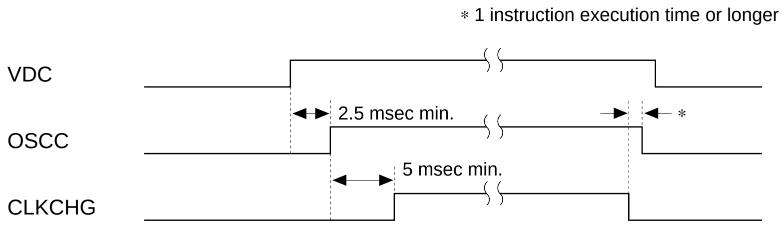


7.7 Timing Chart

Reset

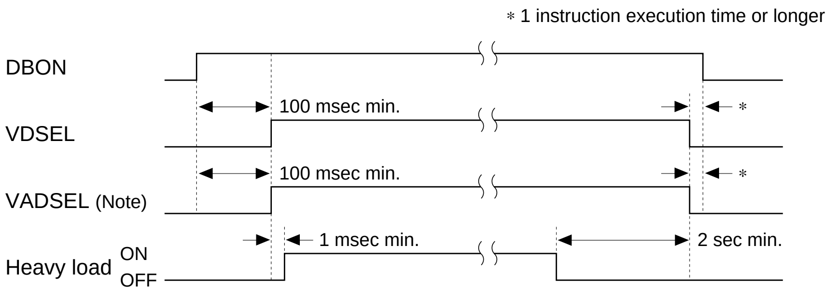


System clock switching



(Note) When the OSC1 oscillation circuit has been selected as the CR oscillation circuit, it is not necessary to set the VDC register.
Whether the VDC register value is "1" or "0" does not matter.

Supply voltage VC2 mode control during heavy load driving



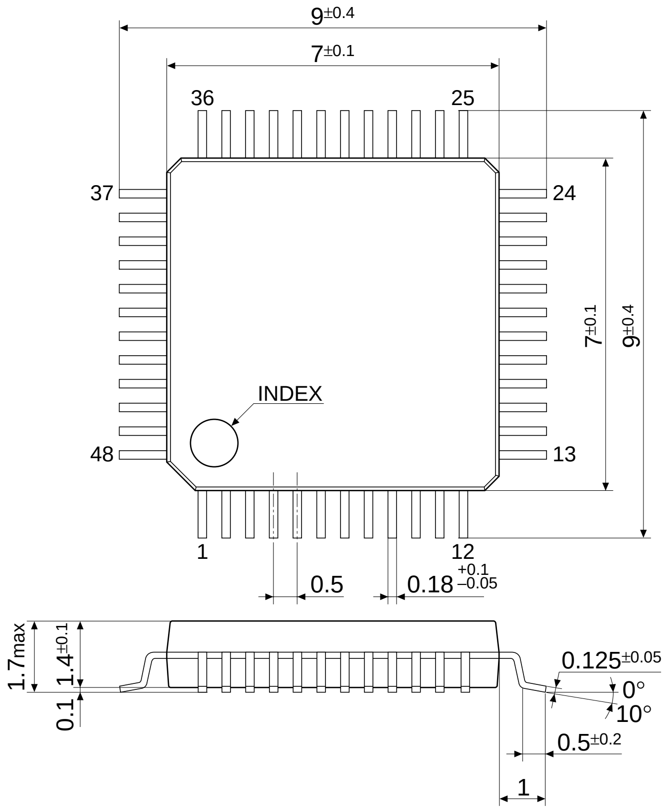
(Note) VADSEL is used only when it is required.

CHAPTER 8 PACKAGE

8.1 Plastic Package

QFP12-48pin

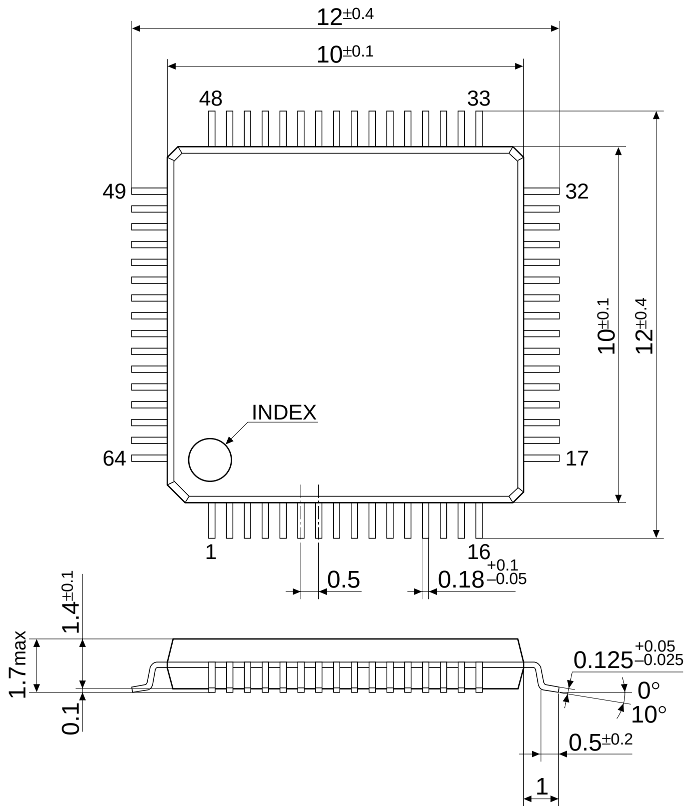
(Unit: mm)



The dimensions are subject to change without notice.

QFP13-64pin

(Unit: mm)

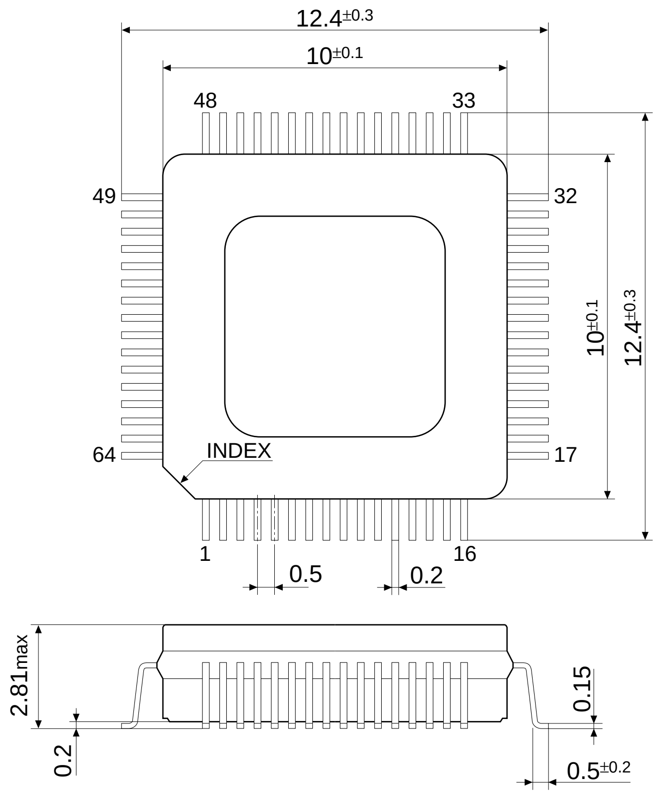


The dimensions are subject to change without notice.

8.2 Ceramic Package for Test Samples

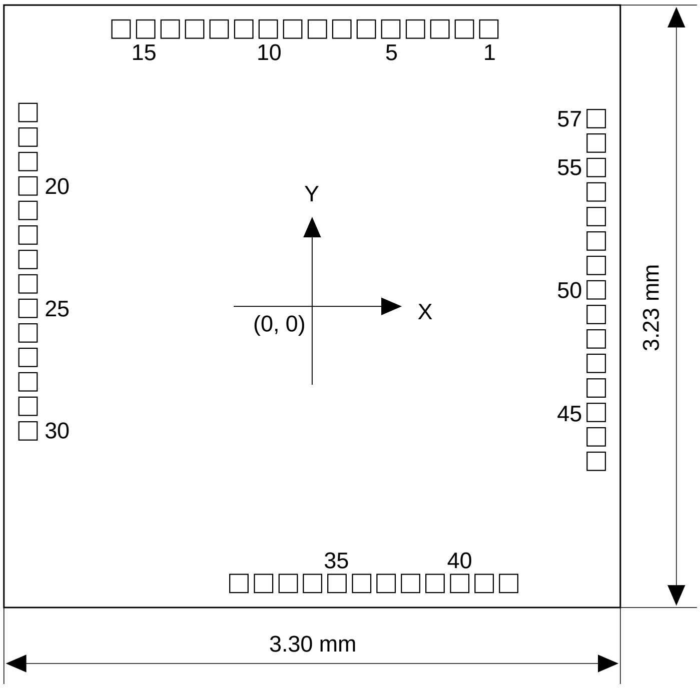
QFP13-64pin

(Unit: mm)



CHAPTER 9 PAD LAYOUT

9.1 Diagram of Pad Layout



Chip thickness: 400 µm
Pad opening: 98 µm

9.2 Pad Coordinates

Unit: µm

No.	Pad name	X	Y	No.	Pad name	X	Y	No.	Pad name	X	Y
1	P43	946	1486	20	P00	-1521	645	39	K11	658	-1486
2	P42	815	1486	21	R23	-1521	514	40	K12	790	-1486
3	P41	684	1486	22	R22	-1521	382	41	K13	921	-1486
4	P40	553	1486	23	R21	-1521	251	42	K20	1052	-1486
5	P33	421	1486	24	R20	-1521	120	43	VSS	1521	-831
6	P32	290	1486	25	R13	-1521	-11	44	OSC1	1521	-700
7	P31	159	1486	26	R12	-1521	-143	45	OSC2	1521	-569
8	P30	28	1486	27	R11	-1521	-274	46	VD1	1521	-438
9	P23	-104	1486	28	R10	-1521	-405	47	OSC3	1521	-306
10	P22	-235	1486	29	R03	-1521	-536	48	OSC4	1521	-175
11	P21	-366	1486	30	R02	-1521	-668	49	VDD	1521	-44
12	P20	-498	1486	31	R01	-392	-1486	50	$\overline{\text{RESET}}$	1521	88
13	P13	-629	1486	32	R00	-260	-1486	51	$\overline{\text{TEST}}$	1521	219
14	P12	-760	1486	33	BZ	-128	-1486	52	AVDD	1521	350
15	P11	-891	1486	34	K00	2	-1486	53	AVSS	1521	481
16	P10	-1023	1486	35	K01	133	-1486	54	AVREF	1521	613
17	P03	-1521	1039	36	K02	265	-1486	55	CB	1521	744
18	P02	-1521	907	37	K03	396	-1486	56	CA	1521	875
19	P01	-1521	776	38	K10	527	-1486	57	VC2	1521	1006

EPSON International Sales Operations

AMERICA

EPSON ELECTRONICS AMERICA, INC.

- HEADQUARTERS -
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Alpharetta, GA 30005, U.S.A.
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EUROPE

EPSON EUROPE ELECTRONICS GmbH

- HEADQUARTERS -
Riesstrasse 15
80992 Muenchen, GERMANY
Phone: +49-(0)89-14005-0 Fax: +49-(0)89-14005-110

- GERMANY -
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Phone: +49-(0)217-15045-0 Fax: +49-(0)217-15045-10

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ASIA

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EPSON HONG KONG LTD.
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- CHINA -
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- SINGAPORE -
EPSON SINGAPORE PTE., LTD.
No. 1 Temasek Avenue, #36-00
Millenia Tower, SINGAPORE 039192
Phone: +65-337-7911 Fax: +65-334-2716

- KOREA -
SEIKO EPSON CORPORATION
KOREA OFFICE
50F, KLI 63 Bldg., 60 Yoido-Dong
Youngdeungpo-Ku, Seoul, 150-010, KOREA
Phone: 02-784-6027 Fax: 02-767-3677

- JAPAN -
SEIKO EPSON CORPORATION
ELECTRONIC DEVICES MARKETING DIVISION

Electronic Device Marketing Department
IC Marketing & Engineering Group
421-8, Hino, Hino-shi, Tokyo 191-8501, JAPAN
Phone: +81-(0)42-587-5816 Fax: +81-(0)42-587-5624

ED International Marketing Department I
(Europe & U.S.A.)
421-8, Hino, Hino-shi, Tokyo 191-8501, JAPAN
Phone: +81-(0)42-587-5812 Fax: +81-(0)42-587-5564

ED International Marketing Department II
(Asia)
421-8, Hino, Hino-shi, Tokyo 191-8501, JAPAN
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