MF861-03

EPSON

CMOS 4-BIT SINGLE CHIP MICROCOMPUTER

E0C63B08 TECHNICAL MANUAL

E0C63B08 Technical Hardware

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CHAPTER 1 OUTLINE

The E0C63B08 is a microcomputer which has a high-performance 4-bit CPU E0C63000 as the core CPU, ROM (8,192 words × 13 bits), RAM (1,024 words × 4 bits), serial interface, watchdog timer, programmable timer, time base counters (2 systems), SVD circuit, a dot-matrix LCD driver that can drive a maximum 32 segments × 4 commons and a gate array that consists of 11,000 gates built-in. The E0C63B08 features low voltage/high speed (400 kHz) operation and low current consumption while the LCD is ON (current consumption in HALT: 1.3 μA), this makes it suitable for battery driven portable equipment such as numeric pagers.

1.1 Features

OSC1 oscillation circuit	32.768 kHz /76.8 kHz /153.6 kHz (Typ.) Crystal oscillation circuit (∗1)
OSC3 oscillation circuit	400 kHz (Typ.) CR oscillation circuit Operatable in 0.9 V
Instruction set	Basic instruction: 46 types (411 instructions with all) Addressing mode: 8 types
Instruction execution time	During operation at 32.768 kHz: 61 μsec 122 μsec 183 μsec During operation at 76.8 kHz: 26 μsec 52 μsec 78 μsec During operation at 153.6 kHz: 13 μsec 26 μsec 39 μsec During operation at 400 kHz: 5 μsec 10 μsec 15 μsec
ROM capacity	Code ROM: 8,192 words × 13 bits
RAM capacity	Data memory: 1,024 words × 4 bits Display memory: 32 words × 4 bits
Input port	8 bits (Pull-up resistors may be supplemented ∗1)
Output port	8 bits (It is possible to switch the 2 bits to special output ∗2)
I/O port	12 bits (It is possible to switch the 4 bits to serial input/output ∗2)
Serial interface	1 port (8-bit clock synchronous system)
LCD driver	32 segments × 4, 3 or 2 commons (∗2) 1/3 or 1/2 bias drive (∗1)
Time base counter	2 systems (Clock timer, stopwatch timer)
Programmable timer	Built-in, 2 inputs × 8 bits, with event counter function
Watchdog timer	Built-in
Gate array	SOG: 11,000 gates Number of terminals: 16 bits CPU interface: Bus interface
Buzzer output	Buzzer frequency: 2 kHz or 4 kHz (∗2)
Supply voltage detection (SVD) circuit	16 values, programmable (1.05 V to 2.60 V)
External interrupt	Input port interrupt: 2 systems
Internal interrupt	Clock timer interrupt: 4 systems Stopwatch timer interrupt: 2 systems Programmable timer interrupt: 2 systems Serial interface interrupt: 1 system Gate array interrupt: 4 systems
Power supply voltage	0.9 V to 3.6 V
Operating temperature range	-20°C to 70°C

Current consumption (Typ.) .... Single clock:
During HALT (32 kHz)
1.5 V (normal mode, LCD power OFF) 1.2 μA
1.5 V (normal mode, LCD power ON) 1.9 μA
3.0 V (halver mode, LCD power ON) 1.3 μA
During operation (32 kHz)
1.5 V (normal mode, LCD power ON) 5.3 μA
3.0 V (halver mode, LCD power ON) 3.2 μA
Twin clock:
During operation (400 kHz)
3.0 V (normal mode, LCD power ON) 87.5 μA

Package .... QFP15-100pin (plastic) or chip

∗1: Can be selected with mask option ∗2: Can be selected with software

1.2 Block Diagram

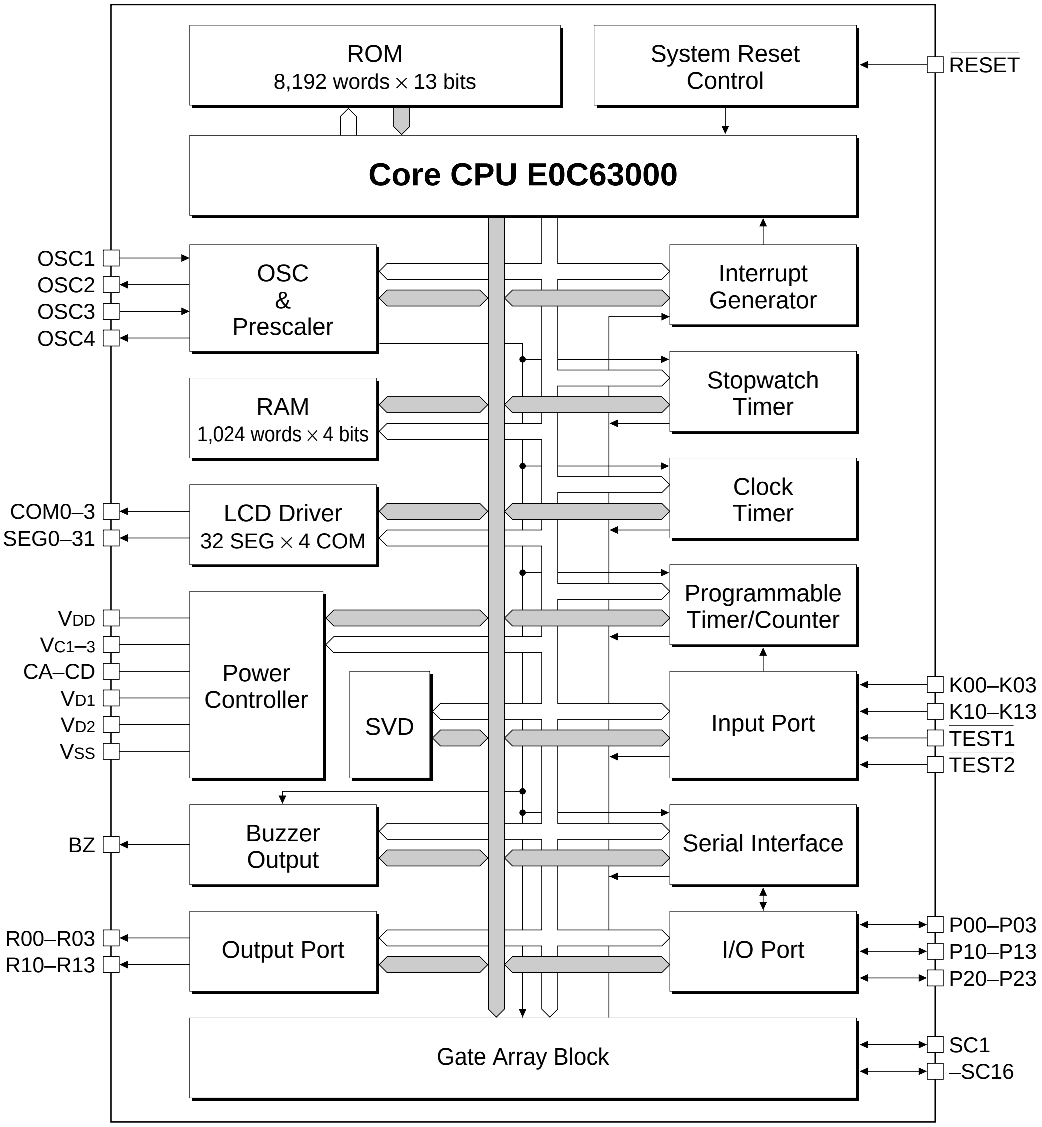
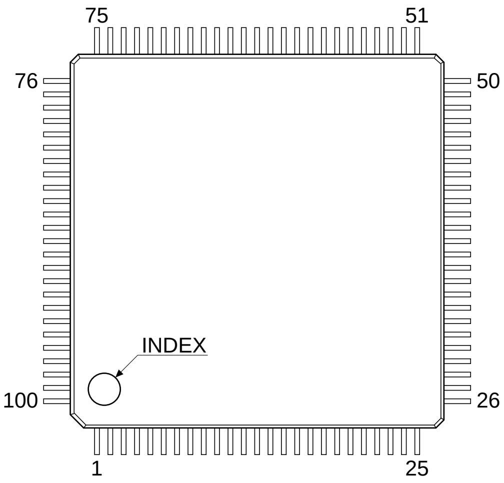


Fig. 1.2.1 Block diagram

1.3 Pin Layout Diagram

QFP15-100pin



No.	Name	No.	Name	No.	Name	No.	Name
1	SEG25	26	N.C.	51	BZ	76	SEG0
2	SEG26	27	CA	52	K00	77	SEG1
3	SEG27	28	$\overline{\text{RESET}}$	53	K01	78	SEG2
4	SEG28	29	$\overline{\text{TEST2}}$	54	K02	79	SEG3
5	SEG29	30	$\overline{\text{TEST1}}$	55	K03	80	SEG4
6	SEG30	31	P23	56	K10	81	SEG5
7	SEG31	32	P22	57	K11	82	SEG6
8	COM0	33	P21	58	K12	83	SEG7
9	COM1	34	P20	59	K13	84	SEG8
10	COM2	35	P13	60	SC1	85	SEG9
11	COM3	36	P12	61	SC2	86	SEG10
12	CD	37	P11	62	SC3	87	SEG11
13	CC	38	P10	63	SC4	88	SEG12
14	V_{C3}	39	P03	64	SC5	89	SEG13
15	V_{C2}	40	P02	65	SC6	90	SEG14
16	V_{C1}	41	P01	66	SC7	91	SEG15
17	V_{D2}	42	P00	67	SC8	92	SEG16
18	V_{SS}	43	R13	68	SC9	93	SEG17
19	OSC1	44	R12	69	SC10	94	SEG18
20	OSC2	45	R11	70	SC11	95	SEG19
21	V_{D1}	46	R10	71	SC12	96	SEG20
22	OSC3	47	R03	72	SC13	97	SEG21
23	OSC4	48	R02	73	SC14	98	SEG22
24	V_{DD}	49	R01	74	SC15	99	SEG23
25	CB	50	R00	75	SC16	100	SEG24

N.C. : No Connection

Fig. 1.3.1 Pin layout diagram

1.4 Pin Description

Table 1.4.1 Pin description

Pin name	Pin No.	In/Out	Function
VDD	24	–	Power (+) supply pin
VSS	18	–	Power (–) supply pin
VD1	21	–	Oscillation/internal logic system regulated voltage output pin
VD2	17	–	Supply voltage doubler/halver output pin
VC1–VC3	16–14	–	LCD system power supply pin 1/3 or 1/2 bias (selected by mask option)
CA, CB	27, 25	–	LCD system boosting/reducing capacitor connecting pin
CC, CD	13, 12	–	Supply voltage doubling/halving capacitor connecting pin
OSC1	19	I	Crystal oscillation input pin
OSC2	20	O	Crystal oscillation output pin
OSC3	22	I	CR oscillation input pin
OSC4	23	O	CR oscillation output pin
K00–K03	52–55	I	Input port
K10–K13	56–59	I	Input port
P00–P03	42–39	I/O	I/O port
P10–P13	38–35	I/O	I/O port (switching to serial I/F input/output is possible by software)
P20–P23	34–31	I/O	I/O port
R00	50	O	Output port
R01	49	O	Output port
R02	48	O	Output port (switching to TOUT output is possible by software)
R03	47	O	Output port (switching to FOUT output is possible by software)
R10–R13	46–43	O	Output port
COM0–COM3	8–11	O	LCD common output pin (1/4, 1/3, 1/2 duty can be selected by software)
SEG0–SEG31	76–100, 1–7	O	LCD segment output pin
BZ	51	O	Buzzer output pin
SC1–SC16	60–75	I, O, I/O	G/A input/output pin
$\overline{\text{RESET}}$	28	I	Initial reset input pin
$\overline{\text{TEST1}}$	30	I	Testing input pin
$\overline{\text{TEST2}}$	29	I	Testing input pin

1.5 Mask Option

Mask options shown below are provided for the E0C63B08. Several hardware specifications are prepared in each mask option, and one of them can be selected according to the application. The function option generator FOG63B08 and the segment option generator SOG63B08, that have been prepared as the development software tool of E0C63B08, are used for this selection. Mask pattern of the IC is finally generated based on the data created by the FOG63B08 and the SOG63B08. Refer to the "E0C63B08 Development Tool Manual" for the FOG63B08 and the SOG63B08.

<Functions selectable with E0C63B08 mask options>

(1) External reset by simultaneous LOW input to the input port (K00–K03)

This function resets the IC when several keys are pressed simultaneously. The mask option is used to select whether this function is used or not. Further when the function is used, a combination of the input ports (K00–K03), which are connected to the keys to be pressed simultaneously, can be selected.
Refer to Section 2.2.2, "Simultaneous low input to terminals K00–K03", for details.

(2) Time authorize circuit for the simultaneous LOW input reset function

When using the external reset function (shown in 1 above), using the time authorize circuit or not can be selected by the mask option. The reset function works only when the input time of simultaneous LOW is more than the rule time if the time authorize circuit is being used.
Refer to Section 2.2.2, "Simultaneous low input to terminals K00–K03", for details.

(3) Input port pull-up resistor

The mask option is used to select whether the pull-up resistor is supplemented to the input ports or not. It is possible to select for each bit of the input ports.
Refer to Section 4.5.3, "Mask option", for details.

(4) Output specification of the output port

Either complementary output or N-channel open drain output can be selected as the output specification for the output ports. The selection is done in 1-bit units or 4-bit units depending on the output port.

1-bit unit: R00, R01, R02, R03
4-bit unit: R10–R13

Refer to Section 4.6.2, "Mask option", for details.

(5) Output specification / pull-up resistor of the I/O ports

Either complementary output or N-channel open drain output can be selected as the output specification when the I/O port is in the output mode. Further, whether or not the pull-up resistors working in the input mode are supplemented can be selected. The selection is done in 1-bit units or 4-bit units depending on the I/O port.

1-bit unit: P20, P21, P22, P23
4-bit unit: P00–P03, P10–P13

Refer to Section 4.7.2, "Mask option", for details.

(6) LCD drive bias

The LCD drive method can be selected from a 1/3 bias drive or a 1/2 bias drive.
Refer to Section 4.8.4, "Mask option", for details.

(7) LCD segment specification

The display memory can be allocated to the optional SEG terminal. It is also possible to set the optional SEG terminal for DC output.
Refer to Section 4.8.4, "Mask option", for details.

(8) Synchronous clock polarity in the serial interface

The polarity of the synchronous clock $\overline{\text{SCLK}}$ and the $\overline{\text{SRDY}}$ signal in slave mode of the serial interface is selected by the mask option. Either positive polarity or negative polarity can be selected.
Refer to Section 4.12.2, "Mask option", for details.

(9) Polarity of the buzzer output signal

It is possible to select the polarity of the buzzer signal output from the BZ terminal. Select either positive polarity or negative polarity according to the external drive transistor to be used.
Refer to Section 4.13.2, "Mask option", for details.

(10)OSC1 oscillation frequency

The oscillation frequency of the OSC1 oscillation circuit (crystal oscillation circuit) can be selected from 32.768 kHz, 76.8 kHz and 153.6 kHz (Typ.). Select one according to the crystal oscillator to be used.
Refer to Section 4.4.2, "OSC1 oscillation circuit", for details.

CHAPTER 2 POWER SUPPLY AND INITIAL RESET

2.1 Power Supply

The E0C63B08 operating power voltage is as follows:

0.9 V to 3.6 V

Note: When a voltage within 0.9 V to 1.25 V is used as the operating power voltage, software control is necessary (see Section 4.2).

The E0C63B08 operates by applying a single power supply within the above range between V_{DD} and V_{SS}. The E0C63B08 itself generates the voltage necessary for all the internal circuits by the built-in power supply circuits shown in Table 2.1.1.

Table 2.1.1 Power supply circuits

Circuit	Power supply circuit	Output voltage
Oscillation and internal circuits	Oscillation system voltage regulator	V_{D1}
LCD driver	LCD system voltage circuit	V_{C1}–V_{C3}
Oscillation sysrem voltage regulator and LCD system voltage circuit	Supply voltage doubler/halver	V_{D2}

Note:
- *Do not drive external loads with the output voltage from the internal power supply circuits.*
- *See Chapter 7, "Electrical Characteristics", for voltage values and drive capability.*

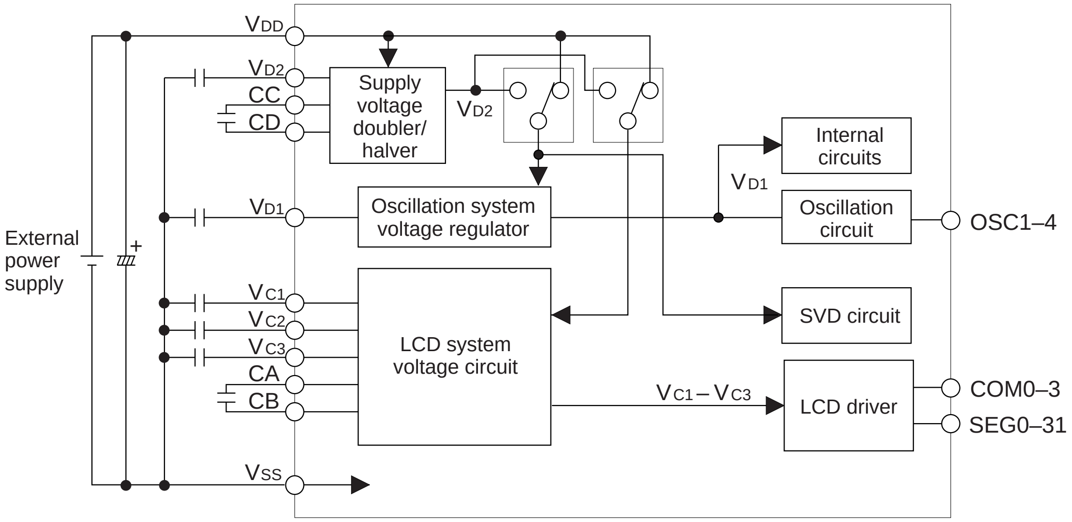


Fig. 2.1.1 Configuration of power supply

2.1.1 Voltage <VD1> for oscillation circuit and internal circuits

VD1 is a voltage for the oscillation circuit and the internal logic circuits, and is generated by the oscillation system voltage regulator for stabilizing the oscillation.
The E0C63B08 is designed with twin clock specification; it has two types of oscillation circuits OSC1 and OSC3 built-in. Use OSC1 clock for normal operation, and switch it to OSC3 by the software when high-speed operation is necessary. When switching the clock, the operating voltage VD1 must be switched by the software to stabilize the operation of the oscillation circuit and internal circuits.
The oscillation system voltage regulator can output the following two types of VD1 voltage. It should be set at the value according to the oscillation circuit and oscillation frequency by the software.

1. Single clock operation (OSC1): VD1 = 1.2 V
2. Twin clock operation (OSC3, Max. 400 kHz): VD1 = 1.45 V

Refer to Section 4.4, "Oscillation Circuit", for the VD1 switching procedure.

To generate the voltage above, a larger voltage (Single clock operation: 1.25 V or more, Twin clock operation: 2.2 V or more) is needed for the oscillation system voltage regulator. Thus the oscillation system voltage regulator can be driven by the voltage VD2 that is boosted to double the power supply voltage (details are explained later). Either the VDD or VD2 can be set by the software to drive the oscillation system voltage regulator.

2.1.2 Voltage <VC1–VC3> for LCD driving

VC1 to VC3 are the voltages for LCD drive, and are generated by the LCD system voltage circuit to stabilize the display quality.

The LCD system voltage circuit generates VC1 with the voltage regulator built-in, and generates two other voltages by boosting the voltage of VC1 (VC2 = 2•VC1, VC3 = 3•VC1). When 1/2 bias is selected by mask option, VC2 becomes the same level with VC1. (VC2 = VC1, VC3 = 2•VC1).

1.25 V or more voltage is needed to generate the voltage VC1, therefore, the LCD system voltage circuit can also be driven with the VD2 voltage boosted from the power supply voltage same as the oscillation system voltage regulator. This selection can be done separately from the oscillation system voltage regulator.
Refer to Chapter 7, "Electrical Characteristics", for voltage values of VC1 to VC3.

2.1.3 Voltage doubler/halver and operating mode

The power supply circuit has the voltage doubler/halver built-in to generate the above mentioned voltages for the oscillation circuit/internal circuits and LCD driving even if the supply voltage is less than those setting voltages, or to reduce current consumption when the power supply voltage has some redundancy. The voltage doubler/halver doubles or halves the voltage supplied from outside, and generates the VD2 voltage for the internal power supply circuits (oscillation system voltage regulator and LCD system voltage circuit).
There are the following three operating modes depending on the status of the voltage doubler/halver, and switching between them is done by the software. Further the mode setting can be done for the oscillation system voltage regulator and the LCD system voltage circuit, independently.

(1) Doubler mode

The E0C63B08 operates with 0.9–3.6 V supply voltage. However, a minimum 1.25 V supply voltage during single clock operation (OSC1) or a minimum 2.2 V during twin clock operation (OSC3, Max. 400 kHz) is needed for the oscillation system voltage regulator. Therefore, when operating with the following supply voltage (V_{DD}), perform a doubling using the voltage doubler/halver and drive the oscillation system regulated voltage circuit with the V_{D2}.

- During single clock operation (OSC1): V_{DD} = 0.9–1.25 V (V_{D2} = 1.8–2.5 V, with doubling)
- During twin clock operation (OSC3, Max. 400 kHz): V_{DD} = 0.9–2.2 V (V_{D2} = 1.8–4.4 V, with doubling)

Operating mode at this time is the doubler mode.
A minimum 1.25 V supply voltage is necessary for the LCD system voltage circuit same as above. Therefore, when operating with 0.9–1.25 V supply voltage V_{DD}, perform a doubling using the voltage doubler/halver and drive the LCD system voltage circuit with V_{D2}. Since this control can independently be done from the oscillation system voltage regulator, when the supply voltage V_{DD} is more than 1.25 V, it is not necessary to operate the LCD system voltage circuit with the doubler mode even if the oscillation system voltage regulator is operated with the doubler mode for OSC3 (Max. 400 kHz).
When the supply voltage is more than needed for operation, do not set in this mode because doubling voltage increases current consumption.

Note: Set the doubler mode when a supply voltage drop is detected by the SVD circuit, such as during heavy load operation (driving buzzer or lamp) or by battery deletion. (*)

(2) Normal mode

In this mode, the internal power circuit directly operates by the power supply voltage V_{DD} within the range of 1.25–3.6 V (2.2–3.6 V when the OSC3 clock is used) without the voltage doubler/halver. At initial reset, this mode is set.

(3) Halver mode

The halver mode can be set when a 2.6–3.6 V power supply voltage is used to operate. This mode halves the power supply voltage using the voltage halver, and operates the internal power circuit using its output voltage V_{D2}. Therefore, current consumption can be reduced to about half of the normal mode.

Note: The OSC3 oscillation circuit cannot be used in the halver mode. Turning the OSC3 oscillation circuit ON in this mode may cause malfunction.

Table 2.1.3.1 Correspondence between power supply voltage and operating mode

Power supply circuit	Operating condition	Power supply voltage V_{DD} (V)			
		0.9–1.25	1.25–2.2	2.2–2.6	2.6–3.6
Oscillation system voltage regulator	OSC1	Doubler mode	Normal mode *		Halver or Normal mode
	OSC3, 400 kHz	Doubler mode		Normal mode	
LCD system voltage circuit		Doubler mode	Normal mode *		Halver or Normal mode

* See above Note.

Refer to Section 4.2, "Setting of Power Supply and Operating Mode", for setting procedure of the operating mode.

2.2 Initial Reset

To initialize the E0C63B08 circuits, initial reset must be executed. There are three ways of doing this.

(1) External initial reset by the $\overline{\text{RESET}}$ terminal
(2) External initial reset by simultaneous low input to terminals K00–K03 (mask option setting)
(3) Initial reset by the oscillation detection circuit

Be sure to use reset functions (1) or (2) at power-on and be sure to initialize securely. In normal operation, the internal circuits may be initialized by any of the above three types.

Figure 2.2.1 shows the configuration of the initial reset circuit.

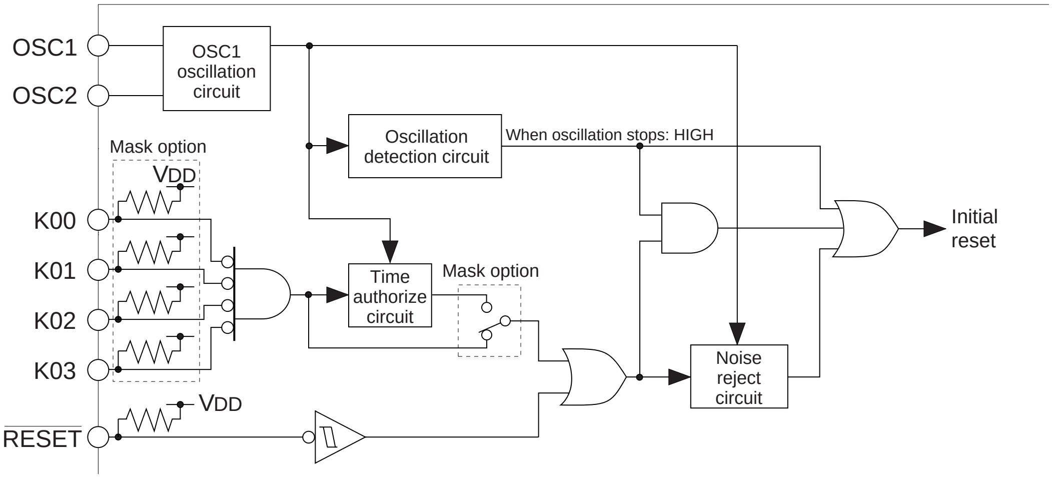


Fig. 2.2.1 Configuration of initial reset circuit

2.2.1 Reset terminal ($\overline{\text{RESET}}$)

The initial resetting can be done by externally setting the $\overline{\text{RESET}}$ terminal to a low level. However, be sure to observe the following precautions, because the reset signal passes through the noise reject circuit.
When the $\overline{\text{RESET}}$ terminal is used for initial resetting during operation, a pulse (low level) of 0.4 msec or less is considered to be noise by the noise reject circuit. Maintain a low level of 1.5 msec to securely perform the initial reset. However, it is necessary that the prescaler set properly according to the OSC1 oscillation frequency. If it is not set properly, the times change as shown in Table 2.2.1.1.
When the $\overline{\text{RESET}}$ terminal goes high, the CPU starts operating.

Table 2.2.1.1 Minimum reset pulse width depending on prescaler setting

Prescaler setting	OSC1 oscillation frequency	Noise reject	Minimum reset pulse width
32.768 kHz	32.768 kHz	0.4 msec	1.5 msec
	76.8 kHz	0.2 msec	0.8 msec
	153.6 kHz	0.1 msec	0.4 msec
76.8 kHz	32.768 kHz	0.2 msec	0.8 msec
	76.8 kHz	0.4 msec	1.5 msec
	153.6 kHz	0.9 msec	3.0 msec
153.6 kHz (default)	32.768 kHz	1.9 msec	6.0 msec
	76.8 kHz	0.9 msec	3.0 msec
	153.6 kHz	0.4 msec	1.5 msec

Refer to Section 4.4, "Oscillation Circuit", for setting of the prescaler.

Since the noise reject circuit does not operate when oscillation is stopped, the noise reject circuit is bypassed until oscillation starts. Therefore, it is necessary to maintain the reset input at a low level until stabilizing oscillation after turning power on. To reset securely at power-on, maintain a low level for at least the following time after oscillation is stabilized.

When the OSC1 oscillation frequency is 32.768 kHz:	6.0 msec
When the OSC1 oscillation frequency is 76.8 kHz:	3.0 msec
When the OSC1 oscillation frequency is 153.6 kHz:	1.5 msec

2.2.2 Simultaneous low input to terminals K00–K03

Another way of executing initial reset externally is to input a low signal simultaneously to the input ports (K00–K03) selected with the mask option.
Since this initial reset also passes through the same noise reject circuit as the reset terminal, maintain the specified input port terminal at low level for 1.5 msec (when the prescaler is set properly) or more during operation. When the power is turned ON, maintain the specified input port terminal at low level until oscillation is stabilized the same as the reset terminal.
Table 2.2.2.1 shows the combinations of input ports (K00–K03) that can be selected with the mask option.

Table 2.2.2.1 Combinations of input ports

1	Not use
2	K00∗K01∗K02∗K03
3	K00∗K01∗K02
4	K00∗K01

When, for instance, mask option 2 (K00∗K01∗K02∗K03) is selected, initial reset is executed when the signals input to the four ports K00–K03 are all low at the same time. When 3 or 4 is selected, the initial reset is done when a key entry including a combination of selected input ports is made.
Further, the time authorize circuit can be selected with the mask option. The time authorize circuit checks the input time of the simultaneous low input and performs initial reset if that time is the defined time (1 to 2 sec) or more.
If using this function, make sure that the specified ports do not go low at the same time during ordinary operation.

2.2.3 Oscillation detection circuit

The oscillation detection circuit outputs the initial reset signal at power-on until the OSC1 oscillation circuit starts oscillating, or when the OSC1 oscillation circuit stops oscillating for some reason.
However, for the initial reset at power-on, use a simultaneous low input of the input ports (K00–K03) or reset terminal, but do not execute it by this function alone.

2.2.4 Internal register at initial resetting

Initial reset initializes the CPU as shown in Table 2.2.4.1.

The registers and flags which are not initialized by initial reset should be initialized in the program if necessary.
In particular, the stack pointers SP1 and SP2 must be set as a pair because all the interrupts including NMI are masked after initial reset until both the SP1 and SP2 stack pointers are set with software.

When data is written to the EXT register, the E flag is set and the following instruction will be executed in the extended addressing mode. If an instruction which does not permit extended operation is used as the following instruction, the operation is not guaranteed. Therefore, do not write data to the EXT register for initialization only.
Refer to the "E0C63000 Core CPU Manual" for extended addressing and usable instructions.

Table 2.2.4.1 Initial values

CPU core			
Name	Symbol	Number of bits	Setting value
Data register A	A	4	Undefined
Data register B	B	4	Undefined
Extension register EXT	EXT	8	Undefined
Index register X	X	16	Undefined
Index register Y	Y	16	Undefined
Program counter	PC	16	0110H
Stack pointer SP1	SP1	8	Undefined
Stack pointer SP2	SP2	8	Undefined
Zero flag	Z	1	Undefined
Carry flag	C	1	Undefined
Interrupt flag	I	1	0
Extension flag	E	1	0
Queue register	Q	16	Undefined

Peripheral circuits		
Name	Number of bits	Setting value
RAM	4	Undefined
Display memory	4	Undefined
Other pheripheral circuits	–	∗

∗ See Section 4.1, "Memory Map".

2.2.5 Terminal settings at initial resetting

The output port (R) terminals and I/O port (P) terminals are shared with special output terminals and input/output terminals of the serial interface. These functions are selected by the software. At initial reset, these terminals are set to the general purpose output port terminals and I/O port terminals. Set them according to the system in the initial routine. In addition, take care of the initial status of output terminals when designing a system.
Table 2.2.5.1 shows the list of the shared terminal settings.

Table 2.2.5.1 List of shared terminal settings

Terminal name	Terminal status at initial reset	Special output		Serial I/F	
		TOUT	FOUT	Master	Slave
R00	R00 (High output)				
R01	R01 (High output)				
R02	R02 (High output)	TOUT			
R03	R03 (High output)		FOUT		
R10–R13	R10–R13 (High output)				
P00–P03	P00–P03 (Input & Pull-up ∗)				
P10	P10 (Input & Pull-up ∗)			SIN(I)	SIN(I)
P11	P11 (Input & Pull-up ∗)			SOUT(O)	SOUT(O)
P12	P12 (Input & Pull-up ∗)			$\overline{\text{SCLK}}$(O)	$\overline{\text{SCLK}}$(I)
P13	P13 (Input & Pull-up ∗)				$\overline{\text{SRDY}}$(O)
P20–P23	P20–P23 (Input & Pull-up ∗)				

∗ When "with pull-up" is selected by mask option (high impedance when "gate direct" is selected)

For setting procedure of the functions, see explanations for each of the peripheral circuits.

2.3 Test Terminal ($\overline{\text{TEST1}}$, $\overline{\text{TEST2}}$)

These are the terminals used for the factory inspection of the IC. During normal operation, connect the $\overline{\text{TEST1}}$ and $\overline{\text{TEST2}}$ terminals to V_{DD}.

CHAPTER 3 *CPU, ROM, RAM*

3.1 CPU

The E0C63B08 has a 4-bit core CPU E0C63000 built-in as its CPU part.
Refer to the "E0C63000 Core CPU Manual" for the E0C63000.

Note: The SLP instruction cannot be used because the SLEEP operation is not assumed in the E0C63B08.

3.2 Code ROM

The built-in code ROM is a mask ROM for loading programs, and has a capacity of 8,192 steps × 13 bits. The core CPU can linearly access the program space up to step FFFFH from step 0000H, however, the program area of the E0C63B08 is step 0000H to step 1FFFH. The program start address after initial reset is assigned to step 0110H. The non-maskable interrupt (NMI) vector and hardware interrupt vectors are allocated to step 0100H and steps 0102H–010EH, respectively.

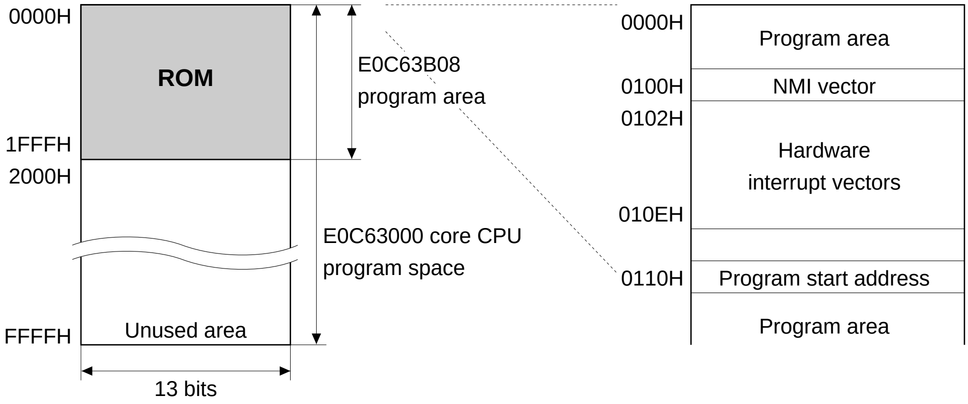


Fig. 3.2.1 Configuration of code ROM

3.3 RAM

The RAM is a data memory for storing various kinds of data, and has a capacity of 1,024 words × 4 bits. The RAM area is assigned to addresses 0000H to 03FFH on the data memory map. Addresses 0100H to 01FFH are 4-bit/16-bit data accessible areas and in other areas it is only possible to access 4-bit data.
When programming, keep the following points in mind.

(1) Part of the RAM area is used as a stack area for subroutine call and register evacuation, so pay attention not to overlap the data area and stack area.

(2) The E0C63000 core CPU handles the stack using the stack pointer for 4-bit data (SP2) and the stack pointer for 16-bit data (SP1).
16-bit data are accessed in stack handling by SP1, therefore, this stack area should be allocated to the area where 4-bit/16-bit access is possible (0100H to 01FFH). The stack pointers SP1 and SP2 change cyclically within their respective range: the range of SP1 is 0000H to 03FFH and the range of SP2 is 0000H to 00FFH. Therefore, pay attention to the SP1 value because it may be set to 0200H or more exceeding the 4-bit/16-bit accessible range in the E0C63B08 or it may be set to 00FFH or less. Memory accesses except for stack operations by SP1 are 4-bit data access.
After initial reset, all the interrupts including NMI are masked until both the stack pointers SP1 and SP2 are set by software. Further, if either SP1 or SP2 is re-set when both are set already, the interrupts including NMI are masked again until the other is re-set. Therefore, the settings of SP1 and SP2 must be done as a pair.

(3) Subroutine calls use 4 words (for PC evacuation) in the stack area for 16-bit data (SP1). Interrupts use 4 words (for PC evacuation) in the stack area for 16-bit data (SP1) and 1 word (for F register evacuation) in the stack area for 4-bit data.

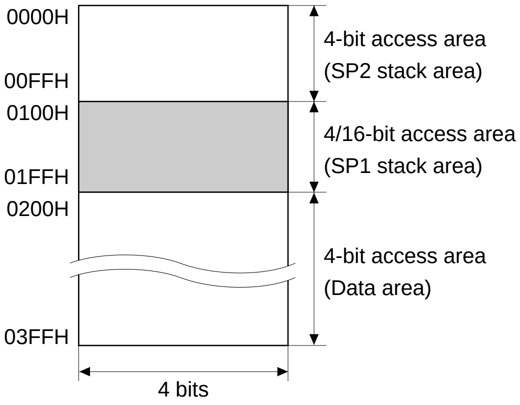


Fig. 3.3.1 Configuration of data RAM

CHAPTER 4 PERIPHERAL CIRCUITS AND OPERATION

The peripheral circuits of E0C63B08 (timer, G/A, I/O, etc.) are interfaced with the CPU in the memory mapped I/O method. Thus, all the peripheral circuits can be controlled by accessing the I/O memory on the memory map using the memory operation instructions. The following sections explain the detailed operation of each peripheral circuit.

4.1 Memory Map

The E0C63B08 data memory consists of 1,024-word RAM, 32-word display memory, 63-word peripheral I/O memory and 64-word G/A (custom block) I/O memory area. Figure 4.1.1 shows the overall memory map of the E0C63B08, and Tables 4.1.1(a)–(e) the peripheral circuits' (I/O space) memory maps.

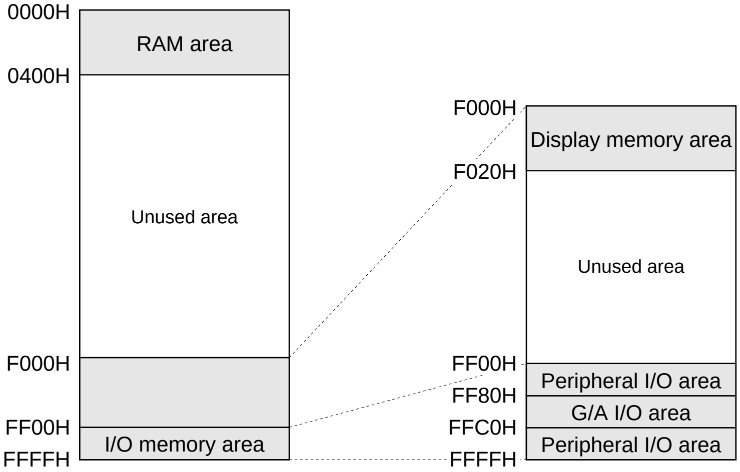


Fig. 4.1.1 Memory map

Note: Memory is not implemented in unused areas within the memory map. Further, some non-implementation areas and unused (access prohibition) areas exist in the peripheral I/O area. If the program that accesses these areas is generated, its operation cannot be guaranteed. Refer to the I/O memory maps shown in Tables 4.1.1 (a)–(e) for the peripheral I/O area.

Table 4.1.1 (a) I/O memory map (FF00H–FF26H)

Address	Register								Comment
	D3	D2	D1	D0	Name	Init *1	1	0	
FF00H	CLKCHG	OSCC	0	VDC	CLKCHG	0	OSC3	OSC1	CPU clock switch
					OSCC	0	On	Off	OSC3 oscillation On/Off
	R/W		R	R/W	0 *3	– *2			Unused
					VDC	0	1.45 V	1.2 V	CPU operating voltage switch (1.2 V: OSC1, 1.45 V: OSC3)
FF01H	VCSEL	VDSEL	HLON	DBON	VCSEL	0	V_{D2}	V_{DD}	Power supply selection for LCD system voltage circuit
					VDSEL	0	V_{D2}	V_{DD}	Power supply selection for oscillation system voltage regulator
	R/W				HLON	0	On	Off	Halver On/Off
					DBON	0	On	Off	Doubler On/Off
FF02H	0	0	PRSM1	PRSM0	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R		R/W		PRSM1	1			OSC1 prescaler selection [PRSM1, 0] 0 1 2, 3 f_{OSC1} (kHz) 32.768 76.8 153.6
					PRSM0	1			
FF04H	SVDS3	SVDS2	SVDS1	SVDS0	SVDS3	0			SVD criteria voltage setting [SVDS3–0] 0 1 2 3 4 5 6 7 Voltage(V) 1.05 1.10 1.15 1.20 1.25 1.30 1.40 1.60 [SVDS3–0] 8 9 10 11 12 13 14 15 Voltage(V) 1.95 2.00 2.05 2.10 2.20 2.30 2.50 2.60
					SVDS2	0			
	R/W				SVDS1	0			
					SVDS0	0			
FF05H	0	0	SVDDT	SVDON	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R			R/W	SVDDT	0	Low	Normal	SVD evaluation data
					SVDON	0	On	Off	SVD circuit On/Off
FF06H	FOUTE	0	FOFQ1	FOFQ0	FOUTE	0	Enable	Disable	FOUT output enable
					0 *3	– *2			Unused
	R/W	R	R/W		FOFQ1	0			FOUT frequency selection [FOFQ1, 0] 0 1 2 3 f_{OSC1}=32kHz f_{OSC1}/64 f_{OSC1}/8 f_{OSC1} f_{OSC3} f_{OSC1}=76kHz f_{OSC1}/128 f_{OSC1}/16 f_{OSC1} f_{OSC3} f_{OSC1}=153kHz f_{OSC1}/256 f_{OSC1}/32 f_{OSC1} f_{OSC3}
					FOFQ0	0			
FF07H	0	0	WDEN	WDRST	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R		R/W	W	WDEN	1	Enable	Disable	Watchdog timer enable
					WDRST*3	Reset	Reset	Invalid	Watchdog timer reset (writing)
FF20H	SIK03	SIK02	SIK01	SIK00	SIK03	0	Enable	Disable	K00–K03 interrupt selection register
					SIK02	0	Enable	Disable	
	R/W				SIK01	0	Enable	Disable	
					SIK00	0	Enable	Disable	
FF21H	K03	K02	K01	K00	K03	– *2	High	Low	K00–K03 input port data
					K02	– *2	High	Low	
	R				K01	– *2	High	Low	
					K00	– *2	High	Low	
FF22H	KCP03	KCP02	KCP01	KCP00	KCP03	1	↓	↑	K00–K03 input comparison register
					KCP02	1	↓	↑	
	R/W				KCP01	1	↓	↑	
					KCP00	1	↓	↑	
FF24H	SIK13	SIK12	SIK11	SIK10	SIK13	0	Enable	Disable	K10–K13 interrupt selection register
					SIK12	0	Enable	Disable	
	R/W				SIK11	0	Enable	Disable	
					SIK10	0	Enable	Disable	
FF25H	K13	K12	K11	K10	K13	– *2	High	Low	K10–K13 input port data
					K12	– *2	High	Low	
	R				K11	– *2	High	Low	
					K10	– *2	High	Low	
FF26H	KCP13	KCP12	KCP11	KCP10	KCP13	1	↓	↑	K10–K13 input comparison register
					KCP12	1	↓	↑	
	R/W				KCP11	1	↓	↑	
					KCP10	1	↓	↑	

Remarks

*1 Initial value at initial reset
*2 Not set in the circuit
*3 Constantly "0" when being read

Table 4.1.1 (b) I/O memory map (FF30H–FF46H)

Address	Register								Comment
	D3	D2	D1	D0	Name	Init *1	1	0	
FF30H	R03HIZ	R02HIZ	R01HIZ	R00HIZ	R03HIZ	0	High-Z	Output	R03 output high impedance control (FOUTE=0) FOUT output high impedance control (FOUTE=1)
					R02HIZ	0	High-Z	Output	R02 output high impedance control (PTOUT=0) TOUT output high impedance control (PTOUT=1)
	R/W				R01HIZ	0	High-Z	Output	R01 output high impedance control
					R00HIZ	0	High-Z	Output	R00 output high impedance control
FF31H	R03	R02	R01	R00	R03	1	High	Low	R03 output port data (FOUTE=0) Fix at "1" when FOUT is used
					R02	1	High	Low	R02 output port data (PTOUT=0) Fix at "1" when TOUT is used
	R/W				R01	1	High	Low	R01 output port data
					R00	1	High	Low	R00 output port data
FF32H	0	0	0	R1HIZ	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R			R/W	0 *3	– *2			Unused
					R1HIZ	0	High-Z	Output	R1 output high impedance control
FF33H	R13	R12	R11	R10	R13	1	High	Low	R10–R13 output port data
					R12	1	High	Low	
	R/W				R11	1	High	Low	
					R10	1	High	Low	
FF40H	IOC03	IOC02	IOC01	IOC00	IOC03	0	Output	Input	P00–P03 I/O control register
					IOC02	0	Output	Input	
	R/W				IOC01	0	Output	Input	
					IOC00	0	Output	Input	
FF41H	PUL03	PUL02	PUL01	PUL00	PUL03	1	On	Off	P00–P03 pull-up control register
					PUL02	1	On	Off	
	R/W				PUL01	1	On	Off	
					PUL00	1	On	Off	
FF42H	P03	P02	P01	P00	P03	– *2	High	Low	P00–P03 I/O port data
					P02	– *2	High	Low	
	R/W				P01	– *2	High	Low	
					P00	– *2	High	Low	
FF44H	IOC13	IOC12	IOC11	IOC10	IOC13	0	Output	Input	P13 I/O control register functions as a general-purpose register when SIF (slave) is selected
					IOC12	0	Output	Input	P12 I/O control register (ESIF=0) functions as a general-purpose register when SIF is selected
	R/W				IOC11	0	Output	Input	P11 I/O control register (ESIF=0) functions as a general-purpose register when SIF is selected
					IOC10	0	Output	Input	P10 I/O control register (ESIF=0) functions as a general-purpose register when SIF is selected
FF45H	PUL13	PUL12	PUL11	PUL10	PUL13	1	On	Off	P13 pull-up control register functions as a general-purpose register when SIF (slave) is selected
					PUL12	1	On	Off	P12 pull-up control register (ESIF=0) functions as a general-purpose register when SIF (master) is selected $\overline{\text{SCLK}}$ (I) pull-up control register when SIF (slave) is selected
	R/W				PUL11	1	On	Off	P11 pull-up control register (ESIF=0) functions as a general-purpose register when SIF is selected
					PUL10	1	On	Off	P10 pull-up control register (ESIF=0) SIN pull-up control register when SIF is selected
FF46H	P13	P12	P11	P10	P13	– *2	High	Low	P13 I/O port data functions as a general-purpose register when SIF (slave) is selected
					P12	– *2	High	Low	P12 I/O port data (ESIF=0) functions as a general-purpose register when SIF is selected
	R/W				P11	– *2	High	Low	P11 I/O port data (ESIF=0) functions as a general-purpose register when SIF is selected
					P10	– *2	High	Low	P10 I/O port data (ESIF=0) functions as a general-purpose register when SIF is selected

Table 4.1.1 (c) I/O memory map (FF48H–FF7AH)

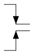
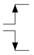
Address	Register								Comment
	D3	D2	D1	D0	Name	Init *1	1	0	
FF48H	IOC23	IOC22	IOC21	IOC20	IOC23	0	Output	Input	P20–P23 I/O control register
					IOC22	0	Output	Input	
	R/W				IOC21	0	Output	Input	
					IOC20	0	Output	Input	
FF49H	PUL23	PUL22	PUL21	PUL20	PUL23	1	On	Off	P20–P23 pull-up control register
					PUL22	1	On	Off	
	R/W				PUL21	1	On	Off	
					PUL20	1	On	Off	
FF4AH	P23	P22	P21	P20	P23	– *2	High	Low	P20–P23 I/O port data
					P22	– *2	High	Low	
	R/W				P21	– *2	High	Low	
					P20	– *2	High	Low	
FF60H	LDUTY1	LDUTY0	VCCHG	LPWR	LDUTY1	0			LCD drive duty switch [LDUTY1, 0] 0 1 2, 3 Duty 1/4 1/3 1/2
					LDUTY0	0			
	R/W				VCCHG	0			General-purpose register (reserved register)
					LPWR	0	On	Off	LCD power On/Off
FF61H	0	ALOFF	ALON	STCD	0 *3	– *2			Unused
					ALOFF	1	All Off	Normal	LCD all OFF control
	R	R/W			ALON	0	All On	Normal	LCD all ON control
					STCD	0	Static	Dynamic	Common output signal control
FF64H	0	0	BZFQ	BZON	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R		R/W		BZFQ	0	2 kHz	4 kHz	Buzzer frequency selection
					BZON	0	On	Off	Buzzer output On/Off
FF70H	0	0	SCTRG	ESIF	0 *3	– *2			Unused
					0 *3	– *2			Unused
					SCTRG	0	Trigger	Invalid	Serial I/F clock trigger (writing)
	R		R/W				Run	Stop	Serial I/F clock status (reading)
					ESIF	0	SIF	I/O	Serial I/F enable (P1 port function selection)
FF71H	SDP	SCPS	SCS1	SCS0	SDP	0	MSB first	LSB first	Serial I/F data input/output permutation
					SCPS	0			Serial I/F clock phase selection
									–Negative polarity (mask option)
	R/W								–Positive polarity (mask option)
					SCS1	0			Serial I/F clock mode selection [SCS1, 0] 0 1 Clock Slave PT [SCS1, 0] 2 3 Clock OSC1/2 OSC1
					SCS0	0			
FF72H	SD3	SD2	SD1	SD0	SD3	– *2	High	Low	MSB
					SD2	– *2	High	Low	Serial I/F transmit/receive data (low-order 4 bits)
	R/W				SD1	– *2	High	Low	
					SD0	– *2	High	Low	LSB
FF73H	SD7	SD6	SD5	SD4	SD7	– *2	High	Low	MSB
					SD6	– *2	High	Low	Serial I/F transmit/receive data (high-order 4 bits)
	R/W				SD5	– *2	High	Low	
					SD4	– *2	High	Low	LSB
FF78H	0	0	TMRST	TMRUN	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R		W	R/W	TMRST*3	Reset	Reset	Invalid	Clock timer reset (writing)
					TMRUN	0	Run	Stop	Clock timer Run/Stop
FF79H	TM3	TM2	TM1	TM0	TM3	0			Clock timer data (16 Hz)
					TM2	0			Clock timer data (32 Hz)
	R				TM1	0			Clock timer data (64 Hz)
					TM0	0			Clock timer data (128 Hz)
FF7AH	TM7	TM6	TM5	TM4	TM7	0			Clock timer data (1 Hz)
					TM6	0			Clock timer data (2 Hz)
	R				TM5	0			Clock timer data (4 Hz)
					TM4	0			Clock timer data (8 Hz)

Table 4.1.1 (d) I/O memory map (FF7CH–FFCBH)

Address	Register								Comment
	D3	D2	D1	D0	Name	Init *1	1	0	
FF7CH	0	0	SWRST	SWRUN	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R		W	R/W	SWRST*3	Reset	Reset	Invalid	Stopwatch timer reset (writing)
					SWRUN	0	Run	Stop	Stopwatch timer Run/Stop
FF7DH	SWD3	SWD2	SWD1	SWD0	SWD3	0			Stopwatch timer data BCD (1/100 sec)
					SWD2	0			
	R				SWD1	0			
					SWD0	0			
FF7EH	SWD7	SWD6	SWD5	SWD4	SWD7	0			Stopwatch timer data BCD (1/10 sec)
					SWD6	0			
	R				SWD5	0			
					SWD4	0			
FFC0H	0	EVCNT	FCSEL	PLPOL	0 *3	– *2			Unused
					EVCNT	0	Event ct.	Timer	Timer 0 counter mode selection
	R	R/W			FCSEL	0	With NR	No NR	Timer 0 function selection (for event counter mode)
					PLPOL	0	↑	↓	Timer 0 pulse polarity selection (for event counter mode)
FFC1H	CHSEL	PTOUT	CKSEL1	CKSEL0	CHSEL	0	Timer1	Timer0	TOUT output channel selection
					PTOUT	0	On	Off	TOUT output control
	R/W				CKSEL1	0	OSC3	OSC1	Prescaler 1 source clock selection
					CKSEL0	0	OSC3	OSC1	Prescaler 0 source clock selection
FFC2H	PTPS01	PTPS00	PTRST0	PTRUN0	PTPS01	0			Prescaler 0 division ratio selection [PTPS01, 00] 0 1 2 3 Division ratio 1/1 1/4 1/32 1/256
					PTPS00	0			
	R/W		W	R/W	PTRST0*3	– *2	Reset	Invalid	Timer 0 reset (reload)
					PTRUN0	0	Run	Stop	Timer 0 Run/Stop
FFC3H	PTPS11	PTPS10	PTRST1	PTRUN1	PTPS11	0			Prescaler 1 division ratio selection [PTPS11, 10] 0 1 2 3 Division ratio 1/1 1/4 1/32 1/256
					PTPS10	0			
	R/W		W	R/W	PTRST1*3	– *2	Reset	Invalid	Timer 1 reset (reload)
					PTRUN1	0	Run	Stop	Timer 1 Run/Stop
FFC4H	RLD03	RLD02	RLD01	RLD00	RLD03	0			MSB
					RLD02	0			Programmable timer 0 reload data (low-order 4 bits)
	R/W				RLD01	0			
					RLD00	0			LSB
FFC5H	RLD07	RLD06	RLD05	RLD04	RLD07	0			MSB
					RLD06	0			Programmable timer 0 reload data (high-order 4 bits)
	R/W				RLD05	0			
					RLD04	0			LSB
FFC6H	RLD13	RLD12	RLD11	RLD10	RLD13	0			MSB
					RLD12	0			Programmable timer 1 reload data (low-order 4 bits)
	R/W				RLD11	0			
					RLD10	0			LSB
FFC7H	RLD17	RLD16	RLD15	RLD14	RLD17	0			MSB
					RLD16	0			Programmable timer 1 reload data (high-order 4 bits)
	R/W				RLD15	0			
					RLD14	0			LSB
FFC8H	PTD03	PTD02	PTD01	PTD00	PTD03	0			MSB
					PTD02	0			Programmable timer 0 data (low-order 4 bits)
	R				PTD01	0			
					PTD00	0			LSB
FFC9H	PTD07	PTD06	PTD05	PTD04	PTD07	0			MSB
					PTD06	0			Programmable timer 0 data (high-order 4 bits)
	R				PTD05	0			
					PTD04	0			LSB
FFCAH	PTD13	PTD12	PTD11	PTD10	PTD13	0			MSB
					PTD12	0			Programmable timer 1 data (low-order 4 bits)
	R				PTD11	0			
					PTD10	0			LSB
FFCBH	PTD17	PTD16	PTD15	PTD14	PTD17	0			MSB
					PTD16	0			Programmable timer 1 data (high-order 4 bits)
	R				PTD15	0			
					PTD14	0			LSB

Table 4.1.1 (e) I/O memory map (FFE0H–FFF7H)

Address	Register								Comment
	D3	D2	D1	D0	Name	Init *1	1	0	
FFE0H	EISCB3	EISCB2	EISCB1	EISCB0	EISCB3	0	Enable	Mask	Interrupt mask register (Custom block 3)
					EISCB2	0	Enable	Mask	Interrupt mask register (Custom block 2)
	R/W				EISCB1	0	Enable	Mask	Interrupt mask register (Custom block 1)
					EISCB0	0	Enable	Mask	Interrupt mask register (Custom block 0)
FFE2H	0	0	EIPT1	EIPT0	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R		R/W		EIPT1	0	Enable	Mask	Interrupt mask register (Programmable timer 1)
					EIPT0	0	Enable	Mask	Interrupt mask register (Programmable timer 0)
FFE3H	0	0	0	EISIF	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R			R/W	0 *3	– *2			Unused
					EISIF	0	Enable	Mask	Interrupt mask register (Serial I/F)
FFE4H	0	0	0	EIK0	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R			R/W	0 *3	– *2			Unused
					EIK0	0	Enable	Mask	Interrupt mask register (K00–K03)
FFE5H	0	0	0	EIK1	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R			R/W	0 *3	– *2			Unused
					EIK1	0	Enable	Mask	Interrupt mask register (K10–K13)
FFE6H	EIT3	EIT2	EIT1	EIT0	EIT3	0	Enable	Mask	Interrupt mask register (Clock timer 1 Hz)
					EIT2	0	Enable	Mask	Interrupt mask register (Clock timer 2 Hz)
	R/W				EIT1	0	Enable	Mask	Interrupt mask register (Clock timer 8 Hz)
					EIT0	0	Enable	Mask	Interrupt mask register (Clock timer 16 Hz)
FFE7H	0	0	EISW1	EISW10	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R		R/W		EISW1	0	Enable	Mask	Interrupt mask register (Stopwatch timer 1 Hz)
					EISW10	0	Enable	Mask	Interrupt mask register (Stopwatch timer 10 Hz)
FFF0H	ISCB3	ISCB2	ISCB1	ISCB0	ISCB3	0	(R)	(R)	Interrupt factor flag (Custom block 3)
					ISCB2	0	Yes	No	Interrupt factor flag (Custom block 2)
	R/W				ISCB1	0	(W)	(W)	Interrupt factor flag (Custom block 1)
					ISCB0	0	Reset	Invalid	Interrupt factor flag (Custom block 0)
FFF2H	0	0	IPT1	IPT0	0 *3	– *2	(R)	(R)	Unused
					0 *3	– *2	Yes	No	Unused
	R		R/W		IPT1	0	(W)	(W)	Interrupt factor flag (Programmable timer 1)
					IPT0	0	Reset	Invalid	Interrupt factor flag (Programmable timer 0)
FFF3H	0	0	0	ISIF	0 *3	– *2	(R)	(R)	Unused
					0 *3	– *2	Yes	No	Unused
	R			R/W	0 *3	– *2	(W)	(W)	Unused
					ISIF	0	Reset	Invalid	Interrupt factor flag (Serial I/F)
FFF4H	0	0	0	IK0	0 *3	– *2	(R)	(R)	Unused
					0 *3	– *2	Yes	No	Unused
	R			R/W	0 *3	– *2	(W)	(W)	Unused
					IK0	0	Reset	Invalid	Interrupt factor flag (K00–K03)
FFF5H	0	0	0	IK1	0 *3	– *2	(R)	(R)	Unused
					0 *3	– *2	Yes	No	Unused
	R			R/W	0 *3	– *2	(W)	(W)	Unused
					IK1	0	Reset	Invalid	Interrupt factor flag (K10–K13)
FFF6H	IT3	IT2	IT1	IT0	IT3	0	(R)	(R)	Interrupt factor flag (Clock timer 1 Hz)
					IT2	0	Yes	No	Interrupt factor flag (Clock timer 2 Hz)
	R/W				IT1	0	(W)	(W)	Interrupt factor flag (Clock timer 8 Hz)
					IT0	0	Reset	Invalid	Interrupt factor flag (Clock timer 16 Hz)
FFF7H	0	0	ISW1	ISW10	0 *3	– *2	(R)	(R)	Unused
					0 *3	– *2	Yes	No	Unused
	R		R/W		ISW1	0	(W)	(W)	Interrupt factor flag (Stopwatch timer 1 Hz)
					ISW10	0	Reset	Invalid	Interrupt factor flag (Stopwatch timer 10 Hz)

4.2 Setting of Power Supply and Operating Mode

This section explains how to control the operating mode according to the supply voltage. Refer to Section 2.1, "Power Supply" for the configuration of the power supply circuit.

4.2.1 Control of supply voltage doubler/halver

When the voltage value necessary to drive the oscillation system voltage regulator and the LCD system voltage circuit is not provided from the power supply voltage supplied externally, the E0C63B08 drives each of the power supply circuits using the voltage that is doubled with the power supply voltage by the supply voltage doubler/halver. On the other hand, when the power supply voltage has a margin, it drives the power supply circuits using the halved voltage to reduce current consumption. The supply voltage doubler/halver is controlled using the registers DBON and HLON.

• For normal operation (when doubling/halves is not done):	Set DBON = "0" and HLON = "0"
• To double the power supply voltage:	Set DBON = "1" and HLON = "0"
• To halve the power supply voltage:	Set DBON = "0" and HLON = "1"

The supply voltage doubler/halver is common to the oscillation system voltage regulator and the LCD system voltage circuit. Therefore when using the doubled or halved voltage for either of these circuits, set the supply voltage doubler/halver accordingly. The doubled/halved voltage is output as V_{D2} from the supply voltage doubler/halver.

Note: The DBON has priority over the HLON.

The oscillation system voltage regulator and the LCD system voltage circuit can independently select the drive voltage among V_{DD} and V_{D2}. This operation mode is controlled using the register VDSEL for the oscillation system voltage regulator and the register VCSEL for the LCD system voltage circuit. By writing "1" to the register, V_{D2} is selected as the drive voltage and writing "0" selects V_{DD}. Approximately 100 msec is necessary until the V_{D2} voltage stables after turning the supply voltage doubler/halver ON by the HLON or DBON. Therefore, the operating mode should be switched as in the following sequence.

Normal mode → Halver/doubler mode

1. Turn the supply voltage doubler/halver ON (set HLON = "1" or DBON = "1").
2. Maintain 100 msec or more.
3. Set "1" in the VDSEL (for the oscillation system voltage regulator) or VCSEL (for the LCD system voltage circuit).

Halver/doubler mode → Normal mode

1. Set "0" in the VDSEL or VCSEL.
2. Turn the supply voltage doubler/halver OFF (set HLON = "0" or DBON = "0").

Note:
- *If the power supply voltage is out of the specified voltage range for an operating mode, do not switch into the operating mode. It may cause malfunction or increase current consumption.*
- *When operating the E0C63B08 with a 0.9–1.25 V power supply voltage, software control is necessary. Set both the oscillation system voltage regulator and the LCD system voltage circuit into doubler mode. At initial reset the normal mode is set.*
- *When switching from the doubler/halver mode to the normal mode, use separate instructions to switch the mode (VDSEL = "0" or VCSEL = "0") and turn the voltage doubler/halver OFF (HLON = "0" or DBON = "0"). Simultaneous processing with a single instruction may cause malfunction.*

4.2.2 Operating mode for the oscillation system voltage regulator and the internal operating voltage

The oscillation system voltage regulator generates the operating voltage VD1 for the oscillation circuit and internal logic circuits. This VD1 voltage must be switched according to the oscillation circuit to be used. Further the operating mode for the oscillation system voltage regulator must be switched depending on the power supply voltage.
Control of VD1 and the oscillation circuit will be explained in Section 4.4, "Oscillation Circuit". This section explains the operating mode for the oscillation system voltage regulator that must be set before controlling them. The following shows the setting contents according to the power supply voltage and the oscillation circuit.

Table 4.2.2.1 Power supply voltage and operating mode

Power supply circuit	Operating condition	Operating voltage VD1	Power supply voltage VDD (V)			
			0.9–1.25	1.25–2.2	2.2–2.6	2.6–3.6
Oscillation system voltage regulator	OSC1	1.2 V	Doubler mode	Normal mode *		Halver or Normal mode
	OSC3, 400 kHz	1.45 V	Doubler mode		Normal mode	

* Set the doubler mode when a supply voltage drop is detected by the SVD circuit, such as during a heavy load operation (driving buzzer or lamp) or by battery deletion.

(1) Power supply voltage VDD = 0.9 V to 1.25 V

When the power supply voltage is in this range, the oscillation system voltage regulator can operate only in the doubler mode.
Set the doubler mode with software, and do not change it to another mode during operation.

(2) Power supply voltage VDD = 1.25 V to 2.2 V

When the CPU operates with the OSC1 clock (OSC3 oscillation circuit is OFF), the oscillation system voltage regulator can operate in the normal mode. Be sure not to set in the halver mode.
It is necessary to set the doubler mode when operating the CPU with the OSC3 clock. Set the operating mode as in the following sequence.
When switching the CPU clock from OSC1 to OSC3 (Max. 400 kHz), set the doubler mode before switching VD1 to 1.45 V (VD1 switching is necessary before turning the OSC3 oscillation circuit on. See Section 4.4). Switching the OSC3 clock leaving in the normal mode may cause malfunction. On the other hand, when switching from OSC3 (Max. 400 kHz) to OSC1, after turning the OSC3 oscillation circuit off, return VD1 to 1.2 V then return to the normal mode.
As described above, OSC3 (Max. 400 kHz) clock can be used by setting the doubler mode, but 3.6 V or more is generated by doubling if the supply voltage is 1.8 V or more. It does not cause any problems in operation, but, it is not advisable to reduce current consumption. When OSC3 (Max. 400 kHz) is used, do not use 1.8–2.2 V supply voltage, if possible.

(3) Power supply voltage VDD = 2.2 V to 2.6 V

When the power supply voltage is in this range, the oscillation system voltage regulator can always operate in the normal mode regardless of the oscillation circuit setting (OSC1, OSC3). Be sure not to set to the halver mode or to the doubler mode.

(4) Power supply voltage VDD = 2.6 V to 3.6 V

When the power supply voltage is in this range, the oscillation system voltage regulator can always operate in the normal mode regardless of the oscillation circuit setting. Be sure not to set in the doubler mode.
When the CPU operates with the OSC1 clock (OSC3 oscillation circuit is OFF), the halver mode can be set to reduce current consumption.
The OSC3 oscillation circuit can be used in this voltage range, however, it is limited in the case of the normal mode. Do not turn the OSC3 oscillation circuit ON during operation in the halver mode.
When using the OSC3 clock, switch the operating mode to the normal mode first.

4.2.3 Operating mode for LCD system voltage circuit

The LCD system voltage circuit generates the voltage V_{C1}, V_{C2} and V_{C3} for driving the LCD. The LCD system voltage circuit generates V_{C1} by the regulator, and boosts it to generate the other 2 voltages. Turning the LCD power supply circuit ON/OFF can be controlled using the register LPWR. The LCD drive voltage is output to the LCD driver only when the circuit is ON (LPWR = "1").
The operating mode should be set according to the power supply voltage for the LCD system voltage circuit set the same as the oscillation system voltage regulator.
The following shows the setting contents according to the power supply voltage.

Table 4.2.3.1 Supply voltage and operating mode

Power supply circuit	Power supply voltage V_{DD} (V)			
	0.9–1.25	1.25–2.2	2.2–2.6	2.6–3.6
LCD system voltage circuit	Doubler mode	Normal mode *		Halver or Normal mode

* Set the doubler mode when a supply voltage drop is detected by the SVD circuit, such as during a heavy load operation (driving buzzer or lamp) or by battery deletion.

(1) Power supply voltage V_{DD} = 0.9 V to 1.25 V

When the power supply voltage is in this range, the LCD system voltage circuit can operate only in the doubler mode.
Set the doubler mode with software, and do not change it to another mode during operation.

(2) Power supply voltage V_{DD} = 1.25 V to 2.6 V

When the power supply voltage is in this range, the LCD system voltage circuit can operate only in the normal mode.

(3) Power supply voltage V_{DD} = 2.6 V to 3.6 V

When the power supply voltage is in this range, the LCD system voltage circuit can operate in the halver mode. It is possible to operate in the normal mode, but be sure not to set to the doubler mode.

4.2.4 I/O memory of power supply and operating mode

Table 4.2.4.1 shows the I/O addresses and control bits for the power supply and the operation mode.

Table 4.2.4.1 Control bits of power supply and operating mode

Address	Register								Comment
	D3	D2	D1	D0	Name	Init *1	1	0	
FF01H	VCSEL	VDSEL	HLON	DBON	VCSEL	0	VD2	VDD	Power supply selection for LCD system voltage circuit
					VDSEL	0	VD2	VDD	Power supply selection for oscillation system voltage regulator
	R/W				HLON	0	On	Off	Halver On/Off
					DBON	0	On	Off	Doubler On/Off
FF60H	LDUTY1	LDUTY0	VCCHG	LPWR	LDUTY1	0			LCD drive duty [LDUTY1, 0] 0 1 2, 3
					LDUTY0	0			switch Duty 1/4 1/3 1/2
	R/W				VCCHG	0			General-purpose register (reserved register)
					LPWR	0	On	Off	LCD power On/Off

*1 Initial value at initial reset

*2 Not set in the circuit

*3 Constantly "0" when being read

DBON: Doubler control (ON/OFF) register (FF01H•D0)

Controls doubling ON/OFF for the voltage doubler/halver.

When "1" is written: Doubler ON
When "0" is written: Doubler OFF
Reading: Valid

When the power supply voltage is in a range of 0.9 to 1.25 V, generate VD2 by doubling the supply voltage to drive the internal power supply circuit. When "1" is written to the DBON register, the voltage doubler/halver generates VD2 by doubling the supply voltage. When "0" is written, doubling is not performed.
When the power supply voltage is 1.25 V or more, do not double the voltage. However, this does not apply when the battery voltage falls by heavy load such as driving a buzzer and turning a lamp on.
The DBON has priority over the HLON.
At initial reset, this register is set to "0".

HLON: Halver control (ON/OFF) register (FF01H•D1)

Controls halves ON/OFF for the voltage doubler/halver.

When "1" is written: Halver ON
When "0" is written: Halver OFF
Reading: Valid

When the power supply voltage is in a range of 2.6 to 3.6 V, the internal power supply circuit can be driven by the halved voltage to reduce current consumption. When "1" is written to the HLON register, the voltage doubler/halver generates VD2 by halving the supply voltage. When "0" is written, halving is not performed. When the power supply voltage is 2.6 V or less, do not halve the voltage.
At initial reset, this register is set to "0".

VDSEL: Power supply selection register for oscillation system voltage regulator (FF01H•D2)

Selects the power supply for the oscillation system voltage regulator.

When "1" is written: VD2
When "0" is written: VDD
Reading: Valid

When "1" is written to the VDSEL register, the oscillation system voltage regulator operates with VD2 output from the voltage doubler/halver. The doubler mode or the halver mode is set according to the DBON and HLON settings. When "0" is written to the VDSEL register, the oscillation system voltage regulator operates with VDD and the operating mode becomes the normal mode.
When switching from the normal mode to the doubler/halver mode, the VDSEL register should be set to "1" after taking a 100 msec or longer interval for the VD2 to stabilize from setting the DBON or HLON register to "1".
At initial reset, this register is set to "0".

VCSEL: Power supply selection register for LCD system voltage circuit (FF01H•D3)

Selects the power supply for the LCD system voltage circuit.

When "1" is written: V_{D2}
When "0" is written: V_{DD}
Reading: Valid

When "1" is written to the VCSEL register, the LCD system voltage circuit operates with V_{D2} output from the voltage doubler/halver. The doubler mode or the halver mode is set according to the DBON and HLON settings. When "0" is written to the VCSEL register, the LCD system voltage circuit operates with V_{DD} and the operating mode becomes the normal mode.
When switching from the normal mode to the doubler/halver mode, the VCSEL register should be set to "1" after taking a 100 msec or longer interval for the V_{D2} to stabilize from setting the DBON or HLON register to "1".
At initial reset, this register is set to "0".

LPWR: LCD power control (ON/OFF) register (FF60H•D0)

Turns the LCD system voltage circuit ON/OFF.

When "1" is written: ON
When "0" is written: OFF
Reading: Valid

When "1" is written to the LPWR register, the LCD system voltage circuit goes ON and generates the LCD drive voltage. When "0" is written, the LCD drive voltage is not output.
At initial reset, this register is set to "0".

4.2.5 Programming notes

(1) When operating the E0C63B08 with a 0.9–1.25 V power supply voltage, software control is necessary. Set both the oscillation system voltage regulator and the LCD system voltage circuit to doubler mode.

(2) If the power supply voltage is out of the specified voltage range for an operating mode, do not switch to the operating mode. It may cause malfunction or increase current consumption.

(3) Do not set the registers HLON (halves) and DBON (doubling) to "1" simultaneously.

(4) When switching from the normal mode to the doubler/halver mode, the VCSEL register should be set to "1" after taking a 100 msec or longer interval for the V_{D2} to stabilize from switching the DBON or HLON register to "1".

(5) When switching from the doubler/halver mode to the normal mode, use separate instructions to switch the mode (VDSEL = "0" or VCSEL = "0") and turn the voltage doubler/halver OFF (HLON = "0" or DBON = "0"). Simultaneous processing with a single instruction may cause malfunction.

(6) The OSC3 oscillation circuit cannot operate in halver mode. When the supply voltage is in the range of 0.9 V to 2.2 V, the OSC3 oscillation circuit can only operate in the doubler mode. When the supply voltage is in the range of 2.2 V to 3.6 V, it can operate in the normal mode.

4.3 Watchdog Timer

4.3.1 Configuration of watchdog timer

The E0C63B08 has a built-in watchdog timer that operates with a 256 Hz divided clock from the OSC1 as the source clock. The watchdog timer starts operating after initial reset, however, it can be stopped by the software. The watchdog timer must be reset cyclically by the software while it operates. If the watchdog timer is not reset in at least 3–4 seconds, it generates a non-maskable interrupt (NMI) to the CPU.
Figure 4.3.1.1 is the block diagram of the watchdog timer.

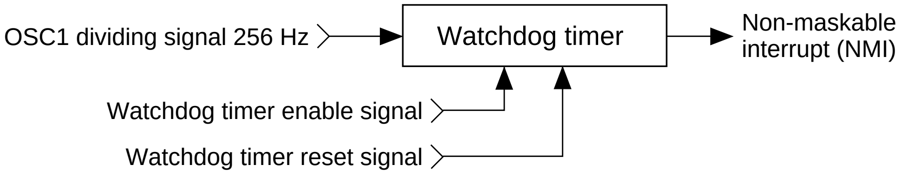


Fig. 4.3.1.1 Watchdog timer block diagram

The watchdog timer contains a 10-bit binary counter, and generates the non-maskable interrupt when the last stage of the counter (0.25 Hz) overflows.
Watchdog timer reset processing in the program's main routine enables detection of program overrun, such as when the main routine's watchdog timer processing is bypassed. Ordinarily this routine is incorporated where periodic processing takes place, just as for the timer interrupt routine.
The watchdog timer operates in the HALT mode. If a HALT status continues for 3–4 seconds, the non-maskable interrupt releases the HALT status.

4.3.2 Interrupt function

If the watchdog timer is not reset periodically, the non-maskable interrupt (NMI) is generated to the core CPU. Since this interrupt cannot be masked, it is accepted even in the interrupt disable status (I flag = "1"). However, it is not accepted when the CPU is in the interrupt mask state until SP1 and SP2 are set as a pair, such as after initial reset or during re-setting the stack pointer. The interrupt vector of NMI is assigned to 0100H in the program memory.

4.3.3 I/O memory of watchdog timer

Table 4.3.3.1 shows the I/O address and control bits for the watchdog timer.

Table 4.3.3.1 Control bits of watchdog timer

Address	Register								Comment
	D3	D2	D1	D0	Name	Init *1	1	0	
FF07H	0	0	WDEN	WDRST	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R		R/W	W	WDEN	1	Enable	Disable	Watchdog timer enable
					WDRST*3	Reset	Reset	Invalid	Watchdog timer reset (writing)

*1 Initial value at initial reset

*2 Not set in the circuit

*3 Constantly "0" when being read

WDEN: Watchdog timer enable register (FF07H•D1)

Selects whether the watchdog timer is used (enabled) or not (disabled).

When "1" is written: Enabled
When "0" is written: Disabled
Reading: Valid

When "1" is written to the WDEN register, the watchdog timer starts count operation. When "0" is written, the watchdog timer does not count and does not generate the interrupt (NMI).
At initial reset, this register is set to "1".

WDRST: Watchdog timer reset (FF07H•D0)

Resets the watchdog timer.

When "1" is written: Watchdog timer is reset
When "0" is written: No operation
Reading: Always "0"

When "1" is written to WDRST, the watchdog timer is reset and restarts immediately after that. When "0" is written, no operation results.
This bit is dedicated for writing, and is always "0" for reading.

4.3.4 Programming notes

(1) When the watchdog timer is being used, the software must reset it within 3-second cycles.

(2) Because the watchdog timer is set in operation state by initial reset, set the watchdog timer to disabled state (not used) before generating an interrupt (NMI) if it is not used.

4.4 Oscillation Circuit

4.4.1 Configuration of oscillation circuit

The E0C63B08 has two oscillation circuits (OSC1 and OSC3). OSC1 is a crystal oscillation circuit that supplies the operating clock to the CPU and peripheral circuits. OSC3 is a CR oscillation circuit. When processing with the E0C63B08 requires high-speed operation, the CPU operating clock can be switched from OSC1 to OSC3 by the software. To stabilize operation of the internal circuits, the operating voltage VD1 must be switched according to the oscillation circuit to be used. Figure 4.4.1.1 is the block diagram of this oscillation system.

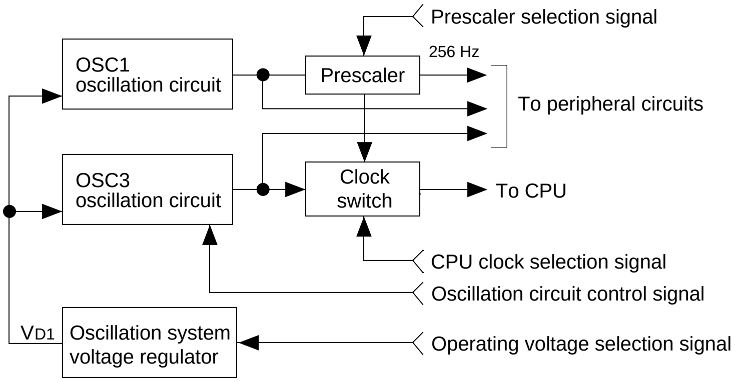


Fig. 4.4.1.1 Oscillation system block diagram

The OSC1 oscillation circuit can deal with three types of oscillation frequencies (32.768 kHz, 76.8 kHz or 153.6 kHz). For this purpose, the prescaler (dividing stages) for the frequencies are connected to the OSC1 oscillation circuit, and one of them should be selected by the software according to the frequency to be used.

4.4.2 OSC1 oscillation circuit

The E0C63B08 has a built-in crystal oscillation circuit (OSC1 oscillation circuit). The oscillation frequency can be selected from 32.768 kHz, 76.8 kHz and 153.6 kHz (Typ.) by mask option. The OSC1 oscillation circuit generates the operating clock for the CPU and peripheral circuits by connecting a crystal oscillator and a trimmer capacitor (5–25 pF) as the external elements.
Figure 4.4.2.1 is the block diagram of the OSC1 oscillation circuit.

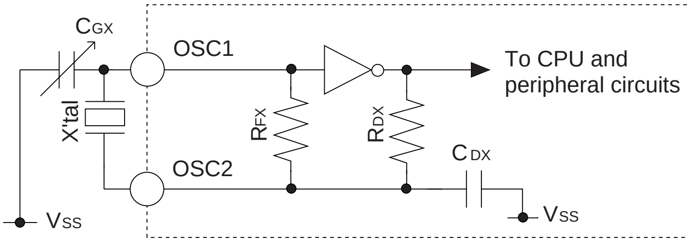


Fig. 4.4.2.1 OSC1 oscillation circuit

As shown in Figure 4.4.2.1, the crystal oscillation circuit can be configured simply by connecting the crystal oscillator (X'tal) between the OSC1 and OSC2 terminals and the trimmer capacitor (CGX) between the OSC1 and VSS terminals.

Note: The OSC1 oscillation circuit deals with three types of crystal oscillators (32.768 kHz, 76.8 kHz or 153.6 kHz), however, it is necessary to set the prescaler to correspond with the frequency of the oscillator being used. Be sure to set the prescaler properly in the initial routine, which is executed immediately after initial reset, before controlling peripheral circuits.

4.4.3 OSC3 oscillation circuit

The E0C63B08 has built-in the OSC3 oscillation circuit that generates the CPU's sub-clock (Max. 400 kHz) for high speed operation and the source clock for peripheral circuits needing a high speed clock (programmable timer, FOUT output). OSC3 is a CR oscillation circuit. A resistor is required as an external element when using the OSC3 oscillation circuit.
Figure 4.4.3.1 is the block diagram of the OSC3 oscillation circuit (CR oscillation circuit).

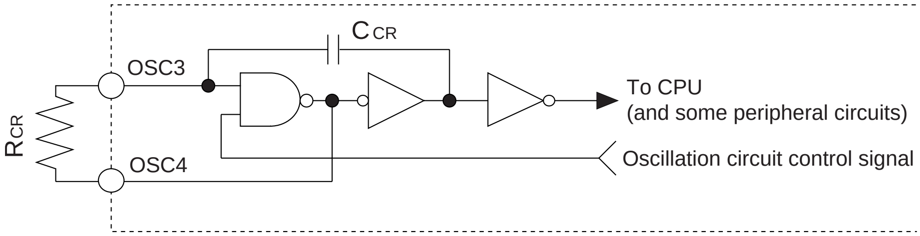


Fig. 4.4.3.1 OSC3 oscillation circuit (CR oscillation circuit)

As shown in Figure 4.4.3.1, the CR oscillation circuit can be configured simply by connecting the resistor RCR between the OSC3 and OSC4 terminals. See Chapter 7, "Electrical Characteristics" for resistance value of RCR.
To reduce current consumption of the OSC3 oscillation circuit, oscillation can be stopped by the software (OSCC register).
Note, however, to operate the OSC3 oscillation circuit, when the supply voltage VDD is 2.2 V or less, the oscillation system voltage regulator must be operated in the doubler mode. (See Section 4.2.)

4.4.4 Switching of operating voltage

The CPU system clock is switched to OSC1 or OSC3 by the software (CLKCHG register). In this case, to obtain stable operation, the operating voltage VD1 for the internal circuits must be switched by the software (VDC register). As described in Section 4.2, "Setting of Power Supply and Operating Mode", the oscillation system voltage regulator that generates VD1 must be set in an appropriate operating mode according to the supply voltage.
Table 4.4.4.1 shows the correspondence of the system clock, operating voltage VD1 and operating mode for the oscillation system voltage regulator.

Table 4.4.4.1 System clock and operating voltage

System clock	Operating voltage VD1	Operating mode according to supply voltage VDD (V)			
		0.9–1.25	1.25–2.2	2.2–2.6	2.6–3.6
OSC1	1.2 V	Doubler mode	Normal mode *		Halver or Normal mode
OSC3, 400 kHz	1.45 V	Doubler mode		Normal mode	

* Set the doubler mode when a power supply voltage drop is detected by the SVD circuit, such as during a heavy load operation (driving buzzer or lamp) or by battery deletion.

When switching the operating voltage and the system clock, properly set the operating mode for the oscillation system voltage regulator before and after. (See Section 4.2, "Setting of Power Supply and Operation Mode".)

When OSC3 is to be used as the CPU system clock, it should be done as the following procedure using the software: first switch the operating mode (if necessary) and the operating voltage VD1, turn the OSC3 oscillation ON after waiting 2.5 msec or more for the above operation to stabilize, switch the clock after waiting 5 msec or more for oscillation stabilization.

When switching from OSC3 to OSC1, turn the OSC3 oscillation circuit OFF after switching the clock then set the operating voltage V_{D1} to 1.2 V. After that, switch the operating mode if necessary.

OSC1 → OSC3

1. Set operation mode for OSC3. ∗
2. Set VDC to "1" (1.2 V → 1.45 V).
3. Maintain 2.5 msec or more.
4. Set OSCC to "1" (OSC3 oscillation ON).
5. Maintain 5 msec or more.
6. Set CLKCHG to "1" (OSC1 → OSC3).

OSC3 → OSC1

1. Set CLKCHG to "0" (OSC3 → OSC1).
2. Set OSCC to "0" (OSC3 oscillation OFF).
3. Set VDC to "0" (1.45 V → 1.2 V).
4. Set operation mode for OSC1. ∗

(∗: Should be done only when necessary.)

The following shows the operating mode settings for the oscillation system voltage regulator depending on the power supply voltage.

(1) Power supply voltage V_{DD} = 0.9 V to 1.25 V

When the power supply voltage is in this range, the oscillation system voltage regulator can be operated only in the doubler mode.

(2) Power supply voltage V_{DD} = 1.25 V to 2.2 V

When the system clock is OSC1, operate the oscillation system voltage regulator in the normal mode. When operating the OSC3 oscillation circuit, set the doubler mode.

(3) Power supply voltage V_{DD} = 2.2 V to 2.6 V

When the power supply voltage is in this range, the oscillation system voltage regulator can always be operated in the normal mode regardless of the system clock selection. Therefore, it is nor necessary to switch the operating mode before and after switching the system clock.

(4) Power supply voltage V_{DD} = 2.6 V to 3.6 V

When the system clock is OSC1, the halver mode can be set to reduce current consumption. In this case, return to the normal mode before switching the system clock to OSC3. It is unnecessary to switch the operating mode before and after switching the system clock when operating in the normal mode. After switching from OSC3 to OSC1, return to the halver mode.

Be sure not to switch to the OSC3 clock in the halver mode because it may cause malfunction.

Note: Switching the operating voltage when the power supply voltage is lower than the set voltage (that can generate V_{D1}) may cause malfunction. Switch the operating voltage only after making sure that the power supply voltage is more than the set voltage using the SVD circuit.

4.4.5 Clock frequency and instruction execution time

Table 4.4.5.1 shows the instruction execution time according to each frequency of the system clock.

Table 4.4.5.1 Clock frequency and instruction execution time

Clock frequency	Instruction execution time (µsec)		
	1-cycle instruction	2-cycle instruction	3-cycle instruction
OSC1: 32.768 kHz	61	122	183
OSC1: 76.8 kHz	26	52	78
OSC1: 153.6 kHz	13	26	39
OSC3: 400 kHz	5	10	15

4.4.6 I/O memory of oscillation circuit

Table 4.4.6.1 shows the I/O addresses and the control bits for the oscillation circuit.

Table 4.4.6.1 Control bits of oscillation circuit

Address	Register				Comment				
	D3	D2	D1	D0	Name	Init *1	1	0	
FF00H	CLKCHG	OSCC	0	VDC	CLKCHG	0	OSC3	OSC1	CPU clock switch
					OSCC	0	On	Off	OSC3 oscillation On/Off
	R/W		R	R/W	0 *3	– *2			Unused
					VDC	0	1.45 V	1.2 V	CPU operating voltage switch (1.2 V: OSC1, 1.45 V: OSC3)
FF02H	0	0	PRSM1	PRSM0	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R		R/W		PRSM1	1			OSC1 prescaler selection [PRSM1, 0] 0 1 2, 3 fOSC1 (kHz) 32.768 76.8 153.6
					PRSM0	1			

*1 Initial value at initial reset

*2 Not set in the circuit

*3 Constantly "0" when being read

PRSM1, PRSM0: OSC1 prescaler selection register (FF02H•D1, D0)

Selects the prescaler for the OSC1 oscillation circuit.

Table 4.4.6.2 Prescaler selection

PRSM1	PRSM0	Oscillation frequency
1	*	153.6 kHz
0	1	76.8 kHz
0	0	32.768 kHz

Select one according to the connected oscillator.
To operate the timers properly, be sure to set the prescaler to correspond with the frequency of the connected oscillator in the initial routine immediately after initial reset before controlling the peripheral circuits.
At initial reset, this register is set to "11B".

VDC: CPU operating voltage switching register (FF00H•D0)

Switches the operating voltage V_{D1}.

When "1" is written: 1.45 V (for OSC3 operation)
When "0" is written: 1.2 V (for OSC1 operation)
Reading: Valid

When switching the CPU system clock, the operating voltage V_{D1} should also be switched according to the clock.
When switching from OSC1 to OSC3, first set V_{D1} to 1.45 V. After that maintain 2.5 msec or more, and then turn the OSC3 oscillation ON.
When switching from OSC3 to OSC1, set V_{D1} to 1.2 V after switching to OSC1 and turning the OSC3 oscillation OFF.
It is necessary to switch the operating mode for the oscillation system voltage regulator depending on the power supply voltage.
At initial reset, this register is set to "0".

OSCC: OSC3 oscillation control register (FF00H•D2)

Controls oscillation ON/OFF for the OSC3 oscillation circuit.

When "1" is written: OSC3 oscillation ON
When "0" is written: OSC3 oscillation OFF
Reading: Valid

When it is necessary to operate the CPU at high speed, set OSCC to "1". At other times, set it to "0" to reduce current consumption. Furthermore, when turning the OSC3 oscillation circuit ON and OFF, it is necessary to switch the operating voltage V_{D1}.
At initial reset, this register is set to "0".

CLKCHG: CPU system clock switching register (FF00H•D3)

The CPU's operation clock is selected with this register.

When "1" is written: OSC3 clock is selected
When "0" is written: OSC1 clock is selected
Reading: Valid

When the CPU clock is to be OSC3, set CLKCHG to "1"; for OSC1, set CLKCHG to "0".
After turning the OSC3 oscillation ON (OSCC = "1"), switching of the clock should be done after waiting 5 msec or more.
When V_{D1} is 1.2 V (VDC = "0"), setting of CLKCHG = "1" becomes invalid and switching to OSC3 is not performed.
At initial reset, this register is set to "0".

4.4.7 Programming notes

(1) The OSC1 oscillation circuit deals with three types of crystal oscillators (can be selected from 32.768 kHz, 76.8 kHz and 153.6 kHz by mask option), however, it is necessary to set the prescaler to correspond with the frequency of the oscillator being used. Be sure to set the prescaler properly in the initial routine, which is executed immediately after initial reset, before controlling peripheral circuits.

(2) When switching the CPU system clock from OSC1 to OSC3, first set V_{D1} and the operating mode. After that maintain 2.5 msec or more, and then turn the OSC3 oscillation ON.
When switching from OSC3 to OSC1, set V_{D1} and the operating mode after switching to OSC1 and turning the OSC3 oscillation OFF.

(3) It takes at least 5 msec from the time the OSC3 oscillation circuit goes ON until the oscillation stabilizes. Consequently, when switching the CPU operation clock from OSC1 to OSC3, do this after a minimum of 5 msec have elapsed since the OSC3 oscillation went ON.
Further, the oscillation stabilization time varies depending on the external oscillator characteristics and conditions of use, so allow ample margin when setting the wait time.

(4) When switching the clock form OSC3 to OSC1, use a separate instruction for switching the OSC3 oscillation OFF. An error in the CPU operation can result if this processing is performed at the same time by the one instruction.

(5) Switching the operating voltage when the power supply voltage is lower than the set voltage (that can generate V_{D1}) may cause malfunction. Switch the operating voltage only after making sure that the power supply voltage is more than the set voltage using the SVD circuit.

4.5 Input Ports (K00–K03 and K10–K13)

4.5.1 Configuration of input ports

The E0C63B08 has eight bits general-purpose input ports. Each of the input port terminals (K00–K03, K10–K13) provides internal pull-up resistor. Pull-up resistor can be selected for each bit with the mask option.
Figure 4.5.1.1 shows the configuration of input port.

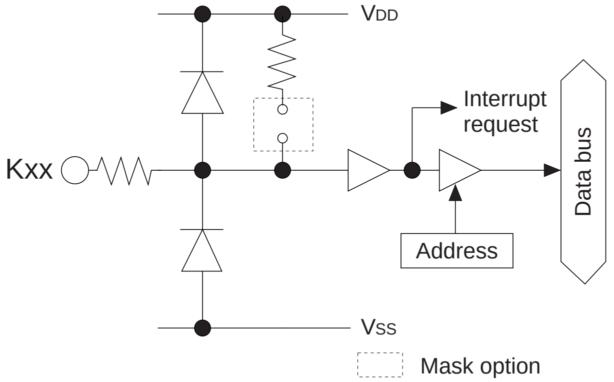


Fig. 4.5.1.1 Configuration of input port

Selection of "With pull-up resistor" with the mask option suits input from the push switch, key matrix, and so forth. When "Gate direct" is selected, the port can be used for slide switch input and interfacing with other LSIs.

4.5.2 Interrupt function

All eight bits of the input ports (K00–K03, K10–K13) provide the interrupt function. The conditions for issuing an interrupt can be set by the software. Further, whether to mask the interrupt function can be selected by the software.
Figure 4.5.2.1 shows the configuration of K00–K03 (K10–K13) interrupt circuit.

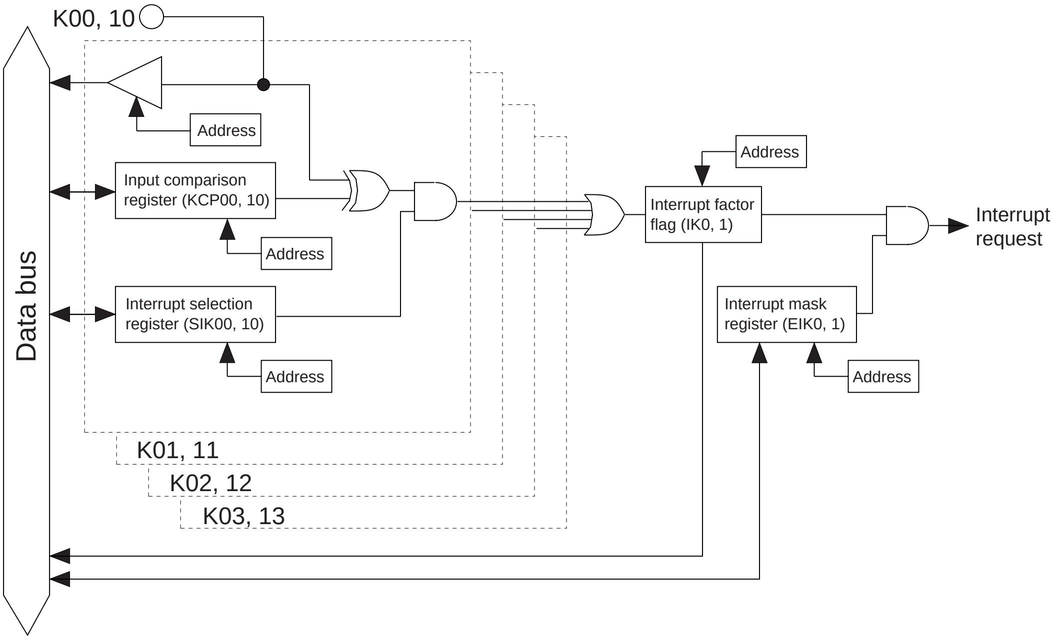


Fig. 4.5.2.1 Input interrupt circuit configuration

The interrupt selection register (SIK) and input comparison register (KCP) are individually set for the input ports K00–K03 and K10–K13, and can specify the terminals for generating interrupt and interrupt timing.

The interrupt selection registers (SIK00–SIK03, SIK10–SIK13) select what input of K00–K03 and K10–K13 to use for the interrupt. Writing "1" into an interrupt selection register incorporates that input port into the interrupt generation conditions. The changing the input port where the interrupt selection register has been set to "0" does not affect the generation of the interrupt.

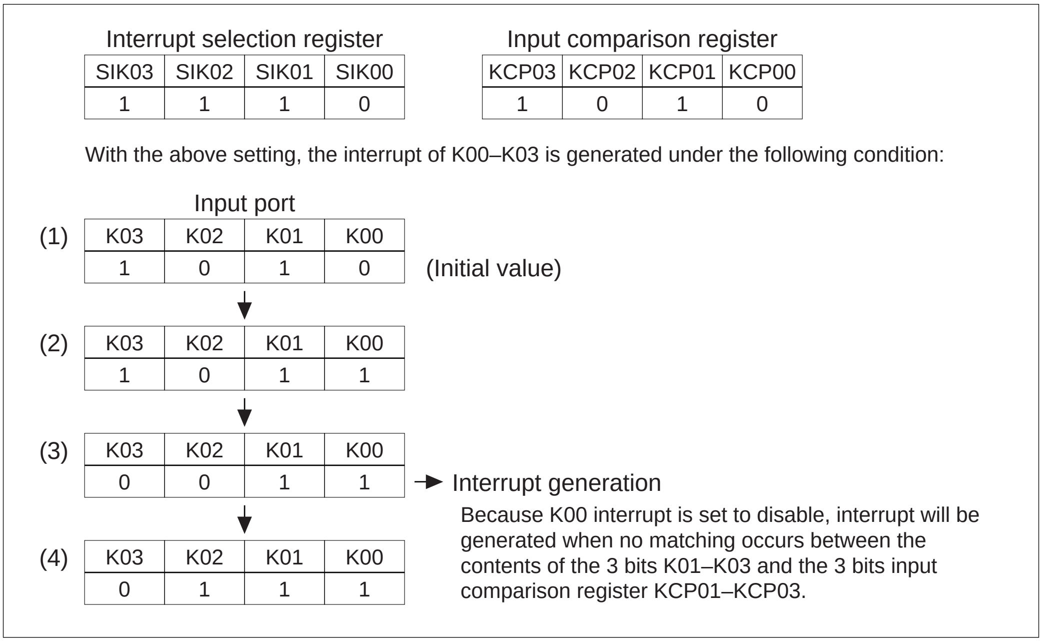
The input interrupt timing can select that the interrupt be generated at the rising edge of the input or that it be generated at the falling edge according to the set value of the input comparison registers (KCP00–KCP03, KCP10–KCP13).

By setting these two conditions, the interrupt for K00–K03 or K10–K13 is generated when input ports in which an interrupt has been enabled by the input selection registers and the contents of the input comparison registers have been changed from matching to no matching.

The interrupt mask registers (EIK0, EIK1) enable the interrupt mask to be selected for K00–K03 and K10–K13.

When the interrupt is generated, the interrupt factor flag (IK0, IK1) is set to "1".

Figure 4.5.2.2 shows an example of an interrupt for K00–K03.



Interrupt selection register

SIK03	SIK02	SIK01	SIK00
1	1	1	0

Input comparison register

KCP03	KCP02	KCP01	KCP00
1	0	1	0

With the above setting, the interrupt of K00–K03 is generated under the following condition:

Input port

(1)

K03	K02	K01	K00
1	0	1	0

(Initial value)

(2)

K03	K02	K01	K00
1	0	1	1

(3)

K03	K02	K01	K00
0	0	1	1

Interrupt generation

Because K00 interrupt is set to disable, interrupt will be generated when no matching occurs between the contents of the 3 bits K01–K03 and the 3 bits input comparison register KCP01–KCP03.

(4)

K03	K02	K01	K00
0	1	1	1

Fig. 4.5.2.2 Example of interrupt of K00–K03

K00 interrupt is disabled by the interrupt selection register (SIK00), so that an interrupt does not occur at (2). At (3), K03 changes to "0"; the data of the terminals that are interrupt enabled no longer match the data of the input comparison registers, so that interrupt occurs. As already explained, the condition for the interrupt to occur is the change in the port data and contents of the input comparison registers from matching to no matching. Hence, in (4), when the no matching status changes to another no matching status, an interrupt does not occur. Further, terminals that have been masked for interrupt do not affect the conditions for interrupt generation.

4.5.3 Mask option

Internal pull-up resistor can be selected for each of the eight bits of the input ports (K00–K03, K10–K13) with the input port mask option.

When "Gate direct" is selected, take care that the floating status does not occur for the input. Select "With pull-up resistor" for input ports that are not being used.

4.5.4 I/O memory of input ports

Table 4.5.4.1 shows the I/O addresses and the control bits for the input ports.

Table 4.5.4.1 Control bits of input ports

Address	Register								Comment
	D3	D2	D1	D0	Name	Init *1	1	0	
FF20H	SIK03	SIK02	SIK01	SIK00	SIK03	0	Enable	Disable	K00–K03 interrupt selection register
					SIK02	0	Enable	Disable	
	R/W				SIK01	0	Enable	Disable	
					SIK00	0	Enable	Disable	
FF21H	K03	K02	K01	K00	K03	– *2	High	Low	K00–K03 input port data
					K02	– *2	High	Low	
	R				K01	– *2	High	Low	
					K00	– *2	High	Low	
FF22H	KCP03	KCP02	KCP01	KCP00	KCP03	1	↓	↑	K00–K03 input comparison register
					KCP02	1	↓	↑	
	R/W				KCP01	1	↓	↑	
					KCP00	1	↓	↑	
FF24H	SIK13	SIK12	SIK11	SIK10	SIK13	0	Enable	Disable	K10–K13 interrupt selection register
					SIK12	0	Enable	Disable	
	R/W				SIK11	0	Enable	Disable	
					SIK10	0	Enable	Disable	
FF25H	K13	K12	K11	K10	K13	– *2	High	Low	K10–K13 input port data
					K12	– *2	High	Low	
	R				K11	– *2	High	Low	
					K10	– *2	High	Low	
FF26H	KCP13	KCP12	KCP11	KCP10	KCP13	1	↓	↑	K10–K13 input comparison register
					KCP12	1	↓	↑	
	R/W				KCP11	1	↓	↑	
					KCP10	1	↓	↑	
FFE4H	0	0	0	EIK0	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R			R/W	0 *3	– *2			Unused
					EIK0	0	Enable	Mask	Interrupt mask register (K00–K03)
FFE5H	0	0	0	EIK1	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R			R/W	0 *3	– *2			Unused
					EIK1	0	Enable	Mask	Interrupt mask register (K10–K13)
FFF4H	0	0	0	IK0	0 *3	– *2	(R)	(R)	Unused
					0 *3	– *2	Yes	No	Unused
	R			R/W	0 *3	– *2	(W)	(W)	Unused
					IK0	0	Reset	Invalid	Interrupt factor flag (K00–K03)
FFF5H	0	0	0	IK1	0 *3	– *2	(R)	(R)	Unused
					0 *3	– *2	Yes	No	Unused
	R			R/W	0 *3	– *2	(W)	(W)	Unused
					IK1	0	Reset	Invalid	Interrupt factor flag (K10–K13)

*1 Initial value at initial reset

*2 Not set in the circuit

*3 Constantly "0" when being read

K00–K03: K0 port input port data (FF21H)
K10–K13: K1 port input port data (FF25H)

Input data of the input port terminals can be read with these registers.

When "1" is read: High level
When "0" is read: Low level
Writing: Invalid

The reading is "1" when the terminal voltage of the eight bits of the input ports (K00–K03, K10–K13) goes high (VDD), and "0" when the voltage goes low (VSS).
These bits are dedicated for reading, so writing cannot be done.

SIK00–SIK03: K0 port interrupt selection register (FF20H)
SIK10–SIK13: K1 port interrupt selection register (FF24H)

Selects the ports to be used for the K00–K03 and K10–K13 input interrupts.

When "1" is written: Enable
When "0" is written: Disable
Reading: Valid

Enables the interrupt for the input ports (K00–K03, K10–K13) for which "1" has been written into the interrupt selection registers (SIK00–SIK03, SIK10–SIK13). The input port set for "0" does not affect the interrupt generation condition.
At initial reset, these registers are set to "0".

KCP00–KCP03: K0 port input comparison register (FF22H)
KCP10–KCP13: K1 port input comparison register (FF26H)

Interrupt conditions for terminals K00–K03 and K10–K13 can be set with these registers.

When "1" is written: Falling edge
When "0" is written: Rising edge
Reading: Valid

The interrupt conditions can be set for the rising or falling edge of input for each of the eight bits (K00–K03 and K10–K13), through the input comparison registers (KCP00–KCP03 and KCP10–KCP13).
For KCP00–KCP03, a comparison is done only with the ports that are enabled by the interrupt among K00–K03 by means of the SIK00–SIK03 registers. For KCP10–KCP13, a comparison is done only with the ports that are enabled by the interrupt among K10–K13 by means of the SIK10–SIK13 registers.
At initial reset, these registers are set to "0".

EIK0: K0 input interrupt mask register (FFE4H•D0)
EIK1: K1 input interrupt mask register (FFE5H•D0)

Masking the interrupt of the input port can be selected with these registers.

When "1" is written: Enable
When "0" is written: Mask
Reading: Valid

With these registers, masking of the input port interrupt can be selected for each of the two systems (K00–K03, K10–K13).
At initial reset, these registers are set to "0".

IK0: K0 input interrupt factor flag (FFF4H•D0)
IK1: K1 input interrupt factor flag (FFF5H•D0)

These flags indicate the occurrence of input interrupt.

When "1" is read: Interrupt has occurred
When "0" is read: Interrupt has not occurred

When "1" is written: Flag is reset
When "0" is written: Invalid

The interrupt factor flags IK0 and IK1 are associated with K00–K03 and K10–K13, respectively. From the status of these flags, the software can decide whether an input interrupt has occurred.
The interrupt factor flag is set to "1" when the interrupt condition is established regardless of the interrupt mask register setting. However, the interrupt does not occur to the CPU when the interrupt is masked.
These flags are reset to "0" by writing "1" to them.
After an interrupt occurs, the same interrupt will occur again if the interrupt enabled state (I flag = "1") is set or the RETI instruction is executed unless the interrupt factor flag is reset. Therefore, be sure to reset (write "1" to) the interrupt factor flag in the interrupt service routine before shifting to the interrupt enabled state.
At initial reset, these flags are set to "0".

4.5.5 Programming notes

(1) When input ports are changed from low to high by pull-up resistors, the rise of the waveform is delayed on account of the time constant of the pull-up resistor and input gate capacitance. Hence, when fetching input ports, set an appropriate waiting time.
Particular care needs to be taken of the key scan during key matrix configuration.
Make this waiting time the amount of time or more calculated by the following expression.
$10 \times C \times R$
C: terminal capacitance 5 pF + parasitic capacitance ? pF
R: pull-up resistance 300 kΩ

(2) The K13 terminal functions as the clock input terminal for the programmable timer, and the input signal is shared with the input port and the programmable timer. Therefore, when the K13 terminal is set to the clock input terminal for the programmable timer, take care of the interrupt setting.

(3) After an interrupt occurs, the same interrupt will occur again if the interrupt enabled state (I flag = "1") is set or the RETI instruction is executed unless the interrupt factor flag is reset. Therefore, be sure to reset (write "1" to) the interrupt factor flag in the interrupt service routine before shifting to the interrupt enabled state.

4.6 Output Ports (R00–R03 and R10–R13)

4.6.1 Configuration of output ports

The E0C63B08 has 8 bits general output ports.
Output specifications of the output ports can be selected individually with the mask option. Two kinds of output specifications are available: complementary output and N-channel open drain output.
Figure 4.6.1.1 shows the configuration of the output port.

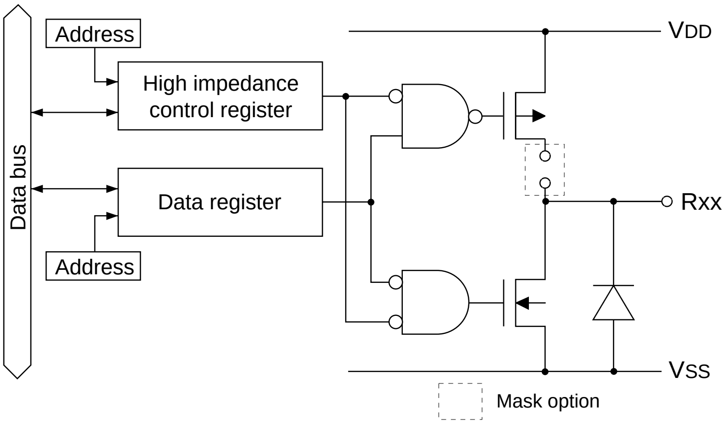


Fig. 4.6.1.1 Configuration of output port

The R02 and R03 output terminals are shared with special output terminals (TOUT, FOUT), and this function is selected by the software.
At initial reset, these are all set to the general purpose output port.
Table 4.6.1.1 shows the setting of the output terminals by function selection.

Table 4.6.1.1 Function setting of output terminals

Terminal name	Terminal status at initial reset	Special output	
		TOUT	FOUT
R00	R00 (High output)	R00	R00
R01	R01 (High output)	R01	R01
R02	R02 (High output)	TOUT	
R03	R03 (High output)		FOUT
R10–R13	R10–R13 (High output)	R10–R13	R10–R13

When using the output port (R02, R03) as the special output port, the data register must be fixed at "1" and the high impedance control register must be fixd at "0" (data output).

4.6.2 Mask option

Output specifications of the output ports can be selected with the mask option.
The output specifications of the output ports R00–R03 can be selected from either complementary output or N-channel open drain output individually (in 1-bit units), and for 4 bits of the output ports R10–R13, it can be selected in mass.
This mask option is effective even when the output port (R02, R03) is used for special output port.

4.6.3 High impedance control

The terminal output status of the output ports can be set to a high impedance status. This control is done using the high impedance control registers.
The high impedance control registers are provided to correspond with the output ports as shown below.

High impedance control register	Corresponding output port
R00HIZ	R00 (1-bit)
R01HIZ	R01 (1-bit)
R02HIZ	R02 (1-bit)
R03HIZ	R03 (1-bit)
R1HIZ	R10–R13 (4-bit)

When "1" is written to the high impedance control register, the corresponding output port terminal goes into high impedance status. When "0" is written, the port outputs a signal according to the data register.

4.6.4 Special output

In addition to the regular DC output, special output can be selected for the output ports R02 and R03 as shown in Table 4.6.4.1 with the software.
Figure 4.6.4.1 shows the configuration of the R02 and R03 output ports.

Table 4.6.4.1 Special output

Terminal	Special output	Output control register
R03	FOUT	FOUTE
R02	TOUT	PTOUT

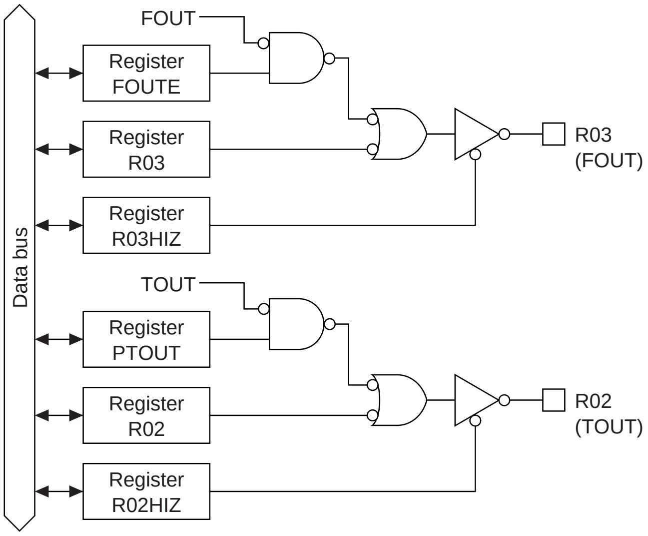


Fig. 4.6.4.1 Configuration of R02 and R03 output ports

At initial reset, the output port data register is set to "1" and the high impedance control register is set to "0". Consequently, the output terminal goes high (VDD).
When using the output port (R02, R03) as the special output port, fix the data register (R02, R03) at "1" and the high impedance control register (R02HIZ, R03HIZ) at "0" (data output). The respective signal should be turned ON and OFF using the special output control register.

Note:
- *Be aware that the output terminal is fixed at a low (VSS) level the same as the DC output if "0" is written to the R02 and R03 registers when the special output has been selected.*
- *Be aware that the output terminal shifts into high impedance status when "1" is written to the high impedance control register (R02HIZ, R03HIZ).*

- **TOUT (R02)**

The R02 terminal can output a TOUT signal.
The TOUT signal is the clock that is output from the programmable timer, and can be used to provide a clock signal to an external device.
To output the TOUT signal, fix the R02 register at "1" and the R02HIZ register at "0", and turn the signal ON and OFF using the PTOUT register. It is, however, necessary to control the programmable timer.
Refer to Section 4.11, "Programmable Timer" for details of the programmable timer.

Note: A hazard may occur when the TOUT signal is turned ON and OFF.

Figure 4.6.4.2 shows the output waveform of the TOUT signal.

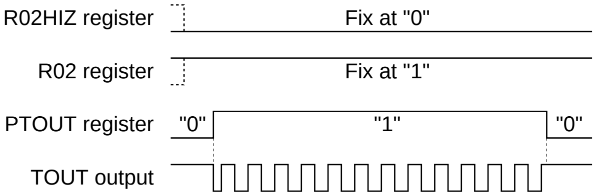


Fig. 4.6.4.2 Output waveform of TOUT signal

- **FOUT (R03)**

The R03 terminal can output a FOUT signal.
The FOUT signal is a clock (f_{OSC1} or f_{OSC3}) that is output from the oscillation circuit or a clock that the f_{OSC1} clock has divided in the internal circuit, and can be used to provide a clock signal to an external device.
To output the FOUT signal, fix the R03 register at "1" and the R03HIZ register at "0", and turn the signal ON and OFF using the FOUTE register.
The frequency of the output clock may be selected from among 4 types shown in Table 4.6.4.2 by setting the FOFQ0 and FOFQ1 registers.

Table 4.6.4.2 FOUT clock frequency

FOFQ1	FOFQ0	Clock frequency		
		f_{OSC1}=32.768 kHz	f_{OSC1}=76.8 kHz	f_{OSC1}=153.6 kHz
1	1	f_{OSC3}	f_{OSC3}	f_{OSC3}
1	0	f_{OSC1}	f_{OSC1}	f_{OSC1}
0	1	$f_{OSC1} \times 1/8$	$f_{OSC1} \times 1/16$	$f_{OSC1} \times 1/32$
0	0	$f_{OSC1} \times 1/64$	$f_{OSC1} \times 1/128$	$f_{OSC1} \times 1/256$

f_{OSC1}: Clock that is output from the OSC1 oscillation circuit
f_{OSC3}: Clock that is output from the OSC3 oscillation circuit

When f_{OSC3} is selected for the FOUT signal frequency, it is necessary to control the OSC3 oscillation circuit and the oscillation system voltage regulator before output.
Refer to Section 4.4, "Oscillation Circuit", for the control and notes.

Note: A hazard may occur when the FOUT signal is turned ON and OFF.

Figure 4.6.4.3 shows the output waveform of the FOUT signal.

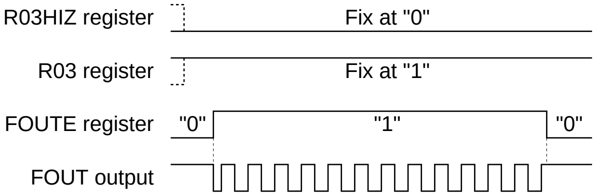


Fig. 4.6.4.3 Output waveform of FOUT signal

4.6.5 I/O memory of output ports

Table 4.6.5.1 shows the I/O addresses and control bits for the output ports.

Table 4.6.5.1 Control bits of output ports

Address	Register								Comment
	D3	D2	D1	D0	Name	Init *1	1	0	
FF06H	FOUTE	0	FOFQ1	FOFQ0	FOUTE	0	Enable	Disable	FOUT output enable
	R/W	R	R/W		0 *3	– *2			Unused
					FOFQ1	0			FOUT frequency selection [FOFQ1, 0] 0 1 2 3 f_{OSC1}=32kHz f_{OSC1}/64 f_{OSC1}/8 f_{OSC1} f_{OSC3} f_{OSC1}=76kHz f_{OSC1}/128 f_{OSC1}/16 f_{OSC1} f_{OSC3} f_{OSC1}=153kHz f_{OSC1}/256 f_{OSC1}/32 f_{OSC1} f_{OSC3}
					FOFQ0	0			
FF30H	R03HIZ	R02HIZ	R01HIZ	R00HIZ	R03HIZ	0	High-Z	Output	R03 output high impedance control (FOUTE=0) FOUT output high impedance control (FOUTE=1)
	R/W				R02HIZ	0	High-Z	Output	R02 output high impedance control (PTOUT=0) TOUT output high impedance control (PTOUT=1)
					R01HIZ	0	High-Z	Output	R01 output high impedance control
					R00HIZ	0	High-Z	Output	R00 output high impedance control
FF31H	R03	R02	R01	R00	R03	1	High	Low	R03 output port data (FOUTE=0) Fix at "1" when FOUT is used
	R/W				R02	1	High	Low	R02 output port data (PTOUT=0) Fix at "1" when TOUT is used
					R01	1	High	Low	R01 output port data
					R00	1	High	Low	R00 output port data
FF32H	0	0	0	R1HIZ	0 *3	– *2			Unused
	R			R/W	0 *3	– *2			Unused
					0 *3	– *2			Unused
					R1HIZ	0	High-Z	Output	R1 output high impedance control
FF33H	R13	R12	R11	R10	R13	1	High	Low	R10–R13 output port data
	R/W				R12	1	High	Low	
					R11	1	High	Low	
					R10	1	High	Low	
FFC1H	CHSEL	PTOUT	CKSEL1	CKSEL0	CHSEL	0	Timer 1	Timer 0	TOUT output channel selection
	R/W				PTOUT	0	On	Off	TOUT output control
					CKSEL1	0	OSC3	OSC1	Prescaler 1 source clock selection
					CKSEL0	0	OSC3	OSC1	Prescaler 0 source clock selection

*1 Initial value at initial reset

*2 Not set in the circuit

*3 Constantly "0" when being read

R00HIZ–R03HIZ: R0 port high impedance control register (FF30H)
R1HIZ: R1 port high impedance control register (FF32H•D0)

Controls high impedance output of the output port.

When "1" is written: High impedance
When "0" is written: Data output
Reading: Valid

By writing "0" to the high impedance control register, the corresponding output terminal outputs according to the data register. When "1" is written, it shifts into high impedance status.
When the output ports R02 and R03 are used for special output (TOUT, FOUT), fix the R02HIZ register and the R03HIZ register at "0" (data output).
At initial reset, these registers are set to "0".

R00–R03: R0 output port data register (FF31H)
R10–R13: R1 output port data register (FF33H)

Set the output data for the output ports.

When "1" is written: High level output
When "0" is written: Low level output
Reading: Valid

The output port terminals output the data written in the corresponding data registers without changing it. When "1" is written to the register, the output port terminal goes high (V_{DD}), and when "0" is written, the output port terminal goes low (V_{SS}).

When the output ports R02 and R03 are used for special output (TOUT, FOUT), fix the R02 register and the R03 register at "1".
At initial reset, these registers are all set to "1".

FOUTE: FOUT output control register (FF06H•D3)

Controls the FOUT output.

When "1" is written: FOUT output ON
When "0" is written: FOUT output OFF
Reading: Valid

By writing "1" to the FOUTE register when the R03 register has been set to "1" and the R03HIZ register has been set to "0", an FOUT signal is output from the R03 terminal. When "0" is written, the R03 terminal goes high (V_{DD}).
When using the R03 output port for DC output, fix this register at "0".
At initial reset, this register is set to "0".

FOFQ0, FOFQ1: FOUT frequency selection register (FF06H•D0, D1)

Selects a frequency of the FOUT signal.

Table 4.6.5.2 FOUT clock frequency

FOFQ1	FOFQ0	Clock frequency		
		f_{OSC1}=32.768 kHz	f_{OSC1}=76.8 kHz	f_{OSC1}=153.6 kHz
1	1	f_{OSC3}	f_{OSC3}	f_{OSC3}
1	0	f_{OSC1}	f_{OSC1}	f_{OSC1}
0	1	$f_{OSC1} \times 1/8$	$f_{OSC1} \times 1/16$	$f_{OSC1} \times 1/32$
0	0	$f_{OSC1} \times 1/64$	$f_{OSC1} \times 1/128$	$f_{OSC1} \times 1/256$

At initial reset, this register is set to "0".

PTOUT: TOUT output control register (FFC1H•D2)

Controls the TOUT output.

When "1" is written: TOUT output ON
When "0" is written: TOUT output OFF
Reading: Valid

By writing "1" to the PTOUT register when the R02 register has been set to "1" and the R02HIZ register has been set to "0", the TOUT signal is output from the R02 terminal. When "0" is written, the R02 terminal goes high (V_{DD}).
When using the R02 output port for DC output, fix this register at "0".
At initial reset, this register is set to "0".

4.6.6 Programming notes

(1) When using the output port (R02, R03) as the special output port, fix the data register (R02, R03) at "1" and the high impedance control register (R02HIZ, R03HIZ) at "0" (data output).
Be aware that the output terminal is fixed at a low (V_{SS}) level the same as the DC output if "0" is written to the R02 and R03 registers when the special output has been selected.
Be aware that the output terminal shifts into high impedance status when "1" is written to the high impedance control register (R02HIZ, R03HIZ).

(2) A hazard may occur when the FOUT signal and the TOUT signal are turned ON and OFF.

(3) When f_{OSC3} is selected for the FOUT signal frequency, it is necessary to control the OSC3 oscillation circuit and the oscillation system voltage regulator before output.
Refer to Section 4.4, "Oscillation Circuit", for the control and notes.

4.7 I/O Ports (P00–P03, P10–P13 and P20–P23)

4.7.1 Configuration of I/O ports

The E0C63B08 has 12 bits general-purpose I/O ports. Figure 4.7.1.1 shows the configuration of the I/O port.

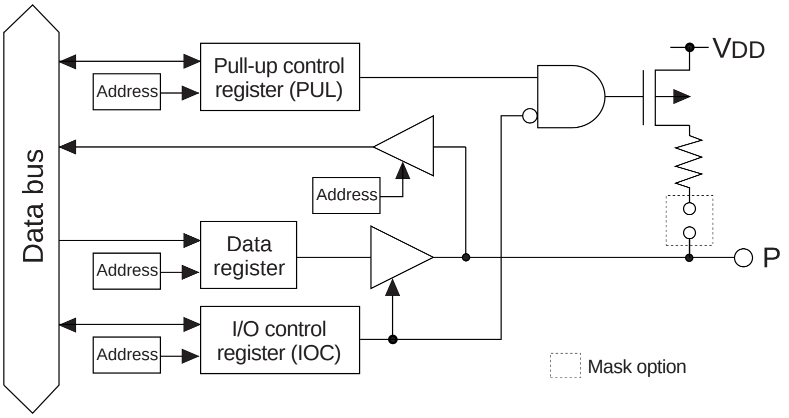


Fig. 4.7.1.1 Configuration of I/O port

The P10–P13 I/O port terminals are shared with the serial interface input/output terminals and this function is selected by the software.

At initial reset, these are all set to the I/O port.

Table 4.7.1.1 shows the setting of the input/output terminals by function selection.

Table 4.7.1.1 Function setting of input/output terminals

Terminal name	Terminal status at initial reset	Serial I/F	
		Master	Slave
P00–P03	P00–P03 (Input & pull-up ∗)	P00–P03	P00–P03
P10	P10 (Input & pull-up ∗)	SIN(I)	SIN(I)
P11	P11 (Input & pull-up ∗)	SOUT(O)	SOUT(O)
P12	P12 (Input & pull-up ∗)	$\overline{\text{SCLK}}$(O)	$\overline{\text{SCLK}}$(I)
P13	P13 (Input & pull-up ∗)	P13	$\overline{\text{SRDY}}$(O)
P20–P23	P20–P23 (Input & pull-up ∗)	P20–P23	P20–P23

∗ When "with pull-up resistor" is selected by the mask option
(high impedance when "gate direct" is set)

When these ports are used as I/O ports, the ports can be set to either input mode or output mode (in 1-bit unit). Modes can be set by writing data to the I/O control registers.

Refer to Section 4.12, "Serial Interface", for control of the serial interface.

4.7.2 Mask option

Output specification for the output mode and addition of pull-up resistors can be selected as the terminal specification of the I/O port. Three selection items are available: complementary output, N-channel open drain output (with pull-up) and N-channel open drain output (without pull-up). They are selected in 1-bit units or 4-bit units depending on the terminal group.

Ports to be selected in 1-bit units: P20, P21, P22, P23
Ports to be selected in 4-bit units: P00–P03, P10–P13

When N-channel open drain output (with pull-up) is selected, do not apply a voltage exceeding the power supply voltage to the port.
When N-channel open drain output (without pull-up) is selected, a voltage within the ruled range (see Chapter 7, "Electrical Characteristics") can be applied to the port. However, take care that the floating status does not occur during input mode.

This option is effective even when I/O ports (P10–P13) are used for input/output of the serial interface.

4.7.3 I/O control registers and input/output mode

Input or output mode can be set for the I/O ports by writing data into the corresponding I/O control registers IOCxx.

To set the input mode, write "0" to the I/O control register. When an I/O port is set to input mode, it becomes high impedance status and works as an input port.
However, when the pull-up explained in the following section has been set by software, the input line is pulled up only during this input mode.

To set the output mode, write "1" is to the I/O control register. When an I/O port is set to output mode , it works as an output port, it outputs a high level (VDD) when the port output data is "1", and a low level (VSS) when the port output data is "0".

If perform the read out in each mode; when output mode, the register value is read out, and when input mode, the port value is read out.

At initial reset, the I/O control registers are set to "0", and the I/O ports enter the input mode.

The I/O control registers of the ports that are set as input/output for the serial interface can be used as general purpose registers that do not affect the I/O control. (See Table 4.7.1.1.)

4.7.4 Pull-up during input mode

A pull-up resistor that operates during the input mode is built into each I/O port of the E0C63B08. Mask option can set the use or non-use of this pull-up. The pull-up resistor becomes effective by writing "1" to the pull-up control register PULxx that corresponds to each port, and the input line is pulled up during the input mode. When "0" has been written, no pull-up is done.
At initial reset, the pull-up control registers are set to "1".
The pull-up control registers of the ports in which "without pull-up" have been selected can be used as general purpose registers. Even when "with pull-up" has been selected, the pull-up control registers of the ports, that are set as input/output for the serial interface, can be used as general purpose registers that do not affect the pull-up control. (See Table 4.7.1.1.)
The pull-up control registers of the port, that are set as input for the serial interface, function the same as the I/O port.

4.7.5 I/O memory of I/O ports

Table 4.7.5.1 show the I/O addresses and the control bits for the I/O ports.

Table 4.7.5.1 Control bits of I/O ports

Address	Register								Comment
	D3	D2	D1	D0	Name	Init *1	1	0	
FF40H	IOC03	IOC02	IOC01	IOC00	IOC03	0	Output	Input	P00–P03 I/O control register
					IOC02	0	Output	Input	
	R/W				IOC01	0	Output	Input	
					IOC00	0	Output	Input	
FF41H	PUL03	PUL02	PUL01	PUL00	PUL03	1	On	Off	P00–P03 pull-up control register
					PUL02	1	On	Off	
	R/W				PUL01	1	On	Off	
					PUL00	1	On	Off	
FF42H	P03	P02	P01	P00	P03	– *2	High	Low	P00–P03 I/O port data
					P02	– *2	High	Low	
	R/W				P01	– *2	High	Low	
					P00	– *2	High	Low	
FF44H	IOC13	IOC12	IOC11	IOC10	IOC13	0	Output	Input	P13 I/O control register functions as a general-purpose register when SIF (slave) is selected
					IOC12	0	Output	Input	P12 I/O control register (ESIF=0) functions as a general-purpose register when SIF is selected
	R/W				IOC11	0	Output	Input	P11 I/O control register (ESIF=0) functions as a general-purpose register when SIF is selected
					IOC10	0	Output	Input	P10 I/O control register (ESIF=0) functions as a general-purpose register when SIF is selected
FF45H	PUL13	PUL12	PUL11	PUL10	PUL13	1	On	Off	P13 pull-up control register functions as a general-purpose register when SIF (slave) is selected
					PUL12	1	On	Off	P12 pull-up control register (ESIF=0) functions as a general-purpose register when SIF (master) is selected $\overline{\text{SCLK}}$ (I) pull-up control register when SIF (slave) is selected
	R/W				PUL11	1	On	Off	P11 pull-up control register (ESIF=0) functions as a general-purpose register when SIF is selected
					PUL10	1	On	Off	P10 pull-up control register (ESIF=0) SIN pull-up control register when SIF is selected
FF46H	P13	P12	P11	P10	P13	– *2	High	Low	P13 I/O port data functions as a general-purpose register when SIF (slave) is selected
					P12	– *2	High	Low	P12 I/O port data (ESIF=0) functions as a general-purpose register when SIF is selected
	R/W				P11	– *2	High	Low	P11 I/O port data (ESIF=0) functions as a general-purpose register when SIF is selected
					P10	– *2	High	Low	P10 I/O port data (ESIF=0) functions as a general-purpose register when SIF is selected
FF48H	IOC23	IOC22	IOC21	IOC20	IOC23	0	Output	Input	P20–P23 I/O control register
					IOC22	0	Output	Input	
	R/W				IOC21	0	Output	Input	
					IOC20	0	Output	Input	
FF49H	PUL23	PUL22	PUL21	PUL20	PUL23	1	On	Off	P20–P23 pull-up control register
					PUL22	1	On	Off	
	R/W				PUL21	1	On	Off	
					PUL20	1	On	Off	
FF4AH	P23	P22	P21	P20	P23	– *2	High	Low	P20–P23 I/O port data
					P22	– *2	High	Low	
					P21	– *2	High	Low	
					P20	– *2	High	Low	
FF70H	0	0	SCTRG	ESIF	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R		R/W		SCTRG	0	Trigger Run	Invalid Stop	Serial I/F clock trigger (writing) Serial I/F clock status (reading)
					ESIF	0	SIF	I/O	Serial I/F enable (P1 port function selection)

*1 Initial value at initial reset

*2 Not set in the circuit

*3 Constantly "0" when being read

ESIF: Serial interface enable register (FF70H•D0)

Selects function for P10–P13.

When "1" is written: Serial interface input/output port
When "0" is written: I/O port
Reading: Valid

When using the serial interface, write "1" to this register and when P10–P13 are used as the I/O port, write "0". The configuration of the terminals within P10–P13 that are used for the serial interface is decided by the mode selected with the SCS1 and SCS0 registers (see Section 4.12).
In the slave mode, all the P10–P13 ports are set to the serial interface input/output port. In the master mode, P10–P12 are set to the serial interface input/output port and P13 can be used as the I/O port.
At initial reset, this register is set to "0".

P00–P03: P0 I/O port data register (FF42H)
P10–P13: P1 I/O port data register (FF46H)
P20–P23: P2 I/O port data register (FF4AH)

I/O port data can be read and output data can be set through these registers.

- ***When writing data***

When "1" is written: High level
When "0" is written: Low level

When an I/O port is set to the output mode, the written data is output unchanged from the I/O port terminal. When "1" is written as the port data, the port terminal goes high (VDD), and when "0" is written, the terminal goes low (VSS).
Port data can be written also in the input mode.

- ***When reading data***

When "1" is read: High level
When "0" is read: Low level

The terminal voltage level of the I/O port is read out. When the I/O port is in the input mode the voltage level being input to the port terminal can be read out; in the output mode the register value can be read. When the terminal voltage is high (VDD) the port data that can be read is "1", and when the terminal voltage is low (VSS) the data is "0".
When "with pull-up resistor" has been selected with the mask option and the PUL register is set to "1", the built-in pull-up resister goes ON during input mode, so that the I/O port terminal is pulled up.

The data registers of the ports (P10–P12 or P10–P13) that are set as input/output for the serial interface can be used as general purpose registers that do not affect the input/output.

Note: When in the input mode, I/O ports are changed from low to high by pull-up resistor, the rise of the waveform is delayed on account of the time constant of the pull-up resistor and input gate capacitance. Hence, when fetching input ports, set an appropriate wait time.
Particular care needs to be taken of the key scan during key matrix configuration.
Make this waiting time the amount of time or more calculated by the following expression.
$10 \times C \times R$
C: terminal capacitance 5 pF + parasitic capacitance ? pF
R: pull-up resistance 300 kΩ

IOC00–IOC03: P0 port I/O control register (FF40H)
IOC10–IOC13: P1 port I/O control register (FF44H)
IOC20–IOC23: P2 port I/O control register (FF48H)

The input and output modes of the I/O ports are set with these registers.

When "1" is written: Output mode
When "0" is written: Input mode
Reading: Valid

The input and output modes of the I/O ports are set in 1-bit unit.
Writing "1" to the I/O control register makes the corresponding I/O port enter the output mode, and writing "0" induces the input mode.
At initial reset, these registers are all set to "0", so the I/O ports are in the input mode.
The I/O control registers of the ports (P10–P12 or P10–P13) that are set as input/output for the serial interface can be used as general purpose registers that do not affect the input/output.

PUL00–PUL03: P0 port pull-up control register (FF41H)
PUL10–PUL13: P1 port pull-up control register (FF45H)
PUL20–PUL23: P2 port pull-up control register (FF49H)

The pull-up during the input mode are set with these registers.

When "1" is written: Pull-up ON
When "0" is written: Pull-up OFF
Reading: Valid

The built-in pull-up resistor which is turned ON during input mode is set to enable in 1-bit units. (The pull-up resistor is included into the ports selected by the mask option.)
By writing "1" to the pull-up control register, the corresponding I/O ports are pulled up (during input mode), while writing "0" turns the pull-up function OFF.
At initial reset, these registers are all set to "1", so the pull-up function is set to ON.

The pull-up control registers of the ports in which the pull-up resistor is not included become the general purpose register. The registers of the ports that are set as input/output for the serial interface can also be used as general purpose registers that do not affect the pull-up control.
The pull-up control registers of the port that are set as input for the serial interface function the same as the I/O port.

4.7.6 Programming note

When in the input mode, I/O ports are changed from low to high by pull-up resistor, the rise of the waveform is delayed on account of the time constant of the pull-up resistor and input gate capacitance. Hence, when fetching input ports, set an appropriate wait time.
Particular care needs to be taken of the key scan during key matrix configuration.
Make this waiting time the amount of time or more calculated by the following expression.
$10 \times C \times R$

C: terminal capacitance 5 pF + parasitic capacitance ? pF
R: pull-up resistance 300 kΩ

4.8 LCD Driver (COM0–COM3, SEG0–SEG31)

4.8.1 Configuration of LCD driver

The E0C63B08 has 4 common terminals (COM0–COM3) and 32 segment terminals (SEG0–SEG31), so that it can drive an LCD with a maximum of 128 (32 × 4) segments.
The driving method is 1/4 duty, 1/3 duty or 1/2 duty dynamic drive with four voltages (1/3 bias), V_{SS}, V_{C1}, V_{C2} and V_{C3}. It is also possible to set static drive. The drive duty and static drive can be selected by software. In addition, drive waveform with three voltages (1/2 bias) of V_{SS}, $V_{C1} = V_{C2}$ and V_{C3} can be selected by mask option.

4.8.2 Power supply for LCD driving

The LCD drive voltage V_{C1} is generated by the LCD system regulated voltage circuit, and V_{C2} and V_{C3} are generated by boosting the V_{C1} voltage with the LCD system voltage booster circuit.
To generate V_{C1} when the supply voltage V_{DD} is 1.25 V or less, it is necessary to drive the LCD system voltage circuit in the doubler mode. When the supply voltage V_{DD} is 2.5 V or more, it is possible to drive in the halver mode.
Refer to Section 4.2, "Setting of Power Supply and Operating Mode", for setting operating modes such as the doubler mode.

The LCD system voltage circuit that generates V_{C1}–V_{C3} is turned ON and OFF by the LCD power control register LPWR.
By setting LPWR to "1", the LCD system voltage circuit generates V_{C1}–V_{C3}. When LPWR is set to "0", V_{C1}–V_{C3} becomes V_{SS} level. In this case, all outputs from the COM terminals and SEG terminals go to V_{SS} level.
To display the LCD, the LCD drive power must be ON by previously setting LPWR to "1".
SEG output ports that are set for DC output by the mask option operate same as the output (R) port regardless of the power ON/OFF control.

4.8.3 Control of LCD display and drive waveform

(1) Display ON/OFF control

The E0C63B08 incorporates the ALON and ALOFF registers to blink display. When "1" is written to ALON, all the segments go ON, and when "1" is written to ALOFF, all the segments go OFF. At such a time, an ON waveform or an OFF waveform is output from SEG terminals. When "0" is written to these registers, normal display is performed. Furthermore, when "1" is written to both of the ALON and ALOFF, ALON (all ON) has priority over the ALOFF (all OFF). At initial reset, both the registers are set to "0" (normal display). However, the LCD power is OFF at initial reset, so the display is actually performed when the LCD power is turned ON (LPWR = "1").

(2) Setting of drive duty

In the E0C63B08, the drive duty can be set to 1/4, 1/3 or 1/2 by the software. This setting is done using the LDUTY1 and LDUTY0 registers as shown in Table 4.8.3.1.

Table 4.8.3.1 LCD drive duty setting

LDUTY1	LDUTY0	Drive duty	Common terminal used	Maximum segment number	Frame frequency ∗
1	∗	1/2	COM0, COM1	64 (32 × 2)	32 Hz
0	1	1/3	COM0–COM2	96 (32 × 3)	42.7 Hz
0	0	1/4	COM0–COM3	128 (32 × 4)	32 Hz

∗ When f_{OSC1} = 32.768 kHz

Figures 4.8.3.1 to 4.8.3.6 show the dynamic drive waveform according to the drive bias and duty.

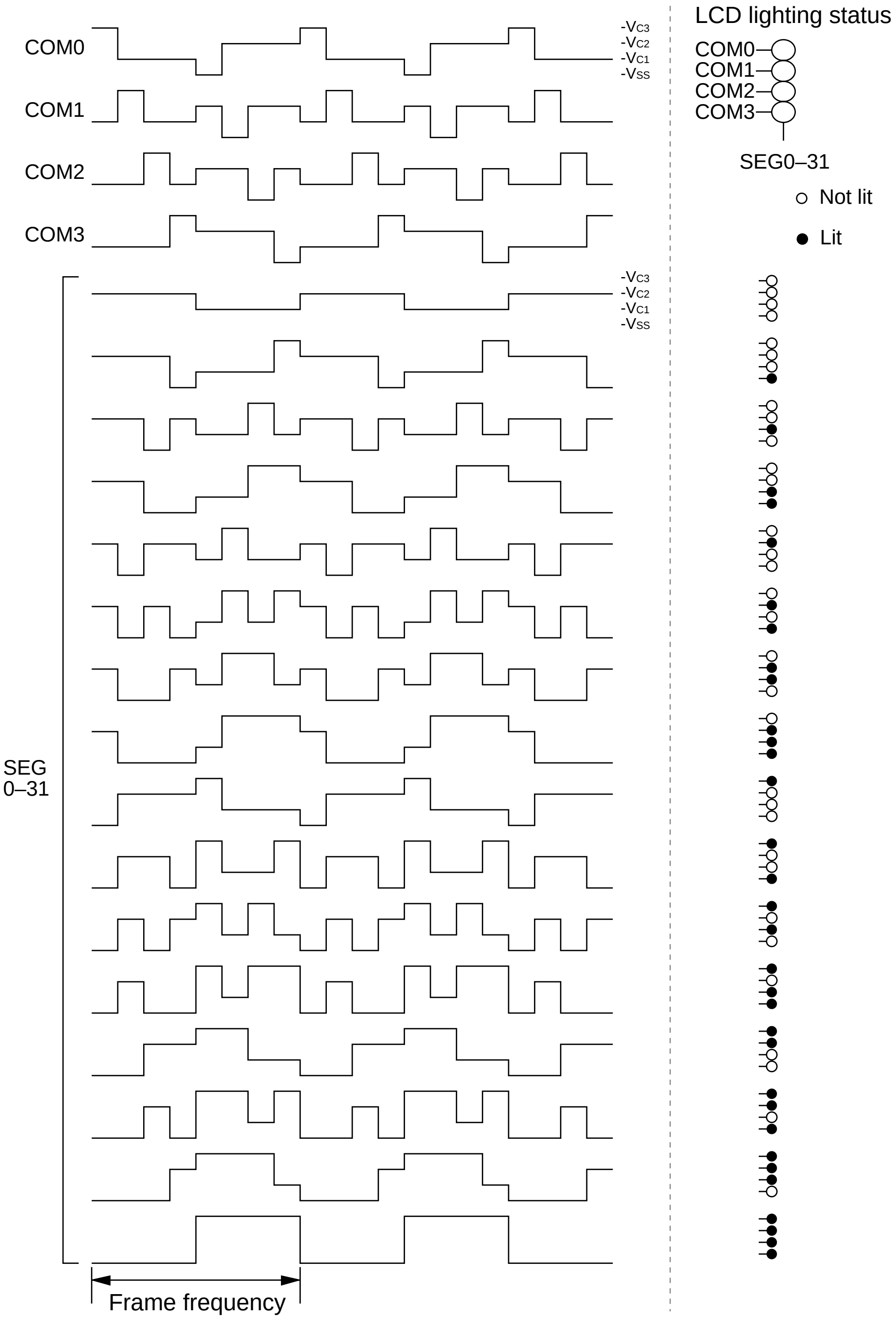


Fig. 4.8.3.1 Dynamic drive waveform for 1/4 duty (1/3 bias)

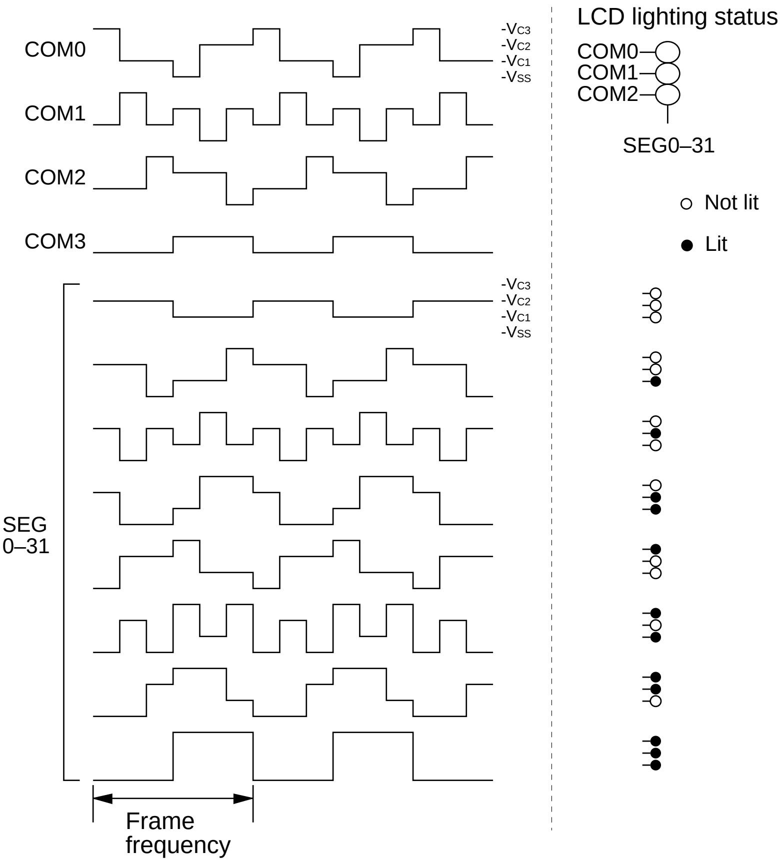


Fig. 4.8.3.2 Dynamic drive waveform for 1/3 duty (1/3 bias)

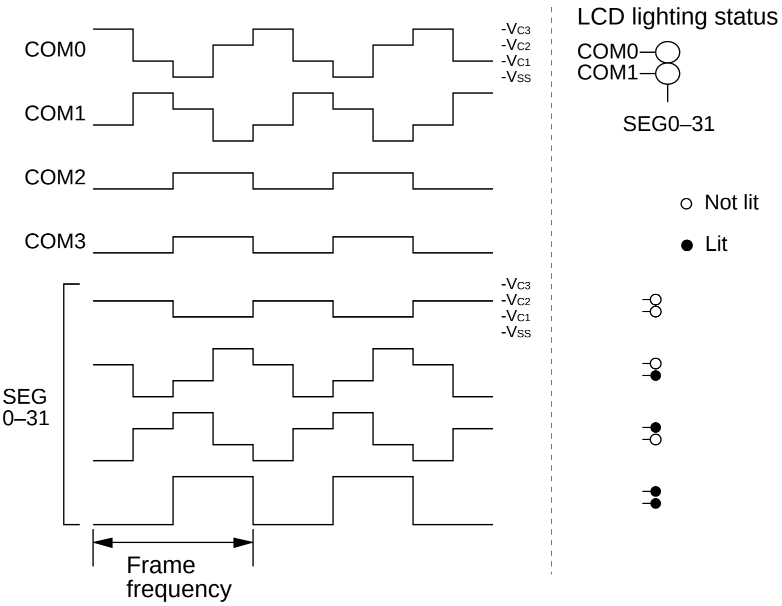


Fig. 4.8.3.3 Dynamic drive waveform for 1/2 duty (1/3 bias)

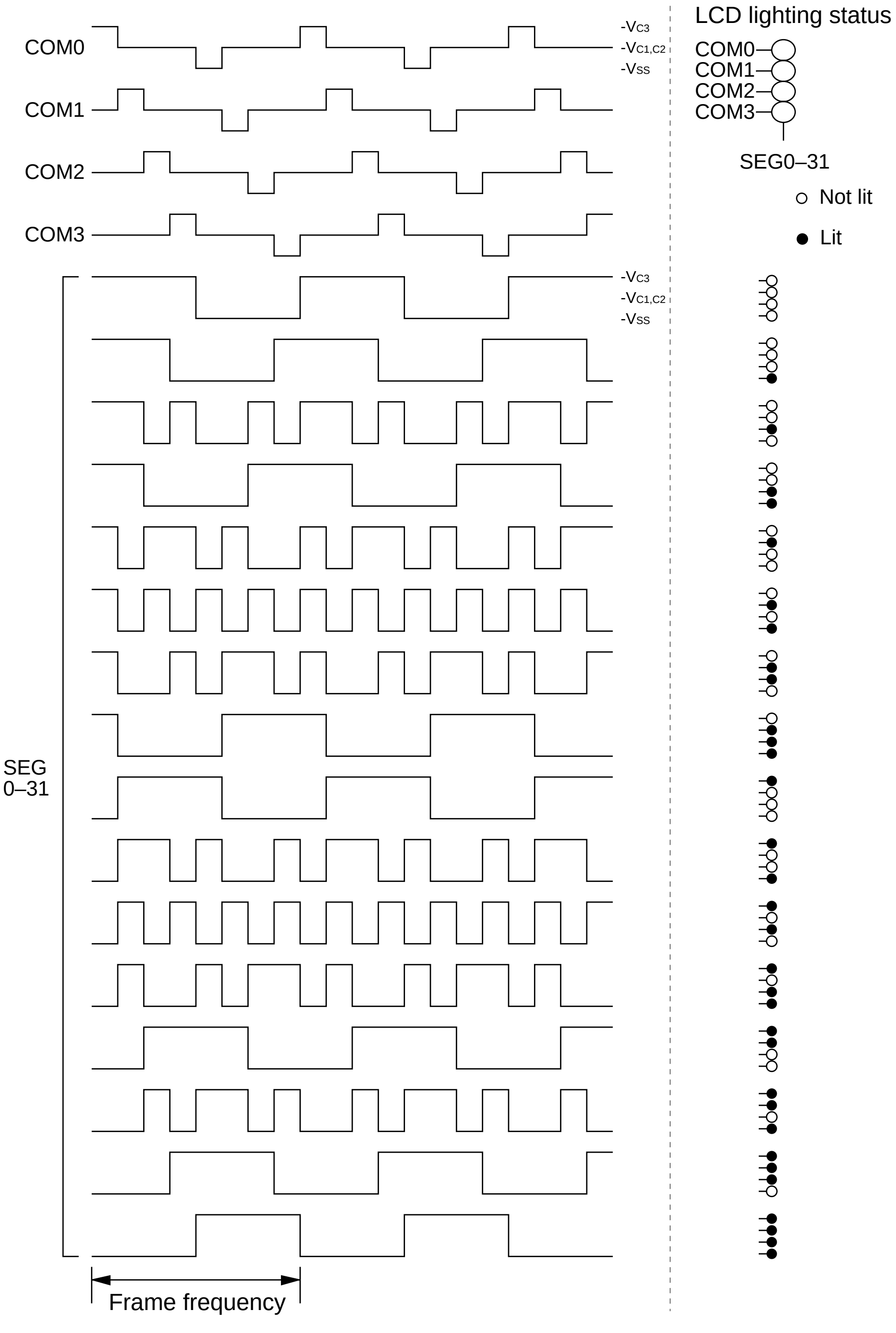


Fig. 4.8.3.4 Dynamic drive waveform for 1/4 duty (1/2 bias)

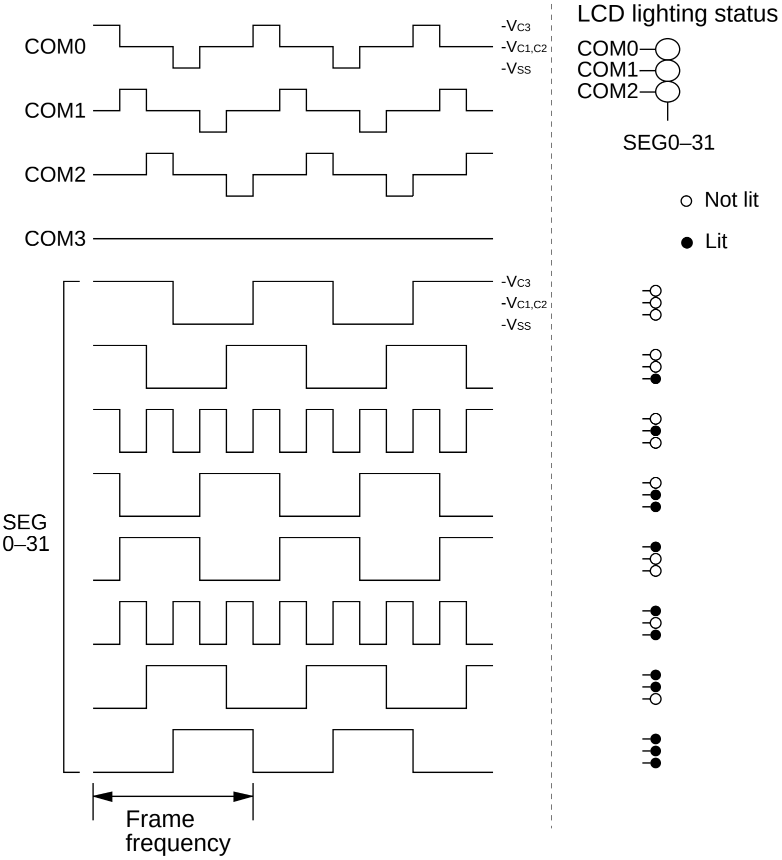


Fig. 4.8.3.5 Dynamic drive waveform for 1/3 duty (1/2 bias)

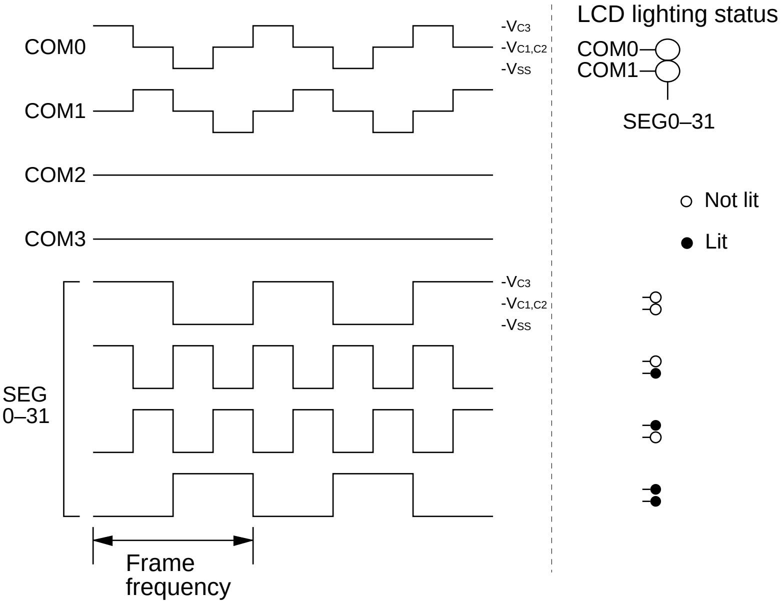


Fig. 4.8.3.6 Dynamic drive waveform for 1/2 duty (1/2 bias)

(3) Static drive

The E0C63B08 provides software setting of the LCD static drive.

To set in static drive, write "1" to the common output signal control register STCD. Then, by writing "1" to any one of COM0 to COM3 (display memory) corresponding to the SEG terminal, the SEG terminal outputs a static ON waveform. When all the COM0 to COM3 bits are set to "0", the SEG terminal outputs a dynamic OFF waveform.

Figures 4.8.3.7 and 4.8.3.8 show the static drive waveform for 1/3 bias and 1/2 bias.

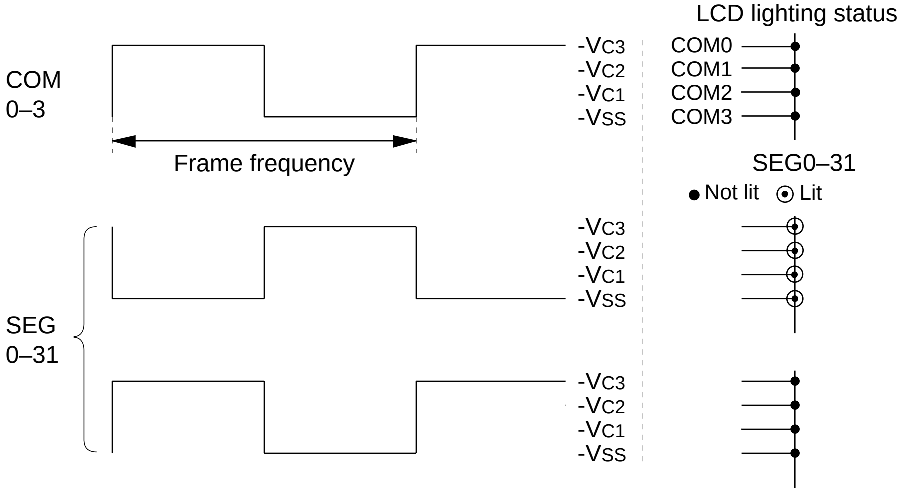


Fig. 4.8.3.7 Static drive waveform (1/3 bias)

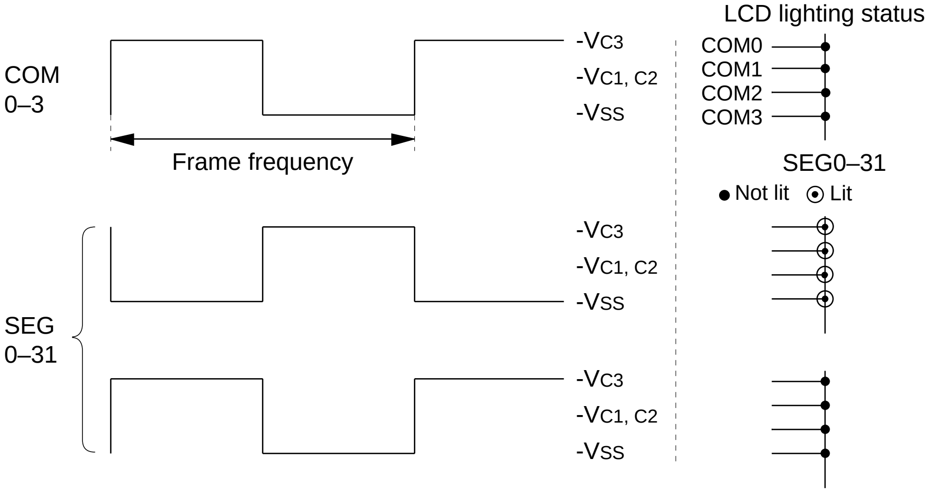


Fig. 4.8.3.8 Static drive waveform (1/2 bias)

4.8.4 Mask option

(1) Segment allocation

Up to 128 bits of the display memory can be selected from the data memory addresses F000H to F01FH.

The LCD driver has a segment decoder built-in, and the data bit (D0–D3) of the optional address in the display memory area (F000H–F01FH) can be allocated to the optional segment. This makes design easy by increasing the degree of freedom with which the liquid crystal panel can be designed.

The allocated segment displays when the bit for the display memory is set to "1", and goes out when bit is set to "0".

Figure 4.8.4.1 shows an example of the relationship between the LCD segments (on the panel) and the display memory for the case of 1/3 duty.

Address	Data			
	D3	D2	D1	D0
F00AH	d	c	b	a
F00BH	p	g	f	e
F00CH	d'	c'	b'	a'
F00DH	p'	g'	f'	e'

Display memory allocation

	Common 0	Common 1	Common 2
SEG10	F00A, D0 (a)	F00B, D1 (f)	F00B, D0 (e)
SEG11	F00A, D1 (b)	F00B, D2 (g)	F00A, D3 (d)
SEG12	F00D, D1 (f')	F00A, D2 (c)	F00B, D3 (p)

Pin address allocation

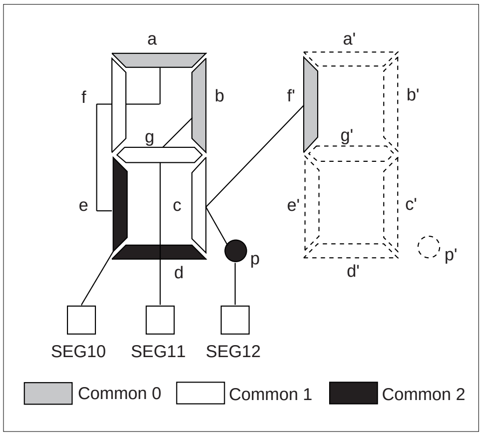


Fig. 4.8.4.1 Segment allocation

At initial reset, the contents of the display memory are undefined, therefore it is necessary to initialize by software. Since the display memory permits reading and writing, the addresses/bits that are not used on the LCD display can be used as general-purpose registers.

(2) Output specification

① The segment terminals (SEG0–SEG31) can be selected with the mask option in pairs∗ for either segment signal output or DC output (V_{DD} and V_{SS} binary output).
When DC output is selected, the data corresponding to COM0 of each segment terminal is output.

② When DC output is selected, either complementary output or N-channel open drain output can be selected for each terminal with the mask option.

∗ The terminal pairs are combination of SEG2 × n and SEG2 × n + 1 (where n is an integer from 0 to 15).

(3) LCD drive bias

The LCD drive method can be selected from a 1/3 bias drive (V_{SS}, V_{C1}, V_{C2}, V_{C3}) or a 1/2 bias drive (V_{SS}, $V_{C1} = V_{C2}$, V_{C3}).

4.8.5 I/O memory of LCD driver

Table 4.8.5.1 shows the I/O addresses and the control bits for the LCD driver. Figure 4.8.5.1 shows the display memory map.

Table 4.8.5.1 Control bits of LCD driver

Address	Register								Comment
	D3	D2	D1	D0	Name	Init *1	1	0	
FF60H	LDUTY1	LDUTY0	VCCHG	LPWR	LDUTY1	0			LCD drive duty switch [LDUTY1, 0] 0 1 2, 3 Duty 1/4 1/3 1/2
					LDUTY0	0			
	R/W				VCCHG	0			General-purpose register (reserved register)
					LPWR	0	On	Off	LCD power On/Off
FF61H	0	ALOFF	ALON	STCD	0 *3	– *2			Unused
					ALOFF	1	All Off	Normal	LCD all OFF control
	R	R/W			ALON	0	All On	Normal	LCD all ON control
					STCD	0	Static	Dynamic	Common output signal control

*1 Initial value at initial reset

*2 Not set in the circuit

*3 Constantly "0" when being read

Base address \ Low	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
F000	Display memory (32 words × 4 bits) R/W															
F010																

Fig. 4.8.5.1 Display memory map

LPWR: LCD power control (ON/OFF) register (FF60H•D0)

Turns the LCD system voltage circuit ON and OFF.

When "1" is written: ON
When "0" is written: OFF
Reading: Valid

When "1" is written to the LPWR register, the LCD system voltage circuit goes ON and generates the LCD drive voltage. When "0" is written, all the LCD drive voltages go to V_{SS} level.
It takes about 100 msec for the LCD drive voltage to stabilize after starting up the LCD system voltage circuit by writing "1" to the LPWR register.
This control does not affect to SEG terminals that have been set for DC output.
At initial reset, this register is set to "0".

LDUTY0, LDUTY1: LCD drive duty switching register (FF60H•D2, D3)

Selects the LCD drive duty.

Table 4.8.5.2 Drive duty setting

LDUTY1	LDUTY0	Drive duty	Common terminal used	Maximum segment number	Frame frequency *
1	*	1/2	COM0, COM1	64 (32 × 2)	32 Hz
0	1	1/3	COM0–COM2	96 (32 × 3)	42.7 Hz
0	0	1/4	COM0–COM3	128 (32 × 4)	32 Hz

* When f_{OSC1} = 32.768 kHz

At initial reset, this register is set to "0".

STCD: Common output signal control register (FF61H•D0)

Switches the LCD driving method.

When "1" is written: Static drive
When "0" is written: Dynamic drive
Reading: Valid

By writing "1" to STCD, static drive is selected, and dynamic drive is selected when "0" is written.
At initial reset, this register is set to "0".

ALON: LCD all ON control register (FF61H•D1)

Displays the all LCD segments ON.

When "1" is written: All LCD segments displayed
When "0" is written: Normal display
Reading: Valid

By writing "1" to the ALON register, all the LCD segments goes ON, and when "0" is written, it returns to normal display.
This function outputs an ON waveform to the SEG terminals, and segments not affect the content of the display memory.
ALON has priority over ALOFF.
At initial reset, this register is set to "0".

ALOFF: LCD all OFF control register (FF61H•D2)

Fade outs the all LCD segments.

When "1" is written: All LCD segments fade out
When "0" is written: Normal display
Reading: Valid

By writing "1" to the ALOFF register, all the LCD segments goes OFF, and when "0" is written, it returns to normal display.
This function outputs an OFF waveform to the SEG terminals, and does not affect the content of the display memory.
At initial reset, this register is set to "0".

Display memory (F000H–F01FH)

The LCD segments are lit or turned off depending on this data.

When "1" is written: Lit
When "0" is written: Not lit
Reading: Invalid

By writing data into the display memory allocated to the LCD segment (on the panel), the segment can be lit or put out.
At initial reset, the contents of the display memory are undefined, therefore it is necessary to initialize by software. Since the display memory permits reading and writing, the addresses/bits that are not used on the LCD display can be used as general-purpose registers.

4.8.6 Programming notes

(1) The contents of the display memory are undefined until the area is initialized (through, for instance, memory clear processing by the CPU). Initialize the display memory by executing initial processing.

(2) 100 msec or more time is necessary for stabilizing the LCD drive voltages V_{C1}, V_{C2} and V_{C3} after setting the LCD power control register LPWR to "1". Be careful of the segment-on right after the power is turned on.

4.9 Clock Timer

4.9.1 Configuration of clock timer

The E0C63B08 has a built-in clock timer that uses OSC1 (crystal oscillator) as the source oscillator. The clock timer is configured of an 8-bit binary counter that serves as the input clock, f_{OSC1} divided clock output from the prescaler. Timer data (128–16 Hz and 8–1 Hz) can be read out by the software.
Figure 4.9.1.1 is the block diagram for the clock timer.

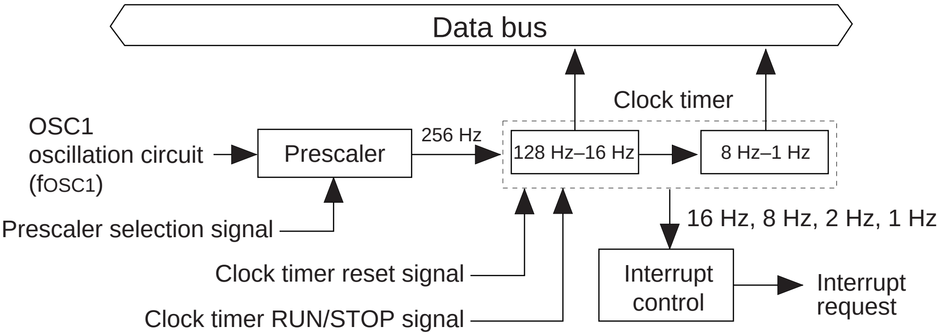


Fig. 4.9.1.1 Block diagram for the clock timer

Ordinarily, this clock timer is used for all types of timing functions such as clocks.
The clock timer uses the clock output from the prescaler. For this reason, the prescaler must be set correctly according to the frequency (32.768 kHz/76.8 kHz/153.6 kHz) of the crystal oscillator used for OSC1 oscillation (see Section 4.4, "Oscillation Circuit").

4.9.2 Data reading and hold function

The 8 bits timer data are allocated to the address FF79H and FF7AH.

<FF79H>	D0: TM0 = 128 Hz	D1: TM1 = 64 Hz	D2: TM2 = 32 Hz	D3: TM3 = 16 Hz
<FF7AH>	D0: TM4 = 8 Hz	D1: TM5 = 4 Hz	D2: TM6 = 2 Hz	D3: TM7 = 1 Hz

Since the clock timer data has been allocated to two addresses, a carry is generated from the low-order data within the count (TM0–TM3: 128–16 Hz) to the high-order data (TM4–TM7: 8–1 Hz). When this carry is generated between the reading of the low-order data and the high-order data, a content combining the two does not become the correct value (the low-order data is read as FFH and the high-order data becomes the value that is counted up 1 from that point).
The high-order data hold function in the E0C63B08 is designed to operate to avoid this. This function temporarily stops the counting up of the high-order data (by carry from the low-order data) at the point where the low-order data has been read and consequently the time during which the high-order data is held is the shorter of the two indicated here following.

1. Period until it reads the high-order data.
2. 0.48–1.5 msec ∗ (f_{OSC1} = 32.768 kHz)
   0.41–1.25 msec ∗ (f_{OSC1} = 76.8 kHz or 153.6 kHz) ∗ Varies due to the read timing

Note: Since the low-order data is not held when the high-order data has previously been read, the low-order data should be read first.

4.9.3 Interrupt function

The clock timer can cause interrupts at the falling edge of 16 Hz, 8 Hz, 2 Hz and 1 Hz signals. Software can set whether to mask any of these frequencies.
Figure 4.9.3.1 is the timing chart of the clock timer.

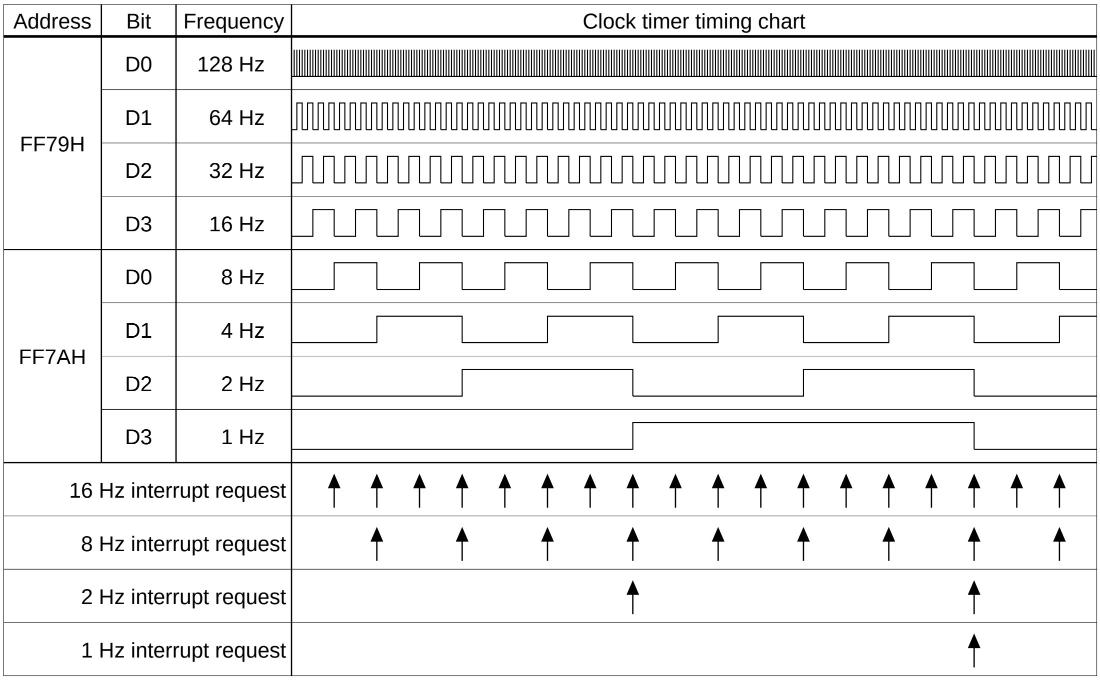


Fig. 4.9.3.1 Timing chart of clock timer

As shown in Figure 4.9.3.1, interrupt is generated at the falling edge of the frequencies (16 Hz, 8 Hz, 2 Hz, 1 Hz). At this time, the corresponding interrupt factor flag (IT0, IT1, IT2, IT3) is set to "1". Selection of whether to mask the separate interrupts can be made with the interrupt mask registers (EIT0, EIT1, EIT2, EIT3). However, regardless of the interrupt mask register setting, the interrupt factor flag is set to "1" at the falling edge of the corresponding signal.

4.9.4 I/O memory of clock timer

Table 4.9.4.1 shows the I/O addresses and the control bits for the clock timer.

Table 4.9.4.1 Control bits of clock timer

Address	Register								Comment
	D3	D2	D1	D0	Name	Init *1	1	0	
FF78H	0	0	TMRST	TMRUN	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R		W	R/W	TMRST*3	Reset	Reset	Invalid	Clock timer reset (writing)
					TMRUN	0	Run	Stop	Clock timer Run/Stop
FF79H	TM3	TM2	TM1	TM0	TM3	0			Clock timer data (16 Hz)
					TM2	0			Clock timer data (32 Hz)
	R				TM1	0			Clock timer data (64 Hz)
					TM0	0			Clock timer data (128 Hz)
FF7AH	TM7	TM6	TM5	TM4	TM7	0			Clock timer data (1 Hz)
					TM6	0			Clock timer data (2 Hz)
	R				TM5	0			Clock timer data (4 Hz)
					TM4	0			Clock timer data (8 Hz)
FFE6H	EIT3	EIT2	EIT1	EIT0	EIT3	0	Enable	Mask	Interrupt mask register (Clock timer 1 Hz)
					EIT2	0	Enable	Mask	Interrupt mask register (Clock timer 2 Hz)
	R/W				EIT1	0	Enable	Mask	Interrupt mask register (Clock timer 8 Hz)
					EIT0	0	Enable	Mask	Interrupt mask register (Clock timer 16 Hz)
FFF6H	IT3	IT2	IT1	IT0	IT3	0	(R)	(R)	Interrupt factor flag (Clock timer 1 Hz)
					IT2	0	Yes	No	Interrupt factor flag (Clock timer 2 Hz)
	R/W				IT1	0	(W)	(W)	Interrupt factor flag (Clock timer 8 Hz)
					IT0	0	Reset	Invalid	Interrupt factor flag (Clock timer 16 Hz)

*1 Initial value at initial reset

*2 Not set in the circuit

*3 Constantly "0" when being read

TM0–TM7: Timer data (FF79H, FF7AH)

The 128–1 Hz timer data of the clock timer can be read out with these registers. These eight bits are read only, and writing operations are invalid.

By reading the low-order data (FF79H), the high-order data (FF7AH) is held until reading or during the following time (one of shorter of them).

0.48–1.5 msec (f_{OSC1} = 32.768 kHz)
0.41–1.25 msec (f_{OSC1} = 38.4 kHz or 76.8 kHz)

At initial reset, the timer data is initialized to "00H".

TMRST: Clock timer reset (FF78H•D1)

This bit resets the clock timer.

When "1" is written: Clock timer reset
When "0" is written: No operation
Reading: Always "0"

The clock timer is reset by writing "1" to TMRST. When the clock timer is reset in the RUN status, operation restarts immediately. Also, in the STOP status the reset data is maintained. No operation results when "0" is written to TMRST.

This bit is write-only, and so is always "0" at reading.

TMRUN: Clock timer RUN/STOP control register (FF78H•D0)

Controls RUN/STOP of the clock timer.

When "1" is written: RUN
When "0" is written: STOP
Reading: Valid

The clock timer enters the RUN status when "1" is written to the TMRUN register, and the STOP status when "0" is written.
In the STOP status, the timer data is maintained until the next RUN status or the timer is reset. Also, when the STOP status changes to the RUN status, the data that is maintained can be used for resuming the count.
At initial reset, this register is set to "0".

EIT0: 16 Hz interrupt mask register (FFE6H•D0)
EIT1: 8 Hz interrupt mask register (FFE6H•D1)
EIT2: 2 Hz interrupt mask register (FFE6H•D2)
EIT3: 1 Hz interrupt mask register (FFE6H•D3)

These registers are used to select whether to mask the clock timer interrupt.

When "1" is written: Enabled
When "0" is written: Masked
Reading: Valid

The interrupt mask registers (EIT0, EIT1, EIT2, EIT3) are used to select whether to mask the interrupt to the separate frequencies (16 Hz, 8 Hz, 2 Hz, 1 Hz).
At initial reset, these registers are set to "0".

IT0: 16 Hz interrupt factor flag (FFF6H•D0)
IT1: 8 Hz interrupt factor flag (FFF6H•D1)
IT2: 2 Hz interrupt factor flag (FFF6H•D2)
IT3: 1 Hz interrupt factor flag (FFF6H•D3)

These flags indicate the status of the clock timer interrupt.

When "1" is read: Interrupt has occurred
When "0" is read: Interrupt has not occurred

When "1" is written: Flag is reset
When "0" is written: Invalid

The interrupt factor flags (IT0, IT1, IT2, IT3) correspond to the clock timer interrupts of the respective frequencies (16 Hz, 8 Hz, 2 Hz, 1 Hz). The software can judge from these flags whether there is a clock timer interrupt. However, even if the interrupt is masked, the flags are set to "1" at the falling edge of the signal.
These flags are reset to "0" by writing "1" to them.
After an interrupt occurs, the same interrupt will occur again if the interrupt enabled state (I flag = "1") is set or the RETI instruction is executed unless the interrupt factor flag is reset. Therefore, be sure to reset (write "1" to) the interrupt factor flag in the interrupt service routine before shifting to the interrupt enabled state.
At initial reset, these flags are set to "0".

4.9.5 Programming notes

(1) To operate the clock timer correctly, the prescaler must be set to suit the crystal oscillator used for the OSC1 oscillation circuit.

(2) Be sure to read timer data in the order of low-order data (TM0–TM3) then high-order data (TM4–TM7).

(3) After an interrupt occurs, the same interrupt will occur again if the interrupt enabled state (I flag = "1") is set or the RETI instruction is executed unless the interrupt factor flag is reset. Therefore, be sure to reset (write "1" to) the interrupt factor flag in the interrupt service routine before shifting to the interrupt enabled state.

4.10 Stopwatch Timer

4.10.1 Configuration of stopwatch timer

The E0C63B08 has 1/100 sec unit and 1/10 sec unit stopwatch timer built-in. The stopwatch timer is configured with a 2 levels 4-bit BCD counter which has an input clock approximating 100 Hz signal (signal divided from OSC1 to the closest 100 Hz) and data can be read in units of 4 bits by software.
Figure 4.10.1.1 shows the configuration of the stopwatch timer.

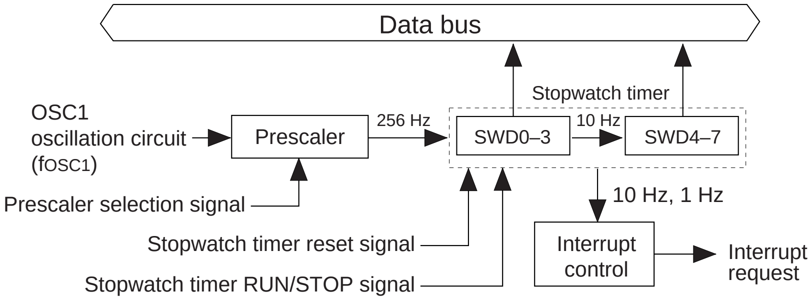


Fig. 4.10.1.1 Configuration of stopwatch timer

The stopwatch timer can be used as a separate timer from the clock timer. In particular, digital watch stopwatch functions can be realized easily with software.
The stopwatch timer uses the clock output from the prescaler. For this reason, the prescaler must be set correctly according to the frequency (32.768 kHz/76.8 kHz/153.6 kHz) of the crystal oscillator used for OSC1 oscillation (see Section 4.4, "Oscillation Circuit").

4.10.2 Count-up pattern

The stopwatch timer is configured of 4-bit BCD counters SWD0–SWD3 and SWD4–SWD7.
The counter SWD0–SWD3, at the stage preceding the stopwatch timer, has an approximated 100 Hz signal for the input clock. It counts up every 1/100 sec, and generates an approximated 10 Hz signal. The counter SWD4–SWD7 has an approximated 10 Hz signal generated by the counter SWD0–SWD3 for the input clock. In count-up every 1/10 sec, and generated 1 Hz signal.
Figure 4.10.2.1 shows the count-up pattern of the stopwatch timer.

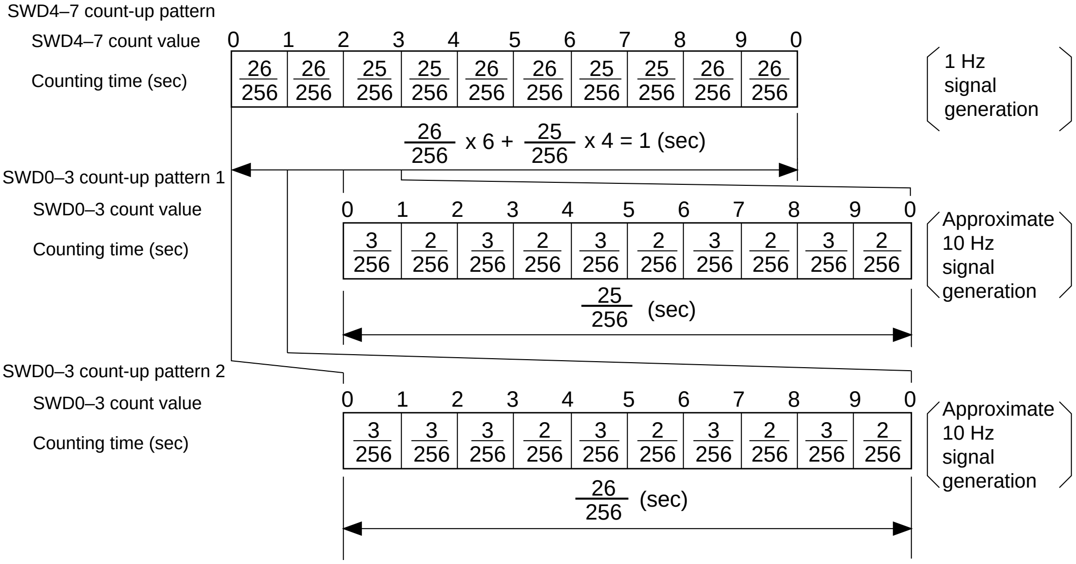


Fig. 4.10.2.1 Count-up pattern of stopwatch timer

SWD0–SWD3 generates an approximated 10 Hz signal from the basic 256 Hz signal (output from the prescaler). The count-up intervals are 2/256 sec and 3/256 sec, so that finally two patterns are generated: 25/256 sec and 26/256 sec intervals. Consequently, these patterns do not amount to an accurate 1/100 sec.
SWD4–SWD7 counts the approximated 10 Hz signals generated by the 25/256 sec and 26/256 sec intervals in the ratio of 4 : 6, to generate a 1 Hz signal. The count-up intervals are 25/256 sec and 26/256 sec, which do not amount to an accurate 1/10 sec.

4.10.3 Interrupt function

The stopwatch timers SWD0–SWD3 and SWD4–SWD7, through their respective overflows, can generate 10 Hz (approximate 10 Hz) and 1 Hz interrupts.
Figure 4.10.3.1 shows the timing chart for the stopwatch timer.

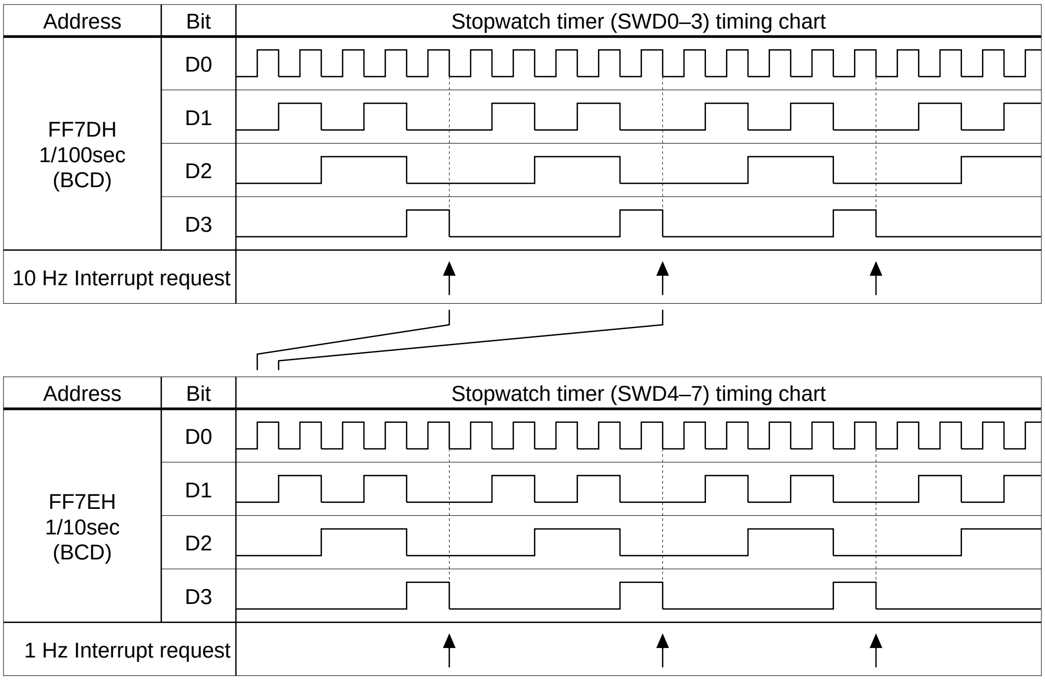


Fig. 4.10.3.1 Timing chart for stopwatch timer

The stopwatch interrupts are generated by the overflow of their respective counters SWD0–SWD3 and SWD4–SWD7 (changing "9" to "0"). At this time, the corresponding interrupt factor flags (ISW10 and ISW1) are set to "1".
The respective interrupts can be masked separately using the interrupt mask registers (EISW10 and EISW1). However, regardless of the setting of the interrupt mask registers, the interrupt factor flags are set to "1" by the overflow of their corresponding counters.

4.10.4 I/O memory of stopwatch timer

Table 4.10.4.1 shows the I/O addresses and the control bits for the stopwatch timer.

Table 4.10.4.1 Control bits of stopwatch timer

Address	Register								Comment
	D3	D2	D1	D0	Name	Init *1	1	0	
FF7CH	0	0	SWRST	SWRUN	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R		W	R/W	SWRST*3	Reset	Reset	Invalid	Stopwatch timer reset (writing)
					SWRUN	0	Run	Stop	Stopwatch timer Run/Stop
FF7DH	SWD3	SWD2	SWD1	SWD0	SWD3	0			Stopwatch timer data BCD (1/100 sec)
					SWD2	0			
	R				SWD1	0			
					SWD0	0			
FF7EH	SWD7	SWD6	SWD5	SWD4	SWD7	0			Stopwatch timer data BCD (1/10 sec)
					SWD6	0			
	R				SWD5	0			
					SWD4	0			
FFE7H	0	0	EISW1	EISW10	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R		R/W		EISW1	0	Enable	Mask	Interrupt mask register (Stopwatch timer 1 Hz)
					EISW10	0	Enable	Mask	Interrupt mask register (Stopwatch timer 10 Hz)
FFF7H	0	0	ISW1	ISW10	0 *3	– *2	(R)	(R)	Unused
					0 *3	– *2	Yes	No	Unused
	R		R/W		ISW1	0	(W)	(W)	Interrupt factor flag (Stopwatch timer 1 Hz)
					ISW10	0	Reset	Invalid	Interrupt factor flag (Stopwatch timer 10 Hz)

*1 Initial value at initial reset

*2 Not set in the circuit

*3 Constantly "0" when being read

SWD0–SWD7: Stopwatch timer data (FF7DH, FF7EH)

The 1/100 sec and the 1/10 sec data (BCD) can be read from SWD0–SWD3 and SWD4–SWD7, respectively. These eight bits are read only, and writing operations are invalid.
At initial reset, the timer data is initialized to "00H".

SWRST: Stopwatch timer reset (FF7CH•D1)

When "1" is written: Stopwatch timer reset
When "0" is written: No operation
Reading: Always "0"

The stopwatch timer is reset by writing "1" to SWRST. All timer data is set to "0". When the stopwatch timer is reset in the RUN status, operation restarts immediately. Also, in the STOP status the reset data is maintained. No operation results when "0" is written to SWRST.
This bit is write-only, and so is always "0" at reading.

SWRUN: Stopwatch timer RUN/STOP control register (FF7CH•D0)

Controls RUN/STOP of the stopwatch timer.

When "1" is written: RUN
When "0" is written: STOP
Reading: Valid

The stopwatch timer enters the RUN status when "1" is written to the SWRUN register, and the STOP status when "0" is written.
In the STOP status, the timer data is maintained until the next RUN status or the timer is reset. Also, when the STOP status changes to the RUN status, the data that is maintained can be used for resuming the count.

When data of the counter is read at run mode, proper reading may not be obtained due to the carry from low-order digits (SWD0–SWD3) into high-order digits (SWD4–SWD7) (i.e., in case SWD0–SWD3 and SWD4–SWD7 reading span the timing of the carry). To avoid this occurrence, perform the reading after suspending the counter once and then set the SWRUN to "1" again.
Moreover, it is required that the suspension period not exceed 976 μsec (1/4 cycle of 256 Hz).
At initial reset, this register is set to "0".

EISW10: 10Hz interrupt mask register (FFE7H•D0)
EISW1: 1Hz interrupt mask register (FFE7H•D1)

These registers are used to select whether to mask the stopwatch timer interrupt.

When "1" is written: Enabled
When "0" is written: Masked
Reading: Valid

The interrupt mask registers (EISW10, EISW1) are used to select whether to mask the interrupt to the separate frequencies (10 Hz, 1 Hz).
At initial reset, these registers are set to "0".

ISW10: 10 Hz interrupt factor flag (FFF7H•D0)
ISW1: 1 Hz interrupt factor flag (FFF7H•D1)

These flags indicate the status of the stopwatch timer interrupt.

When "1" is read: Interrupt has occurred
When "0" is read: Interrupt has not occurred

When "1" is written: Flag is reset
When "0" is written: Invalid

The interrupt factor flags ISW10 and ISW1 correspond to 10 Hz and 1 Hz stopwatch timer interrupts, respectively. The software can judge from these flags whether there is a stopwatch timer interrupt. However, even if the interrupt is masked, the flags are set to "1" by the overflow of the corresponding counters.
These flags are reset to "0" by writing "1" to them.
After an interrupt occurs, the same interrupt will occur again if the interrupt enabled state (I flag = "1") is set or the RETI instruction is executed unless the interrupt factor flag is reset. Therefore, be sure to reset (write "1" to) the interrupt factor flag in the interrupt service routine before shifting to the interrupt enabled state.
At initial reset, these flags are set to "0".

4.10.5 Programming notes

(1) To operate the stopwatch timer correctly, the prescaler must be set to suit the crystal oscillator used for the OSC1 oscillation circuit.

(2) When data of the counter is read at run mode, perform the reading after suspending the counter once and then set SWRUN to "1" again. Moreover, it is required that the suspension period not exceed 976 μsec (1/4 cycle of 256 Hz).

(3) After an interrupt occurs, the same interrupt will occur again if the interrupt enabled state (I flag = "1") is set or the RETI instruction is executed unless the interrupt factor flag is reset. Therefore, be sure to reset (write "1" to) the interrupt factor flag in the interrupt service routine before shifting to the interrupt enabled state.

4.11 Programmable Timer

4.11.1 Configuration of programmable timer

The E0C63B08 has two 8-bit programmable timer systems (timer 0 and timer 1) built-in.
Timer 0 and timer 1 are composed of 8-bit presettable down counters and they can be used as 8-bit × 2 channel programmable timers. Timer 0 also has an event counter function using the K13 input port terminal.
Figure 4.11.1.1 shows the configuration of the programmable timer.

The programmable timer is designed to count down from the initial value set in the counter with software. An underflow according to the initial value occurs by counting down and is used for the following functions:

- Presetting the initial value to the counter to generate the periodical underflow signal
- Generating an interrupt
- Generating a TOUT signal output from the R02 output port terminal
- Generating the synchronous clock source for the serial interface (timer 1 underflow is used, and it is possible to set the transfer rate)

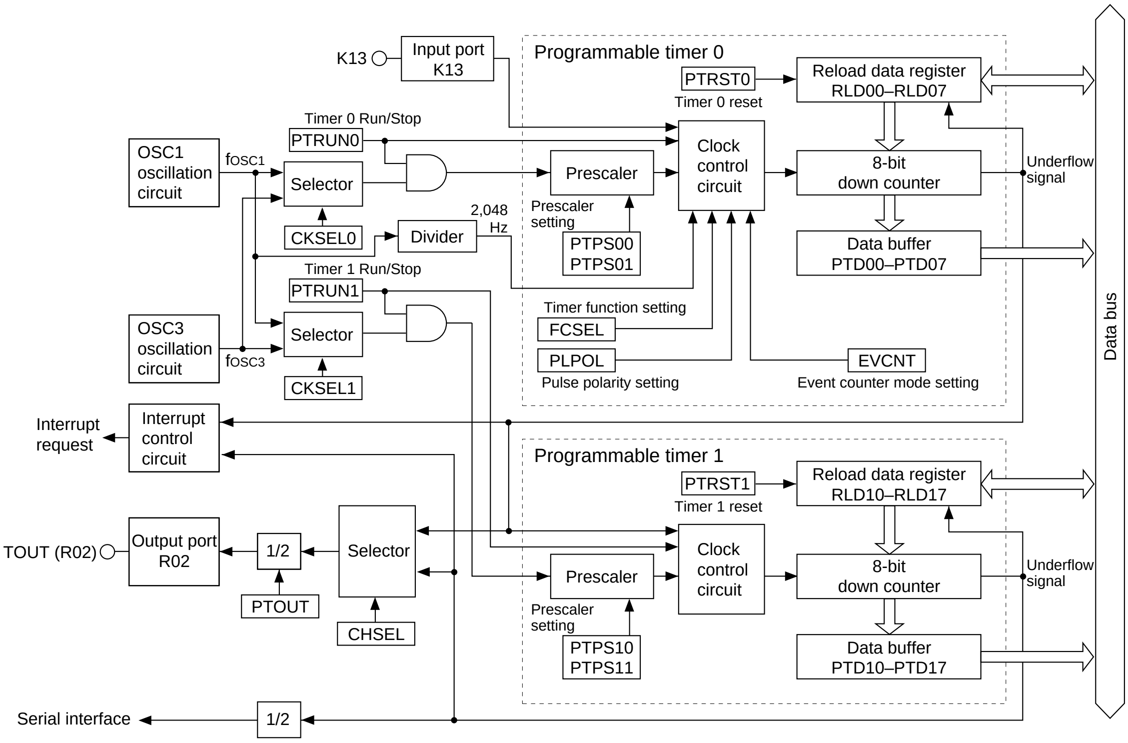


Fig. 4.11.1.1 Configuration of programmable timer

4.11.2 Setting of initial value and counting down

Timers 0 and 1 each have a down counter and reload data register.

The reload data registers RLD00–RLD07 (timer 0) and RLD10–RLD17 (timer 1) are used to set the initial value to the down counter.
By writing "1" to the timer reset bit PTRST0 (timer 0) or PTRST1 (timer 1), the down counter loads the initial value set in the reload register RLD. Therefore, down-counting is executed from the stored initial value by the input clock.

The registers PTRUN0 (timer 0) and PTRUN1 (timer 1) are provided to control the RUN/STOP for timers 0 and 1. By writing "1" to the register after presetting the reload data to the down counter, the down counter starts counting down. Writing "0" stops the input count clock and the down counter stops counting. This control (RUN/STOP) does not affect the counter data. The counter maintains its data while stopped, and can restart counting continuing from that data.

The counter data can be read via the data buffers PTD00–PTD07 (timer 0) and PTD10–PTD17 (timer 1) in optional timing. However, the counter has the data hold function the same as the clock timer, that holds the high-order data when the low-order data is read in order to prevent the borrowing operation between low- and high-order reading, therefore be sure to read the low-order data first.

The counter reloads the initial value set in the reload data register RLD when an underflow occurs through the count down. It continues counting down from the initial value after reloading.
In addition to reloading the counter, this underflow signal controls the interrupt generation, pulse (TOUT signal) output and clock supplying to the serial interface.

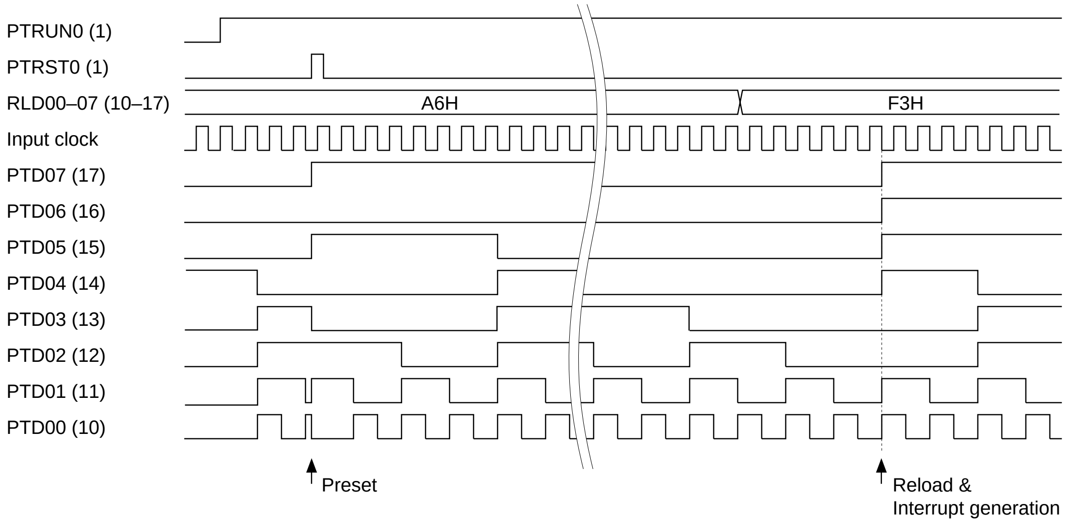


Fig. 4.11.2.1 Basic operation timing of down counter

4.11.3 Counter mode

The programmable timer can operate in two counter modes, timer mode and event counter mode. It can be selected by software.

(1) Timer mode

The timer mode counts down using the prescaler output as an input clock. In this mode, the programmable timer operates as a periodical timer using the OSC1 or OSC3 oscillation clock as a clock source. Timer 0 can operate in both the timer mode and the event counter mode. The mode can be switched using the timer 0 counter mode selection register EVCNT. When the EVCNT register is set to "0", timer 0 operates in the timer mode.
Timer 1 operates only in the timer mode.
At initial reset, this mode is set.

Refer to Section 4.11.2, "Setting of initial value and counting down" for basic operation and control.

The input clock in the timer mode is generated by the prescaler built into the programmable timer. The prescaler generates the input clock by dividing the OSC1 or OSC3 oscillation clock. Refer to the next section for setting the input clock.

(2) Event counter mode

The timer 0 has an event counter function that counts an external clock input to the input port K13. This function is selected by writing "1" to the timer 0 counter mode selection register EVCNT. The timer 1 operates only in the timer mode, and cannot be used as an event counter.

In the event counter mode, the clock is supplied to timer 0 from outside of the IC, therefore, the settings of the timer 0 prescaler division ratio selection registers PTPS00 and PTPS01 and the settings of the timer 0 source clock selection register CKSEL0 become invalid.

Count down timing can be selected from either the falling or rising edge of the input clock using the timer 0 pulse polarity selection register PLPOL. When "0" is written to the PLPOL register, the falling edge is selected, and when "1" is written, the rising edge is selected. The count down timing is shown in Figure 4.11.3.1.

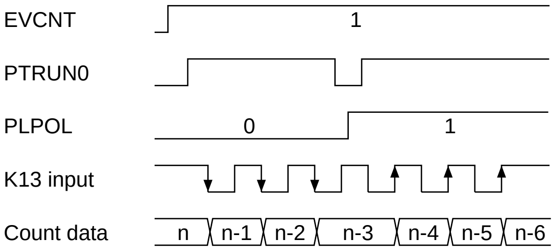


Fig. 4.11.3.1 Timing chart in event counter mode

The event counter mode also includes a noise reject function to eliminate noise such as chattering on the external clock (K13 input signal). This function is selected by writing "1" to the timer 0 function selection register FCSEL.
When "with noise rejector" is selected, an input pulse width for both low and high levels must be 0.98 msec or more to count reliably. (The noise rejecter allows the counter to input the clock at the second falling edge of the internal 2,048 Hz signal after changing the input level of the K13 input port terminal. Consequently, the pulse width of noise that can reliably be rejected is 0.48 msec or less.) Figure 4.11.3.2 shows the count down timing with noise rejecter.

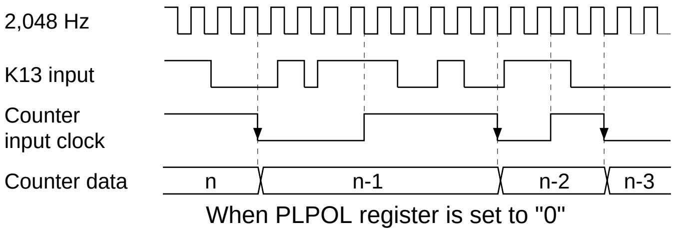


Fig. 4.11.3.2 Count down timing with noise rejecter

The operation of the event counter mode is the same as the timer mode except it uses the K13 input as the clock.
Refer to Section 4.11.2, "Setting of initial value and counting down" for basic operation and control.

4.11.4 Setting of input clock in timer mode

Timer 0 and timer 1 each include a prescaler. The prescalers generate the input clock for each timer by dividing the source clock supplied from the OSC1 or OSC3 oscillation circuit.
The source clock (OSC1 or OSC3) and the division ratio of the prescaler can be selected with software for timer 0 and timer 1 individually.
The set input clock is used for the count clock during operation in the timer mode. When the timer 0 is used in the event counter mode, the following settings become invalid.

The input clock is set in the following sequence.

(1) Selection of source clock

Select the source clock input to each prescaler from either OSC1 or OSC3. This selection is done using the source clock selection registers CKSEL0 (timer 0) and CKSEL1 (timer 1); when "0" is written to the register, OSC1 is selected and when "1" is written, OSC3 is selected.
When the OSC3 oscillation clock is selected for the clock source, it is necessary to turn the OSC3 oscillation ON, prior to using the programmable timer. However the OSC3 oscillation circuit requires a time interval of several msec to several 10 msec from turning the circuit ON until the oscillation stabilizes. Therefore, allow an adequate interval from turning the OSC3 oscillation circuit ON to starting the programmable timer. Refer to Section 4.4, "Oscillation Circuit", for the control and notes of the OSC3 oscillation circuit.
At initial reset, the OSC3 oscillation circuit is set in the OFF state.

(2) Selection of prescaler division ratio

Select the division ratio for each prescaler from among 4 types. This selection is done using the prescaler division ratio selection registers PTPS00/PTPSC01 (timer 0) and PTPS10/PTPS11 (timer 1). Table 4.11.4.1 shows the correspondence between the setting value and the division ratio.

Table 4.11.4.1 Selection of prescaler division ratio

PTPS11 PTPS01	PTPS10 PTPS00	Prescaler division ratio
1	1	Source clock / 256
1	0	Source clock / 32
0	1	Source clock / 4
0	0	Source clock / 1

By writing "1" to the register PTRUN0 (timer 0) or PTRUN1 (timer 1), the prescaler inputs the source clock and outputs the clock divided by the selected division ratio. The counter starts counting down by inputting the clock.

4.11.5 Interrupt function

The programmable timer can generate an interrupt due to an underflow of the timer 0 and timer 1. See Figure 4.11.2.1 for the interrupt timing.

An underflow of timer 0 and timer 1 sets the corresponding interrupt factor flag IPT0 (timer 0) or IPT1 (timer 1) to "1", and generates an interrupt. The interrupt can also be masked by setting the corresponding interrupt mask register EIPT0 (timer 0) or EIPT1 (timer 1). However, the interrupt factor flag is set to "1" by an underflow of the corresponding timer regardless of the interrupt mask register setting.

4.11.6 Setting of TOUT output

The programmable timer can generate a TOUT signal due to an underflow of timer 0 or timer 1. The TOUT signal is generated by dividing the underflows in 1/2. It is possible to select which timer's underflow is to be used by the TOUT output channel selection register CHSEL. When "0" is written to the CHSEL register, timer 0 is selected and when "1" is written, timer 1 is selected.
Figure 4.11.6.1 shows the TOUT signal waveform when the channel is changed.

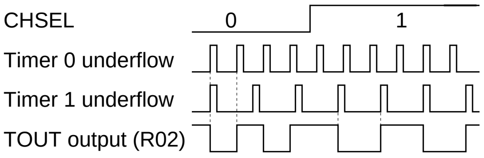


Fig. 4.11.6.1 TOUT signal waveform at channel change

The TOUT signal can be output from the R02 output port terminal. Programmable clocks can be supplied to external devices.
Figure 4.11.6.2 shows the configuration of the output port R02.

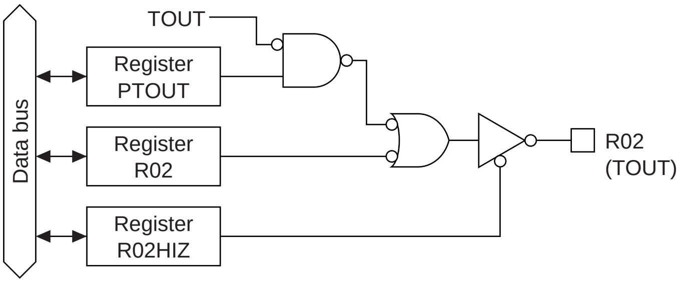


Fig. 4.11.6.2 Configuration of R02

The output of a TOUT signal is controlled by the PTOUT register. When "1" is written to the PTOUT register, the TOUT signal is output from the R02 output port terminal and when "0" is written, the terminal goes to a high (VDD) level. However, the data register R02 must always be "1" and the high impedance control register R02HIZ must always be "0" (data output state).

Since the TOUT signal is generated asynchronously from the PTOUT register, a hazard within 1/2 cycle is generated when the signal is turned ON and OFF by setting the register.
Figure 4.11.6.3 shows the output waveform of the TOUT signal.

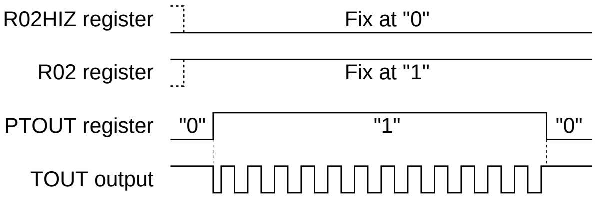


Fig. 4.11.6.3 Output waveform of the TOUT signal

4.11.7 Transfer rate setting for serial interface

The signal that is made from underflows of timer 1 by dividing them in 1/2, can be used as the clock source for the serial interface.
The programmable timer outputs the clock to the serial interface by setting timer 1 into RUN state (PTRUN = "1"). It is not necessary to control with the PTOUT register.

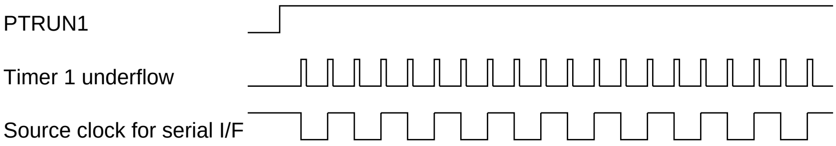


Fig. 4.11.7.1 Synchronous clock of serial interface

A setting value for the RLD1X register according to a transfer rate is calculated by the following expression:

RLD1X = fosc / (2 ∗ bps ∗ division ratio of the prescaler) - 1
fosc: Oscillation frequency (OSC1/OSC3)
bps: Transfer rate
(00H can be set to RLD1X)

4.11.8 I/O memory of programmable timer

Table 4.11.8.1 shows the I/O addresses and the control bits for the programmable timer.

Table 4.11.8.1 Control bits of programmable timer

Address	Register								Comment
	D3	D2	D1	D0	Name	Init *1	1	0	
FFC0H	0	EVCNT	FCSEL	PLPOL	0 *3	– *2			Unused
					EVCNT	0	Event ct.	Timer	Timer 0 counter mode selection
	R	R/W			FCSEL	0	With NR	No NR	Timer 0 function selection (for event counter mode)
					PLPOL	0	↑	↓	Timer 0 pulse polarity selection (for event counter mode)
FFC1H	CHSEL	PTOUT	CKSEL1	CKSEL0	CHSEL	0	Timer1	Timer0	TOUT output channel selection
					PTOUT	0	On	Off	TOUT output control
	R/W				CKSEL1	0	OSC3	OSC1	Prescaler 1 source clock selection
					CKSEL0	0	OSC3	OSC1	Prescaler 0 source clock selection
FFC2H	PTPS01	PTPS00	PTRST0	PTRUN0	PTPS01	0			Prescaler 0 division ratio selection [PTPS01, 00] 0 1 2 3 Division ratio 1/1 1/4 1/32 1/256
					PTPS00	0			
	R/W		W	R/W	PTRST0*3	– *2	Reset	Invalid	Timer 0 reset (reload)
					PTRUN0	0	Run	Stop	Timer 0 Run/Stop
FFC3H	PTPS11	PTPS10	PTRST1	PTRUN1	PTPS11	0			Prescaler 1 division ratio selection [PTPS11, 10] 0 1 2 3 Division ratio 1/1 1/4 1/32 1/256
					PTPS10	0			
	R/W		W	R/W	PTRST1*3	– *2	Reset	Invalid	Timer 1 reset (reload)
					PTRUN1	0	Run	Stop	Timer 1 Run/Stop
FFC4H	RLD03	RLD02	RLD01	RLD00	RLD03	0			MSB
					RLD02	0			Programmable timer 0 reload data (low-order 4 bits)
	R/W				RLD01	0			
					RLD00	0			LSB
FFC5H	RLD07	RLD06	RLD05	RLD04	RLD07	0			MSB
					RLD06	0			Programmable timer 0 reload data (high-order 4 bits)
	R/W				RLD05	0			
					RLD04	0			LSB
FFC6H	RLD13	RLD12	RLD11	RLD10	RLD13	0			MSB
					RLD12	0			Programmable timer 1 reload data (low-order 4 bits)
	R/W				RLD11	0			
					RLD10	0			LSB
FFC7H	RLD17	RLD16	RLD15	RLD14	RLD17	0			MSB
					RLD16	0			Programmable timer 1 reload data (high-order 4 bits)
	R/W				RLD15	0			
					RLD14	0			LSB
FFC8H	PTD03	PTD02	PTD01	PTD00	PTD03	0			MSB
					PTD02	0			Programmable timer 0 data (low-order 4 bits)
	R				PTD01	0			
					PTD00	0			LSB
FFC9H	PTD07	PTD06	PTD05	PTD04	PTD07	0			MSB
					PTD06	0			Programmable timer 0 data (high-order 4 bits)
	R				PTD05	0			
					PTD04	0			LSB
FFCAH	PTD13	PTD12	PTD11	PTD10	PTD13	0			MSB
					PTD12	0			Programmable timer 1 data (low-order 4 bits)
	R				PTD11	0			
					PTD10	0			LSB
FFCBH	PTD17	PTD16	PTD15	PTD14	PTD17	0			MSB
					PTD16	0			Programmable timer 1 data (high-order 4 bits)
	R				PTD15	0			
					PTD14	0			LSB
FFE2H	0	0	EIPT1	EIPT0	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R		R/W		EIPT1	0	Enable	Mask	Interrupt mask register (Programmable timer 1)
					EIPT0	0	Enable	Mask	Interrupt mask register (Programmable timer 0)
FFF2H	0	0	IPT1	IPT0	0 *3	– *2	(R)	(R)	Unused
					0 *3	– *2	Yes	No	Unused
	R		R/W		IPT1	0	(W)	(W)	Interrupt factor flag (Programmable timer 1)
					IPT0	0	Reset	Invalid	Interrupt factor flag (Programmable timer 0)

*1 Initial value at initial reset

*2 Not set in the circuit

*3 Constantly "0" when being read

CKSEL0: Prescaler 0 source clock selection register (FFC1H•D0)
CKSEL1: Prescaler 1 source clock selection register (FFC1H•D1)

Selects the source clock of the prescaler.

When "1" is written: OSC3 clock
When "0" is written: OSC1 clock
Reading: Valid

The source clock for the prescaler is selected from OSC1 or OSC3. When "0" is written to the CKSEL0 register, the OSC1 clock is selected as the input clock for the prescaler 0 (for timer 0) and when "1" is written, the OSC3 clock is selected.
Same as above, the source clock for prescaler 1 is selected by the CKSEL1 register.
When the event counter mode is selected to timer 0, the setting of the CKSEL0 register becomes invalid.
At initial reset, these registers are set to "0".

PTPS00, PTPS01: Timer 0 prescaler division ratio selection register (FFC2H•D2, D3)
PTPS10, PTPS11: Timer 1 prescaler division ratio selection register (FFC3H•D2, D3)

Selects the division ratio of the prescaler.
Two bits of PSC00 and PSC01 are the prescaler division ratio selection register for timer 0, and two bits of PSC10 and PSC11 are for timer 1. The prescaler division ratios that can be set by these registers are shown in Table 4.11.8.2.

Table 4.11.8.2 Selection of prescaler division ratio

PTPS11 PTPS01	PTPS10 PTPS00	Prescaler division ratio
1	1	Source clock / 256
1	0	Source clock / 32
0	1	Source clock / 4
0	0	Source clock / 1

When the event counter mode is selected to timer 0, the setting of the PTPS00 and PTPS01 becomes invalid.
At initial reset, these registers are set to "0".

EVCNT: Timer 0 counter mode selection register (FFC0H•D2)

Selects a counter mode for timer 0.

When "1" is written: Event counter mode
When "0" is written: Timer mode
Reading: Valid

The counter mode for timer 0 is selected from either the event counter mode or timer mode. When "1" is written to the EVCNT register, the event counter mode is selected and when "0" is written, the timer mode is selected.
At initial reset, this register is set to "0".

FCSEL: Timer 0 function selection register (FFC0H•D1)

Selects whether the noise rejector of the clock input circuit will be used or not in the event counter mode.

When "1" is written: With noise rejecter
When "0" is written: Without noise rejecter
Reading: Valid

When "1" is written to the FCSEL register, the noise rejecter is used and counting is done by an external clock (K13) with 0.98 msec or more pulse width. (The noise rejecter allows the counter to input the clock at the second falling edge of the internal 2,048 Hz signal after changing the input level of the K13 input port terminal. Consequently, the pulse width of noise that can reliably be rejected is 0.48 msec or less.)
When "0" is written to the FCSEL register, the noise rejector is not used and the counting is done directly by an external clock input to the K13 input port terminal.
Setting of this register is effective only when timer 0 is used in the event counter mode.
At initial reset, this register is set to "0".

PLPOL: Timer 0 pulse polarity selection register (FFC0H•D0)

Selects the count pulse polarity in the event counter mode.

When "1" is written: Rising edge
When "0" is written: Falling edge
Reading: Valid

The count timing in the event counter mode (timer 0) is selected from either the falling edge of the external clock input to the K10 input port terminal or the rising edge. When "0" is written to the PLPOL register, the falling edge is selected and when "1" is written, the rising edge is selected.
Setting of this register is effective only when timer 0 is used in the event counter mode.
At initial reset, this register is set to "0".

RLD00–RLD07: Timer 0 reload data register (FFC4H, FFC5H)
RLD10–RLD17: Timer 1 reload data register (FFC6H, FFC7H)

Sets the initial value for the counter.
The reload data written in this register is loaded to the respective counters. The counter counts down using the data as the initial value for counting.
Reload data is loaded to the counter when the counter is reset by writing "1" to the PTRST0 or PTRST1 register, or when counter underflow occurs.
At initial reset, these registers are set to "00H".

PTD00–PTD07: Timer 0 counter data (FFC8H, FFC9H)
PTD10–PTD17: Timer 1 counter data (FFCAH, FFCBH)

Count data in the programmable timer can be read from these latches.
The low-order 4 bits of the count data in timer 0 can be read from PTD00–PTD03, and the high-order data can be read from PTD04–PTD07. Similarly, for timer 1, the low-order 4 bits can be read from PTD10–PTD13, and the high-order data can be read from PTD14–PTD17.
Since the high-order 4 bits are held by reading the low-order 4 bits, be sure to read the low-order 4 bits first.
Since these latches are exclusively for reading, the writing operation is invalid.
At initial reset, these counter data are set to "00H".

PTRST0: Timer 0 reset (reload) (FFC2H•D1)
PTRST1: Timer 1 reset (reload) (FFC3H•D1)

Resets the timer and presets reload data to the counter.

When "1" is written:	Reset
When "0" is written:	No operation
Reading:	Always "0"

By writing "1" to PTRST0, the reload data in the reload register PLD00–PLD07 is preset to the counter in timer 0. Similarly, the reload data in PLD10–PLD17 is preset to the counter in timer 1 by PTRST1.
When the counter is preset in the RUN status, the counter restarts immediately after presetting. In the case of STOP status, the reload data is preset to the counter and is maintained.
No operation results when "0" is written.
Since these bits are exclusively for writing, always set to "0" during reading.

PTRUN0: Timer 0 RUN/STOP control register (FFC2H•D0)
PTRUN1: Timer 1 RUN/STOP control register (FFC3H•D0)

Controls the RUN / STOP of the counter.

When "1" is written:	RUN
When "0" is written:	STOP
Reading:	Valid

The counter in timer 0 starts counting down by writing "1" to the PTRUN0 register and stops by writing "0".
In STOP status, the counter data is maintained until the counter is reset or is set in the next RUN status.
When STOP status changes to RUN status, the data that has been maintained can be used for resuming the count.
Same as above, the timer 1 counter is controlled by the PTRUN1 register.
At initial reset, these registers are set to "0".

CHSEL: TOUT output channel selection register (FFC1H•D3)

Selects the channel used for TOUT signal output.

When "1" is written:	Timer 1
When "0" is written:	Timer 0
Reading:	Valid

This register selects which timer's underflow (timer 0 or timer 1) is used to generate a TOUT signal. When "0" is written to the CHSEL register, timer 0 is selected and when "1" is written, timer 1 is selected.
At initial reset, this register is set to "0".

PTOUT: TOUT output control register (FFC1H•D2)

Turns TOUT signal output ON and OFF.

When "1" is written:	ON
When "0" is written:	OFF
Reading:	Valid

PTOUT is the output control register for the TOUT signal. When "1" is written to the register, the TOUT signal is output from the output port terminal R02 and when "0" is written, the terminal goes to a high (VDD) level. However, the data register R02 must always be "1" and the high impedance control register R02HIZ must always be "0" (data output state).
At initial reset, this register is set to "0".

EIPT0: Timer 0 interrupt mask register (FFE2H•D0)
EIPT1: Timer 1 interrupt mask register (FFE2H•D1)

These registers are used to select whether to mask the programmable timer interrupt or not.

When "1" is written:	Enabled
When "0" is written:	Masked
Reading:	Valid

Timer 0 and timer 1 interrupts can be masked individually by the interrupt mask registers EIPT0 (timer 0) and EIPT1 (timer 1).
At initial reset, these registers are set to "0".

IPT0: Timer 0 interrupt factor flag (FFF2H•D0)
IPT1: Timer 1 interrupt factor flag (FFF2H•D1)

These flags indicate the status of the programmable timer interrupt.

When "1" is read:	Interrupt has occurred
When "0" is read:	Interrupt has not occurred

When "1" is written:	Flag is reset
When "0" is written:	Invalid

The interrupt factor flags IPT0 and IPT1 correspond to timer 0 and timer 1 interrupts, respectively. The software can judge from these flags whether there is a programmable timer interrupt. However, even if the interrupt is masked, the flags are set to "1" by the underflows of the corresponding counters.
These flags are reset to "0" by writing "1" to them.
After an interrupt occurs, the same interrupt will occur again if the interrupt enabled state (I flag = "1") is set or the RETI instruction is executed unless the interrupt factor flag is reset. Therefore, be sure to reset (write "1" to) the interrupt factor flag in the interrupt service routine before shifting to the interrupt enabled state.
At initial reset, these flags are set to "0".

4.11.9 Programming notes

(1) When reading counter data, be sure to read the low-order 4 bits (PTD00–PTD03, PTD10–PTD13) first. Furthermore, the high-order 4 bits (PTD04–PTD07, PTD14–PTD17) should be read within 0.73 msec of reading the low-order 4 bits (PTD00–PTD03, PTD10–PTD13).

(2) The programmable timer actually enters RUN/STOP status in synchronization with the falling edge of the input clock after writing to the PTRUN0/PTRUN1 register. Consequently, when "0" is written to the PTRUN0/PTRUN1 register, the timer enters STOP status at the point where the counter is decremented (-1). The PTRUN0/PTRUN1 register maintains "1" for reading until the timer actually stops.
Figure 4.11.9.1 shows the timing chart for the RUN/STOP control.

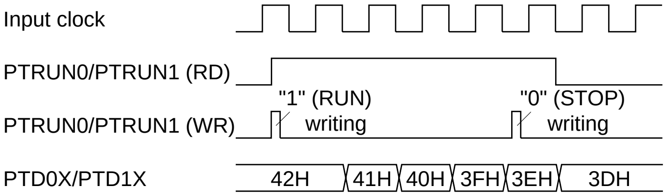


Fig. 4.11.9.1 Timing chart for RUN/STOP control

It is the same even in the event counter mode. Therefore, be aware that the counter does not enter RUN/STOP status if a clock is not input after setting the RUN/STOP control register (PTRUN0).

(3) Since the TOUT signal is generated asynchronously from the PTOUT register, a hazard within 1/2 cycle is generated when the signal is turned ON and OFF by setting the register.

(4) When the OSC3 oscillation clock is selected for the clock source, it is necessary to turn the OSC3 oscillation ON, prior to using the programmable timer. However the OSC3 oscillation circuit requires a time interval of several msec to several 10 msec from turning the circuit ON until the oscillation stabilizes. Therefore, allow an adequate interval from turning the OSC3 oscillation circuit ON to starting the programmable timer. Refer to Section 4.4, "Oscillation Circuit", for the control and notes of the OSC3 oscillation circuit.
At initial reset, the OSC3 oscillation circuit is set in the OFF state.

(5) After an interrupt occurs, the same interrupt will occur again if the interrupt enabled state (I flag = "1") is set or the RETI instruction is executed unless the interrupt factor flag is reset. Therefore, be sure to reset (write "1" to) the interrupt factor flag in the interrupt service routine before shifting to the interrupt enabled state.

4.12 Serial Interface (SIN, SOUT, $\overline{\text{SCLK}}$, $\overline{\text{SRDY}}$)

4.12.1 Configuration of serial interface

The E0C63B08 has a synchronous clock type 8 bits serial interface built-in.
The configuration of the serial interface is shown in Figure 4.12.1.1.
The CPU, via the 8-bit shift register, can read the serial input data from the SIN terminal. Moreover, via the same 8-bit shift register, it can convert parallel data to serial data and output it to the SOUT terminal.
The synchronous clock for serial data input/output may be set by selecting by software any one of three types of master mode (internal clock mode: when the E0C63B08 is to be the master for serial input/output) and a type of slave mode (external clock mode: when the E0C63B08 is to be the slave for serial input/output).
Also, when the serial interface is used at slave mode, $\overline{\text{SRDY}}$ signal which indicates whether or not the serial interface is available to transmit or receive can be output to the $\overline{\text{SRDY}}$ terminal.

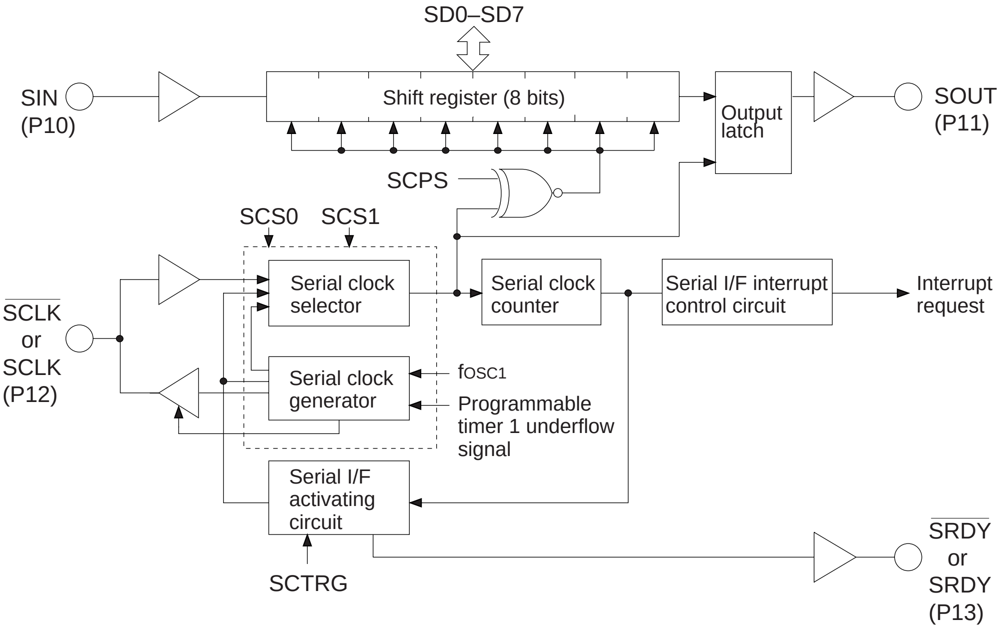


Fig. 4.12.1.1 Configuration of serial interface

The input/output ports of the serial interface are shared with the I/O ports P10–P13, and function of these ports can be selected through the software.
P10–P13 terminals and serial input/output correspondence are as follows:

Master mode	***Slave mode***
P10 = SIN (I)	P10 = SIN (I)
P11 = SOUT (O)	P11 = SOUT (O)
P12 = $\overline{\text{SCLK}}$ (O)	P12 = $\overline{\text{SCLK}}$ (I)
P13 = I/O port (I/O)	P13 = $\overline{\text{SRDY}}$ (O)

Note: At initial reset, P10–P13 are set to I/O ports.
When using the serial interface, switch the function (ESIF = "1") in the initial routine.

4.12.2 Mask option

(1) Terminal specification

Since the input/output terminals of the serial interface is shared with the I/O ports (P10–P13), the mask option that selects the output specification for the I/O port is also applied to the serial interface. Three types of specifications are available: complementary output, N-channel open drain (with pull-up) and N-channel open drain (without pull-up). Specification for 4 bits of P10–P13 port can be selected in mass. Select a terminal specification according to the master/slave mode setting.

When N-channel open drain (with pull-up) is selected, do not apply a voltage exceeding the power supply voltage to the port.
When N-channel open drain (without pull-up) is selected, a voltage within the ruled range (see Chapter 7, "Electrical Characteristics") can be applied to the port. However, take care that the floating status does not occur on the input terminal.

(2) Polarity of synchronous clock and ready signal

Polarity of the synchronous clock and the ready signal that is output in the slave mode can be selected from either positive polarity (high active, SCLK & SRDY) or negative polarity (low active, $\overline{\text{SCLK}}$ & $\overline{\text{SRDY}}$).
When operating the serial interface in the slave mode, the synchronous clock is input from a external device. Be aware that the terminal specification is pull-up only and a pull-down resistor cannot be built in if positive polarity is selected.
In the following explanation, it is assumed that negative polarity ($\overline{\text{SCLK}}$, $\overline{\text{SRDY}}$) has been selected.

4.12.3 Master mode and slave mode of serial interface

The serial interface of the E0C63B08 has two types of operation mode: master mode and slave mode.
The master mode uses an internal clock as the synchronous clock for the built-in shift register, and outputs this internal clock from the $\overline{\text{SCLK}}$ (P12) terminal to control the external (slave side) serial device.
In the slave mode, the synchronous clock output from the external (master side) serial device is input from the $\overline{\text{SCLK}}$ (P12) terminal and it is used as the synchronous clock for the built-in shift register.
The master mode and slave mode are selected by writing data to the SCS1 and SCS0 registers.
When the master mode is selected, a synchronous clock may be selected from among 3 types as shown in Table 4.12.3.1.

Table 4.12.3.1 Synchronous clock selection

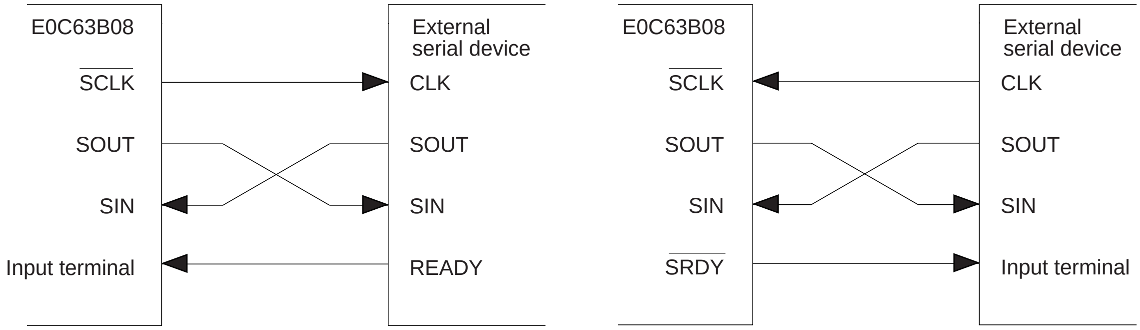
SCS1	SCS0	Mode	Synchronous clock
1	1	Master mode	OSC1
1	0		OSC1 /2
0	1		Programmable timer
0	0	Slave mode	External clock

When the programmable timer is selected, the signal that is generated by dividing the underflow signal of the programmable timer (timer 1) in 1/2 is used as the synchronous clock. In this case, the programmable timer must be controlled before operating the serial interface. Refer to Section 4.11, "Programmable Timer" for the control of the programmable timer.

At initial reset, the slave mode (external clock mode) is selected.
Moreover, the synchronous clock, along with the input/output of the 8-bit serial data, is controlled as follows:

- In the master mode, after output of 8 clocks from the $\overline{\text{SCLK}}$ (P12) terminal, clock output is automatically suspended and the $\overline{\text{SCLK}}$ (P12) terminal is fixed at high level.
- In the slave mode, after input of 8 clocks to the $\overline{\text{SCLK}}$ (P12) terminal, subsequent clock inputs are masked.

A sample basic serial input/output portion connection is shown in Figure 4.12.3.1.



(a) Master mode (b) Slave mode

Fig. 4.12.3.1 Sample basic connection of serial input/output section

4.12.4 Data input/output and interrupt function

The serial interface of E0C63B08 can input/output data via the internal 8-bit shift register. The shift register operates by synchronizing with either the synchronous clock output from the $\overline{\text{SCLK}}$ (P12) terminal (master mode), or the synchronous clock input to the $\overline{\text{SCLK}}$ (P12) terminal (slave mode).
The serial interface generates an interrupt on completion of the 8-bit serial data input/output. Detection of serial data input/output is done by counting of the synchronous clock $\overline{\text{SCLK}}$; the clock completes input/output operation when 8 counts (equivalent to 8 cycles) have been made and then generates an interrupt.
The serial data input/output procedure is explained below:

(1) Serial data output procedure and interrupt

The E0C63B08 serial interface is capable of outputting parallel data as serial data, in units of 8 bits.
By setting the parallel data to the data registers SD0–SD3 (FF72H) and SD4–SD7 (FF73H) and writing "1" to SCTRG bit (FF70H•D1), it synchronizes with the synchronous clock and the serial data is output to the SOUT (P11) terminal. The synchronous clock used here is as follows: in the master mode, internal clock which is output to the $\overline{\text{SCLK}}$ (P12) terminal while in the slave mode, external clock which is input from the $\overline{\text{SCLK}}$ (P12) terminal.
Shift timing of serial data is as follows:

- ***When negative polarity is selected for the synchronous clock (mask option):***
  The serial data output to the SOUT (P11) terminal changes at the falling edge of the clock input or output from/to the $\overline{\text{SCLK}}$ (P12) terminal. The data in the shift register is shifted at the falling edge of the $\overline{\text{SCLK}}$ signal when the SCPS register (FF71H•D2) is "1" and is shifted at the rising edge of the $\overline{\text{SCLK}}$ signal when the SCPS register is "0".

- ***When positive polarity is selected for the synchronous clock (mask option):***
  The serial data output to the SOUT (P11) terminal changes at the rising edge of the clock input or output from/to the SCLK (P12) terminal. The data in the shift register is shifted at the rising edge of the SCLK signal when the SCPS register is "1" and is shifted at the falling edge of the SCLK signal when the SCPS register is "0".

When the output of the 8-bit data from SD0 to SD7 is completed, the interrupt factor flag ISIF (FFF3H•D0) is set to "1" and an interrupt occurs. Moreover, the interrupt can be masked by the interrupt mask register EISIF (FFE3H•D0). However, regardless of the interrupt mask register setting, the interrupt factor flag is set to "1" after output of the 8-bit data.

(2) Serial data input procedure and interrupt

The E0C63B08 serial interface is capable of inputting serial data as parallel data, in units of 8 bits.
The serial data is input from the SIN (P10) terminal, synchronizes with the synchronous clock, and is sequentially read in the 8-bit shift register. As in the above item (1), the synchronous clock used here is as follows: in the master mode, internal clock which is output to the $\overline{\text{SCLK}}$ (P12) terminal while in the slave mode, external clock which is input from the $\overline{\text{SCLK}}$ (P12) terminal.
Shift timing of serial data is as follows:

- ***When negative polarity is selected for the synchronous clock (mask option):***

  The serial data is read into the built-in shift register at the falling edge of the $\overline{\text{SCLK}}$ signal when the SCPS register is "1" and is read at the rising edge of the $\overline{\text{SCLK}}$ signal when the SCPS register is "0". The shift register is sequentially shifted as the data is fetched.

- ***When positive polarity is selected for the synchronous clock (mask option):***

  The serial data is read into the built-in shift register at the rising edge of the SCLK signal when the SCPS register is "1" and is read at the falling edge of the SCLK signal when the SCPS register is "0". The shift register is sequentially shifted as the data is fetched.

When the input of the 8-bit data from SD0 to SD7 is completed, the interrupt factor flag ISIF is set to "1" and an interrupt is generated. Moreover, the interrupt can be masked by the interrupt mask register EISIF. However, regardless of the interrupt mask register setting, the interrupt factor flag is set to "1" after input of the 8-bit data.
The data input in the shift register can be read from data registers SD0–SD7 by software.

(3) Serial data input/output permutation

The E0C63B08 allows the input/output permutation of serial data to be selected by the SDP register (FF71H•D3) as to either LSB first or MSB first. The block diagram showing input/output permutation in case of LSB first and MSB first is provided in Figure 4.12.4.1. The SDP register should be set before setting data to SD0–SD7.

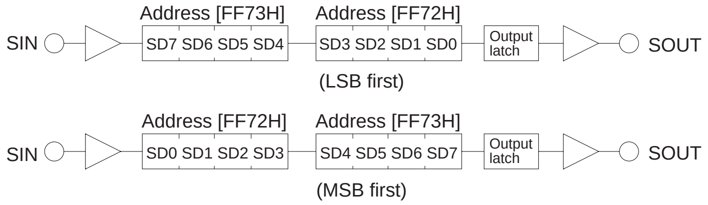


Fig. 4.12.4.1 Serial data input/output permutation

(4) $\overline{\text{SRDY}}$ signal

When the E0C63B08 serial interface is used in the slave mode (external clock mode), $\overline{\text{SRDY}}$ signal is used to indicate whether the internal serial interface is available to transmit or receive data for the master side (external) serial device. $\overline{\text{SRDY}}$ signal is output from the $\overline{\text{SRDY}}$ (P13) terminal.
Output timing of $\overline{\text{SRDY}}$ signal is as follows:

- ***When negative polarity is selected (mask option):***

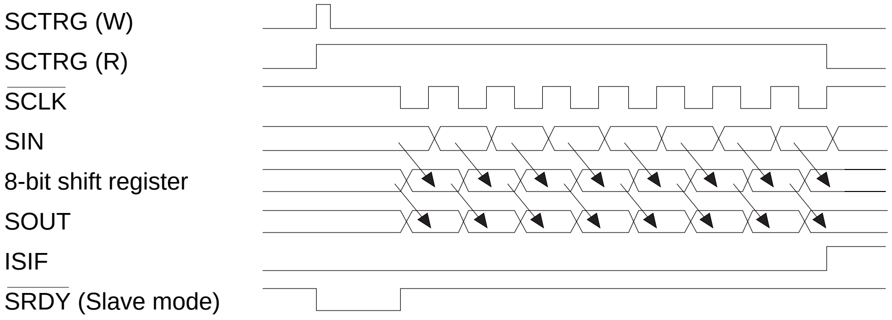
  $\overline{\text{SRDY}}$ signal goes "0" (low) when the E0C63B08 serial interface is available to transmit or receive data; normally, it is at "1" (high).
  $\overline{\text{SRDY}}$ signal changes from "1" to "0" immediately after "1" is written to SCTRG and returns from "0" to "1" when "0" is input to the $\overline{\text{SCLK}}$ (P12) terminal (i.e., when the serial input/output begins transmitting or receiving data). Moreover, when high-order data is read from or written to SD4–SD7, the $\overline{\text{SRDY}}$ signal returns to "1".

- ***When positive polarity is selected (mask option):***

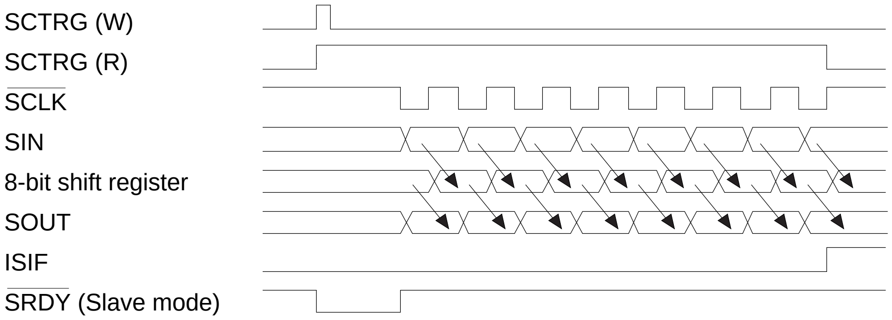
  SRDY signal goes "1" (high) when the E0C63B08 serial interface is available to transmit or receive data; normally, it is at "0" (low).
  SRDY signal changes from "0" to "1" immediately after "1" is written to SCTRG and returns from "1" to "0" when "1" is input to the SCLK (P12) terminal (i.e., when the serial input/output begins transmitting or receiving data). Moreover, when high-order data is read from or written to SD4–SD7, the SRDY signal returns to "0".

(5) Timing chart

The E0C63B08 serial interface timing charts are shown in Figures 4.12.4.2 and 4.12.4.3.

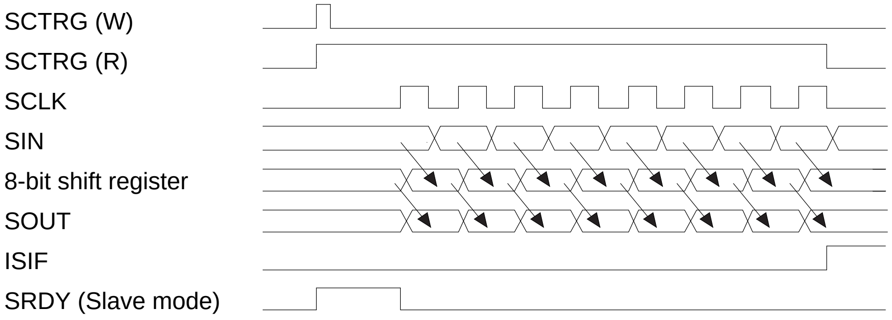


(a) When SCPS = "1"

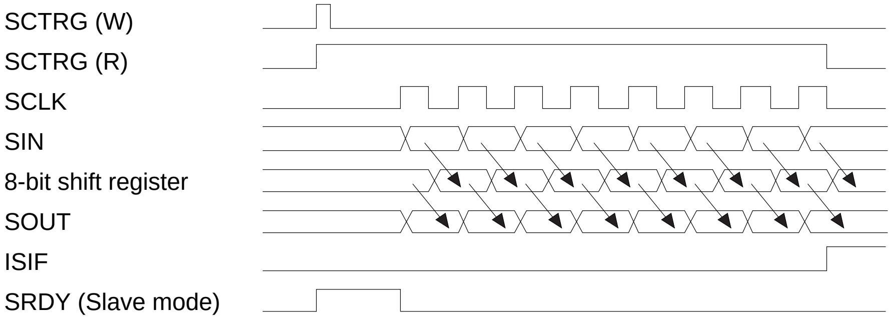


(b) When SCPS = "0"

Fig. 4.12.4.2 Serial interface timing chart (when synchronous clock is negative polarity $\overline{\text{SCLK}}$)



(a) When SCPS = "1"



(b) When SCPS = "0"

Fig. 4.12.4.3 Serial interface timing chart (when synchronous clock is positive polarity SCLK)

4.12.5 I/O memory of serial interface

Table 4.12.5.1 shows the I/O addresses and the control bits for the serial interface.

Table 4.12.5.1 Control bits of serial interface

Address	Register								Comment
	D3	D2	D1	D0	Name	Init *1	1	0	
FF45H	PUL13	PUL12	PUL11	PUL10	PUL13	1	On	Off	P13 pull-up control register functions as a general-purpose register when SIF (slave) is selected
	R/W				PUL12	1	On	Off	P12 pull-up control register (ESIF=0) functions as a general-purpose register when SIF (master) is selected $\overline{\text{SCLK}}$ (I) pull-up control register when SIF (slave) is selected
					PUL11	1	On	Off	P11 pull-up control register (ESIF=0) functions as a general-purpose register when SIF is selected
					PUL10	1	On	Off	P10 pull-up control register (ESIF=0) SIN pull-up control register when SIF is selected
FF70H	0	0	SCTRG	ESIF	0 *3	– *2			Unused
	R		R/W		0 *3	– *2			Unused
					SCTRG	0	Trigger	Invalid	Serial I/F clock trigger (writing)
							Run	Stop	Serial I/F clock status (reading)
					ESIF	0	SIF	I/O	Serial I/F enable (P1 port function selection)
FF71H	SDP	SCPS	SCS1	SCS0	SDP	0	MSB first	LSB first	Serial I/F data input/output permutation
	R/W				SCPS	0			Serial I/F clock phase selection
							↓	↑	–Negative polarity (mask option)
							↑	↓	–Positive polarity (mask option)
					SCS1	0			Serial I/F clock mode selection [SCS1, 0] 0 1 Clock Slave PT
					SCS0	0			[SCS1, 0] 2 3 Clock OSC1/2 OSC1
FF72H	SD3	SD2	SD1	SD0	SD3	– *2	High	Low	MSB
	R/W				SD2	– *2	High	Low	Serial I/F transmit/receive data (low-order 4 bits)
					SD1	– *2	High	Low	
					SD0	– *2	High	Low	LSB
FF73H	SD7	SD6	SD5	SD4	SD7	– *2	High	Low	MSB
	R/W				SD6	– *2	High	Low	Serial I/F transmit/receive data (high-order 4 bits)
					SD5	– *2	High	Low	
					SD4	– *2	High	Low	LSB
FFE3H	0	0	0	EISIF	0 *3	– *2			Unused
	R			R/W	0 *3	– *2			Unused
					0 *3	– *2			Unused
					EISIF	0	Enable	Mask	Interrupt mask register (Serial I/F)
FFF3H	0	0	0	ISIF	0 *3	– *2	(R)	(R)	Unused
	R			R/W	0 *3	– *2	Yes	No	Unused
					0 *3	– *2	(W)	(W)	Unused
					ISIF	0	Reset	Invalid	Interrupt factor flag (Serial I/F)

*1 Initial value at initial reset

*2 Not set in the circuit

*3 Constantly "0" when being read

ESIF: Serial interface enable register (P1 port function selection) (FF70H•D0)

Sets P10–P13 to the input/output port for the serial interface.

When "1" is written: Serial interface
When "0" is written: I/O port
Reading: Valid

When "1" is written to the ESIF register, P10, P11, P12 and P13 function as SIN, SOUT, $\overline{\text{SCLK}}$, $\overline{\text{SRDY}}$, respectively.
In the slave mode, the P13 terminal functions as $\overline{\text{SRDY}}$ output terminal, while in the master mode, it functions as the I/O port terminal.
At initial reset, this register is set to "0".

PUL10: SIN (P10) pull-up control register (FF45H•D0)
PUL12: $\overline{\text{SCLK}}$ (P12) pull-up control register (FF45H•D2)

Sets the pull-up of the SIN terminal and the $\overline{\text{SCLK}}$ terminals (in the slave mode).

When "1" is written: Pull-up ON
When "0" is written: Pull-up OFF
Reading: Valid

Sets the pull-up resistor built into the SIN (P10) and $\overline{\text{SCLK}}$ (P12) terminals to ON or OFF. (Pull-up resistor is only built in the port selected by mask option.)
$\overline{\text{SCLK}}$ pull-up is effective only in the slave mode. In the master mode, the PUL12 register can be used as a general purpose register.
At initial reset, these registers are set to "1" and pull-up goes ON.

SCS1, SCS0: Clock mode selection register (FF71H•D0, D1)

Selects the synchronous clock ($\overline{\text{SCLK}}$) for the serial interface.

Table 4.12.5.2 Synchronous clock selection

SCS1	SCS0	Mode	Synchronous clock
1	1	Master mode	OSC1
1	0		OSC1 /2
0	1		Programmable timer
0	0	Slave mode	External clock

Synchronous clock ($\overline{\text{SCLK}}$) is selected from among the above 4 types: 3 types of internal clock and external clock.
When the programmable timer is selected, the signal that is generated by dividing the underflow signal of the programmable timer (timer 1) in 1/2 is used as the synchronous clock. In this case, the programmable timer must be controlled before operating the serial interface. Refer to Section 4.11, "Programmable Timer" for the control of the programmable timer.
At initial reset, external clock is selected.

SCPS: Clock phase selection register (FF71H•D2)

Selects the timing for reading in the serial data input from the SIN (P10) terminal.

• ***When negative polarity is selected:***

When "1" is written: Falling edge of $\overline{\text{SCLK}}$
When "0" is written: Rising edge of $\overline{\text{SCLK}}$
Reading: Valid

• ***When positive polarity is selected:***

When "1" is written: Rising edge of SCLK
When "0" is written: Falling edge of SCLK
Reading: Valid

Select whether the fetching for the serial input data to registers (SD0–SD7) at the rising edge or falling edge of the synchronous signal.
Pay attention to the polarity of the synchronous clock selected by the mask option because the selection content is different.
The input data fetch timing may be selected but output timing for output data is fixed at the falling edge of $\overline{\text{SCLK}}$ (when negative polarity is selected) or at the rising edge of SCLK (when positive polarity is selected).
At initial reset, this register is set to "0".

SDP: Data input/output permutation selection register (FF71H•D3)

Selects the serial data input/output permutation.

When "1" is written: MSB first
When "0" is written: LSB first
Reading: Valid

Select whether the data input/output permutation will be MSB first or LSB first.
At initial reset, this register is set to "0".

SCTRG: Clock trigger/status (FF70H•D1)

This is a trigger to start input/output of synchronous clock ($\overline{\text{SCLK}}$).

- ***When writing***

When "1" is written: Trigger
When "0" is written: No operation

When this trigger is supplied to the serial interface activating circuit, the synchronous clock ($\overline{\text{SCLK}}$) input/output is started.
As a trigger condition, it is required that data writing or reading on data registers SD0–SD7 be performed prior to writing "1" to SCTRG. (The internal circuit of the serial interface is initiated through data writing/reading on data registers SD0–SD7.) In addition, be sure to enable the serial interface with the ESIF register before setting the trigger.
Supply trigger only once every time the serial interface is placed in the RUN state. Refrain from performing trigger input multiple times, as leads to malfunctioning.
Moreover, when the synchronous clock $\overline{\text{SCLK}}$ is external clock, start to input the external clock after the trigger.

- ***When reading***

When "1" is read: RUN (during input/output the synchronous clock)
When "0" is read: STOP (the synchronous clock stops)
Writing: Invalid

When this bit is read, it indicates the status of serial interface clock.
After "1" is written to SCTRG, this value is latched till serial interface clock stops (8 clock counts). Therefore, if "1" is read, it indicates that the synchronous clock is in input/output operation.
When the synchronous clock input/output is completed, this latch is reset to "0".
At initial reset, this bit is set to "0".

SD0–SD3, SD4–SD7: Serial interface data register (FF72H, FF73H)

These registers are used for writing and reading serial data.

- ***When writing***

When "1" is written: High level
When "0" is written: Low level

Write data to be output in these registers. The register data is converted into serial data and output from the SOUT (P11) terminal; data bits set at "1" are output as high (V_{DD}) level and data bits set at "0" are output as low (V_{SS}) level.

- ***When reading***

When "1" is read: High level
When "0" is read: Low level

The serial data input from the SIN (P10) terminal can be read from these registers.
The serial data input from the SIN (P10) terminal is converted into parallel data, as a high (V_{DD}) level bit into "1" and as a low (V_{SS}) level bit into "0", and is loaded to these registers. Perform data reading only while the serial interface is not running (i.e., the synchronous clock is neither being input or output).

At initial reset, these registers are undefined.

EISIF: Interrupt mask register (FFE3H•D0)

Masking the interrupt of the serial interface can be selected with this register.

When "1" is written: Enabled
When "0" is written: Masked
Reading: Valid

With this register, it is possible to select whether the serial interface interrupt is to be masked or not.
At initial reset, this register is set to "0".

ISIF: Interrupt factor flag (FFF3H•D0)

This flag indicates the occurrence of serial interface interrupt.

When "1" is read: Interrupt has occurred
When "0" is read: Interrupt has not occurred
Writing: Invalid

From the status of this flag, the software can decide whether the serial interface interrupt.
This flag is set to "1" after an 8-bit data input/output even if the interrupt is masked.
This flag is reset to "0" by writing "1" to it.
After an interrupt occurs, the same interrupt will occur again if the interrupt enabled state (I flag = "1") is set or the RETI instruction is executed unless the interrupt factor flag is reset. Therefore, be sure to reset (write "1" to) the interrupt factor flag in the interrupt service routine before shifting to the interrupt enabled state.
At initial reset, this flag is set to "0".

4.12.6 Programming notes

(1) Perform data writing/reading to the data registers SD0–SD7 only while the serial interface is not running (i.e., the synchronous clock is neither being input or output).

(2) As a trigger condition, it is required that data writing or reading on data registers SD0–SD7 be performed prior to writing "1" to SCTRG. (The internal circuit of the serial interface is initiated through data writing/reading on data registers SD0–SD7.) In addition, be sure to enable the serial interface with the ESIF register before setting the trigger.
Supply trigger only once every time the serial interface is placed in the RUN state. Refrain from performing trigger input multiple times, as leads to malfunctioning. Moreover, when the synchronous clock $\overline{\text{SCLK}}$ is external clock, start to input the external clock after the trigger.

(3) Setting of the input/output permutation (MSB first/LSB first) with the SDP register should be done before setting data to SD0–SD7.

(4) After an interrupt occurs, the same interrupt will occur again if the interrupt enabled state (I flag = "1") is set or the RETI instruction is executed unless the interrupt factor flag is reset. Therefore, be sure to reset (write "1" to) the interrupt factor flag in the interrupt service routine before shifting to the interrupt enabled state.

4.13 Buzzer Output Circuit

4.13.1 Configuration of buzzer output circuit

The E0C63B08 is capable of generating buzzer signal to drive a piezo-electric buzzer. The buzzer signal is output from the BZ terminal by software control. Furthermore, the buzzer signal frequency can be set to 2 kHz or 4 kHz by software.
Figure 4.13.1.1 shows the configuration of the buzzer output circuit.

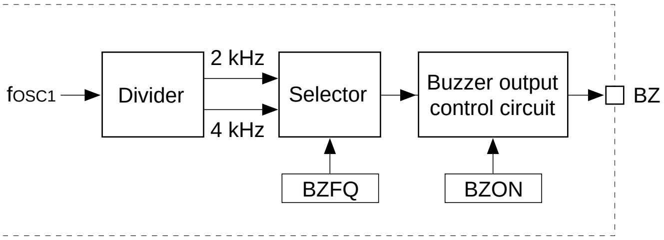
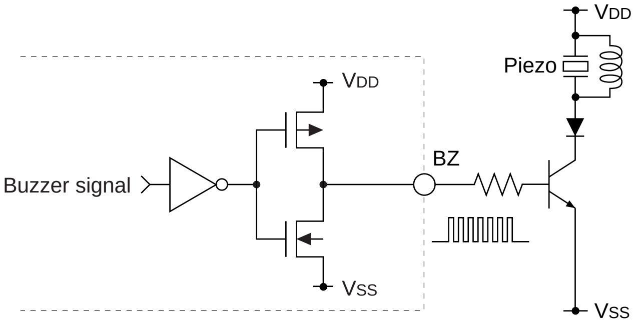


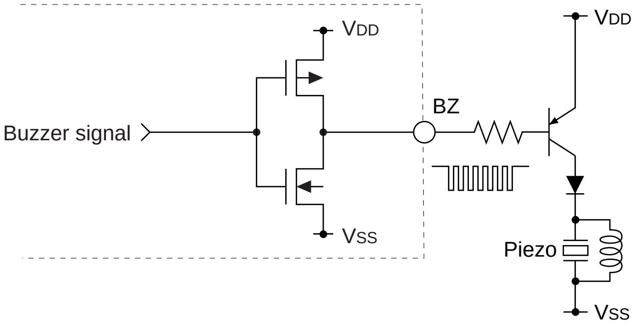
Fig. 4.13.1.1 Configuration of buzzer output circuit

4.13.2 Mask option

Polarity of the buzzer signal output from the BZ terminal can be selected as either positive polarity or negative polarity. Figure 4.13.2.1 shows each output circuit configuration and the output waveform.
When positive polarity is selected, the BZ terminal goes to a low (VSS) level when the buzzer signal is not output. Select positive polarity when driving a piezo buzzer by externally connecting an NPN transistor.
When negative polarity is selected, the BZ terminal goes to a high (VDD) level when the buzzer signal is not output. Select negative polarity when driving a piezo buzzer by externally connecting a PNP transistor.



(a) When positive polarity is selected



(b) When negative polarity is selected

Fig. 4.13.2.1 Configuration of output circuit

4.13.3 Control of buzzer output

The buzzer signal frequency is selected by the buzzer frequency selection register BZFQ. When "1" is written to the BZFQ register, the frequency is set to 2 kHz. When "0" is written, it is set to 4 kHz. This signal is generated by dividing the f_{OSC1}.

f_{OSC1}	2 kHz	4 kHz
32.768 kHz	f_{OSC1} /16	f_{OSC1} /8
76.8 kHz	f_{OSC1} /32	f_{OSC1} /16
153.6 kHz	f_{OSC1} /64	f_{OSC1} /32

The buzzer signal is output from the BZ terminal by writing "1" to the buzzer output control register BZON.

When negative polarity is selected, the BZ terminal goes to a high (V_{DD}) level by writing "0" to the BZON register. When positive polarity is selected, the BZ terminal goes to a low (V_{SS}) level by writing "0".

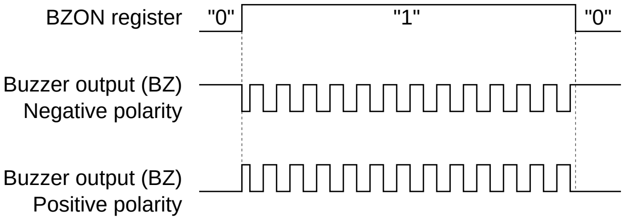


Fig. 4.13.3.1 Timing chart of buzzer signal output

Note: Since it generates a buzzer signal that is out of synchronization with the BZON register, hazards may at times be produced when the signal goes ON/OFF due to the setting of the BZON register.

4.13.4 I/O memory of buzzer output circuit

Table 4.13.4.1 shows the I/O address and the control bits for the buzzer output circuit.

Table 4.13.4.1 Control bits of buzzer output circuit

Address	Register								Comment
	D3	D2	D1	D0	Name	Init *1	1	0	
FF64H	0	0	BZFQ	BZON	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R		R/W		BZFQ	0	2 kHz	4 kHz	Buzzer frequency selection
					BZON	0	On	Off	Buzzer output On/Off

*1 Initial value at initial reset

*2 Not set in the circuit

*3 Constantly "0" when being read

BZFQ: Buzzer frequency selection register (FF64H•D1)

Selects the buzzer signal frequency.

When "1" is written: 2 kHz
When "0" is written: 4 kHz
Reading: Valid

When "1" is written to BZFQ, the frequency is set to 2 kHz. When "0" is written, it is set to 4 kHz.
At initial reset, this register is set to "0".

BZON: Buzzer output control (ON/OFF) register (FF64H•D0)

Controls the buzzer signal output.

When "1" is written: Buzzer output ON
When "0" is written: Buzzer output OFF
Reading: Valid

When "1" is written to BZON, the buzzer signal is output from the BZ terminal. When "0" is written, the BZ terminal goes to a high (VDD) level (when negative polarity is selected by mask option) or to a low (VSS) level (when positive polarity is selected by mask option).
At initial reset, this register is set to "0".

4.13.5 Programming note

Since it generates a buzzer signal that is out of synchronization with the BZON register, hazards may at times be produced when the signal goes ON/OFF due to the setting of the BZON register.

4.14 SVD (Supply Voltage Detection) Circuit

4.14.1 Configuration of SVD circuit

The E0C63B08 has a built-in SVD (supply voltage detection) circuit, so that the software can find when the source voltage lowers. Turning the SVD circuit ON/OFF and the SVD criteria voltage setting can be done with software.
Figure 4.14.1.1 shows the configuration of the SVD circuit.

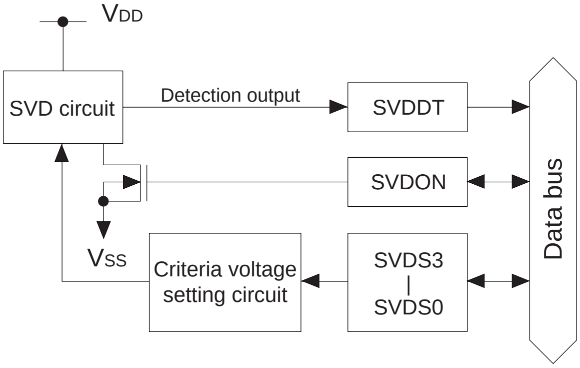


Fig. 4.14.1.1 Configuration of SVD circuit

4.14.2 SVD operation

The SVD circuit compares the criteria voltage set by software and the supply voltage (VDD–VSS) and sets its results into the SVDDT latch. By reading the data of this SVDDT latch, it can be determined by means of software whether the supply voltage is normal or has dropped.
The criteria voltage can be set for the 16 types shown in Table 4.14.2.1 by the SVDS3–SVDS0 registers.

Table 4.14.2.1 Criteria voltage setting

SVDS3	SVDS2	SVDS1	SVDS0	Criteria voltage (V)
0	1	1	1	1.60
0	1	1	0	1.40
0	1	0	1	1.30
0	1	0	0	1.25
0	0	1	1	1.20
0	0	1	0	1.15
0	0	0	1	1.10
0	0	0	0	1.05

SVDS3	SVDS2	SVDS1	SVDS0	Criteria voltage (V)
1	1	1	1	2.60
1	1	1	0	2.50
1	1	0	1	2.30
1	1	0	0	2.20
1	0	1	1	2.10
1	0	1	0	2.05
1	0	0	1	2.00
1	0	0	0	1.95

When the SVDON register is set to "1", source voltage detection by the SVD circuit is executed. As soon as the SVDON register is reset to "0", the result is loaded to the SVDDT latch and the SVD circuit goes OFF. To obtain a stable detection result, the SVD circuit must be ON for at least l00 µsec. So, to obtain the SVD detection result, follow the programming sequence below.

1. Set SVDON to "1"
2. Maintain for 100 µsec minimum
3. Set SVDON to "0"
4. Read SVDDT

When the SVD circuit is ON, the IC draws a large current, so keep the SVD circuit off unless it is.

4.14.3 I/O memory of SVD circuit

Table 4.14.3.1 shows the I/O addresses and the control bits for the SVD circuit.

Table 4.14.3.1 Control bits of SVD circuit

Address	Register								Comment
	D3	D2	D1	D0	Name	Init *1	1	0	
FF04H	SVDS3	SVDS2	SVDS1	SVDS0	SVDS3	0			SVD criteria voltage setting [SVDS3–0] 0 1 2 3 4 5 6 7 Voltage(V) 1.05 1.10 1.15 1.20 1.25 1.30 1.40 1.60 [SVDS3–0] 8 9 10 11 12 13 14 15 Voltage(V) 1.95 2.00 2.05 2.10 2.20 2.30 2.50 2.60
					SVDS2	0			
	R/W				SVDS1	0			
					SVDS0	0			
FF05H	0	0	SVDDT	SVDON	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R			R/W	SVDDT	0	Low	Normal	SVD evaluation data
					SVDON	0	On	Off	SVD circuit On/Off

*1 Initial value at initial reset

*2 Not set in the circuit

*3 Constantly "0" when being read

SVDS3–SVDS0: SVD criteria voltage setting register (FF04H)

Criteria voltage for SVD is set as shown in Table 4.14.2.1.
At initial reset, this register is set to "0".

SVDON: SVD control (ON/OFF) register (FF05H•D0)

Turns the SVD circuit ON and OFF.

When "1" is written: SVD circuit ON
When "0" is written: SVD circuit OFF
Reading: Valid

When the SVDON register is set to "1", a source voltage detection is executed by the SVD circuit. As soon as SVDON is reset to "0", the result is loaded to the SVDDT latch. To obtain a stable detection result, the SVD circuit must be ON for at least 100 μsec.
At initial reset, this register is set to "0".

SVDDT: SVD data (FF05H•D1)

This is the result of supply voltage detection.

When "0" is read: Supply voltage (VDD–VSS) ≥ Criteria voltage
When "1" is read: Supply voltage (VDD–VSS) < Criteria voltage
Writing: Invalid

The result of supply voltage detection at time of SVDON is set to "0" can be read from this latch.
At initial reset, SVDDT is set to "0".

4.14.4 Programming notes

(1) To obtain a stable detection result, the SVD circuit must be ON for at least 100 μsec. So, to obtain the SVD detection result, follow the programming sequence below.

1. Set SVDON to "1"
2. Maintain for 100 μsec minimum
3. Set SVDON to "0"
4. Read SVDDT

(2) The SVD circuit should normally be turned OFF because SVD operation increase current consumption.

4.15 Gate Array (Custom Block)

4.15.1 Outline

The E0C63B08 has a gate array (G/A) built-in. It is possible to design peripheral circuits required in addition to the peripheral circuits that have been built in as the standard specification, and to implement to the IC. Thus the E0C63B08 can realize wide applications with one chip as a custom microcomputer that decreases the development cost.
The following shows the characteristics of the built-in G/A.

• Gate density	Maximum 11,000 gates (2-input NAND gate conversion)
• G/A type	Sea of Gates type
• Number of I/O terminals	16 bits
• CPU interface	Bus interface

Refer to the "E0C63A/B Series Gate Array Design Manual" for details of the G/A development.

4.15.2 CPU interface

Figure 4.15.2.1 and Table 4.15.2.1 show the interface signals between the CPU and the G/A.

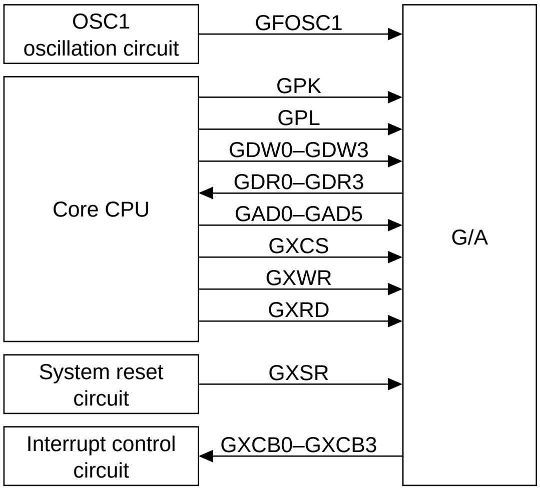


Fig. 4.15.2.1 Interface with core CPU

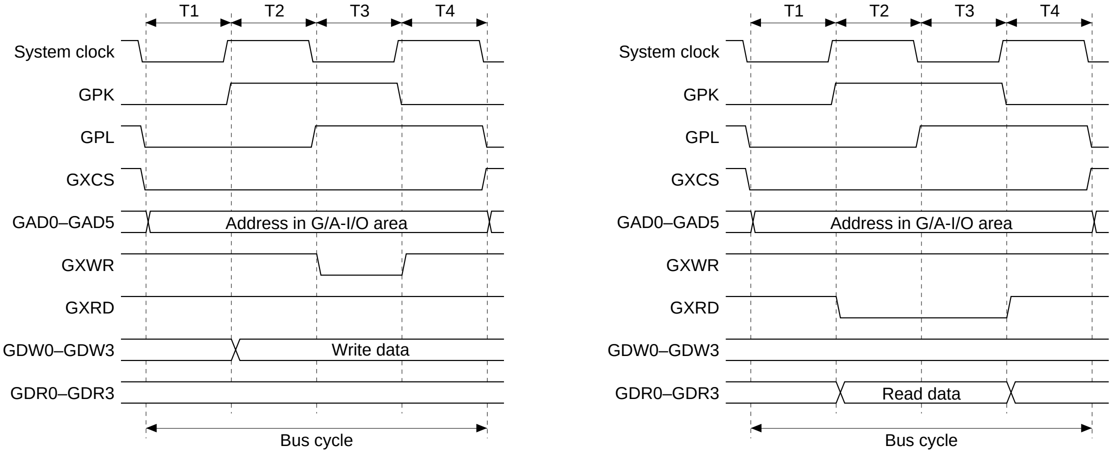
The data transfer between the core CPU and the custom block (peripheral circuit) is done via the bus interface. Up to 64-word I/O memory can be used to assign control registers and data registers according to the custom block (peripheral circuit) to be developed.

Table 4.15.2.1 Interface signals

Signal classification	Signal name	CPU↔G/A	Function
Clock	GFOSC1	→	Clock signal output from the OSC1 oscillation circuit
	GPK	→	2-phase divided clock generated from the system clock
	GPL	→	
Data bus	GDW0–GDW3	→	4-bit data bus (for writing)
	GDR0–GDR3	←	4-bit data bus (for reading)
Address bus	GAD0–GAD5	→	Data address bus
Bus control signal	GXCS	→	Chip select signal for G/A-I/O area (FF80H–FFBFH)
	GXWR	→	Data write signal for G/A-I/O area (FF80H–FFBFH)
	GXRD	→	Data read signal for G/A-I/O area (FF80H–FFBFH)
System control signal	GXSR	→	Reset signal
Interrupt signal	GXCB0–GXCB3	←	Interrupt request signal to the CPU

The control registers and the data registers of the custom block (peripheral circuits) developed are assigned to FF80H–FFBFH in the I/O memory area. It is possible to control (read/write) them the same as other peripheral circuits built into the E0C63B08.

Figure 4.15.2.2 shows the timing chart while accessing the I/O memory.



(a) When 4-bit data is written *(b) When 4-bit data is read*

Fig. 4.15.2.2 Data write/read timing

4.15.3 Interrupt function

4 systems of the interrupts (CB0–CB3) can be used for the custom block. The control method of the interrupt is similar to the other peripheral circuits that have an interrupt function. The interrupt factor flags (ISCB0–ISCB3) and the interrupt mask registers (EISB0–EISB3) are assigned as shown in Table 4.15.3.1.

Table 4.15.3.1 Control addresses for custom block interrupts

Interrupt request	Interrupt factor flag	Interrupt mask register
CB3	ISCB3 (FFF0H•D3)	EISCB3 (FFE0H•D3)
CB2	ISCB2 (FFF0H•D2)	EISCB2 (FFE0H•D2)
CB1	ISCB1 (FFF0H•D1)	EISCB1 (FFE0H•D1)
CB0	ISCB0 (FFF0H•D0)	EISCB0 (FFE0H•D0)

Generation of an interrupt factor (falling edge) sets the corresponding interrupt factor flag to "1", and the interrupt occurs to the CPU. The interrupt can be masked by setting the corresponding interrupt mask register to "0". However, the interrupt factor flag is set to "1" at the falling edge of the corresponding signal regardless of the interrupt mask register setting.

4.15.4 I/O memory of custom block

Table 4.15.4.1 shows the I/O addresses and the control bits that have been set for the custom block.

Table 4.15.4.1 Control bits of custom block

Address	Register								Comment
	D3	D2	D1	D0	Name	Init *1	1	0	
FFE0H	EISCB3	EISCB2	EISCB1	EISCB0	EISCB3	0	Enable	Mask	Interrupt mask register (Custom block 3)
					EISCB2	0	Enable	Mask	Interrupt mask register (Custom block 2)
	R/W				EISCB1	0	Enable	Mask	Interrupt mask register (Custom block 1)
					EISCB0	0	Enable	Mask	Interrupt mask register (Custom block 0)
FFF0H	ISCB3	ISCB2	ISCB1	ISCB0	ISCB3	0	(R)	(R)	Interrupt factor flag (Custom block 3)
					ISCB2	0	Yes	No	Interrupt factor flag (Custom block 2)
	R/W				ISCB1	0	(W)	(W)	Interrupt factor flag (Custom block 1)
					ISCB0	0	Reset	Invalid	Interrupt factor flag (Custom block 0)

*1 Initial value at initial reset

*2 Not set in the circuit

*3 Constantly "0" when being read

EISCB0: Custom block 0 interrupt mask register (FFE0H•D0)
EISCB1: Custom block 1 interrupt mask register (FFE0H•D1)
EISCB2: Custom block 2 interrupt mask register (FFE0H•D2)
EISCB3: Custom block 3 interrupt mask register (FFE0H•D3)

Masking the interrupts of the custom block can be selected with these registers.

When "1" is written: Enable
When "1" is written: Mask
Reading: Valid

Four interrupt factors (CB0, CB1, CB2, CB4) can be masked with the interrupt mask registers EISCB0 (CB0), EISCB1 (CB1), EISCB2 (CB2) and EISCB3 (CB3) individually.
At initial reset, these registers are set to "0".

ISCB0: Custom block 0 interrupt factor flag (FFF0H•D0)
ISCB1: Custom block 1 interrupt factor flag (FFF0H•D1)
ISCB2: Custom block 2 interrupt factor flag (FFF0H•D2)
ISCB3: Custom block 3 interrupt factor flag (FFF0H•D3)

These flags indicate the occurrence of custom block interrupts.

When "1" is read: Interrupt has occurred
When "0" is read: Interrupt has not occurred

When "1" is written: Flag is reset
When "0" is written: Invalid

The interrupt factor flags ISCB0, ISCB1, ISCB2 and ISCB3 are associated with CB0, CB1, CB2 and CB3 interrupts, respectively. From the status of these flags, the software can decide whether a custom block interrupt has occurred. The interrupt factor flag is set to "1" at the falling edge of the corresponding signal regardless of the interrupt mask register setting.
These flags are reset to "0" by writing "1" to them.
After an interrupt occurs, the same interrupt will occur again if the interrupt enabled state (I flag = "1") is set or the RETI instruction is executed unless the interrupt factor flag is reset. Therefore, be sure to reset (write "1" to) the interrupt factor flag in the interrupt service routine before shifting to the interrupt enabled state.
At initial reset, these flags are set to "0".

4.15.5 Programming note

After an interrupt occurs, the same interrupt will occur again if the interrupt enabled state (I flag = "1") is set or the RETI instruction is executed unless the interrupt factor flag is reset. Therefore, be sure to reset (write "1" to) the interrupt factor flag in the interrupt service routine before shifting to the interrupt enabled state.

4.16 Interrupt and HALT

<Interrupt types>

The E0C63B08 provides the following interrupt functions.

External interrupt:	• Input interrupt	(2 systems)
Internal interrupt:	• Watchdog timer interrupt	(NMI, 1 system)
	• Custom block (gate array) interrupt	(4 systems)
	• Programmable timer interrupt	(2 systems)
	• Serial interface interrupt	(1 system)
	• Timer interrupt	(4 systems)
	• Stopwatch timer interrupt	(2 systems)

To authorize interrupt, the interrupt flag must be set to "1" (EI) and the necessary related interrupt mask registers must be set to "1" (enable).
When an interrupt occurs the interrupt flag is automatically reset to "0" (DI), and interrupts after that are inhibited.

The watchdog timer interrupt is an NMI (non-maskable interrupt), therefore, the interrupt is generated regardless of the interrupt flag setting. Also the interrupt mask register is not provided. However, it is possible to not generate NMI since software can stop the watchdog timer operation.

Figure 4.16.1 shows the configuration of the interrupt circuit.

Note: After an initial reset, all the interrupts including NMI are masked until both the stack pointers SP1 and SP2 are set with the software. Be sure to set the SP1 and SP2 in the initialize routine.
Further, when re-setting the stack pointer, the SP1 and SP2 must be set as a pair. When one of them is set, all the interrupts including NMI are masked and interrupts cannot be accepted until the other one is set.

<HALT>

The E0C63B08 has HALT functions that considerably reduce the current consumption when it is not necessary.
The CPU enters HALT status when the HALT instruction is executed.
In HALT status, the operation of the CPU is stopped. However, timers continue counting since the oscillation circuit operates. Reactivating the CPU from HALT status is done by generating a hardware interrupt request including NMI.

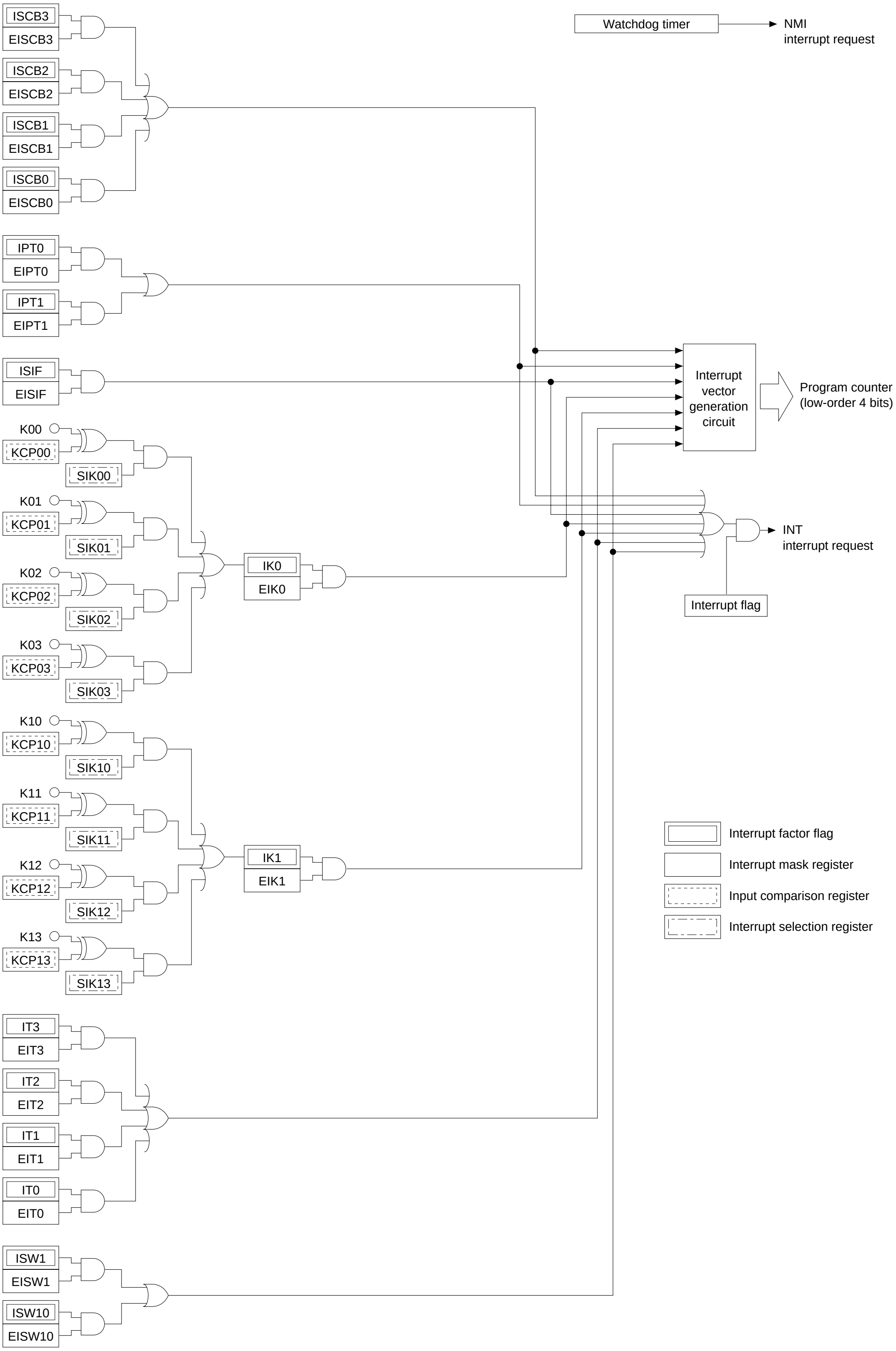


Fig. 4.16.1 Configuration of the interrupt circuit

4.16.1 Interrupt factor

Table 4.16.1.1 shows the factors for generating interrupt requests.

The interrupt flags are set to "1" depending on the corresponding interrupt factors.
The CPU operation is interrupted when an interrupt factor flag is set to "1" if the following conditions are established.

- The corresponding mask register is "1" (enabled)
- The interrupt flag is "1" (EI)

The interrupt factor flag is reset to "0" when "1" is written.
At initial reset, the interrupt factor flags are reset to "0".

∗ Since the watchdog timer's interrupt is NMI, the interrupt is generated regardless of the setting above, and no interrupt factor flag is provided.

Table 4.16.1.1 Interrupt factors

Interrupt factor	Interrupt factor flag
Custom block 3 (falling edge)	ISCB3 (FFF0H•D3)
Custom block 2 (falling edge)	ISCB2 (FFF0H•D2)
Custom block 1 (falling edge)	ISCB1 (FFF0H•D1)
Custom block 0 (falling edge)	ISCB0 (FFF0H•D0)
Programmable timer 1 (counter = 0)	IPT1 (FFF2H•D1)
Programmable timer 0 (counter = 0)	IPT0 (FFF2H•D0)
Serial interface (8-bit data input/output completion)	ISIF (FFF3H•D0)
K00–K03 input (falling edge or rising edge)	IK0 (FFF4H•D0)
K10–K13 input (falling edge or rising edge)	IK1 (FFF5H•D0)
Clock timer 1 Hz (falling edge)	IT3 (FFF6H•D3)
Clock timer 2 Hz (falling edge)	IT2 (FFF6H•D2)
Clock timer 8 Hz (falling edge)	IT1 (FFF6H•D1)
Clock timer 16 Hz (falling edge)	IT0 (FFF6H•D0)
Stopwatch timer (1 Hz)	ISW1 (FFF7H•D1)
Stopwatch timer (10 Hz)	ISW10 (FFF7H•D0)

Note: After an interrupt occurs, the same interrupt will occur again if the interrupt enabled state (I flag = "1") is set or the RETI instruction is executed unless the interrupt factor flag is reset. Therefore, be sure to reset (write "1" to) the interrupt factor flag in the interrupt service routine before shifting to the interrupt enabled state.

4.16.2 Interrupt mask

The interrupt factor flags can be masked by the corresponding interrupt mask registers.
The interrupt mask registers are read/write registers. They are enabled (interrupt authorized) when "1" is written to them, and masked (interrupt inhibited) when "0" is written to them.
At initial reset, the interrupt mask register is set to "0".
Table 4.16.2.1 shows the correspondence between interrupt mask registers and interrupt factor flags.

Table 4.16.2.1 Interrupt mask registers and interrupt factor flags

Interrupt mask register		Interrupt factor flag	
EISCB3	(FFE0H•D3)	ISCB3	(FFF0H•D3)
EISCB2	(FFE0H•D2)	ISCB2	(FFF0H•D2)
EISCB1	(FFE0H•D1)	ISCB1	(FFF0H•D1)
EISCB0	(FFE0H•D0)	ISCB0	(FFF0H•D0)
EIPT1	(FFE2H•D1)	IPT1	(FFF2H•D1)
EIPT0	(FFE2H•D0)	IPT0	(FFF2H•D0)
EISIF	(FFE3H•D0)	ISIF	(FFF3H•D0)
EIK0	(FFE4H•D0)	IK0	(FFF4H•D0)
EIK1	(FFE5H•D0)	IK1	(FFF5H•D0)
EIT3	(FFE 6H•D3)	IT3	(FFF6H•D3)
EIT2	(FFE6H•D2)	IT2	(FFF6H•D2)
EIT1	(FFE6H•D1)	IT1	(FFF6H•D1)
EIT0	(FFE6H•D0)	IT0	(FFF6H•D0)
EISW1	(FFE7H•D1)	ISW1	(FFF7H•D1)
EISW10	(FFE7H•D0)	ISW10	(FFF7H•D0)

4.16.3 Interrupt vector

When an interrupt request is input to the CPU, the CPU begins interrupt processing. After the program being executed is terminated, the interrupt processing is executed in the following order.

1. The content of the flag register is evacuated, then the I flag is reset.
2. The address data (value of program counter) of the program to be executed next is saved in the stack area (RAM).
3. The interrupt request causes the value of the interrupt vector (0100H–010EH) to be set in the program counter.
4. The program at the specified address is executed (execution of interrupt processing routine by software).

Table 4.16.3.1 shows the correspondence of interrupt requests and interrupt vectors.

Table 4.16.3.1 Interrupt request and interrupt vectors

Interrupt vector	Interrupt factor	Priority
0100H	Watchdog timer	High
0102H	Custom block	↑
0104H	Programmable timer	
0106H	Serial interface	
0108H	K00–K03 input	
010AH	K10–K13 input	
010CH	Clock timer	↓
010EH	Stopwatch timer	Low

The four low-order bits of the program counter are indirectly addressed through the interrupt request.

4.16.4 I/O memory of interrupt

Tables 4.16.4.1(a) and (b) show the I/O addresses and the control bits for controlling interrupts.

Table 4.16.4.1(a) Control bits of interrupt (1)

Address	Register								Comment
	D3	D2	D1	D0	Name	Init *1	1	0	
FF20H	SIK03	SIK02	SIK01	SIK00	SIK03	0	Enable	Disable	K00–K03 interrupt selection register
					SIK02	0	Enable	Disable	
	R/W				SIK01	0	Enable	Disable	
					SIK00	0	Enable	Disable	
FF22H	KCP03	KCP02	KCP01	KCP00	KCP03	1	↓	↑	K00–K03 input comparison register
					KCP02	1	↓	↑	
	R/W				KCP01	1	↓	↑	
					KCP00	1	↓	↑	
FF24H	SIK13	SIK12	SIK11	SIK10	SIK13	0	Enable	Disable	K10–K13 interrupt selection register
					SIK12	0	Enable	Disable	
	R/W				SIK11	0	Enable	Disable	
					SIK10	0	Enable	Disable	
FF26H	KCP13	KCP12	KCP11	KCP10	KCP13	1	↓	↑	K10–K13 input comparison register
					KCP12	1	↓	↑	
	R/W				KCP11	1	↓	↑	
					KCP10	1	↓	↑	
FFE0H	EISCB3	EISCB2	EISCB1	EISCB0	EISCB3	0	Enable	Mask	Interrupt mask register (Custom block 3)
					EISCB2	0	Enable	Mask	Interrupt mask register (Custom block 2)
	R/W				EISCB1	0	Enable	Mask	Interrupt mask register (Custom block 1)
					EISCB0	0	Enable	Mask	Interrupt mask register (Custom block 0)
FFE2H	0	0	EIPT1	EIPT0	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R		R/W		EIPT1	0	Enable	Mask	Interrupt mask register (Programmable timer 1)
					EIPT0	0	Enable	Mask	Interrupt mask register (Programmable timer 0)
FFE3H	0	0	0	EISIF	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R			R/W	0 *3	– *2			Unused
					EISIF	0	Enable	Mask	Interrupt mask register (Serial I/F)
FFE4H	0	0	0	EIK0	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R			R/W	0 *3	– *2			Unused
					EIK0	0	Enable	Mask	Interrupt mask register (K00–K03)
FFE5H	0	0	0	EIK1	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R			R/W	0 *3	– *2			Unused
					EIK1	0	Enable	Mask	Interrupt mask register (K10–K13)
FFE6H	EIT3	EIT2	EIT1	EIT0	EIT3	0	Enable	Mask	Interrupt mask register (Clock timer 1 Hz)
					EIT2	0	Enable	Mask	Interrupt mask register (Clock timer 2 Hz)
	R/W				EIT1	0	Enable	Mask	Interrupt mask register (Clock timer 8 Hz)
					EIT0	0	Enable	Mask	Interrupt mask register (Clock timer 16 Hz)
FFE7H	0	0	EISW1	EISW10	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R		R/W		EISW1	0	Enable	Mask	Interrupt mask register (Stopwatch timer 1 Hz)
					EISW10	0	Enable	Mask	Interrupt mask register (Stopwatch timer 10 Hz)

*1 Initial value at initial reset

*2 Not set in the circuit

*3 Constantly "0" when being read

Table 4.16.4.1(b) Control bits of interrupt (2)

Address	Register								Comment
	D3	D2	D1	D0	Name	Init *1	1	0	
FFF0H	ISCB3	ISCB2	ISCB1	ISCB0	ISCB3	0	(R)	(R)	Interrupt factor flag (Custom block 3)
					ISCB2	0	Yes	No	Interrupt factor flag (Custom block 2)
	R/W				ISCB1	0	(W)	(W)	Interrupt factor flag (Custom block 1)
					ISCB0	0	Reset	Invalid	Interrupt factor flag (Custom block 0)
FFF2H	0	0	IPT1	IPT0	0 *3	– *2	(R)	(R)	Unused
					0 *3	– *2	Yes	No	Unused
	R		R/W		IPT1	0	(W)	(W)	Interrupt factor flag (Programmable timer 1)
					IPT0	0	Reset	Invalid	Interrupt factor flag (Programmable timer 0)
FFF3H	0	0	0	ISIF	0 *3	– *2	(R)	(R)	Unused
					0 *3	– *2	Yes	No	Unused
	R			R/W	0 *3	– *2	(W)	(W)	Unused
					ISIF	0	Reset	Invalid	Interrupt factor flag (Serial I/F)
FFF4H	0	0	0	IK0	0 *3	– *2	(R)	(R)	Unused
					0 *3	– *2	Yes	No	Unused
	R			R/W	0 *3	– *2	(W)	(W)	Unused
					IK0	0	Reset	Invalid	Interrupt factor flag (K00–K03)
FFF5H	0	0	0	IK1	0 *3	– *2	(R)	(R)	Unused
					0 *3	– *2	Yes	No	Unused
	R			R/W	0 *3	– *2	(W)	(W)	Unused
					IK1	0	Reset	Invalid	Interrupt factor flag (K10–K13)
FFF6H	IT3	IT2	IT1	IT0	IT3	0	(R)	(R)	Interrupt factor flag (Clock timer 1 Hz)
					IT2	0	Yes	No	Interrupt factor flag (Clock timer 2 Hz)
	R/W				IT1	0	(W)	(W)	Interrupt factor flag (Clock timer 8 Hz)
					IT0	0	Reset	Invalid	Interrupt factor flag (Clock timer 16 Hz)
FFF7H	0	0	ISW1	ISW10	0 *3	– *2	(R)	(R)	Unused
					0 *3	– *2	Yes	No	Unused
	R		R/W		ISW1	0	(W)	(W)	Interrupt factor flag (Stopwatch timer 1 Hz)
					ISW10	0	Reset	Invalid	Interrupt factor flag (Stopwatch timer 10 Hz)

*1 Initial value at initial reset
*2 Not set in the circuit
*3 Constantly "0" when being read

EISCB3–EISCB0: Interrupt mask registers (FFE0H)
ISCB3–ISCB0: Interrupt factor flags (FFF0H)
Refer to Section 4.15, "Gate Array".

EIPT1, EIPT0: Interrupt mask registers (FFE2H•D1, D0)
IPT1, IPT0: Interrupt factor flags (FFF2H•D1, D0)
Refer to Section 4.11, "Programmable Timer".

EISIF: Interrupt mask register (FFE3H•D0)
ISIF: Interrupt factor flag (FFF3H•D0)
Refer to Section 4.12, "Serial Interface".

KCP03–KCP00, KCP13–KCP10: Input comparison registers (FF22H, FF26H)
SIK03–SIK00, SIK13–SIK10: Interrupt selection registers (FF20H, FF24H)
EIK0, EIK1: Interrupt mask registers (FFE4H•D0, FFE5H•D0)
IK0, IK1: Interrupt factor flags (FFF4H•D0, FFF5H•D0)
Refer to Section 4.5, "Input Ports".

EIT3–EIT0: Interrupt mask registers (FFE6H)
IT3–IT0: Interrupt factor flags (FFF6H)
Refer to Section 4.9, "Clock Timer".

EISW1, EISW10: Interrupt mask registers (FFE7H•D1, D0)
ISW1, ISW10: Interrupt factor flags (FFF7H•D1, D0)
Refer to Section 4.10, "Stopwatch Timer".

4.16.5 Programming notes

(1) The interrupt factor flags are set when the interrupt condition is established, even if the interrupt mask registers are set to "0".

(2) After an interrupt occurs, the same interrupt will occur again if the interrupt enabled state (I flag = "1") is set or the RETI instruction is executed unless the interrupt factor flag is reset. Therefore, be sure to reset (write "1" to) the interrupt factor flag in the interrupt service routine before shifting to the interrupt enabled state.

(3) After an initial reset, all the interrupts including NMI are masked until both the stack pointers SP1 and SP2 are set with the software. Be sure to set the SP1 and SP2 in the initialize routine.
Further, when re-setting the stack pointer, the SP1 and SP2 must be set as a pair. When one of them is set, all the interrupts including NMI are masked and interrupts cannot be accepted until the other one is set.

CHAPTER 5 SUMMARY OF NOTES

5.1 Notes for Low Current Consumption

The E0C63B08 contains control registers for each of the circuits so that current consumption can be reduced.
These control registers reduce the current consumption through programs that operate the circuits at the minimum levels.
The following lists the circuits that can control operation and their control registers. Refer to these when programming.

Table 5.1.1 Circuits and control registers

Circuit (and item)	Control register
CPU	HALT instruction
CPU operating frequency	CLKCHG, OSCC
Oscillation system voltage regulator	VDC
LCD system voltage circuit	LPWR
Supply voltage doubler/halver	DBON, HLON, VDSEL, VCSEL
SVD circuit	SVDON

Refer to Chapter 7, "Electrical Characteristics" for current consumption.

Below are the circuit statuses at initial reset.

CPU: Operating status

CPU operating frequency: Low speed side (CLKCHG = "0")
OSC3 oscillation circuit is in OFF status (OSCC = "0")

Oscillation system voltage regulator: Low speed side 1.2 V (VDC = "0")

LCD system voltage circuit: OFF status (LPWR = "0")

Supply voltage doubler/halver: Voltage regulator is driven with V_{DD}, Normal mode
(DBON = "0", HLON = "0", VDSEL = "0", VCSEL = "0")

SVD circuit: OFF status (SVDON = "0")

Also, be careful about panel selection because the current consumption can differ by the order of several μA on account of the LCD panel characteristics.

5.2 Summary of Notes by Function

Here, the cautionary notes are summed up by function category. Keep these notes well in mind when programming.

Memory and stack

(1) Memory is not implemented in unused areas within the memory map. Further, some non-implementation areas and unused (access prohibition) areas exist in the peripheral I/O area. If the program that accesses these areas is generated, its operation cannot be guaranteed. Refer to the I/O memory maps shown in Tables 4.1.1 (a)–(e) for the peripheral I/O area.

(2) Part of the RAM area is used as a stack area for subroutine call and register evacuation, so pay attention not to overlap the data area and stack area.

(3) The E0C63000 core CPU handles the stack using the stack pointer for 4-bit data (SP2) and the stack pointer for 16-bit data (SP1).
16-bit data are accessed in stack handling by SP1, therefore, this stack area should be allocated to the area where 4-bit/16-bit access is possible (0100H to 01FFH). The stack pointers SP1 and SP2 change cyclically within their respective range: the range of SP1 is 0000H to 03FFH and the range of SP2 is 0000H to 00FFH. Therefore, pay attention to the SP1 value because it may be set to 0200H or more exceeding the 4-bit/16-bit accessible range in the E0C63B08 or it may be set to 00FFH or less. Memory accesses except for stack operations by SP1 are 4-bit data access.
After initial reset, all the interrupts including NMI are masked until both the stack pointers SP1 and SP2 are set by software. Further, if either SP1 or SP2 is re-set when both are set already, the interrupts including NMI are masked again until the other is re-set. Therefore, the settings of SP1 and SP2 must be done as a pair.

Power supply and operating mode

(1) When operating the E0C63B08 with a 0.9–1.25 V power supply voltage, software control is necessary. Set both the oscillation system voltage regulator and the LCD system voltage circuit to doubler mode.

(2) If the power supply voltage is out of the specified voltage range for an operating mode, do not switch to the operating mode. It may cause malfunction or increase current consumption.

(3) Do not set the registers HLON (halves) and DBON (doubling) to "1" simultaneously.

(4) When switching from the normal mode to the doubler/halver mode, the VCSEL register should be set to "1" after taking a 100 msec or longer interval for the V_{D2} to stabilize from switching the DBON or HLON register to "1".

(5) When switching from the doubler/halver mode to the normal mode, use separate instructions to switch the mode (VDSEL = "0" or VCSEL = "0") and turn the voltage doubler/halver OFF (HLON = "0" or DBON = "0"). Simultaneous processing with a single instruction may cause malfunction.

(6) The OSC3 oscillation circuit cannot operate in halver mode. When the supply voltage is in the range of 0.9 V to 2.2 V, the OSC3 oscillation circuit can only operate in the doubler mode. When the supply voltage is in the range of 2.2 V to 3.6 V, it can operate in the normal mode.

Watchdog timer

(1) When the watchdog timer is being used, the software must reset it within 3-second cycles.

(2) Because the watchdog timer is set in operation state by initial reset, set the watchdog timer to disabled state (not used) before generating an interrupt (NMI) if it is not used.

Oscillation circuit

(1) The OSC1 oscillation circuit deals with three types of crystal oscillators (can be selected from 32.768 kHz, 76.8 kHz and 153.6 kHz by mask option), however, it is necessary to set the prescaler to correspond with the frequency of the oscillator being used. Be sure to set the prescaler properly in the initial routine, which is executed immediately after initial reset, before controlling peripheral circuits.

(2) When switching the CPU system clock from OSC1 to OSC3, first set V_{D1} and the operating mode. After that maintain 2.5 msec or more, and then turn the OSC3 oscillation ON.
When switching from OSC3 to OSC1, set V_{D1} and the operating mode after switching to OSC1 and turning the OSC3 oscillation OFF.

(3) It takes at least 5 msec from the time the OSC3 oscillation circuit goes ON until the oscillation stabilizes. Consequently, when switching the CPU operation clock from OSC1 to OSC3, do this after a minimum of 5 msec have elapsed since the OSC3 oscillation went ON.
Further, the oscillation stabilization time varies depending on the external oscillator characteristics and conditions of use, so allow ample margin when setting the wait time.

(4) When switching the clock form OSC3 to OSC1, use a separate instruction for switching the OSC3 oscillation OFF. An error in the CPU operation can result if this processing is performed at the same time by the one instruction.

(5) Switching the operating voltage when the power supply voltage is lower than the set voltage (that can generate V_{D1}) may cause malfunction. Switch the operating voltage only after making sure that the power supply voltage is more than the set voltage using the SVD circuit.

Input port

(1) When input ports are changed from low to high by pull-up resistors, the rise of the waveform is delayed on account of the time constant of the pull-up resistor and input gate capacitance. Hence, when fetching input ports, set an appropriate waiting time.
Particular care needs to be taken of the key scan during key matrix configuration.
Make this waiting time the amount of time or more calculated by the following expression.
$10 \times C \times R$
C: terminal capacitance 5 pF + parasitic capacitance ? pF
R: pull-up resistance 300 kΩ

(2) The K13 terminal functions as the clock input terminal for the programmable timer, and the input signal is shared with the input port and the programmable timer. Therefore, when the K13 terminal is set to the clock input terminal for the programmable timer, take care of the interrupt setting.

Output port

(1) When using the output port (R02, R03) as the special output port, fix the data register (R02, R03) at "1" and the high impedance control register (R02HIZ, R03HIZ) at "0" (data output).
Be aware that the output terminal is fixed at a low (V_{SS}) level the same as the DC output if "0" is written to the R02 and R03 registers when the special output has been selected.
Be aware that the output terminal shifts into high impedance status when "1" is written to the high impedance control register (R02HIZ, R03HIZ).

(2) A hazard may occur when the FOUT signal and the TOUT signal are turned ON and OFF.

(3) When f_{OSC3} is selected for the FOUT signal frequency, it is necessary to control the OSC3 oscillation circuit and the oscillation system voltage regulator before output.
Refer to Section 4.4, "Oscillation Circuit", for the control and notes.

I/O port

When in the input mode, I/O ports are changed from low to high by pull-up resistor, the rise of the waveform is delayed on account of the time constant of the pull-up resistor and input gate capacitance. Hence, when fetching input ports, set an appropriate wait time.
Particular care needs to be taken of the key scan during key matrix configuration.
Make this waiting time the amount of time or more calculated by the following expression.
$10 \times C \times R$
C: terminal capacitance 5 pF + parasitic capacitance ? pF
R: pull-up resistance 300 kΩ

LCD driver

(1) The contents of the display memory are undefined until the area is initialized (through, for instance, memory clear processing by the CPU). Initialize the display memory by executing initial processing.

(2) 100 msec or more time is necessary for stabilizing the LCD drive voltages VC1, VC2 and VC3 after setting the LCD power control register LPWR to "1". Be careful of the segment-on right after the power is turned on.

Clock timer

(1) To operate the clock timer correctly, the prescaler must be set to suit the crystal oscillator used for the OSC1 oscillation circuit.

(2) Be sure to read timer data in the order of low-order data (TM0–TM3) then high-order data (TM4–TM7).

Stopwatch timer

(1) To operate the stopwatch timer correctly, the prescaler must be set to suit the crystal oscillator used for the OSC1 oscillation circuit.

(2) When data of the counter is read at run mode, perform the reading after suspending the counter once and then set SWRUN to "1" again. Moreover, it is required that the suspension period not exceed 976 µsec (1/4 cycle of 256 Hz).

Programmable timer

(1) When reading counter data, be sure to read the low-order 4 bits (PTD00–PTD03, PTD10–PTD13) first. Furthermore, the high-order 4 bits (PTD04–PTD07, PTD14–PTD17) should be read within 0.73 msec of reading the low-order 4 bits (PTD00–PTD03, PTD10–PTD13).

(2) The programmable timer actually enters RUN/STOP status in synchronization with the falling edge of the input clock after writing to the PTRUN0/PTRUN1 register. Consequently, when "0" is written to the PTRUN0/PTRUN1 register, the timer enters STOP status at the point where the counter is decremented (-1). The PTRUN0/PTRUN1 register maintains "1" for reading until the timer actually stops.
Figure 5.2.1 shows the timing chart for the RUN/STOP control.

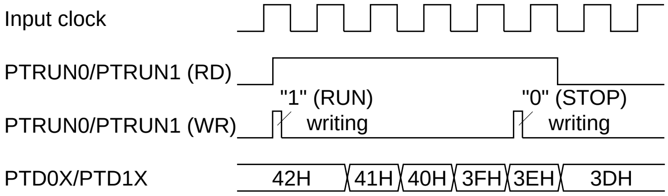


Fig. 5.2.1 Timing chart for RUN/STOP control

It is the same even in the event counter mode. Therefore, be aware that the counter does not enter RUN/STOP status if a clock is not input after setting the RUN/STOP control register (PTRUN0).

(3) Since the TOUT signal is generated asynchronously from the PTOUT register, a hazard within 1/2 cycle is generated when the signal is turned ON and OFF by setting the register.

(4) When the OSC3 oscillation clock is selected for the clock source, it is necessary to turn the OSC3 oscillation ON, prior to using the programmable timer. However the OSC3 oscillation circuit requires a time interval of several msec to several 10 msec from turning the circuit ON until the oscillation stabilizes. Therefore, allow an adequate time interval from turning the OSC3 oscillation circuit ON to starting the programmable timer. Refer to Section 4.4, "Oscillation Circuit", for the control and notes of the OSC3 oscillation circuit. At initial reset, the OSC3 oscillation circuit is set in the OFF state.

Serial interface

(1) Perform data writing/reading to the data registers SD0–SD7 only while the serial interface is halted (i.e., the synchronous clock is neither being input or output).

(2) As a trigger condition, it is required that data writing or reading on data registers SD0–SD7 be performed prior to writing "1" to SCTRG. (The internal circuit of the serial interface is initiated through data writing/reading on data registers SD0–SD7.) In addition, be sure to enable the serial interface with the ESIF register before the trigger.
Supply trigger only once every time the serial interface is placed in the RUN state. Refrain from performing trigger input multiple times, as leads to malfunctioning. Moreover, when the synchronous clock $\overline{\text{SCLK}}$ is external clock, start to input the external clock after the trigger.

(3) Setting of the input/output permutation (MSB first/LSB first) with the SDP register should be done before setting data to SD0–SD7.

Buzzer output circuit

Since it generates a buzzer signal that is out of synchronization with the BZON register, hazards may at times be produced when the signal goes ON/OFF due to the setting of the BZON register.

SVD circuit

(1) To obtain a stable detection result, the SVD circuit must be ON for at least l00 μsec. So, to obtain the SVD detection result, follow the programming sequence below.

1. Set SVDON to "1"
2. Maintain for 100 μsec minimum
3. Set SVDON to "0"
4. Read SVDDT

(2) The SVD circuit should normally be turned OFF because SVD operation increase current consumption.

Interrupt

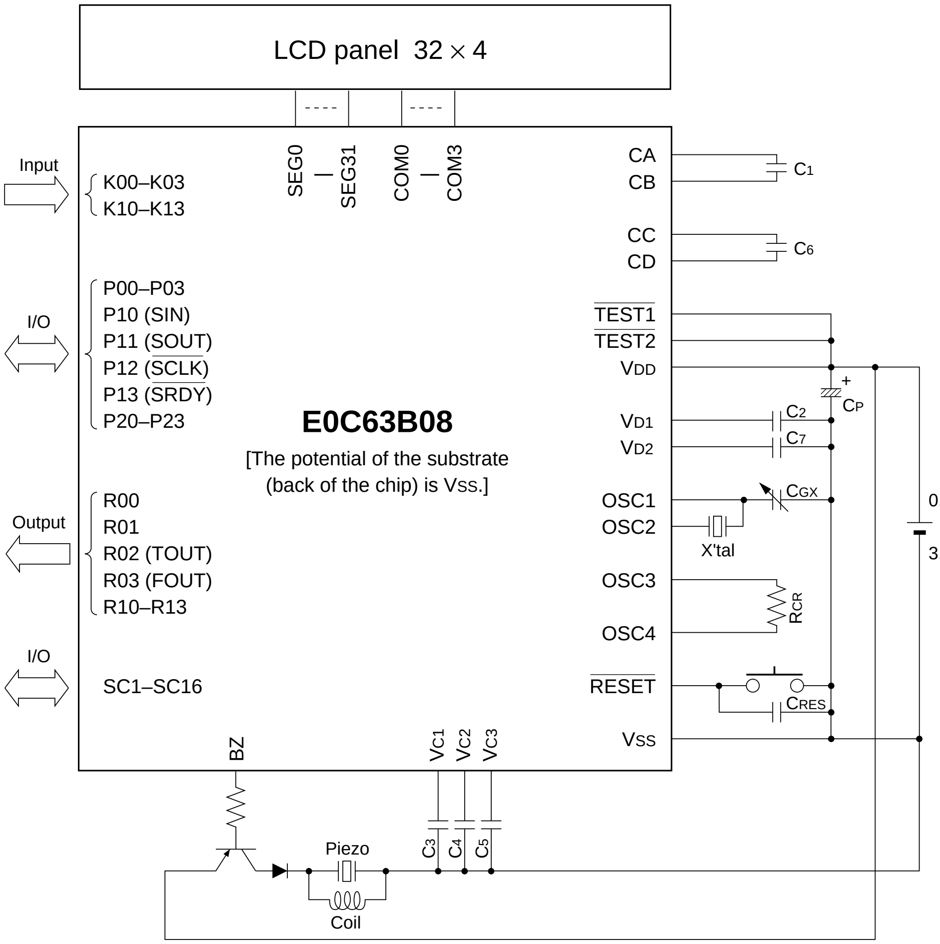
(1) The interrupt factor flags are set when the interrupt condition is established, even if the interrupt mask registers are set to "0".

(2) After an interrupt occurs, the same interrupt will occur again if the interrupt enabled state (I flag = "1") is set or the RETI instruction is executed unless the interrupt factor flag is reset. Therefore, be sure to reset (write "1" to) the interrupt factor flag in the interrupt service routine before shifting to the interrupt enabled state.

(3) After an initial reset, all the interrupts including NMI are masked until both the stack pointers SP1 and SP2 are set with the software. Be sure to set the SP1 and SP2 in the initialize routine.
Further, when re-setting the stack pointer, the SP1 and SP2 must be set as a pair. When one of them is set, all the interrupts including NMI are masked and interrupts cannot be accepted until the other one is set.

CHAPTER 6 BASIC EXTERNAL WIRING DIAGRAM

• When negative polarity is selected for buzzer output (mask option selection)



X'tal	Crystal oscillator	32.768 kHz/76.8 kHz/153.6 kHz, C_I (Max.) = 34 kΩ
C_{GX}	Trimmer capacitor	5–25 pF
R_{CR}	Resistor for CR oscillation	120 kΩ (Max. 400 kHz)
C_1–C_5	Capacitor	0.2 µF
C_6, C_7	Capacitor	0.4 µF
C_P	Capacitor	3.3 µF

Note: The above table is simply an example, and is not guaranteed to work.

Note:

- *In order to prevent unstable operation of the OSC1 oscillation circuit due to current leak between OSC1 and V_{DD}, please keep enough distance between V_{DD} and other signals on the board pattern.*
- *When using the OSC3 oscillation circuit for high speed operation (more than 300 kHz), it is better to double up the capacitors (0.8 µF) for C_6 and C_7.*
- *Precautions for Visible Radiation*

  Visible radiation causes semiconductor devices to change the electrical characteristics. It may cause this IC to malfunction. When developing products which use this IC, consider the following precautions to prevent malfunctions caused by visible radiations.

  (1) Design the product and implement the IC on the board so that it is shielded from visible radiation in actual use.

  (2) The inspection process of the product needs an environment that shields the IC from visible radiation.

  (3) As well as the face of the IC, shield the back and side too.

CHAPTER 7 ELECTRICAL CHARACTERISTICS

7.1 Absolute Maximum Rating

(V_{SS}=0V)

Item	Symbol	Rated value	Unit
Supply voltage	V_{DD}	-0.5 to 7.0	V
Input voltage (1)	V_I	-0.5 to V_{DD} + 0.3	V
Input voltage (2)	V_{IOSC}	-0.5 to V_{D1} + 0.3	V
Permissible total output current ∗1	ΣI_{VDD}	10	mA
Operating temperature	Topr	-20 to 70	°C
Storage temperature	Tstg	-65 to 150	°C
Soldering temperature / time	Tsol	260°C, 10sec (lead section)	–
Permissible dissipation ∗2	P_D	250	mW

∗1 The permissible total output current is the sum total of the current (average current) that simultaneously flows from the output pin (or is drawn in).

∗2 In case of plastic package (QFP15-100pin).

7.2 Recommended Operating Conditions

(Ta=-20 to 70°C)

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Supply voltage	V_{DD}	V_{SS}=0V	Doubler mode (OSC3 OFF)	0.9	1.1	1.25	V
			Doubler mode (OSC3 ON)	0.9	1.1	2.2	V
			Normal mode (OSC3 OFF)	1.25	3.0	3.6	V
			Normal mode (OSC3 ON)	2.2	3.0	3.6	V
			Halver mode (OSC3 OFF)	2.5	3.0	3.6	V
Oscillation frequency	f_{OSC1}	Any one is selected		–	32.768	–	kHz
				–	76.8	–	kHz
				–	153.6	–	kHz
	f_{OSC3}	Duty 50±5%, VDC="1"		50		400	kHz

7.3 DC Characteristics

Unless otherwise specified:
V_{DD}=1.5V, V_{SS}=0V, f_{OSC1}=32.768kHz, Ta=25°C, $V_{D1}/V_{C1}/V_{C2}/V_{C3}$ are internal voltage, C_1–C_5=0.2µF, C_6–C_7=0.4µF

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
High level input voltage (1)	V_{IH1}		K00–03, K10–13 P00–03, P10–13, P20–23	0.8·V_{DD}		V_{DD}	V
High level input voltage (2)	V_{IH2}		$\overline{RESET}$, $\overline{TEST1}$, $\overline{TEST2}$	0.9·V_{DD}		V_{DD}	V
Low level input voltage (1)	V_{IL1}		K00–03, K10–13 P00–03, P10–13, P20–23	0		0.2·V_{DD}	V
Low level input voltage (2)	V_{IL2}		$\overline{RESET}$, $\overline{TEST1}$, $\overline{TEST2}$	0		0.1·V_{DD}	V
High level input current	I_{IH}	V_{IH}=1.5V	K00–03, K10–13 P00–03, P10–13, P20–23 $\overline{RESET}$, $\overline{TEST1}$, $\overline{TEST2}$	0		0.5	µA
Low level input current (1)	I_{IL1}	V_{IL1}=V_{SS} No Pull-up	K00–03, K10–13 P00–03, P10–13, P20–23 $\overline{RESET}$, $\overline{TEST1}$, $\overline{TEST2}$	-0.5		0	µA
Low level input current (2)	I_{IL2}	V_{IL2}=V_{SS} With Pull-up	K00–03, K10–13 P00–03, P10–13, P20–23 $\overline{RESET}$, $\overline{TEST1}$, $\overline{TEST2}$	-8	-5	-3	µA
High level output current (1)	I_{OH1}	V_{OH1}=0.9·V_{DD}	R00–03, R10–13 P00–03, P10–13, P20–23			-0.3	mA
High level output current (2)	I_{OH2}	V_{OH2}=0.9·V_{DD}	BZ			-0.3	mA
Low level output current (1)	I_{OL1}	V_{OL1}=0.1·V_{DD}	R00–03, R10–13 P00–03, P10–13, P20–23	0.7			mA
Low level output current (2)	I_{OL2}	V_{OL2}=0.1·V_{DD}	BZ	0.7			mA
Common output current	I_{OH3}	V_{OH3}=V_{C3}-0.05V	COM0–3			-10	µA
	I_{OL3}	V_{OL3}=V_{SS}+0.05V		10			µA
Segment output current (during LCD output)	I_{OH4}	V_{OH4}=V_{C3}-0.05V	SEG0–31			-10	µA
	I_{OL4}	V_{OL4}=V_{SS}+0.05V		10			µA
Segment output current (during DC output)	I_{OH5}	V_{OH5}=0.9·V_{DD}	SEG0–31			-100	µA
	I_{OL5}	V_{OL5}=0.1·V_{DD}		100			µA

Unless otherwise specified:
V_{DD}=3.0V, V_{SS}=0V, f_{OSC1}=32.768kHz, Ta=25°C, $V_{D1}/V_{C1}/V_{C2}/V_{C3}$ are internal voltage, C_1–C_5=0.2µF, C_6–C_7=0.4µF

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
High level input voltage (1)	V_{IH1}		K00–03, K10–13 P00–03, P10–13, P20–23	0.8·V_{DD}		V_{DD}	V
High level input voltage (2)	V_{IH2}		$\overline{RESET}$, $\overline{TEST1}$, $\overline{TEST2}$	0.9·V_{DD}		V_{DD}	V
Low level input voltage (1)	V_{IL1}		K00–03, K10–13 P00–03, P10–13, P20–23	0		0.2·V_{DD}	V
Low level input voltage (2)	V_{IL2}		$\overline{RESET}$, $\overline{TEST1}$, $\overline{TEST2}$	0		0.1·V_{DD}	V
High level input current	I_{IH}	V_{IH}=3.0V	K00–03, K10–13 P00–03, P10–13, P20–23 $\overline{RESET}$, $\overline{TEST1}$, $\overline{TEST2}$	0		0.5	µA
Low level input current (1)	I_{IL1}	V_{IL1}=V_{SS} No Pull-up	K00–03, K10–13 P00–03, P10–13, P20–23 $\overline{RESET}$, $\overline{TEST1}$, $\overline{TEST2}$	-0.5		0	µA
Low level input current (2)	I_{IL2}	V_{IL2}=V_{SS} With Pull-up	K00–03, K10–13 P00–03, P10–13, P20–23 $\overline{RESET}$, $\overline{TEST1}$, $\overline{TEST2}$	-16	-5	-6	µA
High level output current (1)	I_{OH1}	V_{OH1}=0.9·V_{DD}	R00–03, R10–13 P00–03, P10–13, P20–23			-1.5	mA
High level output current (2)	I_{OH2}	V_{OH2}=0.9·V_{DD}	BZ			-1.5	mA
Low level output current (1)	I_{OL1}	V_{OL1}=0.1·V_{DD}	R00–03, R10–13 P00–03, P10–13, P20–23	6			mA
Low level output current (2)	I_{OL2}	V_{OL2}=0.1·V_{DD}	BZ	6			mA
Common output current	I_{OH3}	V_{OH3}=V_{C3}-0.05V	COM0–3			-10	µA
	I_{OL3}	V_{OL3}=V_{SS}+0.05V		10			µA
Segment output current (during LCD output)	I_{OH4}	V_{OH4}=V_{C3}-0.05V	SEG0–31			-10	µA
	I_{OL4}	V_{OL4}=V_{SS}+0.05V		10			µA
Segment output current (during DC output)	I_{OH5}	V_{OH5}=0.9·V_{DD}	SEG0–31			-300	µA
	I_{OL5}	V_{OL5}=0.1·V_{DD}		300			µA

7.4 Analog Circuit Characteristics and Power Current Consumption

Unless otherwise specified:

V_{DD}=3.0V, V_{SS}=0V, f_{OSC1}=32.768kHz, C_G=25pF, Ta=25°C, V_{D1}/V_{C1}/V_{C2}/V_{C3} are internal voltage, C_1–C_5=0.2µF,

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
LCD drive voltage	V_{C1}	Connect 1 MΩ load resistor between V_{SS} and V_{C1} (without panel load)		0.95	1.05	1.15	V
	V_{C2}	Connect 1 MΩ load resistor between V_{SS} and V_{C2} (without panel load)		2·V_{C1} ×0.9		2·V_{C1} +0.1	V
	V_{C3}	Connect 1 MΩ load resistor between V_{SS} and V_{C3} (without panel load)		3·V_{C1} ×0.9		3·V_{C1} +0.1	V
SVD voltage	V_{SVD}	SVDS0–3="0"		0.95	1.05	1.15	V
		SVDS0–3="1"		1.05	1.10	1.15	
		SVDS0–3="2"		1.10	1.15	1.20	
		SVDS0–3="3"		1.15	1.20	1.25	
		SVDS0–3="4"		1.20	1.25	1.30	
		SVDS0–3="5"		1.25	1.30	1.35	
		SVDS0–3="6"		1.35	1.40	1.45	
		SVDS0–3="7"		1.55	1.60	1.65	
		SVDS0–3="8"		1.90	1.95	2.00	
		SVDS0–3="9"		1.95	2.00	2.05	
		SVDS0–3="10"		2.00	2.05	2.10	
		SVDS0–3="11"		2.05	2.10	2.15	
		SVDS0–3="12"		2.15	2.20	2.25	
		SVDS0–3="13"		2.25	2.30	2.35	
		SVDS0–3="14"		2.45	2.50	2.55	
		SVDS0–3="15"		2.55	2.60	2.65	
SVD circuit response time	t_{SVD}					100	µS
Current consumption	I_{OP}	During HALT Normal mode LCD power OFF	32.768kHz		1.22	1.54	µA
			76.8kHz		1.76	2.13	µA
			153.6kHz		3.48	4.36	µA
		During HALT Normal mode *1 LCD power ON	32.768kHz		1.88	2.19	µA
			76.8kHz		2.42	2.75	µA
			153.6kHz		4.13	5.00	µA
		During HALT Doubler mode (V_{DD}=1.2V) ∗1 LCD power ON	32.768kHz		4.06	4.75	µA
			76.8kHz		5.33	6.08	µA
			153.6kHz		8.88	10.55	µA
		During HALT Halver mode (V_{DD}=3.0V) ∗1 LCD power ON	32.768kHz		1.31	1.50	µA
			76.8kHz		1.70	1.87	µA
			153.6kHz		2.50	2.83	µA
		During execution Normal mode *1 LCD power ON	32.768kHz		5.33	5.83	µA
			76.8kHz		10.75	11.09	µA
			153.6kHz		20.83	22.30	µA
			400kHz (CR oscillation)		87.50	90.00	µA
		During execution Doubler mode (V_{DD}=1.2V) ∗1 LCD power ON	32.768kHz		11.17	12.33	µA
			76.8kHz		20.90	21.00	µA
			153.6kHz		41.70	45.00	µA
			400kHz (CR oscillation)		175.0	177.5	µA
		During execution Halver mode (V_{DD}=3.0V) ∗1 LCD power ON	32.768kHz		3.17	3.33	µA
			76.8kHz		6.00	6.15	µA
			153.6kHz		11.1	11.7	µA

∗1 Without panel load. The SVD circuit is OFF.

7.5 Oscillation Characteristics

The oscillation characteristics change depending on the conditions (components used, board pattern, etc.). Use the following characteristics as reference values.

OSC1 crystal oscillation circuit

Unless otherwise specified:
VDD=3.0V, VSS=0V, fOSC1=32.768kHz, CG=25pF, CD=built-in, Ta=25°C

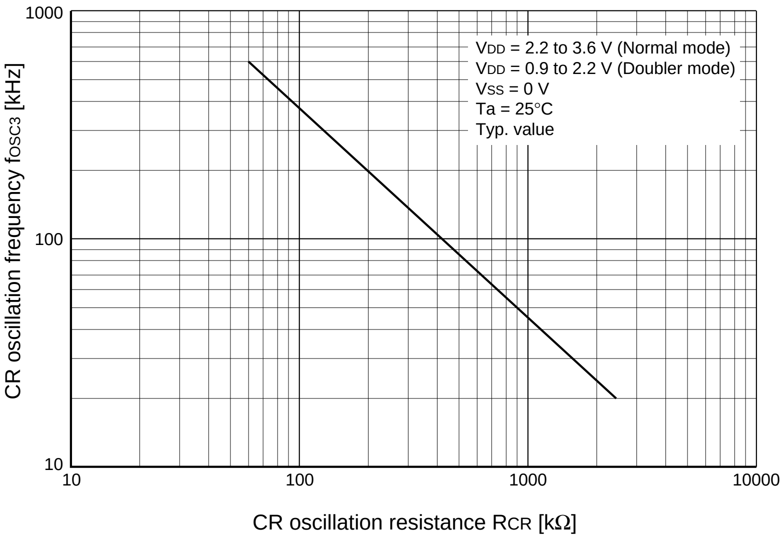
Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Oscillation start voltage	Vsta	tsta≤3sec (VDD)		1.1			V
Oscillation stop voltage	Vstp	tstp≤10sec (VDD)	Normal mode	1.1			V
			Doubler mode	0.9			V
Built-in capacitance (drain)	CD	Including the parasitic capacitance inside the IC (in chip)			14		pF
Frequency/voltage deviation	∂f/∂V	VDD=0.9 to 3.6V	with VDC switching			10	ppm
			without VDC switching			5	ppm
Frequency/IC deviation	∂f/∂IC			-10		10	ppm
Frequency adjustment range	∂f/∂CG	CG=5 to 25pF	32.768kHz	30	40		ppm
			76.8kHz	20	25		ppm
			153.6kHz	8	10		ppm
Harmonic oscillation start voltage	Vhho	CG=5pF (VDD)		3.6			V
Permitted leak resistance	Rleak	Between OSC1 and VDD, VSS		200			MΩ

OSC3 CR oscillation circuit

Unless otherwise specified:
VDD=3.0V, VSS=0V, RCR=120kΩ, Ta=25°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation frequency dispersion	fOSC3		-30	310kHz	30	%
Oscillation start voltage	Vsta	Normal mode (VDD)	2.2			V
		Doubler mode (VDD)	0.9			V
Oscillation start time	tsta	VDD=2.2 to 3.6V (Doubler mode: VDD=0.9 to 2.2V)			3	mS
Oscillation stop voltage	Vstp	Normal mode (VDD)	2.2			V
		Doubler mode (VDD)	0.9			V

CR oscillation frequency-resistance characteristic



7.6 Serial Interface AC Characteristics

Clock synchronous master mode

- ***During 32 kHz operation***

Condition: V_{DD}=1.5V, V_{SS}=0V, Ta=25°C, V_{IH1}=0.8V_{DD}, V_{IL1}=0.2V_{DD}, V_{OH}=0.8V_{DD}, V_{OL}=0.2V_{DD}

Item	Symbol	Min.	Typ.	Max.	Unit
Transmitting data output delay time	tsmd			5	µS
Receiving data input set-up time	tsms	10			µS
Receiving data input hold time	tsmh	5			µS

- ***During 400 kHz operation***

Condition: V_{DD}=3.0V, V_{SS}=0V, Ta=25°C, V_{IH1}=0.8V_{DD}, V_{IL1}=0.2V_{DD}, V_{OH}=0.8V_{DD}, V_{OL}=0.2V_{DD}

Item	Symbol	Min.	Typ.	Max.	Unit
Transmitting data output delay time	tsmd			200	nS
Receiving data input set-up time	tsms	400			nS
Receiving data input hold time	tsmh	200			nS

Clock synchronous slave mode

- ***During 32 kHz operation***

Condition: V_{DD}=1.5V, V_{SS}=0V, Ta=25°C, V_{IH1}=0.8V_{DD}, V_{IL1}=0.2V_{DD}, V_{OH}=0.8V_{DD}, V_{OL}=0.2V_{DD}

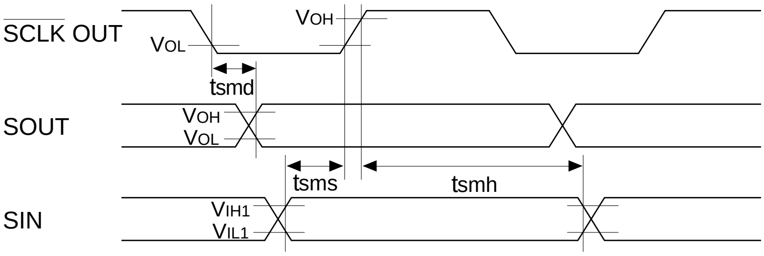
Item	Symbol	Min.	Typ.	Max.	Unit
Transmitting data output delay time	tssd			10	µS
Receiving data input set-up time	tsss	10			µS
Receiving data input hold time	tssh	5			µS

- ***During 400 kHz operation***

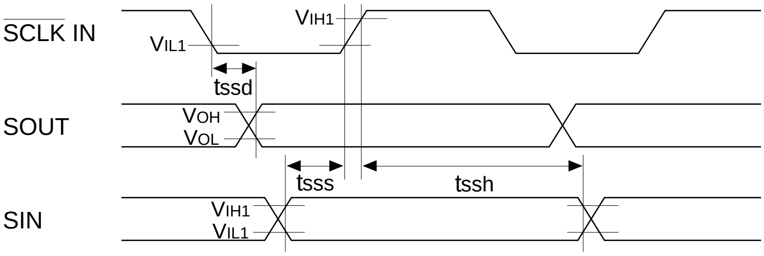
Condition: V_{DD}=3.0V, V_{SS}=0V, Ta=25°C, V_{IH1}=0.8V_{DD}, V_{IL1}=0.2V_{DD}, V_{OH}=0.8V_{DD}, V_{OL}=0.2V_{DD}

Item	Symbol	Min.	Typ.	Max.	Unit
Transmitting data output delay time	tssd			500	nS
Receiving data input set-up time	tsss	400			nS
Receiving data input hold time	tssh	200			nS

<Master mode>

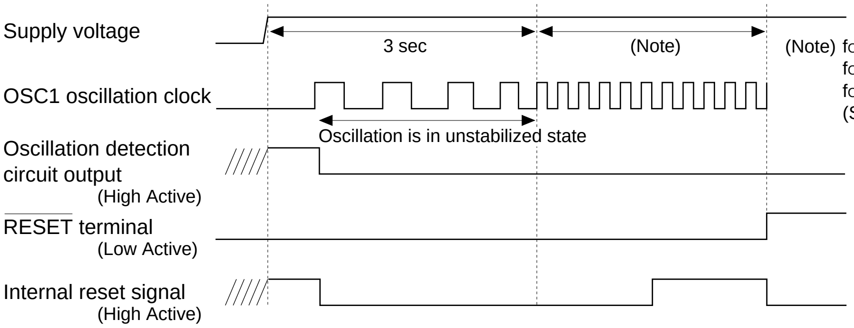


<Slave mode>



7.7 Timing Chart

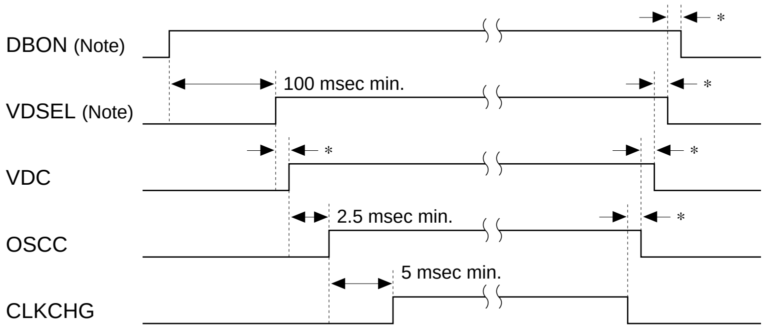
Initial reset



(Note) fOSC1=32.768 kHz : 6 msec min.
fOSC1=76.8 kHz : 3 msec min.
fOSC1=153.6 kHz : 1.5 msec min.
(See Section 2.2.1)

System clock switching

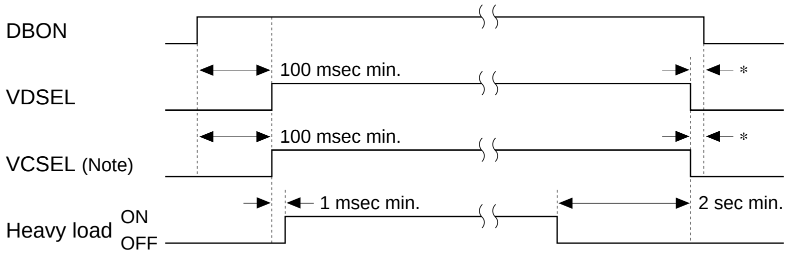
* 1 instruction execution time or longer



(Note) Use DBON and VDSEL only when changes are requied.

Supply voltage doubler control during heavy load driving

* 1 instruction execution time or longer



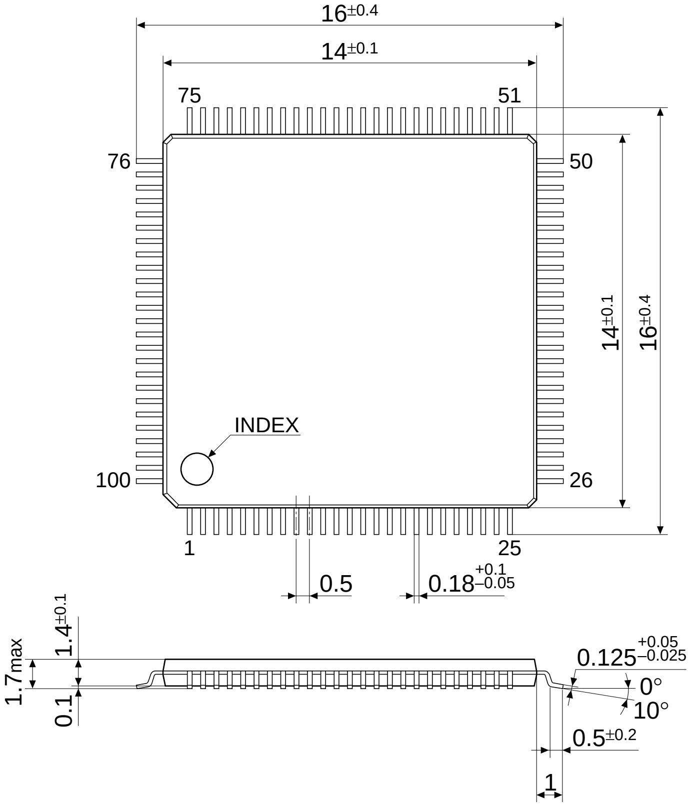
(Note) VCSEL is used only when it is required.

CHAPTER 8 PACKAGE

8.1 Plastic Package

QFP15-100pin

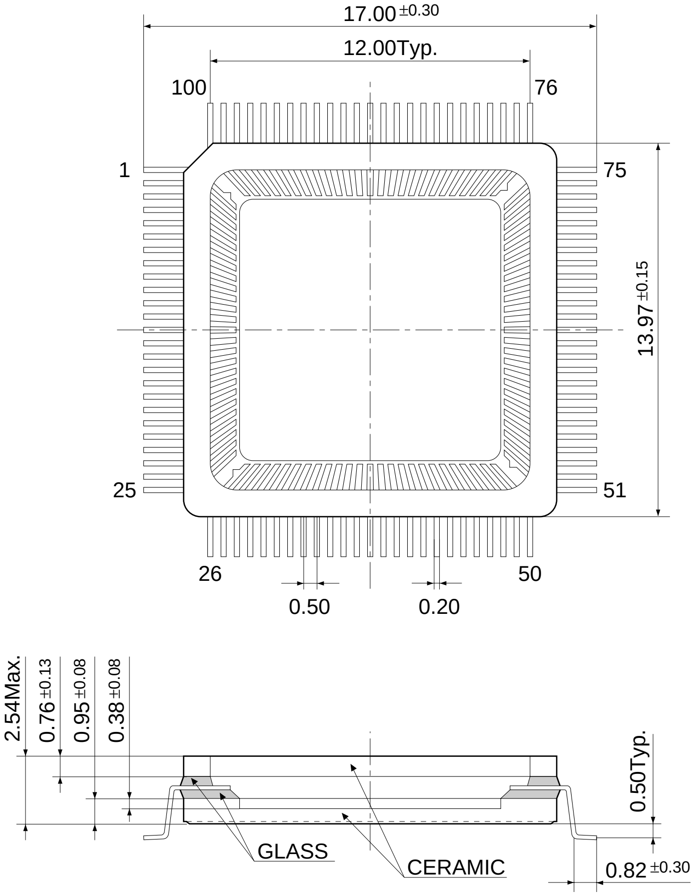
(Unit: mm)



The dimensions are subject to change without notice.

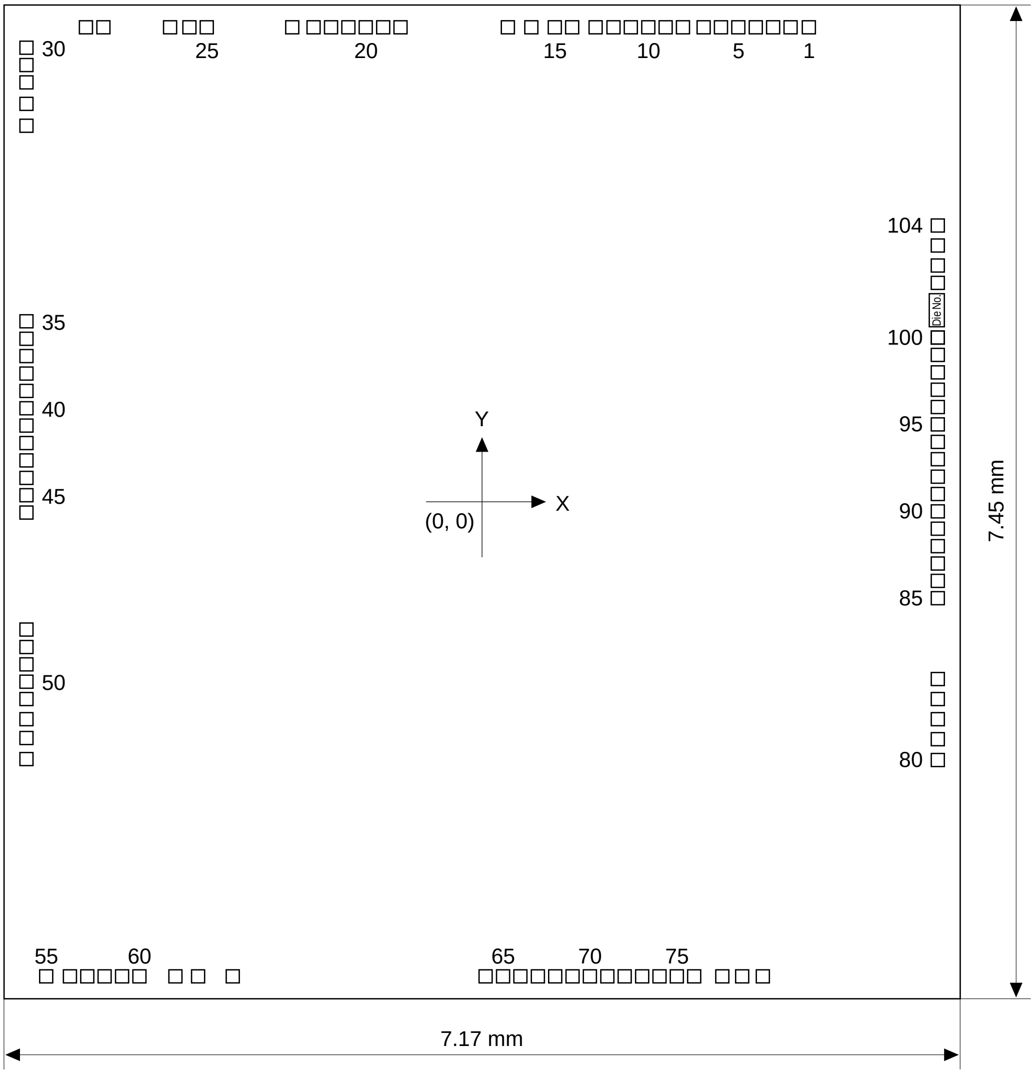
8.2 Ceramic Package for Test Samples

(Unit: mm)



CHAPTER 9 PAD LAYOUT

9.1 Diagram of Pad Layout



Chip thickness: 400 μm
Pad opening: 98 μm

9.2 Pad Coordinates

Unit: mm

No.	Pad name	X	Y	No.	Pad name	X	Y	No.	Pad name	X	Y
1	SEG25	2.450	3.558	36	P22	-3.417	1.223	71	SC8	0.939	-3.557
2	SEG26	2.313	3.558	37	P21	-3.417	1.093	72	SC9	1.069	-3.557
3	SEG27	2.182	3.558	38	P20	-3.417	0.962	73	SC10	1.200	-3.557
4	SEG28	2.052	3.558	39	P13	-3.417	0.832	74	SC11	1.330	-3.557
5	SEG29	1.921	3.558	40	P12	-3.417	0.702	75	SC12	1.460	-3.557
6	SEG30	1.791	3.558	41	P11	-3.417	0.572	76	SC13	1.590	-3.557
7	SEG31	1.661	3.558	42	P10	-3.417	0.441	77	SC14	1.801	-3.557
8	COM0	1.506	3.558	43	P03	-3.417	0.311	78	SC15	1.950	-3.557
9	COM1	1.376	3.558	44	P02	-3.417	0.180	79	SC16	2.105	-3.557
10	COM2	1.246	3.558	45	P01	-3.417	0.050	80	SEG0	3.417	-1.935
11	COM3	1.115	3.558	46	P00	-3.417	-0.080	81	SEG1	3.417	-1.779
12	CD	0.985	3.558	47	R13	-3.417	-0.957	82	SEG2	3.417	-1.629
13	N.C.	0.851	3.558	48	R12	-3.417	-1.088	83	SEG3	3.417	-1.478
14	N.C.	0.675	3.558	49	R11	-3.417	-1.218	84	SEG4	3.417	-1.328
15	N.C.	0.545	3.558	50	R10	-3.417	-1.348	85	SEG5	3.417	-0.722
16	N.C.	0.369	3.558	51	R03	-3.417	-1.478	86	SEG6	3.417	-0.592
17	N.C.	0.193	3.558	52	R02	-3.417	-1.629	87	SEG7	3.417	-0.462
18	CC	-0.612	3.558	53	R01	-3.417	-1.770	88	SEG8	3.417	-0.332
19	VC3	-0.742	3.558	54	R00	-3.417	-1.928	89	SEG9	3.417	-0.201
20	VC2	-0.873	3.558	55	BZ	-3.269	-3.557	90	SEG10	3.417	-0.071
21	VC1	-1.003	3.558	56	K00	-3.091	-3.557	91	SEG11	3.417	0.059
22	VD2	-1.133	3.558	57	K01	-2.961	-3.557	92	SEG12	3.417	0.189
23	VSS	-1.264	3.558	58	K02	-2.831	-3.557	93	SEG13	3.417	0.320
24	OSC1	-1.424	3.558	59	K03	-2.700	-3.557	94	SEG14	3.417	0.450
25	OSC2	-2.065	3.558	60	K10	-2.570	-3.557	95	SEG15	3.417	0.581
26	VD1	-2.195	3.558	61	K11	-2.300	-3.557	96	SEG16	3.417	0.711
27	OSC3	-2.340	3.558	62	K12	-2.130	-3.557	97	SEG17	3.417	0.841
28	OSC4	-2.840	3.558	63	K13	-1.870	-3.557	98	SEG18	3.417	0.971
29	VDD	-2.971	3.558	64	SC1	0.026	-3.557	99	SEG19	3.417	1.102
30	CB	-3.417	3.405	65	SC2	0.157	-3.557	100	SEG20	3.417	1.232
31	CA	-3.417	3.275	66	SC3	0.287	-3.557	101	SEG21	3.417	1.642
32	$\overline{\text{RESET}}$	-3.417	3.145	67	SC4	0.418	-3.557	102	SEG22	3.417	1.772
33	$\overline{\text{TEST2}}$	-3.417	2.984	68	SC5	0.548	-3.557	103	SEG23	3.417	1.922
34	$\overline{\text{TEST1}}$	-3.417	2.820	69	SC6	0.678	-3.557	104	SEG24	3.417	2.072
35	P23	-3.417	1.354	70	SC7	0.808	-3.557				

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First issue DECEMBER 1995, Printed DECEMBER 1999 in Japan Ⓜ A