MF1299-01

EPSON

CMOS 4-BIT SINGLE CHIP MICROCOMPUTER

E0C63P366 TECHNICAL MANUAL

E0C63P366 Technical Hardware

ENERGY SAVING EPSON

SEIKO EPSON CORPORATION

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CONTENTS

CHAPTER 1 OUTLINE

The E0C63P366 is a microcomputer which has a high-performance 4-bit CPU E0C63000 as the core CPU, rewritable ROM (Flash), RAM, serial interface, watchdog timer, programmable timer, time base counter (1 system), SVD circuit, a segment type LCD driver (32 segments × 4 commons), A/D converter and a special input port that can implement key position discrimination function using with the A/D converter. The E0C63P366 has a built-in large capacity Flash ROM (16K × 13 bits) and RAM (2K × 4 bits) that are compatible with the E0C63358 and E0C63158, it can therefore be used as an MTP (Multi-Time Programming) for program development.

1.1 Features

OSC1 oscillation circuit	32.768 kHz (Typ.) crystal oscillation circuit	
OSC3 oscillation circuit	1.8 MHz (Typ.) CR or 4 MHz (Max.) ceramic oscillation circuit (*1)	
Instruction set	Basic instruction:	46 types (411 instructions with all)
	Addressing mode:	8 types
Instruction execution time	At 32.768 kHz operation:	Min. 61 µsec
	At 4 MHz operation:	Min. 0.5 µsec
ROM (Flash) capacity	Code ROM:	16,384 words × 13 bits
	Segment option ROM:	2,048 words × 4 bits
	Programming method:	Parallel or serial programming (exclusive ROM writer is used)
	Rewriting:	100 times
RAM capacity	Data memory:	2,048 words × 4 bits
	Display memory:	32 words × 4 bits
Input port	9 bits	8 bits (with pull-up resistors)
		1 bit (for key position sensing interrupt by A/D)
Output port	12 bits	(2 special outputs are available *2)
I/O port	20 bits	(4 serial inputs/outputs are available *2)
		(4 A/D inputs are available *2)
Serial interface	1 port	(8-bit clock synchronous system)
LCD driver	32 segments × 4, 3 or 2 commons (*2), 1/3 bias drive	
Time base counter	1 system (clock timer)	
Programmable timer	Built-in, 2 channels × 8 bits or 1 channel × 16 bits (*2), with event counter function	
Watchdog timer	Built-in	
A/D converter	8-bit resolution	
	Maximum error: ±3 LSB, A/D clock: OSC1, OSC3 (2.7 V to 5.5 V)	
Buzzer output	Buzzer frequency: 2 kHz or 4 kHz (*2), 2 Hz interval output (*2)	
Supply voltage detection (SVD) circuit	2 values, programmable (2.7 V, 2.8 V)	
External interrupt	Input port interrupt:	2 systems
	Key sensing interrupt:	1 system
Internal interrupt	Clock timer interrupt:	4 systems
	Programmable timer interrupt:	2 systems
	Serial interface interrupt:	1 system
	A/D converter:	1 system
Power supply voltage	2.7 V to 5.5 V	
Operating temperature range	-20°C to 70°C	

Current consumption (Typ.) ..... Single clock:

During HALT (32 kHz)	3.0 V (LCD power OFF)	2.5 µA
	3.0 V (LCD power ON)	37 µA
During operation (32 kHz)	3.0 V (LCD power ON)	120 µA
Twin clock:		
During operation (4 MHz)	3.0 V (LCD power ON)	800 µA

Package ..... QFP15-100pin (plastic) or chip

*1: Can be selected with mask option *2: Can be selected with software

1.2 Block Diagram

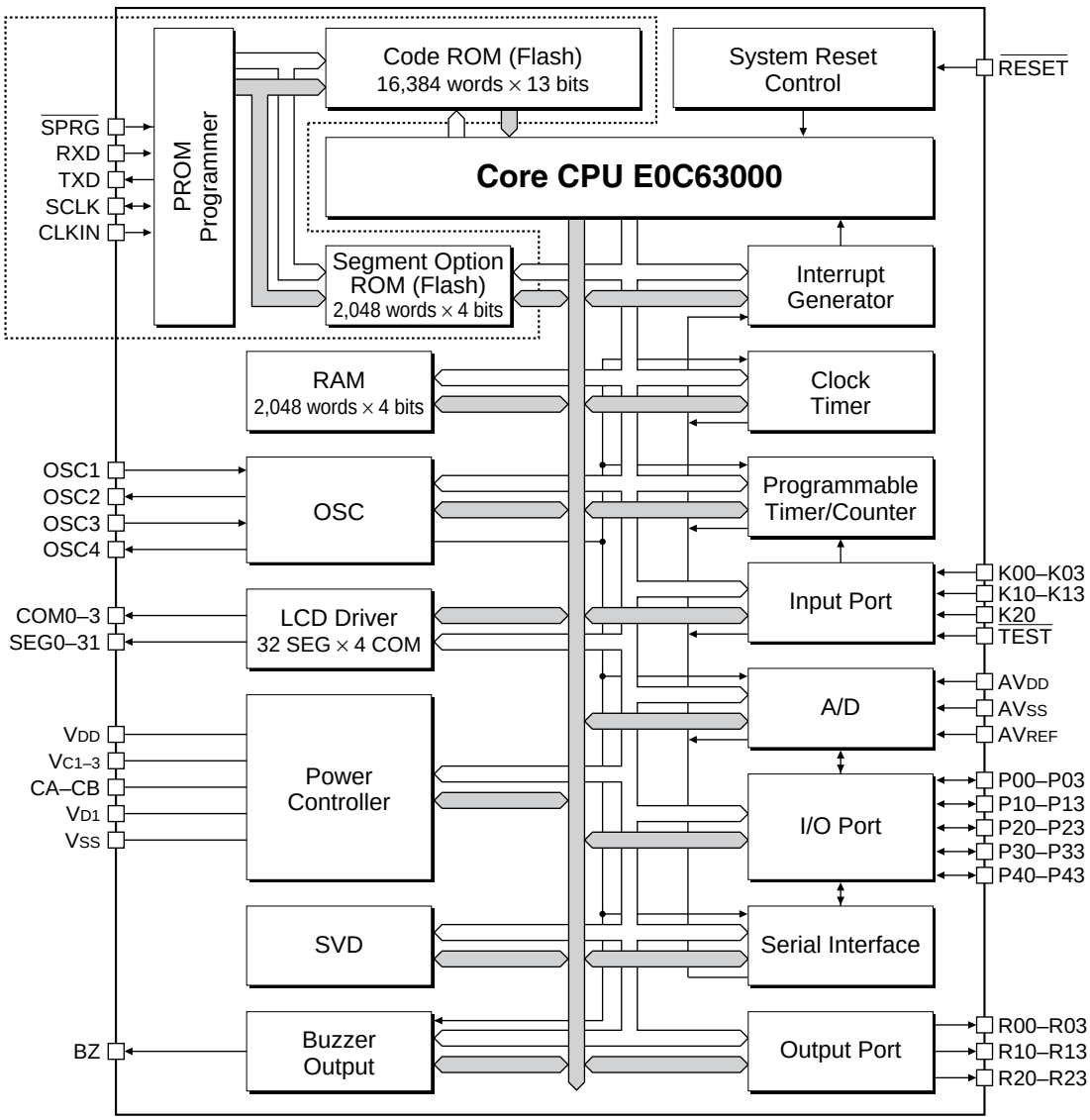
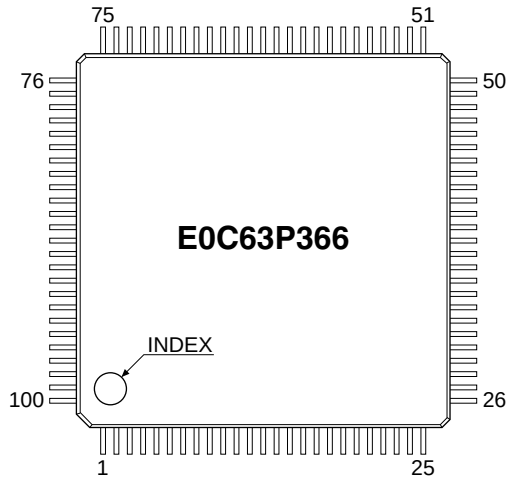


Fig. 1.2.1 Block diagram

1.3 Pin Layout Diagram

QFP15-100pin



No.	Pin name		No.	Pin name		No.	Pin name		No.	Pin name	
	E0C63P366	E0C63358		E0C63P366	E0C63358		E0C63P366	E0C63358		E0C63P366	E0C63358
1	SEG7	SEG7	26	CLKIN	N.C.	51	SCLK	N.C.	76	R13	R13
2	SEG8	SEG8	27	$\overline{SPRG}$	N.C.	52	P43	P43	77	R12	R12
3	SEG9	SEG9	28	COM0	COM0	53	P42	P42	78	R11	R11
4	SEG10	SEG10	29	COM1	COM1	54	P41	P41	79	R10	R10
5	SEG11	SEG11	30	COM2	COM2	55	P40	P40	80	R03	R03
6	SEG12	SEG12	31	COM3	COM3	56	P33	P33	81	R02	R02
7	SEG13	SEG13	32	CB	CB	57	P32	P32	82	R01	R01
8	SEG14	SEG14	33	CA	CA	58	P31	P31	83	R00	R00
9	SEG15	SEG15	34	V_{C3}	V_{C3}	59	P30	P30	84	BZ	BZ
10	SEG16	SEG16	35	V_{C2}	V_{C2}	60	P23	P23	85	K00	K00
11	SEG17	SEG17	36	V_{C1}	V_{C1}	61	P22	P22	86	K01	K01
12	SEG18	SEG18	37	V_{SS}	V_{SS}	62	P21	P21	87	K02	K02
13	SEG19	SEG19	38	OSC1	OSC1	63	P20	P20	88	K03	K03
14	SEG20	SEG20	39	OSC2	OSC2	64	P13	P13	89	K10	K10
15	SEG21	SEG21	40	V_{D1}	V_{D1}	65	P12	P12	90	K11	K11
16	SEG22	SEG22	41	OSC3	OSC3	66	P11	P11	91	K12	K12
17	SEG23	SEG23	42	OSC4	OSC4	67	P10	P10	92	K13	K13
18	SEG24	SEG24	43	V_{DD}	V_{DD}	68	P03	P03	93	K20	K20
19	SEG25	SEG25	44	$\overline{RESET}$	$\overline{RESET}$	69	P02	P02	94	SEG0	SEG0
20	SEG26	SEG26	45	$\overline{TEST}$	$\overline{TEST}$	70	P01	P01	95	SEG1	SEG1
21	SEG27	SEG27	46	AV_{REF}	AV_{REF}	71	P00	P00	96	SEG2	SEG2
22	SEG28	SEG28	47	AV_{DD}	AV_{DD}	72	R23	R23	97	SEG3	SEG3
23	SEG29	SEG29	48	AV_{SS}	AV_{SS}	73	R22	R22	98	SEG4	SEG4
24	SEG30	SEG30	49	RXD	N.C.	74	R21	R21	99	SEG5	SEG5
25	SEG31	SEG31	50	TXD	N.C.	75	R20	R20	100	SEG6	SEG6

N.C. : No Connection

Fig. 1.3.1 Pin layout diagram

1.4 Pin Description

Table 1.4.1 Pin description

Pin name	Pin No.	In/Out	Function
V_{DD}	43	–	Power (+) supply pin
V_{SS}	37	–	Power (–) supply pin
V_{D1}	40	–	Oscillation system regulated voltage output pin
V_{C1}–V_{C3}	36–34	–	LCD system power supply pin 1/3 bias
CA, CB	33, 32	–	LCD system boosting/reducing capacitor connecting pin
OSC1	38	I	Crystal oscillation input pin
OSC2	39	O	Crystal oscillation output pin
OSC3	41	I	Ceramic or CR oscillation input pin (selected by mask option)
OSC4	42	O	Ceramic or CR oscillation output pin (selected by mask option)
K00–K03	85–88	I	Input port
K10–K13	89–92	I	Input port
K20	93	I	Input port with control
P00–P03	71–68	I/O	I/O port
P10–P13	67–64	I/O	I/O port (switching to serial I/F input/output is possible by software)
P20–P23	63–60	I/O	I/O port
P30–P33	59–56	I/O	I/O port
P40–P43	55–52	I/O	I/O port (can be used as A/D input)
R00	83	O	Output port
R01	82	O	Output port
R02	81	O	Output port (switching to TOUT output is possible by software)
R03	80	O	Output port (switching to FOUT output is possible by software)
R10–R13	79–76	O	Output port
R20–R23	75–72	O	Output port
COM0–COM3	28–31	O	LCD common output pin (1/4, 1/3, 1/2 duty can be selected by software)
SEG0–SEG31	94–100, 1–25	O	LCD segment output pin
AV_{DD}	47	–	Power (+) supply pin for A/D converter
AV_{SS}	48	–	Power (–) supply pin for A/D converter
AV_{REF}	46	–	Reference voltage for A/D converter
BZ	84	O	Buzzer output pin
$\overline{\text{RESET}}$	44	I	Initial reset input pin
$\overline{\text{TEST}}$	45	I	Testing input pin
RXD *1	49	I	Serial data input pin for Flash programming
TXD *1	50	O	Serial data output pin for Flash programming
SCLK *1	51	I/O	Serial clock input/output pin for Flash programming
CLKIN *1	26	I	Clock input pin for Flash programming
$\overline{\text{SPRG}}$ *1	27	I	Control pin for Flash programming

*1 N.C. in E0C63358
Refer to Chapter 5, "PROM Programmer and Operating Mode", for the Flash programming pins.

1.5 Mask Option

Mask options shown below are provided for the E0C63P366.

<E0C63P366 mask options>

(1) OSC3 oscillation circuit

Either CR oscillation circuit or ceramic oscillation circuit can be selected as the OSC3 oscillation circuit.
Refer to Section 4.3.3, "OSC3 oscillation circuit", for details.

The other mask options provided for the E0C63358/63158 are fixed as follows in the E0C63P366, so they cannot be selected.

- OSC1 oscillation circuit ..... Crystal oscillation
- Multiple key input reset ..... Not used
- Time authorize for multiple key input ..... Not used
- Input port pull-up resistor ..... Available
- Output port output specifications ..... Complementary output
- I/O port output specifications ..... Complementary output
- I/O port pull-up resistor P1x, P2x, P3x ..... Available
  P4x ..... Not available
- LCD drive bias ..... 1/3 bias
- Serial interface input/output polarity ..... Negative polarity
- Buzzer output specification ..... Negative polarity

1.6 Segment Option

(1) LCD segment allocation

Up to 128 bits of the display memory can be selected from the data memory addresses F000H to F01FH. The LCD driver has a segment decoder built-in, and the data bit (D0–D3) of the optional address in the display memory area (F000H–F01FH) can be allocated to the optional segment. The segment option generator SOG63358, that has been prepared as a development software tool of the E0C63358, is used for this selection.
Refer to Section 4.7.4, "Segment option", for details.

(2) LCD segment output specification

It is possible to set the optional SEG terminal for DC output.
Refer to Section 4.7.4, "Segment option", for details.

(3) Segment option data

Recommended option data is written to the LCD segment opotion PROM before the IC is shipped. Modifying the LCD segment opotion is done at the user's own risk.

CHAPTER 2 POWER SUPPLY AND INITIAL RESET

2.1 Power Supply

The E0C63P366 operating power voltage is as follows:

2.7 V to 5.5 V

The E0C63P366 operates by applying a single power supply within the above range between VDD/AVDD and VSS/AVSS. The E0C63P366 itself generates the voltage necessary for all the internal circuits by the built-in power supply circuits shown in Table 2.1.1.

Table 2.1.1 Power supply circuits

Circuit	Power supply circuit	Output voltage
Oscillation circuit	Oscillation sysrem voltage regulator	VD1
Internal logic circuits	Supply voltage (VDD)	VDD
LCD driver	LCD system voltage circuit	VC1–VC3
Oscillation sysrem voltage regulator	Supply voltage (VDD)	VDD
LCD system voltage circuit	Supply voltage (VDD)	VDD
A/D converter	Analog supply voltage (AVDD) and supply voltage (VDD)	AVDD and VDD

Note: • Do not drive external loads with the output voltage from the internal power supply circuits.

• The internal LCD system voltage circuit (1/3 bias) is always used in the E0C63P366.

• See Chapter 9, "Electrical Characteristics", for voltage values and drive capability.

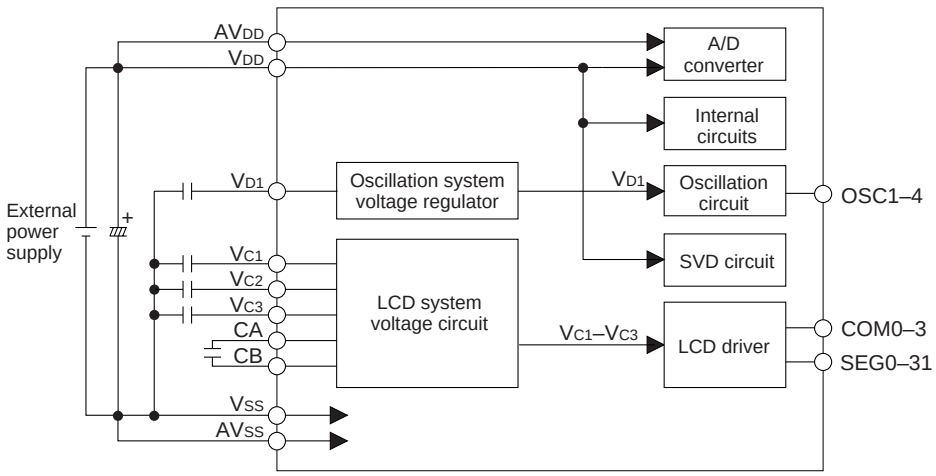


Fig. 2.1.1 Configuration of power supply

2.1.1 Voltage <V_{D1}> for oscillation circuit and internal circuits

V_{D1} is the operating voltage for the oscillation circuit, and is generated by the oscillation system voltage regulator for stabilizing oscillation.
In the E0C63358/63158, it is necessary to switch the V_{D1} voltage level according to the oscillation circuit and operating frequency by controlling the voltage regulator. In the E0C63P366, the V_{D1} voltage level is fixed, so software control for switching the V_{D1} level does not affect the actual output voltage. However, when using the E0C63P366 as a development tool for the E0C63358/63158, the V_{D1} software control sequence must be implemented according to the model.
Refer to Chapter 6, "Differences from Mask ROM Models", for details.

2.1.2 Voltage <V_{C1}–V_{C3}> for LCD driving

V_{C1} to V_{C3} are the voltages for LCD drive, and are generated by the LCD system voltage circuit to stabilize the display quality.
Since the minimum operating voltage of the E0C63P366 is 2.7 V, the LCD system voltage circuit generates V_{C2} as the reference voltage, and generates two other voltages by boosting or reducing V_{C2} (V_{C1} = 1/2•V_{C2}, V_{C3} = 3/2•V_{C2}).
Refer to Chapter 9, "Electrical Characteristics", for voltage values of V_{C1} to V_{C3}.

2.1.3 Operating mode of power supply circuit

The oscillation system voltage regulator and A/D converter power supply circuit operate in normal mode that uses V_{DD} as the power source.
In the E0C63358/63158, a booster mode (V_{C2} mode) is provided in order to guarantee low-voltage operation, therefore it is necessary to switch the operating mode. Since the power supply voltage of the E0C63P366 is 2.7 V or more, this switching is not necessary and the software control does not affect the operating mode. However, when using the E0C63P366 as a development tool for the E0C63358/63158, the operating mode control routine must be implemented according to the model.
Refer to Chapter 6, "Differences from Mask ROM Models", for details.

2.2 Initial Reset

To initialize the E0C63P366 circuits, initial reset must be executed. The E0C63P366 supports an external initial reset using the reset ($\overline{\text{RESET}}$) terminal.

When the power is turned on, be sure to initialize using this reset function. It is not guaranteed that the circuits are initialized by only turning the power on.

Figure 2.2.1 shows the configuration of the initial reset circuit.

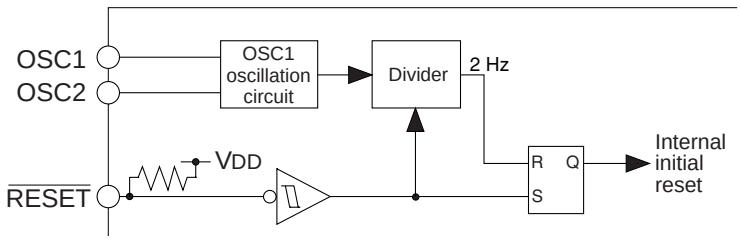


Fig. 2.2.1 Configuration of initial reset circuit

2.2.1 Reset terminal ($\overline{\text{RESET}}$)

Initial reset can be executed externally by setting the reset terminal to a low level (VSS). After that the initial reset is released by setting the reset terminal to a high level (VDD) and the CPU starts operation. The reset input signal is maintained by the RS latch and becomes the internal initial reset signal. The RS latch is designed to be released by a 2 Hz signal (high) that is divided by the OSC1 clock. Therefore in normal operation, a maximum of 250 msec (when fOSC1 = 32.768 kHz) is needed until the internal initial reset is released after the reset terminal goes to high level. Be sure to maintain a reset input of 0.1 msec or more.
However, when turning the power on, the reset terminal should be set at a low level as in the timing shown in Figure 2.2.1.1.

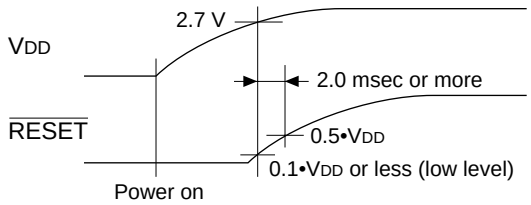


Fig. 2.2.1.1 Initial reset at power on

The reset terminal should be set to 0.1•VDD or less (low level) until the supply voltage becomes 2.7 V or more. After that, a level of 0.5•VDD or less should be maintained more than 2.0 msec.
In the E0C63P366, a low level input to the reset terminal initializes some analog circuits as well as the internal logic. At this time, 10 µA or more current is consumed as the bias current.

2.2.2 Internal register at initial resetting

Initial reset initializes the CPU as shown in Table 2.2.2.1.

The registers and flags which are not initialized by initial reset should be initialized in the program if necessary.
In particular, the stack pointers SP1 and SP2 must be set as a pair because all the interrupts including NMI are masked after initial reset until both the SP1 and SP2 stack pointers are set with software.

When data is written to the EXT register, the E flag is set and the following instruction will be executed in the extended addressing mode. If an instruction which does not permit extended operation is used as the following instruction, the operation is not guaranteed. Therefore, do not write data to the EXT register for initialization only.
Refer to the "E0C63000 Core CPU Manual" for extended addressing and usable instructions.

Table 2.2.2.1 Initial values

CPU core			
Name	Symbol	Number of bits	Setting value
Data register A	A	4	Undefined
Data register B	B	4	Undefined
Extension register EXT	EXT	8	Undefined
Index register X	X	16	Undefined
Index register Y	Y	16	Undefined
Program counter	PC	16	0110H
Stack pointer SP1	SP1	8	Undefined
Stack pointer SP2	SP2	8	Undefined
Zero flag	Z	1	Undefined
Carry flag	C	1	Undefined
Interrupt flag	I	1	0
Extension flag	E	1	0
Queue register	Q	16	Undefined

Peripheral circuits		
Name	Number of bits	Setting value
RAM	4	Undefined
Display memory	4	Undefined
Other pheripheral circuits	–	*

* See Section 4.1, "Memory Map".

2.2.3 Terminal settings at initial resetting

The output port (R) terminals and I/O port (P) terminals are shared with special output terminals, input/output terminals of the serial interface and input terminals of the A/D converter. These functions are selected by the software. At initial reset, these terminals are set to the general purpose output port terminals and I/O port terminals. Set them according to the system in the initial routine. In addition, take care of the initial status of output terminals when designing a system.
Table 2.2.3.1 shows the list of the shared terminal settings.

Table 2.2.3.1 List of shared terminal settings

Terminal name	Terminal status at initial reset	Special output		Serial I/F		A/D converter
		TOUT	FOUT	Master	Slave	
R00	R00 (High output)					
R01	R01 (High output)					
R02	R02 (High output)	TOUT				
R03	R03 (High output)		FOUT			
R10–R13	R10–R13 (High output)					
R20–R23	R20–R23 (High output)					
P00–P03	P00–P03 (Input & Pull-up)					
P10	P10 (Input & Pull-up)			SIN(I)	SIN(I)	
P11	P11 (Input & Pull-up)			SOUT(O)	SOUT(O)	
P12	P12 (Input & Pull-up)			$\overline{\text{SCLK}}$(O)	$\overline{\text{SCLK}}$(I)	
P13	P13 (Input & Pull-up)				$\overline{\text{SRDY}}$(O)	
P20–P23	P20–P23 (Input & Pull-up)					
P30–P33	P30–P33 (Input & Pull-up)					
P40	P40 (Input & high impedance)					AD0(I)
P41	P41 (Input & high impedance)					AD1(I)
P42	P42 (Input & high impedance)					AD2(I)
P43	P43 (Input & high impedance)					AD3(I)

For setting procedure of the functions, see explanations for each of the peripheral circuits.

2.3 Test Terminal ($\overline{TEST}$)

This is the terminal used for the factory inspection of the IC. During normal operation, connect the $\overline{TEST}$ terminal to VDD.

2.4 Terminals for Flash EEPROM

The E0C63P366 has the following terminals used for writing data to the Flash EEPROM and for factory testing.

$\overline{SPRG}$: Flash EEPROM programming control terminal
SCLK: Clock input/output terminal for Flash EEPROM serial programming
RXD: Data input terminal for Flash EEPROM serial programming
TXD: Data output terminal for Flash EEPROM serial programming
CLKIN: Flash EEPROM write-control clock input terminal

The above terminals should be set up according to the operating mode. Refer to Chapter 5, "PROM Programming and Operating Mode", for details.

CHAPTER 3 CPU, ROM, RAM

3.1 CPU

The E0C63P366 has a 4-bit core CPU E0C63000 built-in as its CPU part.
Refer to the "E0C63000 Core CPU Manual" for the E0C63000.

Note: The SLP instruction cannot be used because the SLEEP operation is not assumed in the E0C63P366.

3.2 Code ROM

The built-in code ROM is a Flash ROM for loading programs, and has a capacity of 16,384 steps × 13 bits. The core CPU can linearly access the program space up to step FFFFH from step 0000H, however, the program area of the E0C63P366 is step 0000H to step 3FFFH. The program start address after initial reset is assigned to step 0110H. The non-maskable interrupt (NMI) vector and hardware interrupt vectors are allocated to step 0100H and steps 0102H–010EH, respectively.

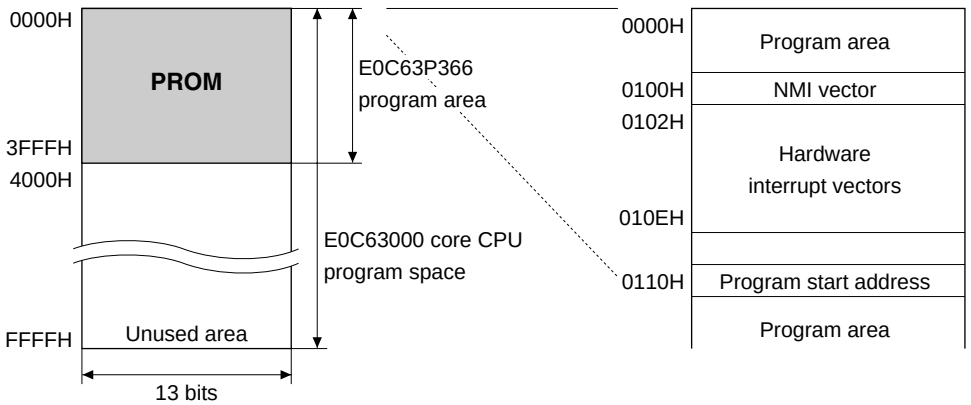


Fig. 3.2.1 Configuration of code ROM

3.3 RAM

The RAM is a data memory for storing various kinds of data, and has a capacity of 2,048 words × 4 bits. The RAM area is assigned to addresses 0000H to 07FFH on the data memory map. Addresses 0100H to 01FFH are 4-bit/16-bit data accessible areas and in other areas it is only possible to access 4-bit data. When programming, keep the following points in mind.

(1) Part of the RAM area is used as a stack area for subroutine call and register evacuation, so pay attention not to overlap the data area and stack area.

(2) The E0C63000 core CPU handles the stack using the stack pointer for 4-bit data (SP2) and the stack pointer for 16-bit data (SP1).
16-bit data are accessed in stack handling by SP1, therefore, this stack area should be allocated to the area where 4-bit/16-bit access is possible (0100H to 01FFH). The stack pointers SP1 and SP2 change cyclically within their respective range: the range of SP1 is 0000H to 03FFH and the range of SP2 is 0000H to 00FFH. Therefore, pay attention to the SP1 value because it may be set to 00FFH or less exceeding the 4-bit/16-bit accessible range in the E0C63P366. Memory accesses except for stack operations by SP1 are 4-bit data access.
After initial reset, all the interrupts including NMI are masked until both the stack pointers SP1 and SP2 are set by software. Further, if either SP1 or SP2 is re-set when both are set already, the interrupts including NMI are masked again until the other is re-set. Therefore, the settings of SP1 and SP2 must be done as a pair.

(3) Subroutine calls use 4 words (for PC evacuation) in the stack area for 16-bit data (SP1). Interrupts use 4 words (for PC evacuation) in the stack area for 16-bit data (SP1) and 1 word (for F register evacuation) in the stack area for 4-bit data.

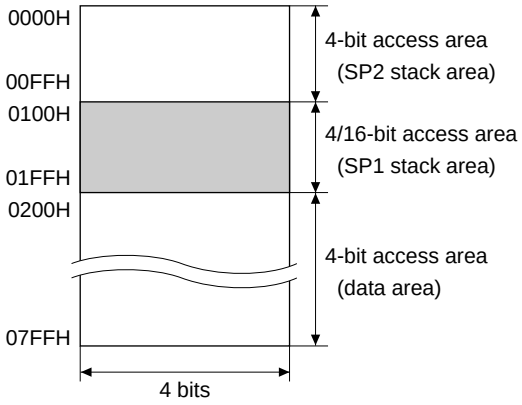


Fig. 3.3.1 Configuration of data RAM

CHAPTER 4 PERIPHERAL CIRCUITS AND OPERATION

The peripheral circuits of the E0C63P366 (timer, A/D, I/O, etc.) are interfaced with the CPU in the memory mapped I/O method. Thus, all the peripheral circuits can be controlled by accessing the I/O memory on the memory map using the memory operation instructions. The following sections explain the detailed operation of each peripheral circuit.

4.1 Memory Map

The E0C63P366 data memory consists of 2,048-word RAM, 32-word display memory and 76-word peripheral I/O memory area. Figure 4.1.1 shows the overall memory map of the E0C63P366, and Tables 4.1.1(a)–(f) the peripheral circuits' (I/O space) memory maps.

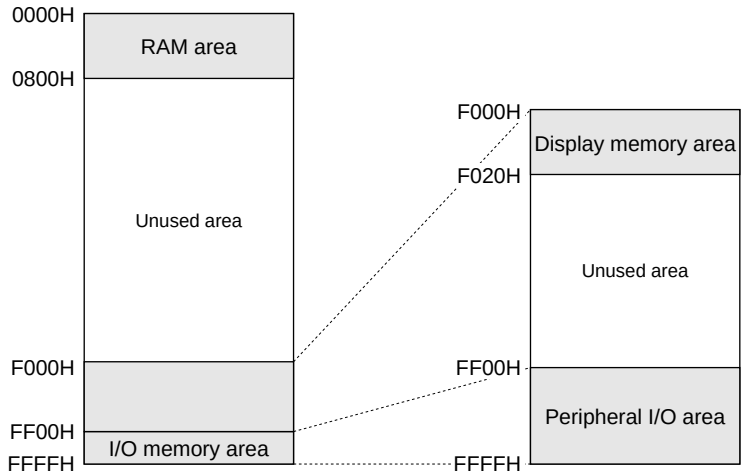


Fig. 4.1.1 Memory map

Note: Memory is not implemented in unused areas within the memory map. Further, some non-implementation areas and unused (access prohibition) areas exist in the peripheral I/O area. If the program that accesses these areas is generated, its operation cannot be guaranteed. Refer to the I/O memory maps shown in Tables 4.1.1 (a)–(f) for the peripheral I/O area.

Table 4.1.1 (a) I/O memory map (FF00H–FF28H)

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
FF00H	CLKCHG	OSCC	0	VDC	CLKCHG	0	OSC3	OSC1	CPU clock switch
					OSCC	0	On	Off	OSC3 oscillation On/Off
	R/W		R	R/W	0 *3	– *2			Unused
					VDC	0	(OSC3)	(OSC1)	(Operating voltage switch)
FF01H	VADSEL	VDSEL	0	DBON	VADSEL	0	(V_{C2})	(V_{DD})	(Power source selection for A/D converter)
					VDSEL	0	(V_{C2})	(V_{DD})	(Power source selection for oscillation system voltage regulator)
	R/W		R	R/W	0 *3	– *2			Unused
					DBON	0	(On)	(Off)	(Voltage doubler On/Off)
FF04H	SVDS3	SVDS2	SVDS1	SVDS0	SVDS3	0			SVD criteria voltage setting [SVDS3–0] 0 1 2 3 4 5 6 7 Voltage(V) – – – – – – – – [SVDS3–0] 8 9 10 11 12 13 14 15 Voltage(V) – – – – – – 2.70 2.80
	R/W				SVDS2	0			
					SVDS1	0			
					SVDS0	0			
FF05H	0	0	SVDDT	SVDON	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R			R/W	SVDDT	0	Low	Normal	SVD evaluation data
					SVDON	0	On	Off	SVD circuit On/Off
FF06H	FOUTE	0	FOFQ1	FOFQ0	FOUTE	0	Enable	Disable	FOUT output enable
					0 *3	– *2			Unused
	R/W	R	R/W		FOFQ1	0			FOUT frequency selection [FOFQ1, 0] 0 1 2 3 Frequency $f_{OSC1}/64$ $f_{OSC1}/8$ f_{OSC1} f_{OSC3}
					FOFQ0	0			
FF07H	0	0	WDEN	WDRST	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R		R/W	W	WDEN	1	Enable	Disable	Watchdog timer enable
					WDRST*3	Reset	Reset	Invalid	Watchdog timer reset (writing)
FF20H	SIK03	SIK02	SIK01	SIK00	SIK03	0	Enable	Disable	K00–K03 interrupt selection register
					SIK02	0	Enable	Disable	
	R/W				SIK01	0	Enable	Disable	
					SIK00	0	Enable	Disable	
FF21H	K03	K02	K01	K00	K03	– *2	High	Low	K00–K03 input port data
					K02	– *2	High	Low	
	R				K01	– *2	High	Low	
					K00	– *2	High	Low	
FF22H	KCP03	KCP02	KCP01	KCP00	KCP03	1	↓	↑	K00–K03 input comparison register
					KCP02	1	↓	↑	
	R/W				KCP01	1	↓	↑	
					KCP00	1	↓	↑	
FF24H	SIK13	SIK12	SIK11	SIK10	SIK13	0	Enable	Disable	K10–K13 interrupt selection register
					SIK12	0	Enable	Disable	
	R/W				SIK11	0	Enable	Disable	
					SIK10	0	Enable	Disable	
FF25H	K13	K12	K11	K10	K13	– *2	High	Low	K10–K13 input port data
					K12	– *2	High	Low	
	R				K11	– *2	High	Low	
					K10	– *2	High	Low	
FF26H	KCP13	KCP12	KCP11	KCP10	KCP13	1	↓	↑	K10–K13 input comparison register
					KCP12	1	↓	↑	
	R/W				KCP11	1	↓	↑	
					KCP10	1	↓	↑	
FF28H	0	0	0	SIK20	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R			R/W	0 *3	– *2			Unused
					SIK20	0	Enable	Disable	K20 interrupt selection register

Remarks

∗1 Initial value at initial reset

∗2 Not set in the circuit

∗3 Constantly "0" when being read

Table 4.1.1 (b) I/O memory map (FF29H–FF44H)

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
FF29H	0	0	0	K20	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R				0 *3	– *2			Unused
					K20	– *2	High	Low	K20 input port data
FF2AH	0	0	0	KCP20	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R			R/W	0 *3	– *2			Unused
					KCP20	1	↓	↑	K20 input comparison register
FF2BH	0	0	0	SENON	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R			R/W	0 *3	– *2			Unused
					SENON	1	On	Off	Key sense On/Off control
FF30H	R03HIZ	R02HIZ	R01HIZ	R00HIZ	R03HIZ	0	High-Z	Output	R03 output high impedance control (FOUTE=0) FOUT output high impedance control (FOUTE=1)
					R02HIZ	0	High-Z	Output	R02 output high impedance control (PTOUT=0) TOUT output high impedance control (PTOUT=1)
	R/W				R01HIZ	0	High-Z	Output	R01 output high impedance control
					R00HIZ	0	High-Z	Output	R00 output high impedance control
FF31H	R03	R02	R01	R00	R03	1	High	Low	R03 output port data (FOUTE=0) Fix at "1" when FOUT is used
					R02	1	High	Low	R02 output port data (PTOUT=0) Fix at "1" when TOUT is used
	R/W				R01	1	High	Low	R01 output port data
					R00	1	High	Low	R00 output port data
FF32H	0	0	0	R1HIZ	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R			R/W	0 *3	– *2			Unused
					R1HIZ	0	High-Z	Output	R1 output high impedance control
FF33H	R13	R12	R11	R10	R13	1	High	Low	R10–R13 output port data
					R12	1	High	Low	
	R/W				R11	1	High	Low	
					R10	1	High	Low	
FF34H	0	0	0	R2HIZ	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R			R/W	0 *3	– *2			Unused
					R2HIZ	0	High-Z	Output	R2 output high impedance control
FF35H	R23	R22	R21	R20	R23	1	High	Low	R20–R23 output port data
					R22	1	High	Low	
	R/W				R21	1	High	Low	
					R20	1	High	Low	
FF40H	IOC03	IOC02	IOC01	IOC00	IOC03	0	Output	Input	P00–P03 I/O control register
					IOC02	0	Output	Input	
	R/W				IOC01	0	Output	Input	
					IOC00	0	Output	Input	
FF41H	PUL03	PUL02	PUL01	PUL00	PUL03	1	On	Off	P00–P03 pull-up control register
					PUL02	1	On	Off	
	R/W				PUL01	1	On	Off	
					PUL00	1	On	Off	
FF42H	P03	P02	P01	P00	P03	– *2	High	Low	P00–P03 I/O port data
					P02	– *2	High	Low	
	R/W				P01	– *2	High	Low	
					P00	– *2	High	Low	
FF44H	IOC13	IOC12	IOC11	IOC10	IOC13	0	Output	Input	P13 I/O control register functions as a general-purpose register when SIF (slave) is selected
					IOC12	0	Output	Input	P12 I/O control register (ESIF=0) functions as a general-purpose register when SIF is selected
	R/W				IOC11	0	Output	Input	P11 I/O control register (ESIF=0) functions as a general-purpose register when SIF is selected
					IOC10	0	Output	Input	P10 I/O control register (ESIF=0) functions as a general-purpose register when SIF is selected

Table 4.1.1 (c) I/O memory map (FF45H–FF51H)

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
FF45H	PUL13	PUL12	PUL11	PUL10	PUL13	1	On	Off	P13 pull-up control register functions as a general-purpose register when SIF (slave) is selected
					PUL12	1	On	Off	P12 pull-up control register (ESIF=0) functions as a general-purpose register when SIF (master) is selected $\overline{SCLK}$ (I) pull-up control register when SIF (slave) is selected
	R/W				PUL11	1	On	Off	P11 pull-up control register (ESIF=0) functions as a general-purpose register when SIF is selected
					PUL10	1	On	Off	P10 pull-up control register (ESIF=0) SIN pull-up control register when SIF is selected
FF46H	P13	P12	P11	P10	P13	– *2	High	Low	P13 I/O port data functions as a general-purpose register when SIF (slave) is selected
					P12	– *2	High	Low	P12 I/O port data (ESIF=0) functions as a general-purpose register when SIF is selected
	R/W				P11	– *2	High	Low	P11 I/O port data (ESIF=0) functions as a general-purpose register when SIF is selected
					P10	– *2	High	Low	P10 I/O port data (ESIF=0) functions as a general-purpose register when SIF is selected
FF48H	IOC23	IOC22	IOC21	IOC20	IOC23	0	Output	Input	P20–P23 I/O control register
					IOC22	0	Output	Input	
	R/W				IOC21	0	Output	Input	
					IOC20	0	Output	Input	
FF49H	PUL23	PUL22	PUL21	PUL20	PUL23	1	On	Off	P20–P23 pull-up control register
					PUL22	1	On	Off	
	R/W				PUL21	1	On	Off	
					PUL20	1	On	Off	
FF4AH	P23	P22	P21	P20	P23	– *2	High	Low	P20–P23 I/O port data
					P22	– *2	High	Low	
	R/W				P21	– *2	High	Low	
					P20	– *2	High	Low	
FF4CH	IOC33	IOC32	IOC31	IOC30	IOC33	0	Output	Input	P30–P33 I/O control register
					IOC32	0	Output	Input	
	R/W				IOC31	0	Output	Input	
					IOC30	0	Output	Input	
FF4DH	PUL33	PUL32	PUL31	PUL30	PUL33	1	On	Off	P30–P33 pull-up control register
					PUL32	1	On	Off	
	R/W				PUL31	1	On	Off	
					PUL30	1	On	Off	
FF4EH	P33	P32	P31	P30	P33	– *2	High	Low	P30–P33 I/O port data
					P32	– *2	High	Low	
	R/W				P31	– *2	High	Low	
					P30	– *2	High	Low	
FF50H	IOC43	IOC42	IOC41	IOC40	IOC43	0	Output	Input	P43 I/O control register (PAD3=0) functions as a general-purpose register when A/D is enabled
					IOC42	0	Output	Input	P42 I/O control register (PAD2=0) functions as a general-purpose register when A/D is enabled
	R/W				IOC41	0	Output	Input	P41 I/O control register (PAD1=0) functions as a general-purpose register when A/D is enabled
					IOC40	0	Output	Input	P40 I/O control register (PAD0=0) functions as a general-purpose register when A/D is enabled
FF51H	PUL43	PUL42	PUL41	PUL40	PUL43	1	1	0	General-purpose register
					PUL42	1	1	0	
	R/W				PUL41	1	1	0	
					PUL40	1	1	0	

Table 4.1.1 (d) I/O memory map (FF52H–FFC1H)

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
FF52H	P43	P42	P41	P40	P43	– *2	High	Low	P43 I/O port data (PAD3=0) functions as a general-purpose register when A/D is enabled
					P42	– *2	High	Low	P42 I/O port data (PAD2=0) functions as a general-purpose register when A/D is enabled
	R/W				P41	– *2	High	Low	P41 I/O port data (PAD1=0) functions as a general-purpose register when A/D is enabled
					P40	– *2	High	Low	P40 I/O port data (PAD0=0) functions as a general-purpose register when A/D is enabled
FF60H	LDUTY1	LDUTY0	VCCHG	LPWR	LDUTY1	0			LCD drive duty switch [LDUTY1, 0]: 0 = Duty 1/4, 1 = Duty 1/3, 2, 3 = Duty 1/2
					LDUTY0	0			
	R/W				VCCHG	0			General-purpose register (reserved register)
					LPWR	0	On	Off	LCD power On/Off
FF61H	0	ALOFF	ALON	STCD	0 *3	– *2			Unused
					ALOFF	1	All Off	Normal	LCD all OFF control
	R	R/W			ALON	0	All On	Normal	LCD all ON control
					STCD	0	Static	Dynamic	Common output signal control
FF64H	0	ENON	BZFQ	BZON	0 *3	– *2			Unused
					ENON	0	On	Off	2 Hz intervai On/Off
	R	R/W			BZFQ	0	2 kHz	4 kHz	Buzzer frequency selection
					BZON	0	On	Off	Buzzer output On/Off
FF70H	0	ESOUT	SCTRG	ESIF	0 *3	– *2			Unused
					ESOUT	0	Enable	Disable	SOUT enable/disable control
	R	R/W			SCTRG	0	Trigger	Invalid	Serial I/F clock trigger (writing)
							Run	Stop	Serial I/F clock status (reading)
					ESIF	0	SIF	I/O	Serial I/F enable (P1 port function selection)
FF71H	SDP	SCPS	SCS1	SCS0	SDP	0	MSB first	LSB first	Serial I/F data input/output permutation
					SCPS	0	↓	↑	Serial I/F clock phase selection [SCS1, 0]: 0 = Clock Slave, 1 = PT
	R/W				SCS1	0			Serial I/F clock mode selection [SCS1, 0]: 2 = Clock OSC1/2, 3 = OSC1
					SCS0	0			
FF72H	SD3	SD2	SD1	SD0	SD3	– *2	High	Low	MSB Serial I/F transmit/receive data (low-order 4 bits) LSB
					SD2	– *2	High	Low	
	R/W				SD1	– *2	High	Low	
					SD0	– *2	High	Low	
FF73H	SD7	SD6	SD5	SD4	SD7	– *2	High	Low	MSB Serial I/F transmit/receive data (high-order 4 bits) LSB
					SD6	– *2	High	Low	
	R/W				SD5	– *2	High	Low	
					SD4	– *2	High	Low	
FF78H	0	0	TMRST	TMRUN	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R		W	R/W	TMRST*3	Reset	Reset	Invalid	Clock timer reset (writing)
					TMRUN	0	Run	Stop	Clock timer Run/Stop
FF79H	TM3	TM2	TM1	TM0	TM3	0			Clock timer data (16 Hz)
					TM2	0			Clock timer data (32 Hz)
	R				TM1	0			Clock timer data (64 Hz)
					TM0	0			Clock timer data (128 Hz)
FF7AH	TM7	TM6	TM5	TM4	TM7	0			Clock timer data (1 Hz)
					TM6	0			Clock timer data (2 Hz)
	R				TM5	0			Clock timer data (4 Hz)
					TM4	0			Clock timer data (8 Hz)
FFC0H	MODE16	EVCNT	FCSEL	PLPOL	MODEL16	0	16 bit × 1	8 bit × 2	8 bit × 2 or 16 bit × 1 timer mode selection
					EVCNT	0	Event ct.	Timer	Timer 0 counter mode selection
	R/W				FCSEL	0	With NR	No NR	Timer 0 function selection (for event counter mode)
					PLPOL	0	↑	↓	Timer 0 pulse polarity selection (for event counter mode)
FFC1H	CHSEL	PTOUT	CKSEL1	CKSEL0	CHSEL	0	Timer1	Timer0	TOUT output channel selection
					PTOUT	0	On	Off	TOUT output control
	R/W				CKSEL1	0	OSC3	OSC1	Prescaler 1 source clock selection
					CKSEL0	0	OSC3	OSC1	Prescaler 0 source clock selection

Table 4.1.1 (e) I/O memory map (FFC2H–FFD3H)

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
FFC2H	PTPS01	PTPS00	PTRST0	PTRUN0	PTPS01	0			Prescaler 0 division ratio selection [PTPS01, 00]: 0 = 1/1, 1 = 1/4, 2 = 1/32, 3 = 1/256
					PTPS00	0			
	R/W		W	R/W	PTRST0*3	– *2	Reset	Invalid	Timer 0 reset (reload)
					PTRUN0	0	Run	Stop	Timer 0 Run/Stop
FFC3H	PTPS11	PTPS10	PTRST1	PTRUN1	PTPS11	0			Prescaler 1 division ratio selection [PTPS11, 10]: 0 = 1/1, 1 = 1/4, 2 = 1/32, 3 = 1/256
					PTPS10	0			
	R/W		W	R/W	PTRST1*3	– *2	Reset	Invalid	Timer 1 reset (reload)
					PTRUN1	0	Run	Stop	Timer 1 Run/Stop
FFC4H	RLD03	RLD02	RLD01	RLD00	RLD03	0			MSB
					RLD02	0			Programmable timer 0 reload data (low-order 4 bits)
	R/W				RLD01	0			
					RLD00	0			LSB
FFC5H	RLD07	RLD06	RLD05	RLD04	RLD07	0			MSB
					RLD06	0			Programmable timer 0 reload data (high-order 4 bits)
	R/W				RLD05	0			
					RLD04	0			LSB
FFC6H	RLD13	RLD12	RLD11	RLD10	RLD13	0			MSB
					RLD12	0			Programmable timer 1 reload data (low-order 4 bits)
	R/W				RLD11	0			
					RLD10	0			LSB
FFC7H	RLD17	RLD16	RLD15	RLD14	RLD17	0			MSB
					RLD16	0			Programmable timer 1 reload data (high-order 4 bits)
	R/W				RLD15	0			
					RLD14	0			LSB
FFC8H	PTD03	PTD02	PTD01	PTD00	PTD03	0			MSB
					PTD02	0			Programmable timer 0 data (low-order 4 bits)
	R				PTD01	0			
					PTD00	0			LSB
FFC9H	PTD07	PTD06	PTD05	PTD04	PTD07	0			MSB
					PTD06	0			Programmable timer 0 data (high-order 4 bits)
	R				PTD05	0			
					PTD04	0			LSB
FFCAH	PTD13	PTD12	PTD11	PTD10	PTD13	0			MSB
					PTD12	0			Programmable timer 1 data (low-order 4 bits)
	R				PTD11	0			
					PTD10	0			LSB
FFCBH	PTD17	PTD16	PTD15	PTD14	PTD17	0			MSB
					PTD16	0			Programmable timer 1 data (high-order 4 bits)
	R				PTD15	0			
					PTD14	0			LSB
FFD0H	ADRUN	ADCLK	CHS1	CHS0	ADRUN	0	Start	Invalid	A/D Run/Off control
					ADCLK	0	OSC3	OSC1	A/D input clock selection
	W	R/W			CHS1	0			A/D input channel selection [CHS1, 0]: 0 = P40, 1 = P41, 2 = P42, 3 = P43
					CHS0	0			
FFD1H	PAD3	PAD2	PAD1	PAD0	PAD3	0	Enable	Disable	P43 input channel enable/disable control
					PAD2	0	Enable	Disable	P42 input channel enable/disable control
	R/W				PAD1	0	Enable	Disable	P41 input channel enable/disable control
					PAD0	0	Enable	Disable	P40 input channel enable/disable control
FFD2H	ADDR3	ADDR2	ADDR1	ADDR0	ADDR3	– *2			A/D converted data (D0–D3)
					ADDR2	– *2			
	R				ADDR1	– *2			
					ADDR0	– *2			
FFD3H	ADDR8	ADDR6	ADDR5	ADDR4	ADDR7	– *2			A/D converted data (D4–D7)
					ADDR6	– *2			
	R				ADDR5	– *2			
					ADDR4	– *2			

Table 4.1.1 (f) I/O memory map (FFE2H–FFF7H)

Address	Register								Comment
	D3	D2	D1	D0	Name	Init *1	1	0	
FFE2H	0	0	EIPT1	EIPT0	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R		R/W		EIPT1	0	Enable	Mask	Interrupt mask register (Programmable timer 1)
					EIPT0	0	Enable	Mask	Interrupt mask register (Programmable timer 0)
FFE3H	0	0	0	EISIF	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R			R/W	0 *3	– *2			Unused
					EISIF	0	Enable	Mask	Interrupt mask register (Serial I/F)
FFE4H	0	0	0	EIK0	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R			R/W	0 *3	– *2			Unused
					EIK0	0	Enable	Mask	Interrupt mask register (K00–K03)
FFE5H	0	0	EIK2	EIK1	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R		R/W		EIK2	0	Enable	Mask	Interrupt mask register (K20)
					EIK1	0	Enable	Mask	Interrupt mask register (K10–K13)
FFE6H	EIT3	EIT2	EIT1	EIT0	EIT3	0	Enable	Mask	Interrupt mask register (Clock timer 1 Hz)
					EIT2	0	Enable	Mask	Interrupt mask register (Clock timer 2 Hz)
	R/W				EIT1	0	Enable	Mask	Interrupt mask register (Clock timer 8 Hz)
					EIT0	0	Enable	Mask	Interrupt mask register (Clock timer 16 Hz)
FFE7H	0	0	0	EIAD	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R			R/W	0 *3	– *2			Unused
					EIAD	0	Enable	Mask	Interrupt mask register (A/D converter)
FFF2H	0	0	IPT1	IPT0	0 *3	– *2	(R)	(R)	Unused
					0 *3	– *2	Yes	No	Unused
	R		R/W		IPT1	0	(W)	(W)	Interrupt factor flag (Programmable timer 1)
					IPT0	0	Reset	Invalid	Interrupt factor flag (Programmable timer 0)
FFF3H	0	0	0	ISIF	0 *3	– *2	(R)	(R)	Unused
					0 *3	– *2	Yes	No	Unused
	R			R/W	0 *3	– *2	(W)	(W)	Unused
					ISIF	0	Reset	Invalid	Interrupt factor flag (Serial I/F)
FFF4H	0	0	0	IK0	0 *3	– *2	(R)	(R)	Unused
					0 *3	– *2	Yes	No	Unused
	R			R/W	0 *3	– *2	(W)	(W)	Unused
					IK0	0	Reset	Invalid	Interrupt factor flag (K00–K03)
FFF5H	0	0	IK2	IK1	0 *3	– *2	(R)	(R)	Unused
					0 *3	– *2	Yes	No	Unused
	R		R/W		IK2	0	(W)	(W)	Interrupt factor flag (K20)
					IK1	0	Reset	Invalid	Interrupt factor flag (K10–K13)
FFF6H	IT3	IT2	IT1	IT0	IT3	0	(R)	(R)	Interrupt factor flag (Clock timer 1 Hz)
					IT2	0	Yes	No	Interrupt factor flag (Clock timer 2 Hz)
	R/W				IT1	0	(W)	(W)	Interrupt factor flag (Clock timer 8 Hz)
					IT0	0	Reset	Invalid	Interrupt factor flag (Clock timer 16 Hz)
FFF7H	0	0	0	IAD	0 *3	– *2	(R)	(R)	Unused
					0 *3	– *2	Yes	No	Unused
	R			R/W	0 *3	– *2	(W)	(W)	Unused
					IAD	0	Reset	Invalid	Interrupt factor flag (A/D converter)

4.2 Watchdog Timer

4.2.1 Configuration of watchdog timer

The E0C63P366 has a built-in watchdog timer that operates with a 256 Hz divided clock from the OSC1 as the source clock. The watchdog timer starts operating after initial reset, however, it can be stopped by the software. The watchdog timer must be reset cyclically by the software while it operates. If the watchdog timer is not reset in at least 3–4 seconds, it generates a non-maskable interrupt (NMI) to the CPU.
Figure 4.2.1.1 is the block diagram of the watchdog timer.

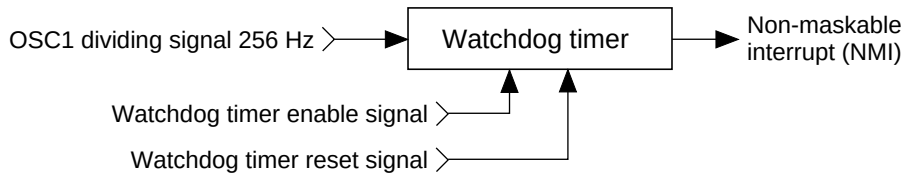


Fig. 4.2.1.1 Watchdog timer block diagram

The watchdog timer contains a 10-bit binary counter, and generates the non-maskable interrupt when the last stage of the counter (0.25 Hz) overflows.
Watchdog timer reset processing in the program's main routine enables detection of program overrun, such as when the main routine's watchdog timer processing is bypassed. Ordinarily this routine is incorporated where periodic processing takes place, just as for the timer interrupt routine.
The watchdog timer operates in the HALT mode. If a HALT status continues for 3–4 seconds, the non-maskable interrupt releases the HALT status.

4.2.2 Interrupt function

If the watchdog timer is not reset periodically, the non-maskable interrupt (NMI) is generated to the core CPU. Since this interrupt cannot be masked, it is accepted even in the interrupt disable status (I flag = "0"). However, it is not accepted when the CPU is in the interrupt mask state until SP1 and SP2 are set as a pair, such as after initial reset or during re-setting the stack pointer. The interrupt vector of NMI is assigned to 0100H in the program memory.

4.2.3 I/O memory of watchdog timer

Table 4.2.3.1 shows the I/O address and control bits for the watchdog timer.

Table 4.2.3.1 Control bits of watchdog timer

Address	Register								Comment
	D3	D2	D1	D0	Name	Init *1	1	0	
FF07H	0	0	WDEN	WDRST	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R		R/W	W	WDEN	1	Enable	Disable	Watchdog timer enable
					WDRST*3	Reset	Reset	Invalid	Watchdog timer reset (writing)

*1 Initial value at initial reset

*2 Not set in the circuit

*3 Constantly "0" when being read

WDEN: Watchdog timer enable register (FF07H•D1)

Selects whether the watchdog timer is used (enabled) or not (disabled).

When "1" is written: Enabled
When "0" is written: Disabled
Reading: Valid

When "1" is written to the WDEN register, the watchdog timer starts count operation. When "0" is written, the watchdog timer does not count and does not generate the interrupt (NMI).
At initial reset, this register is set to "1".

WDRST: Watchdog timer reset (FF07H•D0)

Resets the watchdog timer.

When "1" is written: Watchdog timer is reset
When "0" is written: No operation
Reading: Always "0"

When "1" is written to WDRST, the watchdog timer is reset and restarts immediately after that. When "0" is written, no operation results.
This bit is dedicated for writing, and is always "0" for reading.

4.2.4 Programming notes

(1) When the watchdog timer is being used, the software must reset it within 3-second cycles.

(2) Because the watchdog timer is set in operation state by initial reset, set the watchdog timer to disabled state (not used) before generating an interrupt (NMI) if it is not used.

4.3 Oscillation Circuit

4.3.1 Configuration of oscillation circuit

The E0C63P366 has two oscillation circuits (OSC1 and OSC3). OSC1 is a crystal oscillation circuit that supplies the operating clock to the CPU and peripheral circuits. OSC3 is either a CR or a ceramic oscillation circuit. When processing with the E0C63P366 requires high-speed operation, the CPU operating clock can be switched from OSC1 to OSC3 by the software.
Figure 4.3.1.1 is the block diagram of this oscillation system.

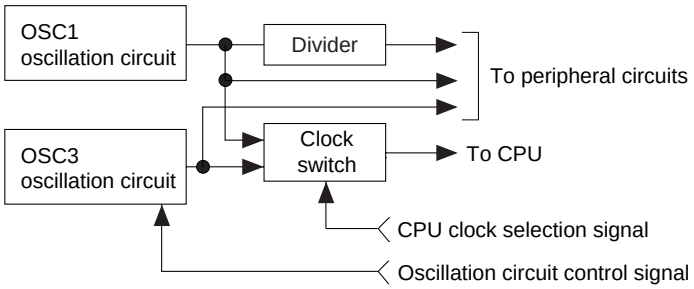


Fig. 4.3.1.1 Oscillation system block diagram

4.3.2 OSC1 oscillation circuit

The OSC1 oscillation circuit generates the main clock for the CPU and the peripheral circuits. The oscillator type is a crystal oscillation circuit and the oscillation frequency is 32.768 kHz (Typ.).
Figure 4.3.2.1 is the block diagram of the OSC1 oscillation circuit.

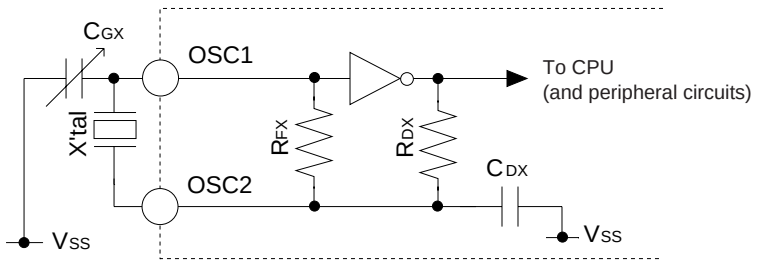
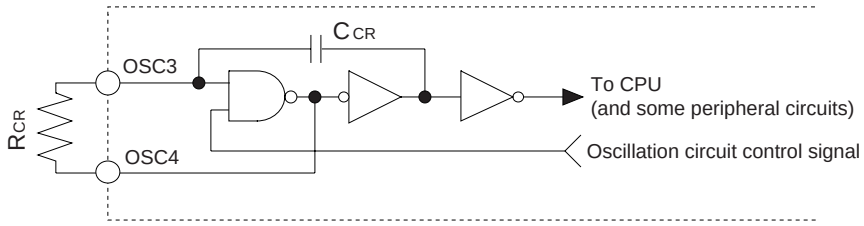


Fig. 4.3.2.1 OSC1 oscillation circuit

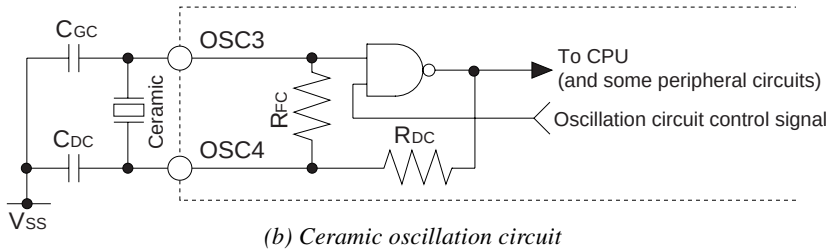
As shown in Figure 4.3.2.1, the crystal oscillation circuit can be configured simply by connecting the crystal oscillator (X'tal) of 32.768 kHz (Typ.) between the OSC1 and OSC2 terminals and the trimmer capacitor (C_{GX}) between the OSC1 and V_{SS} terminals.

4.3.3 OSC3 oscillation circuit

The E0C63P366 has built-in the OSC3 oscillation circuit that generates the CPU's sub-clock for high speed operation and the source clock for peripheral circuits needing a high speed clock (programmable timer, FOUT output). The mask option enables selection of either the CR (Typ. 1.8 MHz) or ceramic (Max. 4 MHz ceramic oscillation) oscillation circuit. When CR oscillation is selected, only a resistance is required as an external element. When ceramic oscillation is selected, a ceramic oscillator and two capacitors (gate and drain capacitance) are required.
Figure 4.3.3.1 is the block diagram of the OSC3 oscillation circuit.



(a) CR oscillation circuit



(b) Ceramic oscillation circuit

Fig. 4.3.3.1 OSC3 oscillation circuit

As shown in Figure 4.3.3.1, the CR oscillation circuit can be configured simply by connecting the resistor RCR between the OSC3 and OSC4 terminals when CR oscillation is selected. See Chapter 9, "Electrical Characteristics" for resistance value of RCR.
When ceramic oscillation is selected, the ceramic oscillation circuit can be configured by connecting the ceramic oscillator (Max. 4 MHz) between the OSC3 and OSC4 terminals, capacitor CGC between the OSC3 and OSC4 terminals, and capacitor CDC between the OSC4 and VSS terminals. For both CGC and CDC, connect capacitors that are about 100 pF. To reduce current consumption of the OSC3 oscillation circuit, oscillation can be stopped by the software (OSCC register).

4.3.4 Operating voltage

The E0C63P366 generates the V_{D1} voltage internally for the oscillation circuit in order to stabilize oscillation. In the E0C63P366, the V_{D1} voltage is used only for the oscillation circuit and the voltage level is fixed at 2.05±0.3 V.
Therefore, setting of the VDC register (FF00H•D0) required in the mask ROM model is invalidated and does not affect the V_{D1} voltage level.
When using the E0C63P366 as a development tool for the E0C63358/63158, switch the operating voltage using the VDC register according to the control sequence of the model (refer to the "Technical Manual").
Furthermore, internal logic circuits (including the OSC3 oscillation circuit) of the E0C63P366 except for the OSC1 oscillation circuit operate with the source voltage supplied between the V_{DD} and V_{SS} terminal.

4.3.5 Switching operating clock

The CPU system clock is switched to OSC1 or OSC3 by the software (CLKCHG register).
When using OSC3 as the CPU system clock, first turn the OSC3 oscillation ON and then switch the clock after waiting 5 msec or more for oscillation stabilization.
When switching from OSC3 to OSC1, turn the OSC3 oscillation circuit OFF after switching the clock.

OSC1 → OSC3

1. Set OSCC to "1" (OSC3 oscillation ON).
2. Maintain 5 msec or more.
3. Set CLKCHG to "1" (OSC1 → OSC3).

OSC3 → OSC1

1. Set CLKCHG to "0" (OSC3 → OSC1).
2. Set OSCC to "0" (OSC3 oscillation OFF).

4.3.6 Clock frequency and instruction execution time

Table 4.3.6.1 shows the instruction execution time according to each frequency of the system clock.

Table 4.3.6.1 Clock frequency and instruction execution time

Clock frequency	Instruction execution time (µsec)		
	1-cycle instruction	2-cycle instruction	3-cycle instruction
OSC1: 32.768 kHz	61	122	183
OSC3: 4 MHz	0.5	1	1.5

4.3.7 I/O memory of oscillation circuit

Table 4.3.7.1 shows the I/O address and the control bits for the oscillation circuit.

Table 4.3.7.1 Control bits of oscillation circuit

Address	Register								Comment
	D3	D2	D1	D0	Name	Init *1	1	0	
FF00H	CLKCHG	OSCC	0	VDC	CLKCHG	0	OSC3	OSC1	CPU clock switch
					OSCC	0	On	Off	OSC3 oscillation On/Off
	R/W		R	R/W	0 *3	– *2			Unused
					VDC	0	(OSC3)	(OSC1)	(Operating voltage switch)

*1 Initial value at initial reset

*2 Not set in the circuit

*3 Constantly "0" when being read

VDC: Operating voltage switching register (FF00H•D0)

In the E0C63P366, the value set in this register does not affect the V_{D1} voltage level. However, note that the register value affects the CLKCHG register that switches the CPU clock.
When using the E0C63P366 as a development tool for the E0C63358/63158, switch the operating voltage using this register according to the control sequence of the model (refer to the "Technical Manual").
At initial reset, this register is set to "0".

OSCC: OSC3 oscillation control register (FF00H•D2)

Controls oscillation ON/OFF for the OSC3 oscillation circuit.

When "1" is written: OSC3 oscillation ON
When "0" is written: OSC3 oscillation OFF
Reading: Valid

When it is necessary to operate the CPU at high speed, set OSCC to "1". At other times, set it to "0" to reduce current consumption.
At initial reset, this register is set to "0".

CLKCHG: CPU system clock switching register (FF00H•D3)

The CPU's operation clock is selected with this register.

When "1" is written: OSC3 clock is selected
When "0" is written: OSC1 clock is selected
Reading: Valid

When the CPU clock is to be OSC3, set CLKCHG to "1"; for OSC1, set CLKCHG to "0".
After turning the OSC3 oscillation ON (OSCC = "1"), switching of the clock should be done after waiting 5 msec or more.
When VDC = "0" and/or when OSC3 oscillation is OFF (OSCC = "0"), setting of CLKCHG = "1" becomes invalid and switching to OSC3 is not performed.
At initial reset, this register is set to "0".

4.3.8 Programming notes

(1) It takes at least 5 msec from the time the OSC3 oscillation circuit goes ON until the oscillation stabilizes. Consequently, when switching the CPU operation clock from OSC1 to OSC3, do this after a minimum of 5 msec have elapsed since the OSC3 oscillation went ON.
Further, the oscillation stabilization time varies depending on the external oscillator characteristics and conditions of use, so allow ample margin when setting the wait time.

(2) When switching the clock form OSC3 to OSC1, use a separate instruction for switching the OSC3 oscillation OFF. An error in the CPU operation can result if this processing is performed at the same time by the one instruction.

(3) In the E0C63P366, the VDC register value does not affect the V_{D1} voltage level. However, note that the CPU clock cannot be switched from OSC1 to OSC3 using the CLKCHG register if the VDC register value is "0".
When using the E0C63P366 as a development tool for the E0C63358/63158, switch the operating voltage using the VDC register according to the control sequence of the model (refer to the "Technical Manual").

4.4 Input Ports (K00–K03, K10–K13 and K20)

4.4.1 Configuration of input ports

The E0C63P366 has nine bits of general-purpose input ports. Each of the input port terminals (K00–K03, K10–K13, K20) provides internal pull-up resistor.
Figure 4.4.1.1 shows the configuration of input port (K00–K03, K10–K13).
Figure 4.4.1.2 shows the configuration of input port (K20).

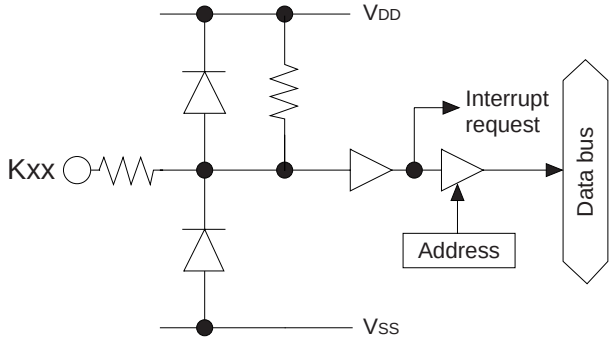


Fig. 4.4.1.1 Configuration of input port (K00–K03, K10–K13)

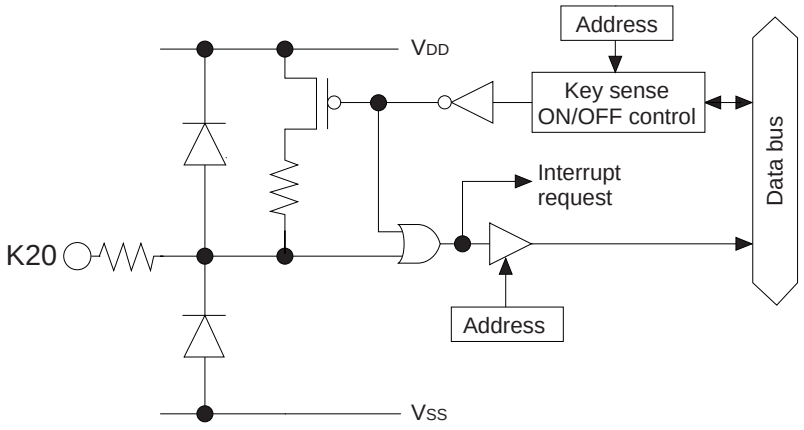


Fig. 4.4.1.2 Configuration of input port (K20)

4.4.2 Interrupt function

All nine bits of the input ports (K00–K03, K10–K13, K20) provide the interrupt function. The conditions for issuing an interrupt can be set by the software. Further, whether to mask the interrupt function can be selected by the software. The input interrupts are divided into three systems: K0 (K00–K03), K1 (K10–K13) and K20 systems.
Figure 4.4.2.1 shows the configuration of K00–K03 (K10–K13) interrupt circuit.
Figure 4.4.2.2 shows the configuration of K20 interrupt circuit.

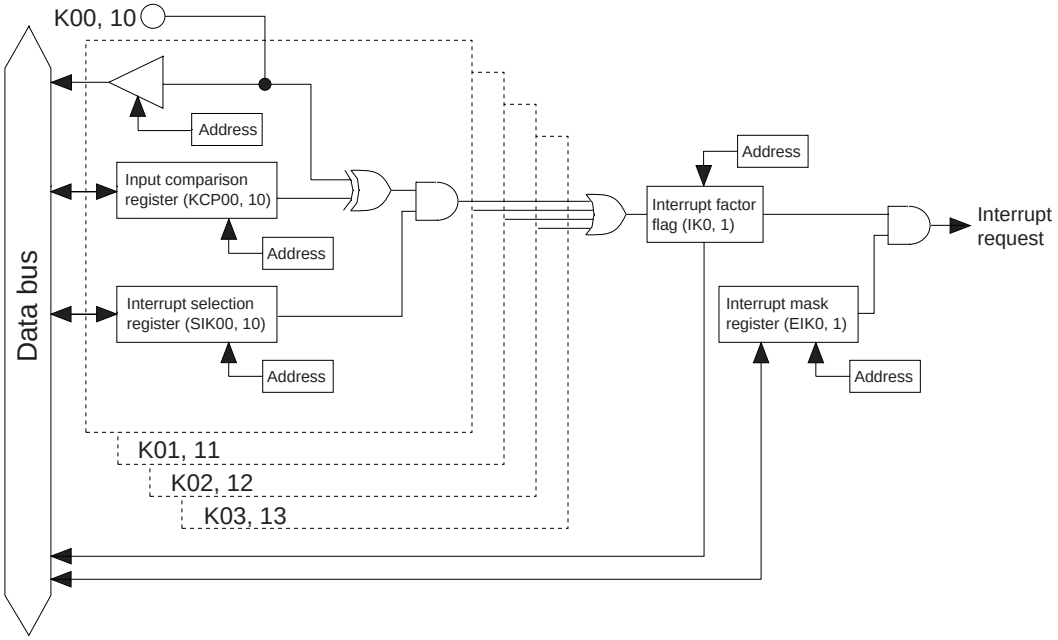


Fig. 4.4.2.1 Input interrupt circuit configuration (K00–K03, K10–K13)

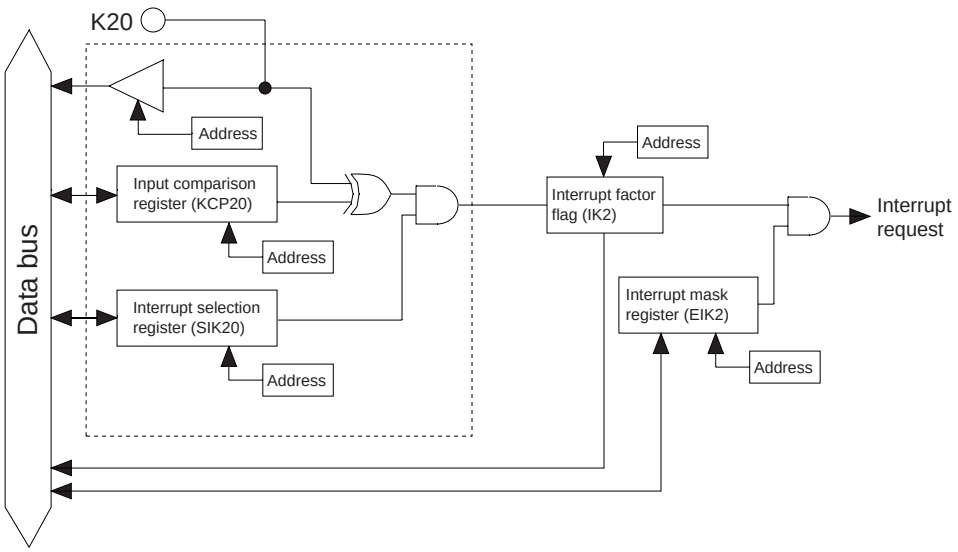


Fig. 4.4.2.2 Input interrupt circuit configuration (K20)

The interrupt selection register (SIK) and input comparison register (KCP) are individually set for the input ports K00–K03, K10–K13 and K20, and can specify the terminals for generating interrupt and interrupt timing.
The interrupt selection registers (SIK00–SIK03, SIK10–SIK13, SIK20) select what input of K00–K03, K10–K13 and K20 to use for the interrupt. Writing "1" into an interrupt selection register incorporates that input port into the interrupt generation conditions. The changing the input port where the interrupt selection register has been set to "0" does not affect the generation of the interrupt.
The input interrupt timing can select that the interrupt be generated at the rising edge of the input or that it be generated at the falling edge according to the set value of the input comparison registers (KCP00–KCP03, KCP10–KCP13, KCP20).
By setting these two conditions, the interrupt for K00–K03, K10–K13 or K20 is generated when input ports in which an interrupt has been enabled by the input selection registers and the contents of the input comparison registers have been changed from matching to no matching.
The interrupt mask registers (EIK0, EIK1, EIK2) enable the interrupt mask to be selected for K00–K03, K10–K13 and K20.
When the interrupt is generated, the interrupt factor flag (IK0, IK1, IK2) is set to "1".
Figure 4.4.2.3 shows an example of an interrupt for K00–K03.

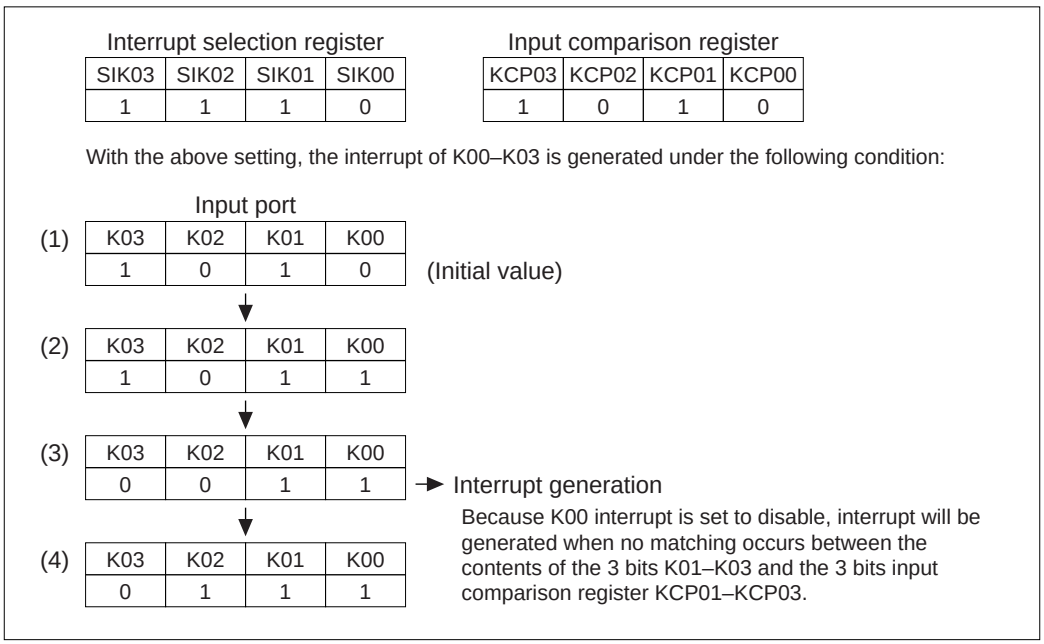


Fig. 4.4.2.3 Example of interrupt of K00–K03

K00 interrupt is disabled by the interrupt selection register (SIK00), so that an interrupt does not occur at (2). At (3), K03 changes to "0"; the data of the terminals that are interrupt enabled no longer match the data of the input comparison registers, so that interrupt occurs. As already explained, the condition for the interrupt to occur is the change in the port data and contents of the input comparison registers from matching to no matching. Hence, in (4), when the no matching status changes to another no matching status, an interrupt does not occur. Further, terminals that have been masked for interrupt do not affect the conditions for interrupt generation.

4.4.3 Mask option

In the E0C63P366, the input port specification is fixed at "Input with pull-up resistor".

4.4.4 I/O memory of input ports

Table 4.4.4.1 shows the I/O addresses and the control bits for the input ports.

Table 4.4.4.1 Control bits of input ports

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
FF20H	SIK03	SIK02	SIK01	SIK00	SIK03	0	Enable	Disable	K00–K03 interrupt selection register
					SIK02	0	Enable	Disable	
	R/W				SIK01	0	Enable	Disable	
					SIK00	0	Enable	Disable	
FF21H	K03	K02	K01	K00	K03	– *2	High	Low	K00–K03 input port data
					K02	– *2	High	Low	
	R				K01	– *2	High	Low	
					K00	– *2	High	Low	
FF22H	KCP03	KCP02	KCP01	KCP00	KCP03	1	↓	↑	K00–K03 input comparison register
					KCP02	1	↓	↑	
	R/W				KCP01	1	↓	↑	
					KCP00	1	↓	↑	
FF24H	SIK13	SIK12	SIK11	SIK10	SIK13	0	Enable	Disable	K10–K13 interrupt selection register
					SIK12	0	Enable	Disable	
	R/W				SIK11	0	Enable	Disable	
					SIK10	0	Enable	Disable	
FF25H	K13	K12	K11	K10	K13	– *2	High	Low	K10–K13 input port data
					K12	– *2	High	Low	
	R				K11	– *2	High	Low	
					K10	– *2	High	Low	
FF26H	KCP13	KCP12	KCP11	KCP10	KCP13	1	↓	↑	K10–K13 input comparison register
					KCP12	1	↓	↑	
	R/W				KCP11	1	↓	↑	
					KCP10	1	↓	↑	
FF28H	0	0	0	SIK20	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R			R/W	0 *3	– *2			Unused
					SIK20	0	Enable	Disable	K20 interrupt selection register
FF29H	0	0	0	K20	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R				0 *3	– *2			Unused
					K20	– *2	High	Low	K20 input port data
FF2AH	0	0	0	KCP20	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R			R/W	0 *3	– *2			Unused
					KCP20	1	↓	↑	K20 input comparison register
FF2BH	0	0	0	SENON	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R			R/W	0 *3	– *2			Unused
					SENON	1	On	Off	Key sense On/Off control
FFE4H	0	0	0	EIK0	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R			R/W	0 *3	– *2			Unused
					EIK0	0	Enable	Mask	Interrupt mask register (K00–K03)
FFE5H	0	0	EIK2	EIK1	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R		R/W		EIK2	0	Enable	Mask	Interrupt mask register (K20)
					EIK1	0	Enable	Mask	Interrupt mask register (K10–K13)
FFF4H	0	0	0	IK0	0 *3	– *2	(R)	(R)	Unused
					0 *3	– *2	Yes	No	Unused
	R			R/W	0 *3	– *2	(W)	(W)	Unused
					IK0	0	Reset	Invalid	Interrupt factor flag (K00–K03)
FFF5H	0	0	IK2	IK1	0 *3	– *2	(R)	(R)	Unused
					0 *3	– *2	Yes	No	Unused
	R		R/W		IK2	0	(W)	(W)	Interrupt factor flag (K20)
					IK1	0	Reset	Invalid	Interrupt factor flag (K10–K13)

*1 Initial value at initial reset *2 Not set in the circuit *3 Constantly "0" when being read

K00–K03: K0 port input port data (FF21H)
K10–K13: K1 port input port data (FF25H)
K20: K20 port input port data (FF29H•D0)

Input data of the input port terminals can be read with these registers.

When "1" is read: High level
When "0" is read: Low level
Writing: Invalid

The reading is "1" when the terminal voltage of the nine bits of the input ports (K00–K03, K10–K13, K20) goes high (V_{DD}), and "0" when the voltage goes low (V_{SS}).
These bits are dedicated for reading, so writing cannot be done.

SIK00–SIK03: K0 port interrupt selection register (FF20H)
SIK10–SIK13: K1 port interrupt selection register (FF24H)
SIK20: K20 port interrupt selection register (FF28H•D0)

Selects the ports to be used for the K00–K03, K10–K13 and K20 input interrupts.

When "1" is written: Enable
When "0" is written: Disable
Reading: Valid

Enables the interrupt for the input ports (K00–K03, K10–K13, K20) for which "1" has been written into the interrupt selection registers (SIK00–SIK03, SIK10–SIK13, SIK20). The input port set for "0" does not affect the interrupt generation condition.
At initial reset, these registers are set to "0".

KCP00–KCP03: K0 port input comparison register (FF22H)
KCP10–KCP13: K1 port input comparison register (FF26H)
KCP20: K20 port input comparison register (FF2AH•D0)

Interrupt conditions for terminals K00–K03, K10–K13 and K20 can be set with these registers.

When "1" is written: Falling edge
When "0" is written: Rising edge
Reading: Valid

The interrupt conditions can be set for the rising or falling edge of input for each of the nine bits (K00–K03, K10–K13, K20), through the input comparison registers (KCP00–KCP03, KCP10–KCP13, KCP20). For KCP00–KCP03, a comparison is done only with the ports that are enabled by the interrupt among K00–K03 by means of the SIK00–SIK03 registers. For KCP10–KCP13, a comparison is done only with the ports that are enabled by the interrupt among K10–K13 by means of the SIK10–SIK13 registers. For KCP20, a comparison is done only when the K20 port has been enabled by means of the SIK20 register.
At initial reset, these registers are set to "1".

EIK0: K0 input interrupt mask register (FFE4H•D0)
EIK1: K1 input interrupt mask register (FFE5H•D0)
EIK2: K20 input interrupt mask register (FFE5H•D1)

Masking the interrupt of the input port can be selected with these registers.

When "1" is written: Enable
When "0" is written: Mask
Reading: Valid

With these registers, masking of the input port interrupt can be selected for each of the three systems (K00–K03, K10–K13, K20).
At initial reset, these registers are set to "0".

IK0: K0 input interrupt factor flag (FFF4H•D0)
IK1: K1 input interrupt factor flag (FFF5H•D0)
IK2: K20 input interrupt factor flag (FFF5H•D1)

These flags indicate the occurrence of input interrupt.

When "1" is read: Interrupt has occurred
When "0" is read: Interrupt has not occurred

When "1" is written: Flag is reset
When "0" is written: Invalid

The interrupt factor flags IK0, IK1 and IK2 are associated with K00–K03, K10–K13 and K20, respectively. From the status of these flags, the software can decide whether an input interrupt has occurred.
The interrupt factor flag is set to "1" when the interrupt condition is established regardless of the interrupt mask register setting. However, the interrupt does not occur to the CPU when the interrupt is masked.
These flags are reset to "0" by writing "1" to them.
After an interrupt occurs, the same interrupt will occur again if the interrupt enabled state (I flag = "1") is set or the RETI instruction is executed unless the interrupt factor flag is reset. Therefore, be sure to reset (write "1" to) the interrupt factor flag in the interrupt service routine before shifting to the interrupt enabled state.
At initial reset, these flags are set to "0".

SENON: K20 port key sense ON/OFF control (FF2BH•D0)

Controls the key sense function.

When "1" is written: On
When "0" is written: Off
Reading: Valid

When using K20 as a general purpose input port, fix this register at "1" (On).
When K20 is used for the key sense function, set SENON on during the key sense stage. If any key is pressed (see Figure 4.4.4.1), the K20 port generates an interrupt to the CPU. Then set SENON to off (K20 port key sense OFF), turn the outside N-P-N transistor on using an output port and start the A/D converter. The A/D converter converts the input voltage that varies according to the pressed key into a digital value. The software can discriminates which key was pressed from the conversion result. After that, turn SENON off to reduce current consumption.

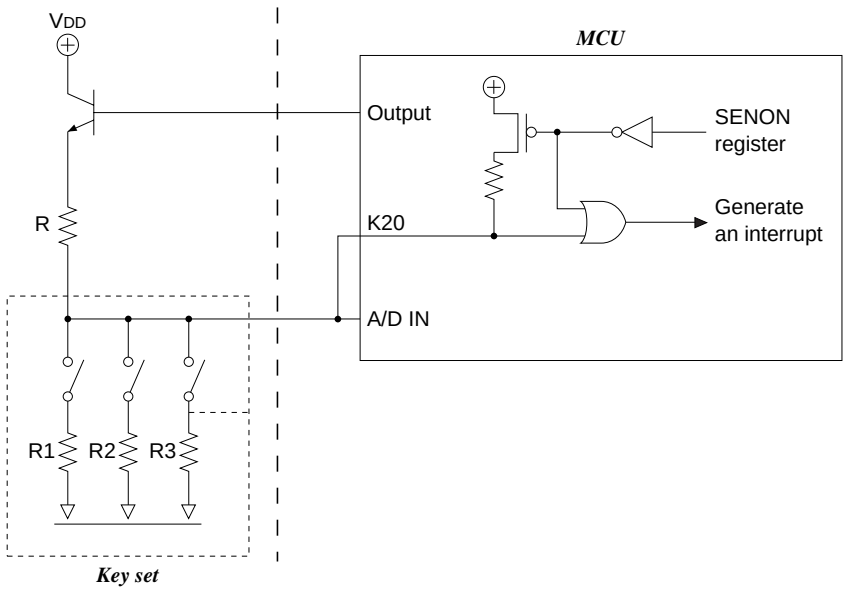


Fig. 4.4.4.1 Key position sensing circuit

This chart is an example of the circuit that discriminates the pressed key with only two wires connected between the MCU chip and the key set. It is useful to reduce the connection wires when the key set location is far from the MCU chip.

Operation: The keys are connected to the ground via a resistor that is different from other keys. So each key will generate a different voltage for inputting to the A/D converter.
Pressing a key generates an interrupt to the MCU. The interrupt turns the transistor on using the output port and starts A/D conversion. The MCU can discriminate the pressed key using the digital value converted by the A/D converter.

4.4.5 Programming notes

(1) When input ports are changed from low to high by pull-up resistors, the rise of the waveform is delayed on account of the time constant of the pull-up resistor and input gate capacitance. Hence, when fetching input ports, set an appropriate waiting time.
Particular care needs to be taken of the key scan during key matrix configuration.
Make this waiting time the amount of time or more calculated by the following expression.
$10 \times C \times R$
C: terminal capacitance 5 pF + parasitic capacitance ? pF
R: pull-up resistance 300 kΩ

(2) The K13 terminal functions as the clock input terminal for the programmable timer, and the input signal is shared with the input port and the programmable timer. Therefore, when the K13 terminal is set to the clock input terminal for the programmable timer, take care of the interrupt setting.

(3) After an interrupt occurs, the same interrupt will occur again if the interrupt enabled state (I flag = "1") is set or the RETI instruction is executed unless the interrupt factor flag is reset. Therefore, be sure to reset (write "1" to) the interrupt factor flag in the interrupt service routine before shifting to the interrupt enabled state.

4.5 Output Ports (R00–R03, R10–R13 and R20–R23)

4.5.1 Configuration of output ports

The E0C63P366 has 12 bits of general output ports.
Output specifications of the output ports are fixed at complementary output.
Figure 4.5.1.1 shows the configuration of the output port.

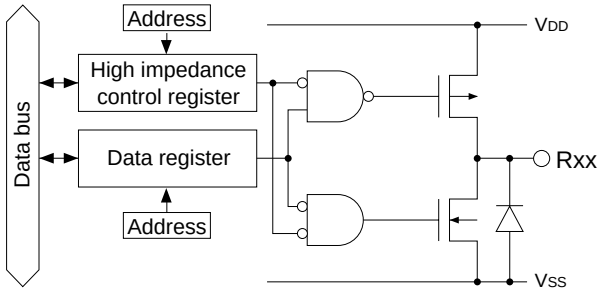


Fig. 4.5.1.1 Configuration of output port

The R02 and R03 output terminals are shared with special output terminals (TOUT, FOUT), and this function is selected by the software.
At initial reset, these are all set to the general purpose output port.
Table 4.5.1.1 shows the setting of the output terminals by function selection.

Table 4.5.1.1 Function setting of output terminals

Terminal name	Terminal status at initial reset	Special output	
		TOUT	FOUT
R00	R00 (High output)	R00	R00
R01	R01 (High output)	R01	R01
R02	R02 (High output)	TOUT	
R03	R03 (High output)		FOUT
R10–R13	R10–R13 (High output)	R10–R13	R10–R13
R20–R23	R20–R23 (High output)	R20–R23	R20–R23

When using the output port (R02, R03) as the special output port, the data register must be fixed at "1" and the high impedance control register must be fixd at "0" (data output).

4.5.2 Mask option

In the E0C63P366, output specifications of all the output ports are fixed at complementary output.

4.5.3 High impedance control

The terminal output status of the output ports can be set to a high impedance status. This control is done using the high impedance control registers.
The high impedance control registers are provided to correspond with the output ports as shown below.

High impedance control register	Corresponding output port
R00HIZ	R00 (1-bit)
R01HIZ	R01 (1-bit)
R02HIZ	R02 (1-bit)
R03HIZ	R03 (1-bit)
R1HIZ	R10–R13 (4-bit)
R2HIZ	R20–R23 (4-bit)

When "1" is written to the high impedance control register, the corresponding output port terminal goes into high impedance status. When "0" is written, the port outputs a signal according to the data register.

4.5.4 Special output

In addition to the regular DC output, special output can be selected for the output ports R02 and R03 as shown in Table 4.5.4.1 with the software.
Figure 4.5.4.1 shows the configuration of the R02 and R03 output ports.

Table 4.5.4.1 Special output

Terminal	Special output	Output control register
R03	FOUT	FOUTE
R02	TOUT	PTOUT

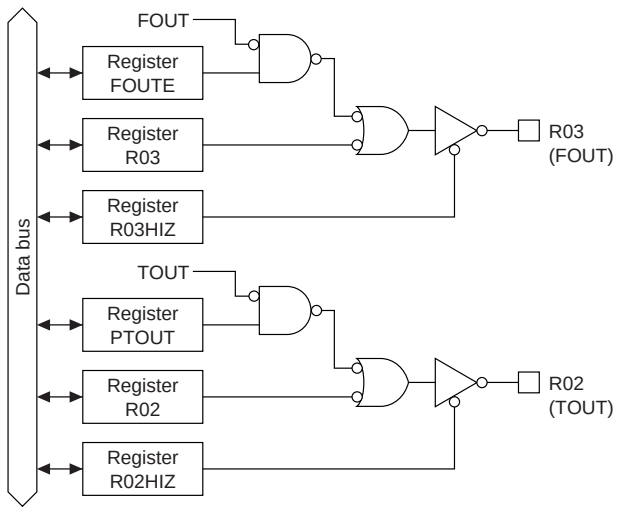


Fig. 4.5.4.1 Configuration of R02 and R03 output ports

At initial reset, the output port data register is set to "1" and the high impedance control register is set to "0". Consequently, the output terminal goes high (V_{DD}).
When using the output port (R02, R03) as the special output port, fix the data register (R02, R03) at "1" and the high impedance control register (R02HIZ, R03HIZ) at "0" (data output). The respective signal should be turned ON and OFF using the special output control register.

Note:
- *Be aware that the output terminal is fixed at a low (Vss) level the same as the DC output if "0" is written to the R02 and R03 registers when the special output has been selected.*
- *Be aware that the output terminal shifts into high impedance status when "1" is written to the high impedance control register (R02HIZ, R03HIZ).*

- **TOUT (R02)**

  The R02 terminal can output a TOUT signal.
  The TOUT signal is the clock that is output from the programmable timer, and can be used to provide a clock signal to an external device.
  To output the TOUT signal, fix the R02 register at "1" and the R02HIZ register at "0", and turn the signal ON and OFF using the PTOUT register. It is, however, necessary to control the programmable timer.
  Refer to Section 4.9, "Programmable Timer" for details of the programmable timer.

Note: A hazard may occur when the TOUT signal is turned ON and OFF.

Figure 4.5.4.2 shows the output waveform of the TOUT signal.

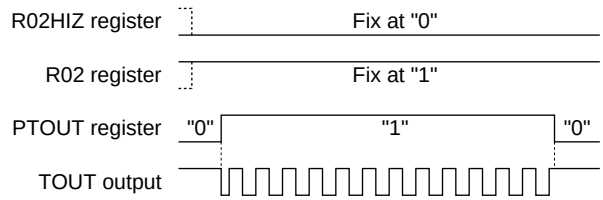


Fig. 4.5.4.2 Output waveform of TOUT signal

- **FOUT (R03)**

  The R03 terminal can output a FOUT signal.
  The FOUT signal is a clock (f_{OSC1} or f_{OSC3}) that is output from the oscillation circuit or a clock that the f_{OSC1} clock has divided in the internal circuit, and can be used to provide a clock signal to an external device.
  To output the FOUT signal, fix the R03 register at "1" and the R03HIZ register at "0", and turn the signal ON and OFF using the FOUTE register.
  The frequency of the output clock may be selected from among 4 types shown in Table 4.5.4.2 by setting the FOFQ0 and FOFQ1 registers.

Table 4.5.4.2 FOUT clock frequency

FOFQ1	FOFQ0	Clock frequency
1	1	f_{OSC3}
1	0	f_{OSC1}
0	1	$f_{OSC1} \times 1/8$
0	0	$f_{OSC1} \times 1/64$

f_{OSC1}: Clock that is output from the OSC1 oscillation circuit
f_{OSC3}: Clock that is output from the OSC3 oscillation circuit

When f_{OSC3} is selected for the FOUT signal frequency, it is necessary to control the OSC3 oscillation circuit before output.
Refer to Section 4.3, "Oscillation Circuit", for the control and notes.

Note: A hazard may occur when the FOUT signal is turned ON and OFF.

Figure 4.5.4.3 shows the output waveform of the FOUT signal.

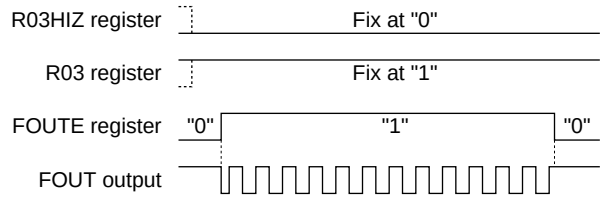


Fig. 4.5.4.3 Output waveform of FOUT signal

4.5.5 I/O memory of output ports

Table 4.5.5.1 shows the I/O addresses and control bits for the output ports.

Table 4.5.5.1 Control bits of output ports

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
FF06H	FOUTE	0	FOFQ1	FOFQ0	FOUTE	0	Enable	Disable	FOUT output enable
					0 *3	– *2			Unused
	R/W	R	R/W		FOFQ1	0			FOUT frequency selection [FOFQ1, 0] 0 1 2 3 / Frequency fOSC1/64 fOSC1/8 fOSC1 fOSC3
					FOFQ0	0			
FF30H	R03HIZ	R02HIZ	R01HIZ	R00HIZ	R03HIZ	0	High-Z	Output	R03 output high impedance control (FOUTE=0) FOUT output high impedance control (FOUTE=1)
					R02HIZ	0	High-Z	Output	R02 output high impedance control (PTOUT=0) TOUT output high impedance control (PTOUT=1)
	R/W				R01HIZ	0	High-Z	Output	R01 output high impedance control
					R00HIZ	0	High-Z	Output	R00 output high impedance control
FF31H	R03	R02	R01	R00	R03	1	High	Low	R03 output port data (FOUTE=0) Fix at "1" when FOUT is used
					R02	1	High	Low	R02 output port data (PTOUT=0) Fix at "1" when TOUT is used
	R/W				R01	1	High	Low	R01 output port data
					R00	1	High	Low	R00 output port data
FF32H	0	0	0	R1HIZ	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R			R/W	0 *3	– *2			Unused
					R1HIZ	0	High-Z	Output	R1 output high impedance control
FF33H	R13	R12	R11	R10	R13	1	High	Low	R10–R13 output port data
					R12	1	High	Low	
	R/W				R11	1	High	Low	
					R10	1	High	Low	
FF34H	0	0	0	R2HIZ	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R			R/W	0 *3	– *2			Unused
					R2HIZ	0	High-Z	Output	R2 output high impedance control
FF35H	R23	R22	R21	R20	R23	1	High	Low	R20–R23 output port data
					R22	1	High	Low	
	R/W				R21	1	High	Low	
					R20	1	High	Low	
FFC1H	CHSEL	PTOUT	CKSEL1	CKSEL0	CHSEL	0	Timer1	Timer0	TOUT output channel selection
					PTOUT	0	On	Off	TOUT output control
	R/W				CKSEL1	0	OSC3	OSC1	Prescaler 1 source clock selection
					CKSEL0	0	OSC3	OSC1	Prescaler 0 source clock selection

*1 Initial value at initial reset

*2 Not set in the circuit

*3 Constantly "0" when being read

R00HIZ–R03HIZ: R0 port high impedance control register (FF30H)
R1HIZ: R1 port high impedance control register (FF32H•D0)
R2HIZ: R2 port high impedance control register (FF34H•D0)

Controls high impedance output of the output port.

When "1" is written: High impedance
When "0" is written: Data output
Reading: Valid

By writing "0" to the high impedance control register, the corresponding output terminal outputs according to the data register. When "1" is written, it shifts into high impedance status.
When the output ports R02 and R03 are used for special output (TOUT, FOUT), fix the R02HIZ register and the R03HIZ register at "0" (data output).
At initial reset, these registers are set to "0".

R00–R03: R0 output port data register (FF31H)
R10–R13: R1 output port data register (FF33H)
R20–R23: R2 output port data register (FF35H)
Set the output data for the output ports.

When "1" is written: High level output
When "0" is written: Low level output
Reading: Valid

The output port terminals output the data written in the corresponding data registers without changing it. When "1" is written to the register, the output port terminal goes high (V_{DD}), and when "0" is written, the output port terminal goes low (V_{SS}).
When the output ports R02 and R03 are used for special output (TOUT, FOUT), fix the R02 register and the R03 register at "1".
At initial reset, these registers are all set to "1".

FOUTE: FOUT output control register (FF06H•D3)
Controls the FOUT output.

When "1" is written: FOUT output ON
When "0" is written: FOUT output OFF
Reading: Valid

By writing "1" to the FOUTE register when the R03 register has been set to "1" and the R03HIZ register has been set to "0", an FOUT signal is output from the R03 terminal. When "0" is written, the R03 terminal goes high (V_{DD}).
When using the R03 output port for DC output, fix this register at "0".
At initial reset, this register is set to "0".

FOFQ0, FOFQ1: FOUT frequency selection register (FF06H•D0, D1)
Selects a frequency of the FOUT signal.

Table 4.5.5.2 FOUT clock frequency

FOFQ1	FOFQ0	Clock frequency
1	1	f_{OSC3}
1	0	f_{OSC1}
0	1	$f_{OSC1} \times 1/8$
0	0	$f_{OSC1} \times 1/64$

At initial reset, this register is set to "0".

PTOUT: TOUT output control register (FFC1H•D2)
Controls the TOUT output.

When "1" is written: TOUT output ON
When "0" is written: TOUT output OFF
Reading: Valid

By writing "1" to the PTOUT register when the R02 register has been set to "1" and the R02HIZ register has been set to "0", the TOUT signal is output from the R02 terminal. When "0" is written, the R02 terminal goes high (V_{DD}).
When using the R02 output port for DC output, fix this register at "0".
At initial reset, this register is set to "0".

4.5.6 Programming notes

(1) When using the output port (R02, R03) as the special output port, fix the data register (R02, R03) at "1" and the high impedance control register (R02HIZ, R03HIZ) at "0" (data output).
Be aware that the output terminal is fixed at a low (V_{SS}) level the same as the DC output if "0" is written to the R02 and R03 registers when the special output has been selected.
Be aware that the output terminal shifts into high impedance status when "1" is written to the high impedance control register (R02HIZ, R03HIZ).

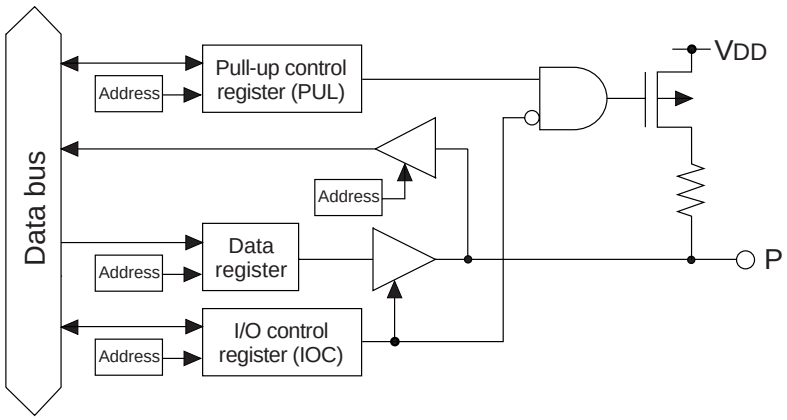
(2) A hazard may occur when the FOUT signal and the TOUT signal are turned ON and OFF.

(3) When f_{OSC3} is selected for the FOUT signal frequency, it is necessary to control the OSC3 oscillation circuit before output.
Refer to Section 4.3, "Oscillation Circuit", for the control and notes.

4.6 I/O Ports (P00–P03, P10–P13, P20–P23, P30–P33 and P40–P43)

4.6.1 Configuration of I/O ports

The E0C63P366 has 20 bits general-purpose I/O ports. Figure 4.6.1.1 shows the configuration of the I/O port. The output specification during output mode is fixed at complementary output and the P10–P13, P20–P23 and P30–P33 ports have built-in pull-up resistors.



∗ P40–P43 ports do not have a pull-up resistor

Fig. 4.6.1.1 Configuration of I/O port

The P10–P13 I/O port terminals are shared with the serial interface input/output terminals and this function is selected by the software. The P40–P43 I/O port terminals are shared with the A/D converter input terminals and this function is also selected by the software.
At initial reset, these are all set to the I/O port.
Table 4.6.1.1 shows the setting of the input/output terminals by function selection.

Table 4.6.1.1 Function setting of input/output terminals

Terminal name	Terminal status at initial reset	Serial I/F		A/D converter
		Master	Slave	
P00–P03	P00–P03 (Input & pull-up)	P00–P03	P00–P03	P00–P03
P10	P10 (Input & pull-up)	SIN(I)	SIN(I)	
P11	P11 (Input & pull-up)	SOUT(O)	SOUT(O)	
P12	P12 (Input & pull-up)	$\overline{\text{SCLK}}$(O)	$\overline{\text{SCLK}}$(I)	
P13	P13 (Input & pull-up)	P13	$\overline{\text{SRDY}}$(O)	
P20–P23	P20–P23 (Input & pull-up)	P20–P23	P20–P23	P20–P23
P30–P33	P30–P33 (Input & pull-up)	P30–P33	P30–P33	P30–P33
P40	P40 (Input & high impedance)			AD0(I)
P41	P41 (Input & high impedance)			AD1(I)
P42	P42 (Input & high impedance)			AD2(I)
P43	P43 (Input & high impedance)			AD3(I)

When these ports are used as I/O ports, the ports can be set to either input mode or output mode (in 1-bit unit). Modes can be set by writing data to the I/O control registers.
Refer to Section 4.10, "Serial Interface", for control of the serial interface.
Refer to Section 4.11, "A/D Converter", for control of the A/D converter.

4.6.2 Mask option

In the E0C63P366, the output specification of all the I/O ports is fixed at "complementary output", and the pull-up option for the P10–P13, P20–P23 and P30–P33 ports is fixed at "with pull-up resistor".

4.6.3 I/O control registers and input/output mode

Input or output mode can be set for the I/O ports by writing data into the corresponding I/O control registers IOCxx.

To set the input mode, write "0" to the I/O control register. When an I/O port is set to input mode, it becomes high impedance status and works as an input port.
However, when the pull-up explained in the following section has been set by software, the input line is pulled up only during this input mode (except for P40–P43).

To set the output mode, write "1" is to the I/O control register. When an I/O port is set to output mode , it works as an output port, it outputs a high level (V_{DD}) when the port output data is "1", and a low level (V_{SS}) when the port output data is "0".

If perform the read out in each mode; when output mode, the register value is read out, and when input mode, the port value is read out.

At initial reset, the I/O control registers are set to "0", and the I/O ports enter the input mode.

The I/O control registers of the ports that are set as input/output for the serial interface and A/D converter can be used as general purpose registers that do not affect the I/O control. (See Table 4.6.1.1.)

4.6.4 Pull-up during input mode

A pull-up resistor that operates during the input mode is built into the I/O ports P10–P13, P20–P23 and P30–P33 of the E0C63P366.
The pull-up resistor becomes effective by writing "1" to the pull-up control register PULxx that corresponds to each port, and the input line is pulled up during the input mode. When "0" has been written, no pull-up is done.
At initial reset, the pull-up control registers are set to "1".
The pull-up control registers of the ports, that are set as input/output for the serial interface, can be used as general purpose registers that do not affect the pull-up control. (See Table 4.6.1.1.)
The pull-up control registers of the port, that are set as input for the serial interface, function the same as the I/O port.

4.6.5 I/O memory of I/O ports

Tables 4.6.5.1(a) and (b) show the I/O addresses and the control bits for the I/O ports.

Table 4.6.5.1(a) Control bits of I/O ports (1)

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
FF40H	IOC03	IOC02	IOC01	IOC00	IOC03	0	Output	Input	P00–P03 I/O control register
					IOC02	0	Output	Input	
	R/W				IOC01	0	Output	Input	
					IOC00	0	Output	Input	
FF41H	PUL03	PUL02	PUL01	PUL00	PUL03	1	On	Off	P00–P03 pull-up control register
					PUL02	1	On	Off	
	R/W				PUL01	1	On	Off	
					PUL00	1	On	Off	
FF42H	P03	P02	P01	P00	P03	– *2	High	Low	P00–P03 I/O port data
					P02	– *2	High	Low	
	R/W				P01	– *2	High	Low	
					P00	– *2	High	Low	
FF44H	IOC13	IOC12	IOC11	IOC10	IOC13	0	Output	Input	P13 I/O control register functions as a general-purpose register when SIF (slave) is selected
					IOC12	0	Output	Input	P12 I/O control register (ESIF=0) functions as a general-purpose register when SIF is selected
	R/W				IOC11	0	Output	Input	P11 I/O control register (ESIF=0) functions as a general-purpose register when SIF is selected
					IOC10	0	Output	Input	P10 I/O control register (ESIF=0) functions as a general-purpose register when SIF is selected
FF45H	PUL13	PUL12	PUL11	PUL10	PUL13	1	On	Off	P13 pull-up control register functions as a general-purpose register when SIF (slave) is selected
					PUL12	1	On	Off	P12 pull-up control register (ESIF=0) functions as a general-purpose register when SIF (master) is selected $\overline{SCLK}$ (I) pull-up control register when SIF (slave) is selected
	R/W				PUL11	1	On	Off	P11 pull-up control register (ESIF=0) functions as a general-purpose register when SIF is selected
					PUL10	1	On	Off	P10 pull-up control register (ESIF=0) SIN pull-up control register when SIF is selected
FF46H	P13	P12	P11	P10	P13	– *2	High	Low	P13 I/O port data functions as a general-purpose register when SIF (slave) is selected
					P12	– *2	High	Low	P12 I/O port data (ESIF=0) functions as a general-purpose register when SIF is selected
	R/W				P11	– *2	High	Low	P11 I/O port data (ESIF=0) functions as a general-purpose register when SIF is selected
					P10	– *2	High	Low	P10 I/O port data (ESIF=0) functions as a general-purpose register when SIF is selected
FF48H	IOC23	IOC22	IOC21	IOC20	IOC23	0	Output	Input	P20–P23 I/O control register
					IOC22	0	Output	Input	
	R/W				IOC21	0	Output	Input	
					IOC20	0	Output	Input	
FF49H	PUL23	PUL22	PUL21	PUL20	PUL23	1	On	Off	P20–P23 pull-up control register
					PUL22	1	On	Off	
	R/W				PUL21	1	On	Off	
					PUL20	1	On	Off	
FF4AH	P23	P22	P21	P20	P23	– *2	High	Low	P20–P23 I/O port data
					P22	– *2	High	Low	
					P21	– *2	High	Low	
					P20	– *2	High	Low	
FF4CH	IOC33	IOC32	IOC31	IOC30	IOC33	0	Output	Input	P30–P33 I/O control register
					IOC32	0	Output	Input	
	R/W				IOC31	0	Output	Input	
					IOC30	0	Output	Input	

*1 Initial value at initial reset

*2 Not set in the circuit

*3 Constantly "0" when being read

Table 4.6.5.1(b) Control bits of I/O ports (2)

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
FF4DH	PUL33	PUL32	PUL31	PUL30	PUL33	1	On	Off	P30–P33 pull-up control register
					PUL32	1	On	Off	
	R/W				PUL31	1	On	Off	
					PUL30	1	On	Off	
FF4EH	P33	P32	P31	P30	P33	– *2	High	Low	P30–P33 I/O port data
					P32	– *2	High	Low	
	R/W				P31	– *2	High	Low	
					P30	– *2	High	Low	
FF50H	IOC43	IOC42	IOC41	IOC40	IOC43	0	Output	Input	P43 I/O control register (PAD3=0) functions as a general-purpose register when A/D is enabled
					IOC42	0	Output	Input	P42 I/O control register (PAD2=0) functions as a general-purpose register when A/D is enabled
	R/W				IOC41	0	Output	Input	P41 I/O control register (PAD1=0) functions as a general-purpose register when A/D is enabled
					IOC40	0	Output	Input	P40 I/O control register (PAD0=0) functions as a general-purpose register when A/D is enabled
FF52H	P43	P42	P41	P40	P43	– *2	High	Low	P43 I/O port data (PAD3=0) functions as a general-purpose register when A/D is enabled
					P42	– *2	High	Low	P42 I/O port data (PAD2=0) functions as a general-purpose register when A/D is enabled
	R/W				P41	– *2	High	Low	P41 I/O port data (PAD1=0) functions as a general-purpose register when A/D is enabled
					P40	– *2	High	Low	P40 I/O port data (PAD0=0) functions as a general-purpose register when A/D is enabled
FF70H	0	ESOUT	SCTRG	ESIF	0 *3	– *2			Unused
					ESOUT	0	Enable	Disable	SOUT enable/disable control
	R	R/W			SCTRG	0	Trigger	Invalid	Serial I/F clock trigger (writing)
							Run	Stop	Serial I/F clock status (reading)
					ESIF	0	SIF	I/O	Serial I/F enable (P1 port function selection)
FFD1H	PAD3	PAD2	PAD1	PAD0	PAD3	0	Enable	Disable	P43 input channel enable/disable control
					PAD2	0	Enable	Disable	P42 input channel enable/disable control
	R/W				PAD1	0	Enable	Disable	P41 input channel enable/disable control
					PAD0	0	Enable	Disable	P40 input channel enable/disable control

*1 Initial value at initial reset

*2 Not set in the circuit

*3 Constantly "0" when being read

ESIF: Serial interface enable register (FF70H•D0)

Selects function for P10–P13.

When "1" is written: Serial interface input/output port
When "0" is written: I/O port
Reading: Valid

When using the serial interface, write "1" to this register and when P10–P13 are used as the I/O port, write "0". The configuration of the terminals within P10–P13 that are used for the serial interface is decided by the mode selected with the SCS1 and SCS0 registers (see Section 4.10).
In the slave mode, all the P10–P13 ports are set to the serial interface input/output port. In the master mode, P10–P12 are set to the serial interface input/output port and P13 can be used as the I/O port.
At initial reset, this register is set to "0".

PAD0–PAD3: A/D input channel enable/disable control register (FFD1H)

Selects function for P40–P43.

When "1" is written: A/D converter input
When "0" is written: I/O port
Reading: Valid

When using the A/D converter, write "1" to the register. PAD0–PAD3 correspond to P40–P43, respectively. When using a port from P40 to P43 as an I/O port, write "0" to the corresponding PAD register.
At initial reset, this register is set to "0".

P00–P03: P0 I/O port data register (FF42H)
P10–P13: P1 I/O port data register (FF46H)
P20–P23: P2 I/O port data register (FF4AH)
P30–P33: P3 I/O port data register (FF4EH)
P40–P43: P4 I/O port data register (FF52H)

I/O port data can be read and output data can be set through these registers.

• ***When writing data***

When "1" is written: High level
When "0" is written: Low level

When an I/O port is set to the output mode, the written data is output unchanged from the I/O port terminal. When "1" is written as the port data, the port terminal goes high (V_{DD}), and when "0" is written, the terminal goes low (V_{SS}).
Port data can be written also in the input mode.

• ***When reading data***

When "1" is read: High level
When "0" is read: Low level

The terminal voltage level of the I/O port is read out. When the I/O port is in the input mode the voltage level being input to the port terminal can be read out; in the output mode the register value can be read. When the terminal voltage is high (V_{DD}) the port data that can be read is "1", and when the terminal voltage is low (V_{SS}) the data is "0".
When the PUL register is set to "1", the built-in pull-up resister goes ON during input mode, so that the I/O port terminal is pulled up (except for P40–P43).

The data registers of the ports that are set as input/output for the serial interface or A/D converter can be used as general purpose registers that do not affect the input/output.

Note: When in the input mode, I/O ports are changed from low to high by pull-up resistor, the rise of the waveform is delayed on account of the time constant of the pull-up resistor and input gate capacitance. Hence, when fetching input ports, set an appropriate wait time.
Particular care needs to be taken of the key scan during key matrix configuration.
Make this waiting time the amount of time or more calculated by the following expression.
$10 \times C \times R$
C: terminal capacitance 5 pF + parasitic capacitance ? pF
R: pull-up resistance 300 kΩ

IOC00–IOC03: P0 port I/O control register (FF40H)
IOC10–IOC13: P1 port I/O control register (FF44H)
IOC20–IOC23: P2 port I/O control register (FF48H)
IOC30–IOC33: P3 port I/O control register (FF4CH)
IOC40–IOC43: P4 port I/O control register (FF50H)
The input and output modes of the I/O ports are set with these registers.

When "1" is written: Output mode
When "0" is written: Input mode
Reading: Valid

The input and output modes of the I/O ports are set in 1-bit unit.
Writing "1" to the I/O control register makes the corresponding I/O port enter the output mode, and writing "0" induces the input mode.
At initial reset, these registers are all set to "0", so the I/O ports are in the input mode.
The I/O control registers of the ports that are set as input/output for the serial interface or A/D converter can be used as general purpose registers that do not affect the input/output.

PUL00–PUL03: P0 port pull-up control register (FF41H)
PUL10–PUL13: P1 port pull-up control register (FF45H)
PUL20–PUL23: P2 port pull-up control register (FF49H)
PUL30–PUL33: P3 port pull-up control register (FF4DH)
The pull-up during the input mode are set with these registers.

When "1" is written: Pull-up ON
When "0" is written: Pull-up OFF
Reading: Valid

The built-in pull-up resistor which is turned ON during input mode is set to enable in 1-bit units. (The pull-up resistor isavailable for the P10–P13, P20–P23, P30–P33 ports.)
By writing "1" to the pull-up control register, the corresponding I/O ports are pulled up (during input mode), while writing "0" turns the pull-up function OFF.
At initial reset, these registers are all set to "1", so the pull-up function is set to ON.

The registers of the ports that are set as input/output for the serial interface or A/D converter can be used as general purpose registers that do not affect the pull-up control.
The pull-up control registers of the port that are set as input for the serial interface function the same as the I/O port.

4.6.6 Programming note

When in the input mode, I/O ports are changed from low to high by pull-up resistor, the rise of the waveform is delayed on account of the time constant of the pull-up resistor and input gate capacitance. Hence, when fetching input ports, set an appropriate wait time.
Particular care needs to be taken of the key scan during key matrix configuration.
Make this waiting time the amount of time or more calculated by the following expression.
$10 \times C \times R$

C: terminal capacitance 5 pF + parasitic capacitance ? pF
R: pull-up resistance 300 kΩ

4.7 LCD Driver (COM0–COM3, SEG0–SEG31)

4.7.1 Configuration of LCD driver

The E0C63P366 has 4 common terminals (COM0–COM3) and 32 segment terminals (SEG0–SEG31), so that it can drive an LCD with a maximum of 128 (32 × 4) segments.
The driving method is 1/4 duty, 1/3 duty or 1/2 duty dynamic drive with four voltages (1/3 bias), V_{SS}, V_{C1}, V_{C2} and V_{C3}. It is also possible to set static drive. The drive duty and static drive can be selected by software.

4.7.2 Power supply for LCD driving

V_{C1}–V_{C3} are the LCD drive voltages generated by the LCD system voltage circuit.
The LCD system voltage circuit generates V_{C2} with the voltage regulator incorporated in itself, and generates two other voltages by boosting or reducing the voltage V_{C2}.
The LCD system voltage circuit that generates V_{C1}–V_{C3} is turned ON and OFF by the LCD power control register LPWR.
By setting LPWR to "1", the LCD system voltage circuit generates V_{C1}–V_{C3}. When LPWR is set to "0", V_{C1}–V_{C3} becomes V_{SS} level. In this case, all outputs from the COM terminals and SEG terminals go to V_{SS} level.
To display the LCD, the LCD drive power must be ON by previously setting LPWR to "1".
Furthermore, SEG output ports that are set for DC output operate same as the output (R) port regardless of the power ON/OFF control.

4.7.3 Control of LCD display and drive waveform

(1) Display ON/OFF control

The E0C63P366 incorporates the ALON and ALOFF registers to blink display. When "1" is written to ALON, all the segments go ON, and when "1" is written to ALOFF, all the segments go OFF. At such a time, an ON waveform or an OFF waveform is output from SEG terminals. When "0" is written to these registers, normal display is performed. Furthermore, when "1" is written to both of the ALON and ALOFF, ALON (all ON) has priority over the ALOFF (all OFF). At initial reset, both the registers are set to "0" (normal display). However, the LCD power is OFF at initial reset, so the display is actually performed when the LCD power is turned ON (LPWR = "1").

(2) Setting of drive duty

In the E0C63P366, the drive duty can be set to 1/4, 1/3 or 1/2 by the software. This setting is done using the LDUTY1 and LDUTY0 registers as shown in Table 4.7.3.1.

Table 4.7.3.1 LCD drive duty setting

LDUTY1	LDUTY0	Drive duty	Common terminal used	Maximum segment number	Frame frequency *
1	*	1/2	COM0, COM1	64 (32 × 2)	32 Hz
0	1	1/3	COM0–COM2	96 (32 × 3)	42.7 Hz
0	0	1/4	COM0–COM3	128 (32 × 4)	32 Hz

* When f_{OSC1} = 32.768 kHz

Figures 4.7.3.1 to 4.7.3.3 show the dynamic drive waveform according to the drive duty.

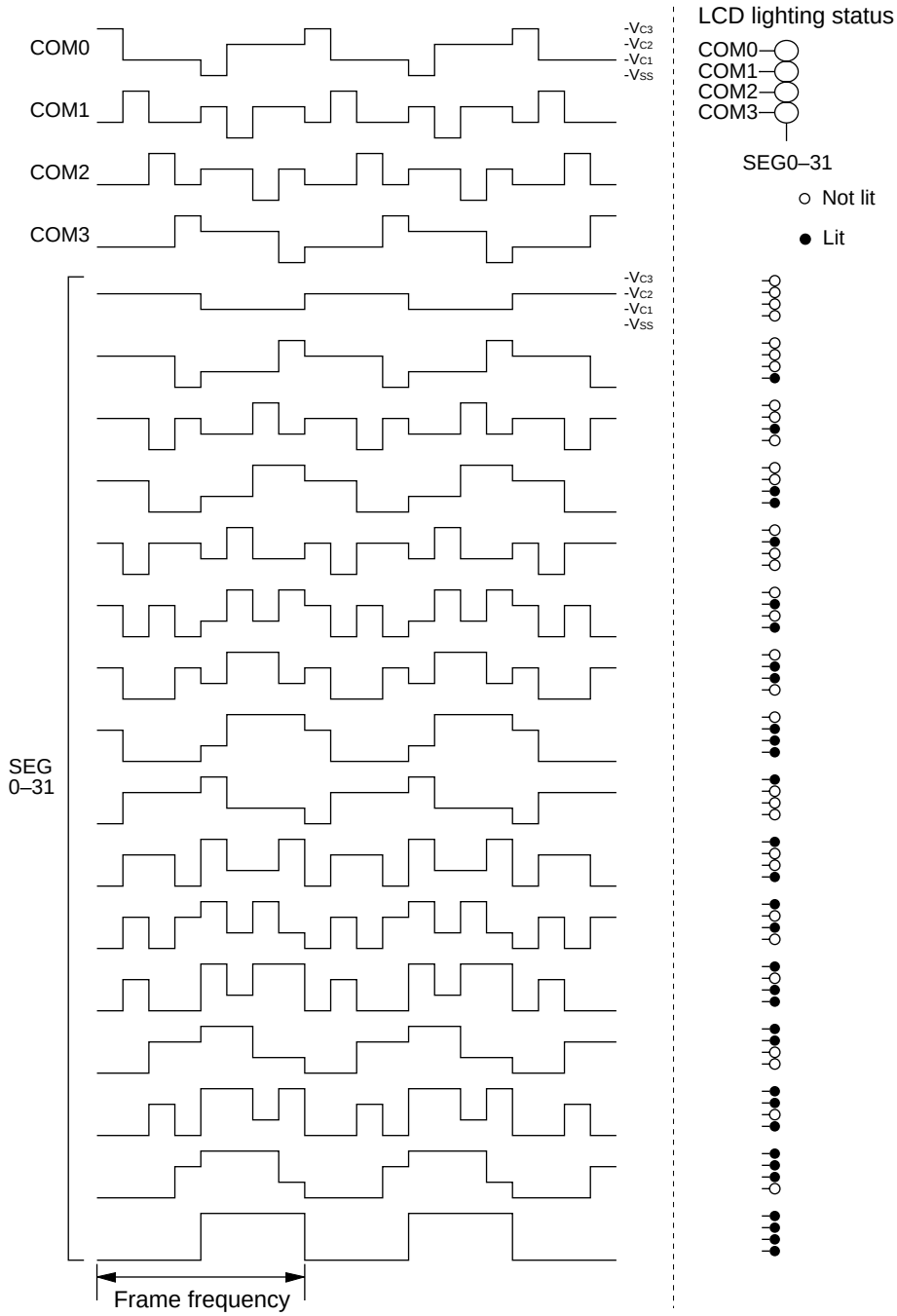


Fig. 4.7.3.1 Dynamic drive waveform for 1/4 duty (1/3 bias)

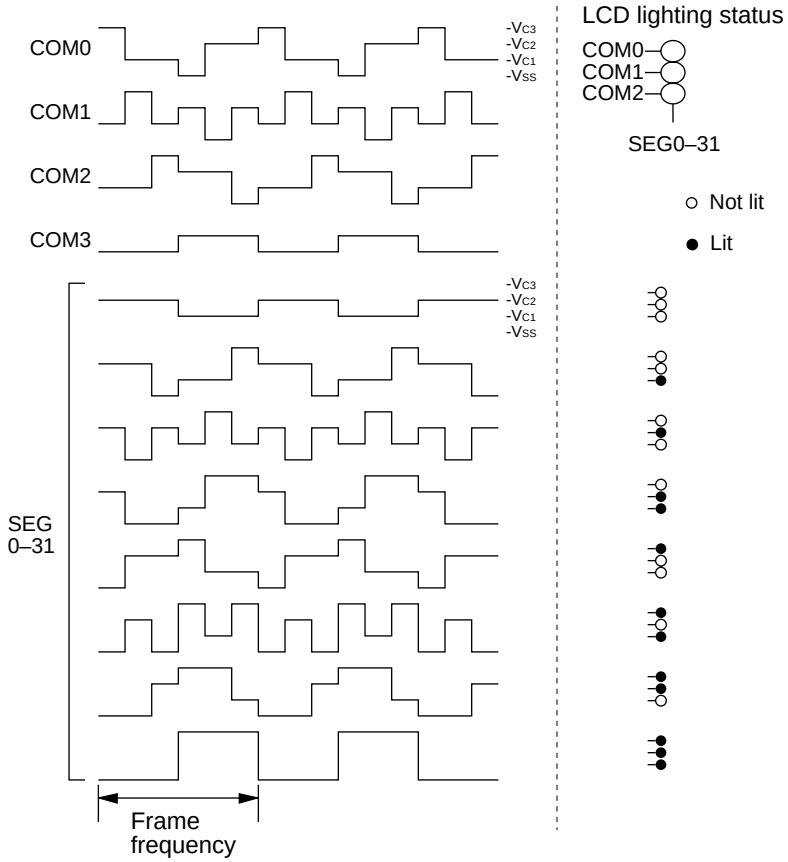


Fig. 4.7.3.2 Dynamic drive waveform for 1/3 duty (1/3 bias)

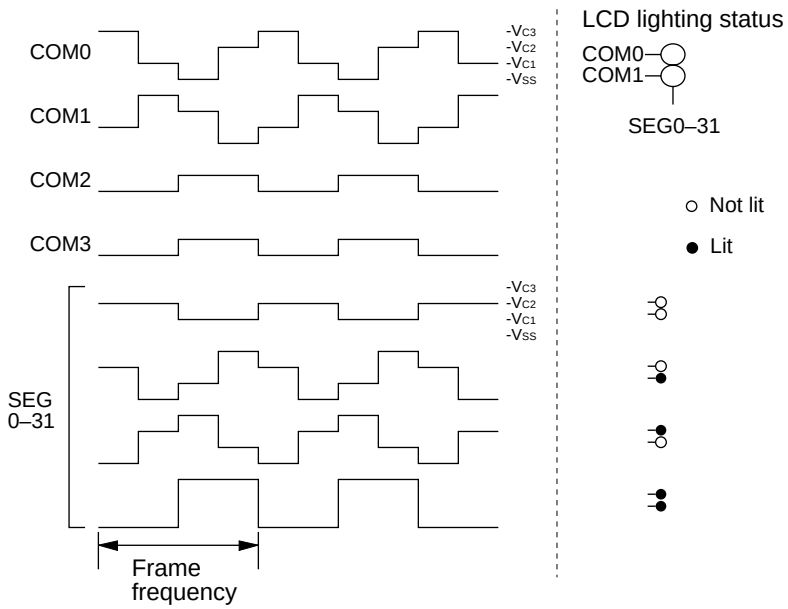


Fig. 4.7.3.3 Dynamic drive waveform for 1/2 duty (1/3 bias)

(3) Static drive

The E0C63P366 provides software setting of the LCD static drive.
To set in static drive, write "1" to the common output signal control register STCD. Then, by writing "1" to any one of COM0 to COM3 (display memory) corresponding to the SEG terminal, the SEG terminal outputs a static ON waveform. When all the COM0 to COM3 bits are set to "0", the SEG terminal outputs a dynamic OFF waveform.
Figure 4.7.3.4 shows the static drive waveform.

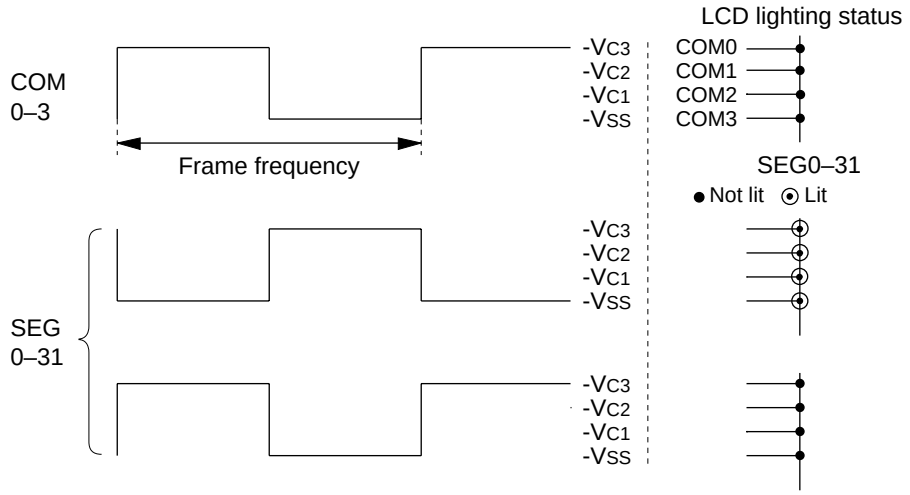


Fig. 4.7.3.4 Static drive waveform (1/3 bias)

4.7.4 Segment option

(1) Segment allocation

Up to 128 bits of the display memory can be selected from the data memory addresses F000H to F01FH.
The LCD driver has a segment decoder built-in, and the data bit (D0–D3) of the optional address in the display memory area (F000H–F01FH) can be allocated to the optional segment. This makes design easy by increasing the degree of freedom with which the liquid crystal panel can be designed.
The allocated segment displays when the bit for the display memory is set to "1", and goes out when bit is set to "0".
Figure 4.7.4.1 shows an example of the relationship between the LCD segments (on the panel) and the display memory for the case of 1/3 duty.

Address	Data			
	D3	D2	D1	D0
F00AH	d	c	b	a
F00BH	p	g	f	e
F00CH	d'	c'	b'	a'
F00DH	p'	g'	f'	e'

Display memory allocation

	Common 0	Common 1	Common 2
SEG10	F00A, D0 (a)	F00B, D1 (f)	F00B, D0 (e)
SEG11	F00A, D1 (b)	F00B, D2 (g)	F00A, D3 (d)
SEG12	F00D, D1 (f')	F00A, D2 (c)	F00B, D3 (p)

Pin address allocation

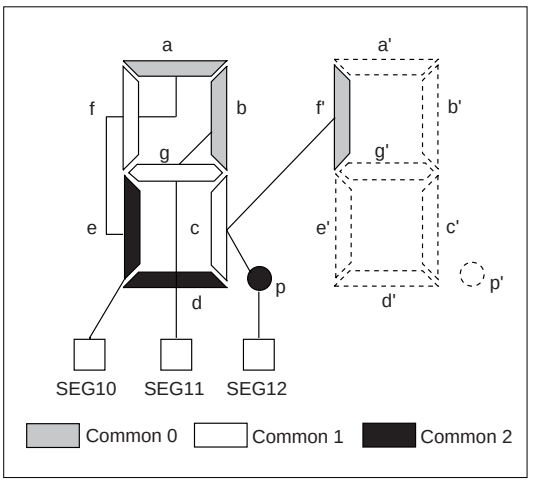


Fig. 4.7.4.1 Segment allocation

At initial reset, the contents of the display memory are undefined, therefore it is necessary to initialize by software. Since the display memory permits reading and writing, the addresses/bits that are not used on the LCD display can be used as general-purpose registers.

(2) Output specification

① The segment terminals (SEG0–SEG31) can be selected in pairs* for either segment signal output or DC output (V_{DD} and V_{SS} binary output).
When DC output is selected, the data corresponding to COM0 of each segment terminal is output.

② When DC output is selected, either complementary output or N-channel open drain output can be selected for each terminal.

* The terminal pairs are combination of SEG2 × n and SEG2 × n + 1 (where n is an integer from 0 to 15).

(3) Segment option

Recommended option data is written to the LCD segment opotion PROM before the IC is shipped. Modifying the LCD segment opotion is done at the user's own risk.
The output specification data for the LCD segment terminals and data for LCD segment assignment to the display memory are generated by converting the segment option document file output from the SOG63358 segment option generator.
By writing the option data to the segment option PROM, the segment terminals are automatically configured with the selected optional specifications.

(4) Recommended segment option data

CP366SEG.SDC (segment option document file)

```
* E0C63P366 SEGMENT OPTION DOCUMENT  V 1.00
*
* FILE NAME    CP366SEG.SDC
* USER'S NAME  EPSON
* INPUT DATE   99/11/10
*
* OPTION NO.12
*
* < LCD SEGMENT DECODE TABLE >
*
* SEG COM0 COM1 COM2 COM3 SPEC
*
    0  000  001  002  003  S
    1  010  011  012  013  S
    2  020  021  022  023  S
    3  030  031  032  033  S
    4  040  041  042  043  S
    5  050  051  052  053  S
    6  060  061  062  063  S
    7  070  071  072  073  S
    8  080  081  082  083  S
    9  090  091  092  093  S
   10  0A0  0A1  0A2  0A3  S
   11  0B0  0B1  0B2  0B3  S
   12  0C0  0C1  0C2  0C3  S
   13  0D0  0D1  0D2  0D3  S
   14  0E0  0E1  0E2  0E3  S
   15  0F0  0F1  0F2  0F3  S
   16  100  101  102  103  S
   17  110  111  112  113  S
   18  120  121  122  123  S
   19  130  131  132  133  S
   20  140  141  142  143  S
   21  150  151  152  153  S
   22  160  161  162  163  S
   23  170  171  172  173  S
   24  180  181  182  183  S
   25  190  191  192  193  S
   26  1A0  1A1  1A2  1A3  S
   27  1B0  1B1  1B2  1B3  S
   28  1C0  1C1  1C2  1C3  S
   29  1D0  1D1  1D2  1D3  S
   30  1E0  1E1  1E2  1E3  S
   31  1F0  1F1  1F2  1F3  S
*EOF
```

4.7.5 Mask option

The E0C63P366 generates the LCD drive voltage using the internal power supply circuit and does not allow use of an external power source.

4.7.6 I/O memory of LCD driver

Table 4.7.6.1 shows the I/O addresses and the control bits for the LCD driver. Figure 4.7.6.1 shows the display memory map.

Table 4.7.6.1 Control bits of LCD driver

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
FF60H	LDUTY1	LDUTY0	VCCHG	LPWR	LDUTY1	0			LCD drive duty switch [LDUTY1, 0]: 0 (Duty 1/4), 1 (1/3), 2, 3 (1/2)
					LDUTY0	0			
	R/W				VCCHG	0			General-purpose register (reserved register)
					LPWR	0	On	Off	LCD power On/Off
FF61H	0	ALOFF	ALON	STCD	0 *3	– *2			Unused
					ALOFF	1	All Off	Normal	LCD all OFF control
	R	R/W			ALON	0	All On	Normal	LCD all ON control
					STCD	0	Static	Dynamic	Common output signal control

*1 Initial value at initial reset

*2 Not set in the circuit

*3 Constantly "0" when being read

Base address \ Low	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
F000	Display memory (32 words × 4 bits) R/W															
F010																

Fig. 4.7.6.1 Display memory map

LPWR: LCD power control (ON/OFF) register (FF60H•D0)

Turns the LCD system voltage circuit ON and OFF.

When "1" is written: ON
When "0" is written: OFF
Reading: Valid

When "1" is written to the LPWR register, the LCD system voltage circuit goes ON and generates the LCD drive voltage. When "0" is written, all the LCD drive voltages go to VSS level.
It takes about 100 msec for the LCD drive voltage to stabilize after starting up the LCD system voltage circuit by writing "1" to the LPWR register.
This control does not affect to SEG terminals that have been set for DC output.
At initial reset, this register is set to "0".

LDUTY0, LDUTY1: LCD drive duty switching register (FF60H•D2, D3)

Selects the LCD drive duty.

Table 4.7.6.2 Drive duty setting

LDUTY1	LDUTY0	Drive duty	Common terminal used	Maximum segment number	Frame frequency *
1	*	1/2	COM0, COM1	64 (32 × 2)	32 Hz
0	1	1/3	COM0–COM2	96 (32 × 3)	42.7 Hz
0	0	1/4	COM0–COM3	128 (32 × 4)	32 Hz

* When f_{OSC1} = 32.768 kHz

At initial reset, this register is set to "0".

STCD: Common output signal control register (FF61H•D0)

Switches the LCD driving method.

When "1" is written: Static drive
When "0" is written: Dynamic drive
Reading: Valid

By writing "1" to STCD, static drive is selected, and dynamic drive is selected when "0" is written.
At initial reset, this register is set to "0".

ALON: LCD all ON control register (FF61H•D1)

Displays the all LCD segments ON.

When "1" is written: All LCD segments displayed
When "0" is written: Normal display
Reading: Valid

By writing "1" to the ALON register, all the LCD segments goes ON, and when "0" is written, it returns to normal display.
This function outputs an ON waveform to the SEG terminals, and segments not affect the content of the display memory.
ALON has priority over ALOFF.
At initial reset, this register is set to "0".

ALOFF: LCD all OFF control register (FF61H•D2)

Fade outs the all LCD segments.

When "1" is written: All LCD segments fade out
When "0" is written: Normal display
Reading: Valid

By writing "1" to the ALOFF register, all the LCD segments goes OFF, and when "0" is written, it returns to normal display.
This function outputs an OFF waveform to the SEG terminals, and does not affect the content of the display memory.
At initial reset, this register is set to "1".

Display memory (F000H–F01FH)

The LCD segments are lit or turned off depending on this data.

When "1" is written: Lit
When "0" is written: Not lit
Reading: Invalid

By writing data into the display memory allocated to the LCD segment (on the panel), the segment can be lit or put out.
At initial reset, the contents of the display memory are undefined, therefore it is necessary to initialize by software. Since the display memory permits reading and writing, the addresses/bits that are not used on the LCD display can be used as general-purpose registers.

4.7.7 Programming notes

(1) The contents of the display memory are undefined until the area is initialized (through, for instance, memory clear processing by the CPU). Initialize the display memory by executing initial processing.

(2) 100 msec or more time is necessary for stabilizing the LCD drive voltages V_{C1}, V_{C2} and V_{C3} after setting the LCD power control register LPWR to "1". Be careful of the segment-on right after the power is turned on.

4.8 Clock Timer

4.8.1 Configuration of clock timer

The E0C63P366 has a built-in clock timer that uses OSC1 (crystal oscillator) as the source oscillator. The clock timer is configured of an 8-bit binary counter that serves as the input clock, fOSC1 divided clock output from the prescaler. Timer data (128–16 Hz and 8–1 Hz) can be read out by the software.
Figure 4.8.1.1 is the block diagram for the clock timer.

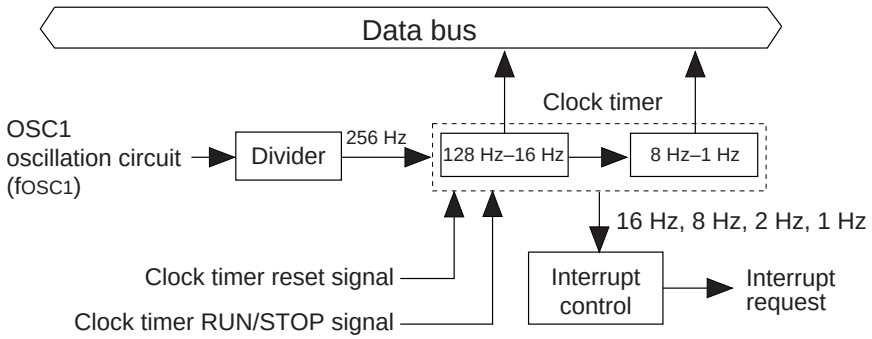


Fig. 4.8.1.1 Block diagram for the clock timer

Ordinarily, this clock timer is used for all types of timing functions such as clocks.

4.8.2 Data reading and hold function

The 8 bits timer data are allocated to the address FF79H and FF7AH.

<FF79H>	D0: TM0 = 128 Hz	D1: TM1 = 64 Hz	D2: TM2 = 32 Hz	D3: TM3 = 16 Hz
<FF7AH>	D0: TM4 = 8 Hz	D1: TM5 = 4 Hz	D2: TM6 = 2 Hz	D3: TM7 = 1 Hz

Since the clock timer data has been allocated to two addresses, a carry is generated from the low-order data within the count (TM0–TM3: 128–16 Hz) to the high-order data (TM4–TM7: 8–1 Hz). When this carry is generated between the reading of the low-order data and the high-order data, a content combining the two does not become the correct value (the low-order data is read as FFH and the high-order data becomes the value that is counted up 1 from that point).
The high-order data hold function in the E0C63P366 is designed to operate to avoid this. This function temporarily stops the counting up of the high-order data (by carry from the low-order data) at the point where the low-order data has been read and consequently the time during which the high-order data is held is the shorter of the two indicated here following.

1. Period until it reads the high-order data.
2. 0.48–1.5 msec (Varies due to the read timing.)

Note: Since the low-order data is not held when the high-order data has previously been read, the low-order data should be read first.

4.8.3 Interrupt function

The clock timer can cause interrupts at the falling edge of 16 Hz, 8 Hz, 2 Hz and 1 Hz signals. Software can set whether to mask any of these frequencies.
Figure 4.8.3.1 is the timing chart of the clock timer.

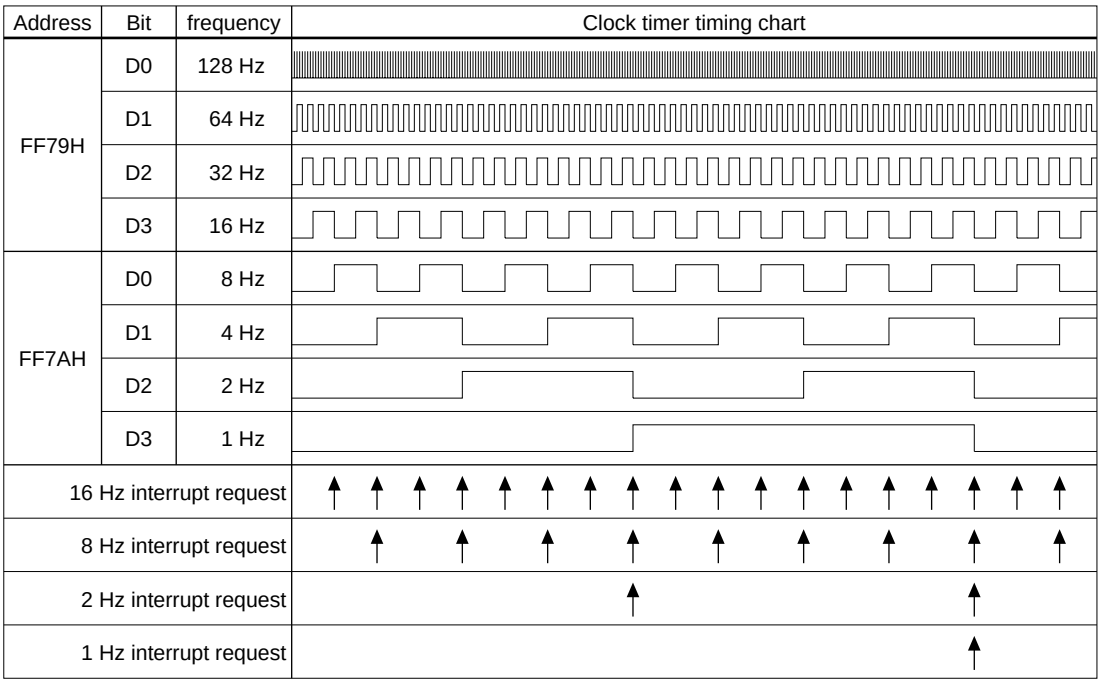


Fig. 4.8.3.1 Timing chart of clock timer

As shown in Figure 4.8.3.1, interrupt is generated at the falling edge of the frequencies (16 Hz, 8 Hz, 2 Hz, 1 Hz). At this time, the corresponding interrupt factor flag (IT0, IT1, IT2, IT3) is set to "1". Selection of whether to mask the separate interrupts can be made with the interrupt mask registers (EIT0, EIT1, EIT2, EIT3). However, regardless of the interrupt mask register setting, the interrupt factor flag is set to "1" at the falling edge of the corresponding signal.

4.8.4 I/O memory of clock timer

Table 4.8.4.1 shows the I/O addresses and the control bits for the clock timer.

Table 4.8.4.1 Control bits of clock timer

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
FF78H	0	0	TMRST	TMRUN	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R		W	R/W	TMRST*3	Reset	Reset	Invalid	Clock timer reset (writing)
					TMRUN	0	Run	Stop	Clock timer Run/Stop
FF79H	TM3	TM2	TM1	TM0	TM3	0			Clock timer data (16 Hz)
					TM2	0			Clock timer data (32 Hz)
	R				TM1	0			Clock timer data (64 Hz)
					TM0	0			Clock timer data (128 Hz)
FF7AH	TM7	TM6	TM5	TM4	TM7	0			Clock timer data (1 Hz)
					TM6	0			Clock timer data (2 Hz)
	R				TM5	0			Clock timer data (4 Hz)
					TM4	0			Clock timer data (8 Hz)
FFE6H	EIT3	EIT2	EIT1	EIT0	EIT3	0	Enable	Mask	Interrupt mask register (Clock timer 1 Hz)
					EIT2	0	Enable	Mask	Interrupt mask register (Clock timer 2 Hz)
	R/W				EIT1	0	Enable	Mask	Interrupt mask register (Clock timer 8 Hz)
					EIT0	0	Enable	Mask	Interrupt mask register (Clock timer 16 Hz)
FFF6H	IT3	IT2	IT1	IT0	IT3	0	(R)	(R)	Interrupt factor flag (Clock timer 1 Hz)
					IT2	0	Yes	No	Interrupt factor flag (Clock timer 2 Hz)
	R/W				IT1	0	(W)	(W)	Interrupt factor flag (Clock timer 8 Hz)
					IT0	0	Reset	Invalid	Interrupt factor flag (Clock timer 16 Hz)

*1 Initial value at initial reset

*2 Not set in the circuit

*3 Constantly "0" when being read

TM0–TM7: Timer data (FF79H, FF7AH)

The 128–1 Hz timer data of the clock timer can be read out with these registers. These eight bits are read only, and writing operations are invalid.
By reading the low-order data (FF79H), the high-order data (FF7AH) is held until reading or for 0.48–1.5 msec (one of shorter of them).
At initial reset, the timer data is initialized to "00H".

TMRST: Clock timer reset (FF78H•D1)

This bit resets the clock timer.

When "1" is written: Clock timer reset
When "0" is written: No operation
Reading: Always "0"

The clock timer is reset by writing "1" to TMRST. When the clock timer is reset in the RUN status, operation restarts immediately. Also, in the STOP status the reset data is maintained. No operation results when "0" is written to TMRST.
This bit is write-only, and so is always "0" at reading.

TMRUN: Clock timer RUN/STOP control register (FF78H•D0)

Controls RUN/STOP of the clock timer.

When "1" is written: RUN
When "0" is written: STOP
Reading: Valid

The clock timer enters the RUN status when "1" is written to the TMRUN register, and the STOP status when "0" is written. In the STOP status, the timer data is maintained until the next RUN status or the timer is reset. Also, when the STOP status changes to the RUN status, the data that is maintained can be used for resuming the count.
At initial reset, this register is set to "0".

EIT0: 16 Hz interrupt mask register (FFE6H•D0)
EIT1: 8 Hz interrupt mask register (FFE6H•D1)
EIT2: 2 Hz interrupt mask register (FFE6H•D2)
EIT3: 1 Hz interrupt mask register (FFE6H•D3)
These registers are used to select whether to mask the clock timer interrupt.

When "1" is written: Enabled
When "0" is written: Masked
Reading: Valid

The interrupt mask registers (EIT0, EIT1, EIT2, EIT3) are used to select whether to mask the interrupt to the separate frequencies (16 Hz, 8 Hz, 2 Hz, 1 Hz).
At initial reset, these registers are set to "0".

IT0: 16 Hz interrupt factor flag (FFF6H•D0)
IT1: 8 Hz interrupt factor flag (FFF6H•D1)
IT2: 2 Hz interrupt factor flag (FFF6H•D2)
IT3: 1 Hz interrupt factor flag (FFF6H•D3)
These flags indicate the status of the clock timer interrupt.

When "1" is read: Interrupt has occurred
When "0" is read: Interrupt has not occurred

When "1" is written: Flag is reset
When "0" is written: Invalid

The interrupt factor flags (IT0, IT1, IT2, IT3) correspond to the clock timer interrupts of the respective frequencies (16 Hz, 8 Hz, 2 Hz, 1 Hz). The software can judge from these flags whether there is a clock timer interrupt. However, even if the interrupt is masked, the flags are set to "1" at the falling edge of the signal.
These flags are reset to "0" by writing "1" to them.
After an interrupt occurs, the same interrupt will occur again if the interrupt enabled state (I flag = "1") is set or the RETI instruction is executed unless the interrupt factor flag is reset. Therefore, be sure to reset (write "1" to) the interrupt factor flag in the interrupt service routine before shifting to the interrupt enabled state.
At initial reset, these flags are set to "0".

4.8.5 Programming notes

(1) Be sure to read timer data in the order of low-order data (TM0–TM3) then high-order data (TM4–TM7).

(2) After an interrupt occurs, the same interrupt will occur again if the interrupt enabled state (I flag = "1") is set or the RETI instruction is executed unless the interrupt factor flag is reset. Therefore, be sure to reset (write "1" to) the interrupt factor flag in the interrupt service routine before shifting to the interrupt enabled state.

4.9 Programmable Timer

4.9.1 Configuration of programmable timer

The E0C63P366 has two 8-bit programmable timer systems (timer 0 and timer 1) built-in.
Timer 0 and timer 1 are composed of 8-bit presettable down counters and they can be used as 8-bit × 2 channel programmable timers or a 16-bit × 1 channel programmable timer by software setting. Timer 0 also has an event counter function using the K13 input port terminal.
Figure 4.9.1.1 shows the configuration of the programmable timer.

The programmable timer is designed to count down from the initial value set in the counter with software. An underflow according to the initial value occurs by counting down and is used for the following functions:

- Presetting the initial value to the counter to generate the periodical underflow signal
- Generating an interrupt
- Generating a TOUT signal output from the R02 output port terminal
- Generating the synchronous clock source for the serial interface (timer 1 underflow is used, and it is possible to set the transfer rate)

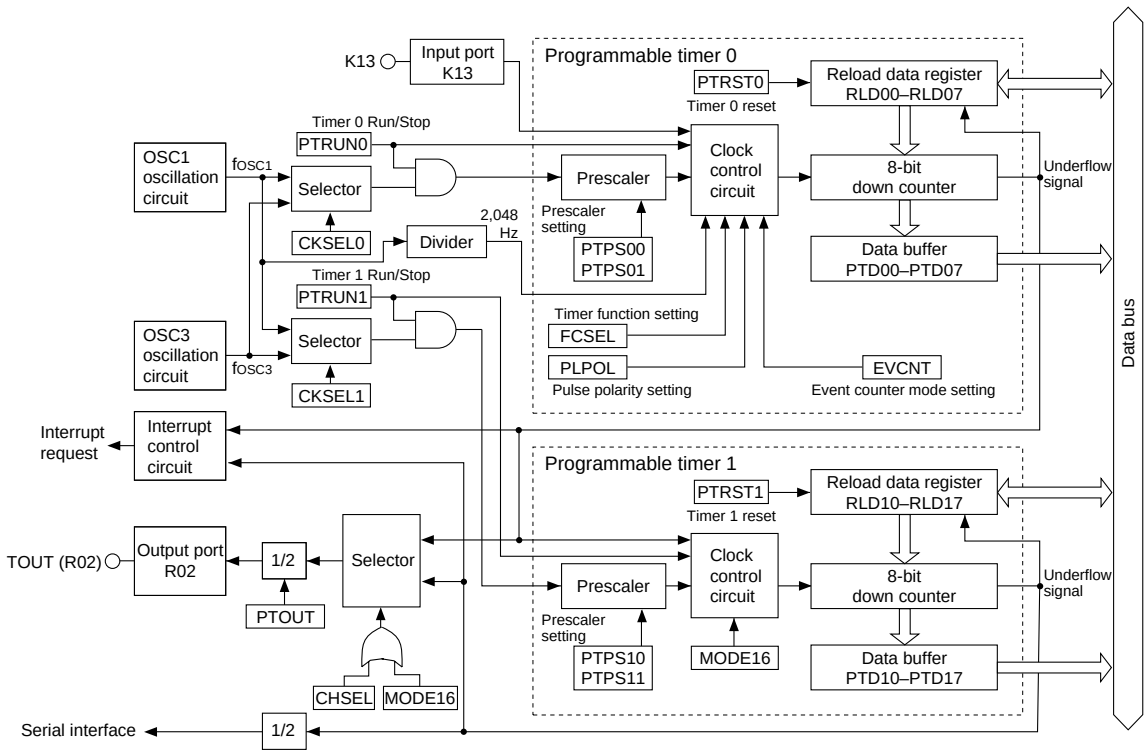


Fig. 4.9.1.1 Configuration of programmable timer

4.9.2 Tow separate 8-bit timer (MODE16 = "0") operation

4.9.2.1 Setting of initial value and counting down

Timers 0 and 1 each have a down counter and reload data register.

The reload data registers RLD00–RLD07 (timer 0) and RLD10–RLD17 (timer 1) are used to set the initial value to the down counter.
By writing "1" to the timer reset bit PTRST0 (timer 0) or PTRST1 (timer 1), the down counter loads the initial value set in the reload register RLD. Therefore, down-counting is executed from the stored initial value by the input clock.

The registers PTRUN0 (timer 0) and PTRUN1 (timer 1) are provided to control the RUN/STOP for timers 0 and 1. By writing "1" to the register after presetting the reload data to the down counter, the down counter starts counting down. Writing "0" stops the input count clock and the down counter stops counting. This control (RUN/STOP) does not affect the counter data. The counter maintains its data while stopped, and can restart counting continuing from that data.

The counter data can be read via the data buffers PTD00–PTD07 (timer 0) and PTD10–PTD17 (timer 1) in optional timing. However, the counter has the data hold function the same as the clock timer, that holds the high-order data when the low-order data is read in order to prevent the borrowing operation between low- and high-order reading, therefore be sure to read the low-order data first.

The counter reloads the initial value set in the reload data register RLD when an underflow occurs through the count down. It continues counting down from the initial value after reloading.
In addition to reloading the counter, this underflow signal controls the interrupt generation, pulse (TOUT signal) output and clock supplying to the serial interface.

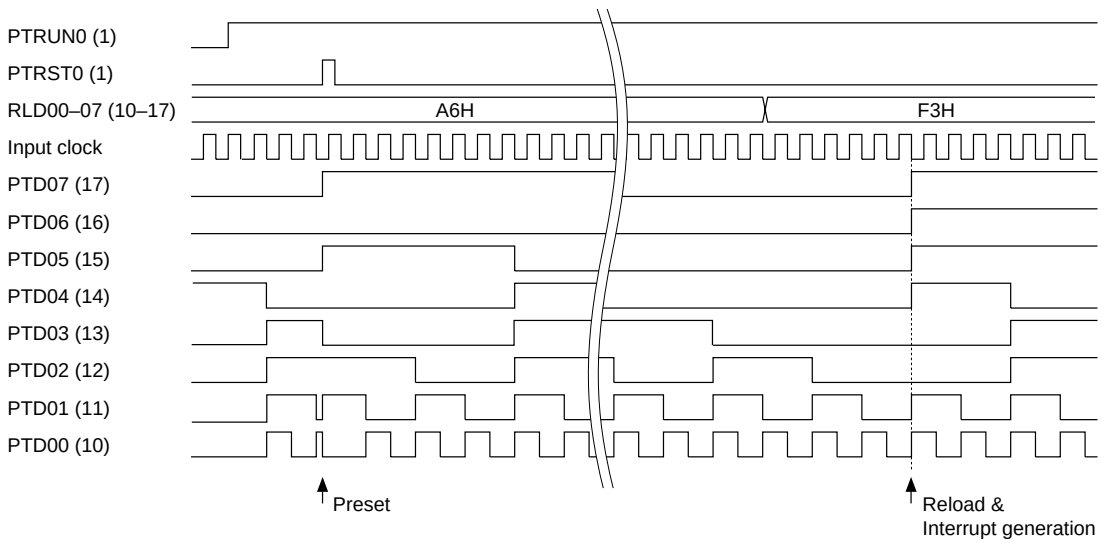


Fig. 4.9.2.1.1 Basic operation timing of down counter

4.9.2.2 Counter mode

The programmable timer can operate in two counter modes, timer mode and event counter mode. It can be selected by software.

(1) Timer mode

The timer mode counts down using the prescaler output as an input clock. In this mode, the programmable timer operates as a periodical timer using the OSC1 or OSC3 oscillation clock as a clock source. Timer 0 can operate in both the timer mode and the event counter mode. The mode can be switched using the timer 0 counter mode selection register EVCNT. When the EVCNT register is set to "0", timer 0 operates in the timer mode.
Timer 1 operates only in the timer mode.
At initial reset, this mode is set.

Refer to Section 4.9.2.1, "Setting of initial value and counting down" for basic operation and control.

The input clock in the timer mode is generated by the prescaler built into the programmable timer. The prescaler generates the input clock by dividing the OSC1 or OSC3 oscillation clock. Refer to the next section for setting the input clock.

(2) Event counter mode

The timer 0 has an event counter function that counts an external clock input to the input port K13. This function is selected by writing "1" to the timer 0 counter mode selection register EVCNT. The timer 1 operates only in the timer mode, and cannot be used as an event counter.

In the event counter mode, the clock is supplied to timer 0 from outside of the IC, therefore, the settings of the timer 0 prescaler division ratio selection registers PTPS00 and PTPS01 and the settings of the timer 0 source clock selection register CKSEL0 become invalid.

Count down timing can be selected from either the falling or rising edge of the input clock using the timer 0 pulse polarity selection register PLPOL. When "0" is written to the PLPOL register, the falling edge is selected, and when "1" is written, the rising edge is selected. The count down timing is shown in Figure 4.9.2.2.1.

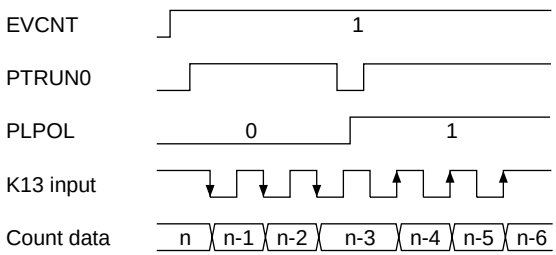


Fig. 4.9.2.2.1 Timing chart in event counter mode

The event counter mode also includes a noise reject function to eliminate noise such as chattering on the external clock (K13 input signal). This function is selected by writing "1" to the timer 0 function selection register FCSEL.
When "with noise rejector" is selected, an input pulse width for both low and high levels must be 0.98 msec or more to count reliably. (The noise rejecter allows the counter to input the clock at the second falling edge of the internal 2,048 Hz signal after changing the input level of the K13 input port terminal. Consequently, the pulse width of noise that can reliably be rejected is 0.48 msec or less.) Figure 4.9.2.2.2 shows the count down timing with noise rejecter.

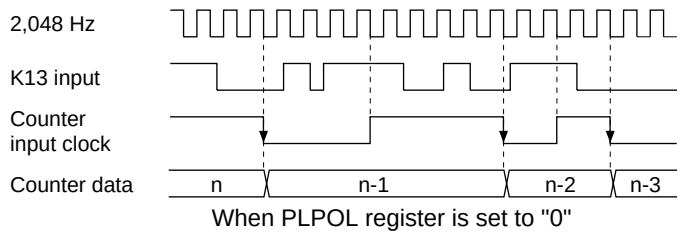


Fig. 4.9.2.2.2 Count down timing with noise rejecter

The operation of the event counter mode is the same as the timer mode except it uses the K13 input as the clock.
Refer to Section 4.9.2.1, "Setting of initial value and counting down" for basic operation and control.

4.9.2.3 Setting of input clock in timer mode

Timer 0 and timer 1 each include a prescaler. The prescalers generate the input clock for each timer by dividing the source clock supplied from the OSC1 or OSC3 oscillation circuit.
The source clock (OSC1 or OSC3) and the division ratio of the prescaler can be selected with software for timer 0 and timer 1 individually.
The set input clock is used for the count clock during operation in the timer mode. When the timer 0 is used in the event counter mode, the following settings become invalid.

The input clock is set in the following sequence.

(1) Selection of source clock

Select the source clock input to each prescaler from either OSC1 or OSC3. This selection is done using the source clock selection registers CKSEL0 (timer 0) and CKSEL1 (timer 1); when "0" is written to the register, OSC1 is selected and when "1" is written, OSC3 is selected.
When the OSC3 oscillation clock is selected for the clock source, it is necessary to turn the OSC3 oscillation ON, prior to using the programmable timer. However the OSC3 oscillation circuit requires a time interval of several msec to several 10 msec from turning the circuit ON until the oscillation stabilizes. Therefore, allow an adequate interval from turning the OSC3 oscillation circuit ON to starting the programmable timer. Refer to Section 4.3, "Oscillation Circuit", for the control and notes of the OSC3 oscillation circuit.
At initial reset, the OSC3 oscillation circuit is set in the OFF state.

(2) Selection of prescaler division ratio

Select the division ratio for each prescaler from among 4 types. This selection is done using the prescaler division ratio selection registers PTPS00/PTPSC01 (timer 0) and PTPS10/PTPS11 (timer 1).
Table 4.9.2.3.1 shows the correspondence between the setting value and the division ratio.

Table 4.9.2.3.1 Selection of prescaler division ratio

PTPS11 PTPS01	PTPS10 PTPS00	Prescaler division ratio
1	1	Source clock / 256
1	0	Source clock / 32
0	1	Source clock / 4
0	0	Source clock / 1

By writing "1" to the register PTRUN0 (timer 0) or PTRUN1 (timer 1), the prescaler inputs the source clock and outputs the clock divided by the selected division ratio. The counter starts counting down by inputting the clock.

4.9.2.4 Interrupt function

The programmable timer can generate an interrupt due to an underflow of the timer 0 and timer 1. See Figure 4.9.2.1.1 for the interrupt timing.

An underflow of timer 0 and timer 1 sets the corresponding interrupt factor flag IPT0 (timer 0) or IPT1 (timer 1) to "1", and generates an interrupt. The interrupt can also be masked by setting the corresponding interrupt mask register EIPT0 (timer 0) or EIPT1 (timer 1). However, the interrupt factor flag is set to "1" by an underflow of the corresponding timer regardless of the interrupt mask register setting.

4.9.2.5 Setting of TOUT output

The programmable timer can generate a TOUT signal due to an underflow of timer 0 or timer 1. The TOUT signal is generated by dividing the underflows in 1/2. It is possible to select which timer's underflow is to be used by the TOUT output channel selection register CHSEL. When "0" is written to the CHSEL register, timer 0 is selected and when "1" is written, timer 1 is selected.
Figure 4.9.2.5.1 shows the TOUT signal waveform when the channel is changed.

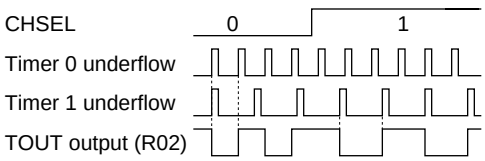


Fig. 4.9.2.5.1 TOUT signal waveform at channel change

The TOUT signal can be output from the R02 output port terminal. Programmable clocks can be supplied to external devices.
Figure 4.9.2.5.2 shows the configuration of the output port R02.

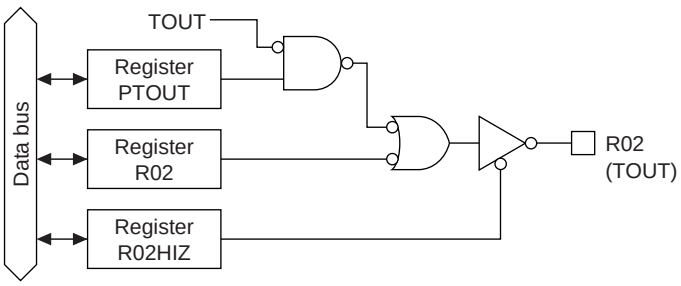


Fig. 4.9.2.5.2 Configuration of R02

The output of a TOUT signal is controlled by the PTOUT register. When "1" is written to the PTOUT register, the TOUT signal is output from the R02 output port terminal and when "0" is written, the terminal goes to a high (V_{DD}) level. However, the data register R02 must always be "1" and the high impedance control register R02HIZ must always be "0" (data output state).

Since the TOUT signal is generated asynchronously from the PTOUT register, a hazard within 1/2 cycle is generated when the signal is turned ON and OFF by setting the register.
Figure 4.9.2.5.3 shows the output waveform of the TOUT signal.

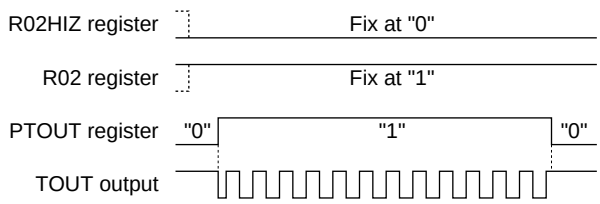


Fig. 4.9.2.5.3 Output waveform of the TOUT signal

4.9.2.6 Transfer rate setting for serial interface

The signal that is made from underflows of timer 1 by dividing them in 1/2, can be used as the clock source for the serial interface.
The programmable timer outputs the clock to the serial interface by setting timer 1 into RUN state (PTRUN1 = "1"). It is not necessary to control with the PTOUT register.

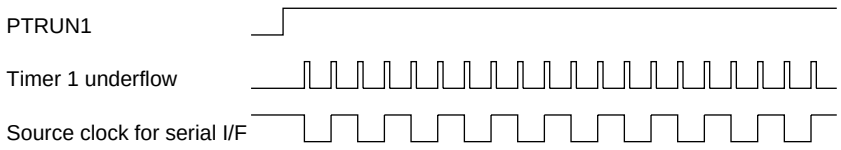


Fig. 4.9.2.6.1 Synchronous clock of serial interface

A setting value for the RLD1X register according to a transfer rate is calculated by the following expression:

RLD1X = fosc / (2 ∗ bps ∗ division ratio of the prescaler) - 1

fosc: Oscillation frequency (OSC1/OSC3)
bps: Transfer rate
(00H can be set to RLD1X)

4.9.3 One channel × 16-bit timer (MODE16 = "1") operation

Timer 0 and timer 1 are chained together to form 16-bit down counter low byte in timer 0, high byte in timer 1.

4.9.3.1 Setting of initial value and counting down

Timers 0 and 1 each have a down counter and reload data register.

The reload data registers RLD00–RLD07 (timer 0) and RLD10–RLD17 (timer 1) are used to set the initial value to the down counter.
By writing "1" to the timer reset bit PTRST0 (timer 0) or PTRST1 (timer 1), the down counter loads the initial value set in the reload register RLD. Therefore, down-counting is executed from the stored initial value by the input clock.

The register PTRUN0 (timer 0) is used to control the RUN/STOP for timers 0 and 1. By writing "1" to the register after presetting the reload data to the down counter, the down counter starts counting down. Writing "0" stops the input count clock and the down counter stops counting. This control (RUN/STOP) does not affect the counter data. The counter maintains its data while stopped, and can restart counting continuing from that data.

The counter data can be read via the data buffers PTD00–PTD07 (timer 0) and PTD10–PTD17 (timer 1) in optional timing. However, the counter has the data hold function the same as the clock timer, that holds the high-order data when the low-order data is read in order to prevent the borrowing operation between low- and high-order reading, therefore be sure to read the low-order data first.

The counter reloads the initial value set in the reload data register RLD when an underflow occurs through the count down. It continues counting down from the initial value after reloading.
In addition to reloading the counter, this underflow signal controls the interrupt generation, pulse (TOUT signal) output and clock supplying to the serial interface.

4.9.3.2 Counter mode

The programmable timer can operate in two counter modes, timer mode and event counter mode. It can be selected by software.

(1) Timer mode

The timer mode counts down using the prescaler output as an input clock. In this mode, the programmable timer operates as a periodical timer using the OSC1 or OSC3 oscillation clock as a clock source. The programmable timer can operate in both the timer mode and the event counter mode. The mode can be switched using the timer 0 counter mode selection register EVCNT. When the EVCNT register is set to "0", the programmable timer operates in the timer mode.
At initial reset, this mode is set.

Refer to Section 4.9.3.1, "Setting of initial value and counting down" for basic operation and control.

The input clock in the timer mode is generated by the prescaler built into the programmable timer. The prescaler generates the input clock by dividing the OSC1 or OSC3 oscillation clock. Refer to the next section for setting the input clock.

(2) Event counter mode

The programmable timer has an event counter function that counts an external clock input to the input port K13. This function is selected by writing "1" to the timer 0 counter mode selection register EVCNT.

In the event counter mode, the clock is supplied to timer 0 from outside of the IC, therefore, the settings of the timer 0 prescaler division ratio selection registers PTPS00 and PTPS01 and the settings of the timer 0 source clock selection register CKSEL0 become invalid.

Count down timing can be selected from either the falling or rising edge of the input clock using the timer 0 pulse polarity selection register PLPOL. When "0" is written to the PLPOL register, the falling edge is selected, and when "1" is written, the rising edge is selected. The count down timing is shown in Figure 4.9.3.2.1.

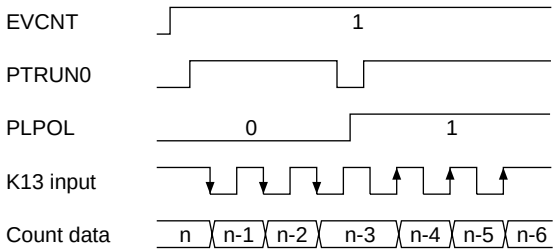


Fig. 4.9.3.2.1 Timing chart in event counter mode

The event counter mode also includes a noise reject function to eliminate noise such as chattering on the external clock (K13 input signal). This function is selected by writing "1" to the timer 0 function selection register FCSEL.
When "with noise rejector" is selected, an input pulse width for both low and high levels must be 0.98 msec or more to count reliably. (The noise rejecter allows the counter to input the clock at the second falling edge of the internal 2,048 Hz signal after changing the input level of the K13 input port terminal. Consequently, the pulse width of noise that can reliably be rejected is 0.48 msec or less.)
Figure 4.9.3.2.2 shows the count down timing with noise rejecter.

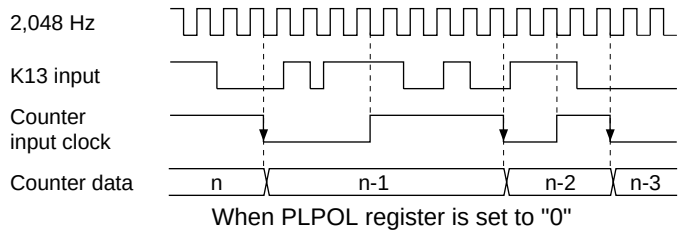


Fig. 4.9.3.2.2 Count down timing with noise rejecter

The operation of the event counter mode is the same as the timer mode except it uses the K13 input as the clock.
Refer to Section 4.9.3.1, "Setting of initial value and counting down" for basic operation and control.

4.9.3.3 Setting of input clock in timer mode

The 16 bit programmable timer include a prescaler. The prescalers generate the input clock for this programmable timer by dividing the source clock supplied from the OSC1 or OSC3 oscillation circuit. The source clock (OSC1 or OSC3) and the division ratio of the prescaler can be selected with software. The set input clock is used for the count clock during operation in the timer mode. When the 16 bit programmable timer is used in the event counter mode, the following settings become invalid.

The input clock is set in the following sequence.

(1) Selection of source clock

Select the source clock input to the prescaler from either OSC1 or OSC3. This selection is done using the source clock selection register CKSEL0 (timer 0); when "0" is written to the register, OSC1 is selected and when "1" is written, OSC3 is selected.
When the OSC3 oscillation clock is selected for the clock source, it is necessary to turn the OSC3 oscillation ON, prior to using the programmable timer. However the OSC3 oscillation circuit requires a time interval of at least 5 msec from turning the circuit ON until the oscillation stabilizes. Therefore, allow an adequate interval from turning the OSC3 oscillation circuit ON to starting the programmable timer. Refer to Section 4.3, "Oscillation Circuit", for the control and notes of the OSC3 oscillation circuit.
At initial reset, the OSC3 oscillation circuit is set in the OFF state.

(2) Selection of prescaler division ratio

Select the division ratio for the prescaler from among 4 types. This selection is done using the prescaler division ratio selection registers PTPS00/PTPSC01 (timer 0). Table 4.9.3.3.1 shows the correspondence between the setting value and the division ratio.

Table 4.9.3.3.1 Selection of prescaler division ratio

PTPS01	PTPS00	Prescaler division ratio
1	1	Source clock / 256
1	0	Source clock / 32
0	1	Source clock / 4
0	0	Source clock / 1

By writing "1" to the register PTRUN0 (timer 0), the prescaler inputs the source clock and outputs the clock divided by the selected division ratio. The counter starts counting down by inputting the clock.

4.9.3.4 Interrupt function

The programmable timer can generate an interrupt due to an underflow.

An underflow of this 16 bit programmable timer sets the corresponding interrupt factor flag IPT1 (timer 1) to "1", and generates an interrupt. The interrupt can also be masked by setting the corresponding interrupt mask register EIPT1 (timer 1). However, the interrupt factor flag is set to "1" by an underflow of the corresponding timer regardless of the interrupt mask register setting.

4.9.3.5 Setting of TOUT output

The programmable timer can generate a TOUT signal due to an underflow of this 16 bit programmable timer. The TOUT signal is generated by dividing the underflows in 1/2.

The TOUT signal can be output from the R02 output port terminal. Programmable clocks can be supplied to external devices.
Figure 4.9.3.5.1 shows the configuration of the output port R02.

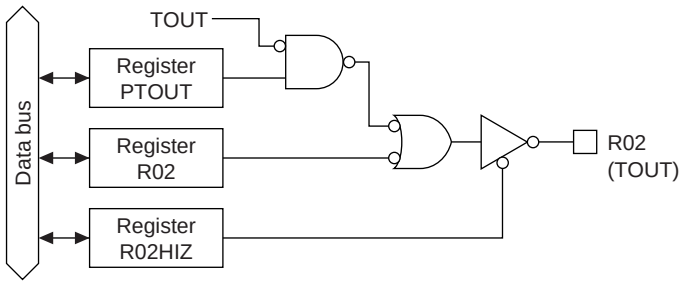


Fig. 4.9.3.5.1 Configuration of R02

The output of a TOUT signal is controlled by the PTOUT register. When "1" is written to the PTOUT register, the TOUT signal is output from the R02 output port terminal and when "0" is written, the terminal goes to a high (V_{DD}) level. However, the data register R02 must always be "1" and the high impedance control register R02HIZ must always be "0" (data output state).

Since the TOUT signal is generated asynchronously from the PTOUT register, a hazard within 1/2 cycle is generated when the signal is turned ON and OFF by setting the register.
Figure 4.9.3.5.2 shows the output waveform of the TOUT signal.

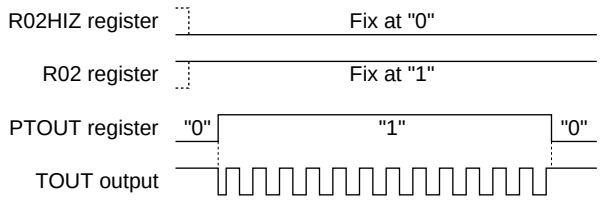


Fig. 4.9.3.5.2 Output waveform of the TOUT signal

4.9.3.6 Transfer rate setting for serial interface

The signal that is made from underflows of the 16 bit programmable timer by dividing them in 1/2, can be used as the clock source for the serial interface.
The programmable timer outputs the clock to the serial interface by setting this 16 bit programmable timer into RUN state (PTRUN0 = "1"). It is not necessary to control with the PTOUT register.

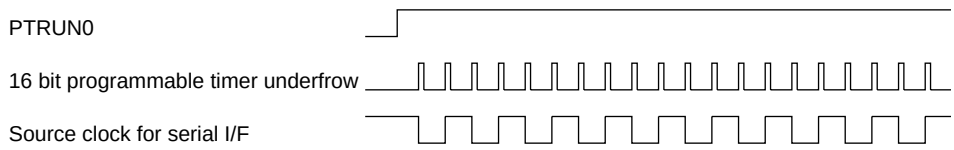


Fig. 4.9.3.6.1 Synchronous clock of serial interface

A setting value for the RLD1X register according to a transfer rate is calculated by the following expression:

RLD1X, RLD0X = fosc / (2 ∗ bps ∗ division ratio of the prescaler) - 1

fosc: Oscillation frequency (OSC1/OSC3)
bps: Transfer rate
(00H can be set to RLD1X)

4.9.4 I/O memory of programmable timer

Table 4.9.4.1 shows the I/O addresses and the control bits for the programmable timer.

Table 4.9.4.1 Control bits of programmable timer

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
FFC0H	MODE16	EVCNT	FCSEL	PLPOL	MODEL16	0	16 bit × 1	8 bit × 2	8 bit × 2 or 16 bit × 1 timer mode selection
					EVCNT	0	Event ct.	Timer	Timer 0 counter mode selection
	R/W				FCSEL	0	With NR	No NR	Timer 0 function selection (for event counter mode)
					PLPOL	0	↑	↓	Timer 0 pulse polarity selection (for event counter mode)
FFC1H	CHSEL	PTOUT	CKSEL1	CKSEL0	CHSEL	0	Timer1	Timer0	TOUT output channel selection
					PTOUT	0	On	Off	TOUT output control
	R/W				CKSEL1	0	OSC3	OSC1	Prescaler 1 source clock selection
					CKSEL0	0	OSC3	OSC1	Prescaler 0 source clock selection
FFC2H	PTPS01	PTPS00	PTRST0	PTRUN0	PTPS01	0			Prescaler 0 division ratio selection [PTPS01, 00]: 0 = 1/1, 1 = 1/4, 2 = 1/32, 3 = 1/256
					PTPS00	0			
	R/W		W	R/W	PTRST0*3	– *2	Reset	Invalid	Timer 0 reset (reload)
					PTRUN0	0	Run	Stop	Timer 0 Run/Stop
FFC3H	PTPS11	PTPS10	PTRST1	PTRUN1	PTPS11	0			Prescaler 1 division ratio selection [PTPS11, 10]: 0 = 1/1, 1 = 1/4, 2 = 1/32, 3 = 1/256
					PTPS10	0			
	R/W		W	R/W	PTRST1*3	– *2	Reset	Invalid	Timer 1 reset (reload)
					PTRUN1	0	Run	Stop	Timer 1 Run/Stop
FFC4H	RLD03	RLD02	RLD01	RLD00	RLD03	0			MSB
					RLD02	0			Programmable timer 0 reload data (low-order 4 bits)
	R/W				RLD01	0			
					RLD00	0			LSB
FFC5H	RLD07	RLD06	RLD05	RLD04	RLD07	0			MSB
					RLD06	0			Programmable timer 0 reload data (high-order 4 bits)
	R/W				RLD05	0			
					RLD04	0			LSB
FFC6H	RLD13	RLD12	RLD11	RLD10	RLD13	0			MSB
					RLD12	0			Programmable timer 1 reload data (low-order 4 bits)
	R/W				RLD11	0			
					RLD10	0			LSB
FFC7H	RLD17	RLD16	RLD15	RLD14	RLD17	0			MSB
					RLD16	0			Programmable timer 1 reload data (high-order 4 bits)
	R/W				RLD15	0			
					RLD14	0			LSB
FFC8H	PTD03	PTD02	PTD01	PTD00	PTD03	0			MSB
					PTD02	0			Programmable timer 0 data (low-order 4 bits)
	R				PTD01	0			
					PTD00	0			LSB
FFC9H	PTD07	PTD06	PTD05	PTD04	PTD07	0			MSB
					PTD06	0			Programmable timer 0 data (high-order 4 bits)
	R				PTD05	0			
					PTD04	0			LSB
FFCAH	PTD13	PTD12	PTD11	PTD10	PTD13	0			MSB
					PTD12	0			Programmable timer 1 data (low-order 4 bits)
	R				PTD11	0			
					PTD10	0			LSB
FFCBH	PTD17	PTD16	PTD15	PTD14	PTD17	0			MSB
					PTD16	0			Programmable timer 1 data (high-order 4 bits)
	R				PTD15	0			
					PTD14	0			LSB
FFE2H	0	0	EIPT1	EIPT0	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R		R/W		EIPT1	0	Enable	Mask	Interrupt mask register (Programmable timer 1)
					EIPT0	0	Enable	Mask	Interrupt mask register (Programmable timer 0)
FFF2H	0	0	IPT1	IPT0	0 *3	– *2	(R)	(R)	Unused
					0 *3	– *2	Yes	No	Unused
	R		R/W		IPT1	0	(W)	(W)	Interrupt factor flag (Programmable timer 1)
					IPT0	0	Reset	Invalid	Interrupt factor flag (Programmable timer 0)

*1 Initial value at initial reset *2 Not set in the circuit *3 Constantly "0" when being read

CKSEL0: Prescaler 0 source clock selection register (FFC1H•D0)
CKSEL1: Prescaler 1 source clock selection register (FFC1H•D1)
Selects the source clock of the prescaler.

When "1" is written: OSC3 clock
When "0" is written: OSC1 clock
Reading: Valid

The source clock for the prescaler is selected from OSC1 or OSC3. When "0" is written to the CKSEL0 register, the OSC1 clock is selected as the input clock for the prescaler 0 (for timer 0) and when "1" is written, the OSC3 clock is selected.
Same as above, the source clock for prescaler 1 is selected by the CKSEL1 register.
When the event counter mode is selected to timer 0, the setting of the CKSEL0 register becomes invalid.
At initial reset, these registers are set to "0".

PTPS00, PTPS01: Timer 0 prescaler division ratio selection register (FFC2H•D2, D3)
PTPS10, PTPS11: Timer 1 prescaler division ratio selection register (FFC3H•D2, D3)
Selects the division ratio of the prescaler.
Two bits of PTPS00 and PTPS01 are the prescaler division ratio selection register for timer 0, and two bits of PTPS10 and PTPS11 are for timer 1. The prescaler division ratios that can be set by these registers are shown in Table 4.9.4.2.

Table 4.9.4.2 Selection of prescaler division ratio

PTPS11 PTPS01	PTPS10 PTPS00	Prescaler division ratio
1	1	Source clock / 256
1	0	Source clock / 32
0	1	Source clock / 4
0	0	Source clock / 1

When the event counter mode is selected to timer 0, the setting of the PTPS00 and PTPS01 becomes invalid.
At initial reset, these registers are set to "0".

EVCNT: Timer 0 counter mode selection register (FFC0H•D2)
Selects a counter mode for timer 0.

When "1" is written: Event counter mode
When "0" is written: Timer mode
Reading: Valid

The counter mode for timer 0 is selected from either the event counter mode or timer mode. When "1" is written to the EVCNT register, the event counter mode is selected and when "0" is written, the timer mode is selected.
At initial reset, this register is set to "0".

MODE16: 8-bit × 2 or 16-bit × 1 timer mode selection register (FFC0H•D3)
Selects 8-bit × 2 channels mode (timer 0 and timer 1) or 16-bit × 1 channel mode.

When "1" is written: 16-bit × 1 channel
When "0" is written: 8-bit × 2 channels (timer 0 and timer 1)
Reading: Valid

When 8-bit × 2 channels is selected, timer 0 and timer 1 can be used independently.
When 16-bit × 1 channel is selected, timer 0 and timer 1 are chained together and are used as a 16-bit programmable timer. The clock is input to timer 0 and interrupts will be generated from timer 1.
At initial reset, this register is set to "0".

FCSEL: Timer 0 function selection register (FFC0H•D1)

Selects whether the noise rejector of the clock input circuit will be used or not in the event counter mode.

When "1" is written: With noise rejecter
When "0" is written: Without noise rejecter
Reading: Valid

When "1" is written to the FCSEL register, the noise rejecter is used and counting is done by an external clock (K13) with 0.98 msec or more pulse width. (The noise rejecter allows the counter to input the clock at the second falling edge of the internal 2,048 Hz signal after changing the input level of the K13 input port terminal. Consequently, the pulse width of noise that can reliably be rejected is 0.48 msec or less.)
When "0" is written to the FCSEL register, the noise rejector is not used and the counting is done directly by an external clock input to the K13 input port terminal.
Setting of this register is effective only when timer 0 is used in the event counter mode.
At initial reset, this register is set to "0".

PLPOL: Timer 0 pulse polarity selection register (FFC0H•D0)

Selects the count pulse polarity in the event counter mode.

When "1" is written: Rising edge
When "0" is written: Falling edge
Reading: Valid

The count timing in the event counter mode (timer 0) is selected from either the falling edge of the external clock input to the K13 input port terminal or the rising edge. When "0" is written to the PLPOL register, the falling edge is selected and when "1" is written, the rising edge is selected.
Setting of this register is effective only when timer 0 is used in the event counter mode.
At initial reset, this register is set to "0".

RLD00–RLD07: Timer 0 reload data register (FFC4H, FFC5H)
RLD10–RLD17: Timer 1 reload data register (FFC6H, FFC7H)

Sets the initial value for the counter.
The reload data written in this register is loaded to the respective counters. The counter counts down using the data as the initial value for counting.
Reload data is loaded to the counter when the counter is reset by writing "1" to the PTRST0 or PTRST1 register, or when counter underflow occurs.
At initial reset, these registers are set to "00H".

PTD00–PTD07: Timer 0 counter data (FFC8H, FFC9H)
PTD10–PTD17: Timer 1 counter data (FFCAH, FFCBH)

Count data in the programmable timer can be read from these latches.
The low-order 4 bits of the count data in timer 0 can be read from PTD00–PTD03, and the high-order data can be read from PTD04–PTD07. Similarly, for timer 1, the low-order 4 bits can be read from PTD10–PTD13, and the high-order data can be read from PTD14–PTD17.
Since the high-order 4 bits are held by reading the low-order 4 bits, be sure to read the low-order 4 bits first.
Since these latches are exclusively for reading, the writing operation is invalid.
At initial reset, these counter data are set to "00H".

PTRST0: Timer 0 reset (reload) (FFC2H•D1)
PTRST1: Timer 1 reset (reload) (FFC3H•D1)
Resets the timer and presets reload data to the counter.

When "1" is written: Reset
When "0" is written: No operation
Reading: Always "0"

By writing "1" to PTRST0, the reload data in the reload register PLD00–PLD07 is preset to the counter in timer 0. Similarly, the reload data in PLD10–PLD17 is preset to the counter in timer 1 by PTRST1.
When the counter is preset in the RUN status, the counter restarts immediately after presetting. In the case of STOP status, the reload data is preset to the counter and is maintained.
No operation results when "0" is written.
Since these bits are exclusively for writing, always set to "0" during reading.

PTRUN0: Timer 0 RUN/STOP control register (FFC2H•D0)
PTRUN1: Timer 1 RUN/STOP control register (FFC3H•D0)
Controls the RUN/STOP of the counter.

When "1" is written: RUN
When "0" is written: STOP
Reading: Valid

The counter in timer 0 starts counting down by writing "1" to the PTRUN0 register and stops by writing "0".
In STOP status, the counter data is maintained until the counter is reset or is set in the next RUN status. When STOP status changes to RUN status, the data that has been maintained can be used for resuming the count.
Same as above, the timer 1 counter is controlled by the PTRUN1 register.
At initial reset, these registers are set to "0".

CHSEL: TOUT output channel selection register (FFC1H•D3)
Selects the channel used for TOUT signal output.

When "1" is written: Timer 1
When "0" is written: Timer 0
Reading: Valid

This register selects which timer's underflow (timer 0 or timer 1) is used to generate a TOUT signal. When "0" is written to the CHSEL register, timer 0 is selected and when "1" is written, timer 1 is selected. In the 16-bit × 2 channels mode (MODE16 = "1"), timer 1 is always selected regardless of this register setting.
At initial reset, this register is set to "0".

PTOUT: TOUT output control register (FFC1H•D2)
Turns TOUT signal output ON and OFF.

When "1" is written: ON
When "0" is written: OFF
Reading: Valid

PTOUT is the output control register for the TOUT signal. When "1" is written to the register, the TOUT signal is output from the output port terminal R02 and when "0" is written, the terminal goes to a high (V_{DD}) level. However, the data register R02 must always be "1" and the high impedance control register R02HIZ must always be "0" (data output state).
At initial reset, this register is set to "0".

EIPT0: Timer 0 interrupt mask register (FFE2H•D0)
EIPT1: Timer 1 interrupt mask register (FFE2H•D1)

These registers are used to select whether to mask the programmable timer interrupt or not.

When "1" is written: Enabled
When "0" is written: Masked
Reading: Valid

Timer 0 and timer 1 interrupts can be masked individually by the interrupt mask registers EIPT0 (timer 0) and EIPT1 (timer 1).
At initial reset, these registers are set to "0".

IPT0: Timer 0 interrupt factor flag (FFF2H•D0)
IPT1: Timer 1 interrupt factor flag (FFF2H•D1)

These flags indicate the status of the programmable timer interrupt.

When "1" is read: Interrupt has occurred
When "0" is read: Interrupt has not occurred

When "1" is written: Flag is reset
When "0" is written: Invalid

The interrupt factor flags IPT0 and IPT1 correspond to timer 0 and timer 1 interrupts, respectively. The software can judge from these flags whether there is a programmable timer interrupt. However, even if the interrupt is masked, the flags are set to "1" by the underflows of the corresponding counters.
These flags are reset to "0" by writing "1" to them.
After an interrupt occurs, the same interrupt will occur again if the interrupt enabled state (I flag = "1") is set or the RETI instruction is executed unless the interrupt factor flag is reset. Therefore, be sure to reset (write "1" to) the interrupt factor flag in the interrupt service routine before shifting to the interrupt enabled state.
At initial reset, these flags are set to "0".

4.9.5 Programming notes

(1) When reading counter data, be sure to read the low-order 4 bits (PTD00–PTD03, PTD10–PTD13) first. Furthermore, the high-order 4 bits (PTD04–PTD07, PTD14–PTD17) should be read within 0.73 msec of reading the low-order 4 bits (PTD00–PTD03, PTD10–PTD13).
For the 16 bit × 1 mode, be sure to read as following sequence:
(PTD00–PTD03) → (PTD04–PTD07) → (PTD10–PTD13) → (PTD14–PTD17)
The read sequence time should be within 1.46 msec.

(2) The programmable timer actually enters RUN/STOP status in synchronization with the falling edge of the input clock after writing to the PTRUN0/PTRUN1 register. Consequently, when "0" is written to the PTRUN0/PTRUN1 register, the timer enters STOP status at the point where the counter is decremented (-1). The PTRUN0/PTRUN1 register maintains "1" for reading until the timer actually stops.
Figure 4.9.5.1 shows the timing chart for the RUN/STOP control.

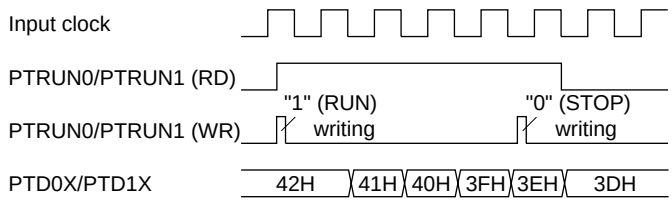


Fig. 4.9.5.1 Timing chart for RUN/STOP control

It is the same even in the event counter mode. Therefore, be aware that the counter does not enter RUN/STOP status if a clock is not input after setting the RUN/STOP control register (PTRUN0).

(3) Since the TOUT signal is generated asynchronously from the PTOUT register, a hazard within 1/2 cycle is generated when the signal is turned ON and OFF by setting the register.

(4) When the OSC3 oscillation clock is selected for the clock source, it is necessary to turn the OSC3 oscillation ON, prior to using the programmable timer. However the OSC3 oscillation circuit requires a time interval of at least 5 msec from turning the circuit ON until the oscillation stabilizes. Therefore, allow an adequate interval from turning the OSC3 oscillation circuit ON to starting the programmable timer. Refer to Section 4.3, "Oscillation Circuit", for the control and notes of the OSC3 oscillation circuit.
At initial reset, the OSC3 oscillation circuit is set in the OFF state.

(5) After an interrupt occurs, the same interrupt will occur again if the interrupt enabled state (I flag = "1") is set or the RETI instruction is executed unless the interrupt factor flag is reset. Therefore, be sure to reset (write "1" to) the interrupt factor flag in the interrupt service routine before shifting to the interrupt enabled state.

4.10 Serial Interface (SIN, SOUT, $\overline{SCLK}$, $\overline{SRDY}$)

4.10.1 Configuration of serial interface

The E0C63P366 has a synchronous clock type 8 bits serial interface built-in.
The configuration of the serial interface is shown in Figure 4.10.1.1.
The CPU, via the 8-bit shift register, can read the serial input data from the SIN terminal. Moreover, via the same 8-bit shift register, it can convert parallel data to serial data and output it to the SOUT terminal.
The synchronous clock for serial data input/output may be set by selecting by software any one of three types of master mode (internal clock mode: when the E0C63P366 is to be the master for serial input/output) and a type of slave mode (external clock mode: when the E0C63P366 is to be the slave for serial input/output).
Also, when the serial interface is used at slave mode, $\overline{SRDY}$ signal which indicates whether or not the serial interface is available to transmit or receive can be output to the $\overline{SRDY}$ terminal.

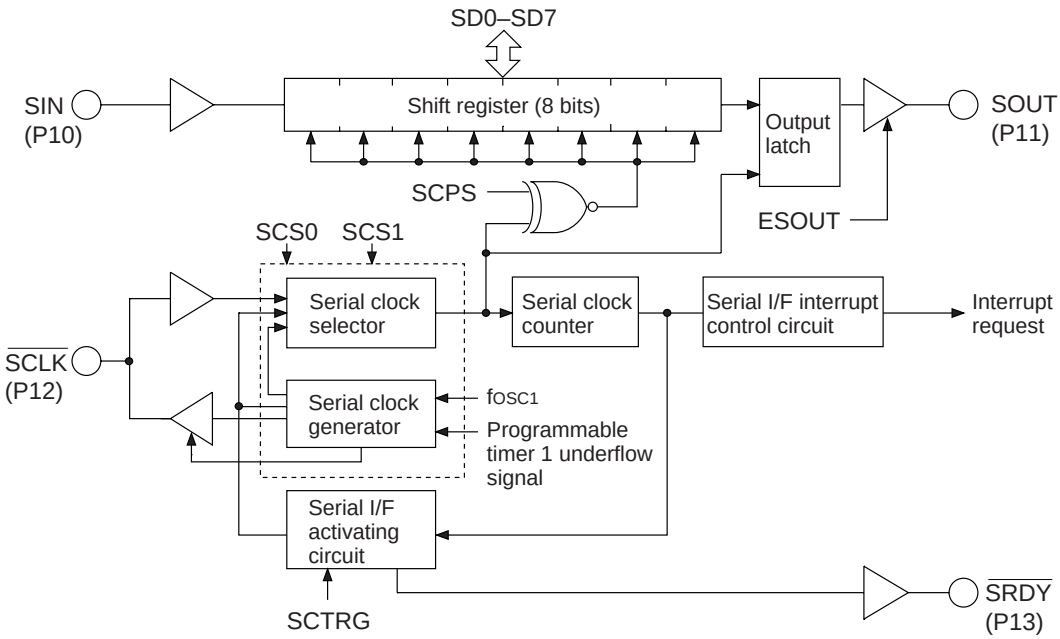


Fig. 4.10.1.1 Configuration of serial interface

The input/output ports of the serial interface are shared with the I/O ports P10–P13, and function of these ports can be selected through the software.
P10–P13 terminals and serial input/output correspondence are as follows:

Master mode	***Slave mode***
P10 = SIN (I)	P10 = SIN (I)
P11 = SOUT (O)	P11 = SOUT (O)
P12 = $\overline{SCLK}$ (O)	P12 = $\overline{SCLK}$ (I)
P13 = I/O port (I/O)	P13 = $\overline{SRDY}$ (O)

Note: At initial reset, P10–P13 are set to I/O ports.
When using the serial interface, switch the function (ESIF = "1") in the initial routine.

The SOUT (data output) signal passes through a tri-state buffer. To output serial data, write "1" to the ESOUT register to set the buffer in data output status. When the ESOUT register is set to "0", the SOUT signal is disabled and the SOUT terminal goes high-impedance status.

4.10.2 Mask option

(1) Terminal specification

Since the input/output terminals of the serial interface is shared with the I/O ports (P10–P13), the terminal specification of the I/O port is also applied to the serial interface.
In the E0C63P366, the I/O ports (P10–P13) specification is fixed at "with pull-up resistor" and "complementary output".
Therefore, the output specification of the terminals SOUT, $\overline{\text{SCLK}}$ (in master mode) and $\overline{\text{SRDY}}$ (in slave mode) that are used as output in the input/output port of the serial interface is fixed at complementary output.
Furthermore, a pull-up resistor is provided for the SIN terminal and the $\overline{\text{SCLK}}$ terminal (in slave mode) that are used as input terminals.

(2) Polarity of synchronous clock and ready signal

Polarity of the synchronous clock and the ready signal that is output in the slave mode is fixed at negative polarity (active low).

4.10.3 Master mode and slave mode of serial interface

The serial interface of the E0C63P366 has two types of operation mode: master mode and slave mode.
The master mode uses an internal clock as the synchronous clock for the built-in shift register, and outputs this internal clock from the $\overline{\text{SCLK}}$ (P12) terminal to control the external (slave side) serial device.
In the slave mode, the synchronous clock output from the external (master side) serial device is input from the $\overline{\text{SCLK}}$ (P12) terminal and it is used as the synchronous clock for the built-in shift register.
The master mode and slave mode are selected by writing data to the SCS1 and SCS0 registers.
When the master mode is selected, a synchronous clock may be selected from among 3 types as shown in Table 4.10.3.1.

Table 4.10.3.1 Synchronous clock selection

SCS1	SCS0	Mode	Synchronous clock
1	1	Master mode	OSC1
1	0		OSC1 /2
0	1		Programmable timer *
0	0	Slave mode	External clock *

∗ The clock frequency is limited to 1 MHz (max.).

When the programmable timer is selected, the signal that is generated by dividing the underflow signal of the programmable timer (timer 1) in 1/2 is used as the synchronous clock. In this case, the programmable timer must be controlled before operating the serial interface. Refer to Section 4.9, "Programmable Timer" for the control of the programmable timer.

At initial reset, the slave mode (external clock mode) is selected.
Moreover, the synchronous clock, along with the input/output of the 8-bit serial data, is controlled as follows:

- In the master mode, after output of 8 clocks from the $\overline{\text{SCLK}}$ (P12) terminal, clock output is automatically suspended and the $\overline{\text{SCLK}}$ (P12) terminal is fixed at high level.
- In the slave mode, after input of 8 clocks to the $\overline{\text{SCLK}}$ (P12) terminal, subsequent clock inputs are masked.

A sample basic serial input/output portion connection is shown in Figure 4.10.3.1.

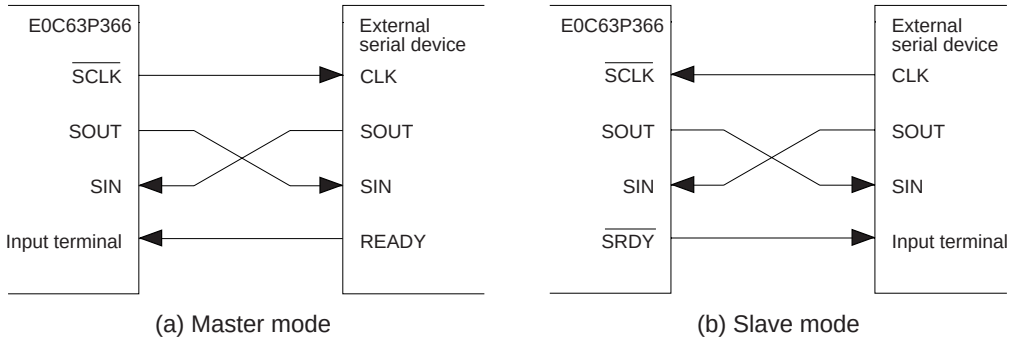


Fig. 4.10.3.1 Sample basic connection of serial input/output section

4.10.4 Data input/output and interrupt function

The serial interface of E0C63P366 can input/output data via the internal 8-bit shift register. The shift register operates by synchronizing with either the synchronous clock output from the $\overline{SCLK}$ (P12) terminal (master mode), or the synchronous clock input to the $\overline{SCLK}$ (P12) terminal (slave mode).
The serial interface generates an interrupt on completion of the 8-bit serial data input/output. Detection of serial data input/output is done by counting of the synchronous clock $\overline{SCLK}$; the clock completes input/output operation when 8 counts (equivalent to 8 cycles) have been made and then generates an interrupt.
The serial data input/output procedure is explained below:

(1) Serial data output procedure and interrupt

The E0C63P366 serial interface is capable of outputting parallel data as serial data, in units of 8 bits. By setting the parallel data to the data registers SD0–SD3 (FF72H) and SD4–SD7 (FF73H) and writing "1" to SCTRG bit (FF70H•D1), it synchronizes with the synchronous clock and the serial data is output to the SOUT (P11) terminal. The synchronous clock used here is as follows: in the master mode, internal clock which is output to the $\overline{SCLK}$ (P12) terminal while in the slave mode, external clock which is input from the $\overline{SCLK}$ (P12) terminal.

The serial data output to the SOUT (P11) terminal changes at the falling edge of the clock input or output from/to the $\overline{SCLK}$ (P12) terminal. The data in the shift register is shifted at the falling edge of the $\overline{SCLK}$ signal when the SCPS register (FF71H•D2) is "1" and is shifted at the rising edge of the $\overline{SCLK}$ signal when the SCPS register is "0".

When the output of the 8-bit data from SD0 to SD7 is completed, the interrupt factor flag ISIF (FFF3H•D0) is set to "1" and an interrupt occurs. Moreover, the interrupt can be masked by the interrupt mask register EISIF (FFE3H•D0). However, regardless of the interrupt mask register setting, the interrupt factor flag is set to "1" after output of the 8-bit data.

(2) Serial data input procedure and interrupt

The E0C63P366 serial interface is capable of inputting serial data as parallel data, in units of 8 bits. The serial data is input from the SIN (P10) terminal, synchronizes with the synchronous clock, and is sequentially read in the 8-bit shift register. As in the above item (1), the synchronous clock used here is as follows: in the master mode, internal clock which is output to the $\overline{SCLK}$ (P12) terminal while in the slave mode, external clock which is input from the $\overline{SCLK}$ (P12) terminal.

The serial data is read into the built-in shift register at the falling edge of the $\overline{SCLK}$ signal when the SCPS register is "1" and is read at the rising edge of the $\overline{SCLK}$ signal when the SCPS register is "0". The shift register is sequentially shifted as the data is fetched.

When the input of the 8-bit data from SD0 to SD7 is completed, the interrupt factor flag ISIF (FFF3H•D0) is set to "1" and an interrupt occurs. Moreover, the interrupt can be masked by the interrupt mask register EISIF (FFE3H•D0). However, regardless of the interrupt mask register setting, the interrupt factor flag is set to "1" after input of the 8-bit data.
The data input in the shift register can be read from data registers SD0–SD7 by software.

(3) Serial data input/output permutation

The E0C63P366 allows the input/output permutation of serial data to be selected by the SDP register (FF71H•D3) as to either LSB first or MSB first. The block diagram showing input/output permutation in case of LSB first and MSB first is provided in Figure 4.10.4.1. The SDP register should be set before setting data to SD0–SD7.

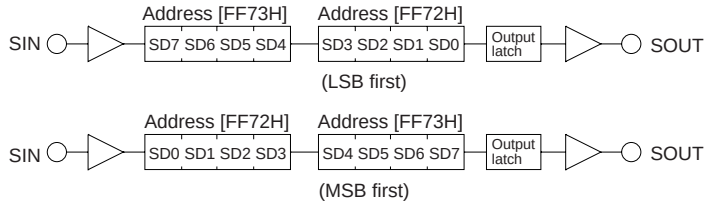


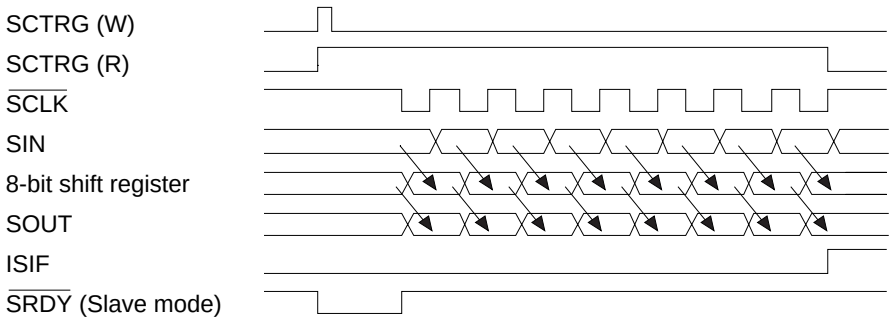
Fig. 4.10.4.1 Serial data input/output permutation

(4) $\overline{\text{SRDY}}$ signal

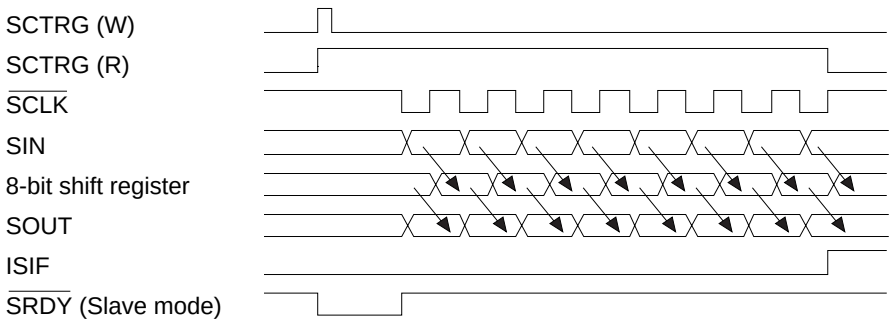
When the E0C63P366 serial interface is used in the slave mode (external clock mode), $\overline{\text{SRDY}}$ signal is used to indicate whether the internal serial interface is available to transmit or receive data for the master side (external) serial device. $\overline{\text{SRDY}}$ signal is output from the $\overline{\text{SRDY}}$ (P13) terminal.
$\overline{\text{SRDY}}$ signal goes "0" (low) when the E0C63P366 serial interface is available to transmit or receive data; normally, it is at "1" (high).
$\overline{\text{SRDY}}$ signal changes from "1" to "0" immediately after "1" is written to SCTRG and returns from "0" to "1" when "0" is input to the $\overline{\text{SCLK}}$ (P12) terminal (i.e., when the serial input/output begins transmitting or receiving data). Moreover, when high-order data is read from or written to SD4–SD7, the $\overline{\text{SRDY}}$ signal returns to "1".

(5) Timing chart

The E0C63P366 serial interface timing chart is shown in Figure 4.10.4.2.



(a) When SCPS = "1"



(b) When SCPS = "0"

Fig. 4.10.4.2 Serial interface timing chart

4.10.5 I/O memory of serial interface

Table 4.10.5.1 shows the I/O addresses and the control bits for the serial interface.

Table 4.10.5.1 Control bits of serial interface

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
FF45H	PUL13	PUL12	PUL11	PUL10	PUL13	1	On	Off	P13 pull-up control register functions as a general-purpose register when SIF (slave) is selected
					PUL12	1	On	Off	P12 pull-up control register (ESIF=0) functions as a general-purpose register when SIF (master) is selected $\overline{SCLK}$ (I) pull-up control register when SIF (slave) is selected
	R/W				PUL11	1	On	Off	P11 pull-up control register (ESIF=0) functions as a general-purpose register when SIF is selected
					PUL10	1	On	Off	P10 pull-up control register (ESIF=0) SIN pull-up control register when SIF is selected
FF70H	0	ESOUT	SCTRG	ESIF	0 *3	– *2			Unused
					ESOUT	0	Enable	Disable	SOUT enable/disable control
					SCTRG	0	Trigger	Invalid	Serial I/F clock trigger (writing)
	R	R/W					Run	Stop	Serial I/F clock status (reading)
					ESIF	0	SIF	I/O	Serial I/F enable (P1 port function selection)
FF71H	SDP	SCPS	SCS1	SCS0	SDP	0	MSB first	LSB first	Serial I/F data input/output permutation
					SCPS	0	↓	↑	Serial I/F clock phase selection [SCS1, 0] 0 1 Clock Slave PT
					SCS1	0			Serial I/F clock mode selection [SCS1, 0] 2 3 Clock OSC1/2 OSC1
	R/W				SCS0	0			
FF72H	SD3	SD2	SD1	SD0	SD3	– *2	High	Low	MSB
					SD2	– *2	High	Low	Serial I/F transmit/receive data (low-order 4 bits)
					SD1	– *2	High	Low	
	R/W				SD0	– *2	High	Low	LSB
FF73H	SD7	SD6	SD5	SD4	SD7	– *2	High	Low	MSB
					SD6	– *2	High	Low	Serial I/F transmit/receive data (high-order 4 bits)
					SD5	– *2	High	Low	
	R/W				SD4	– *2	High	Low	LSB
FFE3H	0	0	0	EISIF	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R			R/W	0 *3	– *2			Unused
					EISIF	0	Enable	Mask	Interrupt mask register (Serial I/F)
FFF3H	0	0	0	ISIF	0 *3	– *2	(R)	(R)	Unused
					0 *3	– *2	Yes	No	Unused
	R			R/W	0 *3	– *2	(W)	(W)	Unused
					ISIF	0	Reset	Invalid	Interrupt factor flag (Serial I/F)

*1 Initial value at initial reset

*2 Not set in the circuit

*3 Constantly "0" when being read

ESIF: Serial interface enable register (P1 port function selection) (FF70H•D0)

Sets P10–P13 to the input/output port for the serial interface.

When "1" is written: Serial interface
When "0" is written: I/O port
Reading: Valid

When "1" is written to the ESIF register, P10, P11, P12 and P13 function as SIN, SOUT, $\overline{SCLK}$, $\overline{SRDY}$, respectively.
In the slave mode, the P13 terminal functions as $\overline{SRDY}$ output terminal, while in the master mode, it functions as the I/O port terminal.
At initial reset, this register is set to "0".

ESOUT: SOUT enable/disable control register (FF70H•D2)

Enables output of the SOUT signal.

When "1" is written: Enabled
When "0" is written: Disabled
Reading: Valid

When "1" is written to the ESOUT register, the SOUT terminal can output serial data. When "0" is written, the SOUT terminal goes high-impedance status.
At initial reset, this register is set to "0".

PUL10: SIN (P10) pull-up control register (FF45H•D0)
PUL12: $\overline{\text{SCLK}}$ (P12) pull-up control register (FF45H•D2)

Sets the pull-up of the SIN terminal and the $\overline{\text{SCLK}}$ terminals (in the slave mode).

When "1" is written: Pull-up ON
When "0" is written: Pull-up OFF
Reading: Valid

Sets the pull-up resistor built into the SIN (P10) and $\overline{\text{SCLK}}$ (P12) terminals to ON or OFF. (Pull-up resistor is only built in the port selected by mask option.)
$\overline{\text{SCLK}}$ pull-up is effective only in the slave mode. In the master mode, the PUL12 register can be used as a general purpose register.
At initial reset, these registers are set to "1" and pull-up goes ON.

SCS1, SCS0: Clock mode selection register (FF71H•D0, D1)

Selects the synchronous clock ($\overline{\text{SCLK}}$) for the serial interface.

Table 4.10.5.2 Synchronous clock selection

SCS1	SCS0	Mode	Synchronous clock
1	1	Master mode	OSC1
1	0		OSC1 /2
0	1		Programmable timer *
0	0	Slave mode	External clock *

* The clock frequency is limited to 1 MHz (max.).

Synchronous clock ($\overline{\text{SCLK}}$) is selected from among the above 4 types: 3 types of internal clock and external clock.
When the programmable timer is selected, the signal that is generated by dividing the underflow signal of the programmable timer (timer 1) in 1/2 is used as the synchronous clock. In this case, the programmable timer must be controlled before operating the serial interface. Refer to Section 4.9, "Programmable Timer" for the control of the programmable timer.
At initial reset, external clock is selected.

SCPS: Clock phase selection register (FF71H•D2)

Selects the timing for reading in the serial data input from the SIN (P10) terminal.

When "1" is written: Falling edge of $\overline{\text{SCLK}}$
When "0" is written: Rising edge of $\overline{\text{SCLK}}$
Reading: Valid

Select whether the fetching for the serial input data to registers (SD0–SD7) at the rising edge or falling edge of the synchronous signal.
Pay attention to the polarity of the synchronous clock selected by the mask option because the selection content is different.
The input data fetch timing may be selected but output timing for output data is fixed at the falling edge of $\overline{\text{SCLK}}$.
At initial reset, this register is set to "0".

SDP: Data input/output permutation selection register (FF71H•D3)

Selects the serial data input/output permutation.

When "1" is written: MSB first
When "0" is written: LSB first
Reading: Valid

Select whether the data input/output permutation will be MSB first or LSB first.
At initial reset, this register is set to "0".

SCTRG: Clock trigger/status (FF70H•D1)

This is a trigger to start input/output of synchronous clock ($\overline{SCLK}$).

• ***When writing***

When "1" is written: Trigger
When "0" is written: No operation

When this trigger is supplied to the serial interface activating circuit, the synchronous clock ($\overline{SCLK}$) input/output is started.
As a trigger condition, it is required that data writing or reading on data registers SD0–SD7 be performed prior to writing "1" to SCTRG. (The internal circuit of the serial interface is initiated through data writing/reading on data registers SD0–SD7.) In addition, be sure to enable the serial interface with the ESIF register before setting the trigger.
Supply trigger only once every time the serial interface is placed in the RUN state. Refrain from performing trigger input multiple times, as leads to malfunctioning.
Moreover, when the synchronous clock $\overline{SCLK}$ is external clock, start to input the external clock after the trigger.

• ***When reading***

When "1" is read: RUN (during input/output the synchronous clock)
When "0" is read: STOP (the synchronous clock stops)

When this bit is read, it indicates the status of serial interface clock.
After "1" is written to SCTRG, this value is latched till serial interface clock stops (8 clock counts). Therefore, if "1" is read, it indicates that the synchronous clock is in input/output operation.
When the synchronous clock input/output is completed, this latch is reset to "0".

At initial reset, this bit is set to "0".

SD0–SD3, SD4–SD7: Serial interface data register (FF72H, FF73H)

These registers are used for writing and reading serial data.

• ***When writing***

When "1" is written: High level
When "0" is written: Low level

Write data to be output in these registers. The register data is converted into serial data and output from the SOUT (P11) terminal; data bits set at "1" are output as high (V_{DD}) level and data bits set at "0" are output as low (V_{SS}) level.

• ***When reading***

When "1" is read: High level
When "0" is read: Low level

The serial data input from the SIN (P10) terminal can be read from these registers.
The serial data input from the SIN (P10) terminal is converted into parallel data, as a high (V_{DD}) level bit into "1" and as a low (V_{SS}) level bit into "0", and is loaded to these registers. Perform data reading only while the serial interface is not running (i.e., the synchronous clock is neither being input or output).

At initial reset, these registers are undefined.

EISIF: Interrupt mask register (FFE3H•D0)

Masking the interrupt of the serial interface can be selected with this register.

When "1" is written: Enabled
When "0" is written: Masked
Reading: Valid

With this register, it is possible to select whether the serial interface interrupt is to be masked or not.
At initial reset, this register is set to "0".

ISIF: Interrupt factor flag (FFF3H•D0)

This flag indicates the occurrence of serial interface interrupt.

When "1" is read: Interrupt has occurred
When "0" is read: Interrupt has not occurred

When "1" is written: Flag is reset
When "0" is written: Invalid

From the status of this flag, the software can decide whether the serial interface interrupt.
This flag is set to "1" after an 8-bit data input/output even if the interrupt is masked.
This flag is reset to "0" by writing "1" to it.
After an interrupt occurs, the same interrupt will occur again if the interrupt enabled state (I flag = "1") is set or the RETI instruction is executed unless the interrupt factor flag is reset. Therefore, be sure to reset (write "1" to) the interrupt factor flag in the interrupt service routine before shifting to the interrupt enabled state.
At initial reset, this flag is set to "0".

4.10.6 Programming notes

(1) Perform data writing/reading to the data registers SD0–SD7 only while the serial interface is not running (i.e., the synchronous clock is neither being input or output).

(2) As a trigger condition, it is required that data writing or reading on data registers SD0–SD7 be performed prior to writing "1" to SCTRG. (The internal circuit of the serial interface is initiated through data writing/reading on data registers SD0–SD7.) In addition, be sure to enable the serial interface with the ESIF register before setting the trigger.
Supply trigger only once every time the serial interface is placed in the RUN state. Refrain from performing trigger input multiple times, as leads to malfunctioning. Moreover, when the synchronous clock $\overline{\text{SCLK}}$ is external clock, start to input the external clock after the trigger.

(3) Setting of the input/output permutation (MSB first/LSB first) with the SDP register should be done before setting data to SD0–SD7.

(4) Be aware that the maximum clock frequency for the serial interface is limited to 1 MHz when OSC3 is used as the clock source of the programmable timer or in the slave mode.

(5) After an interrupt occurs, the same interrupt will occur again if the interrupt enabled state (I flag = "1") is set or the RETI instruction is executed unless the interrupt factor flag is reset. Therefore, be sure to reset (write "1" to) the interrupt factor flag in the interrupt service routine before shifting to the interrupt enabled state.

4.11 A/D Converter

4.11.1 Characteristics and configuration of A/D converter

The E0C63P366 has a built-in A/D converter with the following characteristics.

- Conversion method: Successive-approximation type
- Resolution: 8 bits
  Maximum error: ±3 LSB, A/D clock: OSC1, OSC3, V_{DD} = 2.7 V to 5.5 V
- Input channels: Maximum 4 channels
- Conversion time: Minimum 10.5 µsec (during operation at 2 MHz)
  Minimum 641 µsec (during operation at 32.768 kHz)
- Setting of analog conversion voltage range is possible with reference voltage terminal (AV_{REF})
- A/D conversion result is possible to read from 8-bit data register
- Sample & hold circuit built-in
- A/D conversion completion generates an interrupt

Figure 4.11.1.1 shows the configuration of the A/D converter.

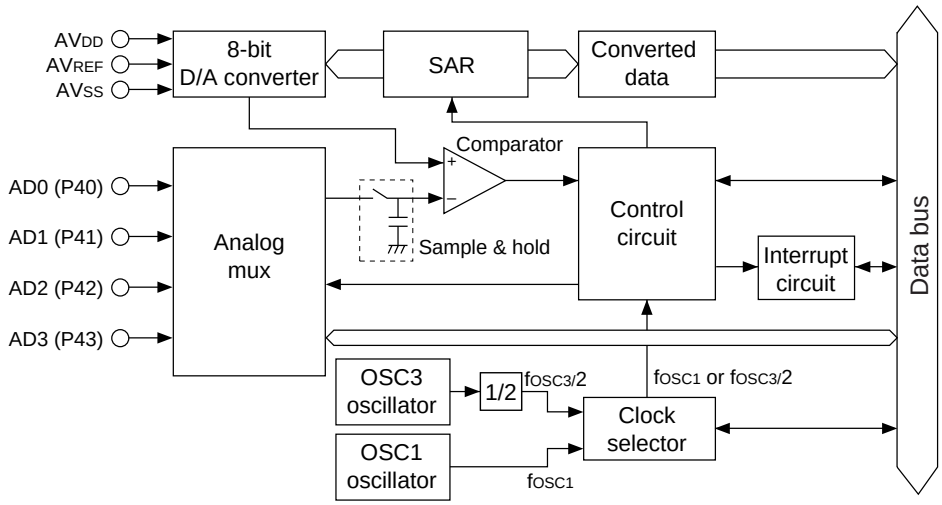


Fig. 4.11.1.1 Configuration of A/D converter

4.11.2 Terminal configuration of A/D converter

The terminals used with the A/D converter are as follows:

AVDD, AVSS (power supply terminal)

The AVDD and AVSS terminals are power supply terminals for the A/D converter. The voltage should be input as AVDD ≤ VDD and AVSS = VSS.

AVREF (reference voltage input terminal)

The AVREF terminal is the reference voltage terminal of the analog block. Input voltage range of the A/D conversion is decided by this input (AVSS–AVREF). The voltage should be input as AVREF ≤ AVDD.

AD0–AD3 (analog input terminal)

The analog input terminals AD0–AD3 are shared with the I/O port terminals P40–P43. Therefore, it is necessary to set them for the A/D converter by software when using them as analog input terminals. This setting can be done for each terminal. (Refer to Section 4.11.4 for setting.)
At initial reset, all the terminals are set in the I/O port terminals.
Analog voltage value AVIN that can be input is in the range of AVSS ≤ AVIN ≤ AVREF.

4.11.3 Mask option

The analog input terminals of the A/D converter are shared with the I/O port terminals P40–P43. Therefore, the terminal specification of the A/D converter is decided by setting the I/O port mask option. In the E0C63P366, the P40–P43 ports specification is fixed at "without pull-up resistor".

4.11.4 Control of A/D converter

(1) Setting of A/D input terminal

When using the A/D converter, it is necessary to set up the terminals used for analog input from the P40–P43 initialized as the I/O port terminals. Four terminals can all be used as analog input terminals.

The PAD (PAD0–PAD3) register is used to set analog input terminals. When the PAD register bits are set to "1", the corresponding terminals function as the analog input terminals.

At initial reset, these terminals are all set in the I/O port terminals, and each terminal goes to a high impedance.

Table 4.11.4.1 Correspondence between A/D input terminal and PAD register

Terminal	A/D input enable /disable	Comment
P40 (AD0)	PAD0	
P41 (AD1)	PAD1	
P42 (AD2)	PAD2	
P43 (AD3)	PAD3	

(2) Setting of input clock

The clock selector selects the A/D conversion clock from OSC1 or OSC3 according to the value written in the ADCLK register. Table 4.11.4.2 shows the input clock selection with the ADCLK register.

Table 4.11.4.2 Input clock selection

ADCLK	Clock source
0	OSC1
1	OSC3/2

The clock selector outputs the selected clock to the A/D converter by writing "1" to the ADRUN register.

Note:
- *Be sure to select (change) the input clock while the A/D converter is stopped. Changing the clock during A/D operation may cause problems.*
- *To prevent malfunction, do not start A/D conversion (writing "1" to the ADRUN register) when the A/D conversion clock is not being output from the clock selector, and do not turn the clock off during A/D conversion.*

(3) Input signal selection

The analog signals from the AD0 (P40)–AD3 (P43) terminals are input to the multiplexer, and the analog input channel for A/D conversion is selected by software. This selection can be done using the CHS register as shown in Table 4.11.4.3.

Table 4.11.4.3 Selection of analog input channel

CHS1	CHS0	Input channel
1	1	AD3 (P43)
1	0	AD2 (P42)
0	1	AD1 (P41)
0	0	AD0 (P40)

(4) A/D conversion operation

An A/D conversion starts by writing "1" to the ADRUN register (FFD0H•D3).
For example, when performing A/D conversion using AD1 as the analog input, write "1" (0, 1) to the CHS register (CHS1, CHS0). However, it is necessary that the P41 terminal has been set as an analog input terminal. Then write "1" to the ADRUN register. The A/D converter starts converting of the analog signal input to the AD1 terminal.

The built-in sample/hold circuit starts sampling of the analog input specified from t_{AD} after writing. When the sampling is completed, the held analog input voltage is converted into a 8-bit digital value in successive-approximation architecture.
The conversion result is loaded into the ADDR (ADDR0–ADDR7) register. ADDR0 is the LSB and ADDR7 is the MSB.

Note: If the CHS register selects an input channel which is not included in the analog input terminals set by the PAD register (the PAD register can select several terminals simultaneously), the A/D conversion does not result in a correct converted value.

Example)
Terminal setting: PAD3 = 1, PAD2–PAD0 = 0 (AD3 terminal is used)
Selection of input channel: CHS1 = 0, CHS0 = 0 (AD0 is selected)
In a setting like this, the A/D conversion result will be invalid because the contents of the settings are not matched.

Figure 4.11.4.1 shows the flow chart for starting an A/D conversion.

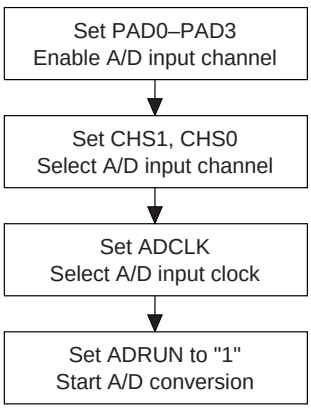


Fig. 4.11.4.1 Flowchart for starting A/D conversion

An A/D conversion is completed when the conversion result is loaded into the ADDR register. At that point, the A/D converter generates an interrupt (explained in the next section).
Figure 4.11.4.2 shows the timing chart of A/D conversion.

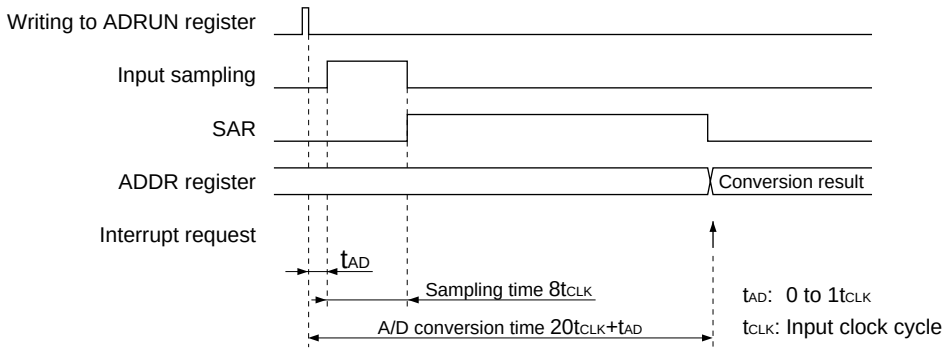


Fig. 4.11.4.2 Timing chart of A/D conversion

4.11.5 Interrupt function

The A/D converter can generate an interrupt when an A/D conversion has completed.
Figure 4.11.5.1 shows the configuration of the A/D converter interrupt circuit.

The A/D converter sets the interrupt factor flag IAD to "1" immediately after storing the conversion result to the ADDR register.
At this time, if the interrupt mask register EIAD is "1" , an interrupt is generated to the CPU.
By setting the EIAD register to "0", the interrupt to the CPU can be disabled. However, the interrupt factor flag is set to "1" when an A/D conversion has completed regardless of the interrupt mask register setting.
The interrupt factor flag set in "1" is reset to "0" by writing "1".

The interrupt vector for the A/D conversion completion has been set in 010EH.

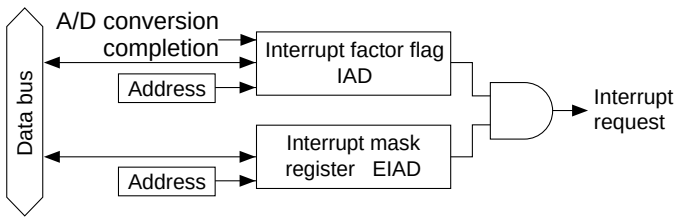


Fig. 4.11.5.1 Configuration of A/D converter interrupt circuit

4.11.6 I/O memory of A/D converter

Table 4.11.6.1 shows the I/O addresses and the control bits for the A/D converter.

Table 4.11.6.1 Control bits of A/D converter

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
FF01H	VADSEL	VDSEL	0	DBON	VADSEL	0	(V_{C2})	(V_{DD})	(Power source selection for A/D converter)
					VDSEL	0	(V_{C2})	(V_{DD})	(Power source selection for oscillation system voltage regulator)
	R/W		R	R/W	0 *3	– *2			Unused
					DBON	0	(On)	(Off)	(Voltage doubler On/Off)
FFD0H	ADRUN	ADCLK	CHS1	CHS0	ADRUN	0	Start	Invalid	A/D Run/Off control
					ADCLK	0	OSC3	OSC1	A/D input clock selection
	W	R/W			CHS1	0			A/D input channel selection [CHS1, 0]: 0 / 1 / 2 / 3 — Input channel: P40 / P41 / P42 / P43
					CHS0	0			
FFD1H	PAD3	PAD2	PAD1	PAD0	PAD3	0	Enable	Disable	P43 input channel enable/disable control
					PAD2	0	Enable	Disable	P42 input channel enable/disable control
	R/W				PAD1	0	Enable	Disable	P41 input channel enable/disable control
					PAD0	0	Enable	Disable	P40 input channel enable/disable control
FFD2H	ADDR3	ADDR2	ADDR1	ADDR0	ADDR3	– *2			A/D converted data (D0–D3)
					ADDR2	– *2			
	R				ADDR1	– *2			
					ADDR0	– *2			
FFD3H	ADDR7	ADDR6	ADDR5	ADDR4	ADDR7	– *2			A/D converted data (D4–D7)
					ADDR6	– *2			
	R				ADDR5	– *2			
					ADDR4	– *2			
FFE7H	0	0	0	EIAD	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R			R/W	0 *3	– *2			Unused
					EIAD	0	Enable	Mask	Interrupt mask register (A/D converter)
FFF7H	0	0	0	IAD	0 *3	– *2	(R)	(R)	Unused
					0 *3	– *2	Yes	No	Unused
	R			R/W	0 *3	– *2	(W)	(W)	Unused
					IAD	0	Reset	Invalid	Interrupt factor flag (A/D converter)

*1 Initial value at initial reset

*2 Not set in the circuit

*3 Constantly "0" when being read

PAD0–PAD3: A/D converter input control register (FFD1H)

Sets the P40–P43 terminals as the analog input terminals for the A/D converter.

When "1" is written: A/D converter input
When "0" is written: I/O port
Reading: Valid

When "1" is written to PADn, the P4n terminal is set to the analog input terminal ADn. (n = 0–3)
When "0" is written, the terminal is used with the I/O port.
At initial reset, this register is set to "0" (I/O port).

ADCLK: A/D converter clock source selection register (FFD0H•D2)

Selects the clock source for the A/D converter.

When "1" is written: OSC3
When "0" is written: OSC1
Reading: Valid

When "1" is written to ADCLK, OSC3 is selected as the clock source for the A/D converter.
When "0" is written, OSC1 is selected.
At initial reset, this register is set to "0" (OSC1).

CHS0, CHS1: Analog input channel selection register (FFD0H•D0, D1)

Selects an analog input channel.

Table 4.11.6.2 Selection of analog input channel

CHS1	CHS0	Input channel
1	1	AD3 (P43)
1	0	AD2 (P42)
0	1	AD1 (P41)
0	0	AD0 (P40)

At initial reset, this register is set to "0" (AD0).

VADSEL: A/D power source selection register (FF01H•D3)

In the E0C63P366, the value set in this register does not affect the operating mode (operating voltage) of the A/D converter. However, when using the E0C63P366 as a development tool for the E0C63358/63158, control the operating voltage using this register according to the control sequence of the model (refer to the "Technical Manual").
At initial reset, this register is set to "0" (VDD).

ADRUN: A/D conversion control (FFD0H•D3)

Starts an A/D conversion.

When "1" is written: Start
When "0" is written: No operation
Reading: Invalid

When "1" is written to ADRUN, the A/D converter starts A/D conversion of the channel selected by the CHS register and stores the conversion result to the ADDR register.
At initial reset, this bit is set to "0".

ADDR0–ADDR7: A/D conversion result (FFD2H/lower 4 bits, FFD3H/upper 4 bits)

A/D conversion result is stored.
ADDR0 is the LSB and ADDR7 is the MSB.
At initial reset, data is undefined.

EIAD: A/D converter interrupt mask register (FFE7H•D0)

This register is used to select whether to mask the A/D converter interrupt or not.

When "1" is written: Enabled
When "0" is written: Masked
Reading: Valid

Writing "1" to the EIAD register enables the A/D converter interrupt and writing "0" disables the interrupt.
At initial reset, this register is set to "0".

IAD: A/D converter interrupt factor flag (FFF7H•D0)

This flag indicates the status of the A/D converter interrupt.

When "1" is read: Interrupt has occurred
When "0" is read: Interrupt has not occurred

When "1" is written: Flag is reset
When "0" is written: Invalid

IAD is the A/D converter interrupt factor flag that is set when an A/D conversion has finished. The software can judge from this flag whether there is an A/D converter interrupt or not. This flag is set to "1" even if the interrupt is masked.
This flag is reset to "0" by writing "1".
After an interrupt occurs, the same interrupt will occur again if the interrupt enabled state (I flag = "1") is set or the RETI instruction is executed unless the interrupt factor flag is reset. Therefore, be sure to reset (write "1" to) the interrupt factor flag in the interrupt service routine before shifting to the interrupt enabled state.
At initial reset, this flag is set to "0".

4.11.7 Programming notes

(1) The A/D converter can operate by inputting the clock from the clock selector. Therefore, it is necessary to select the clock source and to turn the clock output on before starting A/D conversion. Furthermore, it is also necessary that the OSC3 oscillation circuit is operating when using the OSC3 clock.

(2) When using the OSC3 clock as the A/D conversion clock, do not stop the OSC3 oscillation circuit during A/D conversion. If the OSC3 oscillation circuit stops, correct A/D conversion result cannot be obtained.

(3) The input clock and analog input terminals should be set when the A/D converter stops. Changing these settings in the A/D converter operation may cause errors.

(4) To prevent malfunction, do not start A/D conversion (writing "1" to the ADRUN register) when the A/D conversion clock is not being output from the clock selector, and do not turn the clock off during A/D conversion.

(5) If the CHS register selects an input channel which is not included in the analog input terminals set by the PAD register (the PAD register can select several terminals simultaneously), the A/D conversion does not result in a correct converted value.

(6) During A/D conversion, do not operate the P4n terminals which are not used for analog inputs of the A/D converter (for input/output of digital signals). It affects the A/D conversion precision.

(7) In the E0C63P366, the value set in the VADSEL register does not affect the operating mode (operating voltage) of the A/D converter. However, when using the E0C63P366 as a development tool for the E0C63358/63158, control the operating voltage using the VADSEL register according to the control sequence of the model (refer to the "Technical Manual").

4.12 Buzzer Output Circuit

4.12.1 Configuration of buzzer output circuit

The E0C63P366 is capable of generating buzzer signal to drive a piezo-electric buzzer. The buzzer signal is output from the BZ terminal by software control. Furthermore, the buzzer signal frequency can be set to 2 kHz or 4 kHz with 2 Hz interval by software.
Figure 4.12.1.1 shows the configuration of the buzzer output circuit.

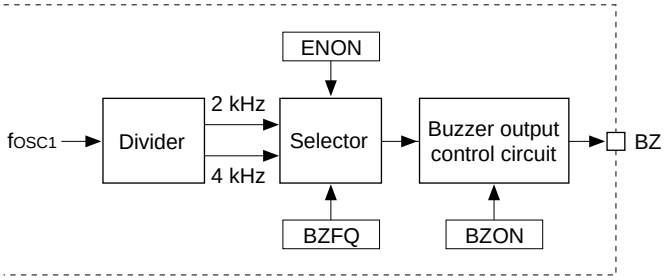


Fig. 4.12.1.1 Configuration of buzzer output circuit

4.12.2 Mask option

In the E0C63P366, polarity of the buzzer signal output from the BZ terminal is fixed at negative polarity. The BZ terminal goes to a high (VDD) level when the buzzer signal is not output. Drive a piezo buzzer by externally connecting an PNP transistor.

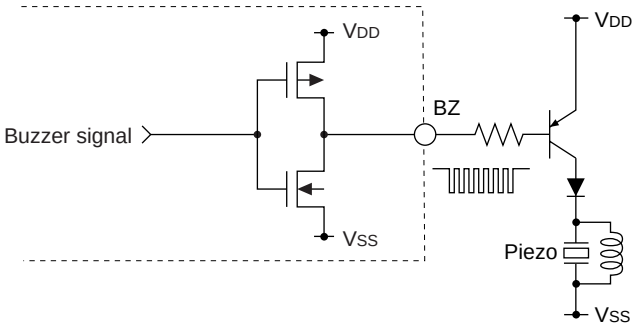


Fig. 4.12.2.1 Configuration of output circuit

4.12.3 Control of buzzer output

The buzzer signal frequency is selected by the buzzer frequency selection register BZFQ. When "1" is written to the BZFQ register, the frequency is set to 2 kHz. When "0" is written, it is set to 4 kHz. This signal is generated by dividing the fOSC1.

fOSC1	2 kHz	4 kHz
32.768 kHz	fOSC1 /16	fOSC1 /8

The buzzer signal is output from the BZ terminal by writing "1" to the buzzer output control register BZON. The BZ terminal goes to a high (VDD) level by writing "0".

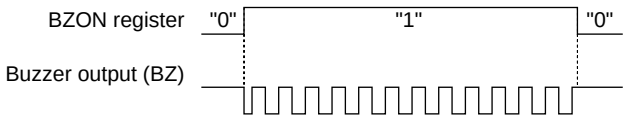


Fig. 4.12.3.1 Timing chart of buzzer signal output

2 Hz intervals can be added to the buzzer signal when "1" is written to the ENON register.

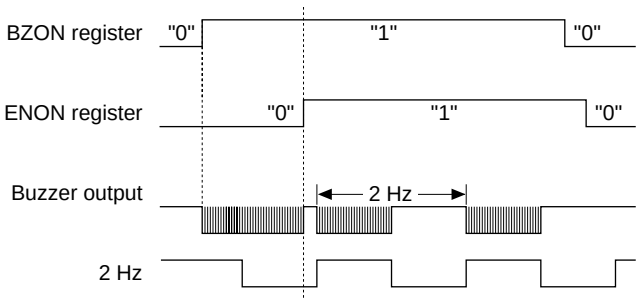


Fig. 4.12.3.2 2 Hz interval

Note: Since it generates a buzzer signal that is out of synchronization with the BZON register, hazards may at times be produced when the signal goes ON/OFF due to the setting of the BZON register.

4.12.4 I/O memory of buzzer output circuit

Table 4.12.4.1 shows the I/O address and the control bits for the buzzer output circuit.

Table 4.12.4.1 Control bits of buzzer output circuit

Address	Register								Comment
	D3	D2	D1	D0	Name	Init *1	1	0	
FF64H	0	ENON	BZFQ	BZON	0 *3	– *2			Unused
					ENON	0	On	Off	2 Hz interval On/Off
	R	R/W			BZFQ	0	2 kHz	4 kHz	Buzzer frequency selection
					BZON	0	On	Off	Buzzer output On/Off

*1 Initial value at initial reset

*2 Not set in the circuit

*3 Constantly "0" when being read

ENON: Interval ON/OFF control register (FF64H•D2)

Controls the addition of a 2 Hz interval onto the buzzer signal.

When "1" is written: ON
When "0" is written: OFF
Reading: Valid

Writing "1" into the ENON causes a 2 Hz ON/OFF interval to be added during buzzer signal output. When "0" has been written, a 2 Hz ON/OFF interval is not added.
At initial reset, this register is set to "0".

BZFQ: Buzzer frequency selection register (FF64H•D1)

Selects the buzzer signal frequency.

When "1" is written: 2 kHz
When "0" is written: 4 kHz
Reading: Valid

When "1" is written to BZFQ, the frequency is set to 2 kHz. When "0" is written, it is set to 4 kHz.
At initial reset, this register is set to "0".

BZON: Buzzer output control (ON/OFF) register (FF64H•D0)

Controls the buzzer signal output.

When "1" is written: Buzzer output ON
When "0" is written: Buzzer output OFF
Reading: Valid

When "1" is written to BZON, the buzzer signal is output from the BZ terminal. When "0" is written, the BZ terminal goes to a high (V_{DD}) level.
At initial reset, this register is set to "0".

4.12.5 Programming note

Since it generates a buzzer signal that is out of synchronization with the BZON register, hazards may at times be produced when the signal goes ON/OFF due to the setting of the BZON register.

4.13 SVD (Supply Voltage Detection) Circuit

4.13.1 Configuration of SVD circuit

The E0C63P366 has a built-in SVD (supply voltage detection) circuit, so that the software can find when the source voltage lowers. Turning the SVD circuit ON/OFF and the SVD criteria voltage setting can be done with software.
Figure 4.13.1.1 shows the configuration of the SVD circuit.

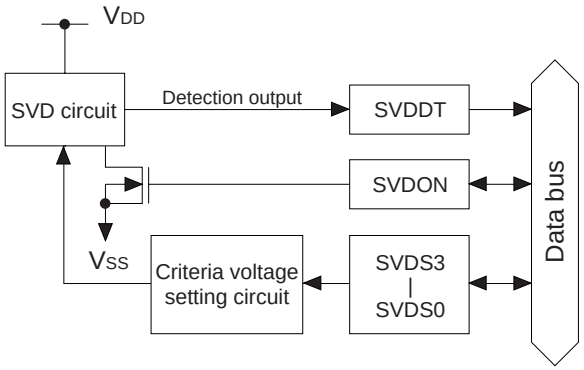


Fig. 4.13.1.1 Configuration of SVD circuit

4.13.2 SVD operation

The SVD circuit compares the criteria voltage set by software and the supply voltage (V_{DD}–V_{SS}) and sets its results into the SVDDT latch. By reading the data of this SVDDT latch, it can be determined by means of software whether the supply voltage is normal or has dropped.
The criteria voltage can be set for the 2 types shown in Table 4.13.2.1 by the SVDS3–SVDS0 registers.

Table 4.13.2.1 Criteria voltage setting

SVDS3	SVDS2	SVDS1	SVDS0	Criteria voltage (V)
0	1	1	1	Not allowed
0	1	1	0	Not allowed
0	1	0	1	Not allowed
0	1	0	0	Not allowed
0	0	1	1	Not allowed
0	0	1	0	Not allowed
0	0	0	1	Not allowed
0	0	0	0	Not allowed

SVDS3	SVDS2	SVDS1	SVDS0	Criteria voltage (V)
1	1	1	1	2.80
1	1	1	0	2.70
1	1	0	1	Not allowed
1	1	0	0	Not allowed
1	0	1	1	Not allowed
1	0	1	0	Not allowed
1	0	0	1	Not allowed
1	0	0	0	Not allowed

Be aware that the SVD circuit in the E0C63P366 does not operate properly if the SVDS register is set to 13 or less, the SVD operation cannot be guaranteed since the lower limit of the operating voltage is 2.7 V.
When the SVDON register is set to "1", source voltage detection by the SVD circuit is executed. As soon as the SVDON register is reset to "0", the result is loaded to the SVDDT latch and the SVD circuit goes OFF. To obtain a stable detection result, the SVD circuit must be ON for at least l00 µsec. So, to obtain the SVD detection result, follow the programming sequence below.

1. Set SVDON to "1"
2. Maintain for 100 µsec minimum
3. Set SVDON to "0"
4. Read SVDDT

When the SVD circuit is ON, the IC draws a large current, so keep the SVD circuit off unless it is.

4.13.3 I/O memory of SVD circuit

Table 4.13.3.1 shows the I/O addresses and the control bits for the SVD circuit.

Table 4.13.3.1 Control bits of SVD circuit

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
FF04H	SVDS3	SVDS2	SVDS1	SVDS0	SVDS3	0			SVD criteria voltage setting
					SVDS2	0			[SVDS3–0] 0 1 2 3 4 5 6 7
	R/W				SVDS1	0			Voltage(V) – – – – – – – –
					SVDS0	0			[SVDS3–0] 8 9 10 11 12 13 14 15
									Voltage(V) – – – – – – 2.70 2.80
FF05H	0	0	SVDDT	SVDON	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R			R/W	SVDDT	0	Low	Normal	SVD evaluation data
					SVDON	0	On	Off	SVD circuit On/Off

*1 Initial value at initial reset

*2 Not set in the circuit

*3 Constantly "0" when being read

SVDS3–SVDS0: SVD criteria voltage setting register (FF04H)

Criteria voltage for SVD is set as shown in Table 4.13.2.1.
At initial reset, this register is set to "0".

SVDON: SVD control (ON/OFF) register (FF05H•D0)

Turns the SVD circuit ON and OFF.

When "1" is written: SVD circuit ON
When "0" is written: SVD circuit OFF
Reading: Valid

When the SVDON register is set to "1", a source voltage detection is executed by the SVD circuit. As soon as SVDON is reset to "0", the result is loaded to the SVDDT latch. To obtain a stable detection result, the SVD circuit must be ON for at least l00 µsec.
At initial reset, this register is set to "0".

SVDDT: SVD data (FF05H•D1)

This is the result of supply voltage detection.

When "0" is read: Supply voltage (V_{DD}–V_{SS}) ≥ Criteria voltage
When "1" is read: Supply voltage (V_{DD}–V_{SS}) < Criteria voltage
Writing: Invalid

The result of supply voltage detection at time of SVDON is set to "0" can be read from this latch.
At initial reset, SVDDT is set to "0".

4.13.4 Programming notes

(1) To obtain a stable detection result, the SVD circuit must be ON for at least l00 µsec. So, to obtain the SVD detection result, follow the programming sequence below.

1. Set SVDON to "1"
2. Maintain for 100 µsec minimum
3. Set SVDON to "0"
4. Read SVDDT

(2) The SVD circuit should normally be turned OFF because SVD operation increase current consumption.

(3) Be aware that the SVD circuit in the E0C63P366 does not operate properly if the SVDS register is set to 13 or less, the SVD operation cannot be guaranteed since the lower limit of the operating voltage is 2.7 V.

4.14 Interrupt and HALT

<Interrupt types>

The E0C63P366 provides the following interrupt functions.

External interrupt:	• Input interrupt	(3 systems)
Internal interrupt:	• Watchdog timer interrupt	(NMI, 1 system)
	• Programmable timer interrupt	(2 systems)
	• Serial interface interrupt	(1 system)
	• Timer interrupt	(4 systems)
	• A/D converter interrupt	(1 system)

To authorize interrupt, the interrupt flag must be set to "1" (EI) and the necessary related interrupt mask registers must be set to "1" (enable).
When an interrupt occurs the interrupt flag is automatically reset to "0" (DI), and interrupts after that are inhibited.

The watchdog timer interrupt is an NMI (non-maskable interrupt), therefore, the interrupt is generated regardless of the interrupt flag setting. Also the interrupt mask register is not provided. However, it is possible to not generate NMI since software can stop the watchdog timer operation.

Figure 4.14.1 shows the configuration of the interrupt circuit.

Note: After an initial reset, all the interrupts including NMI are masked until both the stack pointers SP1 and SP2 are set with the software. Be sure to set the SP1 and SP2 in the initialize routine. Further, when re-setting the stack pointer, the SP1 and SP2 must be set as a pair. When one of them is set, all the interrupts including NMI are masked and interrupts cannot be accepted until the other one is set.

<HALT>

The E0C63P366 has HALT functions that considerably reduce the current consumption when it is not necessary.
The CPU enters HALT status when the HALT instruction is executed.
In HALT status, the operation of the CPU is stopped. However, timers continue counting since the oscillation circuit operates. Reactivating the CPU from HALT status is done by generating a hardware interrupt request including NMI.

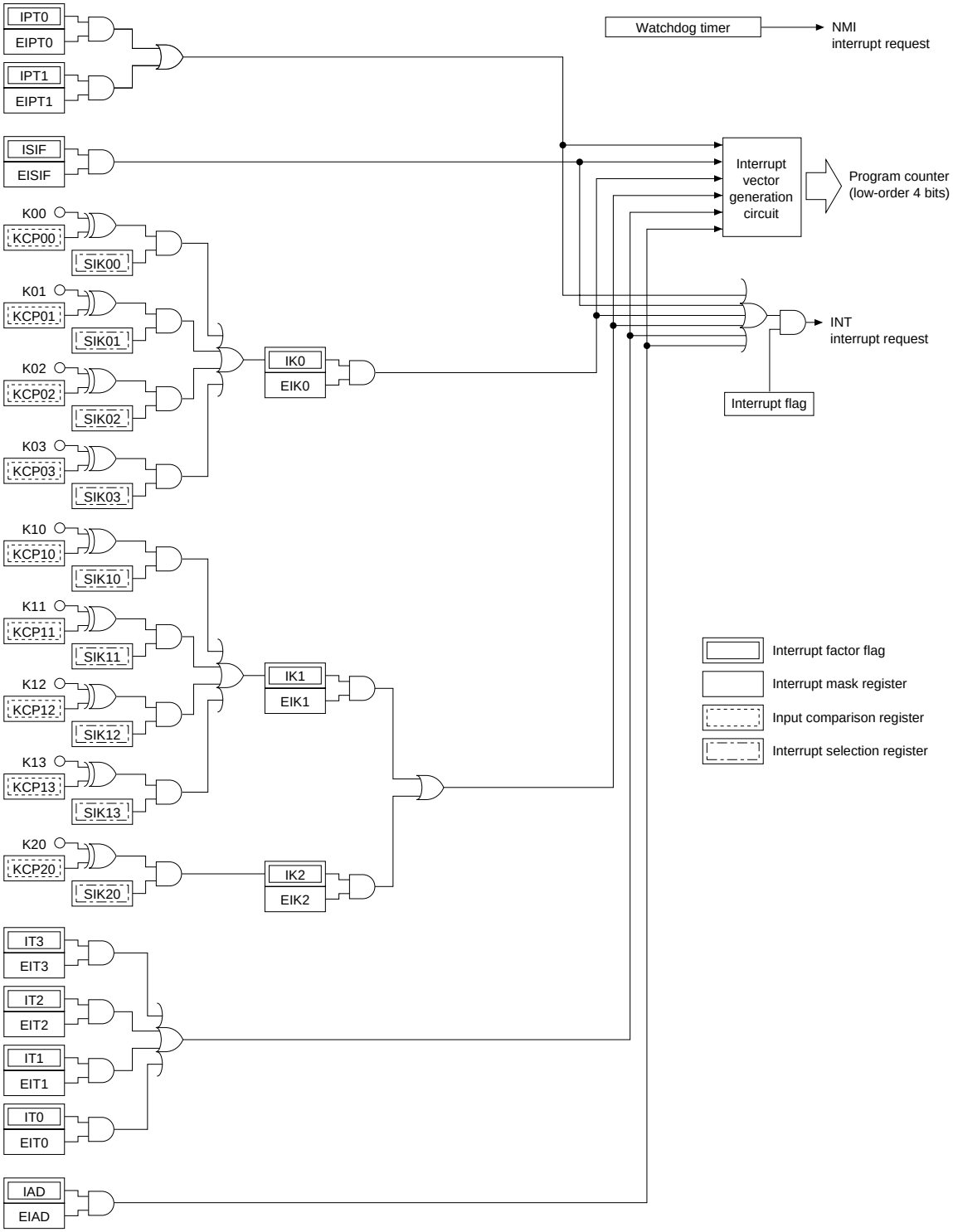


Fig. 4.14.1 Configuration of the interrupt circuit

4.14.1 Interrupt factor

Table 4.14.1.1 shows the factors for generating interrupt requests.

The interrupt flags are set to "1" depending on the corresponding interrupt factors.
The CPU operation is interrupted when an interrupt factor flag is set to "1" if the following conditions are established.

- The corresponding mask register is "1" (enabled)
- The interrupt flag is "1" (EI)

The interrupt factor flag is reset to "0" when "1" is written.
At initial reset, the interrupt factor flags are reset to "0".

* Since the watchdog timer's interrupt is NMI, the interrupt is generated regardless of the setting above, and no interrupt factor flag is provided.

Table 4.14.1.1 Interrupt factors

Interrupt factor	Interrupt factor flag	
Programmable timer 1 (counter = 0)	IPT1	(FFF2H•D1)
Programmable timer 0 (counter = 0)	IPT0	(FFF2H•D0)
Serial interface (8-bit data input/output completion)	ISIF	(FFF3H•D0)
K00–K03 input (falling edge or rising edge)	IK0	(FFF4H•D0)
K10–K13 input (falling edge or rising edge)	IK1	(FFF5H•D0)
K20 input (falling edge or rising edge)	IK2	(FFF5H•D1)
Clock timer 1 Hz (falling edge)	IT3	(FFF6H•D3)
Clock timer 2 Hz (falling edge)	IT2	(FFF6H•D2)
Clock timer 8 Hz (falling edge)	IT1	(FFF6H•D1)
Clock timer 16 Hz (falling edge)	IT0	(FFF6H•D0)
A/D converter	IAD	(FFF7H•D0)

Note: After an interrupt occurs, the same interrupt will occur again if the interrupt enabled state (I flag = "1") is set or the RETI instruction is executed unless the interrupt factor flag is reset. Therefore, be sure to reset (write "1" to) the interrupt factor flag in the interrupt service routine before shifting to the interrupt enabled state.

4.14.2 Interrupt mask

The interrupt factor flags can be masked by the corresponding interrupt mask registers.
The interrupt mask registers are read/write registers. They are enabled (interrupt authorized) when "1" is written to them, and masked (interrupt inhibited) when "0" is written to them.
At initial reset, the interrupt mask register is set to "0".
Table 4.14.2.1 shows the correspondence between interrupt mask registers and interrupt factor flags.

Table 4.14.2.1 Interrupt mask registers and interrupt factor flags

Interrupt mask register		Interrupt factor flag	
EIPT1	(FFE2H•D1)	IPT1	(FFF2H•D1)
EIPT0	(FFE2H•D0)	IPT0	(FFF2H•D0)
EISIF	(FFE3H•D0)	ISIF	(FFF3H•D0)
EIK0	(FFE4H•D0)	IK0	(FFF4H•D0)
EIK1	(FFE5H•D0)	IK1	(FFF5H•D0)
EIK2	(FFE5H•D1)	IK2	(FFF5H•D1)
EIT3	(FFE6H•D3)	IT3	(FFF6H•D3)
EIT2	(FFE6H•D2)	IT2	(FFF6H•D2)
EIT1	(FFE6H•D1)	IT1	(FFF6H•D1)
EIT0	(FFE6H•D0)	IT0	(FFF6H•D0)
EIAD	(FFE7H•D0)	IAD	(FFF7H•D0)

4.14.3 Interrupt vector

When an interrupt request is input to the CPU, the CPU begins interrupt processing. After the program being executed is terminated, the interrupt processing is executed in the following order.

1 The content of the flag register is evacuated, then the I flag is reset.

2 The address data (value of program counter) of the program to be executed next is saved in the stack area (RAM).

3 The interrupt request causes the value of the interrupt vector (0100H–010EH) to be set in the program counter.

4 The program at the specified address is executed (execution of interrupt processing routine by software).

Table 4.14.3.1 shows the correspondence of interrupt requests and interrupt vectors.

Table 4.14.3.1 Interrupt request and interrupt vectors

Interrupt vector	Interrupt factor	Priority
0100H	Watchdog timer	High
0104H	Programmable timer	↑
0106H	Serial interface	
0108H	K00–K03 input	
010AH	K10–K13 input, K20 input	
010CH	Clock timer	↓
010EH	A/D converter	Low

The four low-order bits of the program counter are indirectly addressed through the interrupt request.

4.14.4 I/O memory of interrupt

Tables 4.14.4.1(a) and (b) show the I/O addresses and the control bits for controlling interrupts.

Table 4.14.4.1(a) Control bits of interrupt (1)

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
FF20H	SIK03	SIK02	SIK01	SIK00	SIK03	0	Enable	Disable	K00–K03 interrupt selection register
					SIK02	0	Enable	Disable	
	R/W				SIK01	0	Enable	Disable	
					SIK00	0	Enable	Disable	
FF22H	KCP03	KCP02	KCP01	KCP00	KCP03	1	↓	↑	K00–K03 input comparison register
					KCP02	1	↓	↑	
	R/W				KCP01	1	↓	↑	
					KCP00	1	↓	↑	
FF24H	SIK13	SIK12	SIK11	SIK10	SIK13	0	Enable	Disable	K10–K13 interrupt selection register
					SIK12	0	Enable	Disable	
	R/W				SIK11	0	Enable	Disable	
					SIK10	0	Enable	Disable	
FF26H	KCP13	KCP12	KCP11	KCP10	KCP13	1	↓	↑	K10–K13 input comparison register
					KCP12	1	↓	↑	
	R/W				KCP11	1	↓	↑	
					KCP10	1	↓	↑	
FF28H	0	0	0	SIK20	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R			R/W	0 *3	– *2			Unused
					SIK20	0	Enable	Disable	K20 interrupt selection register
FF2AH	0	0	0	KCP20	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R			R/W	0 *3	– *2			Unused
					KCP20	1	↓	↑	K20 input comparison register
FFE2H	0	0	EIPT1	EIPT0	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R		R/W		EIPT1	0	Enable	Mask	Interrupt mask register (Programmable timer 1)
					EIPT0	0	Enable	Mask	Interrupt mask register (Programmable timer 0)
FFE3H	0	0	0	EISIF	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R			R/W	0 *3	– *2			Unused
					EISIF	0	Enable	Mask	Interrupt mask register (Serial I/F)
FFE4H	0	0	0	EIK0	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R			R/W	0 *3	– *2			Unused
					EIK0	0	Enable	Mask	Interrupt mask register (K00–K03)
FFE5H	0	0	EIK2	EIK1	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R		R/W		EIK2	0	Enable	Mask	Interrupt mask register (K20)
					EIK1	0	Enable	Mask	Interrupt mask register (K10–K13)
FFE6H	EIT3	EIT2	EIT1	EIT0	EIT3	0	Enable	Mask	Interrupt mask register (Clock timer 1 Hz)
					EIT2	0	Enable	Mask	Interrupt mask register (Clock timer 2 Hz)
	R/W				EIT1	0	Enable	Mask	Interrupt mask register (Clock timer 8 Hz)
					EIT0	0	Enable	Mask	Interrupt mask register (Clock timer 16 Hz)
FFE7H	0	0	0	EIAD	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R			R/W	0 *3	– *2			Unused
					EIAD	0	Enable	Mask	Interrupt mask register (A/D converter)

*1 Initial value at initial reset

*2 Not set in the circuit

*3 Constantly "0" when being read

Table 4.14.4.1(b) Control bits of interrupt (2)

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
FFF2H	0	0	IPT1	IPT0	0 *3	– *2	(R)	(R)	Unused
					0 *3	– *2	Yes	No	Unused
	R		R/W		IPT1	0	(W)	(W)	Interrupt factor flag (Programmable timer 1)
					IPT0	0	Reset	Invalid	Interrupt factor flag (Programmable timer 0)
FFF3H	0	0	0	ISIF	0 *3	– *2	(R)	(R)	Unused
					0 *3	– *2	Yes	No	Unused
	R			R/W	0 *3	– *2	(W)	(W)	Unused
					ISIF	0	Reset	Invalid	Interrupt factor flag (Serial I/F)
FFF4H	0	0	0	IK0	0 *3	– *2	(R)	(R)	Unused
					0 *3	– *2	Yes	No	Unused
	R			R/W	0 *3	– *2	(W)	(W)	Unused
					IK0	0	Reset	Invalid	Interrupt factor flag (K00–K03)
FFF5H	0	0	IK2	IK1	0 *3	– *2	(R)	(R)	Unused
					0 *3	– *2	Yes	No	Unused
	R		R/W		IK2	0	(W)	(W)	Interrupt factor flag (K20)
					IK1	0	Reset	Invalid	Interrupt factor flag (K10–K13)
FFF6H	IT3	IT2	IT1	IT0	IT3	0	(R)	(R)	Interrupt factor flag (Clock timer 1 Hz)
					IT2	0	Yes	No	Interrupt factor flag (Clock timer 2 Hz)
	R/W				IT1	0	(W)	(W)	Interrupt factor flag (Clock timer 8 Hz)
					IT0	0	Reset	Invalid	Interrupt factor flag (Clock timer 16 Hz)
FFF7H	0	0	0	IAD	0 *3	– *2	(R)	(R)	Unused
					0 *3	– *2	Yes	No	Unused
	R			R/W	0 *3	– *2	(W)	(W)	Unused
					IAD	0	Reset	Invalid	Interrupt factor flag (A/D converter)

*1 Initial value at initial reset

*2 Not set in the circuit

*3 Constantly "0" when being read

EIPT1, EIPT0: Interrupt mask registers (FFE2H•D1, D0)
IPT1, IPT0: Interrupt factor flags (FFF2H•D1, D0)
Refer to Section 4.9, "Programmable Timer".

EISIF: Interrupt mask register (FFE3H•D0)
ISIF: Interrupt factor flag (FFF3H•D0)
Refer to Section 4.10, "Serial Interface".

KCP03–KCP00, KCP13–KCP10, KCP20: Input comparison registers (FF22H, FF26H, FF2AH•D0)
SIK03–SIK00, SIK13–SIK10, SIK20: Interrupt selection registers (FF20H, FF24H, FF28H•D0)
EIK0, EIK1, EIK2: Interrupt mask registers (FFE4H•D0, FFE5H•D0, FFE5H•D1)
IK0, IK1, IK2: Interrupt factor flags (FFF4H•D0, FFF5H•D0, FFF5H•D1)
Refer to Section 4.4, "Input Ports".

EIT3–EIT0: Interrupt mask registers (FFE6H)
IT3–IT0: Interrupt factor flags (FFF6H)
Refer to Section 4.8, "Clock Timer".

EIAD: Interrupt mask register (FFE7H•D0)
IAD: Interrupt factor flag (FFF7H•D0)
Refer to Section 4.11, "A/D Converter".

4.14.5 Programming notes

(1) The interrupt factor flags are set when the interrupt condition is established, even if the interrupt mask registers are set to "0".

(2) After an interrupt occurs, the same interrupt will occur again if the interrupt enabled state (I flag = "1") is set or the RETI instruction is executed unless the interrupt factor flag is reset. Therefore, be sure to reset (write "1" to) the interrupt factor flag in the interrupt service routine before shifting to the interrupt enabled state.

(3) After an initial reset, all the interrupts including NMI are masked until both the stack pointers SP1 and SP2 are set with the software. Be sure to set the SP1 and SP2 in the initialize routine.
Further, when re-setting the stack pointer, the SP1 and SP2 must be set as a pair. When one of them is set, all the interrupts including NMI are masked and interrupts cannot be accepted until the other one is set.

CHAPTER 5 PROM PROGRAMMING AND OPERATING MODE

The E0C63P366 has built-in Flash EEPROMs as the code ROM and the segment option ROM that allow the developer to program the ROM data using the exclusive PROM writer (Universal ROM Writer II). This chapter explains the PROM programmer that controls data writing and the writing mode.

5.1 Configuration of PROM Programmer

The configuration of the PROM programmer is shown in Figure 5.1.1.

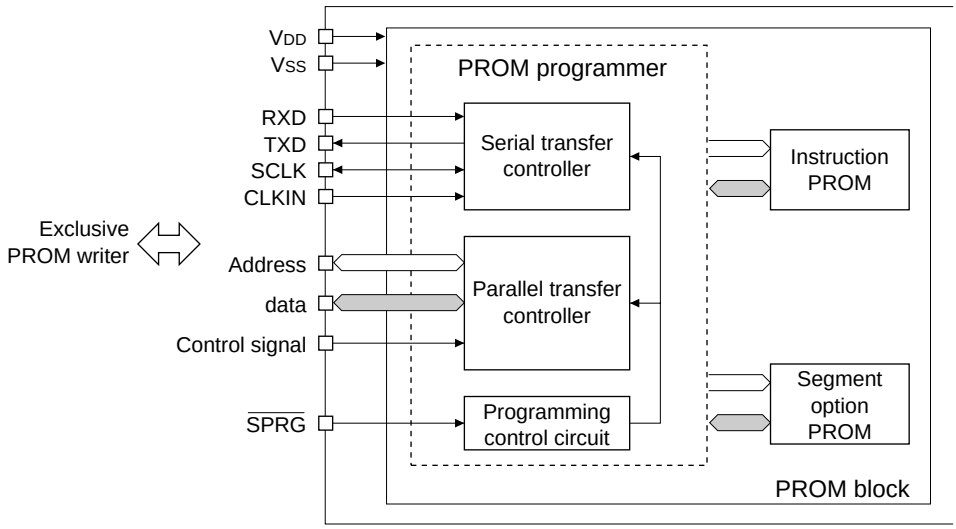


Fig. 5.1.1 Configuration of PROM programmer

The PROM programmer supports the following two writing modes.
1) Serial Programming
2) Parallel Programming

Serial programming mode uses the serial communication ports of the PROM writer and E0C63P366 to write data. This mode enables on-board programming by designing the target board with a serial writing function. In parallel programming mode, the on-chip Flash ROM can be directly programmed using the exclusive PROM writer with the adaptor socket installed. Refer to Section 5.2, "Operating Mode", for each programming method.

Terminals

The E0C63P366 provides the following terminals for programming the Flash EEPROM.

$\overline{\text{SPRG}}$: Flash programming control terminal (pull-up resistor built-in)
When set to High ..... Normal operation mode (The CPU executes the program in the Flash EEPROM.)
When set to Low ..... Programming mode (for writing data to the Flash EEPROM)
SCLK: Serial transfer clock input/output terminal for Serial Programming (pull-up resistor built-in)
RXD: Serial data input terminal for Serial Programming (pull-up resistor built-in)
TXD: Serial data output terminal for Serial Programming
CLKIN: PROM programmer clock input terminal (1 MHz; pull-up resistor built-in)

The five terminals above are provided exclusively for the Flash EEPROM. The E0C63358 and E0C63158 do not have these terminals.

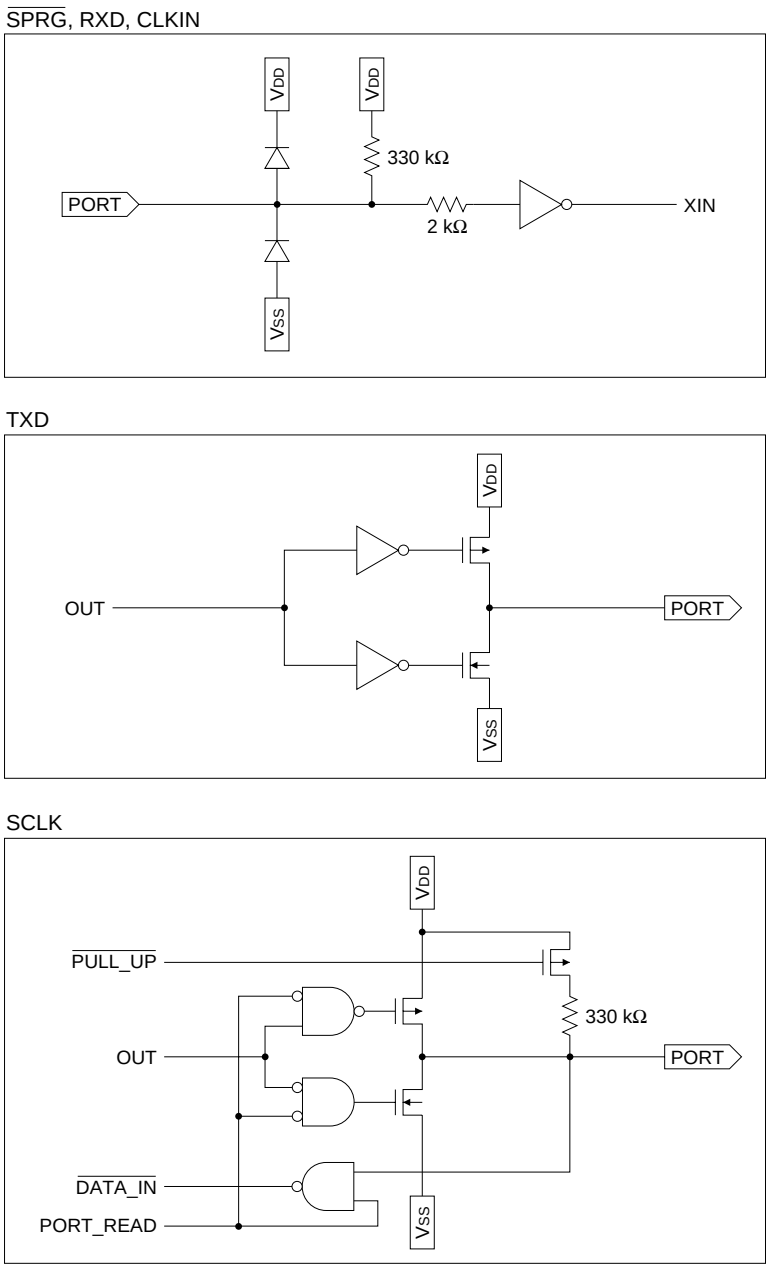


Fig. 5.1.2 Terminal specifications

5.2 Operating Mode

Three operating modes are available in the E0C63P366: one is for normal operation and the others are for programming.
The operating mode is decided by the terminal setting at power-on or initial reset.
When the $\overline{\text{SPRG}}$ terminal is set to Low, the E0C63P366 enters serial programming mode. To operate the E0C63P366 in normal operation mode (to execute the instruction written to the Flash EEPROM after programming), the $\overline{\text{SPRG}}$ terminal should be set to High or open.
The parallel programming including the mode switching and terminal settings is controlled by the exclusive PROM writer.
Table 5.2.1 lists the operating modes.

Table 5.2.1 Mode setting by $\overline{\text{SPRG}}$ terminal

Operating mode	$\overline{\text{SPRG}}$ terminal
Normal mode	High or open
Serial programming mode	Low
Parallel programming mode	Set by PROM writer

5.2.1 Normal operation mode

In this mode, the E0C63000 core CPU and the peripheral circuits operate by the instructions programmed in the Flash EEPROM. The internal code ROM (Flash EEPROM) bit data is set to "1" at shipment.
In normal operation mode, set the terminals for programming the Flash EEPROM as shown in Table 5.2.1.1. The board must be designed so that the terminal settings cannot be changed while the IC is operating.

Table 5.2.1.1 Terminal settings in normal operation mode

Terminal	Setting
$\overline{\text{SPRG}}$	High or open
SCLK	High or open
RXD	High or open
TXD	Open
CLKIN	High or open

5.2.2 Serial programming mode

Serial programming mode writes data to the Flash EEPROM using a serial communication between the exclusive PROM writer (Universal ROM Writer II) and the E0C63P366. By providing a serial communication port on the target board, the E0C63P366 on the board can be programmed (on-board writing).

Table 5.2.2.1 Terminal settings in serial programming mode

Terminal	Setting
$\overline{\text{SPRG}}$	Low
SCLK	Connected to PROM writer
RXD	Connected to PROM writer
TXD	Connected to PROM writer
CLKIN	Connected to PROM writer

When the $\overline{\text{SPRG}}$ terminal is set to Low, the E0C63P366 starts operating in serial programming mode after power-on or an initial reset.
Be sure not to change the $\overline{\text{SPRG}}$ terminal status during normal operation or serial programming, because the operating mode may change according to the terminal status.

The serial programming is performed using the 1 MHz clock supplied from the PROM writer to the CLKIN terminal. Take noise measure into consideration so that noise does not affect the clock line input to the CLKIN terminal when designing the target board.
The PROM writer does not supply the source voltage to the E0C63P366 during serial programming. Therefore, supply a 5 V source voltage between the VDD and VSS terminals of the E0C63P366. Furthermore, to start a serial programming, an initial reset to the E0C63P366 is required. Use the $\overline{\text{RESET}}$ terminal to reset the E0C63P366 securely.

5.2.3 Parallel programming mode

The parallel programming can be performed by installing the E0C63P366 to the exclusive PROM writer via the adaptor socket. In this mode, it is not necessary to set up the programming terminals since it is controlled by the exclusive PROM writer. When using a chip, perform on-board programming in serial programming mode.

CHAPTER 6 DIFFERENCES FROM MASK ROM MODELS

This chapter explains the differences in functions (except for the Flash EEPROM block) between the E0C63P366 and the mask ROM models (E0C63358 and E0C63158).

6.1 Differences from E0C63358

6.1.1 Terminal configuration

The E0C63P366 uses the same package (QFP15-100pin) as the E0C63358. Since the terminals for the PROM programmer added to the E0C63P366 are assigned to the unused terminals of the E0C63358, the terminal assignment is compatible with the E0C63358.

Table 6.1.1.1 Terminal assignment (QFP15-100pin)

No.	Pin name		No.	Pin name		No.	Pin name		No.	Pin name	
	E0C63P366	E0C63358		E0C63P366	E0C63358		E0C63P366	E0C63358		E0C63P366	E0C63358
1	SEG7	SEG7	26	**CLKIN**	N.C.	51	**SCLK**	N.C.	76	R13	R13
2	SEG8	SEG8	27	**$\overline{\text{SPRG}}$**	N.C.	52	P43	P43	77	R12	R12
3	SEG9	SEG9	28	COM0	COM0	53	P42	P42	78	R11	R11
4	SEG10	SEG10	29	COM1	COM1	54	P41	P41	79	R10	R10
5	SEG11	SEG11	30	COM2	COM2	55	P40	P40	80	R03	R03
6	SEG12	SEG12	31	COM3	COM3	56	P33	P33	81	R02	R02
7	SEG13	SEG13	32	CB	CB	57	P32	P32	82	R01	R01
8	SEG14	SEG14	33	CA	CA	58	P31	P31	83	R00	R00
9	SEG15	SEG15	34	V_{C3}	V_{C3}	59	P30	P30	84	BZ	BZ
10	SEG16	SEG16	35	V_{C2}	V_{C2}	60	P23	P23	85	K00	K00
11	SEG17	SEG17	36	V_{C1}	V_{C1}	61	P22	P22	86	K01	K01
12	SEG18	SEG18	37	V_{SS}	V_{SS}	62	P21	P21	87	K02	K02
13	SEG19	SEG19	38	OSC1	OSC1	63	P20	P20	88	K03	K03
14	SEG20	SEG20	39	OSC2	OSC2	64	P13	P13	89	K10	K10
15	SEG21	SEG21	40	V_{D1}	V_{D1}	65	P12	P12	90	K11	K11
16	SEG22	SEG22	41	OSC3	OSC3	66	P11	P11	91	K12	K12
17	SEG23	SEG23	42	OSC4	OSC4	67	P10	P10	92	K13	K13
18	SEG24	SEG24	43	V_{DD}	V_{DD}	68	P03	P03	93	K20	K20
19	SEG25	SEG25	44	$\overline{\text{RESET}}$	$\overline{\text{RESET}}$	69	P02	P02	94	SEG0	SEG0
20	SEG26	SEG26	45	$\overline{\text{TEST}}$	$\overline{\text{TEST}}$	70	P01	P01	95	SEG1	SEG1
21	SEG27	SEG27	46	AV_{REF}	AV_{REF}	71	P00	P00	96	SEG2	SEG2
22	SEG28	SEG28	47	AV_{DD}	AV_{DD}	72	R23	R23	97	SEG3	SEG3
23	SEG29	SEG29	48	AV_{SS}	AV_{SS}	73	R22	R22	98	SEG4	SEG4
24	SEG30	SEG30	49	**RXD**	N.C.	74	R21	R21	99	SEG5	SEG5
25	SEG31	SEG31	50	**TXD**	N.C.	75	R20	R20	100	SEG6	SEG6

N.C. : No Connection

6.1.2 Mask option

The E0C63P366 cannot specify the E0C63358 mask options individually.
The following option combination is provided for the E0C63P366.

Note: Recommended option data is written to the LCD segment opotion PROM before the IC is shipped. Modifying the LCD segment opotion is done at the user's own risk.
For the LCD segment specifications, both the segment allocation and the output specification can be selected similarly to the E0C63358. Create segment option data using the segment option generator SOG63358 and write it to the segment option ROM in the E0C63P366. The selected option specifications are automatically set to each segment terminal.

Table 6.1.2.1 Combination of mask options

Mask option		E0C63P366E (Type E)	E0C63P366F (Type F)
OSC1 oscillation circuit		Crystal (32.768 kHz)	Crystal (32.768 kHz)
OSC3 oscillation circuit		Ceramic	CR
Multiple key reset combination		Not used	Not used
Multiple key reset time authorize		Not used	Not used
Input port pull-up resistors	K00	With pull-up resistor	With pull-up resistor
	K01	With pull-up resistor	With pull-up resistor
	K02	With pull-up resistor	With pull-up resistor
	K03	With pull-up resistor	With pull-up resistor
	K10	With pull-up resistor	With pull-up resistor
	K11	With pull-up resistor	With pull-up resistor
	K12	With pull-up resistor	With pull-up resistor
	K13	With pull-up resistor	With pull-up resistor
	K20	With pull-up resistor	With pull-up resistor
Output port output specifications	R10–R13	Complementary output	Complementary output
	R20–R23	Complementary output	Complementary output
I/O port output specifications	P10–P13	Complementary output	Complementary output
	P20	Complementary output	Complementary output
	P21	Complementary output	Complementary output
	P22	Complementary output	Complementary output
	P23	Complementary output	Complementary output
	P30	Complementary output	Complementary output
	P31	Complementary output	Complementary output
	P32	Complementary output	Complementary output
	P33	Complementary output	Complementary output
	P40	Complementary output	Complementary output
	P41	Complementary output	Complementary output
	P42	Complementary output	Complementary output
	P43	Complementary output	Complementary output
I/O port pull-up resistors	P10–P13	With pull-up resistor	With pull-up resistor
	P20	With pull-up resistor	With pull-up resistor
	P21	With pull-up resistor	With pull-up resistor
	P22	With pull-up resistor	With pull-up resistor
	P23	With pull-up resistor	With pull-up resistor
	P30	With pull-up resistor	With pull-up resistor
	P31	With pull-up resistor	With pull-up resistor
	P32	With pull-up resistor	With pull-up resistor
	P33	With pull-up resistor	With pull-up resistor
	P40	No pull-up resistor	No pull-up resistor
	P41	No pull-up resistor	No pull-up resistor
	P42	No pull-up resistor	No pull-up resistor
	P43	No pull-up resistor	No pull-up resistor
LCD drive bias		1/3 bias (internal)	1/3 bias (internal)
Serial interface signal polarity		Negative polarity	Negative polarity
Buzzer output specification		Negative polarity	Negative polarity

6.1.3 Power supply

Supply voltage range

E0C63P366: 2.7 V to 5.5 V E0C63358: 0.9 V to 3.6 V

The E0C63P366 cannot operate with a less than 2.7 V supply voltage. Note that this difference affects the electrical characteristics.

Operating mode of oscillation system voltage regulator and internal operating voltage

The oscillation system voltage regulator in the E0C63358 can operate in V_{C2} mode (uses the V_{C2} voltage generated by the LCD system voltage circuit) when the supply voltage is within the range of 0.9 V to 1.4 V. When the supply voltage is within the range of 1.4 V to 3.6 V, the oscillation system voltage regulator can operate in normal mode (uses the V_{DD} supply voltage). Therefore, the operating mode of the E0C63358 needs to be switched according to the supply voltage using the VDSEL register (FF01H•D2). Since the E0C63P366 does not operate with less than 2.7 V supply voltage, this switching is not necessary. Although the VDSEL register is provided for developing the E0C63358 application, the register value does not affect the operating mode (fixed at normal mode).
The oscillation system voltage regulator generates the V_{D1} voltage for driving the oscillation circuit. The E0C63358 uses V_{D1} as the operating voltage of the internal logic circuits (CPU, ROM, RAM and peripheral digital circuits) as well. The V_{D1} voltage level must be switched using the VDC register (FF00H•D0) according to the oscillation circuit used and the supply voltage.
In the E0C63P366, this switching is not necessary because the V_{D1} voltage level is fixed at 2.05 V. Furthermore, the V_{D1} voltage is used only for the OSC1 oscillation circuit, and the OSC3 oscillation circuit and other internal logic circuits operate with V_{DD} as the source voltage. The VDC register value does not affect the V_{D1} voltage level (it does however, affect switching of the CPU clock).
Table 6.1.3.1 shows the operating mode of the oscillation system voltage regulator and the V_{D1} voltage value, and Table 6.1.3.2 shows the I/O map of the control registers.

Table 6.1.3.1 Operating mode of oscillation system voltage regulator and V_{D1}

E0C63358

Power supply circuit	Operating condition	V_{D1} (V)	Supply voltage V_{DD} (V)			
			0.9–1.4	1.4–2.3	2.3–3.6	3.6–5.5
Oscillation system voltage regulator	OSC1	1.35	V_{C2} mode	Normal mode		Not allowed
	OSC3, 4 MHz	2.25	Not allowed		Normal mode	Not allowed

E0C63P366

Power supply circuit	Operating condition	V_{D1} (V)	Supply voltage V_{DD} (V)			
			0.9–1.4	1.4–2.7	2.7–3.6	3.6–5.5
Oscillation system voltage regulator	OSC1	2.05	Not allowed		Normal mode	
	OSC3, 4 MHz	V_{DD}	Not allowed		Normal mode	

Table 6.1.3.2 I/O memory map

E0C63358

Address	Register								Comment
	D3	D2	D1	D0	Name	Init	1	0	
FF00H	CLKCHG	OSCC	0	VDC	CLKCHG	0	OSC3	OSC1	CPU clock switch
					OSCC	0	On	Off	OSC3 oscillation On/Off
	R/W		R	R/W	0	–			Unused
					VDC	0	2.25 V	1.35 V	CPU operating voltage switch (1.35 V: OSC1, 2.25 V: OSC3)
FF01H	VADSEL	VDSEL	0	0	VADSEL	0	V_{C2}	V_{DD}	Power source selection for A/D converter
					VDSEL	0	V_{C2}	V_{DD}	Power supply selection for oscillation system voltage regulator
	R/W		R		0	–			Unused
					0	–			Unused

E0C63P366

Address	Register								Comment
	D3	D2	D1	D0	Name	Init	1	0	
FF00H	CLKCHG	OSCC	0	VDC	CLKCHG	0	OSC3	OSC1	CPU clock switch
					OSCC	0	On	Off	OSC3 oscillation On/Off
	R/W		R	R/W	0	–			Unused
					VDC	0	(OSC3)	(OSC1)	(Operating voltage switch, CPU clock switch)
FF01H	VADSEL	VDSEL	0	DBON	VADSEL	0	(V_{C2})	(V_{DD})	(Power source selection for A/D converter)
					VDSEL	0	(V_{C2})	(V_{DD})	(Power source selection for oscillation system voltage regulator)
	R/W		R	R/W	0	–			Unused
					DBON	0	1	0	General-purpose register

LCD drive voltage (V_{C1}–V_{C3})

The LCD system voltage circuit generates V_{C2} with the voltage regulator built-in, and generates two other voltages by boosting or reducing the voltage V_{C2}. ($V_{C1} = 1/2 \bullet V_{C2}$, $V_{C3} = 3/2 \bullet V_{C2}$).
Furthermore, the LCD drive bias option is fixed at 1/3 bias in the E0C63P366. Therefore, the 1/2 bias ($V_{C2} = V_{C1}$, $V_{C3} = 2 \bullet V_{C1}$) drive allowed in the E0C63358 cannot be evaluated.

Operating mode of A/D converter power supply

The A/D converter in the E0C63358 can operate in V_{C2} mode (uses the V_{C2} voltage generated by the LCD system voltage circuit) when the supply voltage is within the range of 0.9 V to 1.6 V. When the supply voltage is within the range of 1.6 V to 3.6 V, the A/D converter can operate in normal mode (uses the V_{DD} supply voltage). Therefore, the operating mode of the E0C63358 needs to be switched according to the supply voltage using the VADSEL register (FF01H•D3). Since the E0C63P366 does not operate with a less than 2.7 V supply voltage, this switching is not necessary. Although the VADSEL register is provided for developing the E0C63358 application, the register value does not affect the operating mode (fixed at normal mode).
Table 6.1.3.3 shows the operating mode of the A/D converter power supply, and Table 6.1.3.4 shows the I/O map of the control registers.

Table 6.1.3.3 Operating mode of A/D converter power supply

E0C63358

Circuit	Supply voltage V_{DD} (V)		
	0.9–1.6	1.6–3.6	3.6–5.5
A/D converter	V_{C2} mode	Normal mode	Not allowed

E0C63P366

Circuit	Supply voltage V_{DD} (V)		
	0.9–2.7	2.7–3.6	3.6–5.5
A/D converter	Not allowed	Normal mode	

Table 6.1.3.4 I/O memory map

E0C63358

Address	Register								Comment
	D3	D2	D1	D0	Name	Init	1	0	
FF01H	VADSEL	VDSEL	0	0	VADSEL	0	V_{C2}	V_{DD}	Power source selection for A/D converter
					VDSEL	0	V_{C2}	V_{DD}	Power supply selection for oscillation system voltage regulator
	R/W		R		0	–			Unused
					0	–			Unused

E0C63P366

Address	Register								Comment
	D3	D2	D1	D0	Name	Init	1	0	
FF01H	VADSEL	VDSEL	0	DBON	VADSEL	0	(V_{C2})	(V_{DD})	(Power source selection for A/D converter)
					VDSEL	0	(V_{C2})	(V_{DD})	(Power source selection for oscillation system voltage regulator)
	R/W		R	R/W	0	–			Unused
					DBON	0	1	0	General-purpose register

6.1.4 Initial reset

When the power is turned on, the reset terminal must be set at Low level until the supply voltage rises to the Vsr level.

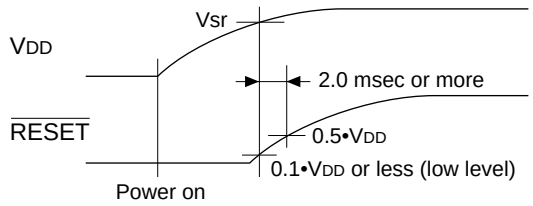


Fig. 6.1.4.1 Initial reset at power-on

The Vsr voltage level is different:
E0C63358: Vsr = 1.4 V
E0C63P366: Vsr = 2.7 V

Furthermore, E0C63P366 uses the initial reset signal as a trigger for setting either the normal operation mode or the programming mode. Therefore, design the reset input circuit so that the IC will be reset for sure. Initial resetting during operation is the same as the E0C63358.
When resetting the IC in the normal operation mode, make sure to fix the $\overline{\text{SPRG}}$ terminal at High level or leave open.

6.1.5 ROM, RAM

The E0C63P366 employs a Flash EEPROM for the internal ROM. The Flash EEPROM can be rewritten up to 100 times. Rewriting data is done at the user's own risk.
Table 6.1.5.1 lists the code ROM and RAM sizes of the E0C63P366 and the E0C63358.

Table 6.1.5.1 Memory size

Memory	E0C63P366	E0C63358
Code ROM	16,384 × 13 bits	8,192 × 13 bits
Data RAM	2,048 × 4 bits	512 × 4 bits

When developing an application for the E0C63358, pay attention to the memory size.

6.1.6 I/O memory

The DBON register (FF01H•D0) exists in the I/O memory of the E0C63P366 in order to develop an E0C63158 application. This register does not exist in the E0C63358. In the E0C63P336, this register functions as a general-purpose register.

6.1.7 Oscillation circuit

In the E0C63P366, only crystal oscillation is available for the OSC1 oscillation circuit and either ceramic or CR oscillation is available for the OSC3 oscillation circuit. The OSC1 CR oscillator option allowed in the E0C63358 cannot be selected.
Furthermore, pay attention to the difference on the oscillation start time according to the supply voltage. Be sure to have enough margin especially for stabilizing the OSC3 oscillation when controlling the peripheral circuit that uses the OSC3 clock.

6.1.8 SVD circuit

The E0C63P366 has a built-in SVD (supply voltage detection) circuit the same as the E0C63358. However, the detection levels are different from those of the E0C63358. Furthermore, there is a great restriction on the operable detection levels in the E0C63P366.

Table 6.1.8.1 Detection levels of SVD circuit

Detection level	E0C63358			E0C63P366		
	Min.	Typ.	Max.	Min.	Typ.	Max.
SVDS3–0 = "0"	0.95	1.05	1.15	Not allowed		
SVDS3–0 = "1"	1.02	1.10	1.18			
SVDS3–0 = "2"	1.07	1.15	1.23			
SVDS3–0 = "3"	1.12	1.20	1.28			
SVDS3–0 = "4"	1.16	1.25	1.34			
SVDS3–0 = "5"	1.21	1.30	1.39			
SVDS3–0 = "6"	1.30	1.40	1.50			
SVDS3–0 = "7"	1.49	1.60	1.71			
SVDS3–0 = "8"	1.81	1.95	2.09			
SVDS3–0 = "9"	1.86	2.00	2.14			
SVDS3–0 = "10"	1.91	2.05	2.19			
SVDS3–0 = "11"	1.95	2.10	2.25			
SVDS3–0 = "12"	2.05	2.20	2.35			
SVDS3–0 = "13"	2.14	2.30	2.46			
SVDS3–0 = "14"	2.33	2.50	2.68	2.50	2.70	2.90
SVDS3–0 = "15"	2.42	2.60	2.78	2.60	2.80	3.00

Be aware that the SVD circuit in the E0C63P366 does not operate properly if the SVDS register is set to 13 or less.

6.2 Differences from E0C63158

6.2.1 Terminal configuration

The design of the E0C63P366 is based on the E0C63358, therefore the terminal configuration and assignment are different from those of the E0C63158 (e.g., the E0C63P366 has LCD driver output terminals that do not exist in the E0C63158). Furthermore, PROM programming terminals are added to the E0C63P366.

Table 6.2.1.1 Terminal assignment comparison list (E0C63158: QFP12-48pin)

E0C63P366		E0C63158		E0C63P366		E0C63158		E0C63P366		E0C63158		E0C63P366		E0C63158	
No.	Pin name	No.	Pin name	No.	Pin name	No.	Pin name	No.	Pin name	No.	Pin name	No.	Pin name	No.	Pin name
1	SEG7	–	–	26	**CLKIN**	–	–(*1)	51	**SCLK**	–	–(*1)	76	R13	30	R13
2	SEG8	–	–	27	**$\overline{\text{SPRG}}$**	–	–(*1)	52	P43	14	P43	77	R12	31	R12
3	SEG9	–	–	28	COM0	–	–	53	P42	15	P42	78	R11	32	R11
4	SEG10	–	–	29	COM1	–	–	54	P41	16	P41	79	R10	33	R10
5	SEG11	–	–	30	COM2	–	–	55	P40	17	P40	80	R03	34	R03
6	SEG12	–	–	31	COM3	–	–	56	P33	–	–	81	R02	35	R02
7	SEG13	–	–	32	CB	11	CB	57	P32	–	–	82	R01	37	R01
8	SEG14	–	–	33	CA	12	CA	58	P31	–	–	83	R00	38	R00
9	SEG15	–	–	34	V_{C3}	–	–	59	P30	–	–	84	BZ	39	BZ
10	SEG16	–	–	35	V_{C2}	13	V_{C2}	60	P23	18	P23	85	K00	40	K00
11	SEG17	–	–	36	V_{C1}	–	–	61	P22	19	P22	86	K01	41	K01
12	SEG18	–	–	37	V_{SS}	1	V_{SS}	62	P21	20	P21	87	K02	42	K02
13	SEG19	–	–	38	OSC1	2	OSC1	63	P20	21	P20	88	K03	43	K03
14	SEG20	–	–	39	OSC2	3	OSC2	64	P13	22	P13	89	K10	44	K10
15	SEG21	–	–	40	V_{D1}	4	V_{D1}	65	P12	23	P12	90	K11	45	K11
16	SEG22	–	–	41	OSC3	5	OSC3	66	P11	24	P11	91	K12	46	K12
17	SEG23	–	–	42	OSC4	6	OSC4	67	P10	25	P10	92	K13	47	K13
18	SEG24	–	–	43	V_{DD}	7	V_{DD}	68	P03	26	P03	93	K20	48	K20
19	SEG25	–	–	44	$\overline{\text{RESET}}$	8	$\overline{\text{RESET}}$	69	P02	27	P02	94	SEG0	–	–
20	SEG26	–	–	45	$\overline{\text{TEST}}$	9	$\overline{\text{TEST}}$	70	P01	28	P01	95	SEG1	–	–
21	SEG27	–	–	46	AV_{REF}	10	V_{REF}	71	P00	29	P00	96	SEG2	–	–
22	SEG28	–	–	47	AV_{DD}	–	–	72	R23	–	–	97	SEG3	–	–
23	SEG29	–	–	48	AV_{SS}	–	–	73	R22	–	–	98	SEG4	–	–
24	SEG30	–	–	49	**RXD**	–	–(*1)	74	R21	–	–	99	SEG5	–	–
25	SEG31	–	–	50	**TXD**	–	–(*1)	75	R20	–	–	100	SEG6	–	–

*1 : Pin for serial programming

Table 6.2.1.2 Terminal assignment comparison list (E0C63158: QFP13-64pin)

E0C63P366		E0C63158		E0C63P366		E0C63158		E0C63P366		E0C63158		E0C63P366		E0C63158	
No.	Pin name	No.	Pin name	No.	Pin name	No.	Pin name	No.	Pin name	No.	Pin name	No.	Pin name	No.	Pin name
1	SEG7	–	–	26	**CLKIN**	–	–(*1)	51	**SCLK**	–	–(*1)	76	R13	41	R13
2	SEG8	–	–	27	**$\overline{\text{SPRG}}$**	–	–(*1)	52	P43	17	P43	77	R12	42	R12
3	SEG9	–	–	28	COM0	–	–	53	P42	18	P42	78	R11	43	R11
4	SEG10	–	–	29	COM1	–	–	54	P41	19	P41	79	R10	44	R10
5	SEG11	–	–	30	COM2	–	–	55	P40	20	P40	80	R03	45	R03
6	SEG12	–	–	31	COM3	–	–	56	P33	21	P33	81	R02	46	R02
7	SEG13	–	–	32	CB	13	CB	57	P32	22	P32	82	R01	52	R01
8	SEG14	–	–	33	CA	14	CA	58	P31	23	P31	83	R00	53	R00
9	SEG15	–	–	34	V_{C3}	–	–	59	P30	24	P30	84	BZ	54	BZ
10	SEG16	–	–	35	V_{C2}	15	V_{C2}	60	P23	25	P23	85	K00	55	K00
11	SEG17	–	–	36	V_{C1}	–	–	61	P22	26	P22	86	K01	56	K01
12	SEG18	–	–	37	V_{SS}	1	V_{SS}	62	P21	27	P21	87	K02	57	K02
13	SEG19	–	–	38	OSC1	2	OSC1	63	P20	28	P20	88	K03	58	K03
14	SEG20	–	–	39	OSC2	3	OSC2	64	P13	29	P13	89	K10	59	K10
15	SEG21	–	–	40	V_{D1}	4	V_{D1}	65	P12	30	P12	90	K11	60	K11
16	SEG22	–	–	41	OSC3	5	OSC3	66	P11	31	P11	91	K12	61	K12
17	SEG23	–	–	42	OSC4	6	OSC4	67	P10	32	P10	92	K13	62	K13
18	SEG24	–	–	43	V_{DD}	7	V_{DD}	68	P03	33	P03	93	K20	63	K20
19	SEG25	–	–	44	$\overline{\text{RESET}}$	8	$\overline{\text{RESET}}$	69	P02	34	P02	94	SEG0	–	–
20	SEG26	–	–	45	$\overline{\text{TEST}}$	9	$\overline{\text{TEST}}$	70	P01	35	P01	95	SEG1	–	–
21	SEG27	–	–	46	AV_{REF}	12	V_{REF}	71	P00	36	P00	96	SEG2	–	–
22	SEG28	–	–	47	AV_{DD}	10	AV_{DD}	72	R23	37	R23	97	SEG3	–	–
23	SEG29	–	–	48	AV_{SS}	11	AV_{SS}	73	R22	38	R22	98	SEG4	–	–
24	SEG30	–	–	49	**RXD**	–	–(*1)	74	R21	39	R21	99	SEG5	–	–
25	SEG31	–	–	50	**TXD**	–	–(*1)	75	R20	40	R20	100	SEG6	–	–

*1 : Pin for serial programming

Table 6.2.1.3 Pad assignment comparison list

E0C63P366		E0C63158		E0C63P366		E0C63158		E0C63P366		E0C63158		E0C63P366		E0C63158	
No.	Pad name	No.	Pad name	No.	Pad name	No.	Pad name	No.	Pad name	No.	Pad name	No.	Pad name	No.	Pad name
79	P43	1	P43	2	R12	26	R12	27	SEG7	–	–	53	**$\overline{\text{SPRG}}$**	–	– (∗1)
80	P42	2	P42	3	R11	27	R11	28	SEG8	–	–	54	COM0	–	–
81	P41	3	P41	4	R10	28	R10	29	SEG9	–	–	55	COM1	–	–
82	P40	4	P40	5	R03	29	R03	30	SEG10	–	–	56	COM2	–	–
83	P33	5	P33	6	R02	30	R02	31	SEG11	–	–	57	COM3	–	–
84	P32	6	P32	7	R01	31	R01	32	SEG12	–	–	58	CB	55	CB
85	P31	7	P31	8	R00	32	R00	33	SEG13	–	–	59	CA	56	CA
86	P30	8	P30	9	BZ	33	BZ	34	SEG14	–	–	60	V_{C3}	–	–
87	P23	9	P23	10	K00	34	K00	35	SEG15	–	–	61	V_{C2}	57	V_{C2}
88	P22	10	P22	11	K01	35	K01	36	SEG16	–	–	62	V_{C1}	–	–
89	P21	11	P21	12	K02	36	K02	37	SEG17	–	–	63	V_{SS}	43	V_{SS}
90	P20	12	P20	13	K03	37	K03	38	SEG18	–	–	64	OSC1	44	OSC1
91	P13	13	P13	14	K10	38	K10	39	SEG19	–	–	65	OSC2	45	OSC2
92	P12	14	P12	15	K11	39	K11	40	SEG20	–	–	66	V_{D1}	46	V_{D1}
93	P11	15	P11	16	K12	40	K12	41	SEG21	–	–	67	OSC3	47	OSC3
94	P10	16	P10	17	K13	41	K13	42	SEG22	–	–	68	OSC4	48	OSC4
95	P03	17	P03	18	K20	42	K20	43	SEG23	–	–	69	V_{DD}	49	V_{DD}
96	P02	18	P02	19	N.C.	–	– (∗2)	44	SEG24	–	–	70	N.C.	–	–
97	P01	19	P01	20	SEG0	–	–	45	SEG25	–	–	71	$\overline{\text{RESET}}$	50	$\overline{\text{RESET}}$
98	P00	20	P00	21	SEG1	–	–	46	SEG26	–	–	72	$\overline{\text{TEST}}$	51	$\overline{\text{TEST}}$
99	R23	21	R23	22	SEG2	–	–	47	SEG27	–	–	73	AV_{REF}	54	V_{REF}
100	R22	22	R22	23	SEG3	–	–	48	SEG28	–	–	74	AV_{DD}	52	AV_{DD}
101	R21	23	R21	24	SEG4	–	–	49	SEG29	–	–	75	AV_{SS}	53	AV_{SS}
102	R20	24	R20	25	SEG5	–	–	50	SEG30	–	–	76	**RXD**	–	– (∗1)
1	R13	25	R13	26	SEG6	–	–	51	SEG31	–	–	77	**TXD**	–	– (∗1)
								52	**CLKIN**	–	– (∗1)	78	**SCLK**	–	– (∗1)

∗1: Pin for serial programming

∗2: Test signal monitor pad (Not used when writing; keep it open)

6.2.2 Mask option

The E0C63P366 cannot specify the E0C63158 mask options individually.
The following option combination is provided for the E0C63P366.

Table 6.2.2.1 Combination of mask options

Mask option		E0C63P366E (Type E)	E0C63P366F (Type F)
OSC1 oscillation circuit		Crystal (32.768 kHz)	Crystal (32.768 kHz)
OSC3 oscillation circuit		Ceramic	CR
Multiple key reset combination		Not used	Not used
Multiple key reset time authorize		Not used	Not used
Input port pull-up resistors	K00	With pull-up resistor	With pull-up resistor
	K01	With pull-up resistor	With pull-up resistor
	K02	With pull-up resistor	With pull-up resistor
	K03	With pull-up resistor	With pull-up resistor
	K10	With pull-up resistor	With pull-up resistor
	K11	With pull-up resistor	With pull-up resistor
	K12	With pull-up resistor	With pull-up resistor
	K13	With pull-up resistor	With pull-up resistor
	K20	With pull-up resistor	With pull-up resistor
Output port output specifications	R10–R13	Complementary output	Complementary output
	R20–R23	Complementary output	Complementary output
I/O port output specifications	P10–P13	Complementary output	Complementary output
	P20	Complementary output	Complementary output
	P21	Complementary output	Complementary output
	P22	Complementary output	Complementary output
	P23	Complementary output	Complementary output
	P30	Complementary output	Complementary output
	P31	Complementary output	Complementary output
	P32	Complementary output	Complementary output
	P33	Complementary output	Complementary output
	P40	Complementary output	Complementary output
	P41	Complementary output	Complementary output
	P42	Complementary output	Complementary output
	P43	Complementary output	Complementary output
I/O port pull-up resistors	P10–P13	With pull-up resistor	With pull-up resistor
	P20	With pull-up resistor	With pull-up resistor
	P21	With pull-up resistor	With pull-up resistor
	P22	With pull-up resistor	With pull-up resistor
	P23	With pull-up resistor	With pull-up resistor
	P30	With pull-up resistor	With pull-up resistor
	P31	With pull-up resistor	With pull-up resistor
	P32	With pull-up resistor	With pull-up resistor
	P33	With pull-up resistor	With pull-up resistor
	P40	No pull-up resistor	No pull-up resistor
	P41	No pull-up resistor	No pull-up resistor
	P42	No pull-up resistor	No pull-up resistor
	P43	No pull-up resistor	No pull-up resistor
Serial interface signal polarity		Negative polarity	Negative polarity
Buzzer output specification		Negative polarity	Negative polarity

6.2.3 Power supply

Supply voltage range

E0C63P366: 2.7 V to 5.5 V E0C63158: 0.9 V to 3.6 V

The E0C63P366 cannot operate with less than 2.7 V supply voltage. Note that this difference affects the electrical characteristics.

Operating mode of oscillation system voltage regulator and internal operating voltage

The oscillation system voltage regulator in the E0C63158 can operate in V_{C2} mode (uses the V_{C2} voltage generated by the voltage doubler) when the supply voltage is within the range of 0.9 V to 1.35 V. When the supply voltage is within the range of 1.35 V to 3.6 V, the oscillation system voltage regulator can operate in normal mode (uses the V_{DD} supply voltage). Therefore, the E0C63158 needs to control the voltage doubler and operating mode according to the supply voltage using the DBON register (FF01H•D0) and the VDSEL register (FF01H•D2). Since the E0C63P366 does not operate with less than 2.7 V supply voltage, this switching is not necessary. Although the DBON and VDSEL registers are provided for developing the E0C63158 application, the register values do not affect the operating mode (fixed at normal mode).
The oscillation system voltage regulator generates the V_{D1} voltage for driving the oscillation circuit. The E0C63158 uses V_{D1} as the operating voltage of the internal logic circuits (CPU, ROM, RAM and peripheral digital circuits) as well. The V_{D1} voltage level must be switched using the VDC register (FF00H•D0) according to the oscillation circuit used and the supply voltage.
In the E0C63P366, this switching is not necessary because the V_{D1} voltage level is fixed at 2.05 V. Furthermore, the V_{D1} voltage is used only for the OSC1 oscillation circuit, and the OSC3 oscillation circuit and other internal logic circuits operate with V_{DD} as the source voltage. The VDC register value does not affect the V_{D1} voltage level (it does however, affect switching of the CPU clock).
Table 6.2.3.1 shows the operating mode of the oscillation system voltage regulator and the V_{D1} voltage value, and Table 6.2.3.2 shows the I/O map of the control registers.

Table 6.2.3.1 Operating mode of oscillation system voltage regulator and V_{D1}

E0C63158

Power supply circuit	Operating condition	V_{D1} (V)	Supply voltage V_{DD} (V)			
			0.9–1.35	1.35–2.2	2.2–3.6	3.6–5.5
Oscillation system voltage regulator	OSC1	1.3	V_{C2} mode	Normal mode		Not allowed
	OSC3, 2 MHz	2.1	Not allowed		Normal mode	Not allowed

E0C63P366

Power supply circuit	Operating condition	V_{D1} (V)	Supply voltage V_{DD} (V)			
			0.9–1.35	1.35–2.7	2.7–3.6	3.6–5.5
Oscillation system voltage regulator	OSC1	2.05	Not allowed		Normal mode	
	OSC3, 4 MHz	V_{DD}	Not allowed		Normal mode	

Table 6.2.3.2 I/O memory map

E0C63158

Address	Register								Comment
	D3	D2	D1	D0	Name	Init	1	0	
FF00H	CLKCHG	OSCC	0	VDC	CLKCHG	0	OSC3	OSC1	CPU clock switch
					OSCC	0	On	Off	OSC3 oscillation On/Off
	R/W		R	R/W	0	–			Unused
					VDC	0	2.1 V	1.3 V	CPU operating voltage switch (1.3 V: OSC1, 2.1 V: OSC3)
FF01H	VADSEL	VDSEL	0	DBON	VADSEL	0	V_{C2}	V_{DD}	Power source selection for A/D converter
					VDSEL	0	V_{C2}	V_{DD}	Power supply selection for oscillation system voltage regulator
	R/W		R	R/W	0	–			Unused
					DBON	0	On	Off	Voltage doubler On/Off

E0C63P366

Address	Register								Comment
	D3	D2	D1	D0	Name	Init	1	0	
FF00H	CLKCHG	OSCC	0	VDC	CLKCHG	0	OSC3	OSC1	CPU clock switch
					OSCC	0	On	Off	OSC3 oscillation On/Off
	R/W		R	R/W	0	–			Unused
					VDC	0	(OSC3)	(OSC1)	(Operating voltage switch, CPU clock switch)
FF01H	VADSEL	VDSEL	0	DBON	VADSEL	0	(V_{C2})	(V_{DD})	(Power source selection for A/D converter)
					VDSEL	0	(V_{C2})	(V_{DD})	(Power source selection for oscillation system voltage regulator)
	R/W		R	R/W	0	–			Unused
					DBON	0	(On)	(Off)	(Voltage doubler On/Off)

LCD system voltage circuit

The E0C63P366 has a built-in LCD system voltage circuit that generates the LCD drive voltage. The E0C63158 does not contain this circuit.

Operating mode of A/D converter power supply

The A/D converter in the E0C63158 can operate in V_{C2} mode (uses the V_{C2} voltage generated by the voltage doubler) when the supply voltage is within the range of 0.9 V to 2.2 V. When the supply voltage is within the range of 2.2 V to 3.6 V, the A/D converter can operate in normal mode (uses the V_{DD} supply voltage). Therefore, the E0C63158 needs to control the voltage doubler and operating mode according to the supply voltage using the DBON register (FF01H•D0) and the VADSEL register (FF01H•D3). Since the E0C63P366 does not operate with less than 2.7 V supply voltage, this switching is not necessary. Although the DBON and VADSEL registers are provided for developing the E0C63158 application, the register value does not affect the operating mode (fixed at normal mode). Table 6.2.3.3 shows the operating mode of the A/D converter power supply, and Table 6.2.3.4 shows the I/O map of the control registers.

Table 6.2.3.3 Operating mode of A/D converter power supply

E0C63158

Circuit	Supply voltage V_{DD} (V)		
	0.9–2.2	2.2–3.6	3.6–5.5
A/D converter	V_{C2} mode	Normal mode	Not allowed

E0C63P366

Circuit	Supply voltage V_{DD} (V)		
	0.9–2.7	2.7–3.6	3.6–5.5
A/D converter	Not allowed	Normal mode	

Table 6.2.3.4 I/O memory map

E0C63158

Address	Register								Comment
	D3	D2	D1	D0	Name	Init	1	0	
FF01H	VADSEL	VDSEL	0	DBON	VADSEL	0	V_{C2}	V_{DD}	Power source selection for A/D converter
					VDSEL	0	V_{C2}	V_{DD}	Power supply selection for oscillation system voltage regulator
	R/W		R	R/W	0	–			Unused
					DBON	0	On	Off	Voltage doubler On/Off

E0C63P366

Address	Register								Comment
	D3	D2	D1	D0	Name	Init	1	0	
FF01H	VADSEL	VDSEL	0	DBON	VADSEL	0	(V_{C2})	(V_{DD})	(Power source selection for A/D converter)
					VDSEL	0	(V_{C2})	(V_{DD})	(Power source selection for oscillation system voltage regulator)
	R/W		R	R/W	0	–			Unused
					DBON	0	(On)	(Off)	(Voltage doubler On/Off)

6.2.4 Initial reset

When the power is turned on, the reset terminal must be set at Low level until the supply voltage rises to the Vsr level.

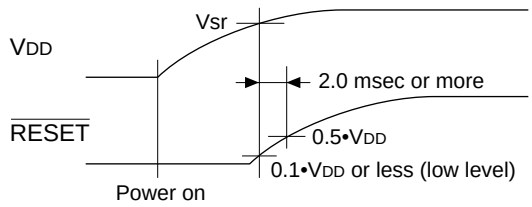


Fig. 6.2.4.1 Initial reset at power-on

The Vsr voltage level is different:
E0C63158: Vsr = 1.3 V
E0C63P366: Vsr = 2.7 V

Furthermore, E0C63P366 uses the initial reset signal as a trigger for setting either the normal operation mode or the programming mode. Therefore, design the reset input circuit so that the IC will be reset for sure. Initial resetting during operation is the same as the E0C63158. When resetting the IC in the normal operation mode, make sure to fix the $\overline{SPRG}$ terminal at High level or leave open.

6.2.5 ROM, RAM

The E0C63P366 employs a Flash EEPROM for the internal ROM. The Flash EEPROM can be rewritten up to 100 times. Rewriting data is done at the user's own risk.
Table 6.2.5.1 lists the code ROM and RAM sizes of the E0C63P366 and the E0C63158.

Table 6.2.5.1 Memory size

Memory	E0C63P366	E0C63158
Code ROM	16,384 × 13 bits	8,192 × 13 bits
Data RAM	2,048 × 4 bits	512 × 4 bits

When developing an application for the E0C63158, pay attention to the memory size.

6.2.6 I/O memory

The LCD driver control registers (FF60H, FF61H) exist in the I/O memory of the E0C63P366 in order to develop a E0C63358 application. These registers do not exist in the E0C63158.

6.2.7 Oscillation circuit

In the E0C63P366, only crystal oscillation is available for the OSC1 oscillation circuit and either ceramic or CR oscillation is available for the OSC3 oscillation circuit. The OSC1 CR oscillator option allowed in the E0C63158 cannot be selected.
Furthermore, pay attention to the difference of the oscillation start time according to the supply voltage. Be sure to have enough margin especially for stabilizing the OSC3 oscillation when controlling the peripheral circuit that uses the OSC3 clock.

6.2.8 SVD circuit

The E0C63P366 has a built-in SVD (supply voltage detection) circuit the same as the E0C63158. However, the detection levels are different from those of the E0C63158. Furthermore, there is a great restriction on the operable detection levels in the E0C63P366.

Table 6.2.8.1 Detection levels of SVD circuit

Detection level	E0C63158			E0C63P366		
	Min.	Typ.	Max.	Min.	Typ.	Max.
SVDS3–0 = "0"	0.95	1.05	1.15	Not allowed		
SVDS3–0 = "1"	1.05	1.10	1.15			
SVDS3–0 = "2"	1.10	1.15	1.20			
SVDS3–0 = "3"	1.15	1.20	1.25			
SVDS3–0 = "4"	1.20	1.25	1.30			
SVDS3–0 = "5"	1.25	1.30	1.35			
SVDS3–0 = "6"	1.35	1.40	1.45			
SVDS3–0 = "7"	1.55	1.60	1.65			
SVDS3–0 = "8"	1.90	1.95	2.00			
SVDS3–0 = "9"	1.95	2.00	2.05			
SVDS3–0 = "10"	2.00	2.05	2.10			
SVDS3–0 = "11"	2.05	2.10	2.15			
SVDS3–0 = "12"	2.15	2.20	2.25			
SVDS3–0 = "13"	2.25	2.30	2.35			
SVDS3–0 = "14"	2.45	2.50	2.55	2.50	2.70	2.90
SVDS3–0 = "15"	2.55	2.60	2.65	2.60	2.80	3.00

Be aware that the SVD circuit in the E0C63P366 does not operate properly if the SVDS register is set to 13 or less.

CHAPTER 7 SUMMARY OF NOTES

7.1 Notes for Low Current Consumption

The E0C63P366 contains control registers for each of the circuits so that current consumption can be reduced.
These control registers reduce the current consumption through programs that operate the circuits at the minimum levels.
The following lists the circuits that can control operation and their control registers. Refer to these when programming.

Table 7.1.1 Circuits and control registers

Circuit (and item)	Control register
CPU	HALT instruction
CPU operating frequency	CLKCHG, OSCC
LCD system voltage circuit	LPWR
SVD circuit	SVDON

Refer to Chapter 9, "Electrical Characteristics" for current consumption.

Below are the circuit statuses at initial reset.

CPU: Operating status

CPU operating frequency: Low speed side (CLKCHG = "0")
OSC3 oscillation circuit is in OFF status (OSCC = "0")

LCD system voltage circuit: OFF status (LPWR = "0")

SVD circuit: OFF status (SVDON = "0")

Also, be careful about panel selection because the current consumption can differ by the order of several µA on account of the LCD panel characteristics.

7.2 Summary of Notes by Function

Here, the cautionary notes are summed up by function category. Keep these notes well in mind when programming.

Memory and stack

(1) Memory is not implemented in unused areas within the memory map. Further, some non-implementation areas and unused (access prohibition) areas exist in the peripheral I/O area. If the program that accesses these areas is generated, its operation cannot be guaranteed. Refer to the I/O memory maps shown in Tables 4.1.1 (a)–(f) for the peripheral I/O area.

(2) Part of the RAM area is used as a stack area for subroutine call and register evacuation, so pay attention not to overlap the data area and stack area.

(3) The E0C63000 core CPU handles the stack using the stack pointer for 4-bit data (SP2) and the stack pointer for 16-bit data (SP1). 16-bit data are accessed in stack handling by SP1, therefore, this stack area should be allocated to the area where 4-bit/16-bit access is possible (0100H to 01FFH). The stack pointers SP1 and SP2 change cyclically within their respective range: the range of SP1 is 0000H to 03FFH and the range of SP2 is 0000H to 00FFH. Therefore, pay attention to the SP1 value because it may be set to 00FFH or less exceeding the 4-bit/16-bit accessible range in the E0C63P366. Memory accesses except for stack operations by SP1 are 4-bit data access.
After initial reset, all the interrupts including NMI are masked until both the stack pointers SP1 and SP2 are set by software. Further, if either SP1 or SP2 is re-set when both are set already, the interrupts including NMI are masked again until the other is re-set. Therefore, the settings of SP1 and SP2 must be done as a pair.

(4) The E0C63P366 has a built-in code ROM and RAM larger than those of the E0C63358 and the E0C63158. When using the E0C63P366 as a development tool of for the E0C63358/63158, pay attention to the memory size.

Power supply and operating mode

Since the E0C63P366 operates with a 2.7 V or more supply voltage, the operating mode of the power supply circuit is fixed at normal mode. Although the operating mode control registers exist, they function as general-purpose registers. It is not necessary to switch the operating mode as with the E0C63358/63158. However, when using the E0C63P366 as a development tool for the E0C63358/63158, program the appropriate control sequence according to the model (refer to the "Technical Manual" of each model).

Watchdog timer

(1) When the watchdog timer is being used, the software must reset it within 3-second cycles.

(2) Because the watchdog timer is set in operation state by initial reset, set the watchdog timer to disabled state (not used) before generating an interrupt (NMI) if it is not used.

Oscillation circuit

(1) It takes at least 5 msec from the time the OSC3 oscillation circuit goes ON until the oscillation stabilizes. Consequently, when switching the CPU operation clock from OSC1 to OSC3, do this after a minimum of 5 msec have elapsed since the OSC3 oscillation went ON. Further, the oscillation stabilization time varies depending on the external oscillator characteristics and conditions of use, so allow ample margin when setting the wait time.

(2) When switching the clock form OSC3 to OSC1, use a separate instruction for switching the OSC3 oscillation OFF. An error in the CPU operation can result if this processing is performed at the same time by the one instruction.

(3) In the E0C63P366, the VDC register value does not affect the V_{D1} voltage level. However, note that the CPU clock cannot be switched from OSC1 to OSC3 using the CLKCHG register if the VDC register value is "0". When using the E0C63P366 as a development tool for the E0C63358/63158, switch the operating voltage using the VDC register according to the control sequence of the model (refer to the "Technical Manual").

Input port

(1) When input ports are changed from low to high by pull-up resistors, the rise of the waveform is delayed on account of the time constant of the pull-up resistor and input gate capacitance. Hence, when fetching input ports, set an appropriate waiting time.
Particular care needs to be taken of the key scan during key matrix configuration.
Make this waiting time the amount of time or more calculated by the following expression.
$10 \times C \times R$
C: terminal capacitance 5 pF + parasitic capacitance ? pF
R: pull-up resistance 300 kΩ

(2) The K13 terminal functions as the clock input terminal for the programmable timer, and the input signal is shared with the input port and the programmable timer. Therefore, when the K13 terminal is set to the clock input terminal for the programmable timer, take care of the interrupt setting.

Output port

(1) When using the output port (R02, R03) as the special output port, fix the data register (R02, R03) at "1" and the high impedance control register (R02HIZ, R03HIZ) at "0" (data output).
Be aware that the output terminal is fixed at a low (V_{SS}) level the same as the DC output if "0" is written to the R02 and R03 registers when the special output has been selected.
Be aware that the output terminal shifts into high impedance status when "1" is written to the high impedance control register (R02HIZ, R03HIZ).

(2) A hazard may occur when the FOUT signal and the TOUT signal are turned ON and OFF.

(3) When f_{OSC3} is selected for the FOUT signal frequency, it is necessary to control the OSC3 oscillation circuit before output. Refer to Section 4.3, "Oscillation Circuit", for the control and notes.

I/O port

When in the input mode, I/O ports are changed from low to high by pull-up resistor, the rise of the waveform is delayed on account of the time constant of the pull-up resistor and input gate capacitance. Hence, when fetching input ports, set an appropriate wait time.
Particular care needs to be taken of the key scan during key matrix configuration.
Make this waiting time the amount of time or more calculated by the following expression.
$10 \times C \times R$
C: terminal capacitance 5 pF + parasitic capacitance ? pF
R: pull-up resistance 300 kΩ

LCD driver

(1) The contents of the display memory are undefined until the area is initialized (through, for instance, memory clear processing by the CPU). Initialize the display memory by executing initial processing.

(2) 100 msec or more time is necessary for stabilizing the LCD drive voltages V_{C1}, V_{C2} and V_{C3} after setting the LCD power control register LPWR to "1". Be careful of the segment-on right after the power is turned on.

Clock timer

Be sure to read timer data in the order of low-order data (TM0–TM3) then high-order data (TM4–TM7).

Programmable timer

(1) When reading counter data, be sure to read the low-order 4 bits (PTD00–PTD03, PTD10–PTD13) first. Furthermore, the high-order 4 bits (PTD04–PTD07, PTD14–PTD17) should be read within 0.73 msec of reading the low-order 4 bits (PTD00–PTD03, PTD10–PTD13).
For the 16 bit × 1 mode, be sure to read as following sequence:
(PTD00–PTD03) → (PTD04–PTD07) → (PTD10–PTD13) → (PTD14–PTD17)
The read sequence time should be within 1.46 msec.

(2) The programmable timer actually enters RUN/STOP status in synchronization with the falling edge of the input clock after writing to the PTRUN0/PTRUN1 register. Consequently, when "0" is written to the PTRUN0/PTRUN1 register, the timer enters STOP status at the point where the counter is decremented (-1). The PTRUN0/PTRUN1 register maintains "1" for reading until the timer actually stops.
Figure 7.2.1 shows the timing chart for the RUN/STOP control.

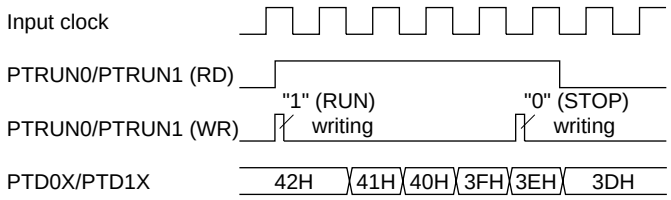


Fig. 7.2.1 Timing chart for RUN/STOP control

It is the same even in the event counter mode. Therefore, be aware that the counter does not enter RUN/STOP status if a clock is not input after setting the RUN/STOP control register (PTRUN0).

(3) Since the TOUT signal is generated asynchronously from the PTOUT register, a hazard within 1/2 cycle is generated when the signal is turned ON and OFF by setting the register.

(4) When the OSC3 oscillation clock is selected for the clock source, it is necessary to turn the OSC3 oscillation ON, prior to using the programmable timer. However the OSC3 oscillation circuit requires a time interval of at least 5 msec from turning the circuit ON until the oscillation stabilizes. Therefore, allow an adequate interval from turning the OSC3 oscillation circuit ON to starting the programmable timer. Refer to Section 4.3, "Oscillation Circuit", for the control and notes of the OSC3 oscillation circuit. At initial reset, the OSC3 oscillation circuit is set in the OFF state.

Serial interface

(1) Perform data writing/reading to the data registers SD0–SD7 only while the serial interface is not running (i.e., the synchronous clock is neither being input or output).

(2) As a trigger condition, it is required that data writing or reading on data registers SD0–SD7 be performed prior to writing "1" to SCTRG. (The internal circuit of the serial interface is initiated through data writing/reading on data registers SD0–SD7.) In addition, be sure to enable the serial interface with the ESIF register before setting the trigger.
Supply trigger only once every time the serial interface is placed in the RUN state. Refrain from performing trigger input multiple times, as leads to malfunctioning. Moreover, when the synchronous clock $\overline{\text{SCLK}}$ is external clock, start to input the external clock after the trigger.

(3) Setting of the input/output permutation (MSB first/LSB first) with the SDP register should be done before setting data to SD0–SD7.

(4) Be aware that the maximum clock frequency for the serial interface is limited to 1 MHz when OSC3 is used as the clock source of the programmable timer or in the slave mode.

A/D converter

(1) The A/D converter can operate by inputting the clock from the clock selector. Therefore, it is necessary to select the clock source and to turn the clock output on before starting A/D conversion. Furthermore, it is also necessary that the OSC3 oscillation circuit is operating when using the OSC3 clock.

(2) When using the OSC3 clock as the A/D conversion clock, do not stop the OSC3 oscillation circuit during A/D conversion. If the OSC3 oscillation circuit stops, correct A/D conversion result cannot be obtained.

(3) The input clock and analog input terminals should be set when the A/D converter stops. Changing these settings in the A/D converter operation may cause errors.

(4) To prevent malfunction, do not start A/D conversion (writing "1" to the ADRUN register) when the A/D conversion clock is not being output from the clock selector, and do not turn the clock off during A/D conversion.

(5) If the CHS register selects an input channel which is not included in the analog input terminals set by the PAD register (the PAD register can select several terminals simultaneously), the A/D conversion does not result in a correct converted value.

(6) During A/D conversion, do not operate the P4n terminals which are not used for analog inputs of the A/D converter (for input/output of digital signals). It affects the A/D conversion precision.

(7) In the E0C63P366, the value set in the VADSEL register does not affect the operating mode (operating voltage) of the A/D converter. However, when using the E0C63P366 as a development tool for the E0C63358/63158, control the operating voltage using the VADSEL register according to the control sequence of the model (refer to the "Technical Manual").

Buzzer output circuit

Since it generates a buzzer signal that is out of synchronization with the BZON register, hazards may at times be produced when the signal goes ON/OFF due to the setting of the BZON register.

SVD circuit

(1) To obtain a stable detection result, the SVD circuit must be ON for at least l00 µsec. So, to obtain the SVD detection result, follow the programming sequence below.

1. Set SVDON to "1"
2. Maintain for 100 µsec minimum
3. Set SVDON to "0"
4. Read SVDDT

(2) The SVD circuit should normally be turned OFF because SVD operation increase current consumption.

(3) Be aware that the SVD circuit in the E0C63P366 does not operate properly if the SVDS register is set to 13 or less, the SVD operation cannot be guaranteed since the lower limit of the operating voltage is 2.7 V.

Interrupt

(1) The interrupt factor flags are set when the interrupt condition is established, even if the interrupt mask registers are set to "0".

(2) After an interrupt occurs, the same interrupt will occur again if the interrupt enabled state (I flag = "1") is set or the RETI instruction is executed unless the interrupt factor flag is reset. Therefore, be sure to reset (write "1" to) the interrupt factor flag in the interrupt service routine before shifting to the interrupt enabled state.

(3) After an initial reset, all the interrupts including NMI are masked until both the stack pointers SP1 and SP2 are set with the software. Be sure to set the SP1 and SP2 in the initialize routine.
Further, when re-setting the stack pointer, the SP1 and SP2 must be set as a pair. When one of them is set, all the interrupts including NMI are masked and interrupts cannot be accepted until the other one is set.

Flash EEPROM

(1) The internal code ROM (Flash EEPROM) bit data is set to "1" at shipment. Therefore, it must be programmed before operating the IC in the normal operation mode (refer to Appendix).

(2) Recommended option data is written to the LCD segment opotion PROM before the IC is shipped. Modifying the LCD segment opotion is done at the user's own risk.

(3) The Flash EEPROM data can be rewritten up to 100 times for both the code and segment option ROMs.
Rewriting data is done at the user's own risk.

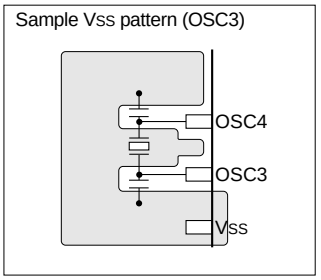
7.3 Precautions on Mounting

<Oscillation Circuit>

- Oscillation characteristics change depending on conditions (board pattern, components used, etc.). In particular, when a ceramic oscillator or crystal oscillator is used, use the oscillator manufacturer's recommended values for constants such as capacitance and resistance.
- Disturbances of the oscillation clock due to noise may cause a malfunction. Consider the following points to prevent this:

  (1) Components which are connected to the OSC1, OSC2, OSC3 and OSC4 terminals, such as oscillators, resistors and capacitors, should be connected in the shortest line.

  (2) As shown in the right hand figure, make a VSS pattern as large as possible at circumscription of the OSC1, OSC2, OSC3 and OSC4 terminals and the components connected to these terminals. Furthermore, do not use this VSS pattern for any purpose other than the oscillation system.



- In order to prevent unstable operation of the oscillation circuit due to current leak between OSC1/OSC3 and VDD, please keep enough distance between OSC1/OSC3 and VDD or other signals on the board pattern.

<Reset Circuit>

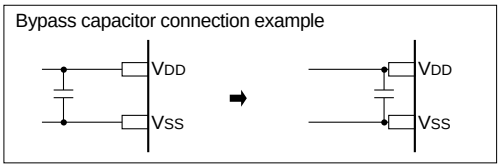
- The power-on reset signal which is input to the $\overline{\text{RESET}}$ terminal changes depending on conditions (power rise time, components used, board pattern, etc.).
  Decide the time constant of the capacitor and resistor after enough tests have been completed with the application product.
  When the built-in pull-up resistor is added to the $\overline{\text{RESET}}$ terminal by mask option, take into consideration dispersion of the resistance for setting the constant.
- In order to prevent any occurrences of unnecessary resetting caused by noise during operating, components such as capacitors and resistors should be connected to the $\overline{\text{RESET}}$ terminal in the shortest line.

<Power Supply Circuit>

- Sudden power supply variation due to noise may cause malfunction. Consider the following points to prevent this:

  (1) The power supply should be connected to the VDD, VSS, AVDD, AVSS and AVREF terminal with patterns as short and large as possible.
  In particular, the power supply for AVDD, AVSS and AVREF affects A/D conversion precision.

  (2) When connecting between the VDD and VSS terminals with a bypass capacitor, the terminals should be connected as short as possible.



  (3) Components which are connected to the VD1, VC1–VC3 terminals, such as capacitors and resistors, should be connected in the shortest line.
  In particular, the VC1–VC3 voltages affect the display quality.

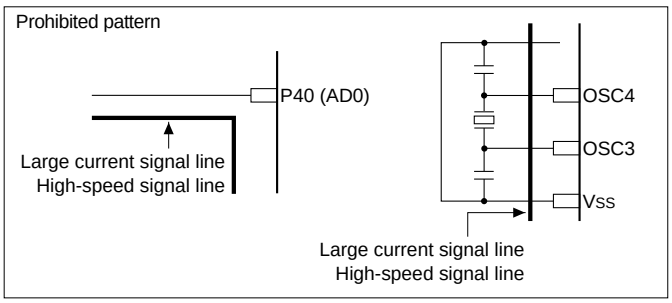
- Do not connect anything to the VC1–VC3 terminals when the LCD driver is not used.

<A/D Converter>

- When the A/D converter is not used, the power supply terminals for the analog system should be connected as shown below.
  AVDD → VDD
  AVSS → VSS
  AVREF → VSS

<Arrangement of Signal Lines>

- In order to prevent generation of electromagnetic induction noise caused by mutual inductance, do not arrange a large current signal line near the circuits that are sensitive to noise such as the oscillation unit and analog input unit.
- When a signal line is parallel with a high-speed line in long distance or intersects a high-speed line, noise may generated by mutual interference between the signals and it may cause a malfunction. Do not arrange a high-speed signal line especially near circuits that are sensitive to noise such as the oscillation unit and analog input unit.



<Precautions for Visible Radiation (when bare chip is mounted)>

- Visible radiation causes semiconductor devices to change the electrical characteristics. It may cause this IC to malfunction. When developing products which use this IC, consider the following precautions to prevent malfunctions caused by visible radiations.

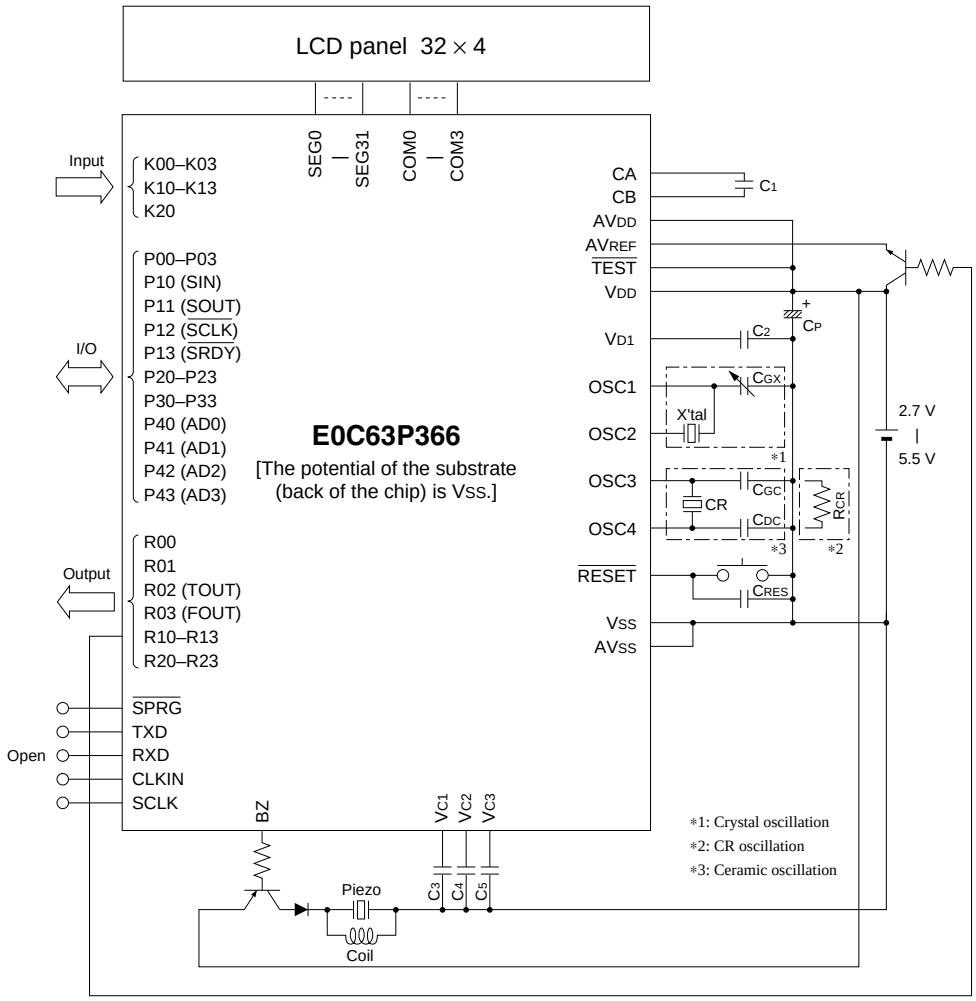
  (1) Design the product and implement the IC on the board so that it is shielded from visible radiation in actual use.

  (2) The inspection process of the product needs an environment that shields the IC from visible radiation.

  (3) As well as the face of the IC, shield the back and side too.

CHAPTER 8 BASIC EXTERNAL WIRING DIAGRAM

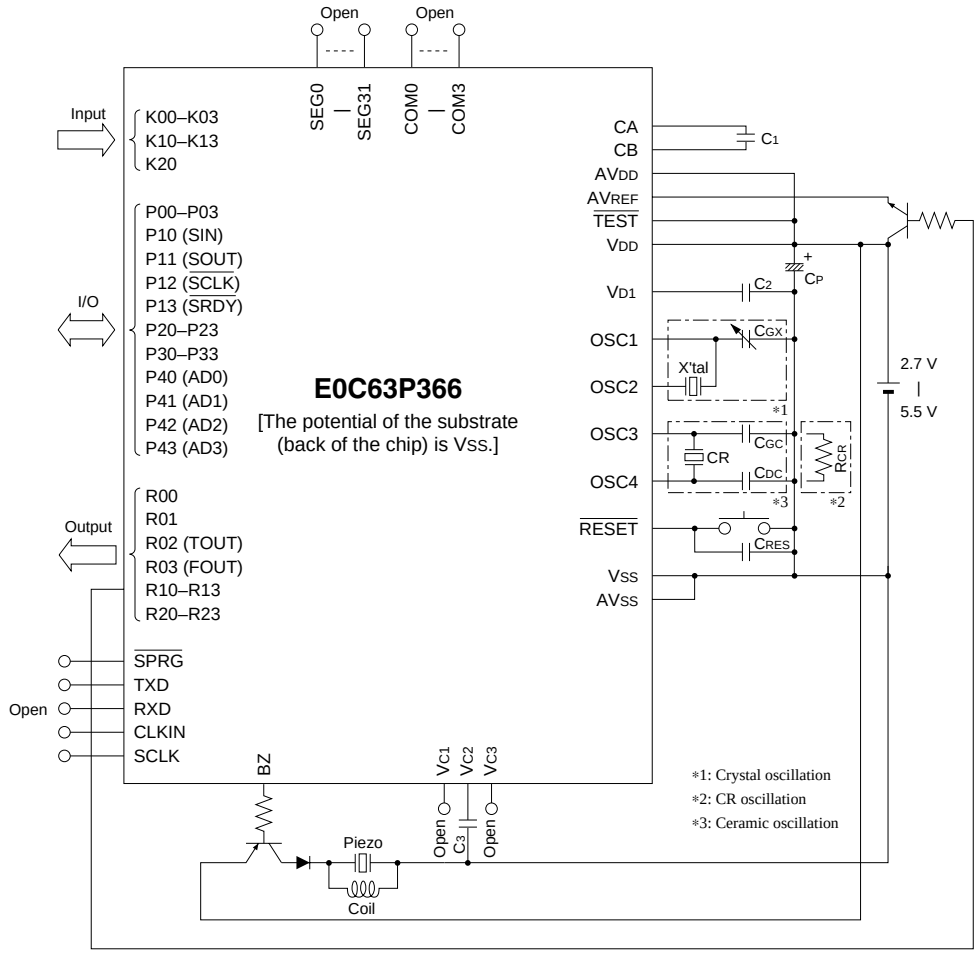
• Normal operating mode (when used as E0C63358 OTP)



X'tal	Crystal oscillator	32.768 kHz, CI (Max.) = 34 kΩ
CGX	Trimmer capacitor	5–25 pF
CR	Ceramic oscillator	4 MHz (3.0 V)
CGC	Gate capacitor	100 pF
CDC	Drain capacitor	100 pF
RCR	Resistor for OSC3 CR oscillation	91 kΩ (1.8 MHz/3.0 V)
C1–C5	Capacitor	0.2 µF
CP	Capacitor	3.3 µF
CRES	RESET terminal capacitor	0.1 µF

Note: The above table is simply an example, and is not guaranteed to work.

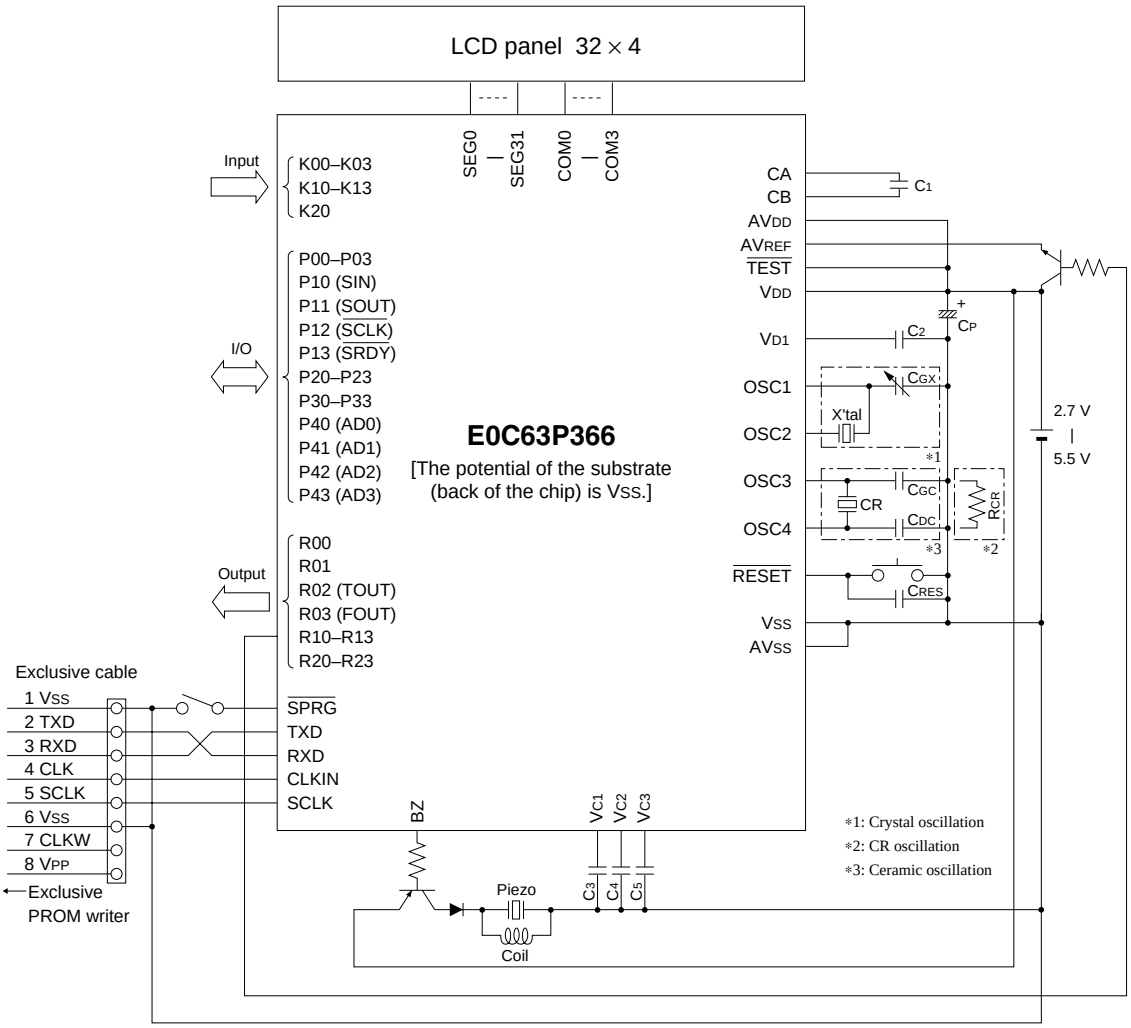
• Normal operating mode (when used as E0C63158 OTP)



X'tal	Crystal oscillator	32.768 kHz, CI (Max.) = 34 kΩ
CGX	Trimmer capacitor	5–25 pF
CR	Ceramic oscillator	4 MHz (3.0 V)
CGC	Gate capacitor	100 pF
CDC	Drain capacitor	100 pF
RCR	Resistor for OSC3 CR oscillation	91 kΩ (1.8 MHz/3.0 V)
C1–C3	Capacitor	0.2 µF
CP	Capacitor	3.3 µF
CRES	RESET terminal capacitor	0.1 µF

Note: The above table is simply an example, and is not guaranteed to work.

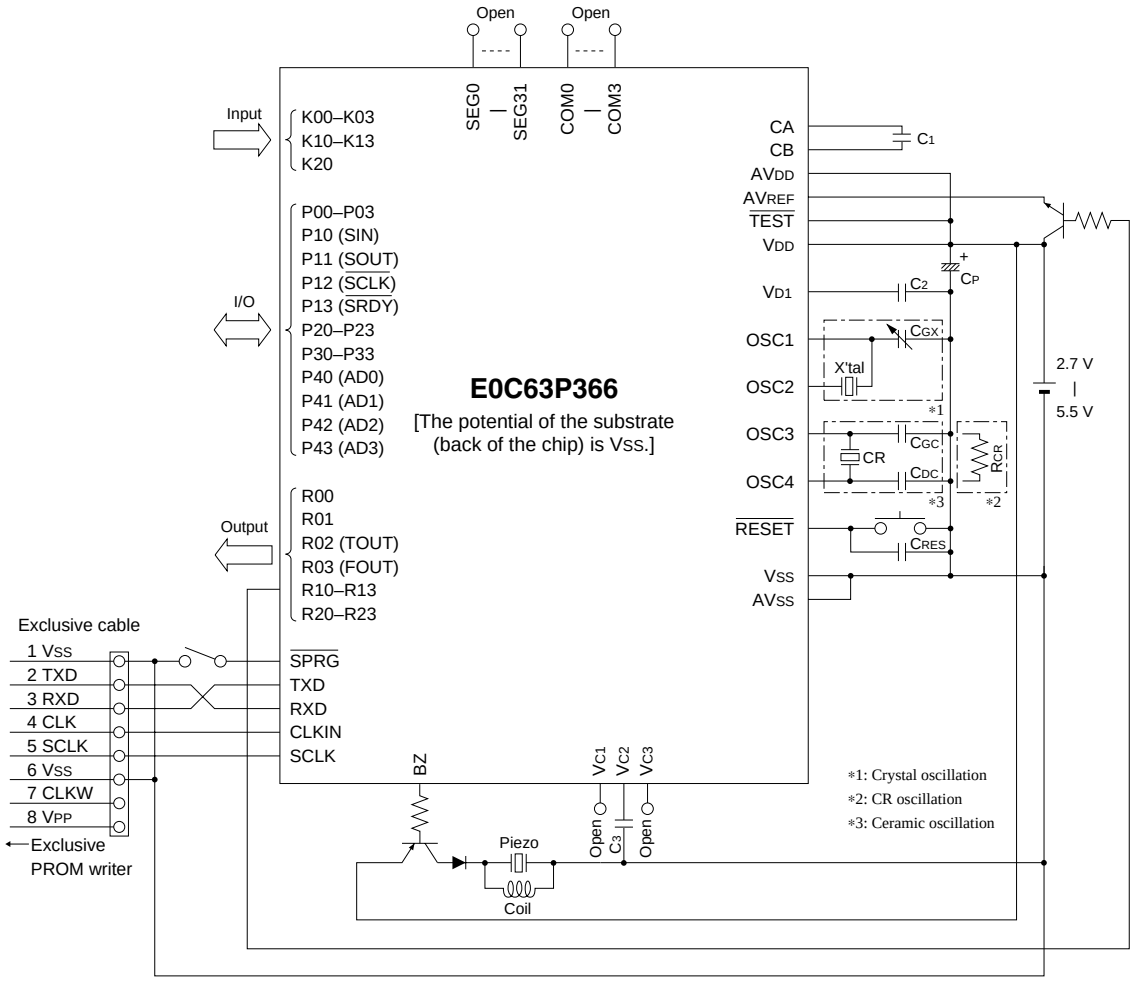
• Serial programming mode (when used as E0C63358 OTP)



X'tal	Crystal oscillator	32.768 kHz, CI (Max.) = 34 kΩ
CGX	Trimmer capacitor	5–25 pF
CR	Ceramic oscillator	4 MHz (3.0 V)
CGC	Gate capacitor	100 pF
CDC	Drain capacitor	100 pF
RCR	Resistor for OSC3 CR oscillation	91 kΩ (1.8 MHz/3.0 V)
C1–C5	Capacitor	0.2 µF
CP	Capacitor	3.3 µF
CRES	RESET terminal capacitor	0.1 µF

Note: The above table is simply an example, and is not guaranteed to work.

• Serial programming mode (when used as E0C63158 OTP)



X'tal	Crystal oscillator	32.768 kHz, CI (Max.) = 34 kΩ
CGX	Trimmer capacitor	5–25 pF
CR	Ceramic oscillator	4 MHz (3.0 V)
CGC	Gate capacitor	100 pF
CDC	Drain capacitor	100 pF
RCR	Resistor for OSC3 CR oscillation	91 kΩ (1.8 MHz/3.0 V)
C1–C3	Capacitor	0.2 µF
CP	Capacitor	3.3 µF
CRES	RESET terminal capacitor	0.1 µF

Note: The above table is simply an example, and is not guaranteed to work.

CHAPTER 9 ELECTRICAL CHARACTERISTICS

Note: The electrical characteristics of the E0C63P366 are different from those of the E0C63358/63158. The following characteristic values should be used as reference values when the E0C63P366 is used as a development tool.

9.1 Absolute Maximum Rating

(VSS=0V)

Item	Symbol	Rated value	Unit
Supply voltage	VDD	-0.5 to 7.0	V
Input voltage (1)	VI	-0.5 to VDD + 0.3	V
Input voltage (2)	VIOSC	-0.5 to VD1 + 0.3	V
Permissible total output current *1	ΣIVDD	10	mA
Operating temperature	Topr	-20 to 70	°C
Storage temperature *2	Tstg	-65 to 150	°C
Soldering temperature / time	Tsol	260°C, 10sec (lead section)	–
Permissible dissipation *3	PD	250	mW

*1 The permissible total output current is the sum total of the current (average current) that simultaneously flows from the output pin (or is drawn in).
*2 The storage temperature cannot guarantee data holding capability.
*3 In case of plastic package (QFP15-100pin).

9.2 Recommended Operating Conditions

(Ta=-20 to 70°C)

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Supply voltage	VDD	VSS=0V	Normal mode	2.7	3.0	5.5	V
	AVDD	AVSS=0V		2.7	3.0	5.5	V
Oscillation frequency	fOSC1	Crystal oscillation		–	32.768	–	kHz
	fOSC3	CR oscillation			1800		kHz
		Ceramic oscillation				4100	kHz

9.3 DC Characteristics

Unless otherwise specified:
V_{DD}=3.0V, V_{SS}=0V, f_{OSC1}=32.768kHz, Ta=25°C, V_{D1}/V_{C1}/V_{C2}/V_{C3} are internal voltage, C_1–C_5=0.2µF

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
High level input voltage (1)	V_{IH1}		K00–03, K10–13, K20, P00–03 P10–13, P20–23, P30–33, P40–43 RXD, SCLK, CLKIN, $\overline{SPRG}$	0.8·V_{DD}		V_{DD}	V
High level input voltage (2)	V_{IH2}		$\overline{RESET}$, $\overline{TEST}$	0.9·V_{DD}		V_{DD}	V
Low level input voltage (1)	V_{IL1}		K00–03, K10–13, K20, P00–03 P10–13, P20–23, P30–33, P40–43 RXD, SCLK, CLKIN, $\overline{SPRG}$	0		0.2·V_{DD}	V
Low level input voltage (2)	V_{IL2}		$\overline{RESET}$, $\overline{TEST}$	0		0.1·V_{DD}	V
High level input current	I_{IH}	V_{IH}=3.0V	K00–03, K10–13, K20, P00–03 P10–13, P20–23, P30–33, P40–43 RXD, SCLK, CLKIN, $\overline{SPRG}$ $\overline{RESET}$, $\overline{TEST}$	0		0.5	µA
Low level input current (1)	I_{IL1}	V_{IL1}=V_{SS} No Pull-up	P40–43	-0.5		0	µA
Low level input current (2)	I_{IL2}	V_{IL2}=V_{SS} With Pull-up	K00–03, K10–13, K20, P00–03 P10–13, P20–23, P30–33, P40–43 RXD, SCLK, CLKIN, $\overline{SPRG}$ $\overline{RESET}$, $\overline{TEST}$	-16	-10	-5	µA
High level output current (1)	I_{OH1}	V_{OH1}=0.9·V_{DD}	R00–03, R10–13, R20–23, P00–03 P10–13, P20–23, P30–33, P40–43 TXD, SCLK			-1.5	mA
High level output current (2)	I_{OH2}	V_{OH2}=0.9·V_{DD}	BZ			-1.5	mA
Low level output current (1)	I_{OL1}	V_{OL1}=0.1·V_{DD}	R00–03, R10–13, R20–23, P00–03 P10–13, P20–23, P30–33, P40–43 TXD, SCLK	3			mA
Low level output current (2)	I_{OL2}	V_{OL2}=0.1·V_{DD}	BZ	3			mA
Common output current	I_{OH3}	V_{OH3}=V_{C5}-0.05V	COM0–3			-10	µA
	I_{OL3}	V_{OL3}=V_{SS}+0.05V		10			µA
Segment output current	I_{OH4}	V_{OH4}=V_{C5}-0.05V	SEG0–31			-10	µA
(during LCD output)	I_{OL4}	V_{OL4}=V_{SS}+0.05V		10			µA
Segment output current	I_{OH5}	V_{OH5}=0.9·V_{DD}	SEG0–31			-220	µA
(during DC output)	I_{OL5}	V_{OL5}=0.1·V_{DD}		220			µA

Unless otherwise specified:
V_{DD}=5.0V, V_{SS}=0V, f_{OSC1}=32.768kHz, Ta=25°C, V_{D1}/V_{C1}/V_{C2}/V_{C3} are internal voltage, C_1–C_5=0.2µF

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
High level input voltage (1)	V_{IH1}		K00–03, K10–13, K20, P00–03 P10–13, P20–23, P30–33, P40–43 RXD, SCLK, CLKIN, $\overline{SPRG}$	0.8·V_{DD}		V_{DD}	V
High level input voltage (2)	V_{IH2}		$\overline{RESET}$, $\overline{TEST}$	0.9·V_{DD}		V_{DD}	V
Low level input voltage (1)	V_{IL1}		K00–03, K10–13, K20, P00–03 P10–13, P20–23, P30–33, P40–43 RXD, SCLK, CLKIN, $\overline{SPRG}$	0		0.2·V_{DD}	V
Low level input voltage (2)	V_{IL2}		$\overline{RESET}$, $\overline{TEST}$	0		0.1·V_{DD}	V
High level input current	I_{IH}	V_{IH}=5.0V	K00–03, K10–13, K20, P00–03 P10–13, P20–23, P30–33, P40–43 RXD, SCLK, CLKIN, $\overline{SPRG}$ $\overline{RESET}$, $\overline{TEST}$	0		0.5	µA
Low level input current (1)	I_{IL1}	V_{IL1}=V_{SS} No Pull-up	P40–43	-0.5		0	µA
Low level input current (2)	I_{IL2}	V_{IL2}=V_{SS} With Pull-up	K00–03, K10–13, K20, P00–03 P10–13, P20–23, P30–33, P40–43 RXD, SCLK, CLKIN, $\overline{SPRG}$ $\overline{RESET}$, $\overline{TEST}$	-25	-15	-10	µA
High level output current (1)	I_{OH1}	V_{OH1}=0.9·V_{DD}	R00–03, R10–13, R20–23, P00–03 P10–13, P20–23, P30–33, P40–43 TXD, SCLK			-3	mA
High level output current (2)	I_{OH2}	V_{OH2}=0.9·V_{DD}	BZ			-3	mA
Low level output current (1)	I_{OL1}	V_{OL1}=0.1·V_{DD}	R00–03, R10–13, R20–23, P00–03 P10–13, P20–23, P30–33, P40–43 TXD, SCLK	6			mA
Low level output current (2)	I_{OL2}	V_{OL2}=0.1·V_{DD}	BZ	6			mA
Common output current	I_{OH3}	V_{OH3}=V_{C5}-0.05V	COM0–3			-10	µA
	I_{OL3}	V_{OL3}=V_{SS}+0.05V		10			µA
Segment output current	I_{OH4}	V_{OH4}=V_{C5}-0.05V	SEG0–31			-10	µA
(during LCD output)	I_{OL4}	V_{OL4}=V_{SS}+0.05V		10			µA
Segment output current	I_{OH5}	V_{OH5}=0.9·V_{DD}	SEG0–31			-660	µA
(during DC output)	I_{OL5}	V_{OL5}=0.1·V_{DD}		660			µA

9.4 Analog Circuit Characteristics and Power Current Consumption

Unless otherwise specified:
V_{DD}=3.0V, V_{SS}=0V, f_{OSC1}=32.768kHz, C_G=25pF, Ta=25°C, V_{D1}/V_{C1}/V_{C2}/V_{C3} are internal voltage, C_1–C_5=0.2µF

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
LCD drive voltage	V_{C1}	Connect 1 MΩ load resistor between V_{SS} and V_{C1} (without panel load)		1/2·V_{C2} -0.1		1/2·V_{C2} ×0.95	V
	V_{C2}	Connect 1 MΩ load resistor between V_{SS} and V_{C2} (without panel load)		Typ. ×0.88	2.10	Typ. ×1.12	V
	V_{C3}	Connect 1 MΩ load resistor between V_{SS} and V_{C3} (without panel load)		3/2·V_{C2} ×0.95		3/2·V_{C2}	V
SVD voltage	V_{SVD}	SVDS0–3="0"		–	–	–	V
		SVDS0–3="1"		–	–	–	
		SVDS0–3="2"		–	–	–	
		SVDS0–3="3"		–	–	–	
		SVDS0–3="4"		–	–	–	
		SVDS0–3="5"		–	–	–	
		SVDS0–3="6"		–	–	–	
		SVDS0–3="7"		–	–	–	
		SVDS0–3="8"		–	–	–	
		SVDS0–3="9"		–	–	–	
		SVDS0–3="10"		–	–	–	
		SVDS0–3="11"		–	–	–	
		SVDS0–3="12"		–	–	–	
		SVDS0–3="13"		–	–	–	
		SVDS0–3="14"		2.50	2.70	2.90	
		SVDS0–3="15"		2.60	2.80	3.00	
SVD circuit response time	t_{SVD}					100	µS
Current consumption	I_{OP}	During HALT Normal mode LCD power OFF	32.768kHz		2.5	6	µA
		During HALT Normal mode *1 LCD power ON	32.768kHz		37	60	µA
		During execution Normal mode *1 LCD power ON	32.768kHz (Crystal oscillation)		120	200	µA
			1.8MHz (CR oscillation)		0.6	0.9	mA
			4MHz (Ceramic oscillation)		0.8	1.2	mA

*1 Without panel load. The SVD circuit and the A/D converter are OFF. AV_{REF} is open.

A/D converter characteristic

Unless otherwise specified:
AV_{DD}=V_{DD}=2.7 to 3.6V, AV_{SS}=V_{SS}=0V, Ta=-25 to 75°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Resolution			8	8	8	bit
Error		3.6V≤V_{DD}≤5.5V Fconv=OSC3/2 or OSC1	-3		3	LSB
		2.7V≤V_{DD}≤3.6V Fconv=OSC3/2 or OSC1	-3		3	LSB
Convertion time	t_{conv}	Fconv=OSC3/2=2MHz			10.5	µS
		Fconv=OSC1=32kHz			641	µS
Input voltage			AV_{SS}		AV_{REF}	V
Reference voltage	AV_{REF}		0.9		AV_{DD}	V
AV_{REF} resistance			15	50		kΩ

9.5 Oscillation Characteristics

The oscillation characteristics change depending on the conditions (components used, board pattern, etc.). Use the following characteristics as reference values.

OSC1 crystal oscillation circuit

Unless otherwise specified:

VDD=3.0V, VSS=0V, fOSC1=32.768kHz, CG=25pF, CD=built-in, Ta=-20 to 70°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start voltage	Vsta	tsta≤3sec (VDD)	2.7			V
Oscillation stop voltage	Vstp	tstp≤10sec (VDD)	2.7			V
Built-in capacitance (drain)	CD	Including the parasitic capacitance inside the IC (in chip)		18		pF
Frequency/voltage deviation	∂f/∂V	VDD=2.7 to 5.5V			5	ppm
Frequency/IC deviation	∂f/∂IC		-10		10	ppm
Frequency adjustment range	∂f/∂CG	CG=5 to 25pF		50		ppm
Harmonic oscillation start voltage	Vhho	CG=5pF (VDD)	5.5			V
Permitted leak resistance	Rleak	Between OSC1 and VDD, VSS	200			MΩ

OSC3 ceramic oscillation circuit

Unless otherwise specified:

VDD=3.0V, VSS=0V, Ceramic oscillator: 4MHz, CGC=CDC=100pF, Ta=-20 to 70°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start voltage	Vsta	Normal mode (VDD)	2.7			V
Oscillation start time	tsta	VDD=2.7 to 5.5V			5	mS
Oscillation stop voltage	Vstp	Normal mode (VDD)	2.7			V

OSC3 CR oscillation circuit

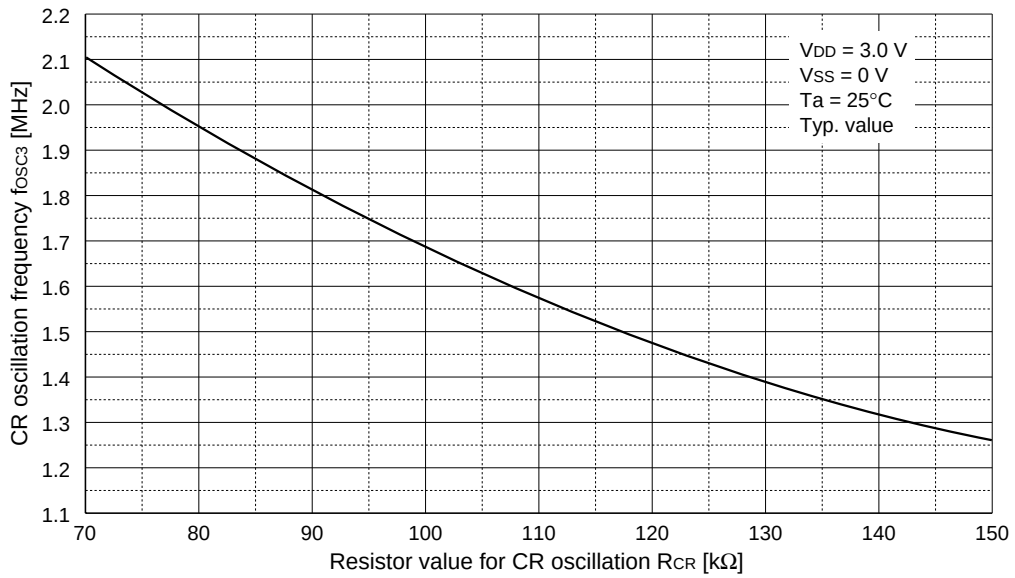
Unless otherwise specified:

VDD=3.0V, VSS=0V, RCR=91kΩ, Ta=25°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation frequency dispersion	fOSC3		-30	1.8MHz	30	%
Oscillation start voltage	Vsta	Normal mode (VDD)	2.7			V
Oscillation start time	tsta	VDD=2.7 to 5.5V			3	mS
Oscillation stop voltage	Vstp	Normal mode (VDD)	2.7			V

OSC3 CR oscillation frequency-resistance characteristic

The oscillation characteristics change depending on the conditions (components used, board pattern, etc.). Use the following characteristics as reference values and evaluate the characteristics on the actual product.



9.6 Serial Interface AC Characteristics

Clock synchronous master mode

• During 32 kHz operation

Condition: V_{DD}=3.0V, V_{SS}=0V, Ta=25°C, V_{IH1}=0.8V_{DD}, V_{IL1}=0.2V_{DD}, V_{OH}=0.8V_{DD}, V_{OL}=0.2V_{DD}

Item	Symbol	Min.	Typ.	Max.	Unit
Transmitting data output delay time	tsmd			5	µS
Receiving data input set-up time	tsms	10			µS
Receiving data input hold time	tsmh	5			µS

• During 1 MHz operation

Condition: V_{DD}=3.0V, V_{SS}=0V, Ta=25°C, V_{IH1}=0.8V_{DD}, V_{IL1}=0.2V_{DD}, V_{OH}=0.8V_{DD}, V_{OL}=0.2V_{DD}

Item	Symbol	Min.	Typ.	Max.	Unit
Transmitting data output delay time	tsmd			200	nS
Receiving data input set-up time	tsms	400			nS
Receiving data input hold time	tsmh	200			nS

Clock synchronous slave mode

• During 32 kHz operation

Condition: V_{DD}=3.0V, V_{SS}=0V, Ta=25°C, V_{IH1}=0.8V_{DD}, V_{IL1}=0.2V_{DD}, V_{OH}=0.8V_{DD}, V_{OL}=0.2V_{DD}

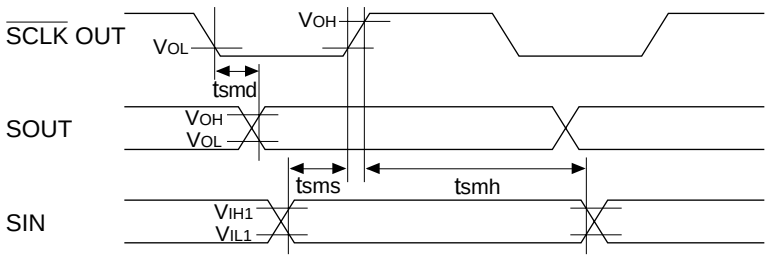
Item	Symbol	Min.	Typ.	Max.	Unit
Transmitting data output delay time	tssd			10	µS
Receiving data input set-up time	tsss	10			µS
Receiving data input hold time	tssh	5			µS

• During 1 MHz operation

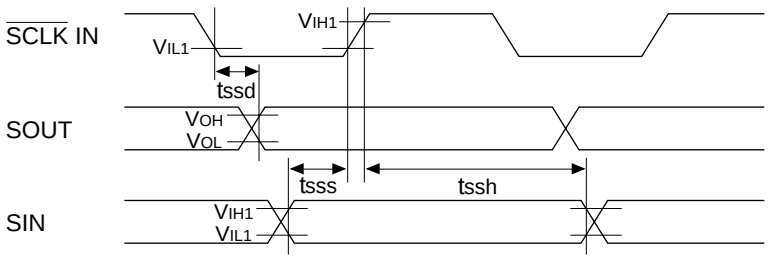
Condition: V_{DD}=3.0V, V_{SS}=0V, Ta=25°C, V_{IH1}=0.8V_{DD}, V_{IL1}=0.2V_{DD}, V_{OH}=0.8V_{DD}, V_{OL}=0.2V_{DD}

Item	Symbol	Min.	Typ.	Max.	Unit
Transmitting data output delay time	tssd			500	nS
Receiving data input set-up time	tsss	400			nS
Receiving data input hold time	tssh	200			nS

<Master mode>

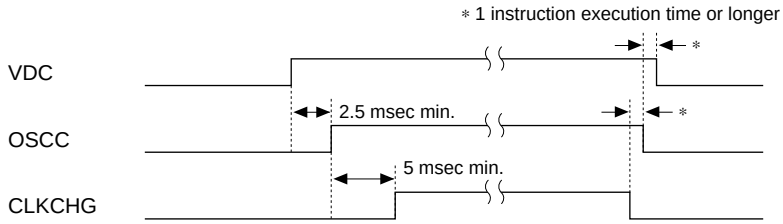


<Slave mode>



9.7 Timing Chart

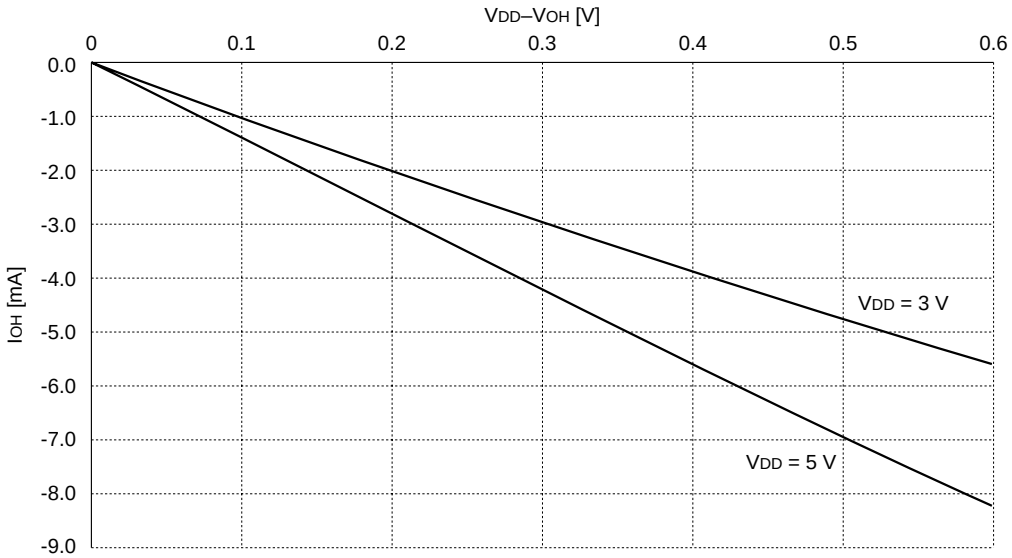
System clock switching



In the E0C63P366, the VDC register value does not affect the V_{D1} voltage level. However, note that the CPU clock cannot be switched from OSC1 to OSC3 using the CLKCHG register if the VDC register value is "0".
Set the VDC register to "1" before switching the CPU clock from OSC1 to OSC3 in the E0C63P366.
When using the E0C63P366 as a development tool for the E0C63358/63158, switch the operating voltage using the VDC register according to the control sequence of the model (refer to the "Technical Manual").

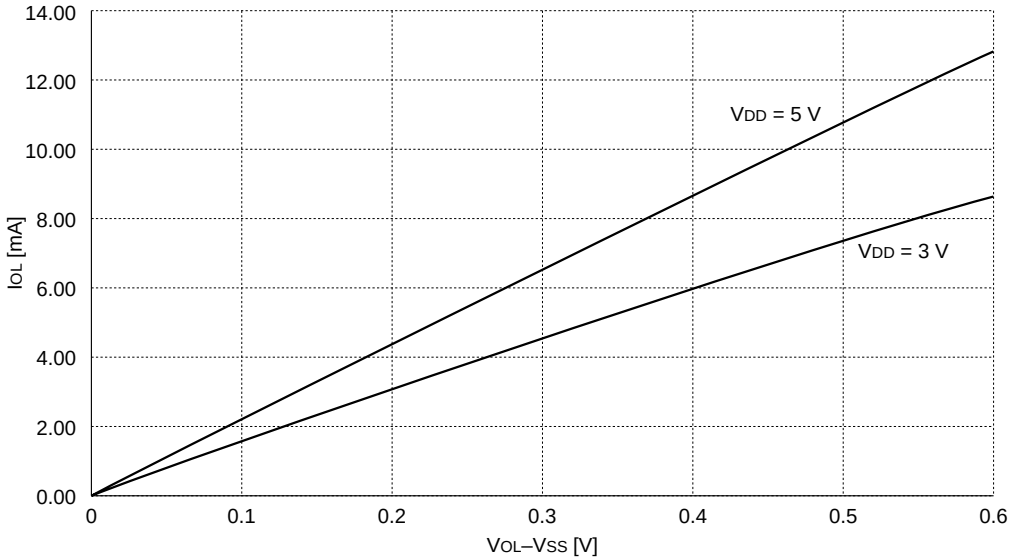
9.8 Characteristics Curves (reference value)

High level output current (Rxx, Pxx, BZ, Typ. value)



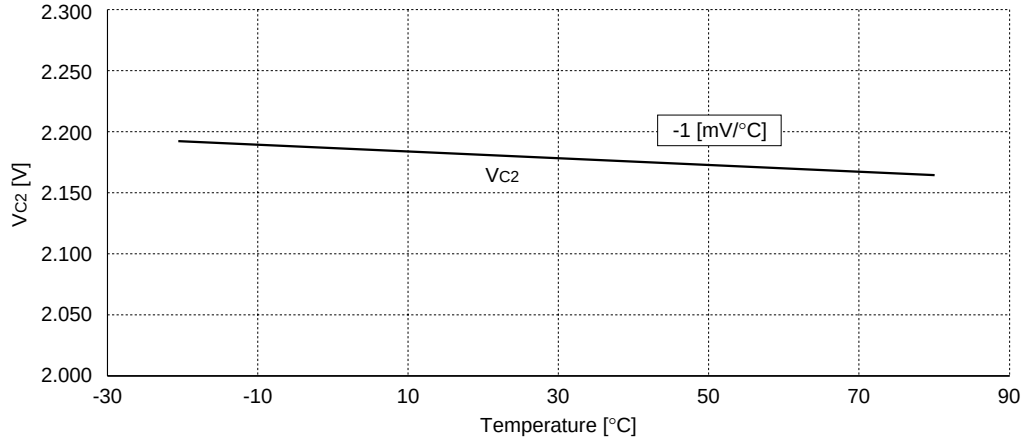
OSC1: 32.768kHz crystal oscillation, V_{SS} = 0V, no panel load, C_{GX} = 25pF, C_{GC} = C_{DC} = 100pF, C_1–C_5 = 0.2µF
This graph is provided only for reference and the characteristic varies according to mounting conditions, parts used and the measurement environment.
The output terminals should be used within the rated value of permissible total output current.

Low level output current (Rxx, Pxx, BZ, Typ. value)



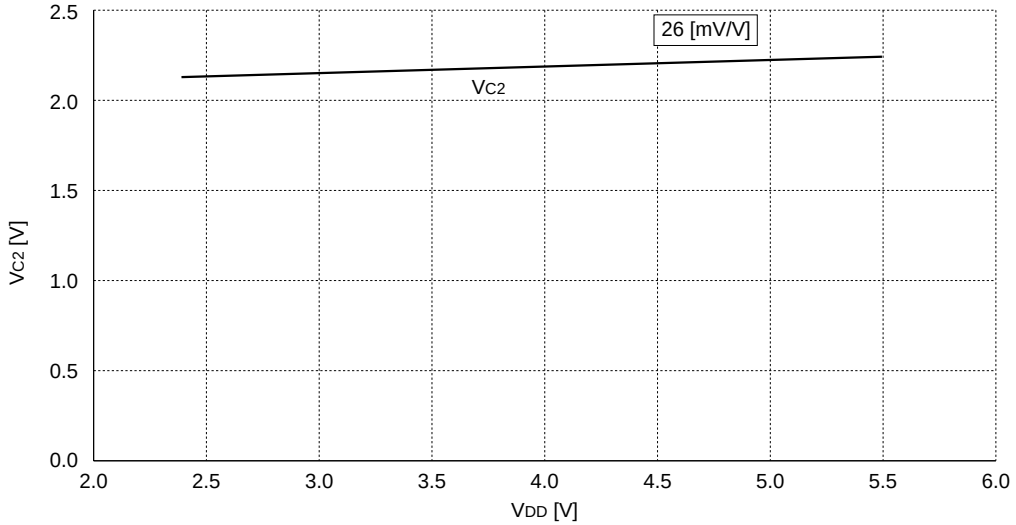
OSC1: 32.768kHz crystal oscillation, V_{SS} = 0V, no panel load, C_{GX} = 25pF, C_{GC} = C_{DC} = 100pF, C_1–C_5 = 0.2µF
This graph is provided only for reference and the characteristic varies according to mounting conditions, parts used and the measurement environment.
The output terminals should be used within the rated value of permissible total output current.

V_{C2} output voltage-temperature characteristic (Typ. value)



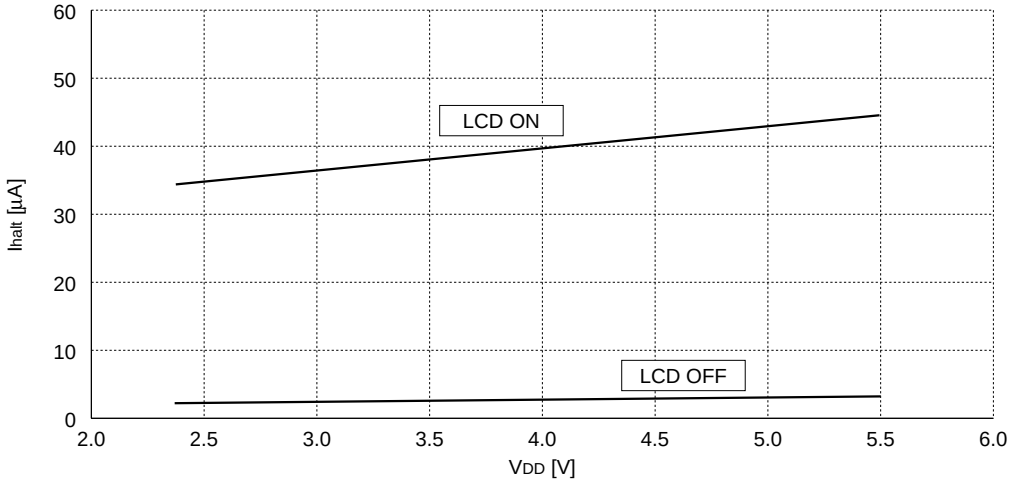
OSC1: 32.768kHz crystal oscillation, V_{DD} = 3V, V_{SS} = 0V, no panel load, C_{GX} = 25pF, C_{GC} = C_{DC} = 100pF, C_1–C_5 = 0.2µF
The LCD drive voltage output from the internal LCD drive power circuit varies depending on temperature. This graph is provided only for reference and the characteristic varies according to mounting conditions, parts used and the measurement environment.

V_{C2} output voltage-supply voltage characteristic (Typ. value)



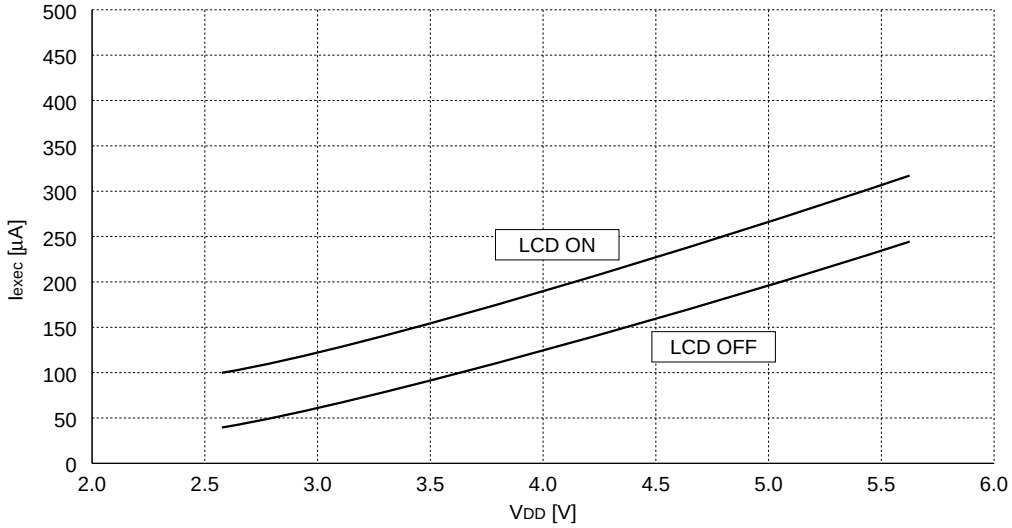
OSC1: 32.768kHz crystal oscillation, Ta =25°C, V_{SS} = 0V, no panel load, C_{GX} = 25pF, C_{GC} = C_{DC} = 100pF, C_1–C_5 = 0.2µF
This graph is provided only for reference and the characteristic varies according to mounting conditions, parts used and the measurement environment.

Power current-supply voltage characteristic (HALT state)



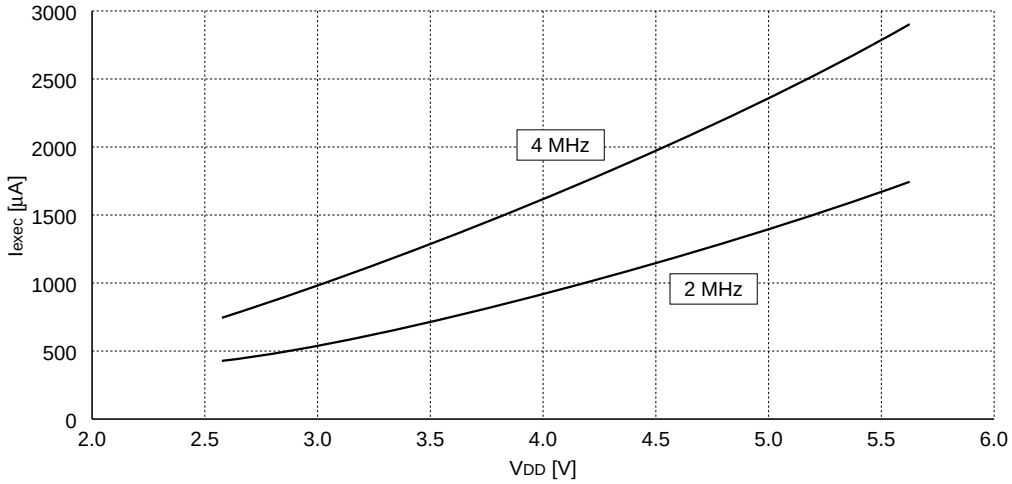
OSC1: 32.768kHz crystal oscillation, Ta =25°C, VSS = 0V, no panel load, CGX = 25pF, CGC = CDC = 100pF
This graph is provided only for reference and the characteristic varies according to mounting conditions, parts used and the measurement environment.

Power current-supply voltage characteristic (RUN state with OSC1 clock)



OSC1: 32.768kHz crystal oscillation, Ta =25°C, VSS = 0V, no panel load, CGX = 25pF, CGC = CDC = 100pF
This graph is provided only for reference and the characteristic varies according to mounting conditions, parts used and the measurement environment.

Power current-supply voltage characteristic (RUN state with OSC3 clock)



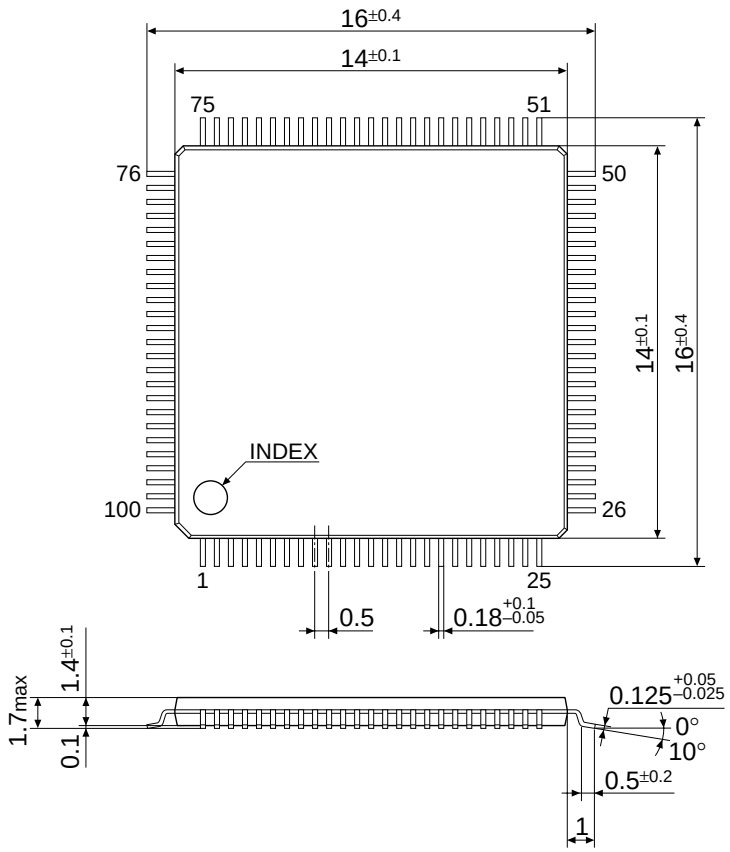
OSC1: 32.768kHz crystal oscillation, Ta =25°C, VSS = 0V, no panel load, CGX = 25pF, CGC = CDC = 100pF
This graph is provided only for reference and the characteristic varies according to mounting conditions, parts used and the measurement environment.

CHAPTER 10 PACKAGE

10.1 Plastic Package

QFP15-100pin

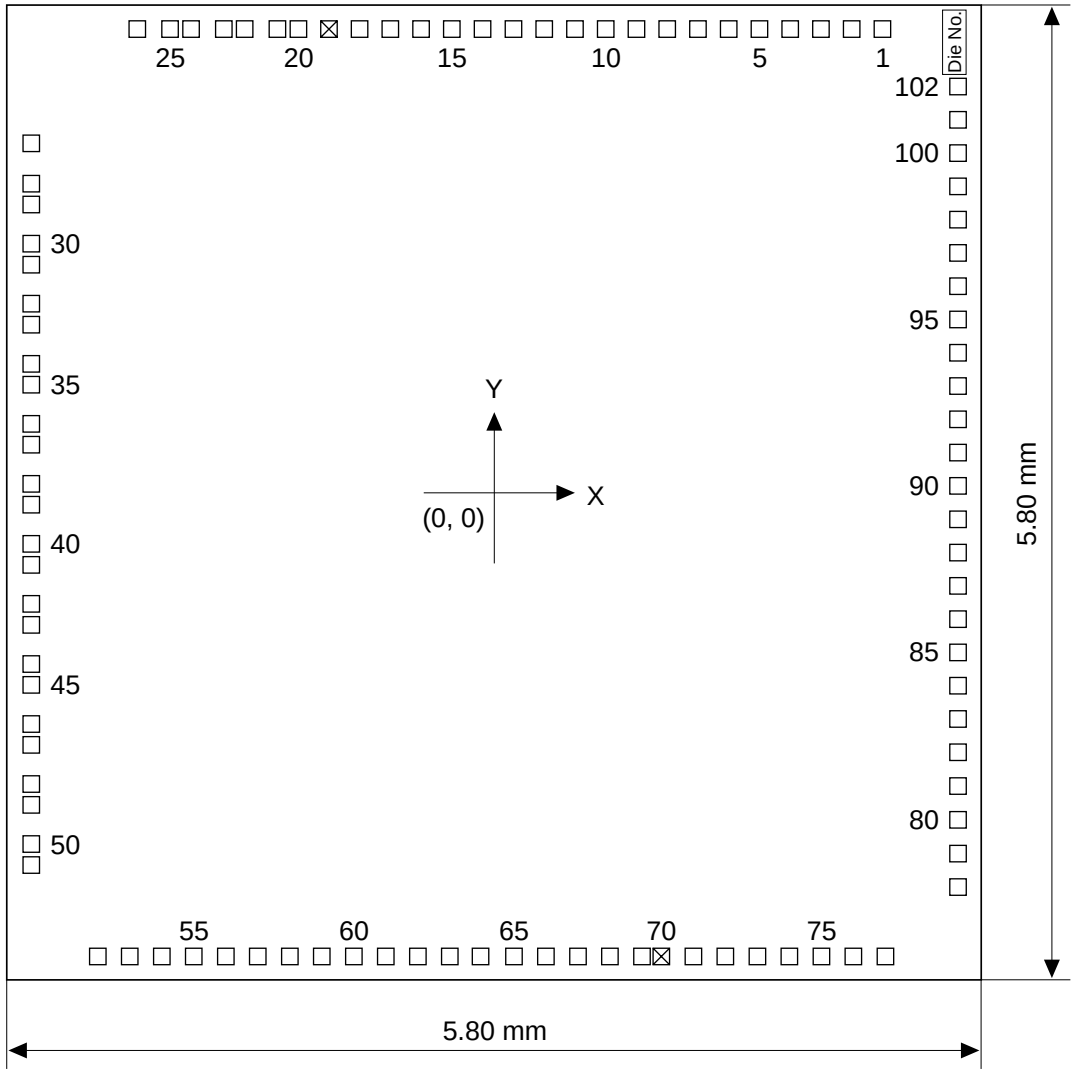
(Unit: mm)



The dimensions are subject to change without notice.

CHAPTER 11 PAD LAYOUT

11.1 Diagram of Pad Layout



Chip thickness: 400 µm
Pad opening: 98 µm

11.2 Pad Coordinates

Unit: mm

No.	Pad name	X	Y	No.	Pad name	X	Y	No.	Pad name	X	Y
1	R13	2,309	2,759	35	SEG15	-2,757	643	69	V_{DD}	878	-2,759
2	R12	2,126	2,759	36	SEG16	-2,757	410	70	N.C.	993	-2,759
3	R11	1,943	2,759	37	SEG17	-2,757	286	71	$\overline{RESET}$	1,184	-2,759
4	R10	1,760	2,759	38	SEG18	-2,757	53	72	$\overline{TEST}$	1,374	-2,759
5	R03	1,577	2,759	39	SEG19	-2,757	-71	73	AVREF	1,565	-2,759
6	R02	1,394	2,759	40	SEG20	-2,757	-304	74	AV_{DD}	1,755	-2,759
7	R01	1,211	2,759	41	SEG21	-2,757	-429	75	AV_{SS}	1,946	-2,759
8	R00	1,028	2,759	42	SEG22	-2,757	-661	76	RXD	2,136	-2,759
9	BZ	845	2,759	43	SEG23	-2,757	-786	77	TXD	2,327	-2,759
10	K00	662	2,759	44	SEG24	-2,757	-1,019	78	SCLK	2,759	-2,346
11	K01	479	2,759	45	SEG25	-2,757	-1,143	79	P43	2,759	-2,147
12	K02	296	2,759	46	SEG26	-2,757	-1,376	80	P42	2,759	-1,946
13	K03	113	2,759	47	SEG27	-2,757	-1,500	81	P41	2,759	-1,745
14	K10	-71	2,759	48	SEG28	-2,757	-1,733	82	P40	2,759	-1,544
15	K11	-254	2,759	49	SEG29	-2,757	-1,857	83	P33	2,759	-1,346
16	K12	-437	2,759	50	SEG30	-2,757	-2,090	84	P32	2,759	-1,148
17	K13	-620	2,759	51	SEG31	-2,757	-2,215	85	P31	2,759	-950
18	K20	-803	2,759	52	CLKIN	-2,361	-2,759	86	P30	2,759	-752
19	N.C.	-986	2,759	53	$\overline{SPRG}$	-2,171	-2,759	87	P23	2,759	-554
20	SEG0	-1,167	2,759	54	COM0	-1,980	-2,759	88	P22	2,759	-356
21	SEG1	-1,292	2,759	55	COM1	-1,790	-2,759	89	P21	2,759	-158
22	SEG2	-1,487	2,759	56	COM2	-1,599	-2,759	90	P20	2,759	41
23	SEG3	-1,611	2,759	57	COM3	-1,409	-2,759	91	P13	2,759	239
24	SEG4	-1,806	2,759	58	CB	-1,218	-2,759	92	P12	2,759	437
25	SEG5	-1,931	2,759	59	CA	-1,028	-2,759	93	P11	2,759	635
26	SEG6	-2,126	2,759	60	V_{C3}	-837	-2,759	94	P10	2,759	833
27	SEG7	-2,757	2,079	61	V_{C2}	-647	-2,759	95	P03	2,759	1,031
28	SEG8	-2,757	1,839	62	V_{C1}	-456	-2,759	96	P02	2,759	1,229
29	SEG9	-2,757	1,715	63	V_{SS}	-266	-2,759	97	P01	2,759	1,427
30	SEG10	-2,757	1,482	64	OSC1	-83	-2,759	98	P00	2,759	1,625
31	SEG11	-2,757	1,357	65	OSC2	116	-2,759	99	R23	2,759	1,823
32	SEG12	-2,757	1,125	66	V_{D1}	306	-2,759	100	R22	2,759	2,021
33	SEG13	-2,757	1,000	67	OSC3	497	-2,759	101	R21	2,759	2,219
34	SEG14	-2,757	767	68	OSC4	687	-2,759	102	R20	2,759	2,417

N.C. : No Connection

APPENDIX PROM PROGRAMMING

A.1 Outline of Writing Tools

Writing of PROM data onto a microcomputer with a Flash EEPROM (hereinafter called Flash built-in microcomputer) is done by exclusive writing tools.
The writing tools, Universal ROM Writer II, Adapter Socket, Universal ROM Writer II Control Software and HEX Data Converter, are provided in the following four tool packages:

1) Universal ROM Writer II Package

This package includes the main unit of Universal ROM Writer II, and can be used for the E0C63 Family and E0C88 Family Flash built-in microcomputers.

2) Adapter Socket Package

Adapter Socket is included. As the socket differs depending on the model of the Flash built-in microcomputer, the package is provided according to model. For the E0C63P366, the E0C63P366 Adapter Socket Package is provided.

3) Universal ROM Writer II Control Software Package

Universal ROM Writer II Control Software is included. As the software differs depending on the model, the package is provided according to model. For the E0C63P366, the E0C63P366 Universal ROM Writer II Control Software Package is provided.

4) Development Tool Package

The HEX Data Converter converts the temporary code generated by the linker into HEX format (Motorola S2 format) and generates a data file that can be loaded to the Universal ROM Writer II Control Software. This software is provided as the Development Tool package of each mask ROM model. Refer to the "Development Tool Manual" included in the package for details.

A.1.1 Universal ROM Writer II

This is a PROM writer for Flash built-in microcomputers. In the onboard serial programming mode, this PROM writer can write data to the PROM in the Flash built-in microcomputer on the target board without other hardware tools. In the parallel programming mode, the PROM writer can write data to the Flash built-in microcomputer through the Adapter Socket for each model installed on it.
It is connected to the host computer (personal computer) via an RS-232C. Its writing and other operations are controlled by the personal computer.
Note that serial programming on the target board and parallel programming with the Adapter Socket cannot be done simultaneously.

Specifications of Control Section

The following describes the switches and connectors on the Universal ROM Writer II.
Figure A.1.1.1 shows an external view of the Universal ROM Writer II control section.

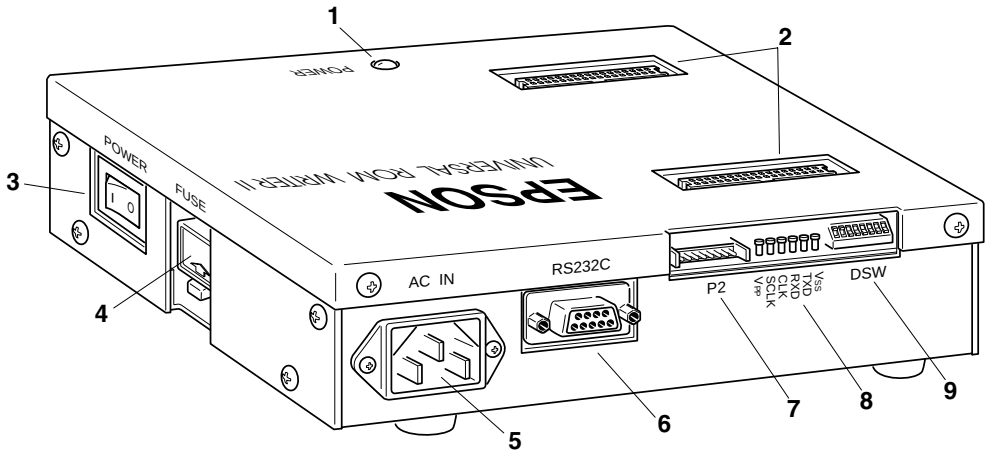


Fig. A.1.1.1 External view of Universal ROM Writer II control section

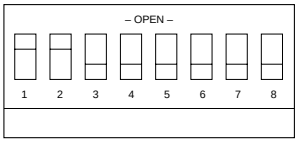
Table A.1.1.1 lists the functions of the control section.

Table A.1.1.1 Functions of control section

No.	Position	Marking	Name	Function
1	Top	POWER	Power on LED	This LED lights in red with the Universal ROM Writer II power on.
2	Top		Connectors for Adapter Socket	These are connectors for Adapter Socket for Flash built-in microcomputers. The Adapter Socket is necessary for parallel programming. Turn the power off before connecting or removing Adapter Socket.
3	Side	POWER	Power switch	This is the power on/off switch of the Universal ROM Writer II. Power on with I; power off with O.
4	Side	FUSE	Fuse holder	A 1 A cartridge fuse is included.
5	Rear	AC IN	Power input connector	This is the connector for the power cable.
6	Rear	RS232C	RS-232C connector	This is the connector for the RS-232C cable. Secure the cable connector with the screws on the cable connector.
7	Rear	P2	SIO connector	This is the connector for the SIO cable. The SIO cable is necessary for serial programming.
8	Rear	VSS, TXD, RXD, CLK, SCLK, VPP	Check pins	These pins are connected to the VSS, TXD, RXD, CLK, SCLK and the VPP signals in the SIO interface. They can be connected to the target board instead of the SIO cable.
9	Rear	DSW	DIP switch	This switch is used to set the transmission rate. It has been set to 9600 bps at the factory.

DIP Switch Setting

The transmission rate of the RS-232C interface between the Universal ROM Writer II and a personal computer can be set with this switch. Figure A.1.1.2 shows the DIP switch settings.



Note: Set all of SW3–8 down.

SW1	SW2	Settings
OPEN	OPEN	Transmission rate = 9600 bps, 8-bit character, 1 stop bit, no parity (factory setting)
DOWN	OPEN	Transmission rate = 4800 bps, 8-bit character, 1 stop bit, no parity
OPEN	DOWN	Transmission rate = 2400 bps, 8-bit character, 1 stop bit, no parity
DOWN	DOWN	Transmission rate = 1200 bps, 8-bit character, 1 stop bit, no parity

Fig. A.1.1.2 DIP switch settings

A.1.2 Adapter Socket

Adapter Socket is used by installing on the Universal ROM Writer II. It is provided according to the model of the Flash built-in microcomputer.

Installing to Universal ROM Writer II

Turn the Universal ROM Writer II off, then install the Adapter Socket to the top connector of the Universal ROM Writer II.

There is a projection on the adapter socket connector to prevent miss-insertion. Lineup the Adapter Socket to fit to the notch of the Universal ROM Writer II connector.

When disconnecting the Adapter Socket, first turn the Universal ROM Writer II off.

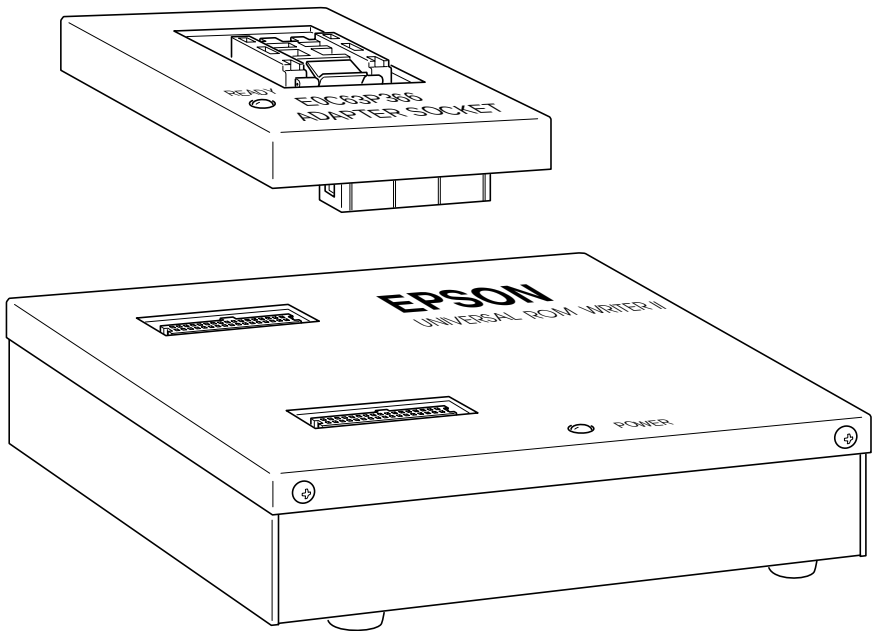
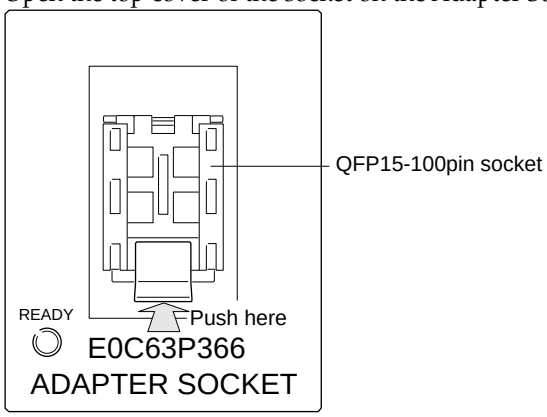


Fig. A.1.2.1 Installation to Universal ROM Writer II

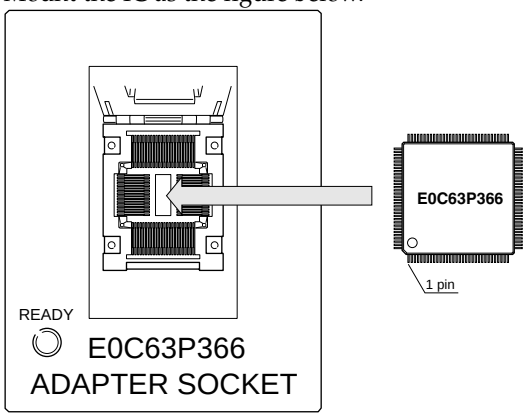
Mounting E0C63P366

Make sure that the Universal ROM Writer II is off or the READY LED on the Adapter Socket is lit when mounting or removing the E0C63P366.

(1) Open the top cover of the socket on the Adapter Socket.

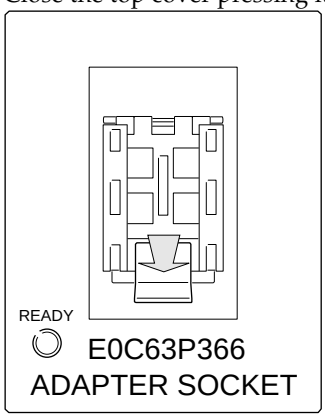


(2) Mount the IC as the figure below.



Note: Be aware that the IC may be damaged if parallel programming is performed by installing the IC to the Adapter Socket in the wrong direction.

(3) Close the top cover pressing it from above.



A.1.3 Universal ROM Writer II Control Software

This software controls the Universal ROM Writer II with the personal computer.
It can realize functions equivalent to a general PROM writer such as writing to the Flash built-in microcomputer and erasing PROM data, PROM data loading from file, saving to file, and PROM data display, by the control of a personal computer.
The Universal ROM Writer II connected to a personal computer through the RS-232C operats by commands sent from the personal computer. Universal ROM Writer II control software interprets the entered commands and controls the Universal ROM Writer II according the commands.
In addition, the Universal ROM Writer II Control Software transfers the firmware (63P366.FRM) to the Universal ROM Writer II, and displays the firmware file name as a prompt.
The file name of the Universal ROM Writer II Control Software is as follows:

- US63P366.EXE (for Windows95/98 English version)
- JP63P366.EXE (for Windows95/98 Japanese version)

A.2 System Environment and Connection

A.2.1 System environment

Prepare a personal computer system as a host computer and the data for writing into the Flash built-in microcomputer.

(1) Personal computer

- IBM-PC/AT or compatible

(2) OS

- Windows95/98 English or Japanese version (MS-DOS prompt is used)

(3) PROM writing tools

- Universal ROM Writer II
- Universal ROM Writer II Control Software
- E0C63P366 Adapter Socket (required only for parallel programming)

(4) Writing data

- Object (program) file (~.srf)
- Segment option document file (~.sdc)

A.2.2 RS-232C settings

Factory settings of the Universal ROM Writer II have been made at 9600 bps transmission rate, 8-bit data, non parity, and 1 stop bit. Transmission rate can be switched using the DIP switch on the Universal ROM Writer II. Since the data format has been fixed, adapt the personal computer setting using the "MODE" command. Furthermore, COM1 must be used as the RS-232C port for this system. Check the port setting of the personal computer before use.
An example for setting 9600 bps transmission rate is shown below.

Example: C>MODE COM1: 9600, n, 8, 1, P

A.2.3 System connection

Connect the Universal ROM Writer II to the personal computer and install the Adapter Socket to the connector on top of the Universal ROM Writer II.
The Adapter Socket is not necessary for serial programming (onboard writing).

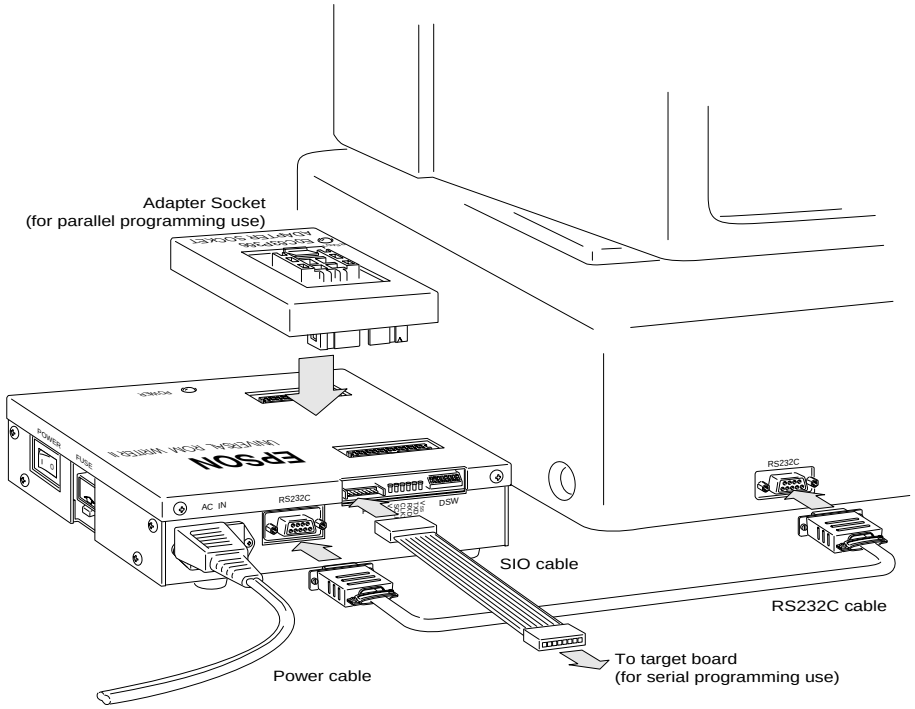


Fig. A.2.3.1 System connection diagram

The system should be connected according to the following procedure.

(1) Connecting power cable

A dedicated power cable is included in the Universal ROM Writer II Package. Connect the power cable to the AC IN connector on the rear panel of the Universal ROM Writer II.

(2) Confirmation of power off status

Make sure the power for the personal computer and the Universal ROM Writer II is switched off.

(3) Connecting RS-232C cable

Connect the Universal ROM Writer II and personal computer with the RS-232C cable. There is an RS-232C connector on the rear panel of the Universal ROM Writer II. The supplied RS-232C cable is for IBM-PC/AT use (9 pins - 9 pins). Figure A.2.3.2 shows the connection of the RS-232C cable, and Table A.2 3.1 lists the signal specifications.

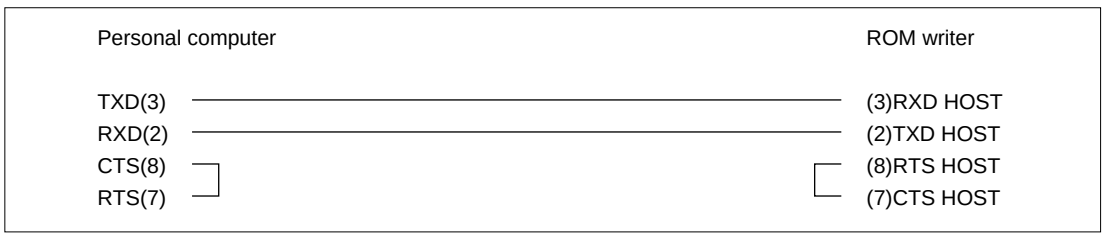


Fig. A.2.3.2 RS-232C cable connection

Table A.2.3.1 Signal specifications

Pin No.	Signal name	Description	Remarks
3	TXD	Transmit data from personal computer to ROM writer	
2	RXD	Receive data of personal computer (from ROM writer)	
7	RTS	Request to send seignal from personal computer	Always on
8	CTS	Clear to send signal from ROM writer	Always on
5	SG	Signal ground	

Connect the 9-pin (male-pin) connector of the RS-232C cable to the Universal ROM Writer II. After connecting the Universal ROM Writer II to the personal computer, secure the connectors with the screws.

(4) Installing Adapter Socket (for parallel programming)

Install the Adapter Socket to the top connector of the Universal ROM Writer II when the power of the Universal ROM Writer II is off.
There is a projection on the Adapter Socket connector that prevents miss-insertion, adapt it to the notch of the Universal ROM Writer II connector and install the Adapter Socket.
Also when disconnecting the Adapter Socket, turn the Universal ROM Writer II off.
In serial programming, it is not necessary to install the Adapter Socket.

(5) Connecting SIO cable (for serial programming)

In serial programming (onboard writing), the SIO cable should be used to connect the target board and the Universal ROM Writer II. Make sure that the target board and the Universal ROM Writer II are off when connecting and disconnecting the SIO cable.
In parallel programming, it is not necessary to connect the SIO cable.

<Notes>

- Serial programming and parallel programming cannot be done simultaneously.
- Turn the power of all equipment off before connecting and disconnecting cables.
- Turn the Universal ROM Writer II off before connecting and disconnecting the Universal ROM Writer II, Adapter Socket and SIO cable.
- Make sure to set COM1 as the RS-232C port.

A.3 PROM Serial Programming Mode

The PROM serial programming mode should be set when writing data to the PROM using a serial transfer from the Universal ROM Writer II. This mode will be mainly used for the programming of chip products, because the programming can be done even when the IC has already been mounted on the board.
To create data to be written to the code ROM, use the E0C63 assembler similar to the E0C63358/E0C63158. To create data to be written to the segment option ROM use the segment option generator SOG63358 similar to the E0C63358.

A.3.1 Connecting to target board

The SIO cable which is attatched to the Universal ROM Writer II should be used for onboard programming of the E0C63P366 on the target board. Figure A.3.1.1 shows the connection of the SIO cable and Table A.3.1.1 lists the signal specifications.

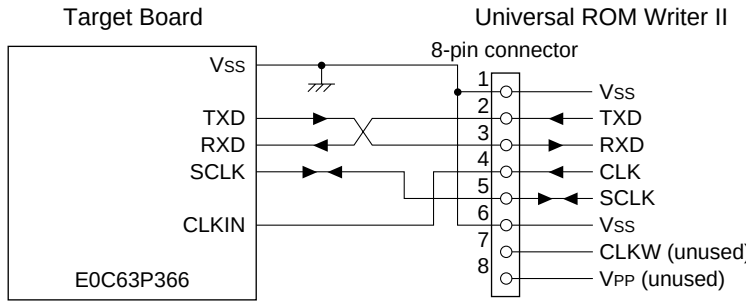


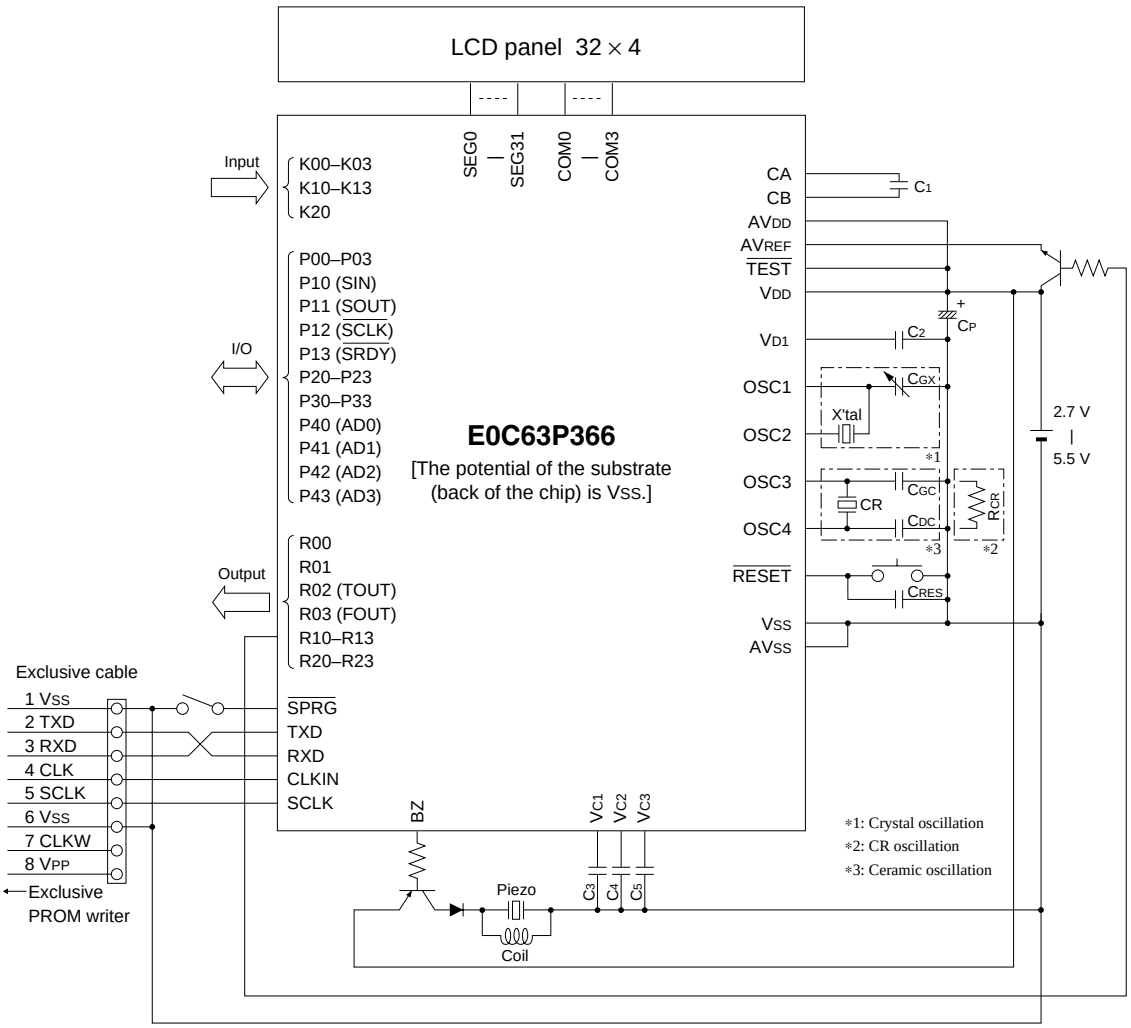
Fig. A.3.1.1 SIO cable connection diagram

Table A.3.1.1 Signal specifications

Connector pin No.	Signal name	Description
1, 6	Vss	Ground pin (Connect to the Vss pin of the E0C63P366.)
2	TXD	Transmit data from the PROM writer to the E0C63P366 (Connect to the RXD pin of the E0C63P366.)
3	RXD	Transmit data from the E0C63P366 (Connect to the TXD pin of the E0C63P366.)
4	CLK	Clock from the PROM writer (1 MHz)
5	SCLK	Serial clock between the PROM writer and the E0C63P366 (Input or output)
7	CLKW	Clock from the PROM writer (3.072 MHz)
8	VPP	VPP (5 V, 12.5 V) supply pin from the PROM writer

In other modes, do not connect signals to the RXD, TXD and SCLK pins of the IC.

A.3.2 Sample connection diagram in PROM serial programming mode



X'tal	Crystal oscillator	32.768 kHz, CI (Max.) = 34 kΩ
CGX	Trimmer capacitor	5–25 pF
CR	Ceramic oscillator	4 MHz (3.0 V)
CGC	Gate capacitor	100 pF
CDC	Drain capacitor	100 pF
RCR	Resistor for OSC3 CR oscillation	91 kΩ (1.8 MHz/3.0 V)
C1–C5	Capacitor	0.2 µF
CP	Capacitor	3.3 µF
CRES	RESET terminal capacitor	0.1 µF

Note: The above table is simply an example, and is not guaranteed to work.

Fig. A.3.2.1 Sample connection diagram in serial programming mode

- Supply 5 V source voltage between the VDD and VSS terminals in serial programming mode. The operatng clock (1 MHz) for serial programming is supplied from the CLK pin of the SIO cable to the E0C63P366.
- When using the serial programming method, provide a switch that can pull the RESET terminal dow to low level on the target board.
- Do not connect the CLKW signal and VPP power from the Universal ROM Writer II.

A.3.3 PROM serial programming procedure

(1) Set the required terminal for serial programming as follows:

$\overline{\text{SPRG}}$:A switch should be provided on the target board to set the $\overline{\text{SPRG}}$ terminal level to Low.

Note: The $\overline{SPRG}$ terminal must be fixed at a Low level in the programming mode and at a High level or open in the normal operation mode. Changing the voltage level may damage the IC.

CLKIN, RXD, TXD, SCLK: Connect to the PROM writer.

(2) Turn the IC (user target board) power (+5 V) on.

(3) Turn the PROM writer on.

(4) Controls the $\overline{\text{RESET}}$ and $\overline{\text{SPRG}}$ terminals as shown in Figure A.3.3.1.

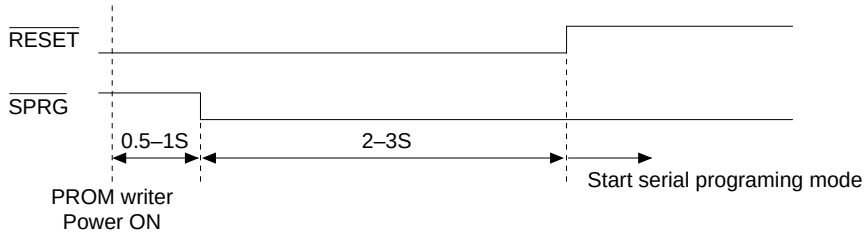


Fig. A.3.3.1 Timing chart for entering serial programming mode

(5) Start up the US63P366.EXE or JP63P366.EXE in the personal computer, then load the 63P366.FRM file. This allows serial programming to begin.

After setting this mode, writing data is controlled by the PROM writer.
Refer to Section A.5, "Writing Prosedure and PROM Writer Command" for the following operations.

A.4 PROM Parallel Programming Mode

In the PROM parallel programming mode, the exclusive PROM writer (Universal ROM Writer II) transfers data in parallel to the IC installed on the PROM writer to write data to it. The terminal setting is done by the PROM writer. Thus there is no precaution on mode setting or board design.
To create data to be written to the code ROM, use the E0C63 assembler similar to the E0C63358/E0C63158. To create data to be written to the segment option ROM use the segment option generator SOG63358 similar to the E0C63358.

A.4.1 PROM parallel programming procedure

(1) Connect the PROM writer to the personal computer using the RS-232C cable.

(2) Install the Adapter Socket to the PROM writer.

(3) Turn on the personal computer and then the PROM writer.

(4) Mount the E0C63P366 on the Adapter Socket (refer to Section A.1.2, "Adapter Socket").
Make sure that the Universal ROM Writer II is off or the READY LED on the Adapter Socket is lit when mounting or removing the E0C63P366.

(5) Start up the US63P366.EXE or JP63P366.EXE in the personal computer, then load the 63P366.FRM file. This allows parallel programming to begin.

Refer to Section A.5, "Writing Prosedure and PROM Writer Command" for the following operations.

A.5 Writing Procedure and PROM Writer Command

A.5.1 Executing HEX63xxx

Execute the HEX63xxx to create the HEX data file (C3xxxyyy.HSA, C3xxxyyy.LSA) from an object file (C3xxxyyy.SRF).
Refer to the "Development Tool Manual" of each model for details of the HEX63xxx.

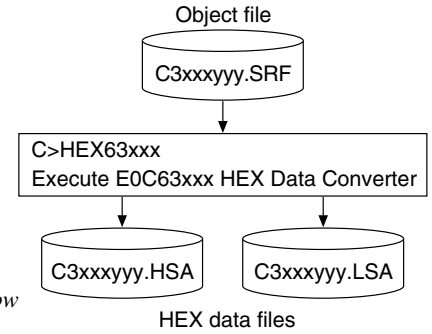


Fig. A.5.1.1 HEX63xxx execution flow

A.5.2 Executing segment option data converter

Execute the SDCP366 to create the segment option ROM HEX data file (CP366xxx.OSA) from a segment option document file (C3358xxx.SDC).

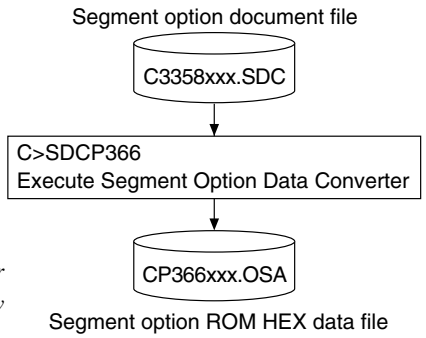


Fig. A.5.2.1 Segment option data converter execution flow

Copy the "SDCP366.EXE" to the current directory.

```
C>SDCP366↵
```

When the above command is executed, the message shown below appears on the screen for entering a segment option document file name.

```
*** Please input SOG document file name ***
Input File Name == c3358xxx.sdc↵
```

Next, enter an output file name.

```
*** Please output SOG HEX file name ***
Output File Name == cp366xxx.osa↵
```

The following message is displayed after the segment option ROM HEX file (CP366xxx.OSA) is generated.

```
Making file is completed
```

A.5.3 Writing HEX data (PROM programming)

(1) Setting RS-232C

An example for setting 9600 bps transmission rate is shown below.

```
C>MODE  COM1:9600,n,8,1,P↵
```

(2) Starting Universal ROM Writer II Control Software

Copy the "US63P366.EXE" or "JP63P366.EXE" and "63P366.FRM" files to the current directory.

```
C>US63P366↵      (Windows95/98 English version)
C>JP63P366↵      (Windows95/98 Japanese version)
```

When the above command is executed, the following message is displayed.
However, when performing serial programming, the E0C63P366 must be set in the serial programming mode before executing US63P366 or JP63P366. Refer to Section A.3.3, "PROM serial programming procedure", for details.

```
UNIVERSAL ROM WRITER     Ver. x.xx
(C)COPYRIGHT 199x SEIKO EPSON CORPORATION

LOADING 63P366 FIRMWARE PROGRAM Ver. x.xx
..........
```

After displaying the message, a prompt as below is displayed.

```
63P366:
```

(3) Loading HEX data

To load the code ROM HEX files (C3358xxx.HSA, C3358xxx.LSA or C3158xxx.HSA, C3158xxx.LSA) to the Universal ROM Writer II, enter as below.

```
63P366:LI c3358xxx↵
```

To load the segment option ROM HEX file (CP366xxx.OSA), enter as below.

```
63P366:LO cp366xxx↵
```

(4) Writing data

Clear (erase) the contents of the code ROM and perform erase check using the following command. All the PROM data bits are cleared to "1" at shipment but erase it once to initialize the contents.

```
63P366:ERSI /E↵      (for parallel programming mode)
63P366:FERSI /E↵     (for serial programming mode)
```

Section A.5.3, "PROM writer commands", for details.

Write code ROM data and verify the written data using the following command.

```
63P366:WI /V↵        (for parallel programming mode)
63P366:FWI /V↵       (for serial programming mode)
```

Clear (erase) the contents of the segment option ROM and perform erase check using the following command.

```
63P366:ERSC /E↵      (for parallel programming mode)
63P366:FERSC /E↵     (for serial programming mode)
```

Write segment option ROM data and verify the written data using the following command.

```
63P366:WC /V↵        (for parallel programming mode)
63P366:FWC /V↵       (for serial programming mode)
```

Note: Recommended option data is written to the LCD segment opotion PROM before the IC is shipped. Modifying the LCD segment opotion is done at the user's own risk.

A.5.4 PROM writer commands

This section explains the commands which can be used in US63P366 and JP63P366.
The following symbols have been used in the explanation:

_ indicates space
A parameter enclosed by [ ] can be omitted
, indicates selection item
↲ indicates Enter key

1 WRITE command (code ROM) for parallel programming

Operation: **WI [_ / V]↲**

Option: /V ..... Verifies data from the code ROM start address after writing.

Description: The buffer RAM data in the PROM writer is written to the code ROM area in the E0C63P366 on the socket. The accessed code ROM address is displayed during writing.
Option specification should be done every time the command is executed.

Example: WI↲ ..... Writes data to the code ROM. Data is not verified.

2 WRITE command (segment option ROM) for parallel programming

Operation: **WC [_ / V]↲**

Option: /V ..... Verifies data from the segment option ROM start address after writing.

Description: The buffer RAM data in the PROM writer is written to the segment option ROM area in the E0C63P366 on the socket. The accessed segment option ROM address is displayed during writing.
Option specification should be done every time the command is executed.

Example: WC↲ ..... Writes data to the segment option ROM. Data is not verified.

3 READ command (code ROM) for parallel programming

Operation: **RI [_ / V]↲**

Option: /V ..... Verifies data from the code ROM start address after reading.

Description: The contents of the code ROM in the E0C63P366 on the socket are read to the buffer RAM in the PROM writer. The accessed code ROM address is displayed during reading.
Option specification should be done every time the command is executed.

Example: RI↲ ..... Reads the contents of the code ROM to the buffer RAM in the PROM writer. Data is not verified.

4 READ command (segment option ROM) for parallel programming

Operation: **RC [_ / V]↲**

Option: /V ..... Verifies data from the segment option ROM start address after reading.

Description: The contents of the segment option ROM in the E0C63P366 on the socket are read to the buffer RAM in the PROM writer. The accessed segment option ROM address is displayed during reading.
Option specification should be done every time the command is executed.

Example: RC↲ ..... Reads the contents of the segment option ROM to the buffer RAM in the PROM writer. Data is not verified.

5 VERIFY command (code ROM) for parallel programming

Operation: **VI**↵

Description: Verifies the contents of the code ROM in the E0C63P366 on the socket and the contents of the buffer RAM in the PROM writer. The accessed code ROM address is displayed during verification. When an error occurs, verification stops. At this time, the address and data of the code ROM and the buffer RAM data are displayed. To resume verification, press Enter.

6 VERIFY command (segment option ROM) for parallel programming

Operation: **VC**↵

Description: Verifies the contents of the segment option ROM in the E0C63P366 on the socket and the contents of the buffer RAM in the PROM writer. The accessed segment option ROM address is displayed during verification. When an error occurs, verification stops. At this time, the address and data of the segment option ROM and the buffer RAM data are displayed. To resume verification, press Enter.

7 ERASE command (code ROM) for parallel programming

Operation: **ERSI [_ / E]**↵

Option: /E ..... Performs erase check from the code ROM start address after erasing.

Description: Erases the code ROM in the E0C63P366 on the socket.
Option specification should be done every time the command is executed.

8 ERASE command (segment option ROM) for parallel programming

Operation: **ERSC [_ / E]**↵

Option: /E ..... Performs erase check from the segment option ROM start address after erasing.

Description: Erases the segment option ROM in the E0C63P366 on the socket.
Option specification should be done every time the command is executed.

9 ERASE ALL command for parallel programming

Operation: **ERSA [_ / E]**↵

Option: /E ..... Perform erase check after erasing.

Description: Erases the code ROM and segment option ROM in the E0C63P366 on the socket and then removes write protect.

10 ERASE CHECK command (code ROM) for parallel programming

Operation: **EI**↵

Description: Checks that the code ROM in the E0C63P366 on the socket has been erased. The code ROM address is displayed during checking. When an error occurs, erase check stops. At this time, the address and data of the code ROM are displayed. To resume erase check, press Enter.

11 ERASE CHECK command (segment option ROM) for parallel programming

Operation: **EC**↵

Description: Checks that the segment option ROM in the E0C63P366 on the socket has been erased. The segment option ROM address is displayed during checking. When an error occurs, erase check stops. At this time, the address and data of the segment option ROM are displayed. To resume erase check, press Enter.

12 PROTECT command for parallel programming

Operation: **PROTECT**↵

Description: Sets the protect bit of the ROM in the E0C63P366 on the socket.
When the protect bit has been set, execution of all the commands except for ERSA are disabled.

13 WRITE command (code ROM) for serial programming

Operation: **FWI [_ / V]**↵

Option: /V ..... Verifies data from the code ROM start address after writing.

Description: The buffer RAM data in the PROM writer is written to the E0C63P366 code ROM on the target board connected to the PROM writer. The accessed code ROM address is displayed during writing.
Option specification should be done every time the command is executed.

Example: `FWI`↵ ..... Writes data to the code ROM. Data is not verified.

14 WRITE command (segment option ROM) for serial programming

Operation: **FWC [_ / V]**↵

Option: /V ..... Verifies data from the segment option ROM start address after writing.

Description: The buffer RAM data in the PROM writer is written to the E0C63P366 segment option ROM on the target board connected to the PROM writer. The accessed segment option ROM address is displayed during writing.
Option specification should be done every time the command is executed.

Example: `FWC`↵ ..... Writes data to the segment option ROM. Data is not verified.

15 READ command (code ROM) for serial programming

Operation: **FRI [_ / V]**↵

Option: /V ..... Verifies data from the code ROM start address after reading.

Description: The contents of the E0C63P366 code ROM on the target board connected to the PROM writer are read to the buffer RAM in the PROM writer. The accessed code ROM address is displayed during reading.
Option specification should be done every time the command is executed.

Example: `FRI`↵ ..... Reads the contents of the code ROM to the buffer RAM in the PROM writer. Data is not verified.

16 READ command (segment option ROM) for serial programming

Operation: **FRC [_ / V]**↵

Option: /V ..... Verifies data from the segment option ROM start address after reading.

Description: The contents of the E0C63P366 segment option ROM on the target board connected to the PROM writer are read to the buffer RAM in the PROM writer. The accessed segment option ROM address is displayed during reading.
Option specification should be done every time the command is executed.

Example: `FRC`↵ ..... Reads the contents of the segment option ROM to the buffer RAM in the PROM writer. Data is not verified.

17 VERIFY command (code ROM) for serial programming

Operation: **FVI**↵

Description: Verifies the contents of the E0C63P366 code ROM on the target board connected to the PROM writer and the contents of the buffer RAM in the PROM writer. The accessed code ROM address is displayed during verification. When an error occurs, verification stops. At this time, the address and data of the code ROM and the buffer RAM data are displayed. To resume verification, press Enter.

18 VERIFY command (segment option ROM) for serial programming

Operation: **FVC**↵

Description: Verifies the contents of the E0C63P366 segment option ROM on the target board connected to the PROM writer and the contents of the buffer RAM in the PROM writer. The accessed segment option ROM address is displayed during verification. When an error occurs, verification stops. At this time, the address and data of the segment option ROM and the buffer RAM data are displayed. To resume verification, press Enter.

19 ERASE command (code ROM) for serial programming

Operation: **FERSI [_ / E]**↵

Option: /E ..... Performs erase check from the code ROM start address after erasing.

Description: Erases the E0C63P366 code ROM on the target board connected to the PROM writer. Option specification should be done every time the command is executed.

20 ERASE command (segment option ROM) for serial programming

Operation: **FERSC [_ / E]**↵

Option: /E ..... Performs erase check from the segment option ROM start address after erasing.

Description: Erases the E0C63P366 segment option ROM on the target board connected to the PROM writer. Option specification should be done every time the command is executed.

21 ERASE ALL command for serial programming

Operation: **FERSA [_ / E]**↵

Option: /E ..... Perform erase check after erasing.

Description: Erases the code ROM and segment option ROM in the E0C63P366 on the target board connected to the PROM writer and then removes write protect.

22 ERASE CHECK command (code ROM) for serial programming

Operation: **FEI**↵

Description: Checks that the E0C63P366 code ROM on the target board connected to the PROM writer has been erased. The code ROM address is displayed during checking. When an error occurs, erase check stops. At this time, the address and data of the code ROM are displayed. To resume erase check, press Enter.

23 ERASE CHECK command (segment option ROM) for serial programming

Operation: **FEC**↵

Description: Checks that the E0C63P366 segment option ROM on the target board connected to the PROM writer has been erased. The segment option ROM address is displayed during checking. When an error occurs, erase check stops. At this time, the address and data of the segment option ROM are displayed. To resume erase check, press Enter.

24 PROTECT command for serial programming

Operation: **FPROTECT**↵

Description: Sets the protect bit of the E0C63P366 ROM on the target board connected to the PROM writer.
When the protect bit has been set, execution of all the commands except for FERSA are disabled.

25 LOAD command (for code ROM file)

Operation: **LI _ file name**↵

Option: file name ..... File name to be loaded (without extension)

Description: The specified code ROM file is loaded in the host computer and transferred to the PROM writer. This command loads two code ROM files converted by the HEX63xxx (high-order HEX data file and low-order HEX data file) for the code ROM. The file name should be specified without the extension.

Example: `LI_C3358001`↵ ..... Loads the C3358001.HSA and C3358001.LSA files.

26 LOAD command (for segment option ROM file)

Operation: **LO _ file name**↵

Option: file name ..... File name to be loaded (without extension)

Description: The specified segment option ROM file is loaded in the host computer and transferred to the PROM writer. This command loads a segment option ROM file changed by the SDCP366. The file name should be specified without the extension.

Example: `LO_CP366001`↵ ..... Loads the CP366001.OSA file.

27 SAVE command (for code ROM file)

Operation: **SI _ file name**↵

Option: file name ..... File name to be saved (without extension)

Description: Saves the code ROM data in the buffer RAM of the PROM writer into two files, a high-order data file with the specified name and .HSA extension and a low-order data file with the specified name and .LSA extension. The file name should be specified without the extension.

Example: `SI_C3358001`↵ ..... Saves the code ROM data into the C3358001.HSA and C3358001.LSA files.

28 SAVE command (for segment option ROM file)

Operation: **SO _ file name↵**

Option: file name ..... File name to be saved (without extension)

Description: Saves the segment option ROM data in the buffer RAM of the PROM writer into a file with the specified name and .OSA extension. The file name should be specified without the extension.

Example: `SO_CP366001↵` ..... Saves the segment option ROM data into the CP366001.OSA file.

29 DUMP command (for code ROM)

Operation: **DI [_ address 1 [_ address 2]] [_/L, /H]↵**

Option: address 1 ..... Dump start address
Can be specified within the range of 0000H to 3FE0H in 20H units.
address 2 ..... Dump end address
Can be specified within the range of 001FH to 3FFFH in 20H units.
/L ..... Displays low-order 8 bit data only (corresponding to C3xxxyyy.LSA)
/H ..... Displays high-order 5 bit data only (corresponding to C3xxxyyy.HSA)

Description: Displays the code ROM data in the buffer RAM with the specified format.
When address 1 and address 2 have been specified, data from address 1 to address 2 is displayed. When address 1 only has been specified, data for the screen size from address 1 is displayed. When both address 1 and address 2 have been omitted, data for the screen size is displayed from the address that follows the previously displayed end address (default address is 00000H).
When the /L and /H options have been omitted, ROM image data is displayed in 13-bit units. When /L has been specified, the low-order 8 bit data is displayed in the C3xxxyyy.LSA HEX file image. When /H has been specified, the high-order 5 bit data is displayed in the C3xxxyyy.HSA HEX file image. When /L or /H has been specified, the addresses are displayed according to the file.
Option specification should be done every time the command is executed.

Examples: `DI_0_1F↵` .. Displays the RAM data corresponding to the code ROM addresses 0 to 1F.

```
00000  1FF0 1EF1 1DF2 1CF3 1BF4 1AF5 19F6 18F7
00008  17F8 16F9 15FA 14FB 13FC 12FD 11FE 10FF
  :                        :
00018  1F78 1F69 1F5A 1F4B 1F3C 1F2D 1F1E 1F0F
```

`DI_0_/L↵` .. Displays data corresponding to the C3xxxyyy.LSA HEX file from address 0.

```
00000  F0 F1 F2 F3 F4 F5 F6 F7 F8 F9 FA FB FC FD FE FF
00010  FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF
  :                          :
000F0  FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF
```

30 DUMP command (for segment option ROM)

Operation: **DC [_ address 1 [_ address 2]] [_/C]↵**

Option: address 1 ..... Dump start address
Can be specified within the range of 0000H to 03E0H in 20H units.
address 2 ..... Dump end address
Can be specified within the range of 001FH to 03FFH in 20H units.
/C ..... Displays in HEX file (C3xxxyyy.SSA) format

Description: Displays the segment option ROM data in the buffer RAM with the specified format. When address 1 and address 2 have been specified, data from address 1 to address 2 is displayed. When address 1 only has been specified, data for the screen size from address 1 is displayed. When both address 1 and address 2 have been omitted, data for the screen size is displayed from the address that follows the previously displayed end address (default address is 00000H).
When /C has been omitted, ROM image data is displayed in 4-bit units. When /C has been specified, data is displayed in the C3xxxyyy.SSA HEX file image.

Examples: `DC_100_1FF↵` ..... Displays data from address 100 to address 1FF in ROM image.

```
00100  0 1 2 3 4 5 6 7 8 9 A B C D E F
00110  0 1 2 3 4 5 6 7 8 9 A B C D E F
  :                   :
001F0  0 1 2 3 4 5 6 7 8 9 A B C D E F
```

`DC_0000_/C↵` ..... Displays data from address 0 in HEX file image.

```
00000  00 01 02 03 04 05 06 07 08 09 0A 0B 0C 0D 0E 0F
00010  00 01 02 03 04 05 06 07 08 09 0A 0B 0C 0D 0E 0F
  :                               :
000F0  00 01 02 03 04 05 06 07 08 09 0A 0B 0C 0D 0E 0F
```

31 LOGGING command

Operation: **LOG _ file name↵**
LOG _ /E↵

Option: file name ..... File name to be logged for screen data, file extension included
/E ..... Terminates data logging.

Description: Data that has been displayed on the screen are saved to a file with the specified file name. The command is terminated by entering LOG_/E.

Examples: `LOG_c3358001.dat↵` ..... After this, data that will be displayed on the screen will be saved in the C3358001.DAT file.
`LOG_/E↵` ..... Logging is terminated, and data after this will not be saved.

32 MACRO execution command

Operation: **MAC _ file name↵**

Option: file name ..... Macro file name including file extension

Description: Reads the specified macro file in which commands have been recorded and executes the commands.

Example: `MAC_c3358.mac↵` ..... The macro file C3358.MAC is loaded and the commands included in the file are executed.

```
LI_c3358001
WI
```

When the file contains the commands indicated at the left, the code ROM data is loaded and written to the code ROM.

33 COMMAND HISTORY

Operation: ↑
↓

Description: Previously input commands are displayed. A command displayed can be re-executed by selecting with ↑ or ↓ and pressing Enter. Up to 20 commands can be stored in the buffer.

34 TEMPLATE

Operation: f1
f3

Description: Previously input command can be re-displayed. Pressing f1 displays the characters of the command one by one, and pressing f3 displays all the characters at once.

Example: When LI_C3358001 has been input previously.

```
f1
L
f1
LI          ..... Pressing f1 displays the characters one by one.
f1
LI_
f3
LI_C3358001 ..... Pressing f3 displays all the characters at once.
```

35 DOS command

Operation: **DOS**↵

Description: Returns to DOS temporally. To return from DOS, enter EXIT.

Example:

```
63P366:DOS↵
C> ..... Returns to DOS.

C>EXIT↵
63P366: ..... Entering EXIT returns to the program.
```

36 HELP command

Operation: **HELP**↵

Description: Command list is displayed.

37 QUIT command

Operation: **Q**↵

Description: Terminates the program and returns to DOS.

A.5.5 List of commands

No.	Item	Operation	Function
1	Parallel writing	WI [_/V]↵	Writes the RAM data to the code ROM on the socket.
2		WC [_/V]↵	Writes the RAM data to the segment option ROM on the socket.
3	Parallel reading	RI [_/V]↵	Reads data from the code ROM on the socket to the RAM.
4		RC [_/V]↵	Reads data from the segment option ROM on the socket to the RAM.
5	Parallel verification	VI↵	Compares data between the code ROM on the socket and the RAM.
6		VC↵	Compares data between the segment option ROM on the socket and the RAM.
7	Parallel erasing	ERSI [_/E]↵	Erases the code ROM on the socket.
8		ERSC [_/E]↵	Erases the segment option ROM on the socket.
9		ERSA [_/E]↵	Erases the code ROM and segment option ROM on the socket and removes write protect.
10	Parallel erase check	EI↵	Performs erase check for the code ROM on the socket.
11		EC↵	Performs erase check for the segment option ROM on the socket.
12	Parallel protection	PROTECT↵	Protects the ROM on the socket.
13			
14	Serial writing	FWI [_/V]↵	Writes the RAM data to the code ROM on the target board.
15		FWC [_/V]↵	Writes the RAM data to the segment option ROM on the target board.
16	Serial reading	FRI [_/V]↵	Reads data from the code ROM on the target board to the RAM.
17		FRC [_/V]↵	Reads data from the segment option ROM on the target board to the RAM.
18	Serial verification	FVI↵	Compares data between the code ROM on the target board and the RAM.
19		FVC↵	Compares data between the segment option ROM on the target board and the RAM.
20	Serial erasing	FERSI [_/E]↵	Erases the code ROM on the target board.
		FERSC [_/E]↵	Erases the segment option ROM on the target board.
21		FERSA [_/E]↵	Erases the code ROM and segment option ROM on the target board and removes write protect.
22	Serial erase check	FEI↵	Performs erase check for the code ROM on the target board.
23		FEC↵	Performs erase check for the segment option ROM on the target board.
24	Serial protection	FPROTECT↵	Protects the ROM on the target board.
25	Loading from file	LI_file name↵	Loads code ROM files from the host computer to the ROM writer.
26		LO_file name↵	Loads a segment option ROM file from the host computer to the ROM writer.
27	Saving to file	SI_file name↵	Saves the code ROM data in the ROM writer as two files in the host computer.
28		SO_file name↵	Saves the segment option ROM data in the ROM writer as a file in the host computer.
29	Dump	DI [_address1 [_adress2]] [_/H,/L]↵	Dumps (displays) the code ROM data in the RAM.
30		DC [_address1 [_address2]] [_/C]↵	Dumps (displays) the segment option ROM data in the RAM.
31	Logging	LOG_file name↵ LOG_/E↵	Saves data displayed on the screen. Terminates by /E.
32	Macro	MAC_file name↵	Executes the commands recorded in the macro file.
33	History	↑ ↓	Displays the commands that have been input.
34	Template	f1 or f3	Displays the previously input command.
35	DOS	DOS↵ EXIT↵	Returns to DOS temporally. Returns from DOS by entering EXIT.
36	HELP	HELP↵	Displays list of commands.
37	QUIT	Q↵	Terminates the program and returns to DOS.

- _ indicates space key.
- A parameter enclosed by [ ] can be omitted.
- , indicates selection item.
- ↵ indicates Enter key.
- Loading and saving file names must not include extension.
- Logging and macro file names must include extension.

A.5.6 Error messages

Error message	Description
ROM WRITER NOT POWER ON	The PROM writer does not respond when a start-up check command is issued.
SUM CHECK ERROR	An IPL checksum error has occurred in the PROM writer.
RAM R/W ERROR	An error has occurred during R/W check for the RAM.
FILE DATA FORMAT ERROR	There is an error in the data format of the file to be transferred.
FILE DATA SUMCHECK ERROR	There is an error in the checksum data of the file.
COMMUNICATION ERROR 1	The PROM writer does not respond when a command is issued from the host computer. The PROM writer sent NAK to the host computer. The host computer sent NAK to the PROM writer.
COMMUNICATION ERROR 2	The onboard ROM sent NAK to the PROM writer. The PROM writer sent NAK to the onboard ROM.
COMMUNICATION ERROR 3	The onboard ROM does not respond when a command is issued from the PROM writer.
WRITE ERROR ADDRESS ROM : RAM XXX XXX XXX WRITE ERROR ADDRESS ROM : RAM XXX X X	An error has occurred during writing data to the ROM (on the socket or target board). An error has occurred during checking after writing.
VERIFY ERROR ADDRESS ROM : RAM XXX XXX XXX VERIFY ERROR ADDRESS ROM : RAM XXX X X	A verification error has occurred.
ERASE ERROR ADDRESS ROM XXX XXX ERASE ERROR ADDRESS ROM XXX X	Data bit other than "1" has been detected during erase check.
COMMAND ERROR	Input format is incorrect. Option is incorrect.
FILE NOT FOUND	The specified file is not found.

A.6 PROM Programming Notes

(1) The code ROM bit data is set to "1" at shipment. Therefore, It must be programmed before operating the IC in the normal operation mode.

(2) The PROM data can be rewritten up to 100 times for both the code and segment option ROMs.

(3) The circuit board should be designed so that the terminals can switch the input signals that differ between the PROM serial programming mode and the normal operation mode.

(4) The terminals for the PROM programmer should be set correctly according to the operating mode and fixed so that they cannot be changed during operation.
Especially the $\overline{\text{SPRG}}$ terminal must be fixed at a Low level in the programming mode, while it must be fixed at a High level or must be opened in the normal operation mode. Changing the voltage level may damage the IC.

(5) When a verify error occurs even if the PROM writing has completed normally, rewrite data without erasing the PROM.

(6) Rewriting the PROM is done at on the user's own risk.

(7) Recommended option data is written to the LCD segment opotion PROM before the IC is shipped. Modifying the LCD segment opotion is done at the user's own risk.

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