EPSON

E0C88112

8-bit Single Chip Microcomputer

Wide Voltage Operation Products

- Original Architecture Core CPU
- 512K-byte Addressable Space
- Wide-range Operating Voltage (1.8V to 5.5V)
- High Speed Operation in Low Voltage (0.48µsec/3.0V)

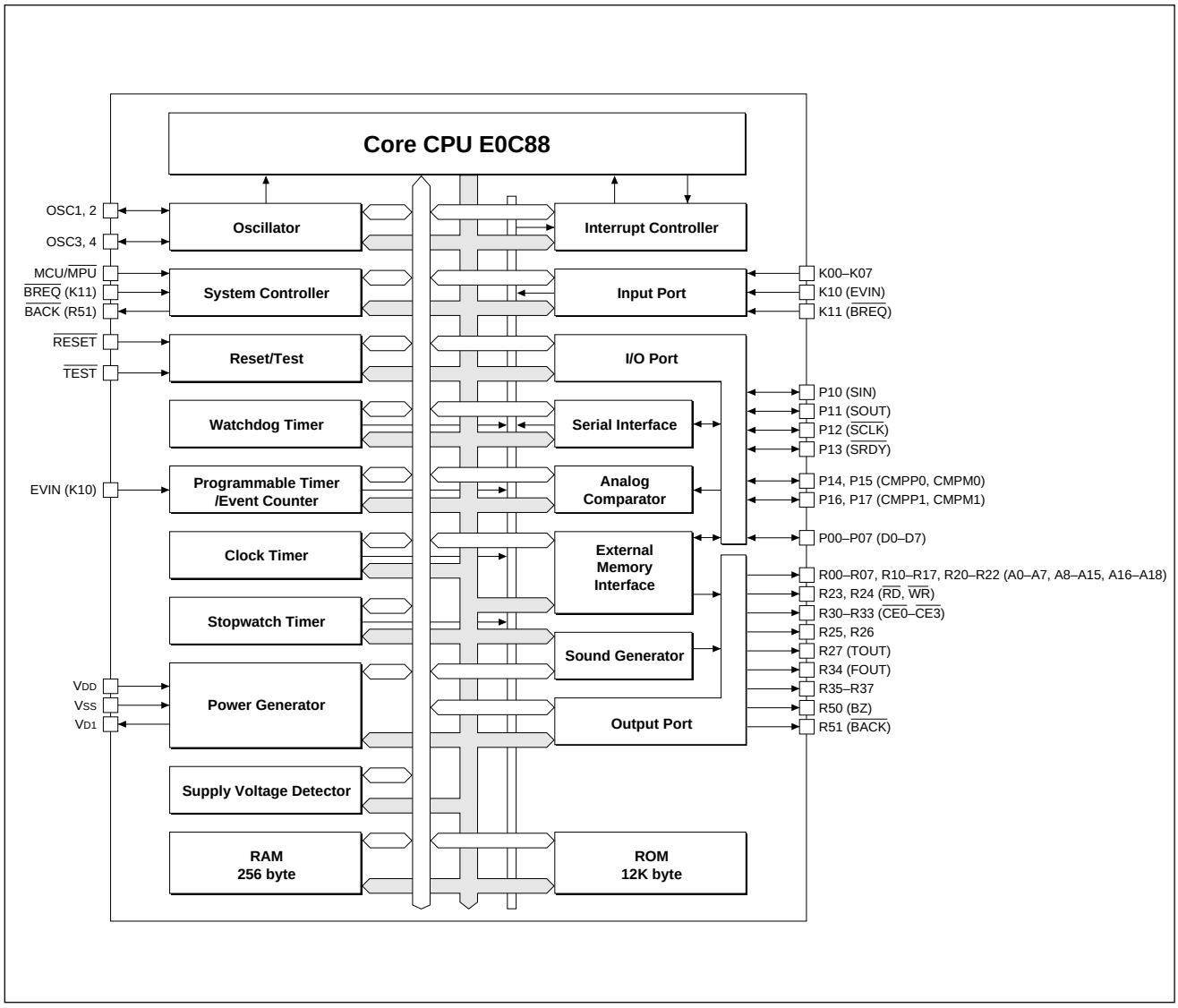
■ DESCRIPTION

The E0C88112 is a CMOS 8-bit microcomputer composed of a CMOS 8-bit core CPU, ROM, RAM, I/O, serial interface, timer and event counter. Systems with a large-sized memory and middle-scale display, such as a high performance data bank or an electronic dictionary, can be realized using the E0C88112 with the SED15 Series LCD driver, RAM and ROM.

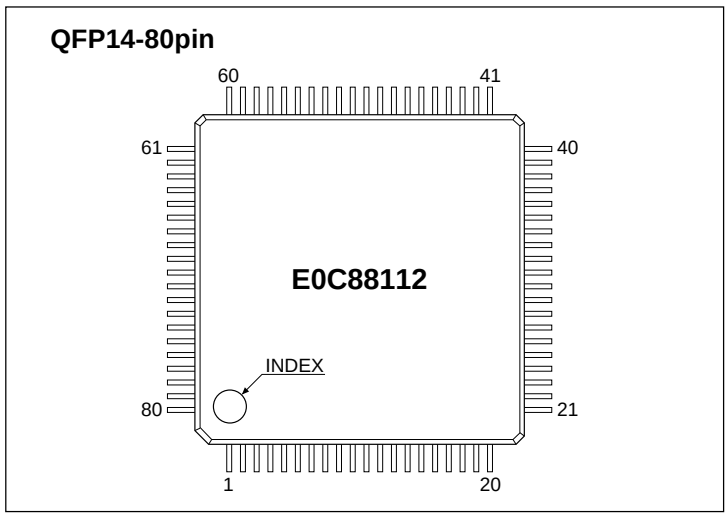
■ FEATURES

- CMOS LSI 8-bit parallel processing
- Clock ..... Twin clock system Low-speed clock : 32.768kHz
  High-speed clock : 4.2MHz (3V) / 8MHz (5V)
- Instruction execution time ..... 0.48µsec (Min.)
- Multiplication and division instructions included
- ROM capacity ..... 12K × 8 bits
- RAM capacity ..... 256 × 8 bits (Working RAM)
- Addressing ..... 512K-byte (19 bits)
  Address bus: 19-bit ROM addressing, 19-bit RAM addressing
  (Can be used as general output ports when the address bus is not used.)
  Data bus : 8 bits
  (Can be used as general I/O ports when the data bus is not used.)
  $\overline{CE}$ signal : 4 bits
  $\overline{WR}$ signal : 1 bit
  $\overline{RD}$ signal : 1 bit
  (Can be used as general output ports when the control signals are not used.)
- I/O port ..... Input only : 10 bits ($\overline{BREQ}$ and EVIN are available by software)
  Output only : 9 bits (BZ, CL, FR, FOUT, TOUT and $\overline{BACK}$ are available by software)
  Bidirectional I/O : 8 bits ($\overline{SRDY}$, $\overline{SCLK}$, SIN, SOUT, CMPP0, CMPM0, CMPP1 and CMPM1 are available by software)
- Serial interface ..... 1 channel (Clock synchronous or Asynchronous can be selected by software)
- Timer ..... 8-bit programmable timer/event counter : 2 channels
  (16-bit 1 channel timer is available)
  Time base counter (8 bits) : 1 channel
  Stopwatch timer (8 bits) : 1 channel
- Sound generator ..... 8 levels, with envelope, volume adjustment and 1 shot functions
- Watchdog timer ..... Generates NMI
- Supply voltage detection (SVD) circuit .... 16 levels (0.2V steps from 1.8V to 5.5V) can be detected
- Analog comparator ..... 2 channels built-in (Bidirectional I/O port is used as the input port)
- Interrupt ..... External : 2 systems (SCI, K inputs)
  Internal : 4 systems (W/D, PTM/EV, TMB, SW)
- Supply voltage ..... 1.8V to 5.5V
- Current consumption ..... SLEEP mode 200nA (3V) (Low power mode)
  HALT mode 1.0µA (32.768kHz/3V) (Low power mode)
  RUN mode 8.0µA (32.768kHz/3V) (Low power mode)
  1.8mA (4.2MHz/3V) (Normal mode)
- Package ..... QFP14-80pin (plastic), QFP15-100pin (plastic)

■ BLOCK DIAGRAM



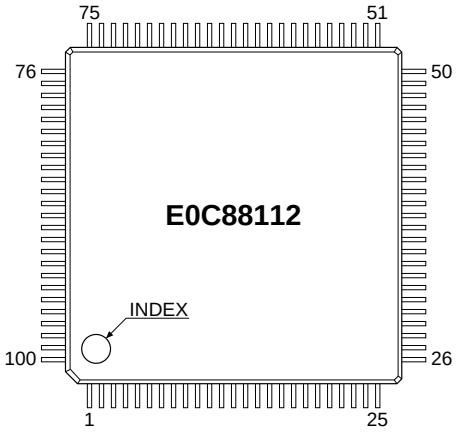
■ PIN CONFIGURATION



Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name
1	R00/A0	21	R24/$\overline{WR}$	41	R50/BZ	61	$\overline{RESET}$
2	R01/A1	22	R25	42	R51/$\overline{BACK}$	62	N.C.
3	R02/A2	23	R26	43	P17/CMPM1	63	K11/$\overline{BREQ}$
4	R03/A3	24	R27/TOUT	44	P16/CMPP1	64	K10/EVIN
5	R04/A4	25	R30/$\overline{CE0}$	45	P15/CMPM0	65	K07
6	R05/A5	26	R31/$\overline{CE1}$	46	P14/CMPP0	66	K06
7	R06/A6	27	R32/$\overline{CE2}$	47	P13/$\overline{SRDY}$	67	K05
8	R07/A7	28	R33/$\overline{CE3}$	48	P12/$\overline{SCLK}$	68	K04
9	R10/A8	29	R34/FOUT	49	P11/SOUT	69	K03
10	R11/A9	30	R35	50	P10/SIN	70	K02
11	R12/A10	31	R36	51	P07/D7	71	K01
12	R13/A11	32	R37	52	P06/D6	72	K00
13	R14/A12	33	*	53	P05/D5	73	MCU/$\overline{MPU}$
14	R15/A13	34	*	54	P04/D4	74	VDD
15	R16/A14	35	*	55	P03/D3	75	OSC4
16	R17/A15	36	*	56	P02/D2	76	OSC3
17	R20/A16	37	*	57	P01/D1	77	VD1
18	R21/A17	38	*	58	P00/D0	78	OSC2
19	R22/A18	39	*	59	N.C.	79	OSC1
20	R23/$\overline{RD}$	40	*	60	$\overline{TEST}$	80	VSS

* Pins No. 33 to 40 are the pads used for outgoing inspection of the IC. Do not connect anything to these pins.
N.C. : No Connection

QFP15-100pin



Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name
1	N.C.	26	N.C.	51	N.C.	76	N.C.
2	N.C.	27	N.C.	52	N.C.	77	N.C.
3	N.C.	28	R00/A0	53	R24/$\overline{WR}$	78	N.C.
4	$\overline{RESET}$	29	R01/A1	54	R25	79	R50/BZ
5	N.C.	30	R02/A2	55	R26	80	R51/$\overline{BACK}$
6	K11/$\overline{BREQ}$	31	R03/A3	56	R27/TOUT	81	P17/CMPM1
7	K10/EVIN	32	R04/A4	57	R30/$\overline{CE0}$	82	P16/CMPP1
8	K07	33	R05/A5	58	R31/$\overline{CE1}$	83	P15/CMPM0
9	K06	34	R06/A6	59	R32/$\overline{CE2}$	84	P14/CMPP0
10	K05	35	R07/A7	60	R33/$\overline{CE3}$	85	P13/$\overline{SRDY}$
11	K04	36	R10/A8	61	R34/FOUT	86	P12/$\overline{SCLK}$
12	K03	37	R11/A9	62	R35	87	P11/SOUT
13	K02	38	R12/A10	63	R36	88	P10/SIN
14	K01	39	R13/A11	64	R37	89	P07/D7
15	K00	40	R14/A12	65	*	90	P06/D6
16	MCU/$\overline{MPU}$	41	R15/A13	66	*	91	P05/D5
17	V_{DD}	42	R16/A14	67	*	92	P04/D4
18	OSC4	43	R17/A15	68	*	93	P03/D3
19	OSC3	44	R20/A16	69	*	94	P02/D2
20	V_{D1}	45	R21/A17	70	*	95	P01/D1
21	OSC2	46	R22/A18	71	*	96	P00/D0
22	OSC1	47	R23/$\overline{RD}$	72	*	97	N.C.
23	V_{SS}	48	N.C.	73	N.C.	98	$\overline{TEST}$
24	N.C.	49	N.C.	74	N.C.	99	N.C.
25	N.C.	50	N.C.	75	N.C.	100	N.C.

* Pins No. 65 to 72 are the pads used for outgoing inspection of the IC. Do not connect anything to these pins.
N.C. : No Connection

■ PIN DESCRIPTION

Pin name	Pin No.		In/Out	Function
	QFP14-80	QFP15-100		
V_{DD}	74	17	–	Power supply (+) terminal
V_{SS}	80	23	–	Power supply (GND) terminal
V_{D1}	77	20	–	Regulated voltage output terminal for oscillators
OSC1	79	22	I	OSC1 oscillation input terminal (crystal oscillation/CR oscillation/external clock input, mask option)
OSC2	78	21	O	OSC1 oscillation output terminal
OSC3	76	19	I	OSC3 oscillation input terminal (crystal/ceramic/CR oscillation/external clock input, mask option)
OSC4	75	18	O	OSC3 oscillation output terminal
MCU/$\overline{MPU}$	73	16	I	Terminal for setting MCU or MPU modes
K00–K07	72–65	15–8	I	Input port (K00–K07) terminal
K10/EVIN	64	7	I	Input port (K10) terminal or event counter external clock (EVIN) input terminal
K11/$\overline{BREQ}$	63	6	I	Input port (K11) terminal or bus request signal ($\overline{BREQ}$) input terminal
R00–R07/A0–A7	1–8	28–35	O	Output port (R00–R07) terminals or address bus (A0–A7)
R10–R17/A8–A15	9–16	36–43	O	Output port (R10–R17) terminals or address bus (A8–A15)
R20–R22/A16–A18	17–19	44–46	O	Output port (R20–R22) terminals or address bus (A16–A18)
R23/$\overline{RD}$	20	47	O	Output port (R23) terminal or read signal ($\overline{RD}$) output terminal
R24/$\overline{WR}$	21	53	O	Output port (R24) terminal or write signal ($\overline{WR}$) output terminal
R25	22	54	O	Output port (R25) terminal
R26	23	55	O	Output port (R26) terminal
R27/TOUT	24	56	O	Output port (R27) terminal or programmable timer underflow signal (TOUT) output terminal
R30–R33/$\overline{CE0}$–$\overline{CE3}$	25–28	57–60	O	Output port (R30–R33) terminals or chip enable ($\overline{CE0}$–$\overline{CE3}$) output terminals
R34/FOUT	29	61	O	Output port (R34) terminal or clock (FOUT) output terminal
R35–R37	30–32	62–64	O	Output port (R35–R37) terminal
R50/BZ	41	79	O	Output port (R50) terminal or buzzer (BZ) output terminal
R51/$\overline{BACK}$	42	80	O	Output port (R51) terminal or bus acknowledge signal ($\overline{BACK}$) output terminal
P00–P07/D0–D7	58–51	96–89	I/O	I/O port (P00–P07) terminals or data bus (D0–D7)
P10/SIN	50	88	I/O	I/O port (P10) terminal or serial I/F data input (SIN) terminal
P11/SOUT	49	87	I/O	I/O port (P11) terminal or serial I/F data output (SOUT) terminal
P12/$\overline{SCLK}$	48	86	I/O	I/O port (P12) terminal or serial I/F clock ($\overline{SCLK}$) I/O terminal
P13/$\overline{SRDY}$	47	85	I/O	I/O port (P13) terminal or serial I/F ready signal ($\overline{SRDY}$) output terminal
P14/CMPP0	46	84	I/O	I/O port (P14) terminal or comparator 0 non-inverted input terminal
P15/CMPM0	45	83	I/O	I/O port (P15) terminal or comparator 0 inverted input terminal
P16/CMPP1	44	82	I/O	I/O port (P16) terminal or comparator 1 non-inverted input terminal
P17/CMPM1	43	81	I/O	I/O port (P17) terminal or comparator 1 inverted input terminal
$\overline{RESET}$	61	4	I	Initial reset input terminal
$\overline{TEST}$ *	60	98	I	Test input terminal

* $\overline{TEST}$ is the terminal used for outgoing inspection of the IC. For normal operation be sure it is connected to V_{DD}.

■ ELECTRICAL CHARACTERISTICS

● Absolute Maximum Ratings

(V_{SS} = 0V)

Rating	Symbol	Condition	Value	Unit	Note
Power voltage	V_{DD}		-0.3 to +7.0	V	
Input voltage	V_I		-0.3 to V_{DD} + 0.3	V	
Output voltage	V_O		-0.3 to V_{DD} + 0.3	V	1
High level output current	I_{OH}	1 terminal	-5	mA	
		Total of all terminals	-20	mA	
Low level output current	I_{OL}	1 terminal	5	mA	
		Total of all terminals	20	mA	
Permitted loss	P_D		200	mW	2
Operating temperature	Topr		-40 to +85	°C	
Storage temperature	Tstg		-65 to +150	°C	

Note) 1 Case that to Nch open drain output by the mask option is included.
2 In case of plastic package.

● Recommended Operating Conditions

(V_{SS} = 0V, Ta = -40 to 85°C)

Condition	Symbol	Remark	Min.	Typ.	Max.	Unit	Note
Operating power voltage (Normal mode)	V_{DD}		2.4		5.5	V	
Operating power voltage (Low power mode)	V_{DD}		1.8		3.5	V	
Operating power voltage (High speed mode)	V_{DD}		3.5		5.5	V	
Operating frequency (Normal mode)	f_{OSC1}	V_{DD} = 2.4 to 5.5V	30	32.768	50	kHz	3
	f_{OSC3}		0.03		4.2	MHz	3
Operating frequency (Low power mode)	f_{OSC1}	V_{DD} = 1.8 to 3.5V	30	32.768	50	kHz	3
Operating frequency (High speed mode)	f_{OSC1}	V_{DD} = 3.5 to 5.5V	30	32.768	50	kHz	3
	f_{OSC3}		0.03		8.2	MHz	3
Capacitor between V_{D1} and V_{SS}	C1			0.1		µF	

Note) 3 When an external clock is input from the OSC1 terminal by the mask option, do not connect anything to the OSC2 terminal, and when an external clock is input from the OSC3 terminal, do not connect to the OSC4 terminal.

● DC Characteristics

(Unless otherwise specified: V_{DD} = 1.8 to 5.5V, V_{SS} = 0V, Ta = -40 to 85°C)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
High level input voltage (1)	V_{IH1}	Kxx, Pxx, MCU/$\overline{MPU}$	0.8V_{DD}		V_{DD}	V	
Low level input voltage (1)	V_{IL1}	Kxx, Pxx, MCU/$\overline{MPU}$	0		0.2V_{DD}	V	
High level input voltage (2) (Normal mode)	V_{IH2}	OSC1, OSC3	1.6		V_{DD}	V	4
High level input voltage (2) (Low power mode)	V_{IH2}	OSC1	1.0		V_{DD}	V	4
High level input voltage (2) (High speed mode)	V_{IH2}	OSC1, OSC3	2.4		V_{DD}	V	4
Low level input voltage (2) (Normal mode)	V_{IL2}	OSC1, OSC3	0		0.6	V	4
Low level input voltage (2) (Low power mode)	V_{IL2}	OSC1	0		0.3	V	4
Low level input voltage (2) (High speed mode)	V_{IL2}	OSC1, OSC3	0		0.9	V	4
High level schmitt input voltage	V_{T+}	$\overline{RESET}$	0.5V_{DD}		0.9V_{DD}	V	
Low level schmitt input voltage	V_{T-}	$\overline{RESET}$	0.1V_{DD}		0.5V_{DD}	V	
High level output current	I_{OH}	Pxx, Rxx, V_{OH} = 0.9V_{DD}			-0.5	mA	
Low level output current	I_{OL}	Pxx, Rxx, V_{OL} = 0.1V_{DD}	0.5			mA	
Input leak current	I_{LI}	Kxx, Pxx, $\overline{RESET}$, MCU/$\overline{MPU}$	-1		1	µA	
Output leak current	I_{LO}	Pxx, Rxx	-1		1	µA	
Input pull-up resistance	R_{IN}	Kxx, Pxx, $\overline{RESET}$, MCU/$\overline{MPU}$	100		500	kΩ	5
Input terminal capacitance	C_{IN}	Kxx, Pxx, V_{IN} = 0 V, f = 1MHz, Ta = 25°C			15	pF	

Note) 4 When external clock is selected by mask option.
5 When addition of pull-up resistor is selected by mask option.

● SVD Circuit

(Unless otherwise specified: V_{DD} = 1.8 to 5.5V, V_{SS} = 0V, Ta = 25°C)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
SVD voltage	V_{SVD}	Level 1 → Level 0	Typ×0.92	1.82	Typ×1.08	V	
		Level 2 → Level 1		2.00		V	
		Level 3 → Level 2		2.18		V	
		Level 4 → Level 3		2.36		V	
		Level 5 → Level 4		2.54		V	
		Level 6 → Level 5		2.72		V	
		Level 7 → Level 6		2.90		V	
		Level 8 → Level 7		3.08		V	
		Level 9 → Level 8		3.26		V	
		Level 10 → Level 9	Typ×0.88	3.45	Typ×1.12	V	
		Level 11 → Level 10		3.65		V	
		Level 12 → Level 11		3.85		V	
		Level 13 → Level 12		4.05		V	
		Level 14 → Level 13		4.25		V	
		Level 15 → Level 14		4.50		V	

● Analog Comparator Circuit

(Unless otherwise specified: V_{DD} = 1.8 to 5.5V, V_{SS} = 0V, Ta = 25°C)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Analog comparator operating voltage input range	V_{CMIP}	Non-inverted input (CMPP)	0.7		V_{DD} - 0.7	V	6
	V_{CMIM}	Inverted input (CMPM)	0.7		V_{DD} - 0.7	V	6
Analog comparator offset voltage	V_{CMOF}	V_{CMIP} = 0.7V to V_{DD} - 0.7V V_{CMIM} = 0.7V to V_{DD} - 0.7V			20	mV	6
Analog comparator stability time	t_{CMP1}				1	mS	7
Analog comparator response time	t_{CMP2}	V_{CMIP} = 0.7V to V_{DD} - 0.7V V_{CMIM} = 0.7V to V_{DD} - 0.7V V_{CMIP} = V_{CMIM} ± 0.025V			2	mS	6 8

Note) 6 When "without pull-up resistor" (comparator input terminal) is selected by mask option.
7 Stability time is the time from turning the circuit ON until the circuit is stabilized.
8 Response time is the time that the output result responds to the input signal.

● Current Consumption

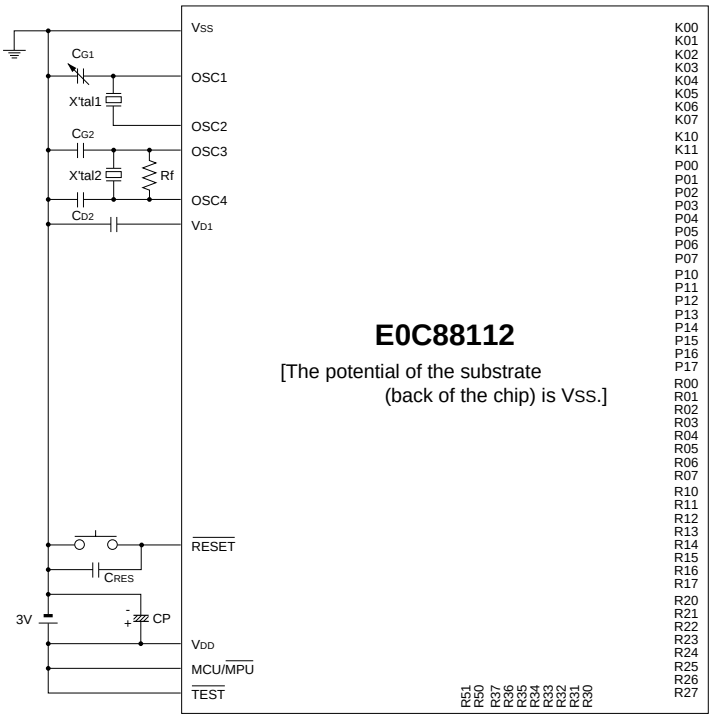
(Unless otherwise specified: V_{DD} = Within the operating voltage in each operating mode, V_{SS} = 0V, Ta = 25°C,
OSC1 = 32.768kHz crystal oscillation, C_G = 10pF, OSC3 = External clock input, Non heavy load protection mode, C1 = 0.1µF)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Power current (Normal mode)	I_{DD1}	In SLEEP status *1		0.3	1	µA	
	I_{DD2}	In HALT status *2		2	5	µA	
	I_{DD3}	CPU is in operating (32.768kHz) *3		14	18	µA	
	I_{DD4}	CPU is in operating (1MHz) *4		0.45	0.60	mA	
	I_{HVL}	In heavy load protection mode		25	50	µA	9
Power current (Low power mode)	I_{DD1}	In SLEEP status *1		0.2	1	µA	
	I_{DD2}	In HALT status *2		1	5	µA	
	I_{DD3}	CPU is in operating (32.768kHz) *3		8	12	µA	
	I_{HVL}	In heavy load protection mode		15	30	µA	9
Power current (High speed mode)	I_{DD1}	In SLEEP status *1		1	3	µA	
	I_{DD2}	In HALT status *2		5	10	µA	
	I_{DD3}	CPU is in operating (32.768kHz) *3		24	30	µA	
	I_{DD4}	CPU is in operating (1MHz) *4		0.70	1.00	mA	
	I_{HVL}	In heavy load protection mode		35	70	µA	9
SVD circuit current	I_{SVDN}	V_{DD} = 3.0V		30	60	µA	10
	I_{SVDH}	In heavy load protection mode		25	75	µA	9
Analog comparator circuit current	I_{CMP1}	CMPXDT = "1"		40	100	µA	
	I_{CMP2}	CMPXDT = "0"		4	10	µA	
OSC1 CR oscillation current	I_{CR1}			20	50	µA	11

*1 OSC1: Stop, OSC3: Stop, CPU, ROM, RAM: SLEEP status, Clock timer: Stop, Others: Stop status
*2 OSC1: Oscillating, OSC3: Stop, CPU, ROM, RAM: HALT status, Clock timer: Operating, Others: Stop status
*3 OSC1: Oscillating, OSC3: Stop, CPU, ROM, RAM: Operating in 32.768kHz, Clock timer: Operating, Others: Stop status
*4 OSC1: Oscillating, OSC3: Oscillating, CPU, ROM, RAM: Operating in 1MHz, Clock timer: Operating, Others: Stop status

Note) 9 It is the value of current which flows in the heavy load protection circuit when in the heavy load protection mode (OSC3 ON or buzzer ON).
10 The value in x V can be found by the following expression:
I_{SVDN} (V_{DD} = x V) = (x × 20) - 30 (Typ. value), I_{SVDN} (V_{DD} = x V) = (x × 30) - 30 (Max. value)
11 When OSC1 CR oscillation circuit is selected by the mask option.

■ BASIC EXTERNAL CONNECTION DIAGRAM

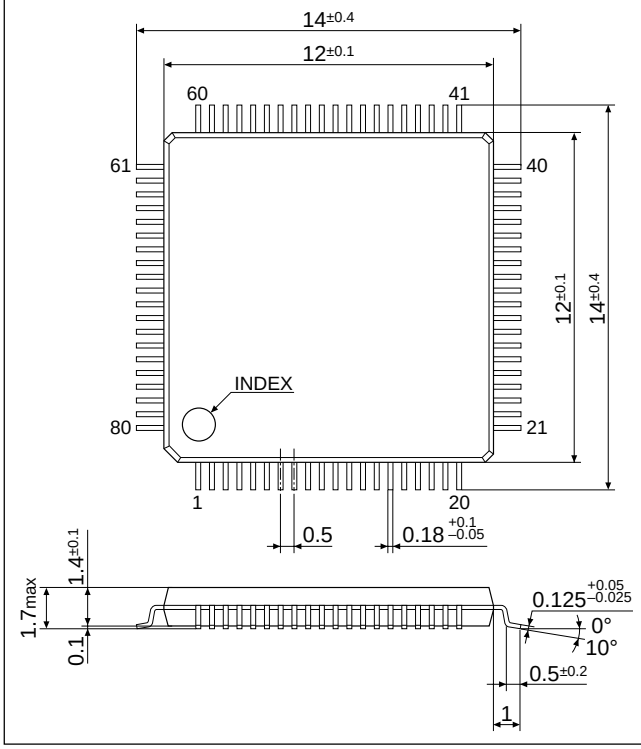


Recommended values for external parts

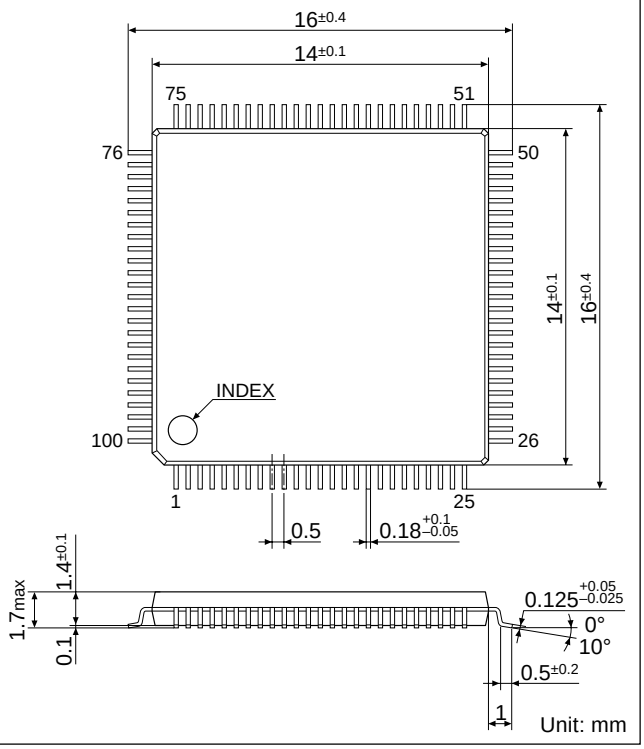
Symbol	Name	Recommended value
X'tal1	Crystal oscillator	32.768kHz, CI(Max.) = 35kΩ
X'tal2	Crystal oscillator	4.2MHz
Rf	Feedback resistor	1MΩ
CG1	Trimmer capacitor	5–25pF
CG2	Gate capacitor	15pF
CD2	Drain capacitor	15pF
CP	Capacitor for power supply	3.3µF
CRES	Capacitor for $\overline{\text{RESET}}$ terminal	0.47µF

■ PACKAGE DIMENSIONS

Plastic QFP14-80pin



Plastic QFP15-100pin



Unit: mm

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